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Reflection Amplifier with Phase Control Suitable for Active Reconfigurable Intelligent Surfaces



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Abstract In this work, an elementary circuit block suitable for Active Reconfigurable Intelligent Surface (ARIS) implementation, at 5.8 GHz, is presented. The chain is composed of a reflection amplifier cascaded to a phase shifter. The block exhibits a variable gain in the 0 to 15 dB range, and a maximum phase shift of 260°,

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by varying the amplifier supply and phase shifter control voltages in the 2.5 V to 3.5 V and 0 V to 5 V ranges, respectively. The maximum power consumption of the cascade is within 52.5 mW. This work is the result of a collaboration between the University of Florence and the University of Perugia, in the frame of the PRIN 2022 SIPT-VARIS project.

Keywords Internet of Things · Negative differential resistance · Phase shifter · Reconfigurable intelligent surfaces · Reflection amplifier

1 Introduction

Nowadays, wireless communications are widely spread and commonly implemented in many application scenarios, such as the Internet of Things (IoT). In this scenario, Reconfigurable Intelligent Surfaces (RISs) have been proposed to improve the quality of these services, [1, 7, 10]. The main advantage of RISs is the ability to backscatter the incident radio wave in arbitrary directions; i.e., allowing to circumvent obstacles like walls, as reported in Fig. 1. Several other use-cases involving RISs are presented in [1]. Although the role of an RIS is well understood in communication theory, the optimal implementation of this device remains a matter of study. Nowadays, RIS architectures are split into two main categories, active and passive, considering the presence or absence of power gain in the backscattering process, [11]. In particular, taking into account Active RISs (ARISs), the presence of gain in the backscattered wave allows for dealing with multiplicative fading issues, which otherwise would affect the passive RIS case, [10]. This effect gives rise to a significant signal attenuation after multiple signal backscatterings, due to the path loss contribution, which is multiplicative instead of additive as in a point-to-point radio link.

A RIS is composed of an antenna array, where each element is driven by a Phase Shifter (PS) and possibly an amplifier, the latter used only within the ARIS case, [11]. An example of passive RIS is presented in [8]. An ARIS element can be implemented with two different approaches, as reported in Fig. 2. The architecture shown in

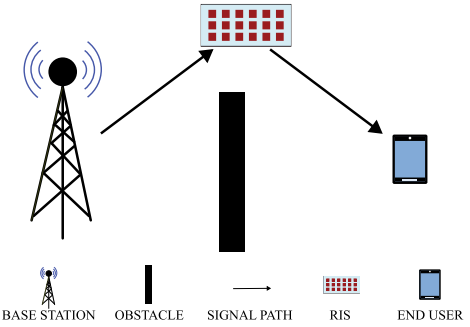
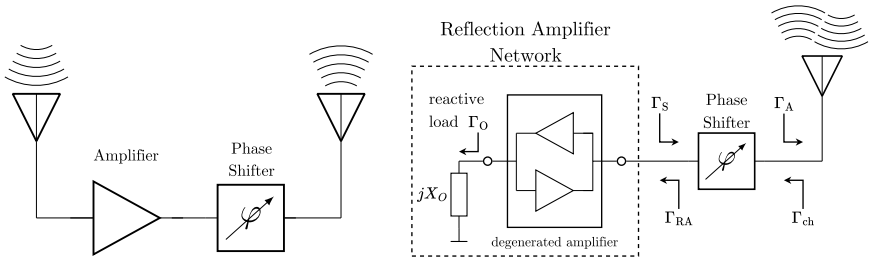


Fig. 1 Conceptual example of RIS deployment in a typical use-case



(a) Dual antenna approach (b) Single antenna approach

Fig. 2 Typical ARIS channel implementation approaches

Fig. 2a considers a chain composed of a receiving antenna, along with an amplifier and a PS, followed in the end by a transmitting antenna, [6]. On the other hand, the second approach reported in Fig. 2b includes only a single antenna, with a Reflection Amplifier (RA) and a PS between them. The latter is the most innovative approach, e.g., the one described in [9], where the antenna is used in both directions Tx and Rx, allowing a significant reduction in physical dimensions and complexity of the RIS, a major concern in an eventual monolithic microwave integrated circuit (MMIC) implementation.

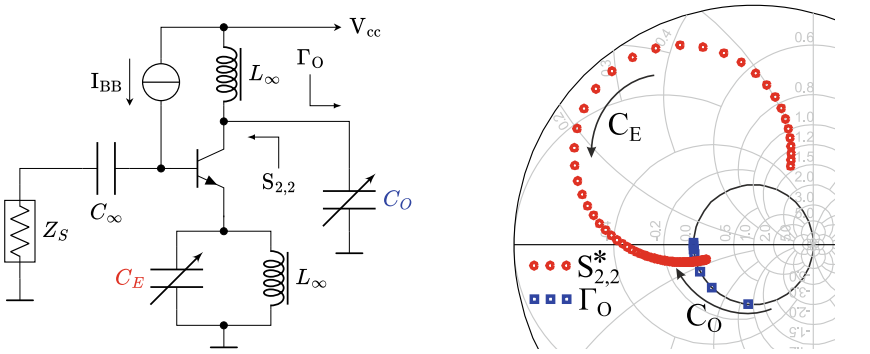
In this paper, we illustrate the design and characterization steps, covering the electronics suitable for a prototype of a single-antenna ARIS channel. The latter has been implemented using widely available commercial off-the-shelf (COTS) components, aimed at a working frequency of 5.8 GHz.

2 Design and Characterization

2.1 ARIS Element Design

The first topic to be described is the RA implementation. The latter can be modeled as an active, single-port network (Fig. 2b), where the input reflection coefficient (Γ_{RA}) has a magnitude greater than unity, to reflect an amplified replica of the incident signal. As a consequence, for an RA, the gain is the magnitude of its reflection coefficient ($|\Gamma_{RA}|$). The proposed RA architecture is based on a variation of the common-emitter BJT or HBT amplifier; the main design principles followed in this work are reported in [3].

Taking into account the simplified schematic in Fig. 3a, the design of the RA requires obtaining a conditionally-stable amplifier, starting from the model of a linear, two-port network, expressed by an $\underline{\underline{S}}$ matrix. The conditional stability is achieved thanks to a capacitive emitter degeneration, which causes a negative real part in the small-signal input impedance, looking into the base, [3, 4]. The degenerating capacitor C_E is tuned to achieve a stability factor $k < 1$, leading to $|S_{2,2}| > 1$ in the



(a) Core schematic of an HBT-based RA. (b) $S^*_{2,2} - \Gamma_O$ contours at 5.8 GHz.

Fig. 3 Graphical design procedure for an RA: in **a** a generic schematic, highlighting the main tunable components, is shown. The C_∞ and L_∞ components represent DC-blocks and DC-feeds, respectively. In **b** are reported the trajectories of: $S^*_{2,2}$, resulting from C_E tuning, and Γ_O, resulting from C_O tuning

desired bandwidth. This process is reported in Fig. 3b, where the $S^*_{2,2}$ response is shown while tuning C_E, at the 5.8 GHz working frequency.

After that, it is possible to complete the RA design by terminating the output, port 2, with a proper reactive load (Γ_0) chosen to have $|\Gamma_{RA}| \gg 1$.

$$\Gamma_{RA} = S_{1,1} + \frac{S_{1,2}\, S_{2,1}\, \Gamma_O}{1 - S_{2,2}\, \Gamma_O}\,. \tag{1}$$

The trajectory of Γ_O, at the working frequency, is also shown in Fig. 3b while tuning the C_O output capacitor. By graphically choosing the $S^*_{2,2}$–Γ_O intercept point, it is possible to tune peak gain and frequency, as explained in (1), obviously avoiding the singularity $|S_{2,2}\, \Gamma_O| = 1$. In this singularity point, the gain diverges asymptotically to infinity; this singularity is the condition for, theoretically, maximizing the gain; however, this point must be avoided or the amplifier will oscillate.

In the author's opinion, a closed-form relation between the degeneration and output loads vs peak gain and frequency is not available at this time, so the circuit was fine-tuned with the help of commercial electromagnetic CAD software.

The RA has been designed for the Industrial, Scientific and Medical (ISM) band, at a working frequency of 5.8 GHz. The circuit is based on a single transistor, emitter-degenerated amplifier, with the output port terminated in a reactive load, as in Fig. 2b. The detailed schematic is reported in Fig. 4, where the red box highlights the RA part. The circuit employs a BFP650 transistor (Si-Ge HBT from Infineon) and is realized on a FR408 substrate, cf. (1) in Fig. 5b.

In this RA, the C_E–L_E group was chosen as a degenerating emitter load. In particular, the capacitor is required as explained previously, while the inductor was added to allow biasing the HBT without the need to add a parallel resistor, which

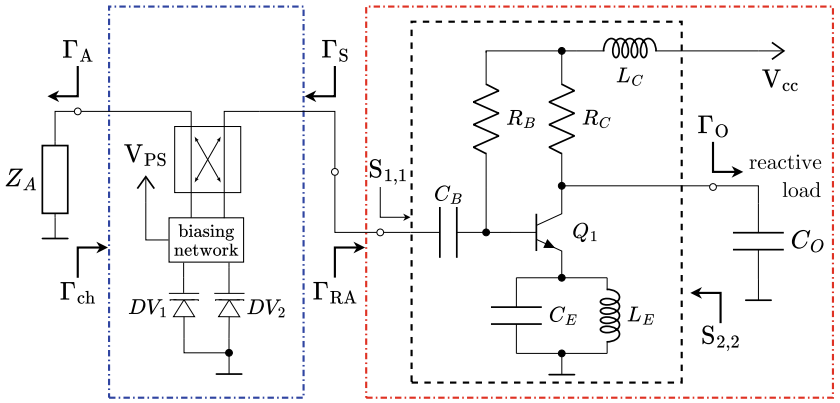
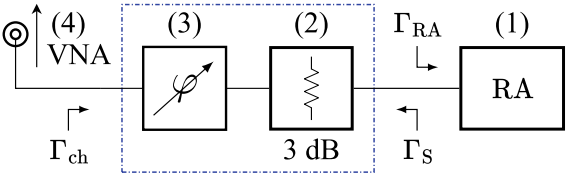
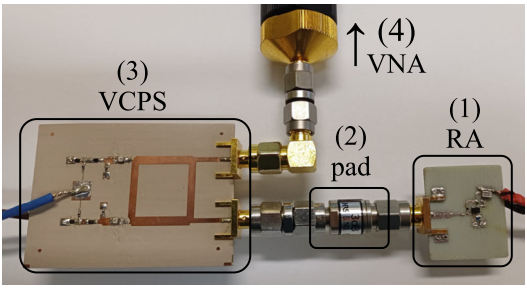


Fig. 4 Schematic diagram of the complete RA (right) and PS block diagram (left), within a single ARIS channel. Employed components in the RA: C_B=0.5pF, C_E=0.4pF, C_O=0.7pF, L_E=2nH, L_C=2nH, R_B=28 kΩ, R_C=80 Ω, Q_1=BFP650, DV_1, DV_2=SMV1249

Fig. 5 Illustration of the DUT and the experimental setup. The phase-shifting chain, blue box in (**a**), includes a 3 dB matching pad, whose contribution is included in the measured Γ_{ch} and Γ_S results



(a) Block diagram.



(b) Photo of the setup.

would have degraded the amplifier's noise figure, even if the latter was not analyzed in the proposed design procedure. In this circuit, gain control has been implemented by varying the transistor's supply voltage (V_{cc}); this effect can be explained by the transistor's transconductance relation with the collector current, since the base supply is also bound to the collector. A similar variable-gain architecture, based on field-effect (HEMT) transistors, was also investigated in [2]. In this work, the transistor is biased with a maximum V_{cc} of 3.5 V and a maximum current of 15 mA, leading to a maximum power consumption of approximately 52.5mW.

The PS is based on a conventional hybrid coupler architecture, [5], and it is realized on a separate PCB that employs the CER10 ceramic substrate, cf. (3) in Fig. 5b. In this architecture, SMV1249 varactor diodes from Skyworks are used to voltage-control the phase shift with V_{PS} signal. The PS conceptual schematic is reported in Fig. 4, highlighted by the blue box.

Particular attention has been paid to stability to avoid oscillations due to the RA, since $|\Gamma_{RA}| > 1$. In addition, a conditional stability design criterion was used, depending on the reflection coefficient seen by the RA's input (Γ_S). The network stability, according to [4], is guaranteed if:

$$1 - \Gamma_S \cdot \Gamma_{RA}, \quad \text{has no right-half plane zeroes.} \tag{2}$$

The (2) can be plotted on a polar plot to evaluate the RA circuit stability thanks to the Nyquist criterion; this is necessary in the proposed application mainly because Γ_S is not a constant value, but varies with the PS control signal, so every voltage value should theoretically be analyzed. This point is well explained in the next Sect. 2.2, cf. Fig. 10, considering also measured results.

2.2 ARIS Chain Characterization

The RA and PS blocks were individually measured before characterizing the complete ARIS channel. All measurements were performed by means of a VNA.

The RA was characterized by measuring the reflective power gain; in Fig. 6, a comparison between the simulated and measured gain magnitude is reported considering a single transistor supply bias (V_{cc} = 3V). From Fig. 6 the working frequency is slightly upper-shifted in the measured circuit, about 5.95 GHz with respect to 5.85 GHz of the simulated circuit; however there is a great accordance between the two plots, in particular concerning the bandwidth and peak gain measurements, i.e. the latter approaching 17 dB. These results highlight the high accuracy of the simulated circuit and the employed components' models.

The PS was characterized by its phase shift and insertion loss performances, at 5.8 GHz, by varying the V_{PS} control signal in the full range allowed by the varactor diodes' breakdown voltage. In the experimental setup used, a 3 dB matching attenuator has been inserted between the RA and the PS, as visible in Fig. 5, to avoid influencing RA performances with variations of Γ_S due to V_{PS} signal. The RA was designed with a constant source impedance of 50 Ω, while in operative conditions the source impedance changes due to phase control. The loss contribution added by the attenuator is considered part of the PS block. PS Measurement results are reported in Fig. 7. In the proposed design, the PS was characterized with a V_{PS} spacing in the 0 to 5 V range, leading to a maximum phase shift of 130° and a maximum insertion loss of 6 dB. The latter value considers the signal flowing in a single direction; therefore, the total loss is doubled in the proposed ARIS channel application.

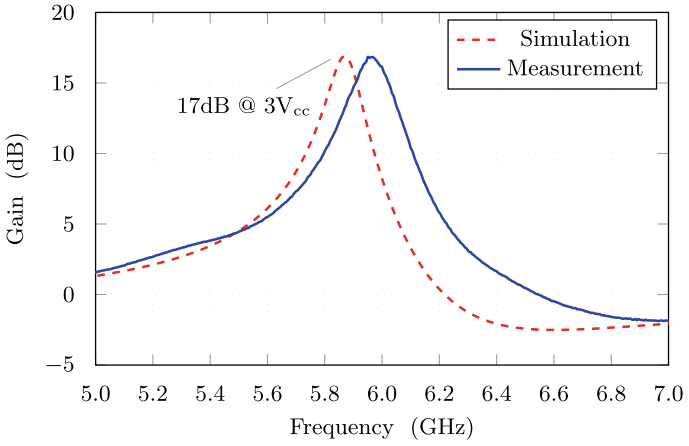


Fig. 6 Simulated and measured reflective gain performances of the RA, terminated on a 50 Ω load (cf. Z_S in Fig. 3a)

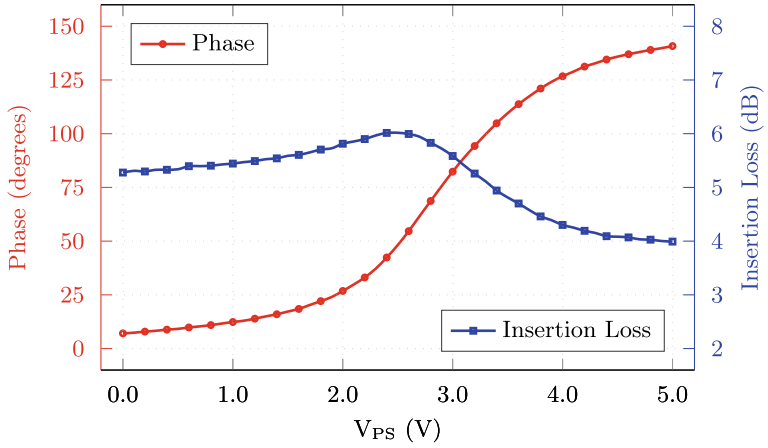


Fig. 7 Measured performances of the experimental cascade, composed of the PS and the 3 dB matching pad (blue box in Fig 5a)

In the second part, the complete RA and PS chain has been experimentally characterized at 5.8 GHz; the setup is shown in Fig. 5.
Performances of the chain evaluated at 5.8 GHz, related to Γ_{ch}: power gain ($|\Gamma_{ch}|_{dB}$) and absolute phase shift ($\angle\Gamma_{ch}$), are reported in Fig. 8. The complete chain's gain has been measured with a variable V_{cc} in the 2.5 to 3.5 V range, leading to a variable gain in the 0 to 15 dB range, reported in the top contour of Fig. 8. The total phase shift is shown in the bottom contour in Fig. 8; it has been measured with V_{PS} spacing in the 0 to 5 V range, same as the PS, achieving a maximum total phase shift of 260°, double of the PS alone.

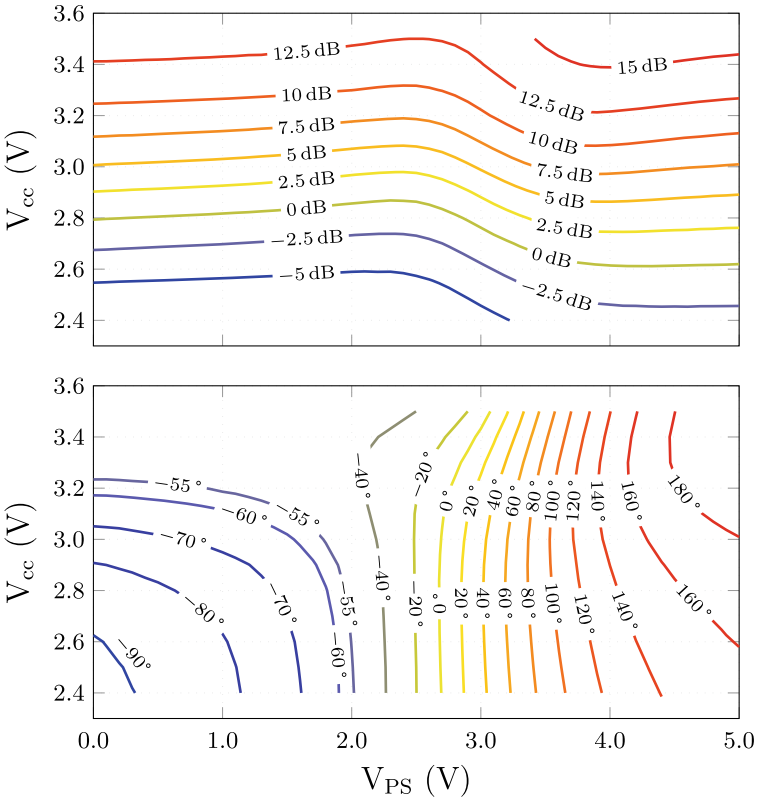


Fig. 8 In the top, measured magnitude of gain ($|\Gamma_{ch}|_{dB}$); in the bottom, absolute phase shift ($\angle\Gamma_{ch}$) of the complete ARIS channel (cf. Γ_{ch} in Fig. 5). Data refer to the constant 5.8 GHz working frequency

In Fig. 9, the Γ_{ch} constellation obtained using a part of the entire phase excursion is shown; the latter has been limited in the region where the phase shift control less affects the RA performances, by looking at Fig. 8 contour plots. This data considers the whole chain, and therefore, the forward-backward signal flow is accounted for. The phase shift segment used for the constellation is the one for V_{PS} in the 2.2V to 4.2V range, where a total phase shift of 180° is obtained. The latter is sufficient for an ARIS application. In the constellation plot, the phase shift is referenced at 0°, since in a phased array system, the relative phase shift is more important than the absolute one.

The measurement results in Figs. 8, 9 and 10 include the loss contribution added by the matching attenuator. The latter here is necessary because of the mentioned Γ_S phase fluctuations. However, the attenuator is not required for stability, since (2) was already satisfied without it.

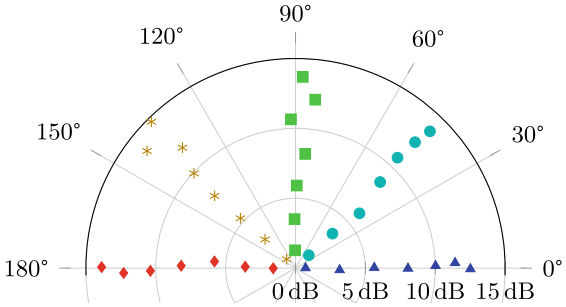
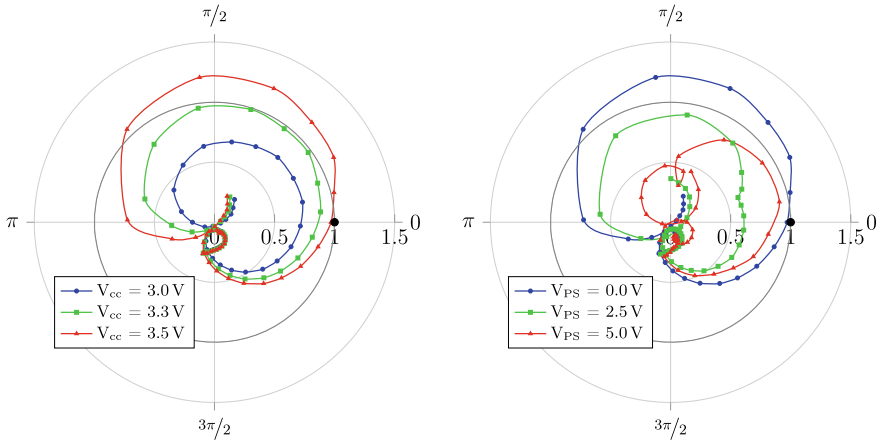


Fig. 9 Constellation plot of measured Γ_{ch}, at the constant 5.8 GHz working frequency. The gain excursion is limited in the 0 to 15 dB range and the relative phase shift is limited in the 0° to 180° range, both from Fig. 8 data



(a) Nyquist plot, with $V_{PS} = 0\,V$ (b) Nyquist plot, with $V_{cc} = 3.5\,V$

Fig. 10 Nyquist plots built with the measured ($\Gamma_S\,\Gamma_{RA}$) function, in the 5 GHz to 7GHz range. The Γ_S is that of the DUT chain (Fig. 5a), with the 3 dB matching pad inserted

3 Conclusion

In this work, an electronic block suitable for Active RIS has been designed and characterized for the 5.8 GHz working frequency. The chain exhibits a gain control span of 15 dB and a maximum relative phase shift of 260°. The latter was reduced to 180°, choosing a phase shifter control voltage range in which the RA negligibly affects the PS performances. The maximum power consumption is 52.5mW. All of these characteristics are very well suited for an ARIS channel implementation using the single-antenna approach.

Further developments will consider radiated measurements in a real environment, including a possible implementation of a multi-channel ARIS array in a monolithic

microwave integrated circuit (MMIC) process. Concerning these potential applications, the necessary study mainly aims at analyzing circuit stability due to channel-to-channel crosstalk, and at a low-power design necessary for further system miniaturization. Noise and large-signal performances are also topics worthy of future investigation.

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