# The Electrical, Thermal and Spatial Integration of a Converter in a Power Electronic Module

*Mark Benjamin Gerber*

# The Electrical, Thermal and Spatial Integration of a Converter in a Power Electronic Module

**PROEFSCHRIFT**

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*For my Father*
*Douglas Arthur Gerber*
*(1950 - 2001)*

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# Table of Contents

# LIST OF SYMBOLS

**Latin Letters**

| | | |
|---|---|---|
| $A$ | Area | [$m^2$] |
| $A$ | Dielectric area | [$m^2$] |
| $A$ | Width of a conductor | [m] |
| $A_c$ | Core area | [$m^2$] |
| $A_w$ | Winding window area | [$m^2$] |
| $B$ | Thickness of a conductor | [m] |
| $B$ | Magnetic flux density | [T] |
| $B_{ave}$ | Average magnetic flux density | [T] |
| $B_{max}$ | Peak magnetic flux density | [T] |
| $C$ | Capacitance | [F] |
| $C_{iss}$ | Gate source capacitance | [F] |
| $C_{14}$ | Bus capacitor on the 14V power net | [F] |
| $C_{42}$ | Bus capacitor on the 42V power net | [F] |
| $D$ | Duty cycle | |
| $d$ | Dielectric thickness | [m] |
| $d$ | Distance between centre of two conductors | [m] |
| $E$ | Energy | [J] |
| $E_{cycle}$ | Energy transferred per switching cycle | [J] |
| $E_{dissipated}$ | Energy dissipated | [J] |
| $E_{inductor}$ | Energy stored in an inductor | [J] |
| $E_{max\_norm}$ | Normalised maximum energy stored in a component | |
| $E_{max\_total}$ | Sum of all the energy stored in the passive components | [J] |
| $E_{max\_X}$ | Maximum energy in component $X$ | [J] |
| $E_{processed}$ | Energy processed | [J] |
| $E_{processed\_X}$ | Maximum energy processed by component $X$ | [J] |
| $f_s$ | Phase arm switching frequency | [Hz] |
| $h$ | The harmonic number | |

| | | |
|---|---|---|
| $h_c$ | Total inductor core height | [m] |
| $h_w$ | Inductor winding window height | [m] |
| $I$ | Average Current | [A] |
| $I_{diode}$ | Average diode current | [A] |
| $I_{DS\_SW}$ | Drain source current | [A] |
| $I_{gate\ driver}$ | Gate driver current | [A] |
| $I_L$ | Average inductor current | [A] |
| $I_{load}$ | Load current | [A] |
| $I_{RMS}$ | RMS current | [A] |
| $I_{RMS\_norm}$ | Normalised RMS current in a component | |
| $I_{rr}$ | Peak revere recovery current | [A] |
| $I_{X\_RMS}$ | RMS current in component $X$ | [A] |
| $I_{14}$ | Average current flowing into or out of the 14V terminals | [A] |
| $I_{42}$ | Average current flowing into or out of the 42V terminals | [A] |
| $i(t)$ | Current as a function of time | [A] |
| $i_{C42}(t)$ | Capacitor current as a function of time | [A] |
| $i_{C14}(t)$ | Capacitor current as a function of time | [A] |
| $i_L(t)$ | Inductor current as a function of time | [A] |
| $i_{L\_phaseY}(t)$ | Current in the inductor in phase $Y$ as a function of time | [A] |
| $i_{SWX\_phaseY}(t)$ | Current in MOSFET $X$ phase $Y$ as a function of time | [A] |
| $J$ | Current Density | [A/m$^2$] |
| $J_0$ | DC component of the current density | [A/m$^2$] |
| $J_h$ | The h$^{th}$ component of the current density Fourier series | [A/m$^2$] |
| $k$ | Thermal conductivity | [W/m·°C] |
| $k_c$ | Inductor core aspect ratio | |
| $k_{fill}$ | Winding window fill factor | |
| $k_{iso}$ | Thermal conductivity of winding isolation | [W/m·°C] |
| $k_{parallel}$ | Thermal conductivity parallel to winding plane | [W/m·°C] |
| $k_{perpendicular}$ | Thermal conductivity perpendicular to winding plane | [W/m·°C] |
| $k_w$ | Inductor winding window aspect ratio | |
| $k_{winding}$ | Thermal conductivity of winding conductor | [W/m·°C] |
| $L$ | Inductance | [H] |
| $L_0$ | Self-inductance of straight conductors | [H] |

| | | |
|---|---|---|
| $L_T$ | Total inductance between conductors | [H] |
| $l$ | Length | [m] |
| $l_c$ | Inductor core length | [m] |
| $l_g$ | Inductor air gap length | [m] |
| $M$ | Mutual inductance | [H] |
| $M_+$ | Positive mutual inductance | [H] |
| $M_-$ | Negative mutual inductance | [H] |
| $N$ | Number of phase | |
| $N_{turns}$ | Number of turns on the inductor winding | |
| $P$ | Power | [W] |
| $P_{cond}$ | Diode conduction losses | [W] |
| $P_{conduction(SW1)}$ | Conduction losses in SW1 | [W] |
| $P_{conduction(SW2)}$ | Conduction losses in SW2 | [W] |
| $P_{cu}$ | Conduction losses in copper | [W] |
| $P_{gate(SW1)}$ | Gate charge losses in SW1 | [W] |
| $P_{gate(SW2)}$ | Gate charge losses in SW2 | [W] |
| $P_{in}$ | Input power | [W] |
| $P_{lost}$ | Power lost | [W] |
| $P_{out}$ | Output power | [W] |
| $P_{rr}$ | Reverse recovery losses | [W] |
| $P_{SW1(off)}$ | The turn off losses in $SW_1$ | [W] |
| $P_{SW1(on)}$ | The turn on losses in $SW_1$ | [W] |
| $P_X$ | Power dissipated in component $X$ | [W] |
| $P_{14}$ | Power flowing into/out of the 14V power bus terminals | [W] |
| $P_{42}$ | Power flowing into/out of the 42V power bus terminals | [W] |
| $Q$ | Heat dissipated by a heat source | [W] |
| $Q_{gd}$ | Gate drain charge | [C] |
| $Q_m$ | Mutual inductance parameter | |
| $Q_{measured}$ | Measured heat flowing through the thermopile | [W] |
| $Q_{max\_X}$ | Maximum charged stored in component $X$ | [C] |
| $Q_{processed\_X}$ | Maximum charge processed in component $X$ | [C] |
| $Q_{rr}$ | Reverse recovery charge | [C] |
| $R$ | Resistance | [Ω] |

| | | |
|---|---|---|
| $R_{DS\_on}$ | MOSFET on resistance | [Ω] |
| $R_{gate}$ | External gate resistance | [Ω] |
| $R_{gate\ driver}$ | Internal resistance of the gate driver | [Ω] |
| $R_t$ | Thermal resistance | [°C/W] |
| $R_{t,conduction}$ | Thermal resistance due to conduction | [°C/W] |
| $R_{t,convection}$ | Thermal resistance due to convection | [°C/W] |
| $R_{t,max}$ | The maximum allowable thermal resistance | [°C/W] |
| $R_{t,nom}$ | The nominal thermal resistance | [˚C/W] |
| $R_{t,radiation}$ | Thermal resistance due to radiation | [°C/W] |
| $r$ | Radius of a circle | [m] |
| $S$ | Diode snappy factor | |
| $T_{ambient}$ | Ambient temperature | [°C] |
| $T_{component}$ | Component temperature | [°C] |
| $T_{dt}$ | Dead time | [s] |
| $T_{environment}$ | Environment temperature | [°C] |
| $T_{heat\ source}$ | Maximum temperature in a heat source | [°C] |
| $T_{max}$ | Maximum desired or allowed temperature | [°C] |
| $T_{module}$ | Module temperature | [°C] |
| $T_s$ | Switching period | [s] |
| $T_{thermal\ interface}$ | Thermal interface temperature | [°C] |
| $t$ | Thickness | [m] |
| $t$ | Time | [s] |
| $t_{con}$ | Total conduction time | [s] |
| $t_{if}$ | MOSFET current fall time | [s] |
| $t_{iso}$ | Thickness of isolation between windings | [m] |
| $t_{ir}$ | MOSFET current rise time | [s] |
| $t_{rr}$ | Total reverse recovery time | [s] |
| $t_{rr1}$ | First interval of the reverse recovery current | [s] |
| $t_{rr2}$ | Second interval of the reverse recovery current | [s] |
| $t_{vf}$ | MOSFET voltage fall time | [s] |
| $t_{vr}$ | MOSFET voltage rise time | [s] |
| $t_{winding}$ | Thickness of planar winding | [m] |
| $V$ | Voltage | [V] |

| | | |
|---|---|---|
| $V_{gate}$ | Voltage applied to gate source | [V] |
| $V_{fw}$ | Diode forward voltage | [V] |
| $V_{plt}$ | MOSFET plateau voltage | [V] |
| $V_s$ | The supply voltage | [V] |
| $V_{th}$ | MOSFET threshold voltage | [V] |
| $V_{thermopile}$ | The thermopile output voltage | [mV] |
| $V_{14}$ | Voltage of the 14V power bus | [V] |
| $V_{42}$ | Voltage of the 42V power bus | [V] |
| $v(t)$ | Voltage as a function of time | [V] |
| $w$ | Width of a conductor | [m] |
| $w_{cen}$ | With of the centre member of the core | [m] |
| $w_w$ | Inductor winding window width | [m] |
| $Y$ | Frequency compensation factor | |
| $Z$ | Impedance | [Ω] |

**Greek Letters**

| | | |
|---|---|---|
| $\Delta B$ | Change in magnetic flux density | [T] |
| $\Delta I_L$ | Inductor current ripple (peak to peak) | [A] |
| $\Delta T$ | Temperature difference | [°C] |
| $\Delta V$ | Voltage ripple | [V] |
| $\varepsilon$ | Permittivity of a material | [F/m] |
| $\varepsilon_0$ | Permittivity of free space | [F/m] |
| $\varepsilon_r$ | Relative permittivity | |
| $\zeta_{relative}$ | Relative Volume Utilisation | |
| $\mu$ | Permeability of material | [H/m] |
| $\mu_0$ | Permeability of free space | [H/m] |
| $\mu_r$ | Relative permeability | |
| $\rho$ | Electrical resistivity | [Ωm] |
| $\phi_h$ | The phase shift of the $h^{th}$ component | [rad] |
| $\psi_{component}$ | Component volume | [$m^3$] |
| $\psi_{core}$ | Inductor core volume | [$m^3$] |
| $\psi_{energy\_storage}$ | Energy storage volume | [$m^3$] |
| $\psi_{field\_establishment}$ | Volume to establish and direct electric or magnetic fields | [$m^3$] |

| | | |
|---|---|---|
| $\psi_{heat\_collector}$ | Volume of the heat collector excluding the heat paths | [$m^3$] |
| $\psi_{inductor}$ | Inductor volume (core and winding) | [$m^3$] |
| $\psi_{other}$ | Volume of remaining component parts | [$m^3$] |
| $\psi_{thermal\_management}$ | Thermal management structure volume | [$m^3$] |
| $\psi_{total}$ | Total module volume | [$m^3$] |
| $\psi_{total\_assembly}$ | Total assembly volume | [$m^3$] |
| $\psi_{unused}$ | The assembly volume not occupied by components | [$m^3$] |
| $\psi_{winding}$ | Inductor winding volume | [$m^3$] |

**Acronyms**

| | | |
|---|---|---|
| *AC* | Alternating current | |
| *AMD* | Arithmetic mean distance | [m] |
| *CCM* | Continuous conduction mode | |
| *COF* | Component optimisation factor | |
| *CPES* | Centre for Power Electronic Systems | |
| *CS* | Component stresses | |
| *CTE* | Coefficient of thermal expansion | [ppm/˚C] |
| *DBC* | Direct bonded copper | |
| *DC* | Direct current | |
| *DCM* | Discontinuous conduction mode | |
| *EMI* | Electromagnetic interference | |
| *ESR* | Effective series resistance | [Ω] |
| *GMD* | Geometric mean distance | [m] |
| *IGBT* | Insulated gate bi-polar transistor | |
| *IMS* | Insulated metal substrate | |
| *IPM* | Integrated power module | |
| *$I^2$PM* | Integrated intelligent power module | |
| *ISG* | Integrated starter/generator | |
| *ISM* | Integrated system module | |
| *MMC* | Metal matrix composite | |
| *MOSFET* | Metal oxide field effect transistor | |
| *PCB* | Printed circuit board | |
| *PM* | Power module | |

| | | |
|---|---|---|
| *RMS* | Root mean square | |
| *SOF* | System optimisation factor | [$J^2$] |
| *VRC* | Volume ratio constant | |
| *ZCCM* | Continuous conduction mode with zero crossing | |
| *ZCS* | Zero current switching | |
| *ZVS* | Zero voltage switching | |

**Vectors**

| | | |
|---|---|---|
| $\nabla T$ | Divergence of the temperature field | [°C/m] |
| $\overline{q}$ | Heat flux vector | [$W/m^2$] |
| $\hat{x}$ | Unit vector in x direction | |
| $\hat{y}$ | Unit vector in y direction | |
| $\hat{z}$ | Unit vector in z direction | |

# Chapter 1

## INTRODUCTION

## 1. Introduction

In the early 1950s the nominal voltage of the automotive power distribution network was doubled from 6V to 12V in response to the 6V power distribution network no longer being capable of meeting the increasing power demand of the passenger vehicles [1-1][1-2]. Today, with the implementation of many additional systems and creature comforts, the 12V power distribution network is facing the same limitations as the 6V distribution network did in the 1950s and is once again about to be changed.

The original conversion from 6V to 12V was a relatively simple matter: the upgrade was made possible with an upgrade kit consisting of a 12V battery, a 14V DC generator, a new ignition coil and a few new lamps. Today the upgrade is far from simple. Modern vehicles have evolved into highly complex and highly optimised systems and to change an aspect as fundamental to that system as the supply voltage level will be a lengthy and complicated process.

In 1994, Mercedes-Benz together with Massachusetts Institute of Technology (MIT) started investigating alternative voltage levels for the passenger vehicle power distribution network [1-3][1-4]. After collaborating for a year and a half with 7 other automotive companies, a proposal was made that the new power distribution network voltage be lifted to 42V, supported by a 36V battery in the so-called "42V PowerNet Bus". The results of the collaboration were made public in 1996 in the August issue of the IEEE Spectrum and were immediately adopted by many automotive companies [1-5].

The voltage level of 42V was selected because it is the highest multiple of 14V[a], including

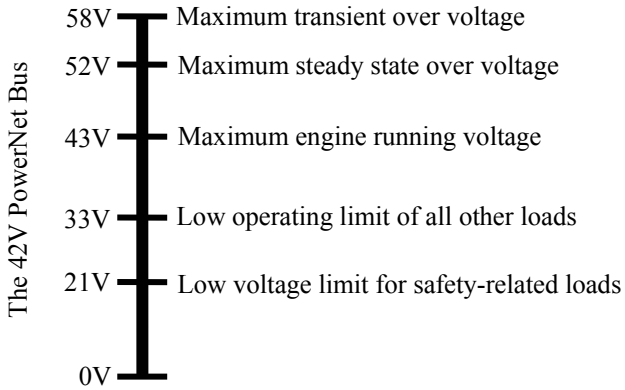


**Figure 1.1. Definition of the 42V PowerNet Bus**

[a] 14V is the Key-on voltage of the 12V power distribution network due to the charging alternator.

transient over voltages, that is below 60V the internationally agreed upon definition of a safe low voltage. The 42V PowerNet Bus is defined as in Figure 1.1 [1-2][1-4].

The main driving force behind the new power distribution network voltage is to increase the efficiency of the passenger vehicles while increasing the level of comfort and safety of the vehicle for its occupants. This means reduced fuel consumption while making the vehicle even more attractive and safe to prospective buyers. To achieve this many auxiliary functions can be added to the vehicle while existing functions need to be mechanically decoupled from the engine crankshaft.

An example of a function being decoupled from the crankshaft is electromagnetically actuated valves [1-1][1-2]. If the valves controlling the gas flow into and out of the engine cylinders are controlled electromagnetically, the engine can be operated more efficiently, resulting in a fuel saving. However, this is only possible if sufficient electrical power is available. With more electrical functions being implemented, the current 12V power distribution network is quickly overloaded, resulting in dangerously high currents. With the implementation of the 42V PowerNet bus, many more electrical functions can be incorporated into the passenger vehicle without resulting in excessively large currents – and thus avoiding additional heavy and costly copper cables.

A second advantage of decoupling functions from the crankshaft is the additional flexibility in the design of the vehicle. For example, if the water pump is driven electrically, it no longer has to be mounted on the engine in such a way as to be driven by the crankshaft but can instead be mounted elsewhere simplifying the design of the engine compartment. This can result in better control over the pump flow rate (being electrically controllable) and a smaller engine compartment.

Examples of other functions that can be implemented with the increased power that the 42V PowerNet bus makes available include [1-2][1-6][1-7]:

i. Fuel economy
   - Electrically driven accessories (water pump, oil pump, fan)
   - Electromagnetically actuated valves
   - Electrically aided steering
   - Electrical air conditioning
   - Stop and go (combustion engine is automatically turned off when stopping and started when driving off)
   - Electrically aided drive train (hybrids, regenerative breaking)
   - Electric turbo boost

ii. Reduced emissions
   - Electrically heated catalytic converter
   - Plasma exhaust processing
   - Electromagnetically actuated valves
   - Stop and go

iii. Comfort and safety
   - Electrically aided steering (drive by wire)
   - Electrically aided braking (break by wire)
   - Electrically aided suspension (active suspension)
   - Electrical de-icing (windscreen defogging)
   - Electrically heated seats
   - On-board entertainment

## 2. The dual voltage architecture

The 42V PowerNet allows many functions to be implemented that the previous 14V system did not allow due to the high power required. Migrating to the 42V system allows these high power levels to be achieved while avoiding heavy cables and high current switch gear, thereby reducing cost. Unfortunately the automotive industry is highly cost competitive and the immediate migration to the new voltage level is not possible due to the huge cost it would incur. Many of the components in the 14V power distribution network are the result of many years of research and optimisation. The simplest example is the 14V lamps used for lighting. To replace this component with an equivalent 42V lamp using the same technology would require a filament that is either 9 times longer or 9 times thinner for the same illumination. This would result in serious reliability issues.

As a trade-off, the new 42V PowerNet is to be introduced in conjunction with the existing 14V power distribution network in a dual voltage architecture. The 42V bus supplies power to the high power loads while the 14V bus supplies power to the low power loads, such as the key-off loads[a]. The advantage of this solution is that the current level of the high power loads can be reduced (due to the higher supply voltage) while still being able to take advantage of the highly optimised, low cost 14V components. The transition period in which both voltages will be present in the automobile is expected to be approximately 10 to 15 years.

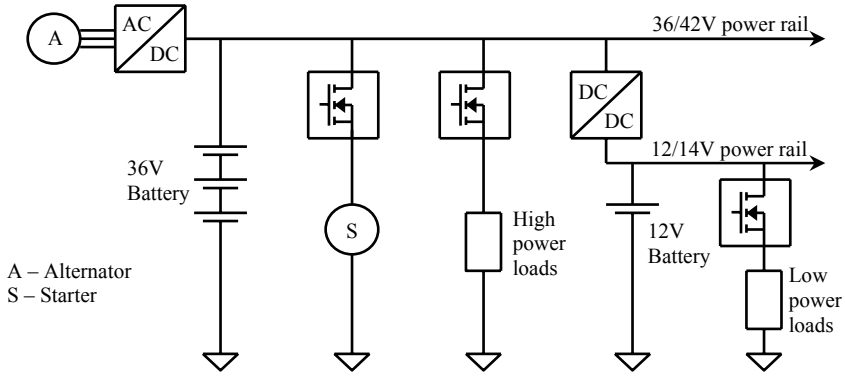


**Figure 1.2a. The dual voltage architecture with two batteries**

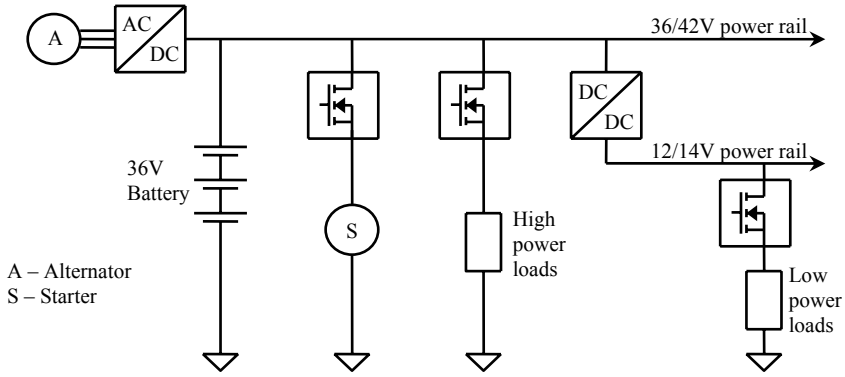


**Figure 1.2b. The dual voltage architecture with one battery**

[a] Key-off loads are loads that require power also when the engine is off. Examples include the on-board entertainment, lighting, navigation, etc.

Several different architectures have been proposed for the implementation of the dual voltage power distribution system [1-4][1-8]. Two examples are illustrated in Figure 1.2, which shows the dual battery system (Figure 1.2a) and the single battery system (Figure 1.2b). In both architectures the starter and generator can be implemented with separate units or a single integrated starter/generator (ISG). The high voltage bus supports the high power loads while the low voltage bus supports the low power loads implemented with the conventional 14V components.

The dual voltage, dual battery system has two batteries, namely a 36V and 12V battery. The 36V battery supplies power to the 42V bus together with the alternator. A bi-directional DC/DC converter interfaces the 42V and the 14V busses to allow the bi-directional flow of energy between the two busses. This configuration is the most flexible and reliable since in the case of an emergency, power can be directed from either the 12V battery to the 42V bus or visa versa. The configuration can be made even more reliable by the inclusion of a separate alternator for the 14V bus.

A low cost alternative to the dual voltage, dual battery system is the dual voltage, single battery system. In this configuration there is only a 36V battery present to supply all the electrical power. The bi-directional DC/DC converter's power rating will also increase to accommodate the peak load of the 14V bus instead of the average power as in the case of the dual voltage, dual battery system.

There are several other possible architecture configurations of the dual voltage power distribution network. However, all the proposed configurations have the bi-directional DC/DC converter in common. The power rating of the DC/DC converter varies between the different configurations depending on if it must process the peak or the average power being transferred between the voltage busses. In the case that the converter must process the peak power, the converter is currently rated around 2kW and the rating is expected to continue rising, while the converter that is designed for the average power is typically rated for approximately 1kW [1-1][1-9][1-10].

# 3. Power electronics in the passenger vehicle

The implementation of 42V in the automobile has opened the door to many new and exciting applications and, as discussed in the previous section, most are realised and/or controlled electrically, thus requiring power electronics. However, the power electronic systems implemented in the automotive environment must be capable of operating in the extreme conditions that they are exposed to.

## 3.1 The automotive environment

Electronic systems implemented in a passenger vehicle are exposed to an extremely harsh environment in terms of high ambient temperatures, large vibration forces, dirt, chemicals, petroleum vapours and various fluids [1-11]. Furthermore, the volume available for the implementation of these systems is becoming ever scarcer since more functions are being implemented in the limited volume available within the passenger vehicle. Under these conditions the implemented electronic and power electronic systems must be reliable, durable, and cost-effective, and must have small volumes.

A typical temperature distribution within a passenger vehicle is illustrated in Figure 1.3 [1-11][1-12][1-13]. The figure shows that the temperature near the internal combustion engine can

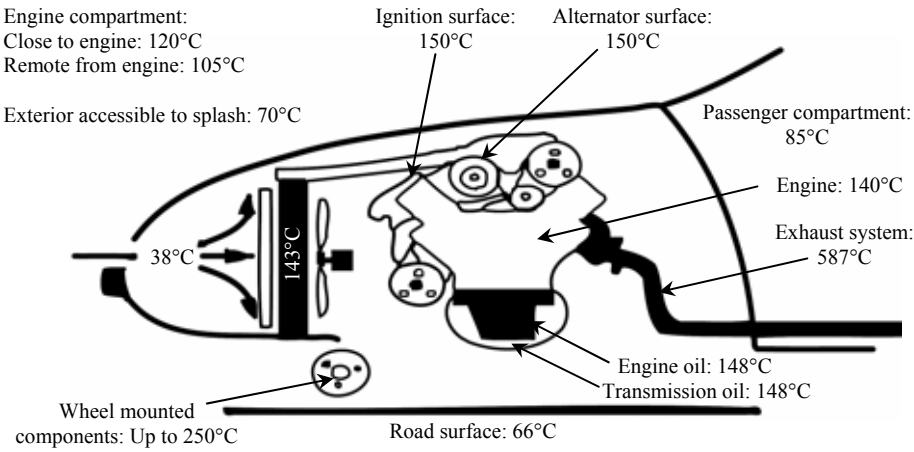


**Figure 1.3. The typical automotive thermal environment**

go as high as 140°C or 150°C, while at a distance from the engine temperatures can drop to between 90°C and 120°C. This is the ambient temperature that the electronic systems implemented in the automotive environment must operate within. A second extreme condition exists when the vehicle is operated in sub-zero conditions. It is then possible for the ambient temperature in which the electronic systems must operate in to be as low as -40°C [1-11][1-12]. Thus any electronic or power electronic system implemented in the engine compartment must operate in a temperature range of at least -40°C to 125°C [1-11].

The heat generated within the internal combustion engine is transferred to the surrounding environment primarily through a circulating liquid coolant and a radiator. The heat is transferred from the internal combustion engine to the liquid coolant and then to the surrounding environment through the radiator. The liquid coolant's nominal temperature is approximately 85°C to 90°C but can be anywhere between -40°C and 125°C under pressure, depending on the surrounding environment and operating conditions [1-2][1-12]. Due to cost restrictions, the same coolant system used to cool the internal combustion engine must also be used, if necessary, to cool any electronic system implemented within the engine compartment. This means that any power electronic system within the engine compartment that needs additional cooling for its operation will be cooled with a coolant that has a nominal temperature of approximately 85°C and a maximum temperature of approximately 125°C. This poses significant challenges to the design of the power electronic systems that are implemented within the automotive environment.

## 3.2 The automotive environment as a technology driver

Since electronics were first implemented in automobiles, their primary function has been to make the vehicles more reliable and safer [1-14]. This trend started with the first 6V systems and has never stopped since – with modern vehicles boasting a large range of safety enhancement features such as air bags, ABS, traction control, etc. The rate at which the electronic systems were introduced into the vehicle for this purpose has so far been determined by the maturity, cost and reliability of the technology [1-14]. This trend is beginning to turn around. The automotive applications and environment are beginning to become the technology drivers.

A clear example of this is illustrated by the 2002 International Technology Roadmap for Semiconductors that reflects the need for electronic components with higher operating

temperatures for application in harsh environments [1-12]. Both the 2002 and 2003 roadmaps raise the operating temperature of power devices from 150°C in 2002 to 200°C by 2007[a]. The power devices with the high operating temperature will be used for the power section of power converters and motor drives for electromechanical actuators. This has led to much interest in silicon carbide (SiC) devices due to their high operating temperature capabilities (in excess of 300°C) [1-2].

Another example of the automotive environment driving a technology is in the development of special capacitors; aluminium electrolytic, metal film and ceramic, for application in the thermally harsh automotive environment [1-15][1-16]. These components are designed to operate with ambient temperatures as high as 150°C to 160°C with an acceptable lifetime. The capacitors are critical to the development of power electronic systems for the automobile since without them very few power electronic systems would be possible.

The automotive environment has also resulted in much research being directed towards the packaging of the high temperature components. An example of a high temperature transmission controller by Daimler-Chrysler is illustrated in Figure 1.4 [1-12]. The transmission controller is designed to in a local ambient temperature of up to 150°C. To achieve this the circuit carrier is ceramic since the maximum operating temperature of ceramic is significantly higher than that of FR4 (PCB). This allows the controller to be located within the transmission, obviating the need for excessive cabling between the transmission and controller and thereby reducing costs, saving space and increasing reliability.

A second example of packaging a power electronic system into the automotive environment is illustrated in Figure 1.5, which shows a three phase inverter integrated into the stator of an electric motor of a mild hybrid passenger vehicle [1-17][1-18][1-19]. The inverter is integrated into the stator of the machine to obviate the need for long cables between the inverter and the machine and saving the additional space the inverter would occupy. Reducing the length of the cables between the machine and the inverter helps to significantly reduce electromagnetic noise

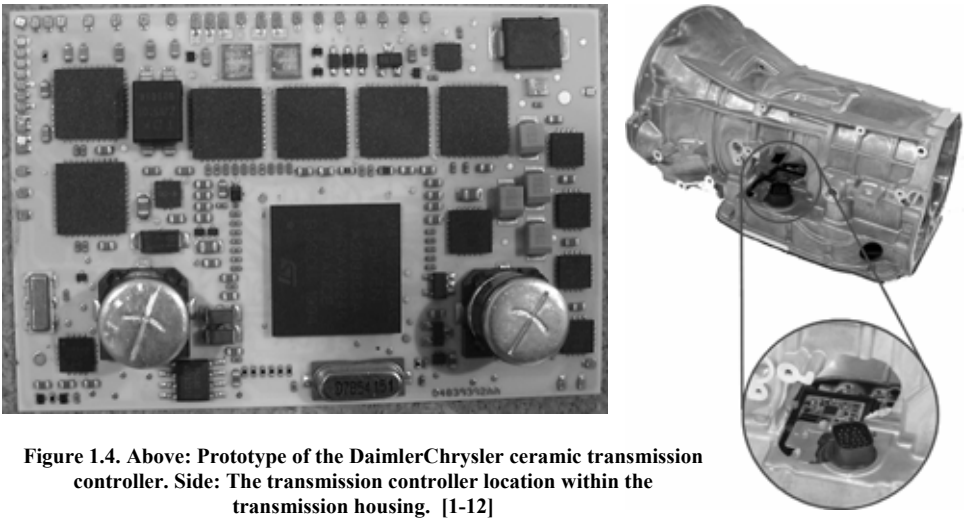

**Figure 1.4. Above: Prototype of the DaimlerChrysler ceramic transmission controller. Side: The transmission controller location within the transmission housing. [1-12]**

[a] It should be noted that for a power device at the maximum rated temperature, the power handling capability of that device is de-rated to zero. Thus, a component rated for 150°C operating in an environment of 150°C will not be able to conduct any current without the device losses raising the components temperature beyond its rating.

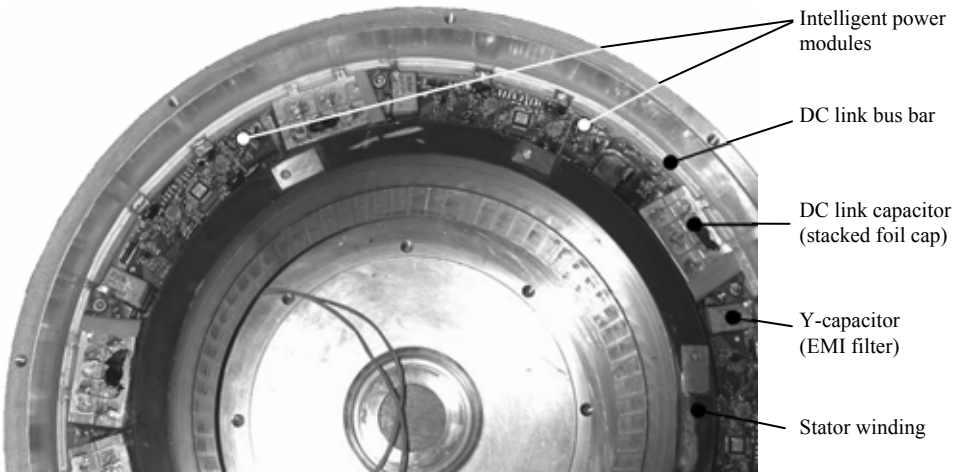


**Figure 1.5. The stator of the induction machine with integrated inverter**

emissions due to the high rate of change in the voltage and current waveforms. The demonstrator in the figure is a 90kVA inverter cooled with the internal combustion engine coolant. The inverter is implemented with novel shaped power modules that use the latest technologies to handle the large power with an ambient temperature of 125°C.

### 3.3 System integration in the automotive environment

Implementing an electronic system, specifically a power electronic system in the automotive environment, requires a multi-disciplinary design. The multi-disciplinary design must take the electrical design of the topology, the design of the thermal management system and the mechanical design into account and optimise them simultaneously [1-20][1-21]. This is a necessity if the electronic or power electronic system is to be successfully integrated into the automotive environment and still meet the given specifications.

## 4. Problem description

The bi-directional DC/DC converter in the dual voltage architecture presents many implementation and system integration challenges. The converter must operate in a high temperature environment with a high power density and have a high efficiency. Very few of the initial attempts at these specifications were successful.

In 2001 the Delft University of Technology in the Netherlands and Siemens AG Corporate Technology, CT PS 2, in Munich, Germany began a project together to investigate high power density, three-dimensional packaging of converters in power electronic modules. This approach to implementing a power converter was selected to implement the automotive DC/DC converter since the objectives of the project coincided well with the requirements of the automotive environment. This thesis is the result of this project.

The main challenge to implementing a complete power converter in a power electronic module is the system integration required to ensure that the electrical, thermal and spatial requirements are all met in the same volume and simultaneously. To be able to perform the system integration required, an intimate understanding of the underlying interdependencies between the different design domains is required. With this knowledge, it is possible to manipulate the designs to meet the required specifications. These design interdependencies and design

manipulations are studied in this thesis. The knowledge gained from the study is used to implement a power converter in a power module with a high power density and capable of operating in high ambient temperature environments.

### 4.1 Thesis objectives

The main objectives of this thesis can be summarised as:

i. *To investigate the possibility of implementing the complete automotive converter in a state of the art power electronic module*

ii. *To analyse the interdependencies that exist between the electrical, the thermal and the spatial design of the power electronic module*

iii. *To develop techniques for a multi-objective design so that the power electronic module can meet all the given specifications*

iv. *To design and construct a high power density, 3D integrated power electronic module prototype for the automotive environment*

### 4.2. The Automotive Power Module Specifications

In order to describe the problem fully, a brief summary of the specifications of the automotive DC/DC converter is included.

The converter is to be capable of bi-directional power transfer of 2kW over an operating voltage range of $11V < V_{14} < 16V$ and $30V < V_{42} < 50V$ where $V_{14}$ and $V_{42}$ are the terminal voltages of the converter. The converter is to be cooled with the internal combustion engine's coolant system. The 2kW power level is to be achieved over the complete coolant temperature range of -40°C to 110°C. For a coolant temperature of between 110°C and 125°C, the output power of the converter is de-rated to 1kW.

The converter is to include the complete power conversion system including the necessary EMI filters, control and auxiliary power supply to produce a complete self-standing power conversion system. The volume of the converter should be as small as possible.

## 5. Thesis Layout

The layout of the thesis is illustrated in Figure 1.6.

Chapter 2 considers the current status of power electronic modules. Various power modules are identified and categorised. The Integrated System Module (ISM) is selected for implementing the automotive DC/DC converter. The consequences of the automotive environment for the design of the module are considered.

Chapter 3 begins the main contribution of the thesis. The chapter considers the interdependence between the electrical, the thermal and the spatial design of a power module. The interdependencies between the different design domains are identified together with trade-offs that can be used to manipulate the design. The intension is to manipulate the design in such a way that the electrical, thermal and spatial aspects of the module design are all optimised in the same volume simultaneously. Each of the three designs is considered in more detail in one of the following three chapters, as illustrated in Figure 1.6.

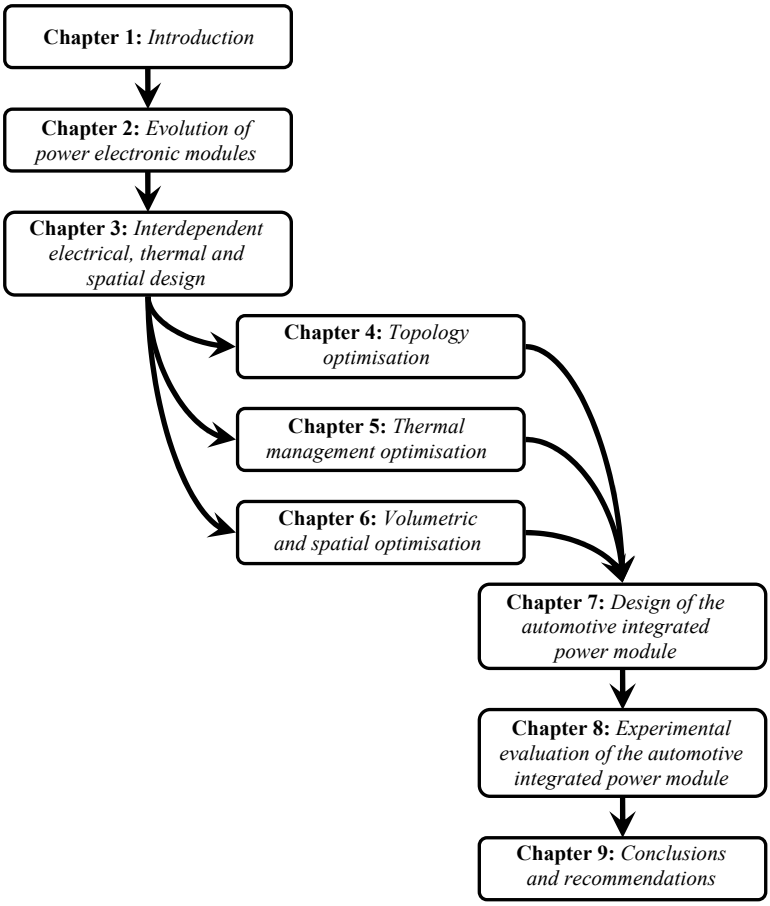


**Figure 1.6. The thesis layout**

The optimisation of the electrical topology implemented in the integrated power module with respect to the integral electrical, thermal and spatial design is considered in Chapter 4. The chapter considered how the topology can be manipulated so as to minimise the requirements the topology imposes on the thermal design in terms of heat and on the spatial design in terms of volume required for energy storage.

Chapter 5 considers the optimisation of the thermal management implemented within the integrated power module in terms of the integral electrical, thermal and spatial design. The chapter considers what measures need to be taken to be able to operate in a high ambient temperature environment and presents methods to achieve this.

The volumetric and spatial optimisation of the power module with respect to the integral electrical, thermal and spatial designs is considered in Chapter 6. The chapter considers how the volume of both the components within the integrated power module and the integrated power module itself can be minimised while still being able to operate in a high temperature environment. Various methods for achieving this are considered.

Chapter 7 presents the development of the experimental automotive prototype converter. The knowledge and techniques presented in the previous chapters are used to design the converter to meet the given specifications.

The experimental converter is evaluated in Chapter 8 and the results are presented.

The thesis is concluded with Chapter 9, which summarises the most important conclusions reached in the thesis. Recommendations for future research on the subject are also made.

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# Chapter 2

## EVOLUTION OF THE POWER ELECTRONIC MODULE

## 1. Introduction

In the previous chapter, the interdependent design of the automotive DC/DC converter for the dual voltage architecture was identified as a central theme of this thesis. As part of the specification, the DC/DC converter must be implemented in the form of a self-contained module that is compatible with the automotive environment. In this chapter, power electronic modules are investigated as a feasible solution to the implementation of the automotive converter requirements.

The development of power electronic modules is considered in section 2. Power electronic modules have evolved from single device components to complete systems integrated into a single module having a high level of functionality and intelligence. Some development trends concerning the modules functionality and intelligence are identified.

In section 3, projections into the future of power electronic modules are made based on the development trends of current power electronic modules.

Section 4 considers implementing the automotive converter in a power electronic module. The boundary conditions that the automotive environment impose on the module are identified and the corresponding assumptions are made. The chapter is concluded by a consideration of what must be investigated to make the automotive power module a reality.

## 2. The evolution of power electronic modules

Power electronic module is a term that is loosely used to refer to anything from a single power semi-conductor to a system of power semi-conductors with the associated control and protection packaged into a single housing structure [2-1][2-2][2-3]. Power electronic modules are generally used in power conversion systems with power ratings starting in the low kilowatt range and extending to very high power ratings. In this section various types of power electronic modules are identified as the module development is considered. The study of power electronic modules is limited to modules or systems with power ratings of more than a few hundred watts to those in the low tens of kilowatts.

### 2.1 Power module definition

A power electronic module can be defined as a packaging strategy that allows from a single to multiple power devices to be packaged together in a single insulated structure with improved thermal performance and reliability and has the possibility of including all or part of the control system, the protection system and the sensing system in the structure. In some cases, the complete power processing system can be packaged in the power module.

There are several variants of power electronic modules available on the market today. Based on definitions used in industry and expanding on these definitions, power electronic modules can

be classified in order of increasing functionality as [2-1]-[2-7]:

i. *Power module (PM).* A power module is a structure that contains one or more power device in a single structure without any auxiliary intelligence.
ii. *Intelligent power module (IPM).* An IPM is a power module with additional functionality integrated into it. An IPM typically contains the power devices, the gate drivers, protection, current sensing and temperature sensing. One such example is the active IPEM (Integrated Power Electronic Module) developed at CPES [2-6].
iii. *Integrated intelligent power module ($I^2PM$).* An $I^2PM$ is a power module with additional intelligence integrated into the power module structure. The typical $I^2PM$ consists of the power devices, the gate drivers, protection, current and temperature sensing, power supply, signal isolation, signal conditioning and possibly a micro-processor.
iv. *Integrated system module (ISM).* The ISM is a complete power conversion system in a single modular structure. The module is self-contained, self-protecting and self-driven. No additional components are required to implement a working system (with the possible exception of EMI filters).

There are several drivers motivating the development of power electronic modules. These drivers can be summarised as [2-1]-[2-4]:

i. *Power density.* With multiple power devices packaged in one structure, the overhead volume required for packaging all of the individual devices is significantly reduced. Further, if functions such as current and temperature sensing are integrated into the power electronic module, then they need not be implemented outside of the module, and this helps to further increase the system's power density.
ii. *Cost reduction.* Modern power electronic modules contain the minimum of materials and are manufactured in a highly automated process with a minimum of auxiliary materials, tools and energy consumption [2-1]. There have been several attempts, and some successes, at standardising power modules' foot prints [2-4]. This reduces the cost of developing new housings for every power module – saving the development engineers time that would have had been spent on attending to packaging and thermal issues. Standardisation reduces the cost of the power modules while increasing their reliability.
iii. *Improved reliability.* Power electronic modules are being manufactured with fewer parts, fewer assembly processes and fewer material interfaces. Thus the assemblies are simple to assemble, and statistically have a lower failure rate.
iv. *Improved thermal performance.* Power electronic modules use advanced material technologies to implement the circuit carriers. For example, IMS (Insulated Metal Substrate) or DBC (Direct Bonded Copper), which allow for thick copper conductors while having very good thermal performance, are commonly used. With these technologies and unique packaging arrangements, thermal resistances as low as 0.01°C/W can be achieved from the power device to the heat sink [2-1][2-2].
v. *Efficiency improvement.* A major concern in the design of a power circuit is the leakage inductance in series with the power devices. This causes voltage overshoot, increasing the blocking voltage requirements of the power devices and increasing the devices' switching losses. The leakage inductance can be significantly reduced by having all the power devices in a single structure, reducing the devices switching losses [2-4]. In addition, if the voltage overshoot is reduced, the blocking voltage rating of the power device can also be reduced. In the case of power MOSFETs, the device on resistance increases exponentially with the peak blocking voltage. If the blocking voltage can be reduced, devices with smaller on resistances can be used,

reducing the devices' conduction losses [2-1].

vi. *EMI reduction.* The voltage overshoot due to the leakage inductance in series with the power devices is a significant source of EMI noise. With the leakage inductance reduced, the voltage overshoot is reduced, which in turn reduces the generated EMI noise.

vii. *High frequency.* The maximum operating frequency of the power devices is determined partly by the switching losses in the devices due to the device switching losses increasing with an increase in the operating frequency. Reducing the voltage overshoot reduces the device switching losses and indirectly can help to reduce the devices conduction losses. With reduced switching losses, the operating frequency can be increased for a given maximum operating temperature.

viii. *Environmental considerations.* Modern power modules are manufactured with lead-free solder and disposable plastic materials. Further, molybdenum is no longer used, and this makes the modules environmentally friendly [2-1].

Power electronic modules are being utilised in increasingly more applications for the above reasons. They are being used in most power ranges and their functionality is still increasing.

## 2.2 Overview of the power electronic module development

The functionality of power electronic modules continues to increase in response to user requirements. In this section, the power electronic module development is briefly considered. Considering how power modules have developed to their current status gives an indication of the trend, if any, the modules have being following. This trend can be extrapolated to see what the future holds for power electronic modules.

### *2.2.1 Power modules (PM)*

Power modules come in many shapes and sizes. Figure 2.1 shows three power modules each implementing a different switching function. In there simplest form, power modules are one or more power semi-conductor devices that have been packaged in a common housing that


**A phase arm power module**
**(Source: Semikron)**

**Low profile power module**
**(Source: Mitsubishi)**

**Econopack power module**
**(Source: Eupec)**

**Figure 2.1. Some typical power modules**

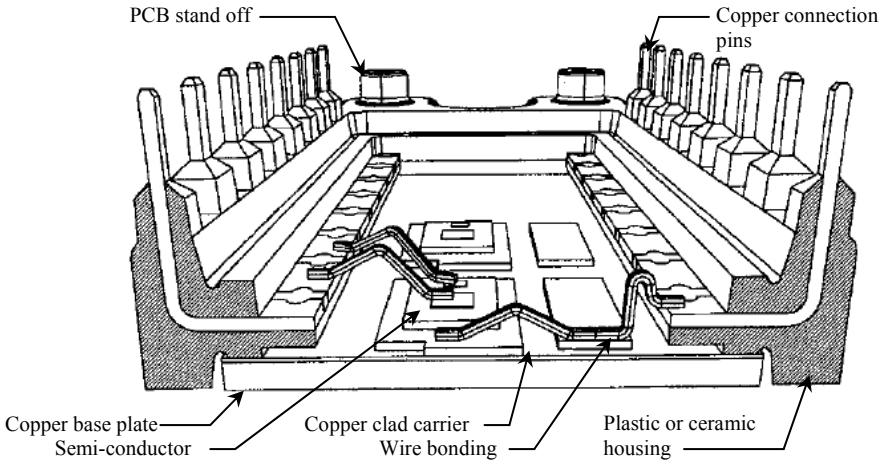



**Figure 2.2. An open section of a typical power module [2-9]**

provides separate interfaces for electrical power and dissipated heat [2-1][2-8]. Generally, power modules are implemented with either power MOSFETs (Metal Oxide Semi-conductor Field Effect Transistors) or IGBTs (Insulated Gate Bi-polar Transistors). IGBTs have the ability to operate at higher power levels with reduced conduction losses, making them suitable for high power applications, whereas MOSFETs can operate at much higher frequencies, making then suitable for applications where fast control and smaller volumes are required [2-4]. The internal configurations of the power modules are highly flexible, allowing for many combinations and circuit configurations to be implemented within similar modules [2-1].

Figure 2.2 shows a cross-section of a typical power module [2-9]. The power module consists of semi-conductor devices mounted on a circuit carrier which is in turn mounted on a heat spreader which serves as the base plate and interface to the heat sink. The semi-conductors are interconnected with wire bonding and protected from the environment by either a moulded plastic or ceramic casing. The casing is normally filled with either silicone gel or epoxy as encapsulate for protection and to minimise the effect of movement and mechanical shock. The casing also provides a mounting point for the module terminals. The module terminals are connected to the circuit carrier usually through wire bonding, pressure contact or by a solder joint. The power module is mounted on the heat sink with screws in mounting holes provided for in the base plate.

Two critical components in any power module are the base plate and the circuit carrier.

There are generally two technologies used to implement the circuit carrier. The first is DBC and the second is IMS [2-1]-[2-5]. DBC consists of a layer of ceramic with a sheet of copper foil bonded to either side. The ceramic can be implemented with either alumina ($Al_2O_3$) or AlN [2-4][2-11]. The ceramic material normally has a thickness of between 0.38mm and 0.68mm depending on the material strength required and the copper layer thickness is normally around 300μm. Ceramic material offers very good thermal performance with the coefficient of thermal conductivity between 100 W/m·K and 170W/m·K for AlN and between 17W/m·K and 35W/m·K for $Al_2O3$ [2-4]. Currently, $Al_2O_3$ is predominately used because the combined CTE (Coefficient of Thermal Expansion) of the DBC substrate is constrained by that of the ceramic and is approximately 6.5ppm/K, which is fairly close to that of silicon, being 4.1ppm/K. The CTE mismatch for AlN is smaller with the CTE of between 3ppm/K and 4ppm/K but is more costly [2-3][2-11]. The DBC substrate is normally soldered onto the base plate; however, there

are examples in which the DBC is attached to the base plate through other means such as pressure contacts [2-11].

The second circuit carrier technology is IMS. IMS typically consists of 100µm thick copper conductors insulated from a base plate by a very thin (typically 100µm to 150µm) organic dielectric insulating layer. The only real performance advantage that IMS has over DBC is that the thermal resistance of IMS degrades slower with thermal cycling than that of DBC [2-2]. The thermal conductivity of the organic layer is generally between 1W/m·K and 3W/m·K, while it has a CTE of approximately 24ppm/K. In addition, due to that low thermal conductivity of the organic layer, the organic layer must be very thin – making the IMS structure fragile and prone to loss of voltage isolation. Since the dielectric layer is so thin, a high parasitic capacitance can also be expected.

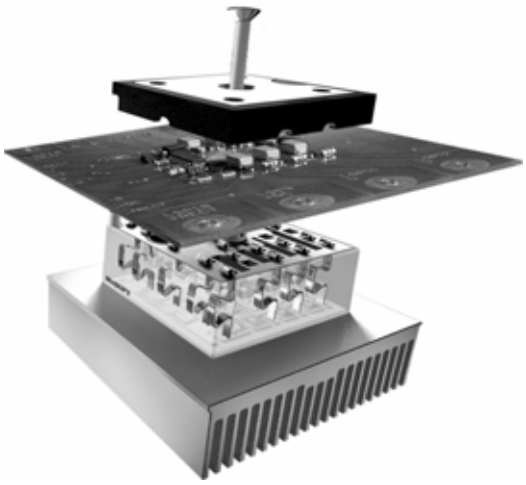
The base plate provides mechanical strength to the power electronic module, but more importantly it functions as a heat spreader, reducing the thermal resistance between the power devices and the heat sink. Base plates are traditionally implemented with either copper or aluminium due to the materials' high thermal conductivities, 390W/m·K and 220W/m·K respectively, and are generally between 3mm and 5mm thick. Both materials have CTEs that are much higher than that of silicon (copper – 17ppm/K and aluminium – 24ppm/K), which has driven industry to investigate alternatives to reduce the CTE mismatch between the power devices and the base plate. Metal matrix composites (MMC) such as Aluminium Silicon Carbide (AlSiC) and Beryllium-Beryllium Oxide (Be-BeO) have grown in popularity due to their better matched CTEs (AlSiC – 7.9 to 12.6ppm/W and Be-BeO – 6.8ppm/K) while still having very high thermal conductivities (175 to 240W/m·K and 240W/m·K respectively) [2-4].

Currently in the most advanced power modules, the base plate is removed from the power module to reduce the cost and to increase the power modules' reliability [2-1]. The metallised ceramic circuit carrier is brought directly into contact with the heat sink, usually through a pressure fixture. This helps to significantly reduce the thermal resistance between the power device and the heat sink.

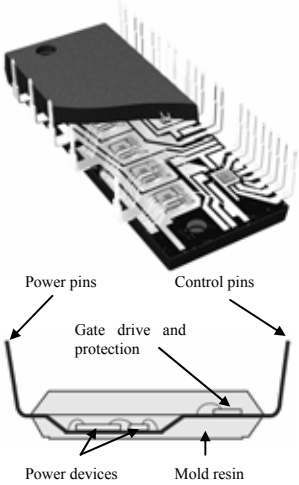
### *2.2.2 Intelligent power modules (IPM)*

The next logical step in the development of the power electronic modules is to include some intelligence into the power module. Intelligence is achieved by including additional sensing such as current and/or temperature sensing. This represents the lowest form of intelligence in power electronic modules [2-1]. A higher level of intelligence can be achieved by integrating the power device gate drivers and protection into the power electronic module.

Two examples of intelligent power modules, sometimes also referred to as integrated power modules, are illustrated in Figure 2.3. The figure shows an IPM for medium power on the left and for low power on the right. The medium power module is a form of low intelligence power module because the power module only has current measuring shunts and a temperature sensor integrated into the module. The power module from Semikron makes use of springs to maintain pressure between the electrical substrate in the power module and the PCB. The IPM is fixed to the PCB with only one screw. The low power module from Mitsubishi on the right of the figure has a higher level of intelligence, with the gate drivers and the protection integrated into the power module [2-10]. The power module is designed to function as a motor driver. There are many more examples available on the market and in the literature.



Mini SKiiP IPM
(Source: Semikron)




MiniDIP-IPM
(Source: Mitsubishi)

**Figure 2.3. Some examples of IPMs**

Figure 2.4 shows a cross-section of an intelligent power module manufactured by Mitsubishi [2-7]. The cross-section shows the IPM with the power electronics implemented as in a conventional power module and the additional gate driver and protection functions are implemented on a PCB that is mounted within the IPM. This approach offers some improvement in the power density of the power processing system but little additional performance is gained in terms of parasitic components (leakage inductance) and thermal performance. The additional intelligence implemented on the PCB is thermally disconnected from the power stage to avoid damaging the PCB and maintain a high level of reliability.

One of the primary limiting components in the power module is the wire bonding that is used for electrical interconnections between the semi-conductors within the module and the module substrate and terminals. The wire bonding does give the power module greater flexibility but also limits the power module's currents capability and reliability. Consequently, alternatives for implementing the interconnections within the IPMs are being developed. One such technology developed at CPES is briefly illustrated for use in IPMs.

***Flip-Chip-on-Flex (FCOF)***

FCOF is an interconnect technology that interconnects power devices and gate driver circuitry

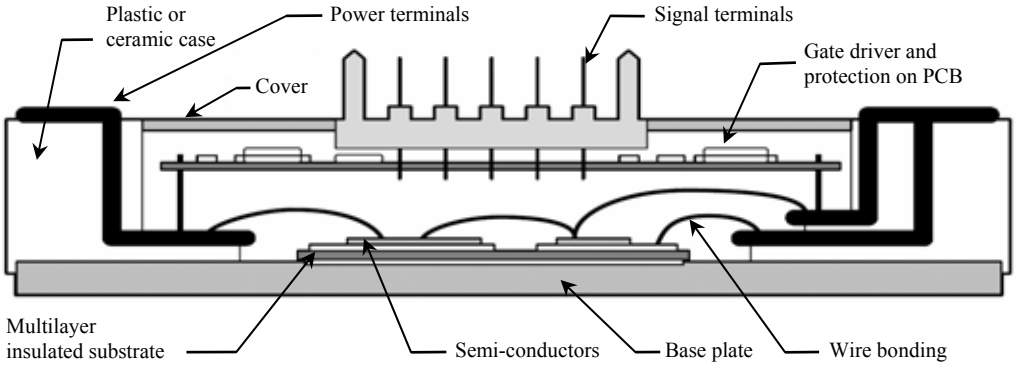



**Figure 2.4. An IPM with the gate driver implemented in the power module [2-7]**

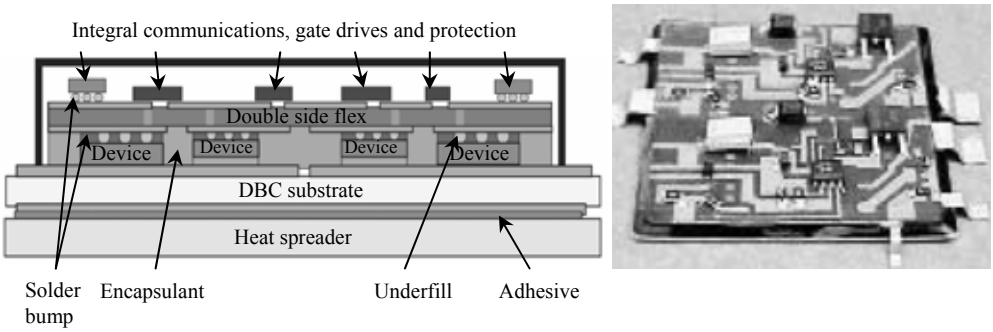



**Figure 2.5. An IPM implemented with Flip-Chip-on-Flex technology [2-13]**

together without the use of wire bonding [2-6][2-12][2-13]. The technology revolves around the use of a double sided flexible substrate and flip chip components.

In an FCOC structure, as illustrated in Figure 2.5, the flexible substrate has a circuit design etched onto both sides. One side of the flex substrate is connected to the power devices while the second side is used to implement a gate driver circuit and some additional protection. Via holes through the substrate allow interconnection between the two layers. The power device structures, termed Die Dimensional Ball Grid Array ($D^2$BGA) structures, together with the appropriate under-fill materials are soldered to the flexible substrate. The $D^2$BGA structure consists of a power chip, inner solder bump, high lead solder balls and moulding resin. To complete the power circuit and to attain good thermal performance the backs of the power devices are soldered onto a DBC substrate.

The under-fill material between the DBC layer and the flexible substrate is used to help alleviate the thermal mechanical stresses in the devices as well as improve the structure's thermal performance. To complete the structure, it is encapsulated for protection.

Replacing the wire bonds with the flexible substrate reduces the parasitic inductance in the power circuit but also allows the IPM to be implemented with a very low profile. An example is illustrated in the right of Figure 2.5.

Other interconnect technologies such as Dimple Array Interconnects addressed in [2-6] and Embedded Power Technology discussed in [2-6], [2-14] and [2-15] have also been developed at CPES to package IPMs with increasing functionality, performance and density. These technologies are not discussed here and the interested reader is referred to the literature.

### *2.2.3 Integrated intelligent power modules ($I^2PM$)*

The next step in the development of the power electronic module is a continuation of the intelligence trend seen thus far. Additional mechanical integration of functions such as internal power supplies for the gate drivers, isolation between the signal interface and the devices, signal conditioning and even microcontrollers for control functions contribute to elevating an intelligent power module to an integrated intelligent power module [2-1]. $I^2$PMs do not include the passive components required for the energy conversion process other than a small ceramic decoupling capacitor if applicable. Two examples of such $I^2$PMs are illustrated in Figure 2.6.

Both $I^2$PEMs shown in the figure use conventional power module technology to implement the power stage of the unit. The additional intelligence functions are implemented on a PCB structure mounted within the module but thermally disconnected from the power stage. This

The $I^2PM$ with integrated gate drives, protection and controller (Source: International Rectifier)


The SKiiP 3 $I^2PM$ with integrated gate drives, protection and controller (Source: Semikron)

**Figure 2.6. Two examples of industrial $I^2PMs$**

approach is highly flexible and saves the power engineer a significant amount of time and effort since he does not have to develop the gate drivers and associated circuitry and protection, dramatically reducing the concept to market time.

Integrated intelligent power modules are very well suited to motor drive applications over a wide power range and this is one of their primary uses [2-16][2-17][2-18]. The reason for this is that there are very few additional components other than a DC bus capacitor required along with the module to implement the rectifier and inverter. With the increased level of intelligence, the control functions of the inverter can easily be implemented within the power module [2-17]. With microcontrollers being integrated into the power module it is possible to implement the complete inverter within the $I^2PM$ while still maintaining a level of flexibility.

It is expected that the trend of integrating microcontrollers and memory into power modules is going to continue and increase. The microcontroller contributes a significant degree of freedom to the module allowing a range of functions, both control and diagnostics, to be implemented with the same hardware. This is expected to lead to a reduction in the cost of the power modules while maintaining the module's reliability and flexibility [2-1][2-17].

### *2.2.4 Integrated system module (ISM)*

The $I^2PM$ represents power modules with a very high level of integrated intelligence. The next

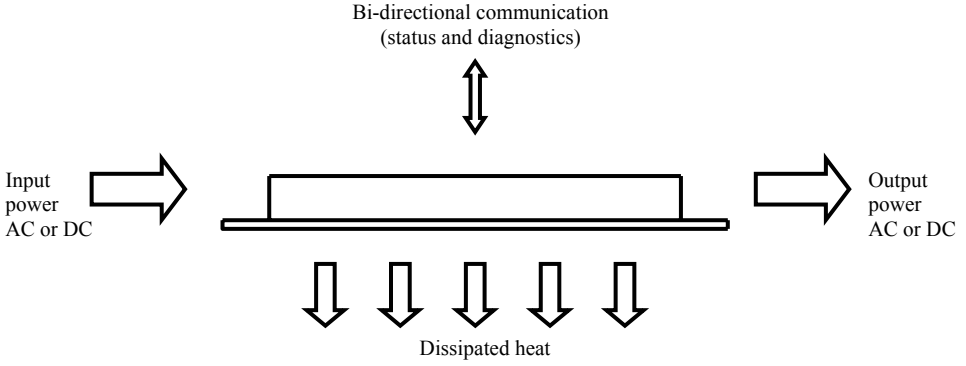



**Figure 2.7. An integrated system module (ISM) showing power, heat and communication flow**

step in the development of the power electronic module is to use the intelligence of the $I^2PM$ but to integrate the complete power circuit, including passive components and filters into a single integrated system module [2-19][2-20]. This is illustrated in Figure 2.7, which shows an ISM with power flowing into the module in the form of either AC or DC and flowing out of the module, again in the form of either AC or DC depending on the module requirements. In this process heat is dissipated and this leaves through the base plate beneath the ISM. A bi-directional communication interface is also required for overhead control and diagnostics of the ISM.

Integrating the passive components required for processing power into the ISM presents significant challenges in both the electromagnetic and thermal design of the components. The available volume within the power module must be used more effectively if a high power density is still to be achieved. To achieve this, the third dimension within the power module is utilised more extensively than in the previous power electronic modules [2-20]-[2-22]. This means that as components required for processing power move into the third dimension, the height of the module, the thermal behaviour of these components becomes more critical since it becomes more difficult to remove the heat from them [2-21]. The passive components implemented in the module's third dimension are different from the components implemented on the PCBs within the previous modules because the passive components are not thermally decoupled from the base plate but require the thermal coupling to the base plate for their thermal management. The circuit processing the power is no longer two-dimensional but three-dimensional. For this reason the use of passive components such as inductors and transformers is still limited in the ISM.

ISMs are generally more application specific but are still flexible and can be found implementing DC/DC point of load converters for distributed systems as well as inverters for motor drive applications. The use of ISMs for these two applications is considered briefly.

#### *2.2.4.1 ISM as an inverter*

An inverter implemented as an ISM for the automotive environment was developed by Semikron and is illustrated in Figure 2.8 [2-5][2-22]. The figure shows an exploded view of the ISM. The automotive environment is well suited to the ISM approach due to the server limitations placed on the volume of the systems implemented within the automotive environment. As the functionality and number of these systems continue to increase, the volume available for them is going to further decrease. The ISM approach saves volume by integrating all the functions required to implement the inverter into a single module. The illustrated module operates with a supply voltage of 42V and delivers a constant load current of $650A_{rms}$.

The ISM is implemented as follows with reference to Figure 2.8 [2-22]: The power devices are implemented using conventional DBC and wire bonding technology. The DBC structure is mounted on a water-cooled heat sink via a pressure plate. By removing the massive solder connection between the DBC and the heat sink, the reliability of the module can be significantly increased. The leakage inductance of the module is significantly reduced by integrating the DC bus capacitor and the bus bar system into the module. The connection between the bus bar and the DBC as well as between the control board and the DBC is maintained with pressure contacts. The complete control system – that is, the gate drivers for the three phases, the current and temperature measurement, the protection and the interface to the overhead controller – is implemented on a PCB mounted within the ISM.

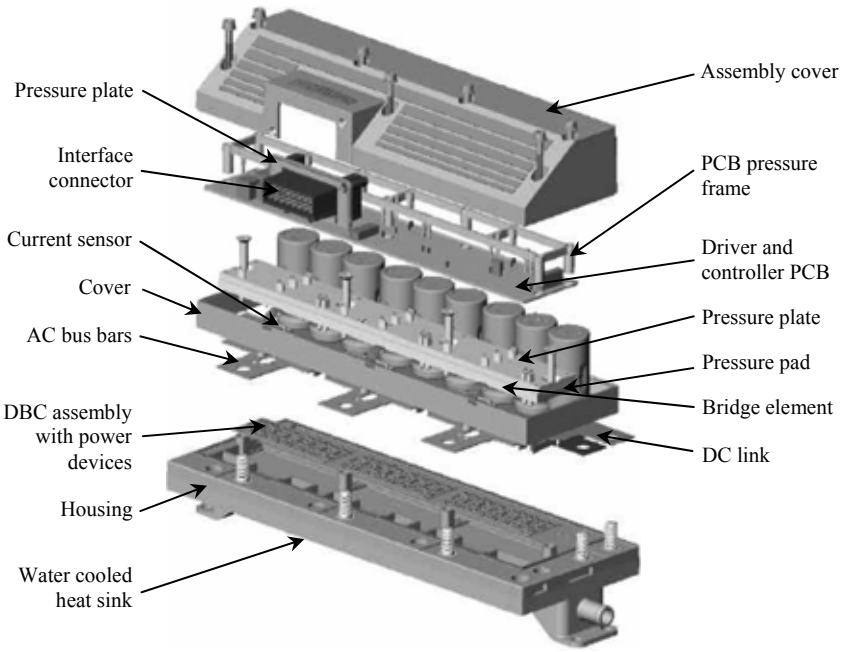



**Figure 2.8. Exploded view of the SKAI ISM inverter developed for the automotive industry [2-22]**

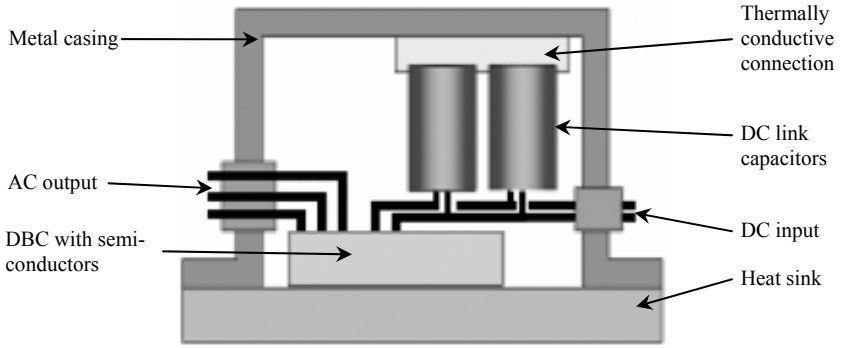



**Figure 2.9. A cross-section of the automotive ISM inverter**

The cooling of the bus capacitors is critical in this application. The module cover is implemented with metal, which offers additional cooling to any components physically attached to it. The bus capacitors are thermally connected to the metal cover to take advantage of this, as illustrated in Figure 2.9.

### *2.2.4.2 ISM as a DC/DC converter*

It is also possible to implement high power density DC/DC converters with the integrated system module approach. An example is the Vicor product range, which consist of DC/DC converters for a range of applications and power ratings. Such a DC/DC converter module is illustrated in Figure 2.10 [2-23]. The ISM contains the complete power converter system including the power devices, passive components, the control, the protection and in some modules, electrical isolation. The modules are self-driven, self-contained and self-protecting. Generally the power modules do not include the necessary EMI filters required to comply with


**Figure 2.10. A DC/DC converter implemented as an ISM [2-23]**

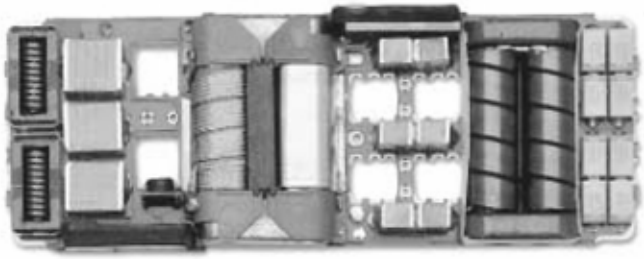


**Figure 2.11. A view of the open ISM [2-24]**

EMI standards. However, techniques such as ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching) are employed to reduce the noise generated. Separate filter modules are available for EMI compliance.

The internal construction of a Vicor ISM is illustrated in Figure 2.11 [2-24]. The figure shows the internal configuration of an ISM with electrical isolation between the two DC terminals. The high frequency transformer and inductors can be seen in the figure. It can be noticed that the inductors and transformer are implemented with a unique core shape to minimise the components volume, not only the electromagnetic volume but also the volume required to connect to the remainder of the circuit. The shape of the passive components is also manipulated to ensure adequate heat flow from the components to the base plate below the components. Six power semi-conductor devices can also be seen.

The power rating of the power modules is generally limited by thermal considerations of the components and the environment. Though the power rating may be limited, modules with very high output current ratings are available, for example 80A at 2V. The maximum operating temperature of such power modules is normally about 100°C [2-23][2-24].

### *2.2.5 Trends in power electronic module development*

The development of power electronic modules has been illustrated by way of several examples. The trends that can be identified can be summarised as follows:

i. As the power electronic module has developed, the functionality in the module has increased significantly for the given power range. Power electronic modules have progressed from single and multiple power devices in a single module to the complete power conversion system integrated into the module while still retaining some flexibility. The use of microcontrollers and microprocessors make implementing significantly more functionality into the modules possible without the penalty of

volume. Power electronic modules are implemented in a range of applications from DC to DC conversion to motor drives over a large power range, illustrating their versatility.

ii. Currently the trend in realising power electronic modules is to implement the power stage with bare die semi-conductors interconnected with wire bonding or similar interconnect technology on a substrate with high thermal performance. The additional intelligence that is integrated into the module is usually implemented on a more conventional circuit carrier, such as PCB and is mounted in the module in such a way as to be thermally disconnected from the power stage. This trend is seen over most of the application and power ranges.

iii. The power density of the systems implemented with power electronic modules has improved as the level of integration in the modules has increased. Integrating the gate drives and protection into the module alleviates the system control from the task, allowing other functions to be implemented or the system to be implemented in a smaller volume. As the integration trend increases, less and less additional volume outside the module needs to be devoted to controlling and protecting the modules, freeing more space and resources for other functions.

iv. In addition to freeing volume, integrating the auxiliary functions into the power electronic modules also saves the design engineers both time and cost. Time is saved since less of the system must be developed due to it already being implemented in the module and cost is saved through the standardisation of the power stages. As the integration trend increases, less auxiliary circuitry will be required to implement the power electronic module in a system, thereby reducing cost and development time.

v. As the level of functionality increases in a power electronic module, the module becomes more application-specific and loses its flexibility. Commercial modules try to retain a level of flexibility by making the voltage and current range over which the modules function as large as possible.

vi. The thermal performance of the power electronic module is limited by the materials or components within the module with the lowest maximum allowable temperature. As the level of functionality in power modules has increased, so the maximum operating temperature of the modules has decreased. The circuit implementing the module's intelligence must operate in the same ambient environment as the power stage, even though it is thermally decoupled from the power stage. Thus the implementation of the intelligence, if additional thermal measures are not taken, can limit the maximum operating temperature of the power electronic module.

## 3. Taking power modules into the future

By extrapolating the current development trends and shortcomings of the power electronic modules, it is possible to make a projection of the future developments in the power electronic modules for similar applications.

The future power electronic module will be based on the ISM concept, which integrates the power electronics, intelligence and diagnostics into a single structure with ever-increasing power density and operating temperature. The ISM offers the greatest level of integration and can still be relatively flexible. Figure 2.12 shows the development of the future power modules based on the ISM. There are six primary fields of development identified surrounding the power electronic module. Each represents a requirement that must be met by the future power module.

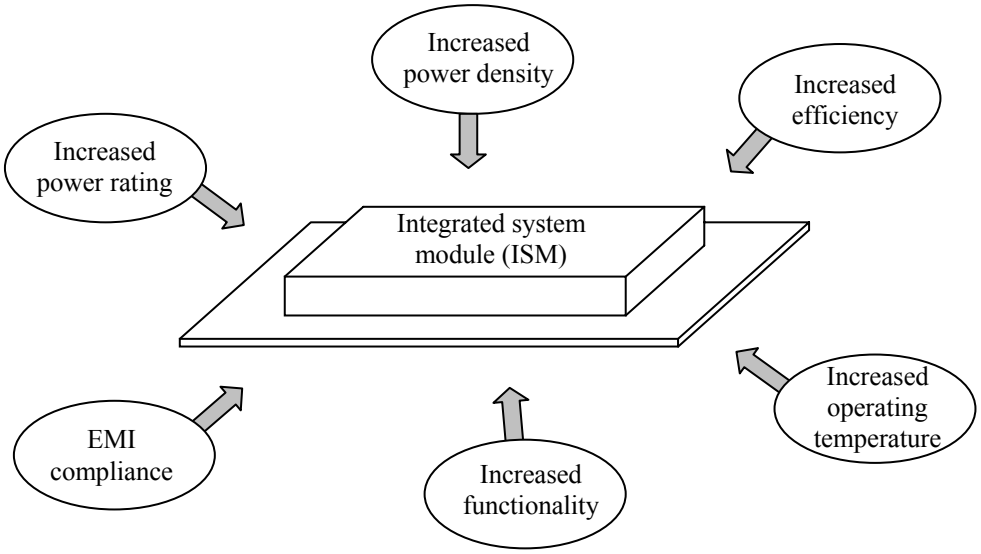



**Figure 2.12. Future requirements of power electronic modules**

The primary fields of development for the future ISM are:

i. *Increased power density*. Driven by applications where volume is becoming an increasingly rare commodity, the power density of the future power electronic modules will continue to increase. Typical examples include the automotive and avionics industries. Even in systems where the overall power density is not a primary driver, the high power density ISM will make space available for other functions to be implemented in. The power density of current ISM systems is typically in the order of 3kW/dm$^3$ (50W/in$^3$) to 4.5kW/dm$^3$ (75W/in$^3$). There are a few examples of higher power densities but they are usually limited to high current and very low voltage (≈2V) applications.

ii. *Increased efficiency*. The efficiency of the ISM must increase if the power density is to increase. The volume of the thermal management depends on the amount of heat dissipated in the module and contributes significantly to the ISM volume. Reducing the losses also reduces the thermal stresses that the components within the ISM must endure, making it possible to perform the same electrical function with smaller components.

iii. *Increased operating temperature*. The operating temperature of the future ISM must increase to remain flexible and to achieve a higher power density. Current ISM systems typically have maximum operating temperatures of either 85°C or 100°C. Generally, the power electronics implemented within the modules have higher maximum operating temperatures, while the passive components that are required to fulfil the energy storage functions have lower maximum temperatures. These are the components that limit the maximum operating temperature of the modules. The reduced maximum operating temperature also limits the environment in which the ISM system can be implemented in. For example, in the automotive environment, the engine coolant is used to cool the power electronics but the coolant has a maximum temperature of 125°C. If the ISM cannot operate with this coolant, then it will more than likely not be implemented in the automotive environment irrespective of the power density and efficiency.

iv. *Increased functionality*. The functionality of the future ISM will continue to increase. This is primarily because most of the intelligence functions can be implemented in

microcontrollers or microprocessors and these can be integrated into the ISM with relative ease and with almost no additional volume.

v. *EMI compliance*. EMI compliance is a major concern for all electronic equipment and systems. This is also true for current and future ISM. EMI compliance will become a minimum requirement for future ISM systems. The EMI filters necessary to meet the EMI requirements will be integrated into the modules.

vi. *Increased power rating*. The current power rating for ISMs is relatively low: it is limited to a few hundred watts, with few examples in the low kilowatts. The limitation is primarily due to the thermal limitations of the passive components within the ISM. For the power rating of the modules to increase, the thermal management of the passive components requires significant improvement. The power rating of future ISMs will increase, increasing the application range.

The development of the future ISM is highly dependent on the heat dissipated in the module and how the heat is removed from the module. All of the above fields of development, with the exception of EMI compliance, are affected directly or indirectly by the dissipated heat and accompanying thermal management. Thus it stands to reason that enhancing the thermal management and minimising the heat dissipated in the module will be central to the development of the future power electronic modules.

# 4. The 3D integrated system module for automotive application

In the previous two sections of this chapter the evolution of the power electronic module was considered and predictions were made at to the future development of the power electronic module. In this section of the chapter an application for the future ISM is considered. The application is the automotive converter that was introduced in the previous chapter.

## 4.1 The ISM as the automotive converter

The automotive converter, introduced in the previous chapter, has many requirements and, on the bases of the specifications outlined in the previous sections of this chapter, can be completely satisfied by the future ISM. The automotive converter requirements can be summarised as:

i. high power density,
ii. high operating temperature,
iii. high efficiency,
iv. high level of intelligence – integrated control, protection and diagnostics and
v. EMI compliance

which correspond very well to the capability of the integrated system module.

In addition, the automotive converter has a power rating of 2kW (higher power rating) and is bi-directional (increased functionality), completing the commonality between the automotive converter and the ISM. This illustrates that the ISM is indeed a viable solution for implementing the automotive converter.

## 4.2 Boundary conditions imposed on the ISM by the automotive environment

The boundary conditions imposed on the ISM by the automotive environment have significant consequences for the design and implementation of the module.

### *4.2.1 The automotive environment*

The automotive environment, specifically the engine compartment of the passenger vehicle, is

an electrically and thermally harsh environment – as illustrated in the previous chapter [2-25] [2-26]. The engine coolant is used to cool the electronic systems implemented in the passenger vehicle's engine compartment and can have a nominal temperature of typically between 85°C and 90°C but can reach temperatures as high as 125°C under pressure. In addition there is very little volume available in the engine compartment in which to implement the automotive converter. With all the new functionality of modern passenger vehicles, unused volume is scarce.

### *4.2.2 Assumptions*

The following assumptions, based on the automotive environment, can be made for the automotive DC/DC converter implemented as an ISM:

i. All the heat dissipated in the ISM must be collected and conducted to the base plate, also referred to as the thermal interface, where it is transferred to the environment. Only thermal conduction can be used to transport the dissipated heat from the heat source to the thermal interface. Thermal radiation and convection cannot be used to implement the necessary thermal management because the location and orientation of the module within the passenger vehicle is unknown. It is not known if the module will be mounted in an air stream or directly on the engine block. Thus, it is assumed that all the heat dissipated in the ISM will be transferred to the environment only through the thermal interface.

ii. It is further assumed that the automotive ISM will be mounted on a liquid-cooled surface and that this surface can be treated as an infinite heat sink. It is assumed that the temperature of the liquid cooler is fixed and is determined only by the engine cooling system. This assumption can be justified by considering the heat capacity of the engine cooling system. The heat that the power converter dissipates in the cooling system is significantly less than what the engine dissipates in it and will not be sufficient to change the coolant's temperature.

Figure 2.13 illustrates the automotive ISM with the surrounding boundary conditions. The dissipated heat is collected and transferred to the environment only through the thermal interface as illustrated. Power can flow in both directions in and out of the module. In the figure, $P_{14}$ represents the power flowing in the 14V bus and $P_{42}$ in the 42V bus. There is also a bi-directional communication channel between the ISM and the vehicle overhead controller.

The automotive ISM uses only thermal conduction to transport the heat dissipated within the module to the thermal interface. From the thermal interface the heat must be exchanged with

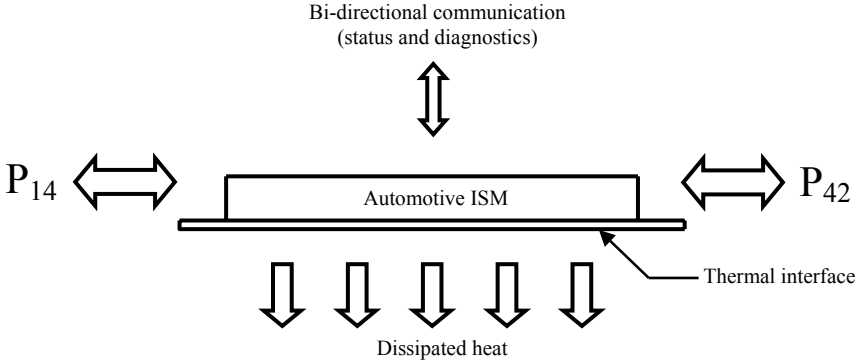



**Figure 2.13. The boundary conditions surrounding the ISM implementing the automotive DC/DC converter**

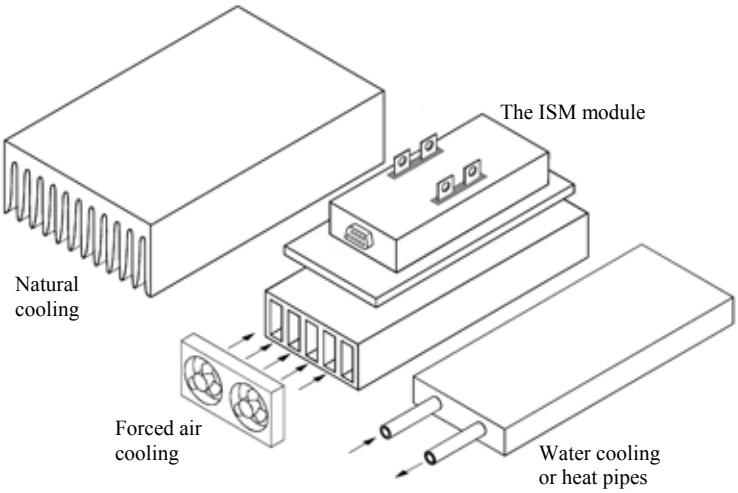



**Figure 2.14. The automotive integrated system module**

the environment. Figure 2.14 illustrates how this can be achieved with the ISM. Since all the dissipated heat is available on a single surface, natural convection, forced convection or even water cooling can be used to transport the dissipated heat to the environment. This means that there is a degree of freedom as to the ISM's positioning and orientation within the larger system.

### 4.3 Making it possible

The design of the automotive ISM is driven primarily by the power density and the high operating temperature requirements. To achieve both of the requirements simultaneously and in the same volume requires that the electrical design, the spatial design and the thermal design of the module must all be optimised for simultaneously and in the same volume.

The power density and operating temperature each have their own requirements on the electrical, thermal and spatial designs. Further, there is significant interaction between the three designs. To optimise the electrical, thermal and spatial designs in the same volume and to meet the power density and operating temperature simultaneously, the interactions between the designs must be investigated and understood. It will then be possible to exploit the interactions to achieve the power density and operating temperature requirements in the ISM. This is the focus of the following chapter. The consequences of the high power density and high operating temperature on the electrical, thermal and spatial designs are considered and the interaction between the three designs is defined.

## 5. Summary

In Chapter 1, designing and implementing the automotive converter as a self-contained module was identified as one of the central themes to the thesis. In this chapter, the development of power electronic module is considered. Several module concepts that could be used to implement the automotive converter are identified. These are considered in section 2.1 and are summarised as:

i. The power module (PM)
ii. The intelligent power module (IPM)

iii. The integrated intelligent power module ($I^2PM$)
iv. The integrated system module (ISM)

Each of the above power electronic module configurations is considered in section 2.2, which provides examples of the implemented modules.

With the development of the power electronic modules considered, some of the development trends can be identified. These are considered in section 2.2.5. Using the identified trends, projections into the future of the power electronic modules can be made and are considered in section 3. It is seen that the ISM is the most suitable candidate for future development due to the high level of functionality and intelligence inherent to the module.

In section 4, the ISM is considered for implementing the automotive converter. The ISM is selected because the complete energy conversion process along with the control, protection and diagnostics can be integrated into a single self-driven, self-contained module. To this end, the boundary conditions that the automotive environment impose on the implementation of the ISM along with the implementation assumptions are considered in section 4.2.

In section 4.3, how to meet both the high power density and high operating temperature requirements of the automotive ISM is briefly considered. The electrical design, the spatial design and the thermal design of the module must be optimised simultaneously and in the same volume. To achieve this the interactions between the three designs must first be considered. This is investigated in Chapter 3.

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# Chapter 3

## INTERDEPENDENT ELECTRICAL, THERMAL AND SPATIAL DESIGN OF A POWER MODULE

## 1. Introduction

In the previous chapter, the integrated system module containing the complete power processing system (both active and passive components) as well as the control, diagnostics and protection system were introduced and considered for the automotive application. The previous chapter concluded by identifying which design aspects must be investigated to make the automotive integrated system module possible. These issues are addressed further in this chapter.

This chapter considers the interdependence between the electrical, thermal and spatial designs that must be considered simultaneously if the ISM is to have both a high power density while being capable of operating in a high temperature environment.

This is done by first considering what the requirements of a topology are, and how this topology has to be implemented in order to achieve a high power density and operate in a high temperature environment. This is addressed in section 2. The contradictions between the two sets of requirements are also identified.

With this in mind, the relationship between the electrical, thermal and spatial designs of the ISM are considered and defined in section 3. Interactions and trade-offs between the three designs are identified and considered with respect to their consequences in the electrical, thermal and spatial designs.

In section 4 the manipulation of the design interactions is considered as a means to achieve the desired objectives. This is done with the aid of the identified trade-offs.

In the last section of the chapter the optimisation of each of the designs is briefly considered. These will be considered in the following three chapters in detail and this section serves only as an introduction to these chapters.

## 2. Design requirements for high power density and high operating temperature

Before a high power density power module for high ambient temperatures can be designed, the requirements that the ISM must meet to achieve this end must be considered. These requirements are broken down into two sets, namely the high power density requirements and the high operating temperature requirements. Each is considered in the following sections.

### 2.1 High power density design requirements

Let Figure 3.1 represent a generic integrated system module. The module has three ports of

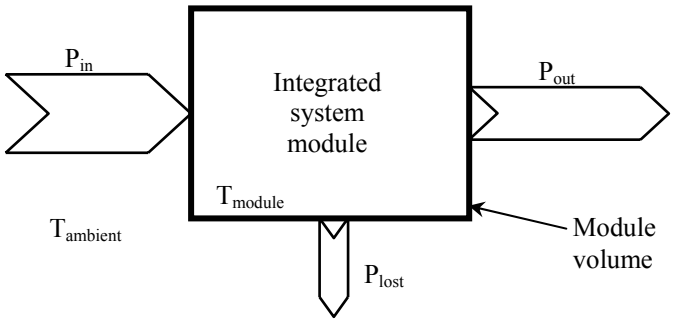


**Figure 3.1. A generic representation of an ISM**

interest. The first is the power input port on the left of the figure, the second is the power output port on the right of the figure and the third is the power lost port. The power entering the module is equal to the sum of the powers exiting the module. The input and output power can have different characteristics (voltage and current values) though both are electrical ports. The ISM requires volume to change the characteristics of the input power to that desired at the output while minimising that which is lost. The volume occupied by the ISM is determined by, amongst other things, materials, construction techniques, the thermal management and the implemented topology. The module operates in the environment with an ambient temperature of $T_{ambient}$ while having a temperature of $T_{module}$ that is determined by the construction of the module, the losses dissipated within the module, the thermal management and $T_{ambient}$.

To design an ISM with a high power density, the concept of power density must first be defined. The power density of the module in Figure 3.1 is defined as the ratio of electrical power delivered from the module ($P_{out}$) to the total volume occupied by the module [3-1]. Mathematically the power density is defined as:

$$Power\ density = \frac{P_{out}}{\psi_{total}} \tag{3.1}$$

where *Power density* is measured in [W/m$^3$],
$P_{out}$ is the electrical power delivered from the module [W]
and $\psi_{total}$ is the total volume of the module required to perform the power conversion [m$^3$].

The power density is a figure of merit that relates how much power is being processed or converted in the available volume. The power density does not make any reference to the heat being dissipated ($P_{lost}$) in the module or operating temperature of the module.

Increasing the power density of the ISM can be achieved by:

i. Increasing the power delivered from the module and/or
ii. Reducing the modules volume for a given power rating.

### *2.1.1 Increasing the delivered power*

To increase the power density of the ISM, the power delivered from the module must be increased while at least maintaining the module's volume. Increasing the modules delivered power can be achieved by either increasing the module's efficiency if the input power is fixed, or increasing the switching frequency for a given energy density.

### *2.1.1.1 Increasing the efficiency*

Increasing the integrated system module's efficiency requires that the losses in both the active and passive components be reduced for a given power rating. This can be achieved through the appropriate choice of the power converter topology and implemented components. In addition, there are several techniques that can be used to help further increase the topology's efficiency. Examples include interleaving of multiple phases, resonant topologies and soft switching techniques [3-2]. These techniques all come at the cost of additional components that could result in a penalty in the implemented topology volume.

As part of increasing the topology efficiency, the stresses in both the active and passive components must be considered. The component stresses are an indication of how hard the component must work for a given set of operational and environmental parameters. For example, high component stresses resulting from large RMS currents in the passive components or large losses in switching devices can result in high component temperatures and large component volumes, reducing the power density of the ISM. A typical example of a component stress reduction technique for passive components is interleaving while for active components, soft switching. Two examples of soft switching cells, namely a zero-voltage-switching (ZVS) cell and a zero-current-switching (ZCS) cell, are illustrated in Figure 3.2 [3-3][3-4].

The two switching cells reduce the switching losses in the switching device for a given set of component and operating parameters. The first cell, the ZVS cell, does this by ensuring that the voltage across the switching device is zero while the device is turned on or off [3-3]. This is normally achieved with an auxiliary circuit of a resonant nature. The second cell is the ZCS cell. This circuit reduces the switching losses by ensuring that the switching device current is zero when the device is turned on or off. Again this is achieved with an auxiliary circuit that is resonant in nature.

Both circuits in Figure 3.2 require an additional auxiliary circuit to achieve the resonant behaviour of the switching device voltage or current required to reduce the device's switching losses. Under certain conditions it is possible for the RMS currents in the additional resonant components to become significantly large, increasing the passive component stresses. When using techniques such as these, care must be taken to avoid the uncontrolled redistribution of losses between the components.

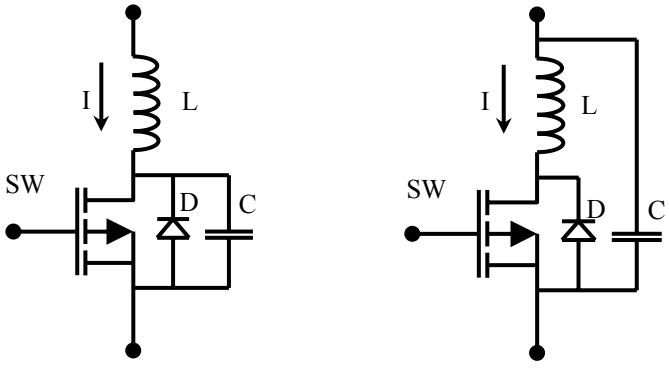


**Figure 3.2. A typical implementation of a ZVS cell (left) and a ZCS cell (right)**

#### *2.1.1.2 Increasing the delivered power*

The power delivered by the module can be written as [3-5]:

$$P_{out} = E_{cycle} \cdot f_s \tag{3.2}$$

where $P_{out}$ is the output power [W],
$E_{cycle}$ is the energy delivered per switching cycle [J]
and $f_s$ is the switching frequency [Hz].

The energy delivered from the power module per switching cycle is determined by the passive component materials, their geometries and the topology in which the components are implemented. This fixes the energy density of the passive components. If the switching frequency of the topology is increased with the same energy density in the passive components, the output power of the module can be increased. However, it must be remembered that changing the switching frequency of the topology while maintaining the passive components energy density results in a change in the energy delivered per switching cycle. Thus doubling the switching frequency does not necessary imply a double in the output power though the output power will be increased.

Increasing the switching frequency also increases the losses in the module. The switching device's switching losses are linearly proportional to the operating frequency, while the passive component's losses tend to increase exponentially with frequency. Thus a balance is reached where the gain in delivered power is traded off against the gain in losses. Circuit manipulation techniques such as soft-switching and interleaving can be used to manipulate the trade-off.

### *2.1.2 Reducing the required volume*

To further increase the power density of the ISM, the volume of the module must be reduced for a given output power. This can be achieved in several different ways or combinations thereof.

#### *2.1.2.1 Increasing the loss density*

The loss density of a component is defined as the ratio of the losses or heat dissipated in the component to the volume of the component. Mathematically the loss density of a component is defined as:

$$Loss\ density = \frac{P_{component}}{\psi_{component}} \tag{3.3}$$

where *Loss density* is measured in [W/m$^3$],
$P_{component}$ is the losses or heat dissipated in the component [W]
and $\psi_{component}$ is the volume of the power component [m$^3$].

The loss density can be determined for individual components, such as inductors, capacitors and switching devices, as well as for systems such as the integrated system module. The loss density is a figure of merit that gives an indication of how much power is dissipated in a given volume but makes no reference to temperature. The maximum achievable loss density is limited by the maximum allowable temperature in the volume. For high power density applications it is desirable to have loss densities as high as possible in both the components and

the system while not exceeding the maximum allowed temperature because then the given volume is dissipating the maximum amount of heat possible.

The loss density of a component or a system is increased in one of two ways. First, the volume of the component or system is kept constant while the heat dissipated therein is increased. The increase in the dissipated heat in both the components and the system is achieved by increasing the components excitation within the material's thermal and electromagnetic limits. Alternately the volume of the component or system is decreased for a given heat dissipation or a given component excitation.

Increasing the loss density is a means of reducing the component's or system's volume provided the material limits are not exceeded. For a high power density application, the preferred means of increasing the loss density is maintaining the level of electrical excitation while reducing the implementation volume (resulting in an increase in the electromagnetic excitation), within the material's capabilities.

#### *2.1.2.2 Reducing the stored energy in passive components*

The volume of passive components is largely determined by the volume required to store the electromagnetic energy (dielectric or magnetic material) and the volume required to establish the electromagnetic fields (inductor windings or capacitor plates). If less energy is to be stored in the component, then the volume required to store and/or establish the required electromagnetic fields can also be reduced, reducing the component's total volume.

Consider an inductor for example. The energy stored in the inductor can be expressed in terms of the geometric and material properties of the materials used to implement the inductor as the area product. The area product is the product of the winding window area and the core area and is written in terms of the inductor material and excitation parameters as [3-3]:

$$A_c A_w = \frac{2E_{inductor}}{B J k_{fill}} \tag{3.4}$$

where $A_c$ is the area of the core [$m^2$],
$A_w$ is the area of the winding window [$m^2$],
$k_{fill}$ is the winding window fill factor ($\leq 1$),
$B$ is the magnetic flux density [T],
$J$ is the current density in the winding [$A/m^2$]
and $E_{inductor}$ is the energy to be stored in the inductor [J] and is given as:

$$E_{inductor} = \frac{1}{2} L I^2 \tag{3.5}$$

where $L$ is the inductor's inductance [H]
and $I$ is the maximum inductor current [A].

The area product of the inductor can be used to estimate the inductor's volume for a given thermal management arrangement [3-6]. It is clear from equation 3.4 that if the volume of the inductor is to be reduced then the area product must be reduced. To reduce the area product either the energy stored in the inductor must be reduced or the current density and/or magnetic flux density must be increased. The magnetic flux density is limited by material properties and the current density is limited by loss and thermal considerations.

A similar argument can be presented for capacitors.

#### *2.1.2.3 Component count*

The component count of a topology is a measure of how many physical components are required to implement the topology. From a high power density perspective, it is generally desirable to have a topology with a low component count as well as having reduced component stresses.

A low passive component count is desired because each component requires volume, not only to establish the electromagnetic fields and for the stored electromagnetic energy but also for the interconnections between the component and the circuit carrier. The interconnections between the component and the circuit carrier are often a source of unusable volume in addition to circuit parasitics. The parasitic inductance due to capacitor leads is an example.

It is also desired to keep the number of active components as low as possible. Active components, though they can be implemented in very small volumes, usually require a large overhead to make them functional, for example, the gate drive circuit and the thermal management required to remove the device losses all require volume. In addition, the parasitics that are associated with active components are a source of losses and EMI compatibility issues.

The component count can be reduced by either selecting a topology with a low component count, or making use of concepts such as component or electromagnetic integration to reduce the number of physical components used to implement a topology.

#### *2.1.2.4 Improved volume usage*

In the practical implementation of any converter there is always unused volume, up to as much as 55% in typical commercial converters [3-7]. If this volume can be effectively used for either thermal management or electrical power processing, the power density of that particular converter can be significantly improved. Figure 3.3 shows an implementation of a typical power module containing only the power semi-conductors and the connection from outside the power module to the semi-conductors [3-8]. The figure shows clearly how much volume is unused within such a power module. If this volume can be utilised, significant improvements

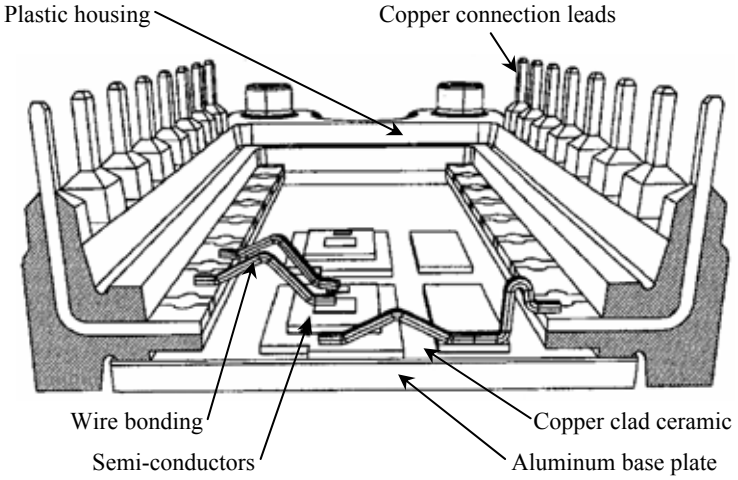


**Figure 3.3. A open sectioned view of the internal structure of a conventional power module containing only the power semi-conductors [3-8]**

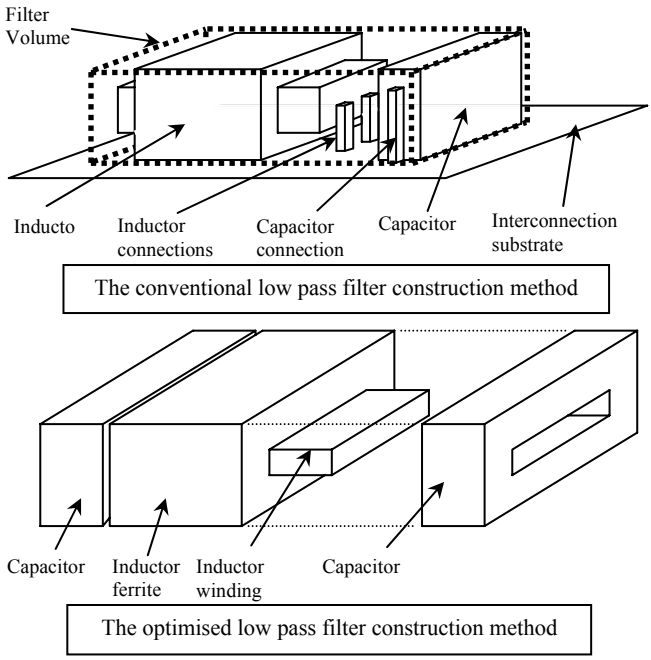


**Figure 3.4. The volumetric optimisation of a low pass filter to increase the power density [3-6]**

in the power density can be made.

In the case of conventional converter structures, the unused volume within the converter exits primarily for two reasons:

i. All of the components in a power converter are manufactured independently and without any thought for the other components used to implement the power converter. The result is that the components have a wide variety of shapes and sizes that are generally geometrically incompatible with each other [3-6][3-9].
ii. The components are generally all implemented on the same plane as the circuit carrier (either DBC or PCB for example), making the implementation two-dimensional in nature [3-10].

These two reasons tend to place significant limitations on the achievable power density. This can be overcome by designing the components in the power converter to fit together more compactly with less wasted space between them. Component shapes can be changed so that they match and complement each other. An example of this approach can be found in reference [3-6] where the volume of a low pass filter is minimised by manipulating the shape and positioning of the inductor and capacitor. The concept is illustrated in Figure 3.4.

A second option is to exploit a three-dimensional approach to implementing the topology. Exploiting the third dimension to implement the topology results in more freedom for the component shapes and removes the two-dimensional limitation placed on the location and positioning of the components due to the circuit carrier. If the components are no longer limited to the two-dimensional construction method, a lot of previously unutilised volume can be used. This can significantly improve the ISM power density [3-11].

#### *2.1.2.5 Increased operating frequency*

It has already been seen that increasing the operating frequency can lead to an increase in the power delivered from the ISM. Alternatively, increasing the operating frequency can also lead to a reduction of the ISM volume while maintaining a constant output power.

If the output power is kept constant and the operating frequency is increased, then the energy delivered per switching cycle can be reduced. A reduction in the energy delivered per switching cycle implies that less energy needs to be stored in the passive components, allowing the components' volume to be reduced within the material limitations. Thus increasing the operating frequency can lead to reducing the components' volume and thereby help to improve the power density.

## 2.2 High operating temperature design requirements

Operating in an environment with a high ambient temperature places many demands on the ISM. The thermal system for the ISM is illustrated in Figure 3.5, which shows an arbitrary component in the ISM operating at a temperature $T_{component}$ that is $\Delta T$ degrees above the thermal interface temperature of $T_{environment}$. The thermal interface is considered the environment because all of the dissipated heat is transferred to the surrounding environment through the thermal interface. The demands placed on the thermal design of the ISM to operate at a high temperature are considered in the following section.

### *2.2.1 Reducing the $\Delta T$ between heat source and heat sink*

The $\Delta T$ referred to in Figure 3.5 is the temperature difference between the environment temperature and the highest temperature in the component. All components have a maximum temperature that cannot be exceeded if the component is to function correctly. In a high temperature environment, this maximum temperature becomes more critical because the temperature difference, the $\Delta T$ between the environment and maximum temperature, can become small. Hypothetically let there be an aluminium electrolytic capacitor in the ISM. If the power module is to operate in an environment where the thermal interface temperature is 125°C and the capacitor has a maximum temperature rating of 150°C, then the maximum allowable $\Delta T$ is only 25°C. All the heat dissipated in the capacitor must be removed from the component and transported to the environment within an absolute maximum temperature rise of 25°C in the capacitor.

The small allowable temperature drop places many restrictions on both the electrical and the thermal operation of the component. Furthermore, the choice of which components to use

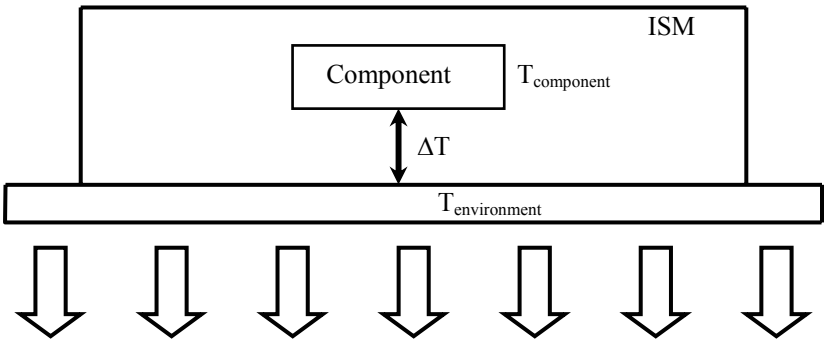


**Figure 3.5. A generic description of the thermal system for the ISM**

becomes significantly more critical. For example, the high temperature environment severely limits the use of aluminium electrolytic capacitors as bus capacitors.

The temperature drop within the IMS from the heat source to the base plate which is the thermal interface to the environment can be derived from Fourier's law for thermal conduction [3-3]:

$$\bar{q} = -k\nabla T \tag{3.6}$$

where $\bar{q}$ is the heat flux vector [W/m$^2$],
$k$ is the material thermal conductivity [W/m·°C]
and $\nabla T$ is the divergence of the temperature field [°C/m].

Simplifying and rewriting in one dimension, equation 3.6 can be written in terms of the thermal resistance as:

$$R_t = \frac{T_{heat\ source} - T_{environment}}{Q} = \frac{\Delta T}{Q} \tag{3.7}$$

where $R_t$ is the effective thermal resistance between the heat source and thermal interface [°C/W],
$T_{heat\ source}$ is the maximum temperature in the component [°C],
$T_{environment}$ is the environment temperature to which the dissipated heat is transported to (the thermal interface temperature) [°C],
$\Delta T$ is the temperature difference [°C]
and $Q$ is the heat being dissipated by the heat source [W].

To reduce the temperature drop between the heat source and the environment, either the thermal resistance or the dissipated heat or both must be reduced.

### *2.2.2 Improving heat removal*

The effectiveness at which the dissipated heat is transported between the heat source and the environment can be significantly improved on by improving the thermal properties of the materials and the geometries of the thermal management structure.

Consider, for example, a one-dimensional heat conductor with a cross-sectional area of $A$, a conduction length of $L$ and a thermal conductivity of $k$. The thermal resistance of the one-dimensional heat conductor can be expressed in terms of the structure geometry and material properties for thermal conduction as [3-3]:

$$R_t = \frac{l}{k \cdot A} \tag{3.8}$$

where $l$ is the length of the heat path [m],
$k$ is the thermal conductivity of the material [W/m·°C]
and $A$ is the cross-sectional area of the heat path [m$^2$].

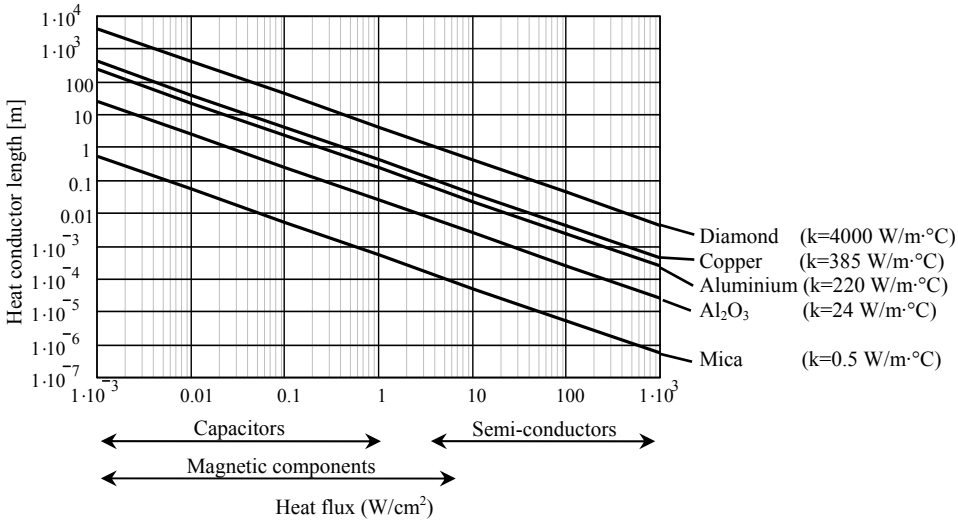


**Figure 3.6 The length of different thermal conductors with a cross-sectional area of 1cm$^2$ and a temperature drop of 10°C for typical heat flux values**

To reduce the thermal resistance between the heat source and the thermal interface, the distance that the dissipated heat is transported must be minimised while the area perpendicular to the heat flow must be maximised. This requires the manipulation and optimisation of the thermal management structure. Increasing the thermal conductivity can be achieved by using a different material. This is often the easiest way to make significant improvements to the thermal resistance.

To illustrate the effect of the thermal conductivity, consider Figure 3.6. The figure shows the length of a one-dimensional thermal conductor comprised of different materials for a fixed $\Delta T$ of 10°C and a fixed conduction area of 1cm$^2$. A typical range of values for the heat flux density is used based on the different electrical components. The figure shows that the length of the thermal conductors can vary significantly with the thermal conduction coefficient and can have lengths as small as 1μm or as long as 4km for a typical range of heat flux values. This is highly impractical but it demonstrates very well the effect that the material choice has on the transportation of the heat between the heat source and the environment.

### *2.2.3 Reducing the losses in components*

If equation 3.7 is considered again, it can be seen that the temperature drop between the heat source and the environment can be further reduced if the heat dissipated in the heat source is reduced for a given thermal resistance.

For passive components the reduction of losses can be achieved by either reducing the energy lost in establishing and maintaining the required electromagnetic fields for a given excitation or by an increase in the volume in which the energy is stored in and fields established. This reduces the level of material excitation per unit volume. In either case, the heat dissipated in the component for the same excitation is reduced. This results in a decrease in the component's loss density.

## 2.3 Contradictions in the design requirements

The design requirements for the high power density integrated system module operating in a

high temperature environment have been considered. If all of these requirements are considered simultaneously, so as to meet them all in a single volume, contradictions between the requirements can be identified.

The most obvious contradiction is the opposing requirements on the loss density of the components within the ISM. To achieve a high power density, the loss density of the components must be made as high as possible for the required excitation within the material and thermal limits. The high loss density ensures that the component volume is at a minimum, improving the power density of the module.

For operation in a high temperature environment, the loss density of the same components in the ISM must be low. A low loss density ensures that the temperature drop between the highest temperature in the component and the environment is small. This is required so that the component can function safely in a high temperature environment without being damaged.

Contradictions such as this must be overcome to implement a high power density integrated system module that is to operate in a high temperature environment.

## 3. Interdependence of the power module design

In the previous section, it was seen that in order to design an integrated system module with a high power density and capable of operating in a high temperature environment, many requirements must be met. These requirements are spread out over the electrical, the spatial and the thermal design domains. Meeting all of these requirements in a single structure simultaneously requires that careful attention is given to how these requirements interact with each other. This is considered in the following section.

To design the ISM in three-dimensional space, the electrical design, the thermal design and the spatial design must be considered simultaneously if the high power density and the high operating temperature requirements are to be met in the module [3-9]-[3-15]. The integrated electrical, spatial and thermal design strives to achieve a packaging solution that has the following characteristics:

i. Meets the terminal conversion requirements at full power (electrical design)
ii. Operates in the desired ambient temperature (thermal design)
iii. Meets the density or volume requirements (spatial design)

To achieve this result, all of the designs must be optimised for the individual design specifications simultaneously. The three designs are tightly interconnected and any change in one design will have consequences for the remaining two. The relationship between the electrical, the spatial and the thermal designs can be graphically illustrated as in Figure 3.7.

The figure shows the three design domains each with their own set of specifications. The three design domains are each connected to the remaining design domains with bidirectional arrows. These bidirectional arrows represent the interactions present between the three designs.

The interactions between the design domains can be summarised as follows:

i. *Dissipated heat*. The interaction between the electrical and thermal designs is through the heat dissipated in the components in the implemented electrical topology. The dissipated heat must be transported from the heat source to the environment in the thermal design.

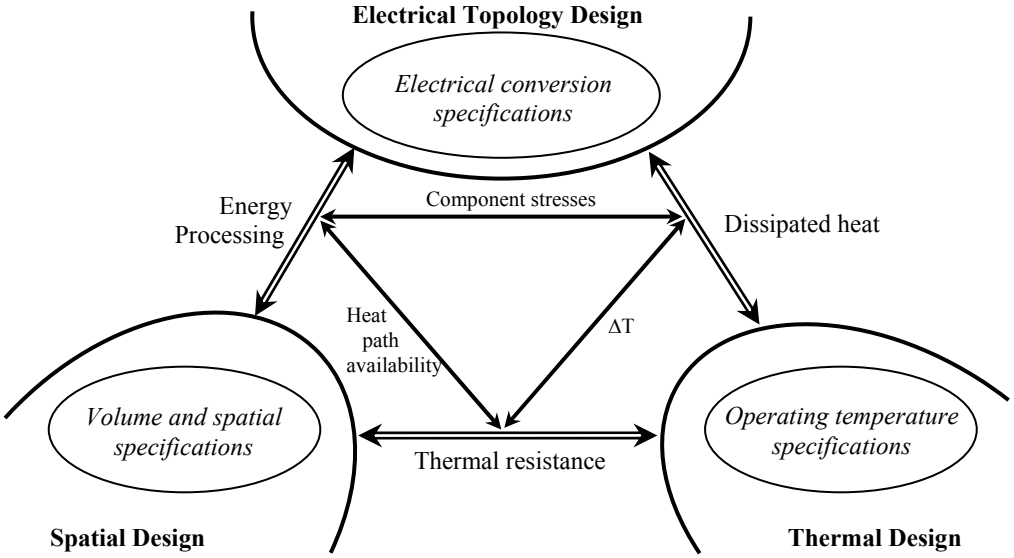


**Figure 3.7. The relationship between the electrical, thermal and spatial design domains**

ii. *Energy processing*. The interaction between the electrical and the spatial designs is through the volume required to establish the electromagnetic fields and to store the electromagnetic energy in the components used to implement the electrical topology.

iii. *Thermal resistance*. The interaction between the spatial and the thermal designs is through the volume and geometry required to establish the required thermal resistance.

Within the triangle created by the design interactions is a second triangle. This triangle represents the trade-offs between the design interactions. The three trade-offs can be summarised as:

i. *Component stresses*. This is the trade-off between the heat dissipated in the components in the topology and the energy that the components must store/process.

ii. $\Delta T$. This is the trade-off between the heat that the electrical topology dissipates into the thermal management structure and the thermal resistance established by the volume and geometry of the thermal management structure.

iii. *Heat path availability*. This is the trade-off between the volume that is used to implement the thermal management structure and the volume required to establish and store the electromagnetic energy.

The identified design interactions and the trade-offs are considered in the following sections.

## 3.1 Electrical topology design

Figure 3.7 shows that the electrical topology design is coupled to the thermal design and the spatial design. The electrical topology converts the input power to the output power according to the module specifications. In doing this heat is dissipated and volume is required for the establishment and storage of energy.

The volume required to establish the electric and magnetic fields and the volume for the energy storage is coupled to the spatial design of the module as required by the electrical topology.

The required volume is made available in the module through the spatial design of the module. In order to achieve a high power density, the selected topology should minimise the amount of energy that is stored at any instant in time. Practically, this implies that a topology with a low component count and small values of inductance and capacitance is more suited to a high power density implementation than a topology with many components and large values of inductance and capacitance (for similar voltage and current ratings).

In summary, for a high power density and high temperature application, a topology is required that has a relatively low component count and has reduced component stresses. The component stresses are linked to both the thermal and spatial designs determining the $\Delta T$ between the component's hotspot and the environment, and the component's volume respectively. The component count is also directly linked to the module's spatial design through the component's volume.

### 3.2 Thermal design

The thermal management design interacts with both the spatial and electrical design of the power module, as illustrated in Figure 3.7. The thermal management must achieve an effective thermal resistance that is below the maximum allowable thermal resistance if the power module is to operate in a high temperature environment. The thermal resistance is a function of the materials' properties and the thermal management geometry, thus requiring volume within the power module to be implemented in.

In addition, the thermal management structure can either help reduce or induce additional losses in the components within the power module, linking the thermal design to the electrical design. An example could be long leads between the decoupling capacitor and a switching device because the thermal management structure forces the two components to be physically far from each other. The additional leakage inductance will result in additional overshoot voltage, which increases the switching device's losses.

In summary, to operate in a high temperature environment with a high power density, the heat that is dissipated in the power module must be minimised and effectively transported to the environment with the minimum $\Delta T$. This links the thermal design to the electrical and spatial design respectively.

### 3.3 Spatial design

The total volume of the power module is determined by the volume required to store and manipulate the electromagnetic energy and the volume required to remove the dissipated heat, as illustrated in Figure 3.7. This links the spatial design of the power module to the electrical and the thermal designs respectively.

The total volume required to store and manipulate the electrical energy is comprised of several contributors, namely:

i. the volume required for the electromagnetic functions (energy stored or processed in inductors, capacitors, transformers, switching devices etc.),
ii. the volume required to implement the electrical carrier (this is the PCB or DBC or any other carrier that is used to implement the electrical conductors),
iii. the volume required to implement the interconnections between the components and the circuit carrier (such as wire-bonding or component leads),
iv. the volume required to implement the mechanical integrity of the components (such as

transformer or inductor winding bobbins and isolation barriers),

v. the volume required for the topology control system.

These all link the electrical design to the spatial design through the volume required to implement the different functions.

The volume required for the thermal management is dependent on the type of thermal management used and the amount of heat that must be transported. For example, using thermal conduction, heat conductors with specific thermal conductivities and geometries are required. The desired $\Delta T$ then determines the minimum volume required for the thermal management.

In summary, to achieve a high power density ISM capable of operating in a high temperature environment the total combined volume of the ISM must be minimised while not exceeding the maximum allowable $\Delta T$.

## 3.4 Trade-offs between the design interactions

The discussion in the previous three sections illustrates how closely the three designs are coupled to each other. The trade-offs between the design interactions, illustrated in Figure 3.7, are a means by which the interaction between the designs can be manipulated. In this section the trade-offs between the design interactions are briefly considered.

### *3.4.1 The component stress trade-off*

In the electrical design of the power module, there is a trade-off between the energy that is stored (in a passive component) or manipulated (by a switching device) to the heat dissipated in that component. In the case of a high power density ISM, the components within the module must all be as small as possible. However, in doing this the material available to store or manipulate the required energy decreases. To meet the same electrical specifications with a smaller active volume, the excitation of the available material must be increased given the material limitations. As the material excitation is increased, so are the material losses. These losses contribute to the component stresses since they determine together with the structure's thermal management the operating temperature of the component within the power module.

The component stresses can be defined mathematically as the ratio of energy that is dissipated in the component to the energy that the component can store or process:

$$CS = \frac{E_{dissipated}}{E_{processed}} \tag{3.9}$$

where $CS$ is the component stress and is dimensionless,
$E_{dissipated}$ is the energy dissipated in the component [J]
and $E_{processed}$ is the energy stored/processed by the component [J].

The component stresses and the exact definition of $E_{dissipated}$ and $E_{processed}$ are considered further in Chapter 4. The component stress as defined in 3.9 should ideally tend toward zero. However, this is limited by material properties and geometries.

### *3.4.2 The $\Delta T$ trade-off*

In the thermal design of the power module, a trade-off exists between the heat dissipated in the

components and the implementation of the thermal management structure. The trade-off is the $\Delta T$ between the component's hot spot and the environment.

The $\Delta T$ is considered a trade-off because of the thermal management's dependence on the spatial design and its implementation in the power module. The temperature drop can experience significant changes for small variations in either the dissipated heat or spatial implementation. Manipulation of either the dissipated heat within the component or the thermal management implementation can be used to maintain or manipulate the component's $\Delta T$ to within the range that the high operating temperature requirement imposes.

### *3.4.3 The heat paths availability trade-off*

The heat path's availability trade-off is a trade-off between the volume required to implement the energy processing functions with a high power density and the volume required to achieve the desired thermal resistance for the high operating temperature requirement. Both the electrical and the thermal functions must be satisfied within the minimum combined volume while meeting the power density and operating temperature requirements.

The total volume of the power converter can be minimised by finding the combined minimum volume by trading off the volume required for the electrical and thermal functions. For example, if the electrical energy processing volume is increased, then the heat dissipated in the components can be reduced and the volume required for the thermal management can be reduced.

## 4. Manipulation of design interdependencies

In the previous section, the interdependence and the trade-offs between the three designs of the integrated system module were identified. In this section the manipulation of these interactions and trade-offs are briefly considered to meet the high power density and high operating temperature requirements of the module.

### 4.1 Increase the ISM power density

The primary objective in increasing the power density of the ISM is to reduce the volume required to implement the module in while still meeting the electrical and thermal specifications. This requires the volume of both the electrical and thermal management functions to be reduced.

The interactions and trade-offs between the three designs can be used to an advantage in increasing the power density in the following ways:

i. *Reducing the stresses in the components by manipulating the electrical topology*. The electrical topology can be changed so as to reduce the stresses in components that contribute significantly to the total volume of the topology. An example could be a bus capacitor with large RMS currents. Reducing the RMS current can lead to the bus capacitance being implemented with a physically smaller component.

ii. *Reducing the energy storage requirements of large components by manipulating the electrical topology.* Reducing the energy storage requirements of passive components, for example, can lead to smaller components. This helps to relax the power density requirements by having a smaller initial volume. Reducing the energy storage requirements can also lead to reduced losses, reducing the volume of the required thermal management.

iii. *Reducing the volume of the thermal management structure*. The volume of the thermal management structure can be manipulated in two ways, or a combination thereof:
    a. The first way to manipulate the volume of the thermal management structure is to change the topology so that less heat is dissipated in the components requiring less thermal management to remain within the allowed $\Delta T$ range.
    b. The second is to manipulate the volume of the thermal management so as to improve the thermal managements effectiveness. This involves manipulating the material properties of the materials and/or manipulating the geometry and volume of the materials used to implement the thermal management.

### 4.2 Increase the ISM operating temperature

The primary objective in increasing the operating temperature of the ISM is to reduce the temperature drop between the components and the environment. This too can be achieved through manipulation of the design interactions and trade-offs.

The interactions and trade-offs between the three designs can be used to an advantage in increasing the integrated system modules' operating temperature in the following ways:

i. *The heat dissipated in the power module can be reduced through manipulating the component stresses*. If the thermal management concept is fixed, then the heat dissipated in the components must be reduced for the required electrical specifications. This requires reducing the component stresses. The component stresses can be reduced by manipulating the topology.
ii. *The heat path availability trade-off can be manipulated to increase the volume available for the thermal management of the power module*. The volume of the thermal management can be increased, helping to reduce the effective thermal resistance between the heat source and environment. Alternatively, the material properties and geometry of the thermal management can be improved.

### 4.3 Increasing both the ISM power density and operating temperature

Several design and trade-off manipulations are listed above. However, since the module is to have both a high power density and high operating temperature simultaneously, not all of the trade-offs and manipulations are useful. A compromise between the power density and operating temperature must be established since some of the manipulations listed are contradictory to each other.

It can also be noted that for most of the manipulations between the design interactions and trade-offs, the manipulation of the topology to reduce component losses and stresses is predominant. This illustrates that the correct choice for the topology is critical in implementing an ISM with both a high power density and high operating temperature.

## 5. Design optimisation

In the previous sections of this chapter, the design requirements for the integrated system module in terms of the power density and operating temperature were considered. It was seen that if these requirements are to be met in the same module then the interactions between the electrical, thermal and spatial designs must be understood so that they can be manipulated to meet the individual thermal, spatial and electrical specifications simultaneously.

Figure 3.8 shows a summary of this process. From the high power density and high operating temperature requirements, the parameters that must be considered and optimised for can be

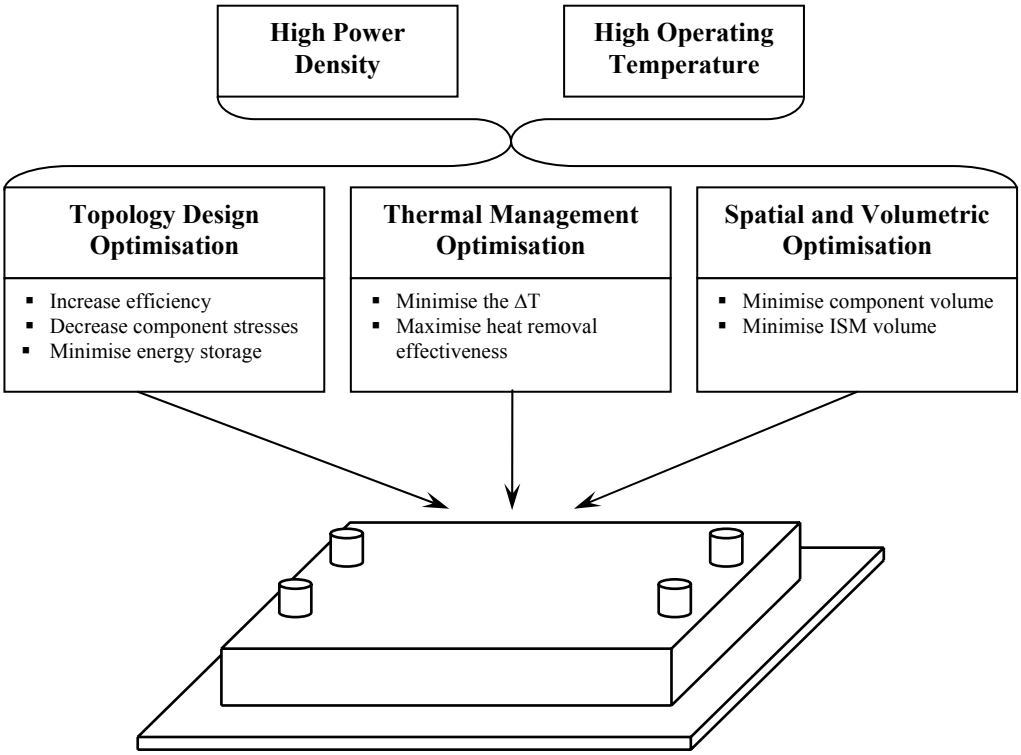


**Figure 3.8. The design optimisation requirements for the power module**

identified for the electrical, thermal and spatial designs. The optimisation of the three designs is considered further in the following three chapters of this thesis and is only introduced here.

## 5.1 Topology design optimisation

The topology design optimisation is critical to meeting the power density and operating temperature requirements in the ISM. As has been seen, the topology design has significant consequences for the both the spatial and thermal design of the module. Through manipulating the topology design, the thermal and spatial designs can be relaxed if the initial volume of the topology and the losses in the components can be minimised.

The parameters that the topology design must be optimised for are:

i. efficiency (maximised),
ii. component stresses (minimised) and
iii. energy storage (minimised).

The optimisation of the topology design for the above parameters is considered in Chapter 4 of this thesis. Additional issues are also identified and considered in the chapter.

## 5.2 Thermal management optimisation

The thermal management optimisation considers how the temperature difference between the heat source and the environment can be maintained in the allowable $\Delta T$ range allowing the ISM to operate in the high temperature environment while still achieving a high power density. The parameters that must be optimised for include:

i. minimise the $\Delta T$ between the heat source and the environment and
ii. maximise heat collection and heat removal effectiveness.

The optimisation of the thermal management design for the above parameters is considered in Chapter 5 of this thesis. Additional issues are also identified and considered in the chapter.

### 5.3 Spatial and volumetric optimisation

The spatial and volumetric optimisation of the ISM minimises the total volume required to implement the module in. The volume of the module, which determines the power density, is highly dependent on both the electrical and thermal designs as has been seen in previous sections of this chapter. To optimise the volume of the power module, the following parameters must be optimised for:

i. minimise component volume and
ii. minimise ISM volume.

The optimisation of the volumetric design for the above parameters is considered in Chapter 6 of this thesis. Additional issues are also identified and considered in the chapter.

## 6. Summary

In this chapter, the interdependence between the electrical, thermal and spatial design domains of the ISM was considered.

The design requirements for implementing an ISM with a high power density and a high operating temperature are considered in section 2. Several different methods of increasing the power density are identified in section 2.1, while those used for increasing the module's operating temperature are identified in section 2.2. Contradictions between the two sets of requirements are also identified.

Once the design requirements for a high power density and high operating temperature are established, the interdependence between the electrical, thermal and spatial designs of the power module design is considered in section 3. The three designs and the interaction between the three designs are considered in sections 3.1 to 3.3. The trade-offs between the three designs are considered in section 3.4.

With the interactions and trade-offs between the three designs identified, manipulation of the design interdependence is considered in section 4. The manipulation of the design interdependence is the means by which the high power density and high operating temperature requirements can be met in the module simultaneously.

The chapter is concluded by considering the parameters that must be optimised for in the ISM design. Optimisation parameters for the electrical, thermal and spatial designs are identified and briefly considered. The parameters identified in sections 5.1 to 5.3 form the bases of the following three chapters of the thesis. A chapter is dedicated to each section (5.1, 5.2 and 5.3) for the optimisation of the identified parameters.

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# Chapter 4

## TOPOLOGY OPTIMISATION

## 1. Introduction

In the previous chapter, the interdependence between the electrical, the thermal and the spatial design domains was considered and the relationship defined. The electrical design considers the electrical topology and identifies which parameters the topology must be optimised for in order to be able to meet the given power density and operating temperature requirements. These parameters are the topology efficiency, the component stresses and the stored energy.

However, before the topology can be optimised, a topology that is suitable to be implemented in a high power density ISM operating in a high temperature environment must be considered. This is achieved by asking two questions:

i. What are the characteristics that a topology must have to make it suitable for implementation in a high power density ISM operating in a high temperature environment?

and

ii. How can these characteristics be manipulated to further increase the ISM's power density and operating temperature?

The first of the two questions is considered in section 2 of this chapter. The characteristics that a topology should exhibit in order to be considered for implementation in a high power density ISM operating in a high temperature environment are considered. Based on the automotive application such a topology is selected for implementation in the ISM in section 3.

The second question is considered at length in sections 4, 5 and 6 of this chapter. These sections illustrate how interleaving can be used to minimise both the energy stored in the topology (section 4) and the RMS currents in the passive components (section 5), helping to reduce both the ISM volume and losses. The results from sections 4 and 5 are used in section 6 to determine the optimum configuration of the selected topology.

## 2. Topology requirements for a high power density and high operating temperature

It was shown in Chapter 3 that there is a strong interdependence between the electrical, spatial and thermal design of the ISM. Figure 4.1 shows only the electrical topology design section of the interdependence diagram. The figure shows the two outputs of the electrical topology design, namely the energy that must be manipulated and transported to meet the electrical specification, and the heat that is dissipated in the topology due to the energy manipulation. The energy that must be manipulated within the ISM contributes to the volume of the module and the heat dissipated together with the module's thermal management determines the operating temperature, as discussed in Chapter 3. Both the maximum energy and dissipated heat have their source in the electrical topology design.

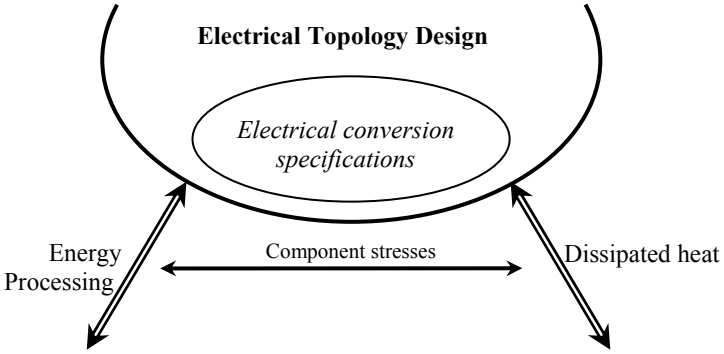



**Figure 4.1. The electrical topology design as defined in Chapter 3**

In this section the characteristics that a topology should exhibit for it to be suitable for implementation in a high power density ISM operating in a high temperature environment are considered.

## 2.1 Topology requirements for high power density applications

The choice of the topology can have significant consequences for the total volume of the module. Unfortunately there is no single topology that will always result in an ISM module with the lowest volume. Issues such as the intended thermal management, isolation and converter specifications play a significant role in selecting the appropriate topology.

A few issues that must be kept in mind when selecting a topology to be implemented in a high power density ISM are:

i. *Energy requires volume*. In any power electronic circuit, the volume required for the energy storage components (inductors and capacitors) is significant in comparison to the topology volume [4-1][4-2]. These components can very easily dominate the total volume of the converter. If the volume of the implemented topology with a given thermal management is to be minimised, the energy that must be stored in the topology must be minimised for a given switching frequency. Increasing the switching frequency can help reduce the energy that must be stored in the topology per switching cycle but often results in increased losses [4-1]. Thus a topology with a low energy storage requirement for a given switching frequency and topology specification is preferred.

ii. *Direct topology*. A direct topology is preferred over an indirect topology for high power density applications. A direct topology is defined as one that has a direct path between the input and output terminals during at least one switching state where an indirect topology does not [4-3]. The presence of transformers or additional filters does not change the definition. Examples of direct topologies include the buck, boost, forward and so on while examples of indirect topologies include the buck/boost, the Cuk, the flyback and so on. The direct topology is preferred for high power density applications because the direct link between the terminals allows some of the electrical energy that must be transferred between the terminals to be transferred without having to first be stored in passive components.

iii. *Component stresses*. The topology should ideally exhibit low component stresses for both the active and passive components. Very few topologies exhibit low component stresses for all the components in the topology. There are always a few components that experience more stresses than other components. In a high power density

application, the topology should be selected in such a way that the component stresses are in the components where they can be accommodated or manipulated.

iv. *Soft-switching*. Soft-switching can be both an advantage and disadvantage when selecting a topology to implement a high power density ISM. The choice of using soft-switching depends primarily on the technology used to implement the switching devices and the thermal management available to cool the devices. If good devices with the appropriate packaging are used and the thermal management is sufficient to remove the heat from the devices while meeting the thermal specifications, then soft-switching can be a hindrance in achieving a high power density. Soft-switching usually requires additional energy to be stored in the topology to achieve the ZVS or ZCS conditions [4-4][4-5]. The additional energy normally comes from an auxiliary circuit or by operating the topology in such a way that the additional energy is stored in the already available passive components [4-4][4-5]. This increases the passive components volume and normally increases the stresses in the passive components significantly. However, if it is not possible to remove the heat dissipated in the switching devices with the available thermal management, then to avoid increasing the volume of the thermal management significantly, soft-switching can become feasible. However, the trade-off between increased thermal management volume without soft-switching and an increase in passive component volume with soft-switching should be considered [4-6].

v. *Ease of control*. The ISM control circuit is normally integrated into the module. This too requires volume. Selecting a topology that is generally easy to control can help to minimise the volume that is occupied by the control system. Furthermore, the control system requires measurements (voltage and current) to control and protect the module. Topologies that can be adequately controlled with only a few measurements are more suited to high power density applications. Current measurements (other than a shunt resistor which is not without drawbacks) in particular can be difficult to implement in a high power density module and should be kept to a minimum [4-7].

## 2.2 Topology requirements for high temperature operation

For operation in a high temperature environment, such as the automotive environment, the temperature drop between the components within the ISM and the thermal interface must be as small as possible [4-8]. The temperature drop is highly dependent on the thermal management and technologies used to implement the components in the module. However, there are a few considerations concerning the topology level that influence the temperature drop and should be considered when selecting a topology to operate in a high temperature environment:

i. *Electrical efficiency*. The topology's electrical efficiency should be as high as possible to minimise the amount of heat that the thermal management structure must contend with. This is achieved by minimising the losses in all of the components within the topology, both active and passive. The losses in the components do not depend only on how the components are implemented (technology, materials and construction) but also on how the components are excited. For example, the topology can be selected so that the RMS currents in the passive components are as small as possible. This will reduce the ohmic loss in the components. Reducing the dielectric, hysteresis or eddy current losses in a component requires optimisation on the component level.

ii. *Temperature sensitivity*. The topology selected to operate in the high temperature environment should be insensitive to variations in the component values as the temperature changes, especially if large temperature variations in the environment are possible. It is well known that the capacitance and the inductance are generally not constant with temperature and can experience significant changes as the temperature

varies. This is particularly true for capacitors with the exception of a few ceramic materials with low values of permittivity [4-9]. Topologies that rely on a very specific value of the inductance or capacitance such as the resonant topologies or resonant transition topologies can experience difficulties and even loss of resonance as their temperature changes if appropriate measures have not been taken.

### 2.3 Combining the topology requirements for high power density and high operating temperature

To operate in a high temperature environment with a high power density, most of the above guidelines placed on the selection of the topology should be met by the topology before any modifications are made to the topology. Ensuring that the topology meets most of the guidelines before any alterations are made to the topology will help reduce the number of alterations required. Topology alterations or manipulations can then be used to improve on the few characteristics that the topology is lacking in for the given specification and environment. Such topology manipulations are considered in the following section of the chapter.

## 3. The topology selected for implementation in the ISM

In the previous section general guidelines on the choice of a topology suitable for implementation in a high power density ISM operating in a high temperature environment were given. In this section, a topology is selected on the basis of these guidelines and how one manipulates the topology to meet the requirements is considered.

### 3.1 The synchronous rectifier phase arm

There are many topologies that satisfy the general guidelines given in the previous section. Only one such topology is selected and considered further. The topology selected for implementation in the ISM is the bi-directional synchronous rectifier (SR) that is illustrated in Figure 4.2. This topology is selected for the following reasons:

i. The topology has a relatively low number of components, making it suitable for high power density applications.
ii. The topology is a direct topology, implying that energy can be transferred directly between the converter terminals during at least one switching interval, thereby reducing the energy storage requirements on the passive components.
iii. The components' stresses are not low especially for the high voltage bus capacitor as will be discussed. However, with the appropriate topology manipulation techniques

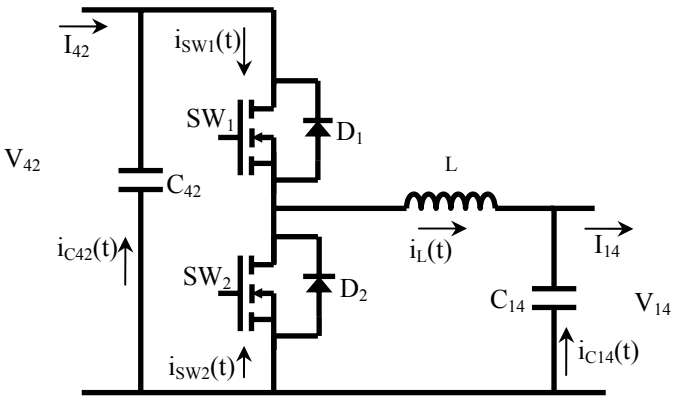



**Figure 4.2. The synchronous rectified bi-directional phase arm**

the component stress can be significantly reduced.

iv. The topology is easy to control using constant frequency PWM and is rugged.

v. The topology is insensitive to temperature-caused component parameter variations such as changes in either the capacitance or inductance values.

vi. The topology is bi-directional as required by the ISM specifications.

This topology is also popular in industry, largely for the reasons mentioned above in addition to being relatively inexpensive to implement and having a high overload capability.

With reference to Figure 4.2 and assuming the automotive environment; $V_{42}$ is the converter terminal connection to the 42V supply and $V_{14}$ is the terminal connecting to the 14V supply. $SW_1$ and $SW_2$ are the main switching devices, with $C_{42}$ and $C_{14}$ being the bus capacitors on the 42V and 14V nets respectively. The topology can operate as either a synchronous buck or as a synchronous boost converter, allowing power to be transferred from either voltage level to the other. The current directions in the figure denote the positive current direction for buck mode.

### 3.2 Converter waveforms

The inductor current labelled $i_L(t)$ in Figure 4.2 determines which mode the converter is operating in. When the average inductor current $I_L$ is positive, that is to say that power is being transferred from $V_{42}$ to $V_{14}$, the converter is functioning in buck mode, and when the average inductor current is negative, the converter is functioning in boost mode.

Figure 4.3 shows the operating waveforms for the converter operating in buck mode. The figure shows the idealised device voltages and currents and the inductor current as a function of time.

The topology operation can be described, assuming the active devices are implemented with MOSFETs, as follows [4-10]: when $SW_1$ is turned on, the voltage difference of $V_{42}$-$V_{14}$ over the inductor causes the current in the inductor to increase. A finite time later, $DT_s$, the device $SW_1$ is turned off and the current commutates to $D_2$, the body diode of the lower MOSFET. A short time later, once the dead time has expired, $SW_2$ is turned on and the inductor current commutates from the devices body diode, $D_2$, to the main channel of $SW_2$. Once the inductor current has commutated to the lower device, $SW_2$, a voltage of $-V_{14}$ appears over the inductor

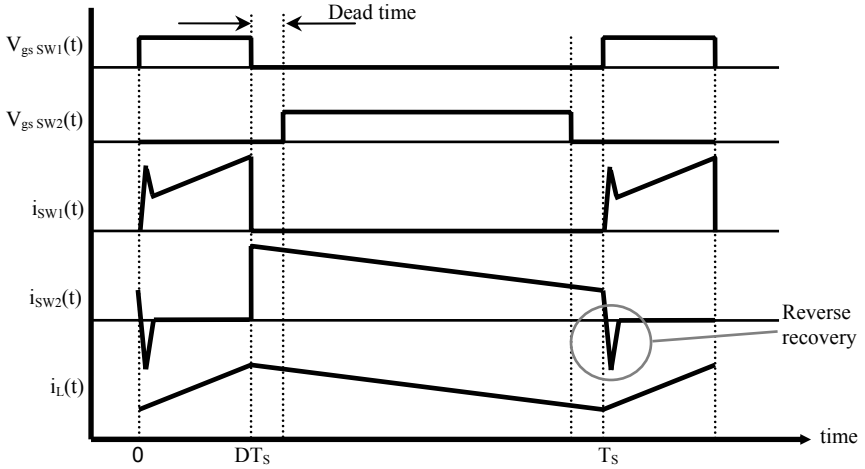



**Figure 4.3. The operating wave forms of the synchronous rectifier operating in buck mode**

causing the inductor current to decrease. Just prior to the beginning of a new period, $SW_2$ is turned off and the inductor current commutates out of the main channel back into the body diode $D_2$. The current continues to flow in the body diode until $SW_1$ is turned on. At this point, the current commutates from the body diode $D_2$ to $SW_1$ causing the body diode to experience reverse recovery. This reverse recovery current flows through both the top and lower device as illustrated in the figure.

The reverse recovery current is a significant drawback in the topology. However, this can be avoided by making the inductor current ripple large enough so that, just prior to turning $SW_1$ on, the inductor current flows in the body diode $D_1$ resulting in zero voltage turn-on [4-11]. However, this comes at the cost of having an inductor ripple current that is at least twice the average inductor current.

Since the topology is synchronously rectified, the inductor current will always keep its triangular shape irrespective of the average value of the inductor current [4-10][4-11]. This means that the relationship between the input voltage and output voltage, in both buck and boost modes, can be described by [4-12]:

$$D = D_{SW1} = \frac{V_{14}}{V_{42}} \tag{4.1}$$

where $V_{14}$ is the voltage on the 14V terminals [V],
$V_{42}$ is the voltage on the 42V terminals [V]
and $D = D_{SW1}$ is the duty cycle of $SW_1$.

The duty cycle of $SW_2$ is:

$$D_{SW2} = 1 - \left( \frac{V_{14}}{V_{42}} + \frac{2T_{dt}}{T_s} \right) \tag{4.2}$$

where $T_{dt}$ is the dead time inserted between the on signals of the two devices to avoid any shoot through current [s]
and $T_s$ is the switching period [s].

### *3.2.1 Continuous conduction mode and continuous conduction mode with zero crossing*

The definition of continuous conduction mode (CCM) and discontinuous conduction mode (DCM) for the synchronous rectifier needs to be reconsidered for the sake of clarity. In the synchronous rectifier topology, the inductor current is always triangular and never becomes discontinuous. Thus true DCM does not exist for this topology. However, the inductor current does pass through zero when the average inductor current is low enough. This results in two possible continuous conduction modes.

The topology is operating in true continuous conduction mode (CCM) when the inductor current (in buck mode or boost mode) does not pass through zero, i.e. the average inductor current is larger than half the inductor peak to peak current ripple:

$$\left| I_L \right| \geq \frac{1}{2} \Delta I_L \tag{4.3}$$

where $|I_L|$ is the absolute of the average inductor current [A],
$\Delta I_L$ is the peak to peak ripple in the inductor current [A] and is given as:

$$\Delta I_L = \frac{V_{42}(1-D)DT_s}{L} \tag{4.4}$$

where $L$ is the inductance [H].

The topology is operating in continuous conduction mode with zero crossing (ZCCM) when the inductor current passes through zero. For the synchronous rectified phase arm, the inductor current will continue flowing once it is negative keeping the triangular waveform but the average inductor current will be smaller than half the peak to peak ripple current:

$$|I_L| < \frac{1}{2}\Delta I_L \tag{4.5}$$

### 3.3 Topology advantages and disadvantages

The topology is successful in industry for the primary reason that it has a very low component count while been very rugged. The topology is easy to control and the functioning of the topology is mostly insensitive to changes in the temperature.

A major disadvantage of the topology, as illustrated in Figure 4.3, is the reverse recovery current in the freewheeling diode. This reverse recovery current, also known as the vertical current, contributes significantly to the losses of the topology in two ways. The first is the reverse recovery losses in the freewheeling diode and the second is a significant increase in the switching losses of the non-freewheeling device. The reverse recovery current flows through the non-freewheeling device while it is still blocking the full bus voltage. This increases the device's switching losses significantly.

Another disadvantage of the topology is that the currents in the bus capacitors can become significantly large. Figure 4.4 shows the typical currents in the two bus capacitors operating in buck mode without the effect of the reverse recovery current. The RMS current, resulting in capacitor losses, can become significant as the current level of the converter increases. This is especially true for the bus capacitor on the 42V level. As the RMS currents increase, the losses and component stresses in the capacitors will also increase, increasing the amount of heat that must be removed from the component with the thermal management structure. This can result in the component overheating. In addition it is not easy to remove heat from bus capacitors due to the construction of the component. Reducing the losses is desirable, and thus the RMS currents in the bus capacitors.

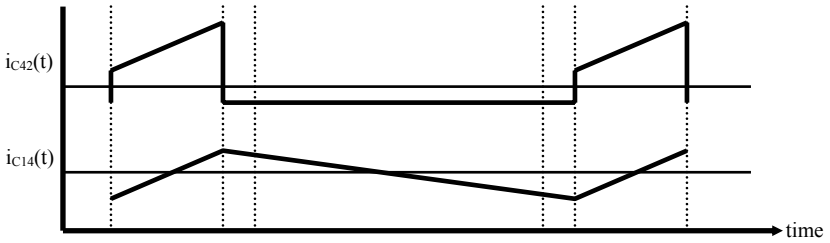



**Figure 4.4. Typical bus capacitor current waveforms for buck mode (without the reverse recovery current)**

## 3.4 Topology manipulation

The synchronous rectified phase arm is the topology to be implemented in the automotive ISM. However, the topology is not without its drawbacks, which can severely limit both the achievable power density and operating temperature of the ISM. The volume of the ISM is limited primarily by the volume required for the passive components and their accompanied cooling structure. Thus, the volume required for the passive components and the heat dissipated in the components must be reduced. This is achieved by manipulating the topology to have the desired characteristics. For the synchronous rectifier, this can be achieved through interleaving multiple phases [4-13][4-14].

### *3.4.1 Interleaving*

Figure 4.5 shows a converter system consisting of *N* paralleled DC/DC converters. All of these converters are connected together so that they share a common bus capacitor on both the 14V and 42V terminals. Each converter within the system of *N* converters is referred to as a phase. The power processed by each phase is $1/N^{th}$ of the rated power of the complete system. In Figure 4.5 each DC/DC converter is implemented with a synchronous rectified phase arm consisting of two active devices and one inductor. Each phase is assumed to be identical to the others as far as possible.

The switching signals of each phase in the converter system are phase shifted in time by $2\pi/N$ degrees. The currents flowing in the bus capacitors will then have a ripple frequency that is *N* times the phase switching frequency and have a ripple and RMS current that is smaller than that of a single phase (the exact reduction is a function not only of the number of phases but also of the component parameters and converter specifications as will be shown). The result is that the RMS currents in the capacitors as well as the maximum energy that must be stored in the components are reduced.

In the following two sections, the exact reduction of RMS currents and energy stored in the passive components is calculated for the multi-phase synchronous rectifier as a function of the number of phases. This is used to determine the optimum number of phases for the given specification.

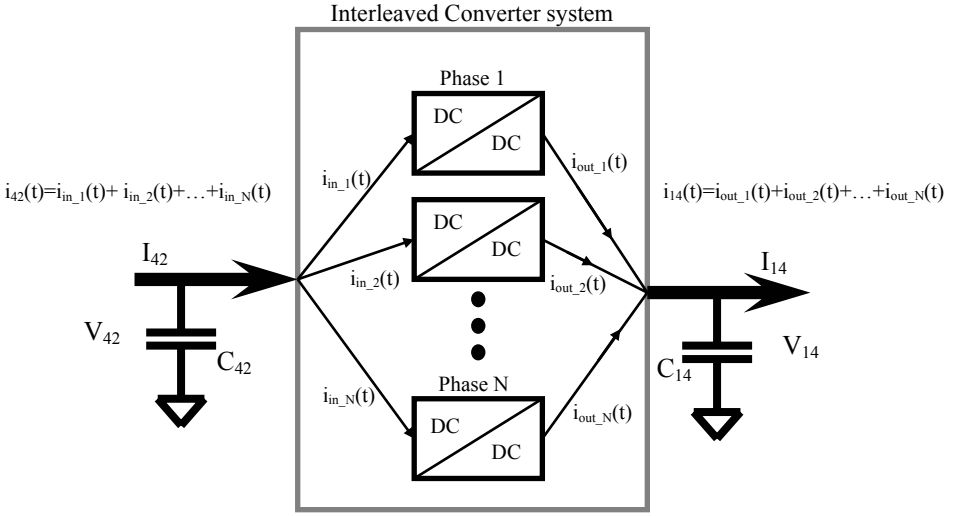



**Figure 4.5. Generic representation of an N-phase interleaved synchronous rectified converter topology**

# 4. Minimising energy storage requirements

Each passive component in the implemented topology will have a maximum energy that it must be capable of storing in order to meet the electrical design specifications. The maximum energy will vary as the design, topology operating point and specifications vary. The maximum energy that the passive component must be capable of storing is directly linked to the volume of that component. To minimise the volume of the passive components, the maximum energy that must be stored in the components must be minimised. In addition, the maximum energy stored in the components can be used to help find the optimum number of phases for the minimum total energy stored in all the passive components simultaneously.

In addition to the maximum energy that must be stored in the passive components, the energy that the components process per switching cycle is also considered. The energy processed per switching cycle is the energy that passes through the passive component during one switching cycle. The energy processed per switching cycle is used to help determine the component stresses as a function of the number of phases and is an indication of how much energy is circulating between the passive components.

The energy manipulated by the active devices is ignored in the following analysis because the volume required to implement the active devices is significantly smaller than that of the passive components.

## 4.1 Energy in the passive components

The maximum and processed energy in each passive component is determined on the basis of

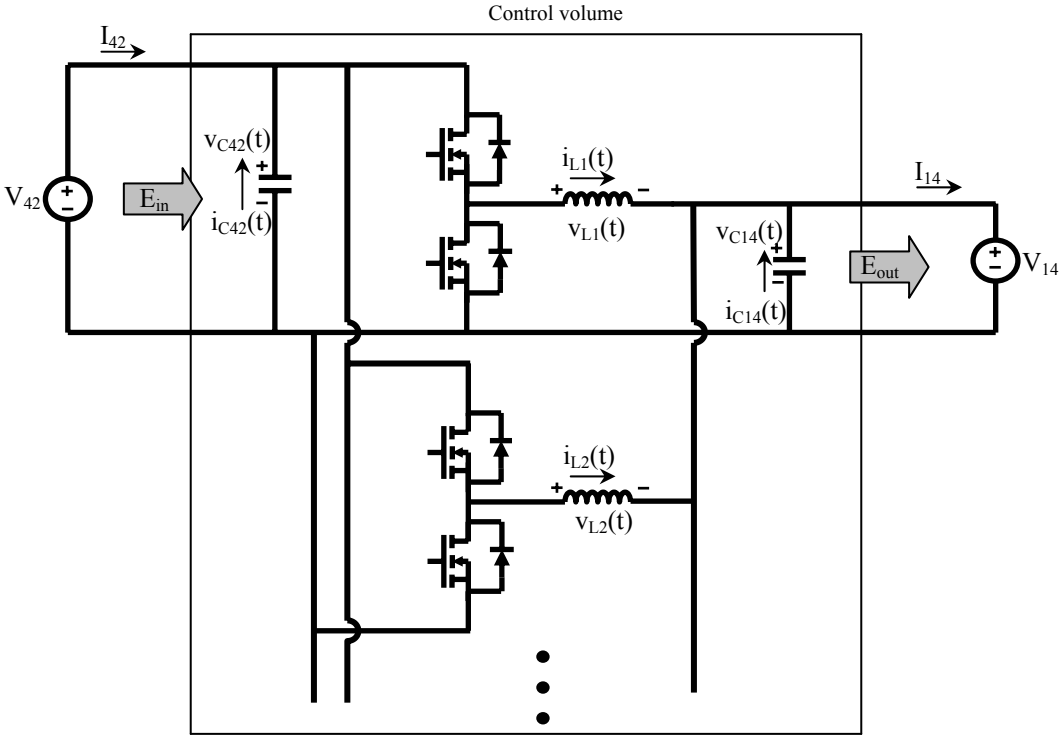



**Figure 4.6. A multi-phase synchronous rectifier with the passive component currents identified for calculating the energy stored in the components**

the topology configuration in Figure 4.6. The figure shows the interleaved synchronous rectifier consisting of an arbitrary number of phases within a defined control volume. For each passive component in the figure, the component voltage and current as a function of time have been identified. The maximum energy stored and the energy processed is calculated for the two bus capacitors and the phase arm inductors. It is assumed that all of the phases are implemented with the same inductor structure and inductance so the maximum energy stored and processed by the inductors is calculated only once and then multiplied by the number of phases. The total energy that must be stored in the control volume is then the sum of maximum energies stored in all the components within the control volume.

## 4.2 Energy in L

The inductor waveforms for a single inductor in a system of $N$ phases are plotted in Figure 4.7. The inductor has only two possible waveforms irrespective of the number of phases. The first is illustrated in the top of Figure 4.7 for CCM and the bottom of the same figure for ZCCM. As the number of phases change, only the average inductor current changes while the current ripple $\Delta I_L$ remains the same for a given set of component parameters and duty cycle.

The border between CCM and ZCCM for the inductor current as a function of the number of phases can be found by determining when the inductor current passes through zero. Thus the boundary condition that must be satisfied to be operating in CCM is:

$$\frac{|I_{14}|}{N} \geq \tfrac{1}{2}\Delta I_L \tag{4.6}$$

where $N$ is the number of phases,
$\Delta I_L$ is as defined in equation 4.4
and $|I_{14}|$ is the average current flowing into or out of the converter 14V terminal [A].

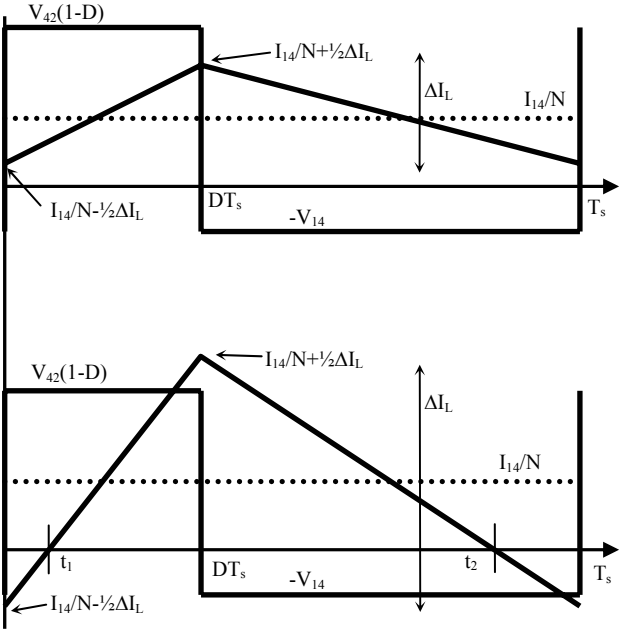



**Figure 4.7. The inductor waveforms for an arbitrary number of phases (Top - CCM, Bottom - ZCCM)**

### 4.2.1 Maximum stored energy

The maximum energy that the inductor must be capable of storing is determined only by the inductor's maximum current and the inductance. The complete calculation method for the maximum energy in the inductor can be found in Appendix A**.** The maximum energy stored in a single inductor in an *N*-phase system, for both buck and boost operation, is:

$$\begin{aligned} E_{\max\_L} &= \tfrac{1}{2} L I_{\max}^2 \\ &= \tfrac{1}{2} L \left( \frac{|I_{14}|}{N} + \tfrac{1}{2} \Delta I_L \right)^2 \end{aligned} \tag{4.7}$$

where $E_{max\_L}$ is the maximum energy that each inductor in the *N*-phase system must be capable of storing [J],

$\frac{|I_{14}|}{N}$ is the average inductor current in an *N*-phase system [A]

and $L$ is the phase inductor's inductance [H].

### 4.2.2 Processed energy

The energy that is processed by the inductor in a single cycle, as illustrated in Figure 4.7, is calculated in Appendix A. In CCM, the energy processed by the inductor in one switching period is the difference in the energies in the component at the end and the beginning of the charging period, where the charging period is $0 \le t \le DT_s$ for buck mode. However, in ZCCM, the energy processed by the inductor is equal to the sum of the two energies being stored in the inductor at different times within the switching period. With reference to the lower figure in Figure 4.7, energy is stored in the inductor in the time intervals $t_1 \le t \le DT_s$ and $t_2 \le t \le T_s$ for buck mode. The total energy being processed by the inductor, for both buck and boost operation, is:

$$E_{processed\_L} = \begin{cases} L \Delta I_L \dfrac{|I_{14}|}{N} & if \dfrac{|I_{14}|}{N} \ge \tfrac{1}{2} \Delta I_L \\ L \left( \left( \dfrac{|I_{14}|}{N} \right)^2 + \tfrac{1}{4} \Delta I_L^2 \right) & if \dfrac{|I_{14}|}{N} < \tfrac{1}{2} \Delta I_L \end{cases} \tag{4.8}$$

where $E_{processed\_L}$ is the energy processed in a single inductor in a single switching period in an *N*-phase system [J].

### 4.2.3 Energy in the inductor(s)

For the purpose of illustrating the effect that the component values and converter specifications have on the maximum stored and processed energies in the inductor(s), the following values are used to plot the above equations: $P=2kW$, $I_{14}=P/V_{14}$, $V_{14}=14V$, $f_s=140kHz$. Two values of $L$ are selected, namely 4µH and 0.4µH, to illustrated the effect of operating in CCM and ZCCM.

Figure 4.8 shows the maximum energy stored in and the energy processed by the inductor in an *N*-phase synchronous rectifier plotted as a function of the duty cycle and the number of phases for the above parameters.

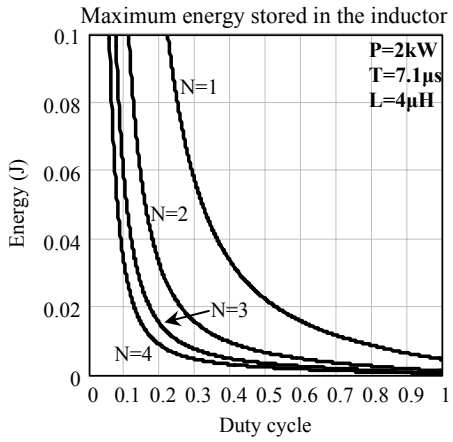



**Figure 4.8a.**

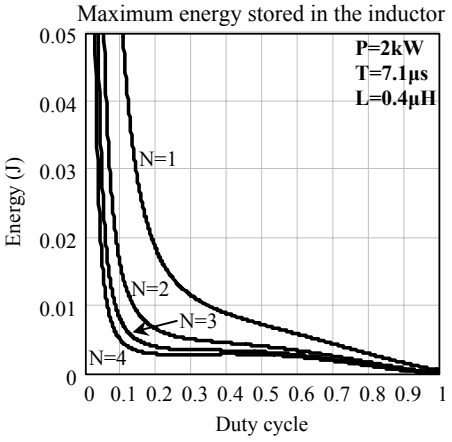



**Figure 4.8b.**

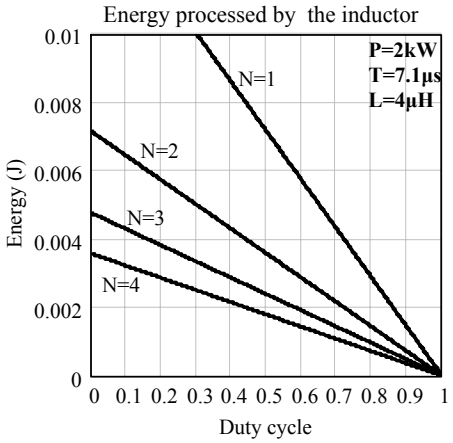



**Figure 4.8c.**

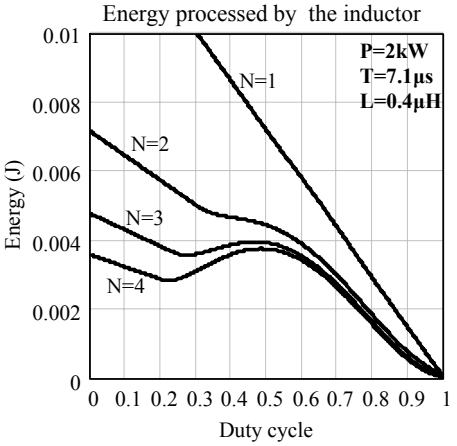



**Figure 4.8d.**

**Figure 4.8. The maximum energy stored and processed by a single inductor in an N-phase system for P = 2kW, T = 7.1µs and 2 different values of inductance**

Figure 4.8a and Figure 4.8b show the maximum energy that the inductor must be capable of storing for a relatively large inductance (4µH) and a relatively small inductance (0.4µH) respectively as a function of the duty cycle and number of phases. Comparing Figure 4.8a and Figure 4.8b it can be seen that the maximum energy stored in the inductor is less for the smaller inductance. This is due to the fact that in ZCCM, all of the energy stored in the inductor is transferred to the load. It can also be expected that this trend will not continue indefinitely as the inductance is further reduced due to the increasing current ripple. For a large inductance, one where the current in the inductor remains in CCM over a large duty cycle range, the maximum energy in the inductor reduces as the number of phases increase. However, for a small inductance when operating in ZCCM, the reduction in the maximum energy as the number of phases increases and can become very small and even lost. In addition, the maximum energy in the inductor at low duty cycles decreases quickly as the number of phases increase. This means that if operating with a low duty cycle such as 20% or 30%, a significant reduction in the maximum stored energy can be achieved by increasing the number of phases.

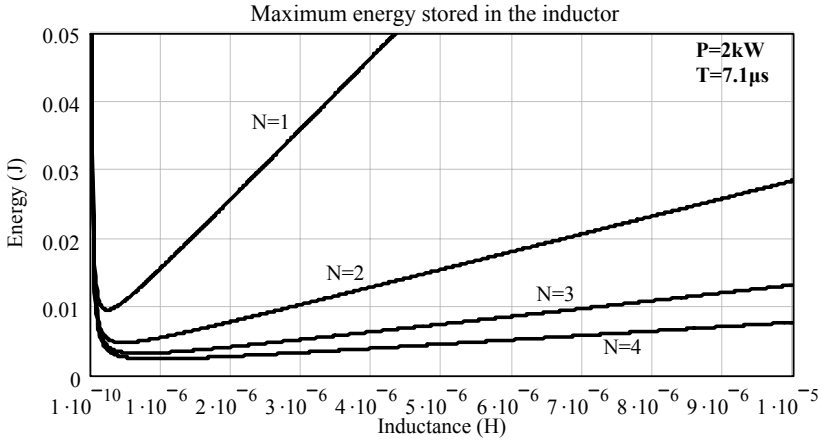



**Figure 4.9. The maximum energy that the inductor must store as a function of the inductance for a duty cycle of 33%**

Figure 4.8c and Figure 4.8d show the energy being processed by a single inductor for the same values of inductance. Figure 4.8c and Figure 4.8d show that as the number of phases increase the amount of energy that each inductor processes decreases linearly in CCM. When operating in ZCCM as in Figure 4.8d, the amount of energy processed by the inductors can increase significantly and any reduction in the energy processed as the number of phases increases can be lost.

Figure 4.9 shows the maximum energy that must be stored in the inductor as a function of the inductance for a duty cycle of 33% ($V_{14}/V_{42}$ nominally). The figure shows that there is a minimum in the energy that the inductor must be capable of storing and this minimum decreases with an increase in the number of phases. The figure also shows that as the number of phases increase, the maximum energy that must be stored in the inductor increases at a slower rate with an increasing inductance. This gives a larger range over which the inductance can be selected while still maintaining the energy in the inductor sufficiently close to the minimum.

The phase arm inductance resulting in the minimum total stored energy in the inductor is:

$$L_{\min\_energy} = \tfrac{1}{2}\frac{NV_{42}^2(1-D)D^2T_s}{P} \tag{4.9}$$

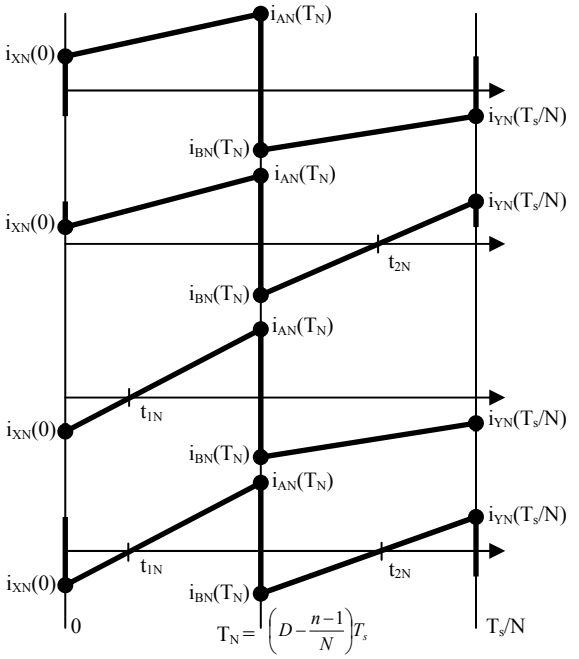
where $L_{min\_energy}$ is the inductance resulting in the minimum stored energy [H]
and $P$ is the converter rated power [W].

## 4.3 Energy in $C_{42}$

To determine the energy stored in and processed by the capacitor, the current flowing into and out of the capacitor as a function of time in terms of the number of phases, duty cycle and inductance is required. Once the capacitor current is known, the electrical charge that the capacitor must store during each charging cycle can be determined. With the electrical charge known, the maximum energy and the energy processed by the capacitor can be determined.

### *4.3.1 Maximum stored energy*

To determine the energy stored in $C_{42}$, the current flowing in the capacitor as a function of the




$$i_{XN}(0) = I_{14}\left(\frac{n}{N} - D\right) - \frac{n}{2D}\Delta I_L\left(D - \frac{n-1}{N}\right)$$

$$i_{YN}\left(\frac{T_s}{N}\right) = I_{14}\left(\frac{n-1}{N} - D\right) - \frac{n-1}{2D}\Delta I_L\left(D - \frac{n}{N}\right)$$

$$i_{AN}\left(\left(D - \frac{n-1}{N}\right)T_s\right) = I_{14}\left(\frac{n}{N} - D\right) + \frac{n}{2D}\Delta I_L\left(D - \frac{n-1}{N}\right)$$

$$i_{BN}\left(\left(D - \frac{n-1}{N}\right)T_s\right) = I_{14}\left(\frac{n-1}{N} - D\right) + \frac{n-1}{2D}\Delta I_L\left(D - \frac{n}{N}\right)$$

$$t_{1N} = \tfrac{1}{2}\left(D - \frac{n-1}{N}\right)T_s - \frac{1}{n}\frac{I_{14}}{\Delta I_L}\left(\frac{n}{N} - D\right)DT_s$$

$$t_{2N} = \tfrac{1}{2}\left(D - \frac{n-2}{N}\right)T_s - \frac{1}{n-1}\frac{I_{14}}{\Delta I_L}\left(\frac{n-1}{N} - D\right)DT_s$$

Where n=1,2,..,N and $\frac{n-1}{N} < D \le \frac{n}{N}$

**Figure 4.10. The 4 basic current waveforms present in $C_{42}$ as a function of the number of phases**

number of phases is required. For an *N*-phase system, the current waveform is repeated *N* times, thus only *1/N* of the complete waveform needs to be analysed. Further, depending on the inductance, there are only 4 possible current waveforms that can flow in the capacitor. These current waveforms are plotted in Figure 4.10. Each waveform consists of two parts. Depending on the inductance value, the charging and discharging periods are different. A complete analysis of the capacitor waveforms can be found in Appendix A.

The maximum charge that the capacitor must store can be calculated from the waveforms in Figure 4.10 and is:

$$Q_{\max\_C_{42}} = \begin{cases} \begin{cases} if\, I_{14}\left(\frac{n}{N} - D\right) \ge \frac{n}{2D}\Delta I_L\left(D - \frac{n-1}{N}\right) \\ \left(I_{14}T_s\left(\frac{n}{N} - D\right)\left(D - \frac{n-1}{N}\right)\right) & if\ I_{14}\left(\frac{n-1}{N} - D\right) \le \frac{n-1}{2D}\Delta I_L\left(D - \frac{n}{N}\right) \\ \frac{1}{2}T_s\left[I_{14}\left(\frac{n}{N} - D\right)\left(D - \frac{n-1}{N}\right) + \frac{n-1}{4D}\Delta I_L\left(D - \frac{n}{N}\right)^2 + \frac{1}{n-1}\frac{I_{14}^2}{\Delta I_L}\left(D - \frac{n-1}{N}\right)^2 D\right] & otherwise \end{cases} \\ \begin{cases} if\, I_{14}\left(\frac{n}{N} - D\right) < \frac{n}{2D}\Delta I_L\left(D - \frac{n-1}{N}\right) \\ \frac{1}{2}T_s\left[I_{14}\left(\frac{n}{N} - D\right)\left(D - \frac{n-1}{N}\right) + \frac{n}{4D}\Delta I_L\left(D - \frac{n-1}{N}\right)^2 + \frac{1}{n}\frac{I_{14}^2}{\Delta I_L}\left(D - \frac{n}{N}\right)^2 D\right] & if\ I_{14}\left(\frac{n-1}{N} - D\right) \le \frac{n-1}{2D}\Delta I_L\left(D - \frac{n}{N}\right) \\ \max\left\{\begin{array}{l} \frac{1}{2}T_s\left[I_{14}\left(\frac{n}{N} - D\right)\left(D - \frac{n-1}{N}\right) + \frac{n}{4D}\Delta I_L\left(D - \frac{n-1}{N}\right)^2 + \frac{1}{n}\frac{I_{14}^2}{\Delta I_L}\left(D - \frac{n}{N}\right)^2 D\right] \\ \frac{1}{2}T_s\left[I_{14}\left(\frac{n}{N} - D\right)\left(\frac{n-1}{N} - D\right) + \frac{n-1}{4D}\Delta I_L\left(D - \frac{n}{N}\right)^2 + \frac{1}{n-1}\frac{I_{14}^2}{\Delta I_L}\left(D - \frac{n-1}{N}\right)^2 D\right] \end{array}\right\} & otherwise \end{cases} \end{cases} \quad (4.10)$$

where $Q_{max\_C42}$ is the maximum electrical charge that is stored in the capacitor [C]

and $n$ is an integer $n \in [1, N]$ satisfying $\frac{n-1}{N} < D \le \frac{n}{N}$.

Equation 4.10 consists of 4 terms depending on the values of points $i_{XN}(0)$ and $i_{YN}(T_s/N)$, which are functions of the topology's operating point and number of phases. In the last term of the equation a maximum function is present. This is necessary because the mode described by this term has two charging intervals and two discharging intervals (see Figure 4.10). The larger of the two charges must be selected as the maximum that the component must store.

The maximum energy stored in the capacitor is:

$$E_{\max\_C_{42}} = \tfrac{1}{2} C_{42} V_{42}^2 \tag{4.11}$$

where $E_{max\_C42}$ is the maximum energy stored in the capacitor [J],
$C_{42}$ is the bus capacitor's capacitance [F]
and $V_{42}$ is the voltage across the capacitor [V].

As the current in the capacitor changes due to changes in the topology, the capacitance requirement for a given voltage ripple will also change. The energy stored in the capacitor can be written for a given voltage ripple, in terms of the maximum charge that must be stored in the capacitor:

$$E_{\max\_C_{42}} = \tfrac{1}{2} \frac{Q_{\max\_C_{42}}}{\Delta V_{42}} V_{42}^2 \tag{4.12}$$

where $\Delta V_{42}$ is the voltage ripple on the capacitor [V].

### 4.3.2 Processed energy

The energy that is processed by the capacitor can also be calculated by determining the total charge stored in the capacitor over one switching period, which is $N$ times that over one steady state cycle:

$$Q_{processed\_C_{42}} = \begin{cases} \text{if } I_{14}\left(\frac{n}{N} - D\right) \geq \frac{n}{2D}\Delta I_L\left(D - \frac{n-1}{N}\right) \\ \begin{cases} N I_{14} T_s \left(\frac{n}{N} - D\right)\left(D - \frac{n-1}{N}\right) & \text{if } I_{14}\left(\frac{n-1}{N} - D\right) \leq \frac{n-1}{2D}\Delta I_L\left(D - \frac{n}{N}\right) \\ \frac{1}{2} N T_s \left[ I_{14}\left(\frac{n}{N} - D\right)\left(D - \frac{n-1}{N}\right) + \frac{n-1}{4D}\Delta I_L \left(D - \frac{n}{N}\right)^2 + \frac{1}{n-1}\frac{I_{14}^2}{\Delta I_L}\left(D - \frac{n-1}{N}\right)^2 D \right] & \text{otherwise} \end{cases} \\ \text{if } I_{14}\left(\frac{n}{N} - D\right) < \frac{n}{2D}\Delta I_L\left(D - \frac{n-1}{N}\right) \\ \begin{cases} \frac{1}{2} N T_s \left[ I_{14}\left(\frac{n}{N} - D\right)\left(D - \frac{n-1}{N}\right) + \frac{n}{4D}\Delta I_L \left(D - \frac{n-1}{N}\right)^2 + \frac{1}{n}\frac{I_{14}^2}{\Delta I_L}\left(D - \frac{n}{N}\right)^2 D \right] & \text{if } I_{14}\left(\frac{n-1}{N} - D\right) \leq \frac{n-1}{2D}\Delta I_L\left(D - \frac{n}{N}\right) \\ \frac{1}{2} N T_s \left[ \frac{1}{4D}\Delta I_L \left( n\left(D - \frac{n-1}{N}\right)^2 + (n-1)\left(D - \frac{n}{N}\right)^2 \right) + \frac{I_{14}^2}{\Delta I_L}\left( \frac{1}{n}\left(D - \frac{n}{N}\right)^2 + \left(\frac{1}{n-1}\right)\left(D - \frac{n-1}{N}\right)^2 \right) D \right] & \text{otherwise} \end{cases} \end{cases} \tag{4.13}$$

where $Q_{processed\_C42}$ is the total charge processed by the capacitor in one switching cycle [C]
and $n$ is an integer $n \in [1, N]$ satisfying $\frac{n-1}{N} < D \leq \frac{n}{N}$.

The total energy that is processed by the bus capacitor in one switching cycle is then:

$$E_{processed\_C_{42}} = Q_{processed\_C_{42}} V_{42} \tag{4.14}$$

Where $E_{processed\_C42}$ is the energy processed by the capacitor in one switching cycle [J]
and $V_{42}$ is the voltage across the capacitor [V].

### 4.3.3 Energy in the capacitor - $C_{42}$

Using the same parameters as for the inductor, the maximum energy stored in $C_{42}$ and the total energy processed by $C_{42}$ in one switching cycle are plotted in Figure 4.11 and Figure 4.12 respectively for a voltage ripple of 1% ($\Delta V_{42}=0.01 \cdot V_{42}$).

Figure 4.11a shows that generally for a large inductance, the maximum energy stored in $C_{42}$ decreases with an increase in the number of phases. This trend is only valid for duty cycles of less than *1/N*. As the duty cycle increases, there are regions where the higher number of phases results in a larger energy storage requirement on $C_{42}$ than a lower number of phases. Figure 4.11b shows the maximum energy stored in the capacitor for a small inductance. In the figure there are discontinuities in the maximum stored energy for two phases and higher. These discontinuities are present due to the maximum function in equation 4.10. At these points

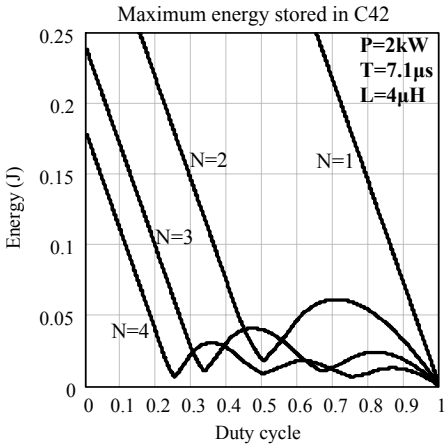



**Figure 4.11a.**

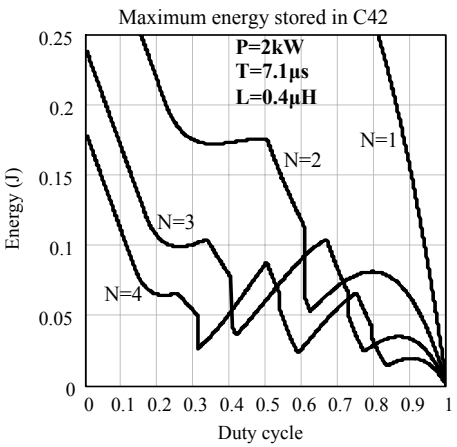



**Figure 4.11b.**

**Figure 4.11. The maximum energy that $C_{42}$ must be capable of storing**

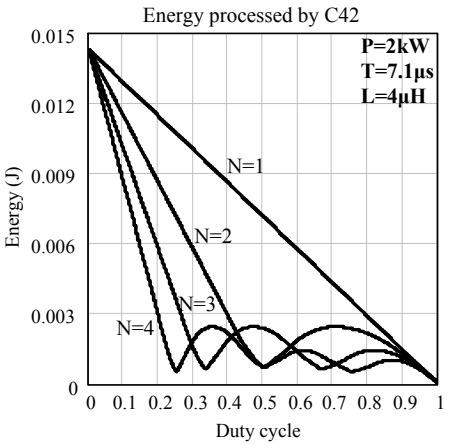



**Figure 4.12a.**

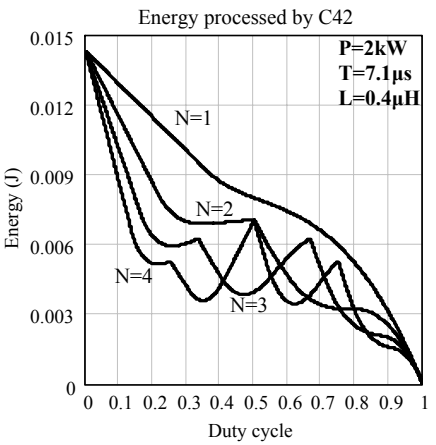



**Figure 4.12b.**

**Figure 4.12. The total energy processed by $C_{42}$ as a function of the number of phases**

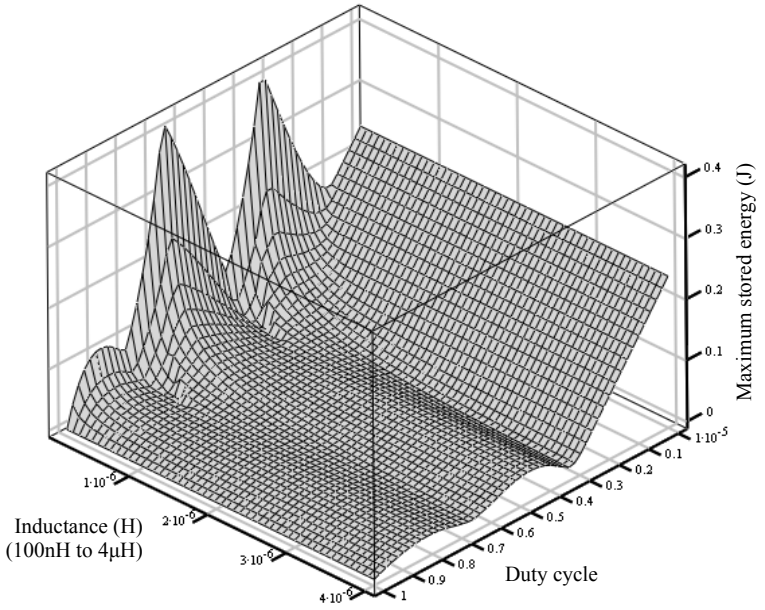



**Figure 4.13. The maximum energy stored in $C_{42}$ for a 3-phase system as a function of the duty cycle and the inductance**

energy is being transferred to the capacitor in two intervals instead of one, reducing the requirements in the maximum energy stored at that point in time. The figure also shows that the maximum storage requirements of $C_{42}$ can become significantly large when the inductance value is reduced, resulting in a capacitor with a large volume being required.

Figure 4.12 shows the total energy processed by the capacitor during one switching cycle. For a large inductance, illustrated in Figure 4.12a, the total energy processed by the capacitor is largest for a single phase. For duty cycles less than *1/N*, the processed energy decreases with an increase in the number of phases, but this trend is not consistent for larger values of the duty cycle. If the inductance value is decreased, as illustrated in Figure 4.12b, the energy that is processed by the capacitor becomes significantly large. Further, the energy processed by the capacitor does not decrease significantly with an increase in the number of phases.

Figure 4.13 shows the maximum energy stored in the capacitor as a function of both the inductance and the duty cycle. Generally, as the inductance increases, the amount of energy that $C_{42}$ must store decreases. However, this decrease is exponential, so the advantage that a very large inductance gives in terms of energy stored in $C_{42}$ is marginal.

## 4.4 Energy in $C_{14}$

The energy stored in $C_{14}$ as a function of the number of phases can be determined from the current flowing through the capacitor, as illustrated in Figure 4.14. The waveform is repeated *N* times in an *N*-phase topology per switching period. The complete analysis can be found in Appendix A.

### *4.4.1 Maximum stored energy*

The maximum energy that is stored in the capacitor is:

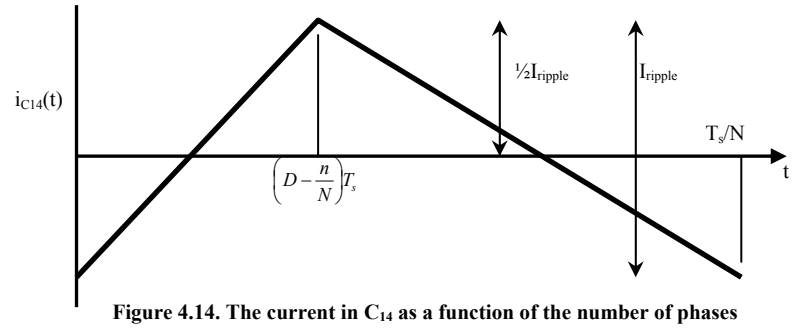



**Figure 4.14. The current in $C_{14}$ as a function of the number of phases**

$$E_{\max\_C_{14}} = \tfrac{1}{2} C_{14} V_{14}^2 = \tfrac{1}{2} \frac{Q_{\max\_C_{14}}}{\Delta V_{14}} V_{14}^2 \tag{4.15}$$

where $E_{max\_C14}$ is the maximum energy stored in the capacitor [J],
$\Delta V_{14}$ is the allowed voltage ripple [V]
and $Q_{max\_C14}$ is the maximum charge that the capacitor must store [C].

The maximum charge stored in the capacitor is calculated for a single charging period as:

$$Q_{\max\_C_{14}} = \frac{1}{8} \frac{V_{42} T_s^2}{L} \left( D - \frac{n-1}{N} \right) \left( \frac{n}{N} - D \right) \qquad if \ \frac{n-1}{N} < D \le \frac{n}{N} \tag{4.16}$$

where $Q_{max\_C14}$ is the maximum charge that is stored in $C_{14}$ [C]
and $n$ is an integer $n \in [1, N]$ satisfying $\frac{n-1}{N} < D \le \frac{n}{N}$.

### *4.4.2 Processed energy*

The total energy that is processed by the capacitor can be found by multiplying equation 4.16 by the voltage across the capacitor and the number of phases to include all the energy passing through the capacitor in one switching period:

$$E_{processed\_C_{14}} = \frac{N}{8} \frac{D V_{42}^2 T_s^2}{L} \left( D - \frac{n-1}{N} \right) \left( \frac{n}{N} - D \right) \qquad if \ \frac{n-1}{N} < D \le \frac{n}{N} \tag{4.17}$$

where $E_{processed\_C14}$ is the total energy processed by the capacitor in one switching period [J].

### *4.4.3 Energy in the capacitor $C_{14}$*

Equations 4.15 and 4.17 are plotted in Figure 4.15 for the same parameters as the inductor and $C_{42}$ and assuming a voltage ripple of 1% of the terminal voltage ($\Delta V_{14}=0.01 \cdot V_{14}$). Figure 4.15a and Figure 4.15b show the maximum energy stored in the capacitor as a function of the duty cycle and number of phases. The figure shows that as the number of phases increase, the peak value of the maximum stored energy decreases, but there are regions where a lower number of phases delivers better performance as regards the stored energy than the higher number of phases. From equation 4.15 it is also clear that the maximum energy stored in the capacitor decreases in inverse proportion to the inductance.

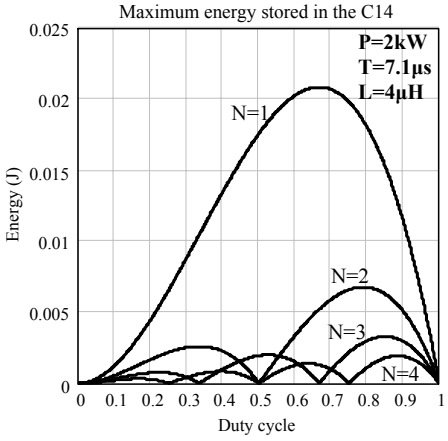



**Figure 4.15a.**

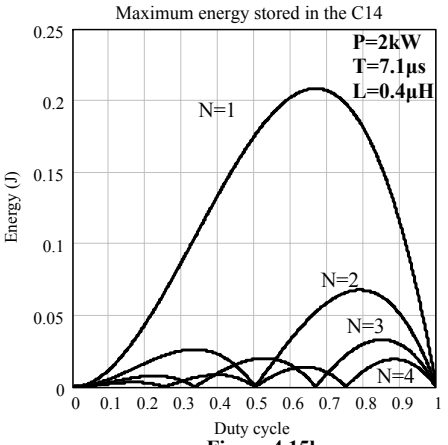



**Figure 4.15b.**

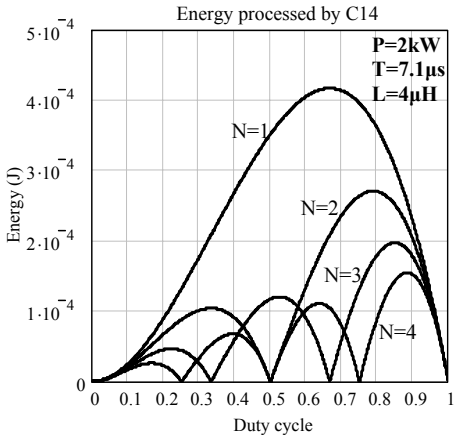



**Figure 4.15c.**

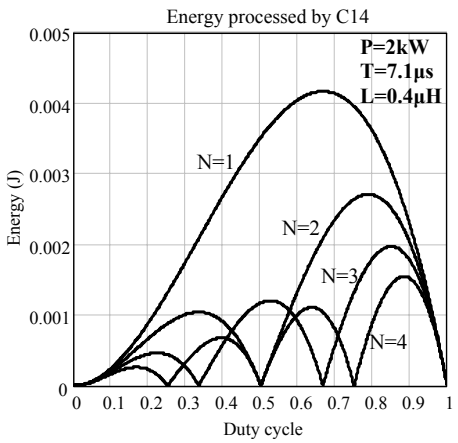



**Figure 4.15d.**

**Figure 4.15. The maximum energy stored and processed by a $C_{14}$ in an N-phase system for P=2kW, T=7.1µs and 2 different values of inductance**

Figure 4.15c and Figure 4.15d show the energy that is processed by the capacitor in one switching period as a function of the number of phases and duty cycle. The energy that is processed by the capacitor during one switching period is significantly less than the maximum energy stored in the capacitor for the same operating point. The processed energy shows similar behaviour as the maximum stored energy as a function of the inductance, number of phases and duty cycle.

### *4.5 Minimum stored and processed energy*

The total energy that must be stored in the module is the sum of the maximum energies that must be stored in all the passive components in an *N*-phase topology:

$$E_{\max\_total} = E_{\max\_C_{14}} + E_{\max\_C_{42}} + N \cdot E_{\max\_L} \tag{4.18}$$

where $E_{max\_total}$ is the maximum combined energy that is stored by all the passive components in the ISM [J].

Similarly, the total energy processed within the module during one switching cycle is the sum of the energies processed by all the passive components within the module:

$$E_{processed\_total} = E_{processed\_C_{14}} + E_{processed\_C_{42}} + N \cdot E_{processed\_L} \tag{4.19}$$

where $E_{processed\_total}$ is the total energy processed by all the passive components [J].

The total energy that is stored in all of the passive components is significant because this energy requires volume to be implemented in within the ISM. If the maximum energy stored in the passive components can be minimised, then less volume will be required within the ISM for the passive components, increasing the ISM's power density. The maximum energy that is stored in all of the passive components simultaneously in the ISM with *N*-phases is plotted in Figure 4.16. Figure 4.16a shows the maximum energy stored with an inductance of 4µH. The maximum energy stored in each phase normalised to that stored in a single phase is plotted in Figure 4.16b. The same is plotted in Figure 4.16c and Figure 4.16d for the case of an inductance value of 0.4µH.

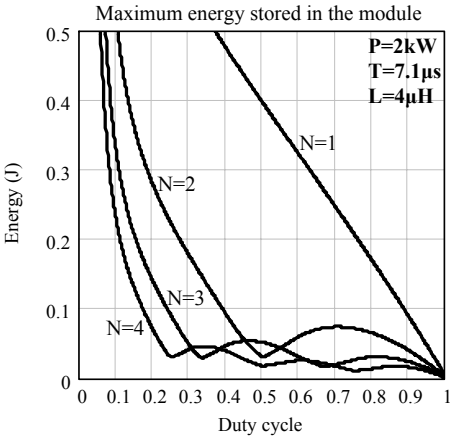



**Figure 4.16a.**

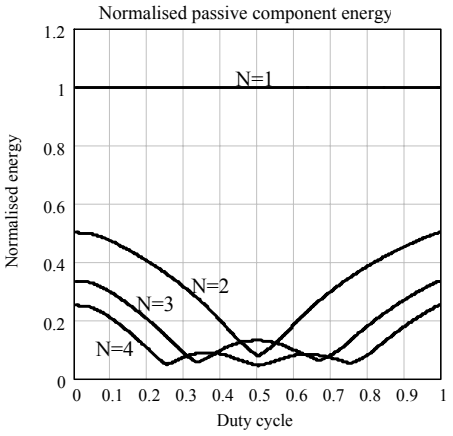



**Figure 4.16b.**

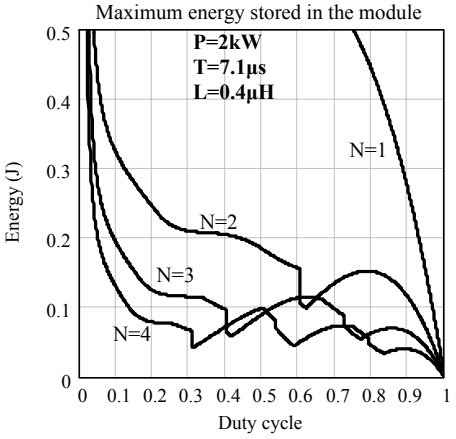



**Figure 4.16c.**

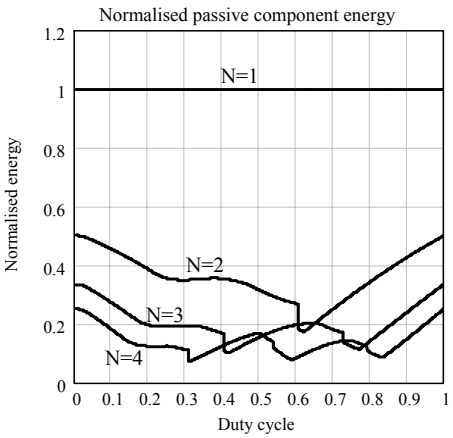



**Figure 4.16d.**

**Figure 4.16. The maximum energy stored in the passive components as a function of the duty cycle and the number of phases for a 2kW system operating at 140kHz**

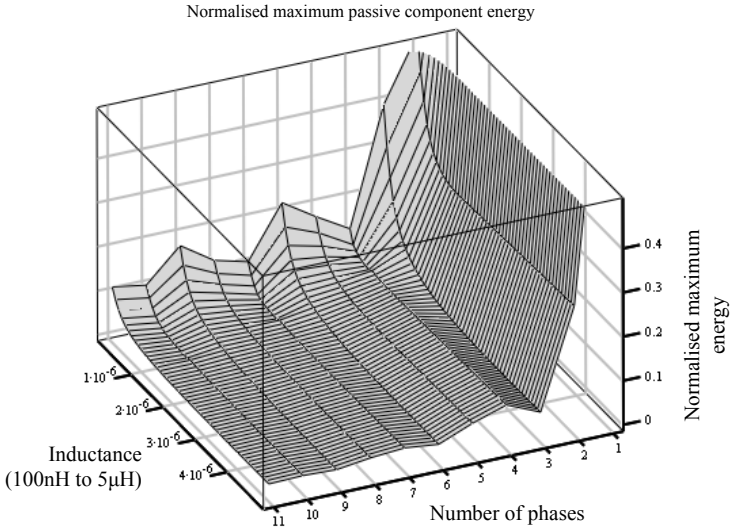



**Figure 4.17. The normalised maximum energy stored in the passive components plotted as a function of the inductance and number of phases for a duty cycle of 33% and power rating of 2kW**

The normalised figures show that a significant reduction in the maximum energy that the passive components must be capable of storing can be achieved by simply increasing the number of phases from one to two. As the number of phases increase further, the advantage gained becomes marginal and at certain duty cycles the advantage can be lost to a lower number of implemented phases.

The total energy that must be stored in all the passive components normalised to that of a single phase topology is plotted in Figure 4.17 as a function of the inductance and number of phases for a duty cycle of 33%, a power rating of 2kW and a switching frequency of 140kHz. The figure shows that as the inductance and number of phases increase, the total energy stored in the module generally decreases. This means that a large number of phases will not necessary have a significant improvement in the reduction of total stored energy compared to a slightly lower number of phases.

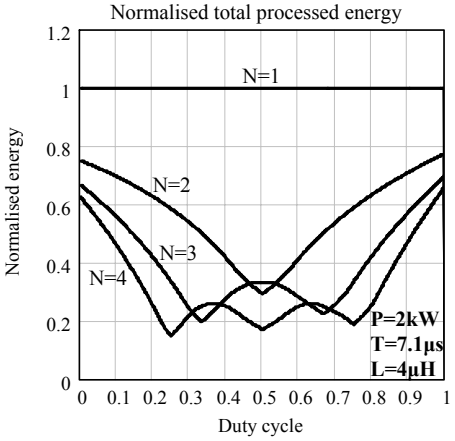



**Figure 4.18a.**

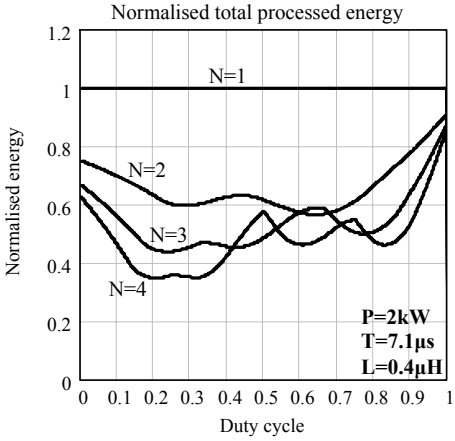



**Figure 4.18b.**

**Figure 4.18. The total energy processed by the passive components normalised to that processed by a single phase topology**

The total energy processed by the passive components, normalised to that processed by a single phase topology for the same specifications as above, is plotted in Figure 4.18 for an inductance of 4μH (Figure 4.18a) and 0.4μH (Figure 4.18b). The two figures show that as the number of phases increase, there is a savings in the total energy being processed by the passive components but, as the inductance decreases, it is possible to lose any advantage gained. This is because the phases will be operating in deep ZCCM and there will be a significant amount of energy circulating between the passive components that does not contribute to the energy being delivered to the load.

# 5. Minimising RMS currents

Minimising the energy that is stored in the ISM for a given set of parameters helps in achieving a high power density, but the losses in the components must also be considered before the optimum number of phases can be selected. The losses in the passive components can be estimated by the product of the square of the RMS current and the components' effective series resistance. The effective series resistance is a function of the components' geometry, construction and materials, but the RMS current is a function of the topology. Thus it is desirable to minimise the RMS currents in the passive components to minimise the losses in the components for a given construction.

## 5.1 The RMS currents for N-phases

The RMS current is determined for each passive component as a function of the number of phases, duty cycle and inductance for a given set of parameters and converter specifications.

### *5.1.1 RMS current in L*

The RMS current in the inductor can be calculated together with Figure 4.7. It is not necessary to distinguish between CCM and ZCCM for the inductor current because the triangular waveform does not change its shape as the number of phases increases, other than the average current. The complete analysis of the inductor current as a function of the number of phases can be found in Appendix B.

The RMS current flowing in the phase arm inductor is calculated as:

$$I_{L\_RMS} = \sqrt{\left(\frac{I_{42}}{ND}\right)^2 + \frac{1}{12}\Delta I_L^2} \tag{4.20}$$

where $I_{L\_RMS}$ is the RMS current in the phase arm inductor [A].

The RMS current in the inductor is plotted in Figure 4.19 for a large inductance (Figure 4.19a) and a small inductance (Figure 4.19b) and with the same parameters as in the previous section. In both figures it can be seen that the RMS current in the inductor can become very large and a significant reduction in the RMS current is achieved when the number of phases is increased. However, there is a limit on how much the RMS current can be reduced for a given inductance. This can be seen from equation 4.20. The equation consists of two terms, one containing the average inductor current ($I_{14} = I_{42}/D$) and one containing the ripple current. As the number of phases increase for a given inductance, the contribution of the average inductor current towards the RMS current will decrease but the contribution due to the ripple current will be unaffected. Furthermore, if the inductance value is decreased, the current ripple, which will increase as the

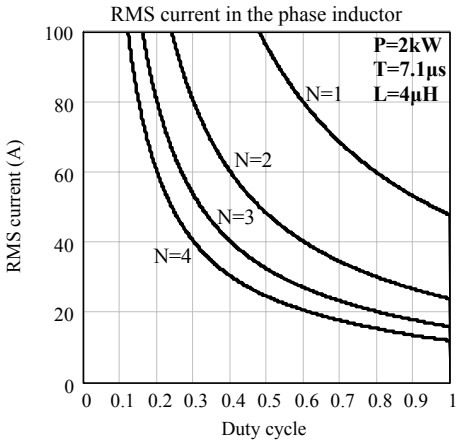



**Figure 4.19a.**

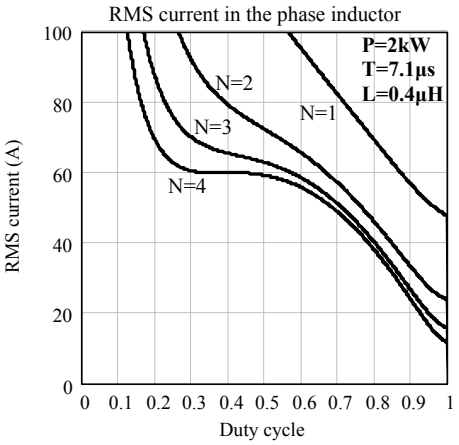



**Figure 4.19b.**

**Figure 4.19. The RMS current in the phase arm inductance for a N-phase topology with a power rating of 2kW and a switching frequency of 140kHz**

inductance decreases, will dominate the RMS inductor current, resulting in larger inductor losses.

Thus to minimise the inductor RMS current, the number of phases can be increased, but the inductance value must also be large enough to prevent the ripple term becoming overly dominant.

### *5.1.2 RMS current in $C_{42}$*

The RMS current in $C_{42}$ is a significant issue in the synchronous rectified topology and can result in very large volumes be required to satisfy both the thermal and energy storage requirements of the component [4-14]. Minimising the RMS current in $C_{42}$ has significant benefits in achieving both a high power density and high operating temperatures.

The RMS current in the capacitor can be determined with the aid of Figure 4.10. The complete derivation can be found in Appendix B. If Figure 4.10 is briefly considered, it can be seen that the capacitor current waveform repeats itself every $T_s/N$ seconds and always consists of two parts, for $t \le \left(D-\frac{n-1}{N}\right)T_s$ and for $t > \left(D-\frac{n-1}{N}\right)T_s$. The current in the capacitor can be determined as a function of the number of phases, topology operating point and specifications as:

$$I_{C_{42}\_RMS} = \sqrt{\frac{I_{42}^2}{D^2}\left(D-\frac{n-1}{N}\right)\left(\frac{n}{N}-D\right)+\frac{N}{12}\Delta I_L^2\left[(n-1)^2\left(\frac{n}{N}-D\right)^3+n^2\left(D-\frac{n-1}{N}\right)^3\right]} \quad (4.21)$$

$$if \quad \frac{n-1}{N} < D \le \frac{n}{N}$$

where $I_{C42\_RMS}$ is the RMS current in $C_{42}$ [A]
and $n$ is an integer $n \in [1, N]$ satisfying $\frac{n-1}{N} < D \le \frac{n}{N}$.

The RMS current in $C_{42}$ consists of two terms; the first is a function of the average load current ($I_{14} = I_{42}/D$) and the second the combined inductor current ripple. The RMS current in $C_{42}$ is a function of the average load current, which implies that as the load current increases, the capacitor RMS current will also increase, limiting the topologies overload capabilities.

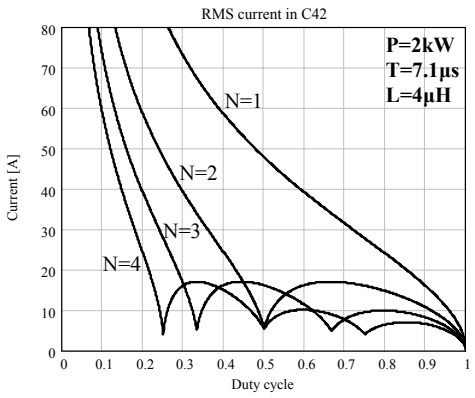



Figure 4.20a.

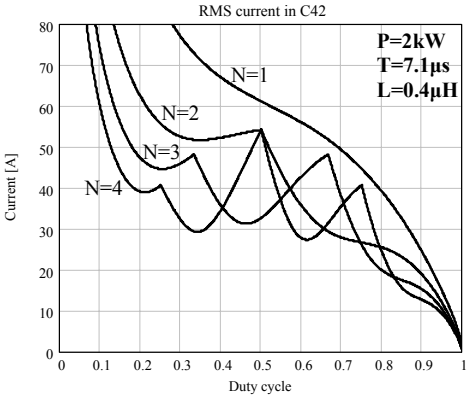



Figure 4.20b.

**Figure 4.20. The RMS current in the $C_{42}$ for a N-phase topology with a power rating of 2kW and a switching frequency of 140kHz**

The RMS current in $C_{42}$ as a function of the number of implemented phases is plotted in Figure 4.20 for the same component parameters and specifications as before. The RMS current in the capacitor for a large value of inductance (4µH) is plotted in Figure 4.20a and for a relatively small value of inductance (0.4µH) in Figure 4.20b. Both figures show that it is possible to have an RMS current in the bus capacitor that exceeds the topology supply current ($I_{42}$ in buck mode), requiring substantial volume to prevent the component from being thermally destroyed. Figure 4.20a shows that for a relatively large value of inductance, a significant reduction in the capacitor RMS current can be achieved with an increase in the number of phases. However, there are points where the higher number of phases do not result in a lower capacitor RMS current. Once such point is with a duty cycle of 50%. At this point a 2-phase topology delivers the same RMS current as a 4-phase topology, whereas a 3-phase topology has a RMS current that is approximately twice as large.

Figure 4.20b shows that as the inductance decreases and the topology operates in ZCCM, the RMS current in $C_{42}$ increases significantly and instead of having local minimums in the RMS current, there are local maximums for duty cycles that are equal to:

$$D = \frac{n}{N} \tag{4.22}$$

where $n = 1, 2, 3 \ldots N$.

This kind of behaviour in the capacitor RMS current is common in VRMs (voltage regulation modules) where the inductance value is made very small to achieve a very fast transient response. By making the inductor very small, the requirements on the supply bus capacitor are significantly increased.

The RMS current in $C_{42}$ normalised to that in a single phase topology is plotted in Figure 4.21 as a function of both the duty cycle and the phase arm inductance for a 3-phase system operating with the same parameters as previously. The figure shows that the RMS current is a strong function of the inductance when the inductance value is small. However, as the inductance increases, the RMS current in the capacitor quickly reaches a minimum value that is relatively independent of the inductance. This means that an inductance value exists that results in a minimum in the $C_{42}$ RMS current for a given number of phases and this inductance value

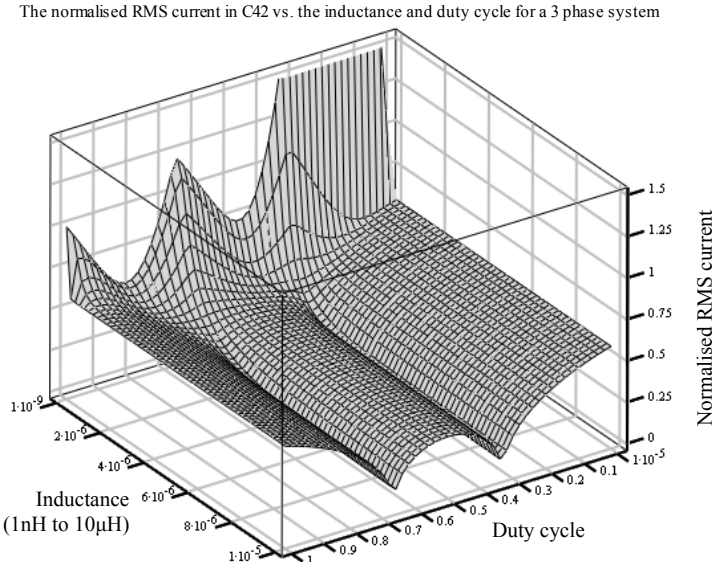



**Figure 4.21. The normalised RMS current in $C_{42}$ for a 3-phase system with a power rating, P=2kW and a switching frequency of 140kHz**

does not have to be significantly large. This is illustrated in Figure 4.22, which shows the RMS current in $C_{42}$ as a function of the inductance and number of phases for a duty cycle of 33%.

### *5.1.3 RMS current in $C_{14}$*

The RMS current in $C_{14}$ can be determined with the aid of Figure 4.14. The complete analysis can be found in Appendix B. The RMS current in $C_{14}$ as a function of the number of phases is:

$$I_{C_{14}\_RMS} = \frac{NV_{42}T_s}{\sqrt{12}L}\left(D-\frac{n-1}{N}\right)\left(\frac{n}{N}-D\right) \qquad if\ \frac{n-1}{N} < D \le \frac{n}{N} \tag{4.23}$$

where $I_{C14\_RMS}$ is the RMS current in $C_{14}$ [A]
and $n$ is an integer $n \in [1, N]$ satisfying $\frac{n-1}{N} < D \le \frac{n}{N}$.

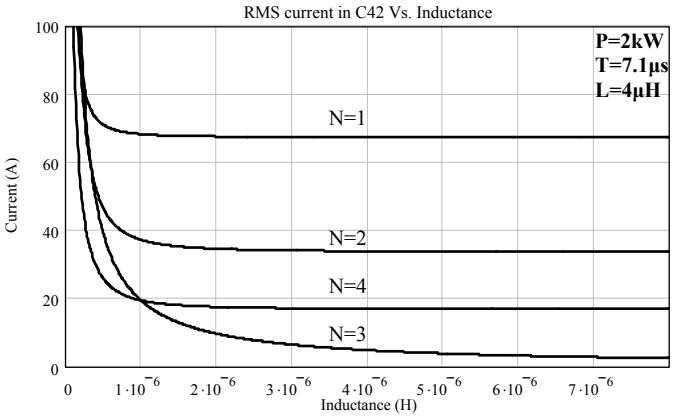



**Figure 4.22. The RMS current in $C_{42}$ as a function of the inductance for a duty cycle D=0.33**

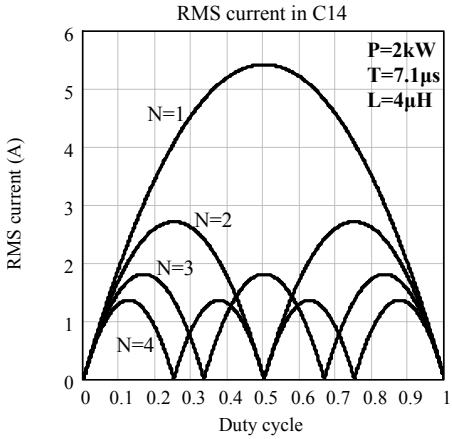



**Figure 4.23a.**

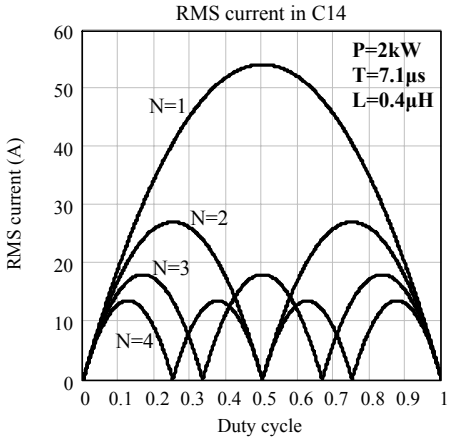



**Figure 4.23a.**

**Figure 4.23. The RMS current in $C_{14}$ as a function of the number of phases and duty cycle**

The RMS current in $C_{14}$, for the same component parameters and topology specifications as previously, has been plotted in Figure 4.23 as a function of the duty cycle and the number of phases. Figure 4.23a plots the RMS current for a large inductance (4µH) and Figure 4.23b for a relatively small inductance of 0.4µH. Since the RMS current in the capacitor is inversely proportional to the inductance, the RMS current in Figure 4.23b is point for point 10 times larger than that in Figure 4.23a.

The figure also shows that as the number of phases increase, the maximum RMS current in the capacitor decreases. However, there are regions in the duty cycle where a lower number of phases results in a lower RMS current in the bus capacitor than a higher number of phases at the same operating point.

For a very small value of inductance, the RMS current in $C_{14}$ can be of the same magnitude as that in $C_{42}$. As the inductance increases, the RMS current in $C_{14}$ decreases significantly, becoming only a fraction of the RMS current in $C_{42}$. Figure 4.24 shows the RMS current in $C_{14}$

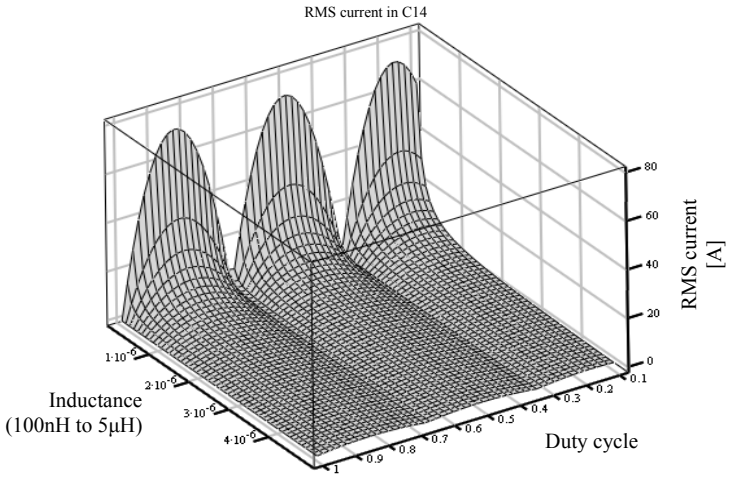



**Figure 4.24. The RMS current in $C_{14}$ for a 3-phase system operating with the same parameters as previously defined**

as a function of the duty cycle and the phase arm inductance for a 3-phase topology with a power rating of 2kW and a switching frequency of 140kHz per phase. The figure shows that as the inductance increases, the RMS current in the capacitor becomes negligible. In addition, under certain duty cycle conditions the RMS current in $C_{14}$ is practically zero for all inductance values. However, this operating point is extremely sensitive because any change in the duty cycle will result in a large change in the capacitor RMS current.

### 5.2 Minimum passive component losses

The losses in the passive components can be approximated by the product of the square of the RMS current in the component and the ESR of the component. The accuracy of this approximation depends on how accurately the ESR is determined for the various components being considered and if it includes frequency dependant, eddy, hysteresis or dielectric losses components. For the purpose of evaluating the approximate losses in the passive components to find the optimum number of phases, the data sheet specifications for suitable components can be used. Once a choice on the number of phases is made, the losses in the passive components can be determined more accurately. Mathematically, the approximated losses in the passive components are:

$$\begin{aligned} P_{C_{14}} &= ESR_{C_{14}} I^2_{C_{14}\_RMS} \\ P_{C_{42}} &= ESR_{C_{42}} I^2_{C_{42}\_RMS} \\ P_L &= ESR_L I^2_{L\_RMS} \end{aligned} \tag{4.24}$$

where $P_{C14}$ are the losses in $C_{14}$ [W],
$ESR_{C14}$ is the approximated ESR in $C_{14}$ [Ω],
$P_{C42}$ are the losses in $C_{42}$ [W],
$ESR_{C42}$ is the approximated ESR in $C_{42}$ [Ω],
$P_L$ are the losses in the phase arm inductor [W]
and $ESR_L$ is the approximated ESR in the inductor [Ω].

The total approximated losses in the two bus capacitors and the $N$ inductors are:

$$P_{passive\_components} = P_{C_{14}} + P_{C42} + N \cdot P_L \tag{4.25}$$

where $P_{passive\_components}$ is the total passive component losses [W].

For purposes of illustration, typical ESR values for the passive components are selected on the basis of components found in a similar converter topology with similar ratings (14/42V, 2kW), to estimate the losses in the passive components as a function of the number of phases and the duty cycle. Two important assumptions are made. Firstly, it is assumed that the ESR values of the components are constant over the whole excitation range. For the bus capacitors this can be justified by the ESR as a function of frequency graph in the data sheets for the selected capacitors – that is, mostly constant over the frequency range of interest. This is because as both the capacitance and frequency increase, the frequency-dependent impedance of the component becomes very small and the resistance of the foils and leads becomes dominant. Secondly, it is assumed that the inductor's ESR does not change as the number of phases increases. This implies that the same inductors are used in all the phases irrespective of the number of phases. This assumption is made to standardise the inductor structures as a function

of the number of phases to make a fair comparison. The ESR values selected for the purposes of illustration are:

- $ESR_{C14} \approx 10m\Omega$
- $ESR_{C42} \approx 80m\Omega$
- $ESR_{L} \approx 4.5m\Omega$

Under these assumptions, the approximated losses can be plotted as a function of the number of phases.

The total losses in the passive components for the assumed component parameters are plotted in Figure 4.25. Figure 4.25a shows the losses in the passive components for an inductance of 4µH while Figure 4.25b shows the same losses normalised to that in the single phase topology. The two graphs show that the losses in the passive components can be significantly reduced as the number of phases are increased. Just increasing the number of phases from one to two can result in a reduction of the passive component losses by anything between 50% and 90%

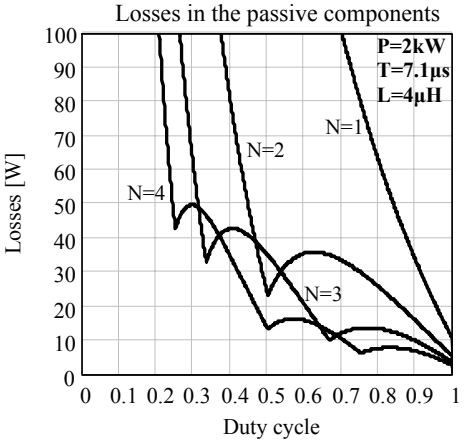



**Figure 4.25a.**

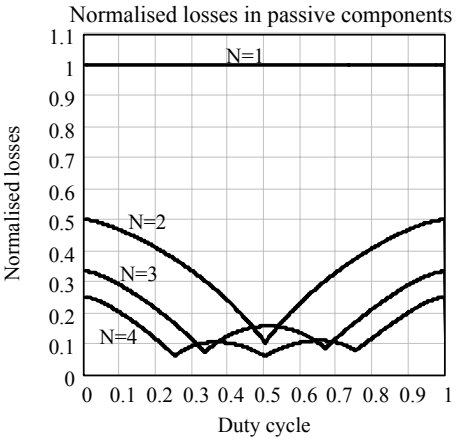



**Figure 4.25b.**

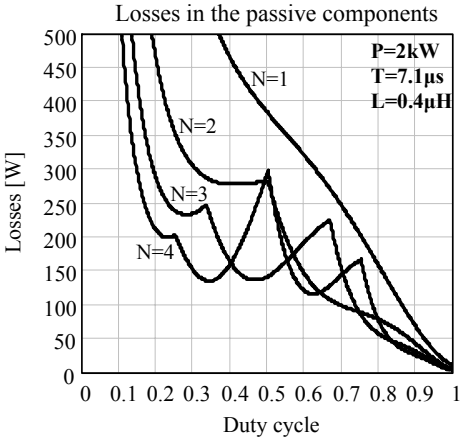



**Figure 4.25c.**

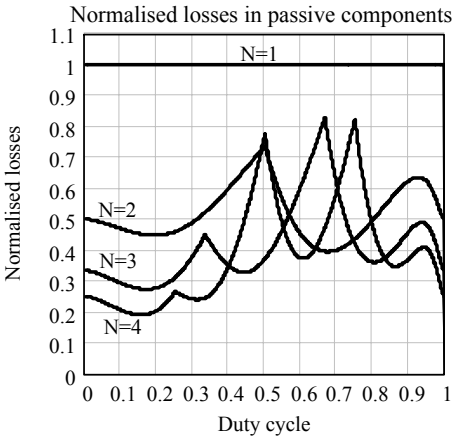



**Figure 4.25d.**

**Figure 4.25. The total losses in the passive components in an N-phase system with $ESR_{C14} \approx 10m\Omega$, $ESR_{C42} \approx 80m\Omega$ and $ESR_{L} \approx 4.5m\Omega$**

depending on the duty cycle. As the number of phases increase, the losses in the passive components can be reduced even further for certain duty cycles.

Figure 4.25c shows the losses in the passive components for an inductance of 0.4µH. The figure shows that the losses can be significantly larger than those with the larger inductance. This is due to the very large ripple in the inductor current. Moreover, the figure shows that for the small inductance there are local maximums in the losses where there were local minimums in the losses for the same duty cycle but a larger inductance. Figure 4.25d shows the losses in the passive components in Figure 4.25c normalised to that in the single phase topology for the same inductance value. The reduction in the losses as the number of phases increase is significantly less than for the larger inductance value.

The losses in the passive components normalised to those in a single phase topology as a function of the inductance for a duty cycle of 33% are plotted in Figure 4.26. The figure shows that as the number of phases increase, the losses in the passive components decrease significantly. The figure also shows that there is a floor value in the losses for a given set of parameters that is relatively independent of the inductance once the inductance exceeds a certain minimum value. This is significant because it means that a very large inductance is not required to minimise the losses in the passive components. The smallest possible inductance can be used and still achieve a minimum in the passive component losses.

# 6. Optimising the topology design

To determine the optimum topology operating point, concerning the passive components, the maximum energy that must be stored in the passive components and the RMS currents in the components must be considered simultaneously and an operating point selected where both are minimised. Only the passive components are considered, because it is assumed that the volume contribution of the passive components together with their necessary thermal management structures is significantly more than that of the active components in the ISM.

## 6.1 The optimum number of phases

The optimum number of phases is considered first on a component and then on a system level.

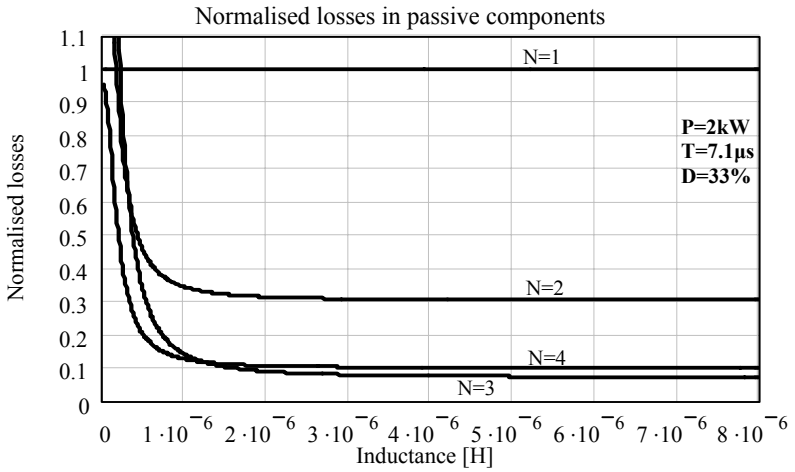



**Figure 4.26. The total losses in the passive components in an N-phase system as a function of the inductance with $ESR_{C14}$≈10mΩ, $ESR_{C42}$≈80mΩ and $ESR_L$≈4.5mΩ**

### 6.1.1 Component level

To determine the optimum number of phases with reference to the passive components, both the maximum energy that must be stored in the components and the RMS current through the components must be considered. Both the energy that must be stored in the passive components and the RMS current in the components can be determined directly from the topology waveforms, as has been done in the previous two sections, without knowing any details specific to the components (such as the ESR or maximum ratings).

To determine the optimum number of phases based on the maximum stored energy in and the RMS currents through the components, the product of the normalised maximum energy stored and normalised RMS current for the specific components is selected as the figure of merit and is referred to as the Component Optimisation Factor (COF). The COF is selected as the figure of merit because the maximum stored energy is representative of the component's volume while the RMS current is representative of the component losses, both as a consequence of the topology. Finding the minimum in the COF can be used to help find the operating point where both the maximum stored energy and the RMS currents are minimised. The COF is defined as:

$$COF = E_{\max\_norm} \cdot I_{RMS\_norm} \tag{4.26}$$

where $COF$ is the component optimisation factor,
$E_{max\_norm}$ is the maximum energy stored in the component normalised to that stored in the component in a single phase topology for the same specifications
and $I_{RMS\_norm}$ is the RMS current in the same component normalised to that stored in the component in a single phase topology for the same specifications.

The COF is determined for all the passive components in the $N$-phase system with the same specifications as in the previous sections and as a function of the duty cycle. The results are plotted in Figure 4.27 for $C_{42}$, $C_{14}$ and the phase arm inductance. The COF is plotted for a phase arm inductance of 4µH on the left of the figure and 0.4µH on the right of the figure.

Figure 4.27a and b show the COF for $C_{42}$. For a large inductance, a significant reduction in the COF is achieved with an increase in the number of phases in addition to having larger duty cycle ranges where the COF is reduced. Local minimums at duty cycles of $D=\frac{n}{N}$ where $n = 1, 2, \ldots N$ help to even further reduce the COF. In the case of a small inductance, as in Figure 4.27b, the reduction in the COF is significantly less than that with a larger inductance. Moreover, instead of having local minimums at $D=\frac{n}{N}$, there are local maximums.

Figure 4.27c and d show the COF for $C_{14}$ as a function of the duty cycle and number of phases. Both figures are the same irrespective of the inductance value. This is because the maximum energy stored in the capacitor and the RMS current in the capacitor are both inversely proportional to the inductance and the inductance is cancelled out when the stored energy and the RMS current are normalised. It is also interesting to note that the COF for $C_{14}$ has a very similar shape to that of $C_{42}$ with a large inductance. The only difference is that the COF extends to zero for $C_{14}$ but is never zero for $C_{42}$.

Figure 4.27e and f show the COF for the phase arm inductor as a function of the number of phases and the duty cycle. Both figures show that as the number of phases increase, the COF decreases. However, as the inductance becomes smaller, the reduction in the COF decreases

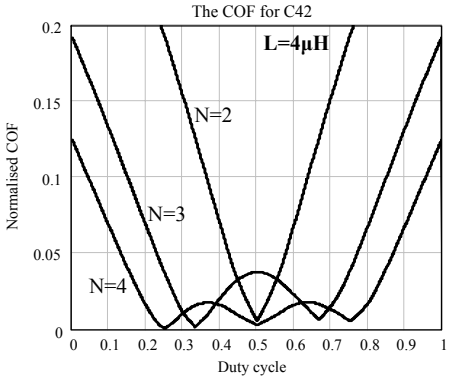



**Figure 4.27a.**

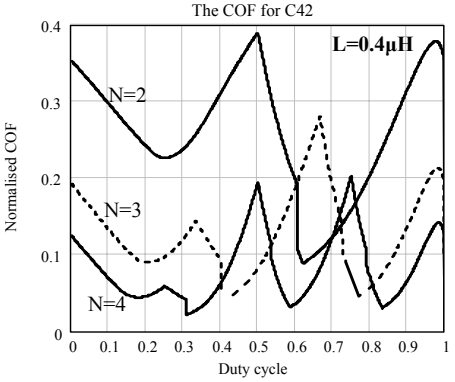



**Figure 4.27b.**

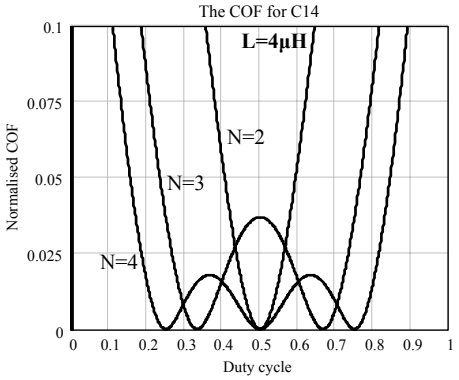



**Figure 4.27c.**

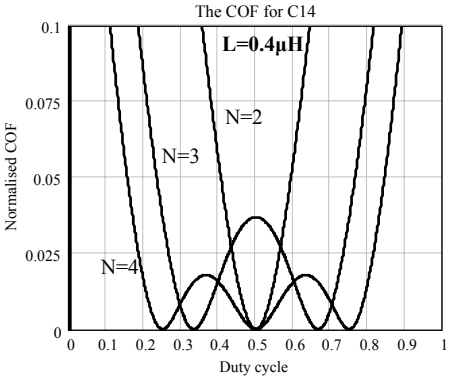



**Figure 4.27d.**

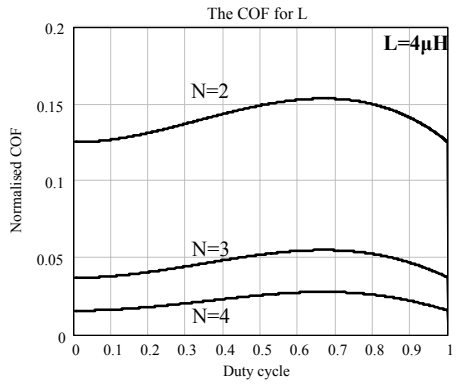



**Figure 4.27e.**

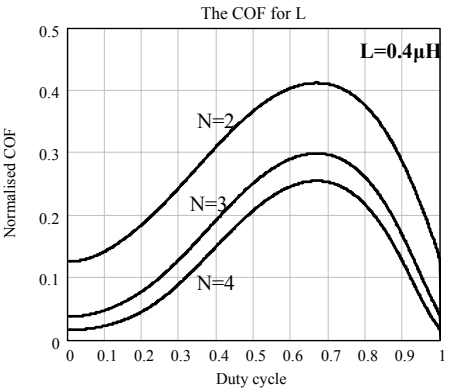



**Figure 4.27f.**

**Figure 4.27. The normalised component optimisation factor for the passive components in a converter with a rated power of 2kW and a switching frequency of 140kHz**

because the current ripple in the inductor becomes dominant in both the energy stored in the component and the RMS current through the component.

From the component perspective, the optimum number of phases is that for which the COF is the smallest for all the passive components at the desired operating point. For example, if the operating duty cycle is 33%, and the inductance is such so as to minimise the RMS current in the passive components (can be selected from Figure 4.22 and Figure 4.24; assume the value of

4μH), then from Figure 4.27 the optimum number of phases is 3 (or multiples of 3) since for this number of phases, the COF is the smallest for most of the passive component. However, if the nominal duty cycle is 33% but the converter must meet the design specification over a duty cycle range of say 20% to 50%, then a 4-phase topology is the better choice because the peak of the COF is smaller for a 4-phase system than a 3-phase system over the duty cycle range.

### *6.1.2 System level*

To determine the optimum number of phases on the system level, the contribution of maximum stored energy and heat dissipated by all the components must be considered and minimised. However, this cannot be done using only the information conveyed in the topology waveforms and an approximation to the losses in the components is required. A new figure of merit, the System Optimisation Factor (SOF), can then be defined as:

$$SOF = E_{\max\_total} \cdot E_{dissipated} \tag{4.27}$$

where $SOF$ is the system optimisation factor [$J^2$],
$E_{max\_total}$ is the total maximum energy stored by all of the passive components [J]
and $E_{dissipated}$ is the total energy lost per switching cycle by all of the passive components [J] and is given as:

$$E_{dissipated} = P_{passive\_components} \cdot T_s \tag{4.28}$$

The product of the total maximum stored energy in all of the passive components and the total energy lost in all of the passive components is selected as the figure of merit to help find the operating point where both are minimised. Each minimum point can be investigated to find the optimum operating point of the system.

The SOF is plotted in Figure 4.28a and normalised in Figure 4.28b to that of a single phase, for the same design specification as used in the previous sections. This is only plotted for the case of a large inductor (4μH). The figure shows that as the number of phases increase, the SOF generally decreases. However, there are regions in the duty cycle where a larger number of phases do not result in the smallest SOF. Further, Figure 4.28b shows that as the number of phases increase, the duty cycle range over which the SOF is reduced increases.

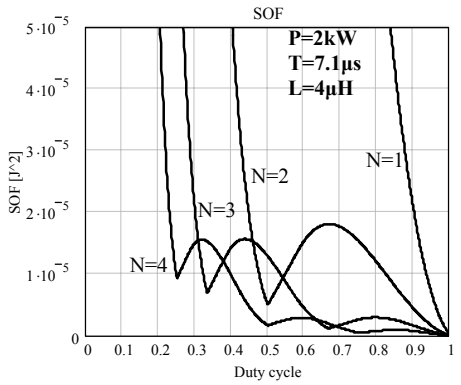



Figure 4.28a.

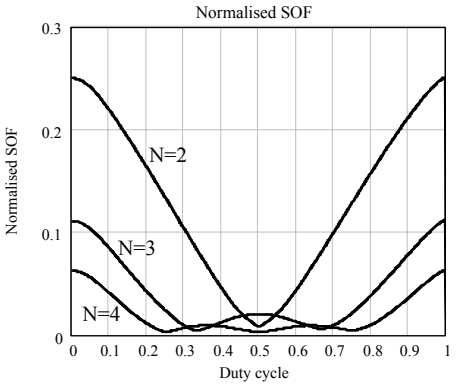



Figure 4.28b.

**Figure 4.28. The system optimisation factor (absolute and normalised) for the N-phase converter**

To determine the optimum number of phases on a system level, the number of phases is chosen so that the SOF is the smallest for or over a given duty cycle range. The accuracy of the calculation depends on how accurate the losses in the different components are modelled.

## 6.2 The component stresses

Component stresses for passive components in terms of processed and dissipated energy were been briefly introduced in Chapter 3 and were defined as:

$$CS = \frac{E_{dissipated}}{E_{processed}} \tag{4.29}$$

where $E_{dissipated}$ is the energy lost in the component [J]
and $E_{processed}$ is the energy processed by the component [J].

Both $E_{dissipated}$ and $E_{processed}$ are known for the passive components assuming the values for the effective series resistance of the passive components are as assumed previously. The component stress, as defined above, is a measure of how much energy is lost for a given amount of processed energy. This gives an indication of how large the component must be given a certain thermal management strategy. The large the component stresses are, the larger the component can be expected to be.

The component stresses, as defined in equation 4.29 are plotted in Figure 4.29 for the component parameters and specifications (including a 1% voltage ripple) as previously defined and for a phase arm inductance of 4μH. Figure 4.29a shows the component stress in $C_{42}$ as a function of the number of phases and the duty cycle. The component stresses in $C_{42}$ normalised to those of a single phase with the same ratings are plotted in Figure 4.29b. Both figures show that as the number of phases increase, the component stresses in $C_{42}$ decrease. There are also local minimums where the component stresses are further reduced. The local minimums create regions where a lower number of phases have lower component stresses than a higher number of phases operating at the same point. This can be used to an advantage in minimising the component volume and losses if it is possible to operate at a local minimum.

Figure 4.29c shows the component stresses in $C_{14}$ and Figure 4.29d shows the same normalised to the component stresses in $C_{14}$ for a single phase topology. The stresses in $C_{14}$ are significantly lower than that in $C_{42}$ for the given phase arm inductance and voltage ripple specification. As the inductance decreases, the difference in the stresses in the two components will also decrease. The two figures also show that it is possible to completely relieve $C_{14}$ of the component stress under certain conditions. This is however not the case in $C_{42}$.

Figure 4.29e and f show the component stress and the component stress normalised to that of a single phase for the inductor respectively. Both figures show that as the number of phases increases the component stresses in the inductor decrease. There are no local minimums in the inductor component stress and the inductor stress cannot be reduced to zero.

In terms of the component stresses, the optimum number of phases is the number of phases where the component stresses in all the passive components are as low as possible for a given set of specifications. For the parameters and specifications used thus far and for an inductance of 4μH, the optimum number of phases is 3 if the duty cycle is 33%. However, if the duty cycle has a range over which the converter must meet specifications, then the optimum number of

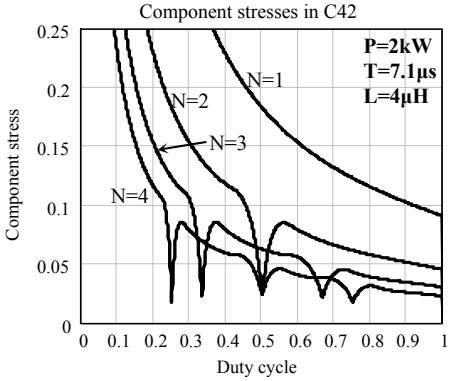



**Figure 4.29a.**

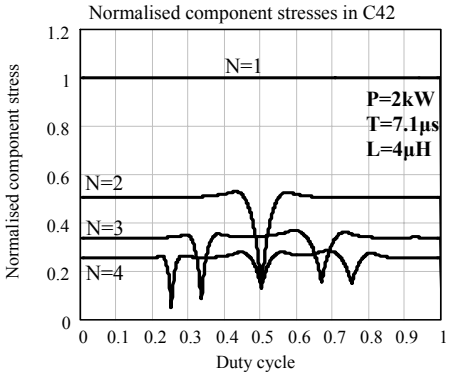



**Figure 4.29b.**

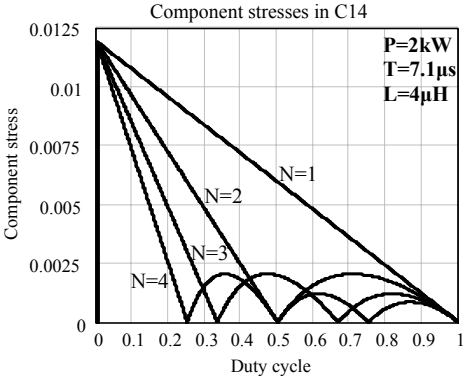



**Figure 4.29c.**

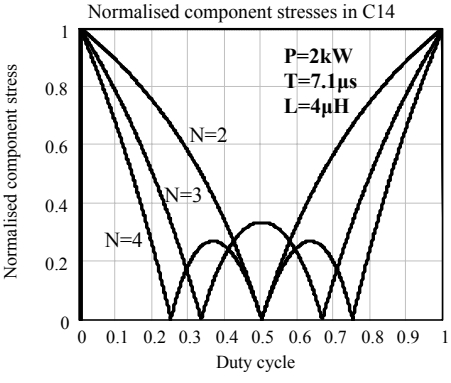



**Figure 4.29d.**

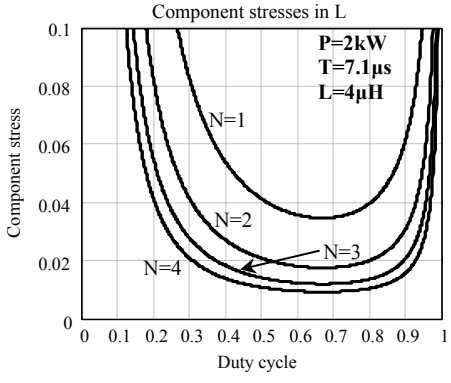



**Figure 4.29e.**

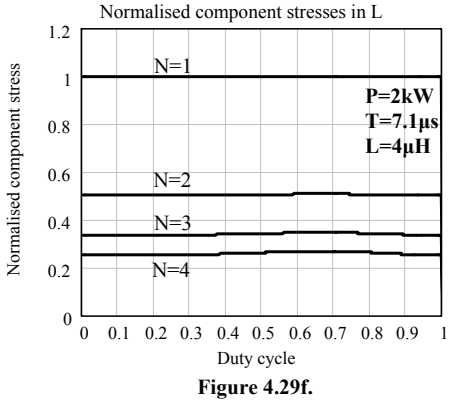



**Figure 4.29f.**

**Figure 4.29. The component stresses for the passive component in a N-phase system as a function of the duty cycle and number of phase**

phases is that which has the lowest overall stresses in the passive components. For the case of the duty cycle having an operating range of 20% to 50%, for example, the optimum number of phases is 4. A higher number of phases is also possible but as has been seen in Figure 4.17, the advantage gained in increasing the number of phases is incremental.

## 7. Summary

In the previous chapter the interdependence between the electrical, the thermal and the spatial

design of an ISM was established. In this chapter, the electrical topology design was considered with reference to this interdependence.

Before the topology can be optimised, the appropriate topology for implementation in the ISM must be identified. There are several issues around the topology that must be considered that have a direct influence on the maximum achievable power density and maximum operating temperature of the topology. These were identified in section 2. Based on these requirements together with the automotive requirements, the multiphase bi-directional synchronous rectifier was selected in section 3 as the topology to be implemented in the automotive ISM (illustrated in Figure 4.2).

Once a topology had been selected, the optimisation of the topology was considered in sections 4 to 6. The topology optimisation seeks to minimise the two outputs of the electrical topology design, namely the maximum energy that must be stored in the topology (coupled to topology volume) and the heat dissipated in the topology (coupled to the operating temperature).

The maximum energy that must be stored in the passive components for the topology to meet electrical specifications is determined along with the total energy that the passive components process in section 4. The maximum stored energy can be used to determine the number of phases requiring the minimum volume for energy storage as illustrated in Figure 4.16 and the total processed energy can be used to help determine the component stresses.

The heat dissipated in the passive components is determined through the RMS currents in the passive components. The RMS currents in the passive components are determined as a function of the number of implemented phases in section 5. Together with approximated values of the components' effective series resistance, the heat dissipated in the ISM can be approximated as in Figure 4.25 and used to help determine the optimum number of phases to implement in the ISM.

In section 6, the maximum energy that must be stored in the passive components and the RMS currents in the components are used together to identify the optimum number of phases to achieve both the minimum energy storage volume and the minimum losses in the passive components. This is achieved by defining two figures of merit, the COF and SOF. In this analysis only the passive components have been considered because the volume contributed to the ISM through the passive components and their corresponding thermal management is significantly greater than that of the active components.

For the automotive ISM application being considered in this thesis, the optimum number of phases is found to be 3 or multiples of 3 since these give both the lowest stored energy and RMS currents in the passive components for a duty cycle of 33% as illustrated in Figure 4.27 and Figure 4.28. However, if the duty cycle varies, then 3 phases is no longer a good choice. For the topology to be optimised over a duty cycle range of 20% to 50% and for the inductance is selected to give the minimum RMS currents, then 4 phases or higher gives the best solution. The maximum number of phases must be limited to a practical value depending on the available materials and construction technologies making a 4-phase topology the most suitable.

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# Chapter 5

## THERMAL MANAGEMENT OPTIMISATION

## 1. Introduction

In Chapter 3, the interdependencies between the electrical, thermal and spatial design domains were identified. Of these interdependencies, manipulation of the electrical design of the topology to be implemented in the automotive ISM was considered in the previous chapter. In this chapter, the thermal design is considered and manipulations are applied to meet the thermal requirements of the ISM.

The thermal design of the components, especially the passive components in the ISM, is critical if the module is to operate successfully in the automotive environment. This chapter begins by first considering what actions must be taken to allow the components to operate in the given environment with the given excitation without using special high temperature components. This is considered in section 2.

In section 3 the thermal management implementation is considered based on the thermal boundary conditions placed on the ISM by the operating environment. The integrated heat sink is defined as a means to implement the required thermal management function capable of achieving the desired temperature drop between the component and the environment. Some examples and advantages of the integrated heat sink are considered.

To illustrate the thermal management concept, a case study is briefly presented in section 4. The case study is an inductor that must be implemented in the ISM. The inductor must have both a small volume and small temperature drop between the maximum temperature in the inductor and the thermal interface of the ISM. Theoretical and experimental results confirm the operation of the inductor and integrated heat sink.

## 2. Operating in high temperature environments

Chapter 3 considered the interactions between the electrical, the thermal and the spatial design of the ISM. The design interaction around the thermal design is briefly repeated in Figure 5.1. The figure shows that the thermal design is connected to the electrical design through the dissipated heat and to the spatial design of the module through the required thermal resistance. The dissipated heat is minimised in Chapter 4 through manipulating the topology and component stresses. On the basis of the amount of heat dissipated and the operating temperature specifications, the required thermal resistance between the heat source and thermal interface can be established. The thermal design of the module is then concerned with how the required thermal resistance can be achieved within the given thermal boundary conditions.

In this section of the chapter, the thermal resistance between the heat source and the thermal interface that is required for the ISM to operate in a high temperature environment is considered. However, before the thermal resistance can be established, the maximum allowed temperature drop must be considered, and this is done in the following section.

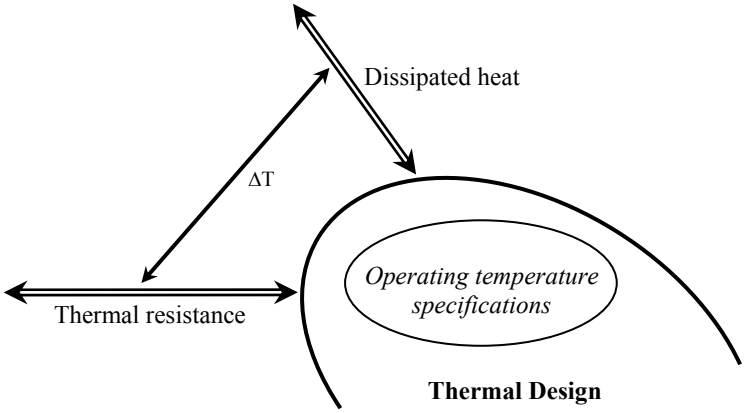


**Figure 5.1. The thermal design as defined in Chapter 3**

## 2.1 Achieving high temperature operation

From a thermal management perspective, the maximum allowed operating temperature of the components within a system or parts thereof forms a fundamental limit on the maximum possible operating temperature of the complete system of components. For the system of components to operate in an environment with a high temperature, the maximum allowable temperature of the components must be at least higher than that imposed on the components by the environment. For example, MOSFETs are currently limited to about 170°C, inductor ferrites to about 200°C (3F3) and capacitors to about 140°C (MKN PEN). Assuming ideal heat transfer to the environment, the maximum environment temperature for a system comprising the above three components is limited by the capacitor to a maximum of 140°C.

Unfortunately the assumption of ideal heat transfer between the components dissipating heat and the high temperature environment is invalid. There is always a temperature difference between the heat source temperature and the environment temperature into which the dissipated heat is being transferred. The temperature difference is [5-1][5-2]:

$$\Delta T = Q \cdot R_t \tag{5.1}$$

where $\Delta T$ is the temperature drop between the heat source temperature and environment temperature [°C],
$Q$ is the heat dissipated in the heat source [W]
and $R_t$ is the thermal resistance of the heat transfer path [°C/W] and is given as [5-1][5-2]:

$$R_t = f\left(R_{t,conduction}, R_{t,radiation}, R_{t,convection}\right) \tag{5.2}$$

where $R_{t,conduction}$ is the thermal resistance of the conduction path [°C/W],
$R_{t,radiation}$ is the thermal resistance due to thermal radiation [°C/W]
and $R_{t,convection}$ is the thermal resistance due to thermal convection [°C/W].

Consider now Figure 5.2. Let the figure represent the temperature drop ($\Delta T$) across two different thermal management implementations, one with a low thermal resistance and one with a high thermal resistance. The vertical axis represents the absolute temperature and the horizontal axis represents the dissipated heat.

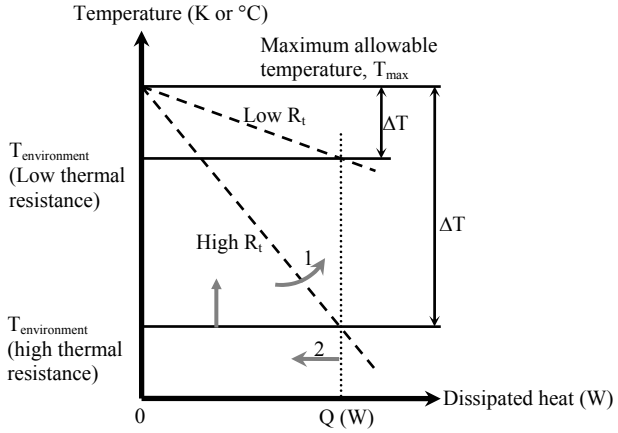


**Figure 5.2. The maximum thermal interface temperature in terms of the thermal resistance**

On the temperature axis, there is a maximum temperature that cannot be exceeded by the individual components and/or the system of components, $T_{max}$. This is the fundamental temperature limit on the components that must not be exceeded in order for thermal failure to be avoided. For a given amount of dissipated heat transported to the environment, there is a temperature drop between the heat source and the environment defined by equation 5.1. The maximum environment temperature that the system of components can operate in is then defined as:

$$T_{environment} = T_{max} - Q \cdot R_t \tag{5.3}$$

where $T_{max}$ is the maximum allowable temperature [°C]
and $T_{environment}$ is the maximum possible environment temperature [°C].

This temperature is illustrated in Figure 5.2 for the two different thermal resistances and dissipated heat, $Q$. As the thermal resistance decreases for a fixed amount of dissipated heat, the gradient of the diagonal line which represents the thermal resistance decreases and the resulting maximum environment temperature increases.

Considering Figure 5.2 further, it can be seen how the maximum environment temperature of the converter system can be increased. There are two ways of achieving this. The first possibility, labelled 1 in Figure 5.2, is by decreasing the thermal resistance of the implemented thermal management structure. This can be achieved through manipulating the thermal management structure material properties and geometries. The reduced thermal resistance will reduce the temperature drop, $\Delta T$, for a given amount of dissipated heat increasing the maximum environment temperature. The second possibility, labelled 2 in Figure 5.2, is to decrease the amount of heat transported by the thermal management structure with a fixed thermal resistance. This will result in an increased maximum environment temperature. Combinations of these methods are also possible.

In order to operate in an environment with a high temperature using conventional components it is necessary that these components have a maximum temperature that is higher than the maximum environment temperature. Moreover, both the thermal resistance between the component and the environment, and the heat dissipated in the component must be reduced. This is necessary to prevent the components from exceeding their maximum temperature.

In the case of the ISM, the environment temperature is the thermal interface temperature (module base plate). The thermal interface is considered as the module's thermal environment because all of the dissipated heat must be transported to and through the thermal interface [5-3]-[5-5]. This is the only path available for transporting the dissipated heat to the vehicle coolant since it is assumed that thermal convection and radiation do not contribute to the thermal management of the ISM.

### 2.2 Operating in a high temperature environment vs. a "normal" environment

The thermal design of a system operating in a high temperature environment is significantly different from that of the same system operating in a normal environment using the same components. A normal environment is considered as one where the environment temperature is limited to room temperature. This is the environment in which the majority of commercial power supplies operate.

The primary difference in the two designs is the maximum allowable thermal resistance between the components and the environment. In a high temperature design, the maximum allowed thermal resistance can be significantly smaller than that of the more conventional design with similar electrical excitation, components and dissipated heat. As a consequence of the smaller thermal resistance in the high temperature design, different approaches are used to implement the thermal management [5-6]. For example, in a high temperature design with a small allowable thermal resistance, the thermal management structure has to transport the dissipated heat to the environment much more effectively than in more conventional designs [5-4][5-5]. This requires more attention and effort to be given to the design and implementation of the thermal management system. Simply using a larger heat sink is insufficient. Operating in a high temperature environment with a high power density requires the simultaneous optimisation of the electrical, thermal and spatial design of the system.

## 3. Thermal management in the ISM

The thermal management to be implemented in the ISM for operating in high temperature environments has been briefly introduced in Chapter 2 and broadly defined in Chapter 3. In this section the thermal management implemented in the module is considered in more detail. With the desired thermal resistance known from the previous section, methods of achieving the thermal resistance are required.

### 3.1 The integrated heat sink concept

In Chapter 2, it was assumed that the heat dissipated by all the components within the ISM must be transferred to the environment through the module's thermal interface. A method of collecting and transporting the dissipated heat to the thermal interface is considered in this section.

#### *3.1.1 Thermal management boundaries conditions*

The boundary conditions for the IMS are illustrated in Figure 5.3 for an arbitrary component within the module. Let the exterior of the ISM be the control volume over which all the heat leaving the module must flow. The temperature is unknown on the top and side surfaces of the control volume. All that is known on these boundaries is that there is no heat flowing over the boundaries in the $y$ direction for the top boundary and the $x$ direction for the side boundaries. Thus the heat flux vector component in the $y$ direction on the top boundary and in the $x$ direction on the side boundaries is zero. This is known as a Neumann boundary [5-7].

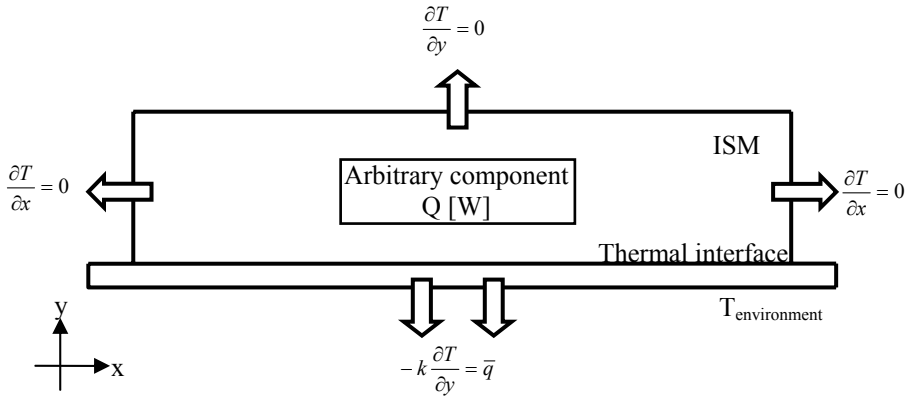


**Figure 5.3. The ISM with the assumed thermal boundary conditions**

On the bottom of the control volume there is a constant temperature surface. It has been assumed that the thermal interface, which is the bottom boundary of the control volume, has a temperature that is equal to $T_{environment}$ considering that in the automotive application, the environment is the engine coolant. This temperature is assumed to be constant across the boundary because of the high thermal conductivity of the base plate. There is heat flow over this boundary in the negative $y$ direction. The amount of heat flow is determined by the heat dissipated within the ISM. This type of boundary is known as a Dirichlet boundary [5-7].

The heat that is dissipated in all of the components within the ISM must be collected and transported to the thermal interface within these boundary conditions. This is achieved with a novel method referred to as the integrated heat sink [5-3][5-4][5-5][5-8].

### *3.1.2 Integrated heat sink structure*

The integrated heat sink is a novel structure that is used to collect heat that is dissipated in any component and transport it to the thermal interface using only thermal conduction within the maximum $\Delta T$ allowed between the component and the thermal interface. In other words, it is a thermal management technique that gives the low thermal resistances that are required to operate with a high temperature environment.

Consider an arbitrary component with a moderate loss density (an inductor for example). Figure 5.4 shows the inductor structure in an arbitrary location within the ISM but not necessary in contact with the thermal interface. Let the inductor dissipate heat, thereby defining its loss density. The heat dissipated in the inductor must be collected and transported to the thermal interface while not exceeding the allowable $\Delta T$ between the component and thermal interface. This is achieved by the structure surrounding the inductor in Figure 5.4 – the integrated heat sink structure. The integrated heat sink is shown to consist of two clearly distinguishable parts. The first, referred to as the heat collector, is the part in immediate and intimate contact with the inductor structure, while the second part, referred to as the heat transportation path (or just heat path), is responsible for transporting the heat collected by the heat collector to the thermal interface.

There is a temperature drop over both the heat collector and heat path that is determined by the amount of heat being transported, the integrated heat sink's geometry and material properties. Manipulating any of these will change the temperature drop between the heat source and thermal interface, allowing the desired $\Delta T$ or thermal resistance to be established.

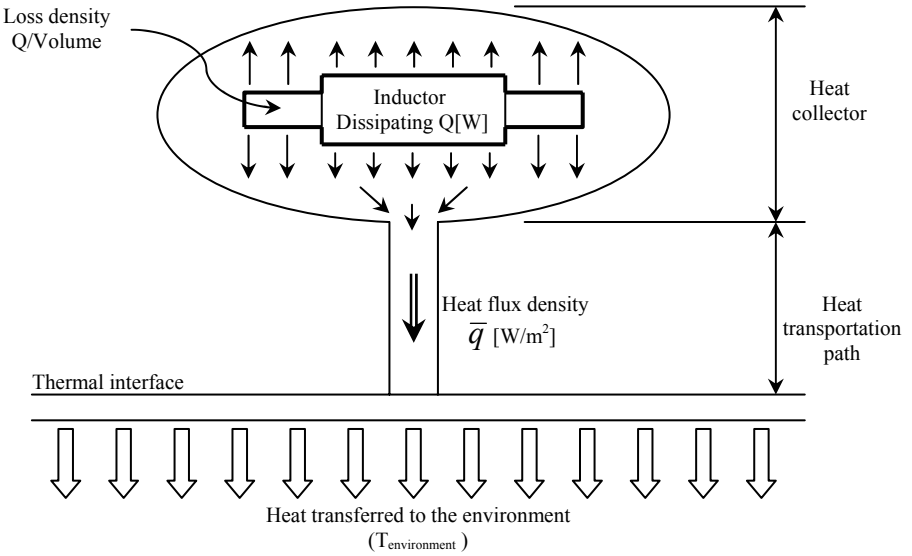


**Figure 5.4. The integrated heat sink for a passive component using only thermal conduction**

The integrated heat sink structure can, in principle, be used to collect and remove the heat dissipated in any component within the ISM irrespective of the component's loss density or location within the module. The primary limitations on the effectiveness of the integrated heat sink are geometrical and material property-based. Since the integrated heat sink conducts heat from the heat source to the environment, the thermal conductivity of the material implementing the integrated heat sink, the distance the heat is transported and the cross-sectional area of the heat paths all play a major role in the integrated heat sink's performance.

## 3.2 Heat paths, heat collectors and heat spreaders

There is a strong similarity between the integrated heat sink and heat spreader structures, with only the function of the heat spreader and the heat collector being reversed. This is illustrated in Figure 5.5. The function of the heat spreader is to reduce the heat flux density of a high loss density component while that of the heat collector is to increase the heat flux density of a low loss density component.

In the following section heat paths and heat collectors are considered individually in addition to heat spreaders.

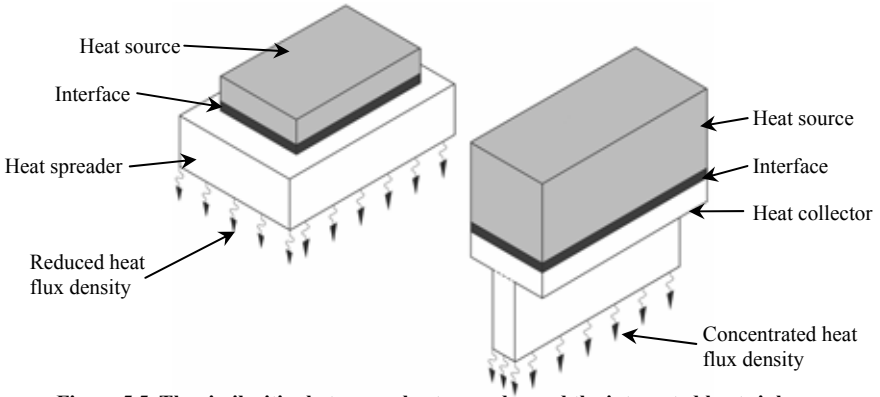


**Figure 5.5. The similarities between a heat spreader and the integrated heat sink**

### 3.2.1 Heat paths

Heat paths are defined as geometrical structures that are designed to transport heat between two points, in this case, the heat collector / heat spreader and the thermal interface. In transporting the heat, there is a temperature drop across the heat path defined by Fourier's law of heat conduction [5-8]:

$$\begin{aligned}\overline{q} &= -k\nabla T \\ &= -k\left(\frac{\partial T}{\partial x}\hat{x} + \frac{\partial T}{\partial y}\hat{y} + \frac{\partial T}{\partial z}\hat{z}\right)\end{aligned} \tag{5.4}$$

where $k$ is the thermal conductivity [W/m·°C],
and $\hat{x}$, $\hat{y}$ and $\hat{z}$ are the unit vectors in the $x$, $y$ and $z$ direction respectively.

If it is assumed that the heat path is implemented with a material that has a high thermal conductivity and a uniform cross-sectional area, and that all the heat entering the heat path at one end leaves at the other end, then the heat path can be approximated as a one-dimensional heat conductor with a uniform or near uniform heat flux density. Under this assumption, equation 5.4 can be simplified to:

$$\frac{Q}{A} = k\frac{\Delta T}{l} \tag{5.5}$$

where $Q$ is the heat being transported by the heat path [W],
$\Delta T$ is the temperature drop over the heat path [°C],
$A$ is the cross-sectional area of the heat path [$m^2$]
and $l$ is the length of the heat path [m].

Equation 5.5 can be rewritten as:

$$\Delta T = \frac{l}{kA}\cdot Q \tag{5.6}$$

where the thermal resistance of the heat path is defined as:

$$R_{heat\ path} = \frac{l}{kA} \tag{5.7}$$

with $R_{heat\ path}$ is the thermal resistance of a one-dimensional heat path [K/°C]

Equation 5.7 shows that the thermal resistance of the heat path is a function of the heat paths geometry (length and cross-sectional area) and the thermal conductivity of the material implementing the heat path.

Consider two heat paths, one implemented with ceramic ($k_{Al2O3}$≈24W/m·°C) and the other implemented with a metal ($k_{copper}$≈385W/m·°C). Let both of the heat paths have the same thermal resistance and cross-sectional area. The ratio of the lengths of the two heat paths can then be written in terms of the materials thermal conductivities as:

$$\frac{l_{copper}}{l_{ceramic}} = \frac{k_{copper}}{k_{ceramic}} \tag{5.8}$$

and is dimensionless.

Equation 5.8 shows that if the cross-sectional area and the thermal resistance of two heat paths are the same, then the ratio of the lengths of the heat paths is equal to the ratio of the thermal conductivities of the materials used to implement the heat paths. This is significant because if two different components are dissipating the same amount of heat and using the two different heat paths, the distance between the components and the heat sink can be significantly different for the same $\Delta T$. For the given example, the heat path implemented with copper is approximately 16 times longer than that implemented with the ceramic for the same $\Delta T$ and cross-sectional area.

The significantly different heat paths lengths can be taken advantage of in the IMS to transport heat greater distances without the penalty of a high $\Delta T$. This is illustrated in Figure 5.6 showing two different heat paths, one for the inductor in the integrated heat sink and one for the switching device, both achieving the required $\Delta T$ along the heat path by using different geometries and thermal conductivities.

The heat path for the inductor structure can be implemented with a material that has a very high thermal conductivity, such as a metal. This results in a heat path that can have a significant length for a relatively small cross-sectional area and an acceptable $\Delta T$. The second heat path is implemented between the switching device and the thermal interface. The heat path must provide electrical isolation between the device and the thermal interface, so an electrically conductive material cannot be used. A ceramic is normally used for this function. The ceramic, having a much lower thermal conductivity has a significantly shorter length than the heat path implemented for the inductor.

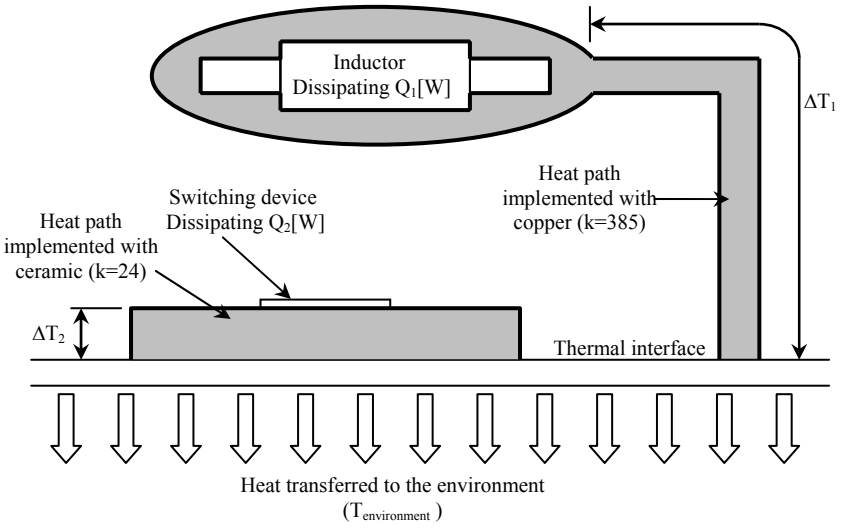


**Figure 5.6. Two heat paths with significantly different lengths and material properties both achieving the required $\Delta T$**

The long heat path of the integrated heat sink allows significant freedom in the location of the component within the ISM. The component can be placed almost anywhere with the module, allowing a more three-dimensional approach to the module compared to the relatively two-dimensional approach seen in conventional modules. Further, the heat path also allows freedom as to where the heat is transferred to the thermal interface. The point where the heat path comes into contact with the thermal interface does not necessary need to be in the vicinity of the component but can be quite a distance away. In addition it can also significantly reduce the surface area on the thermal interface that the component would require to transfer the heat dissipated in it to the thermal interface. This can be seen in Figure 5.6 by considering the surface area of the inductor that would be used to transfer heat to the thermal interface with the cross-sectional area of the heat path.

### *3.2.2 Heat collectors*

A heat collector is defined as a component of the integrated heat sink structure that gathers and collects the heat that is dissipated in an arbitrary component and transports it to the heat path where the dissipated heat is transported to the environment. An example of a heat collector is illustrated in Figure 5.7, which shows an arbitrary component with a moderate loss density in a heat collector with all the dissipated heat being conducted to the thermal interface.

The heat dissipated in the component is collected over all the surfaces where the heat collector is in thermal contact with the component. Depending on the relative surface area of the component in contact with the heat collector and the dissipated heat, the heat flux density of the heat flowing from the component to the heat collector is relatively low. The heat collector then concentrates the heat flux density as the dissipated heat flows towards and into the heat path. A temperature drop between the component hot spot and the entrance to the heat path will exist that is a function of the dissipated heat, the material and geometrical properties of both the component and the heat collector.

The heat flux density in the heat path will be significantly larger than that flowing out of the component due to the smaller conduction area. The large heat flux density in the heat path will result in a large $\Delta T$ between the heat collector and the thermal interface. However, by manipulating the cross-sectional area or the material properties of the heat path, the $\Delta T$ can be maintained within the allowable range.

All of the heat dissipated in the component must be transferred to the heat path through the heat collector. Further, the heat collector will most likely have to be electrically isolated from the component if a metal is used to implement the heat collector. Electrically insulating

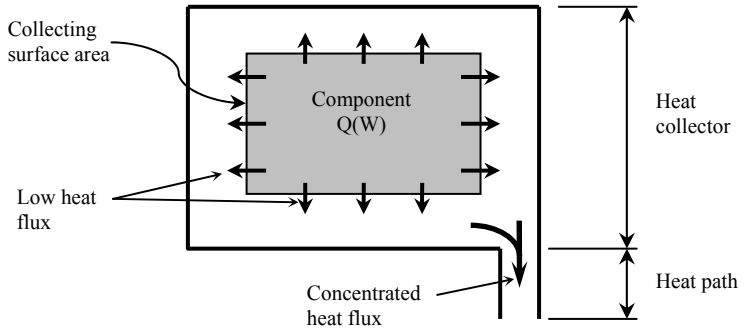


**Figure 5.7. A heat collector for an arbitrary component with a moderate loss density**

materials normally have very low thermal conductivities, thus a large temperature drop can exist over the electrically insulating material. To minimise the temperature drop between the component and the heat collector, the largest possible area should be used to transfer heat from the component to the heat collector. The area used to transfer heat from the component to the heat collector is called the heat collection area. Ideally, the heat collection area should be as large as the component's surface area is. This ensures the lowest possible heat flux density between the component and heat collector for a given heat loss, minimising the temperature drop across the electrical isolation.

A trade-off exists between the temperature difference between the component's maximum temperature and the entrance to the heat path's temperature and the volume of the heat collector. This trade-off is specific to the component and heat collector's geometry. This is due to the relationship between the heat flux density in the heat collector and the heat collector's volume and geometry for a given heat loss. As the heat collectors volume increases for a given component geometry, the heat flux density in the heat collector decreases assuming a high thermal conductivity. The reduced heat flux density will result in a lower $\Delta T$ between the component and the heat path. For a given heat loss and $\Delta T$, an optimum volume (both component and heat collector) exists that is specific to the component. This is considered further in the following chapter concerning the volumetric optimisation of the component and integrated heat sink.

### *3.2.3 Heat spreaders*

Heat spreaders are a well-known technique to reduce the temperature between a component with a very high loss density and the heat path to the environment [5-9][5-10]. A typical heat spreader for an arbitrary component with a very high loss density is illustrated in Figure 5.8. The figure shows the heat source on top of the heat spreader. The heat flux flows out of the heat source having a small cross-sectional area and enters the heat spreader highly concentrated. The heat spreader is typically implemented with a material that has a high thermal conductivity. The concentrated heat flux density is then spread out horizontally through the heat spreader perpendicular to the direction it entered the heat spreader. The heat flux exits the heat spreader with a much lower heat flux density due to the larger area that it flows through. The heat is then transported to the thermal interface through a heat path. A typical example of such an implementation is an active switching device mounted on a DBC carrier. The thick copper conductor between the switching device and the ceramic functions as the heat spreader and the ceramic layer is the heat path to the thermal interface.

The heat spreader reduces the temperature drop between the component and the heat path by reducing the heat flux density flowing through the heat spreader. This function is the exact

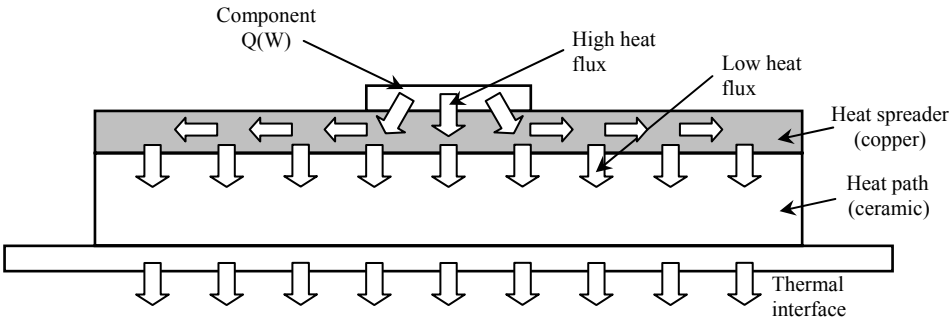


**Figure 5.8. A heat spreader for an arbitrary component with a very high loss density**

opposite to that of the heat collector. Both the heat spreader and the heat collector establish a desired temperature drop between the component and heat path by manipulating the heat flux flowing from the heat source to the heat path.

### 3.3 Placing passive components in the third dimension

An advantage of the integrated heat sink structure is that the components (typically passive components) are connected to the thermal interface only through the heat path leading from the heat collector. The cross-sectional area of the heat path is the only area in contact with the thermal interface that the component requires for a given $\Delta T$. This cross-section area can be significantly smaller than the component's footprint, resulting in significantly less area being occupied on the thermal interface by components with low and moderate loss densities.

The small cross-sectional area and length of the heat path allows the component in the integrated heat sink structure to be placed sufficiently high above the thermal interface to make volume beneath it available for another heat source, possibly with a higher loss density. In other words, the heat path of the integrated heat sink structure can be used to place specific components in the third dimension (the height) of the ISM, reducing the required surface area on the thermal interface. This is illustrated in Figure 5.9, which shows two integrated heat sink structures arranged above each other and sharing a common thermal interface to the environment.

The top integrated heat sink structure in the figure is used to remove the heat dissipated in components with moderate loss densities (such as passive components) and is typically implemented with heat collectors and heat paths. These components are located above a second integrated heat sink structure which is used to remove the heat from components with high loss densities (such as active components). This integrated heat sink structure is typically implemented with heat collectors and/or heat spreaders together with the required heat paths. By reducing the surface area that the low and moderate loss density components require on the thermal interface, more of the available area can be dedicated to achieving the thermal resistance required for the high loss density components which normally require larger surface areas for heat spreaders.

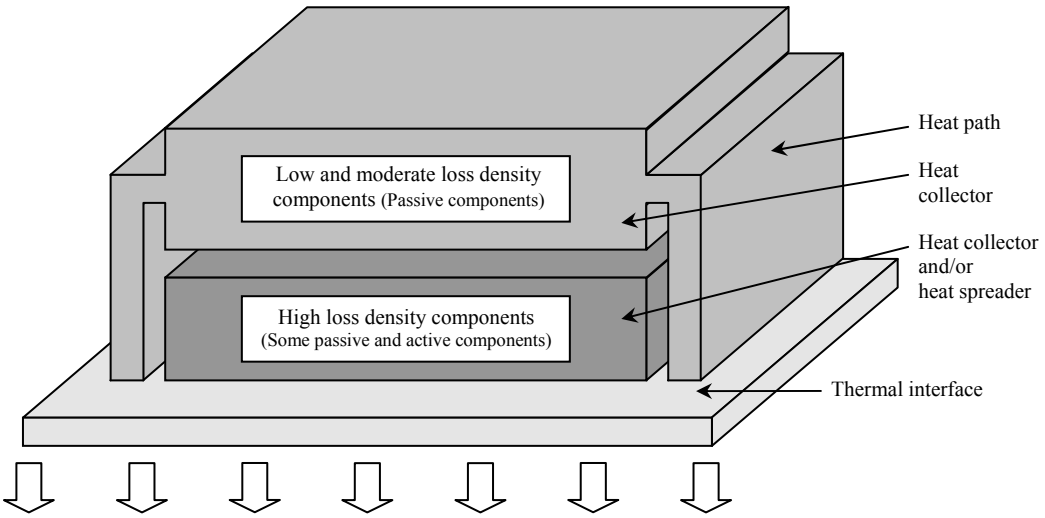


**Figure 5.9. Using the integrated heat sink structure to place components in the 3rd dimension**

Being capable of placing components in the third dimension and still transporting the heat dissipated in the components to the thermal interface helps create significant freedom in the mechanical and spatial design of the ISM. Components can be placed almost anywhere within the module, allowing more focus to be placed on the geometric design of the module while still meeting the thermal and power density specifications.

# 4. Realisation of the integrated heat sink

In this section some practical issues surrounding the implementation of the integrated heat sink structure are considered.

## 4.1 Realising the required thermal resistance

The required thermal resistance can be determined from equation 5.3 in terms of the environment and maximum material temperature as:

$$R_{t,\max} = \frac{T_{\max} - T_{environment}}{Q} \tag{5.9}$$

where $R_{t,max}$ is the maximum allowable thermal resistance of the total heat conduction path [°C/W].

The final implementation of the integrated heat sink and component combination must have a thermal resistance that is at least equal to or smaller than $R_{t,max}$. The realised thermal resistance of the integrated heat sink and component structure can generally be expressed as:

$$R_{t,\max} = f(R_{t,component}, R_{t,heat\ collector}, R_{t,heat\ path}) \tag{5.10}$$

where $R_{t,max}$ is the allowed thermal resistance between the component hotspot and the thermal interface (the environment) [°C/W],
$R_{t,component}$ is the thermal resistance between the component hotspot to the component surface [°C/W],
$R_{t,heat\ collector}$ is either the heat collector's or heat spreaders thermal resistance [°C/W]
and $R_{t,heat\ path}$ is the thermal resistance of the heat path [°C/W].

The exact thermal resistance is a function of the material properties and geometries used to implement the integrated heat sink structure and component.

Figure 5.10 shows three possible implementations of passive components with an integrated heat sink to achieve the required thermal resistance. The figures all have a section of the integrated heat sink removed to reveal the component within the structure. The figures only show the implementation on a conceptual level, so details such as electrical isolation have not been included.

Figure 5.10a and b show two possible implementations of a planar magnetic component, specifically an inductor, in the integrated heat sink. The first example, Figure 5.10a shows the inductor structure in the heat collector with only one heat path leading from the heat collector to the thermal interface. Figure 5.10b also shows the inductor in a heat collector but with two heat paths leading from the heat collector. In addition, the heat paths are located in different positions relative to the inductor. The number of heat paths leading from the heat collector

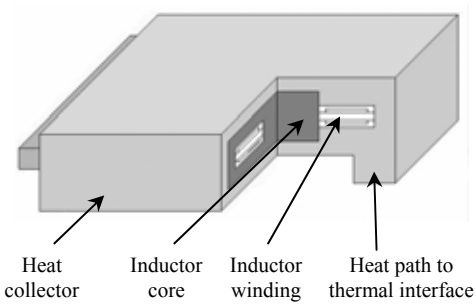


**Figure 5.10a. An inductor in integrated heat sink structure with a single heat path**

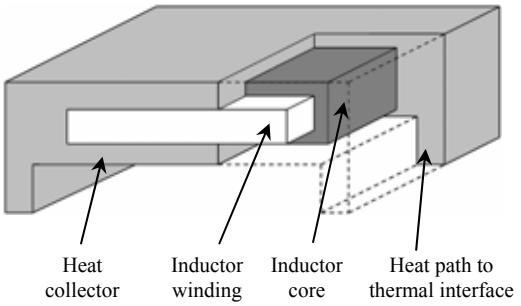


**Figure 5.10b. An inductor in integrated heat sink structure with a dual heat path**

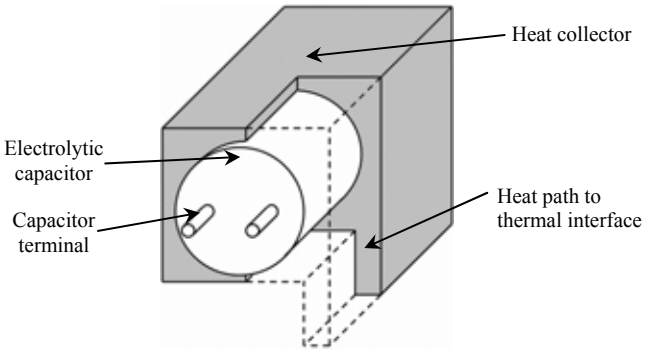


**Figure 5.10c. An electrolytic capacitor in integrated heat sink structure with a single heat path**

**Figure 5.10. Three examples of passive components mounted in integrated heatsink structures**

depends on the maximum allowed temperature drop over the heat path together with the heat path's geometry and materials properties. If the temperature drop over the heat path is too large and the geometry or material cannot be manipulated further, then additional heat paths are required.

In both examples, the inductor core and winding are clamped in the heat collector. If the inductor windings are implemented in a planar fashion, then clamping the windings in the heat collector can provide a very low thermal resistance path for the heat dissipated in the windings to the heat collector. This can contribute to reducing the volume of the inductor and helping to increase the ISM power density.

The third example, in Figure 5.10c, is an electrolytic capacitor mounted horizontally in an integrated heat sink structure with a single heat path leading from the heat collector to the thermal interface. The capacitor is mounted horizontally to maintain a low profile. It is also possible to implement additional heat paths depending on the capacitor's loss density.

Implementing the electrolytic capacitor in the integrated heat sink structure can help to reduce the de-rating that the capacitor must undergo for a given maximum temperature, assuming the thermal interface temperature is lower than the maximum capacitor temperature. This is due to the fact that the thermal resistance between the component and the thermal interface can be significantly lower in the case of the integrated heat sink as compared to natural convection resulting in significantly more heat being required for the same maximum temperature. This

allows the component to operate with a higher loss density without exceeding the capacitor's maximum allowed temperature.

The three examples are all implemented with the maximum heat collection area possible. This is required to reduce the heat collector's thermal resistance, including the thermal resistance over the electrical isolation between the component and the physical heat collector. In the case of the inductor structure, all the available surfaces with the exception of the surface where the winding connections protrude from the component are in thermal contact with the heat collector. Similarly for the capacitor, the only surface not in thermal contact with the heat collector is the surface where the capacitor terminals are located.

### 4.2 Redistribution of dissipated heat within the component

The temperature drop over the heat collector and the heat path can be fine tuned to that required. However, the temperature drop from within the component to the heat collector is more difficult to manipulate because considerations other than thermal must also be considered (electromagnetic for example) and can have a higher priority. For example, materials that have low thermal conductivities that dissipate and conduct heat can have large temperature drops over them, but their geometries are fixed by the required electromagnetic function. A ferrite core is an example.

The large temperature drops over materials with low thermal conductivities can be significantly reduced by redistributing the losses within the component. Consider an inductor, for example. Inductors are conventionally designed to have approximately the same loss in both the inductor core and winding [5-2]. This criterion is set by the fact that the inductor must transfer the heat dissipated in it to the environment through a combination of thermal convection, thermal conduction and thermal radiation. However, in the case of the integrated heat sink structure, heat is removed only with thermal conduction requiring the loss distribution within the component to be rethought.

To minimise the temperature drop between the component and the heat collector, the largest portion of the losses should be located in a part of the component that is in direct thermal contact with the heat collector and has a high thermal conductivity. This ensures a low thermal resistance between the heat source and the heat collector, obviating the need for the heat to travel through a material with a low thermal conductivity. The inductor winding is just such a part. By establishing a good thermal connection between the inductor winding and the heat collector, a large heat flux flowing out of the winding into the heat collector can be established with a small temperature drop. This avoids the need for the heat dissipated in the winding to travel through the inductor core to the heat collector, helping to reduce the maximum temperature in the core material.

Establishing a good thermal connection between the inductor winding and the heat collector can be achieved as illustrated in Figure 5.10a and b, which show the inductor winding clamped in the heat collector. All of the heat in the inductor winding can then flow directly out of the winding and into the heat collector through the winding clamp.

### 4.3 Electromagnetic interaction within the integrated heat sink structure

Due to the close proximity of the integrated heat sink structure and the component within the heat collector, it can be expected that there is some electromagnetic interaction between the component and the integrated heat sink. This is especially the case when a part of the component such as the inductor winding is clamped in the heat collector.

By clamping the inductor winding in the heat collector, the thermal resistance between the thermal interface and the component can be significantly reduced. To maximise the heat transfer from the inductor winding to the heat collector, the winding clamp must be as close as possible to the winding. However, as the winding is brought closer to the winding clamp of the heat collector, the current in the inductor and the resulting magnetic fields will interact with the heat collector, especially if the heat collector is implemented with an electrically conducting material [5-5]. The result is that eddy currents will be induced in the winding clamp in the vicinity immediately around the winding clamp which will have an effect on the current distribution in the inductor winding.

The eddy currents induced in the heat collector will result in additional losses in the inductor and integrated heat sink structure. However, the redistribution of the current in the inductor winding in the winding clamp does not necessarily mean an increase in the total losses. In reference [5-5] it was seen that the total losses in the inductor and integrated heat sink structure were reduced due to the improved current distribution in the inductor winding in the winding clamp.

The consequence of the electromagnetic interaction between the component and the integrated heat sink will be different for different components, material and geometries. This is considered further in the following section of this chapter.

### 4.4 Thermal expansion

As the integrated heat sink and component's temperature changes, the physical dimensions of the different materials will also change due to the materials all having different coefficients of thermal expansion[a]. If the heat collector is dimensioned to fit exactly around the component it is collecting the heat from, then the space required for the thermal expansion of the different materials is not available. This will result in significant stresses building up in the different materials that can lead to the failure of the component or integrated heat sink. However, since thermal conduction is the only means available for the transport of heat, it is required that the surfaces of the heat collector and heat sources be in very good thermal contact.

A solution to the contradictory requirements is to place an additional material between the component and the heat collector that performs the functions of stress relief and electrical isolation while establishing a good thermal connection. This can be achieved by using a thermal interfacing material that has good electrical isolation properties, good thermal properties (good compared to air) and is mechanically compressible.

Figure 5.11 illustrates how this interfacing material is implemented in the integrated heat sink structure. The heat collector is dimensioned just slightly larger than the component and the space between the component and the heat collector is filled with the compressible, electrically isolating, thermally conducting interfacing material. Figure 5.11 shows a cross-section through an inductor core and winding clamped in the heat collector. When the temperature of the various parts is increased and the dimensions change, then the interfacing material inserted between the heat collector and component absorbs the stress across it, preventing the stress building up in the other materials. The pressure over the interfacing material also helps to ensure good thermal contact between the hard and irregular surfaces of the heat collector and component. Such materials are available from several manufactures with Chomerics$^{TM}$ being an example.

[a] $CTE_{copper} \approx 16.6$ ppm, $CTE_{aluminium} \approx 25$ppm, $CTE_{ferrite} \approx 7 – 10$ppm, $CTE_{Al2O3} \approx 6.7$ppm

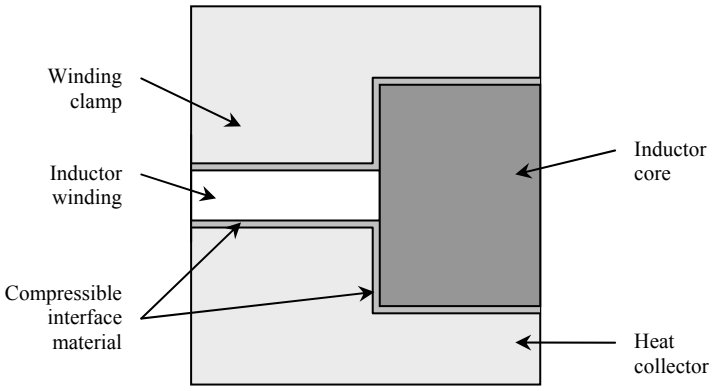


**Figure 5.11. A section of the inductor in the heat collector showing the electrically isolating, thermally conductive compressible interface material**

## 5. Implementation – A case study

In this section of the chapter, the design, implementation and experimental evaluation of a case study illustrating the integrated heat sink structure is presented. The case study considered is the phase arm inductor operating in the synchronous rectifier topology considered in Chapter 4 that is rated for 500W at 14/42V. The phase arm inductor is selected for the case study because of the flexibility available in the component design compared to that of the bus capacitors. The inductor design is not presented in this section but focus is placed on the design and implementation of the integrated heat sink structure.

The integrated heat sink structure that the inductor is implemented in is that illustrated in Figure 5.10b with two heat paths between the heat collector and the thermal interface. For the purposes of illustration, the integrated heat sink structure is designed for a temperature drop between the highest temperature in the inductor and the thermal interface of approximately 10°C for nominal load. In the interest of completeness, all the material and geometrical properties are also presented.

### 5.1 The inductor structure

The inductor to be implemented in the integrated heat sink structure is illustrated in Figure 5.12. The figure shows a planar inductor with the winding and ferrite isolation removed for illustration purposes.

The inductor is implemented with a multi-layer planar winding and two standard ferrite E-cores. The winding is manufactured from several segments stamped out of 0.75mm thick copper foil that are wielded together (laser wielding) to result in the structure shown in the figure. The respective winding layers are isolated from each other with a layer of thermally conductive, electrically isolating material known as Bond Ply™. This material has a high temperature adhesive on both side of the isolation and is used to hold the winding structure together in addition to providing electrical isolation.

The ferrite is isolated from the copper conductors and the integrated heat sink with a flexible fibreglass mesh that is impregnated with fine ceramic beads and a thermally conductive compound. The thermally conductive compound provides good heat conduction between surfaces and the fibreglass base prevents electrical and mechanical breakthrough while absorbing any thermally induced stresses. The material is manufactured by Chomerics™. The integrated heat sink structure is implemented with aluminium.

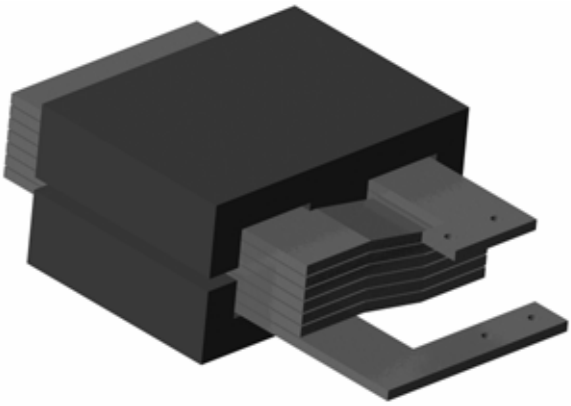

**Figure 5.12. The inductor to be implemented in the integrated heat sink structure**

The implemented inductor is rated for a maximum average current of 45A (peak current of 53.5A) with an inductance of 3.8µH operating with a frequency of 140kHz. The inductor is excited by the synchronous rectifier, which operates over the voltage range of $30V \leq V_{42} \leq 50V$ and $11V \leq V_{14} \leq 16V$. At nominal voltages ($V_{14}$ = 14V and $V_{42}$ = 42V) the nominal inductor current is 37.5A with a peak to peak current ripple of 17A.

The inductor has overall dimensions of: height = 11.4mm, depth = 26.8mm, and width = 21.8mm.

The inductor is implemented with two ferrite E-cores with the following properties:

- Magnetic core: 2 × ELP 22/6/16 manufactured by Epcos
- Core material: N92
- Saturation flux density: 500mT @ 25°C, 440mT @ 100°C
- Initial permeability: 1500 ± 25%
- Effective length: 32.5mm
- Effective area: 78.3mm$^2$
- Effective volume: 2540mm$^3$

The inductor design yields the following design parameters:

- Number of turns: 7
- Winding cross-section 5mm by 0.75mm
- Air gap 2 × 0.9mm
- Nominal current density 10A/mm$^2$
- Maximum current density 14.3A/mm$^2$

The current density in the inductor winding is significantly higher than for conventional inductor designs [5-2]. The current density is increased to reduce the volume of the inductor winding at the cost of increased conduction losses. The losses in the inductor and integrated heat sink structure are considered in the following section.

## 5.2 The integrated heat sink and dissipated heat

To design the integrated heat sink structure, the heat dissipated in the inductor must be known. Further, since the inductor is implemented in such close proximity to another electrically

conductive material, it is expected that there is some electromagnetic interaction between the inductor and integrated heat sink.

The electromagnetic interaction between the inductor and the integrated heat sink structure is in the form of eddy currents that are induced in the heat sink structure due to magnetic flux that leaks into the integrated heat sink structure [5-5][5-11]. This occurs primarily in the region of the air gap in the inductor core and where the inductor winding is clamped in the integrated heat sink. The eddy currents that are induced in the integrated heat sink result in localised heating, increasing the losses of the combined inductor and heat sink structure.

To determine the losses in the inductor and the integrated heat sink structure, the combined structure is electromagnetically simulated in the finite element package ANSYS$^{TM}$. The electromagnetic analysis is done in two dimensions, making two cross-sections of the inductor and integrated heat sink structure necessary. These two cross-sections are illustrated in Figure 5.13, which shows a cross-section through the winding clamp on the left and through the winding window on the right of the figure. The figures include the electrical isolation between the different conductive materials.

To determine the losses in the combined structure, all the dimensions are required. In these simulations the outer dimensions of the heat collector (total heat collector width and height) are not important as long as these dimensions are larger than the sum of the core and core isolation dimensions by several times the skin depth of aluminium at the operating frequency. These

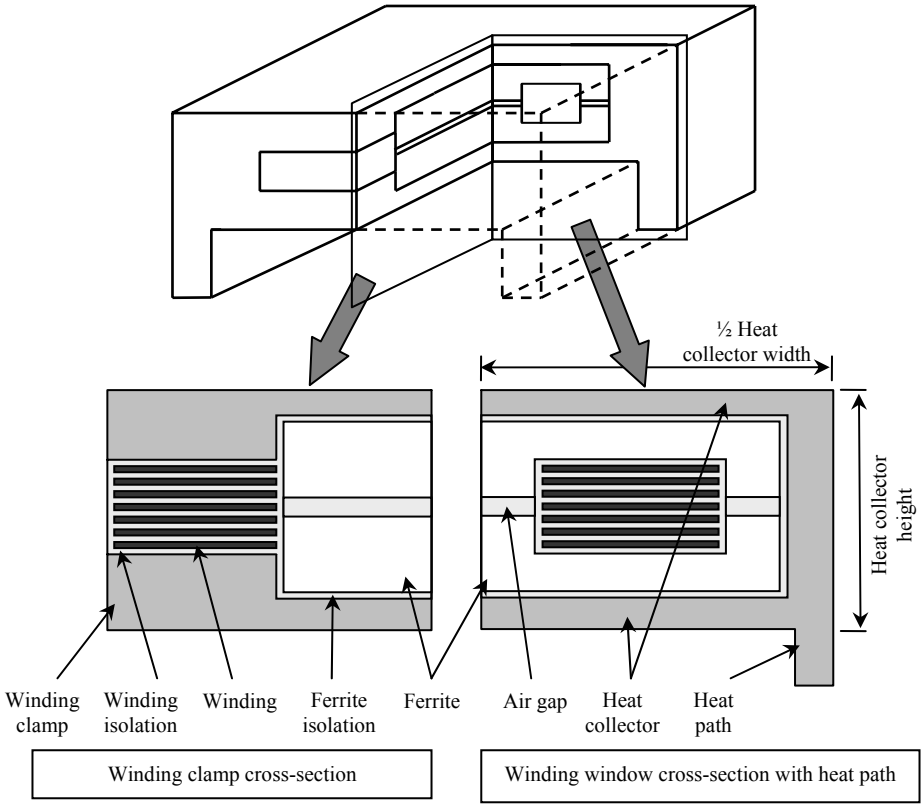


**Figure 5.13. The two inductor structure cross-sections used to calculate the conduction losses in the inductor windings and the integrated heat sink structure**

simulations determine the losses in the structure and do not consider the temperature distribution within the structure.

With all the dimensions of the core and winding known, the only additional dimension that must be fixed is the spacing between the inductor and the integrated heat sink. For this case study this dimension is fixed to 500µm. This dimension is not arbitrarily selected but is slightly less than the thickness of the compressible thermal interfacing material that is placed between the different materials to ensure good thermal coupling and electrical isolation while relieving thermal stresses. All the volume in the integrated heat sink and inductor structure that is not occupied by ferrite, copper or aluminium is filled with the thermally conductive interfacing material to maximise heat transfer.

The integrated heat sink and inductor structure are excited by triangular current waveforms as in Chapter 4. In the finite element program, the simulated structure is excited by sinusoidal waveforms. To determine the losses due to the triangular waveforms, the excitation waveforms must be reduced to their Fourier components and the losses determined for each of the Fourier components. The total losses for a given waveform and structure are then the sum of the losses determined for each of the Fourier components. The complete loss analysis of the inductor and integrated heat sink structure can be found in Appendix C.

The simulation results for the inductor and integrated heat sink structure operating over the defined voltage range with 500W delivered into the load are tabulated in Table 5.1. The table shows the simulated conduction losses in both the copper winding and the aluminium heat sink structure for both of the structure cross-sections. The DC conduction losses in the winding are also included, making it possible to determine the total conduction losses in the winding and integrated heat sink structure.

**Table 5.1. Summary of the conduction losses in the inductor winding and the integrated heat sink structure over the operating voltage range of 30V ≤ $V_{42}$ ≤ 50V and 11V ≤ $V_{14}$ ≤ 16V**

| Terminal voltages (V) | | Conduction losses in winding window (W) | | Conduction losses in the winding clamp (W) | | DC losses in winding (W) | Total conduction losses (W) | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{14}$ | $V_{42}$ | Cu | Al | Cu | Al | Cu | Cu | Al | Inductor |
| 11 | 30 | 0.62 | 0.28 | 0.31 | 0.23 | 4.23 | 5.16 | 0.51 | 5.67 |
| 14 | 30 | 0.5 | 0.22 | 0.25 | 0.18 | 2.61 | 3.36 | 0.4 | 3.76 |
| 16 | 30 | 0.43 | 0.19 | 0.21 | 0.15 | 2 | 2.64 | 0.34 | 2.98 |
| 11 | 36 | 0.84 | 0.37 | 0.42 | 0.31 | 4.23 | 5.49 | 0.68 | 6.17 |
| 14 | 36 | 0.89 | 0.4 | 0.45 | 0.33 | 2.61 | 3.95 | 0.73 | 4.68 |
| 16 | 36 | 0.78 | 0.35 | 0.39 | 0.29 | 2 | 3.17 | 0.64 | 3.81 |
| 11 | 42 | 0.94 | 0.42 | 0.47 | 0.35 | 4.23 | 5.64 | 0.77 | 6.41 |
| 14 | 42 | 1.21 | 0.54 | 0.6 | 0.45 | 2.61 | 4.42 | 0.99 | 5.41 |
| 16 | 42 | 1.22 | 0.55 | 0.61 | 0.45 | 2 | 3.83 | 1 | 4.83 |
| 11 | 46 | 1 | 0.45 | 0.5 | 0.37 | 4.23 | 5.73 | 0.82 | 6.55 |
| 14 | 46 | 1.36 | 0.61 | 0.68 | 0.5 | 2.61 | 4.65 | 1.11 | 5.76 |
| 16 | 46 | 1.48 | 0.61 | 0.74 | 0.5 | 2 | 4.22 | 1.11 | 5.33 |
| 11 | 50 | 1.07 | 0.48 | 0.53 | 0.39 | 4.23 | 5.83 | 0.87 | 6.7 |
| 14 | 50 | 1.46 | 0.66 | 0.73 | 0.54 | 2.61 | 4.8 | 1.2 | 6 |
| 16 | 50 | 1.68 | 0.75 | 0.84 | 0.62 | 2 | 4.52 | 1.37 | 5.89 |

The losses in the copper winding have a maximum value of 5.8W, while there is a maximum of 1.4W dissipated in the integrated heat sink structure. The losses in the winding and integrated heat sink structure for nominal operation are 4.42W and 0.99W respectively.

The core losses for the inductor structure are estimated from the AC component of the magnetic flux density and the material loss density graph in the data sheets of the ferrite material. The core losses are expected to be approximately 0.25W over the entire operating range. The core losses are a small percentage of the conduction losses of the integrated heat sink structure, thus less attention is given to determining the core losses.

### 5.3 The integrated heat sink

The integrated heat sink structure consisting of the heat collector and heat path is illustrated in Figure 5.14, which highlights the defining dimensions of the structure. The dimensions of the heat collector and heat path must be selected so that the temperature difference between the maximum temperature within the structure and the thermal interface is in the order of 10°C.

To determine the dimensions of the heat collector and heat path for the given specification, the dimensions of the heat collector and heat path are allowed to vary over a defined range and the temperature distribution within the structure is calculated using ANSYS™ and the losses calculated in the previous section. The maximum temperature is then determined from the simulation. With the maximum temperatures known, the appropriate dimensions can be selected.

The main dimensions defining the integrated heat sink structure and the range over which the heat collector's dimensions are varied are defined in Table 5.2. Some of the dimensions of the integrated heat sink, such as the heat path length and the heat collector length, are fixed and not varied. The heat path length is fixed because the heat path length determines the integrated heat sink structure's height above the thermal interface as defined in Figure 5.14 and is kept constant to ensure that the different maximum temperatures are comparable. The heat

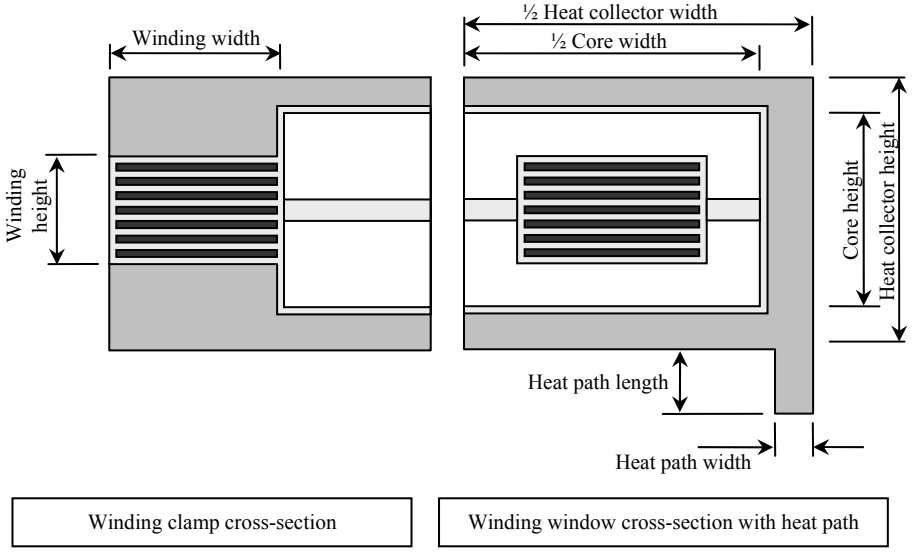


**Figure 5.14. The integrated heat sink dimensions relative to the core**

**Table 5.2. The dimensions of the inductor and integrated heat sink structure.**

| Dimension | Value (mm) | | Dimension | Value (mm) |
|---|---|---|---|---|
| Winding width | 5 | | Winding height | 6 |
| Core width | 21.8 | | Core height (each core) | 5.7 |
| Core length | 15.8 | | Core thickness | 2.5 |
| Heat collector width | 23 – 41 | | Heat collector height | 13 – 22 |
| Heat collector length | 26.8 | | Heat path width | 1 – 5 |
| Heat path length | 5.7 | | | |
| Winding to heat sink isolation thickness | 0.4 | | Core to heat sink isolation thickness | 0.5 |

collector's length is fixed and is given by the sum of the core length, twice the winding width and twice the isolation between the winding and the core (0.5mm).

## 5.4 Finite element thermal model

In order to determine the maximum temperature in the integrated heat sink structure, a three-dimensional model of the inductor and integrated heat sink structure is implemented in ANSYS$^{TM}$. The three-dimensional model is implemented with only one quarter of the total structure geometry due to the high level of symmetry in the structure. The model used in the simulations is shown in Figure 5.15.

The inductor winding in the model is implemented with an equivalent structure that requires a lower number of nodes in ANSYS$^{TM}$ to calculate the temperature. This is required due to the limited number of nodes available. To simplify the winding structure, the windings and the isolation between the windings can be replaced with a single material that has an anisotropic thermal conductivity based on the winding and electrically isolating material dimensions and thermal conductivities.

The thermal conductivity parallel to the inductor winding plane (the $x$ and $z$ directions in Figure 5.15) can be calculated to be [5-12]:

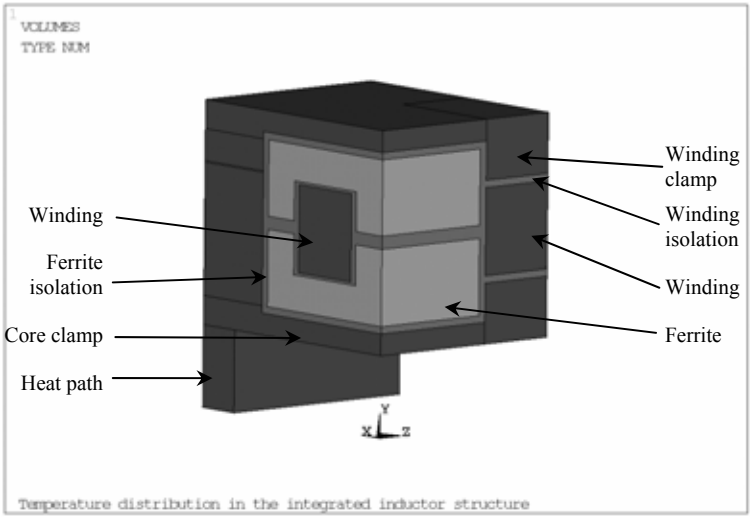


**Figure 5.15. The three-dimensional model used to determine the temperature of the integrated heat sink and inductor structure**

$$k_{parallel} = \frac{k_{winding} \cdot t_{winding} + k_{iso} \cdot t_{iso}}{t_{winding} + t_{iso}} \tag{5.11}$$

while the thermal conductivity perpendicular to the winding plane (the *y* direction in Figure 5.15) can be calculated to be:

$$k_{perpendicular} = \frac{t_{winding} + t_{iso}}{\frac{t_{winding}}{k_{winding}} + \frac{t_{iso}}{k_{iso}}} \tag{5.12}$$

where $t_{winding}$ is the thickness of the copper winding [m],
$t_{iso}$ is the thickness of the isolation material between the conductors [m],
$k_{winding}$ is the thermal conductivity of the copper winding [W/m·°C],
$k_{iso}$ is the thermal conductivity of the isolation material [W/m·°C],
$k_{parallel}$ is the equivalent thermal conductivity of the winding parallel to the winding plane [W/m·°C]
and $k_{perpendicuar}$ is the equivalent thermal conductivity of the winding perpendicular to the winding plane [W/m·°C].

The thermal properties of the different materials used to implement the inductor and integrated heat sink structure are tabulated in Table 5.3.

The temperature distribution in the inductor structure is simulated using the model in Figure 5.15 and the losses tabulated in Table 5.1 for the inductor operating in a synchronous rectifier with terminal voltages of $V_{14}$ = 14V and $V_{42}$ = 42V and delivering 500W to the load. For the purpose of the simulation the thermal interface temperature is 30.5°C, the heat collector height is 15.4mm, the heat collector width is 34mm and the heat path width is 3mm. The simulated result is plotted in Figure 5.16.

The simulation result shows that the maximum temperature in the integrated heat sink structure is in the centre of the winding in the winding clamp. For the case simulated, the maximum temperature in the inductor is 41.76°C, which is 11.26°C above the thermal interface temperature for an inductor that is dissipating a total of 5.66W in a volume of approximately 5.7cm$^3$.

The maximum temperature in the integrated heat sink structure can be calculated in a similar way for the different dimension configurations in Table 5.2. As the dimensions of the integrated heat sink structure change, the maximum temperature in the inductor winding structure will also change.

**Table 5.3. The thermal conductivities of the different materials used to implement the integrated heat sink structure**

| Material | k (W/m·°C) |
|---|---|
| Copper | 380 |
| Aluminium (Alloy 51ST 6082 ) | 120 |
| Ferrite | 3.5 |
| Isolation | 0.9 |
| Winding parallel to winding plane | 325 |
| Winding perpendicular to winding plane | 4 |

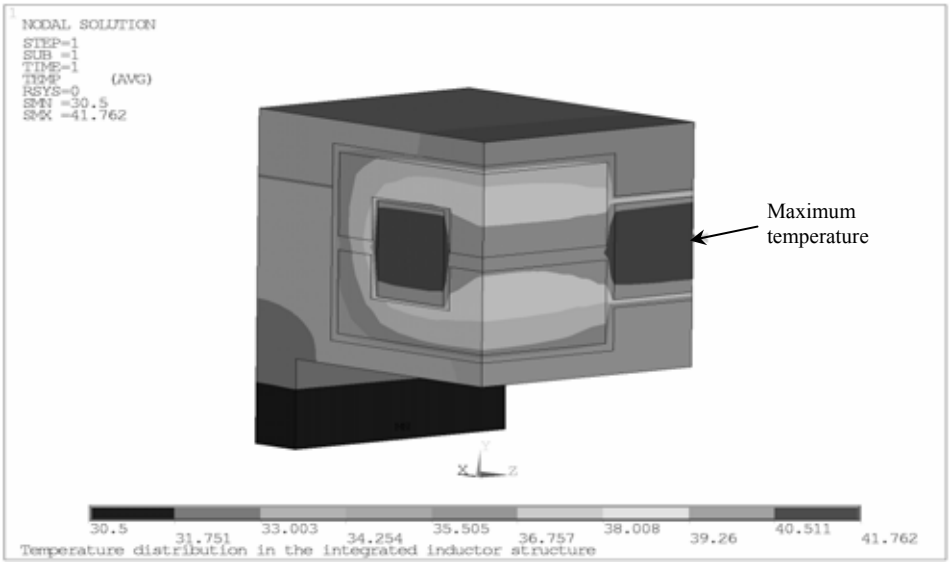


**Figure 5.16. The simulated temperature distribution in the integrated heat sink structure operating at nominal load with a thermal interface temperature of 30.5°C (heat collector width=34mm, heat collector height=15.4mm and heat path width=3mm )**

The simulated maximum temperature rise in the integrated heat sink and inductor structure for the inductor operating at nominal load (synchronous rectifier operating with $V_{14}$ = 14V, $V_{42}$ = 42V at 500W delivered power) and with a thermal interface temperature of 30.5°C is tabulated in Table 5.4 for some combinations of the heat collector geometry. The maximum temperature rise is the maximum temperature in the inductor winding less the thermal interface's temperature. The heat path width is fixed to 3mm for the simulations.

The simulation results, tabulated in Table 5.4, show that the maximum temperature rise in the integrated heat sink and inductor structure is 15.17°C and occurs for the smallest dimensions of the heat collector. On the opposite end of the scale, where the heat collector dimensions are the largest, the maximum temperature drop is reduced to 11.08°C showing only a 4.09°C improvement. Further, the simulations show that as both the heat collector's height and width are increased, the maximum temperature rise tends to decrease to a point after which the maximum temperature rise begins to increase again. This suggests a minimum in the temperature rise that is dependent on the integrated heat sink geometry. The increase is due to the increasing distance between the inductor and the heat path. Determining the optimum dimensions of the integrated heat sink structure are considered in the following chapter. where the volume of the inductor and the integrated heat sink are minimised.

**Table 5.4. The simulated maximum temperature rise in the integrated heat sink structure varying the heat collectors dimensions ($T_{base}$ = 30.5°C, Heat path width = 3mm)**

| | | Maximum temperature rise (°C) | | | | | |
|---|---|---|---|---|---|---|---|
| Heat collector height (mm) | 22 | 14.85 | 11.93 | 11.37 | 11.21 | 11.13 | 11.11 |
| | 19.5 | 14.67 | 11.8 | 11.28 | 11.16 | 11.07 | 11.08 |
| | 17 | 14.63 | 11.73 | 11.27 | 11.17 | 11.12 | 11.15 |
| | 15.4 | 14.65 | 11.75 | 11.33 | 11.26 | 11.26 | 11.3 |
| | 14 | 14.79 | 11.89 | 11.51 | 11.46 | 11.45 | 11.5 |
| | 13 | 15.17 | 12.25 | 11.9 | 11.86 | 11.86 | 11.96 |
| | | 23 | 27 | 31 | 34 | 38 | 41 |
| | | Heat collector width (mm) | | | | | |

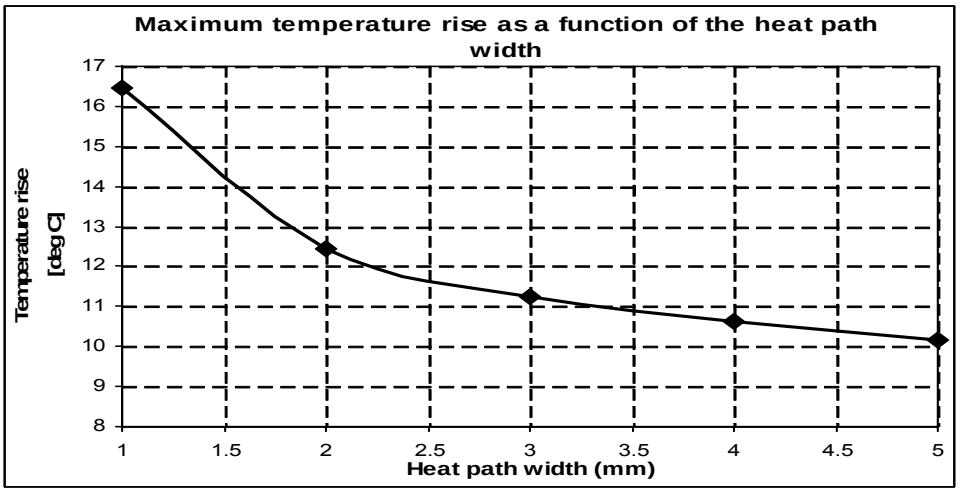


**Figure 5.17. The simulated maximum temperature rise in the integrated heat sink and inductor structure as a function of the heat path width**

If it is assumed that the heat collector's width and height are fixed to 34mm and 15.4mm respectively, then the maximum temperature rise in the integrated heat sink and inductor structure can be manipulated by changing the heat path width. Changing the heat path width for a fixed heat path length will change the maximum temperature rise in the inductor because all of the heat dissipated in the inductor must flow through the heat path to the thermal interface. The simulated temperature rise in the inductor structure for the given heat collector dimensions and the nominal operating point (same as in the previous simulations) is plotted in Figure 5.17.

For the given losses and integrated heat sink dimensions, the maximum temperature in the inductor winding varies from 16.5°C for a heat path width of 1mm to 10.2°C for a heat path width of 5mm. Implementing the heat path with a width smaller than 1mm in this application is difficult due to physical implementation issues and exceeding 5mm results in an unsatisfactory large area on the thermal interface.

If the heat path width is selected as 3mm, it is large enough for easy implementation and small enough not to require a large surface area on the thermal interface, and with the given dimensions of the heat collector, the maximum temperature rise in the inductor is approximately 11.26°C above that of the thermal interface. This is sufficiently close to the desired 10°C temperature rise.

The final dimensions and expected temperature rise of the case study integrated heat sink structure are summarised in Table 5.5.

**Table 5.5. The dimensions and expected temperature rise of the case study**

| Parameter | Value |
|---|---|
| Heat collector height | 15.4 mm |
| Heat collector width | 30mm |
| Heat path width | 3mm |
| | |
| Maximum temperature rise at nominal operation | 11.26°C |

## 5.5 Experimental verification

To verify the functioning of the integrated heat sink and inductor structure, the structure simulated is implemented and experimentally evaluated. The implemented integrated heat sink and inductor structure is photographed in Figure 5.18. The structure is shown mounted on a copper block and a pen is included for scale.

To experimentally evaluate the integrated heat sink and inductor structure, both the losses in the structure and the temperature of the structure must be measured. These can then be compared to the expected values.

### *5.5.1 The experimental setup*

It is desirable to perform the loss and temperature measurement under full electrical excitation to include the losses associated with the non-linear behaviour of the materials when under large signal excitation. To do this, an environment must be created where the integrated heat sink and inductor structure can be excited with normal operating waveforms and all the losses in the structure measured. There are several possible solutions to this problem; however, the calorimeter approach is preferred [5-13][5-14].

The calorimeter approach creates an environment where the component is excited under either full or partial load and all the heat escaping the component into the environment is measured. The problem with this approach is that relatively small amounts of heat are associated with large temperature variations in the component due to the restricted heat exchange.

To measure the losses in the inductor and integrated heat sink under consideration, a variation of the calorimeter is considered where relatively large amounts of heat exchange can take place. This is illustrated in Figure 5.19. The experimental structure consists of the inductor and integrated heat sink structure mounted on a copper heat spreader. This heat spreader is placed on top of a large heat sink with a thermopile placed between the heat spreader and the heat sink. There must be no direct contact between the heat spreader and the heat sink in order to ensure that all the conducted heat passes through the thermopile. The inductor and heat

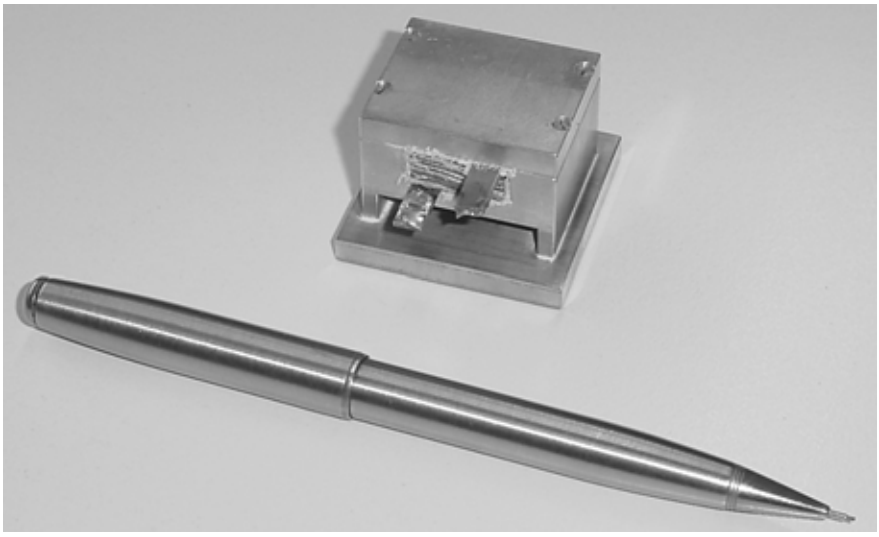

**Figure 5.18. The implemented integrated heat sink and inductor**

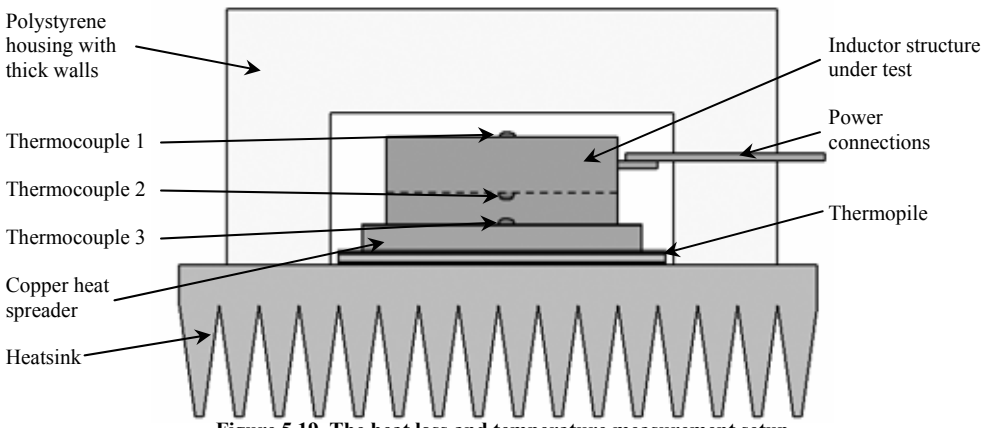


**Figure 5.19. The heat loss and temperature measurement setup**

spreader structure are then entombed in a material with a very low thermal conductivity, such as polystyrene, to ensure that all of the heat dissipated is transported to the heat sink through the thermopile.

The thermopile is a device that measures heat flux flowing through the device and consists of many thermocouples connected in series that are configured in space so that the voltage measured represents the temperature drop over a very thin layer of reference material. This is illustrated in Figure 5.20. The thermopile is manufactured to be very thin, typically 200μm, resulting in a thermal resistance of 0.0008 °C/(W/m$^2$).

The thermopile is used to measure the heat flux flowing between the heat spreader and the heat sink. However, the output of the thermopile is a voltage that is proportional to the heat flux. To determine the heat flowing through the thermopile, the device must be calibrated with a known heat source and the same heat spreader. Using the known heat source and heat spreader, the heat flux can be measured for a known heat loss. This is typically done over a large operating area and the average taken. The measured relationship between the heat loss and the voltage representing the heat flux for a copper heat spreader that measures 40mm by 40mm by 5mm in the configuration illustrated in Figure 5.19 is:

$$Q_{measured} = 0.3227 \cdot V_{thermopile} \tag{5.13}$$

where $Q_{measure}$ is the measured heat flowing through the thermopile [W]
and $V_{thermopile}$ is the output voltage of the thermopile [mV].

In Figure 5.19, three thermocouples have also been identified. These thermocouples are used to measure the surface temperatures on the heat spreader and the integrated heat sink structure. These measurements are compared to the theoretical results in the following section.

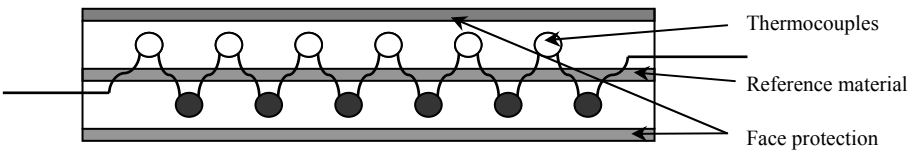


**Figure 5.20. The internal configuration of a thermopile**

### 5.5.2 The measured results

The integrated heat sink and inductor structure is excited with the single phase synchronous rectifier described in Chapter 4. The terminal voltages of the topology are varied over the same operating range as in the simulations while delivering 500W to the load. The three temperatures and the thermopile voltage are recorded once steady state is reached. The results are tabulated in Table 5.6. The measured heat spreader temperature, ($T_3$) which is the thermal interface temperature, is used as an input in the thermal simulation ($T_3$) to calculate the temperatures at the top ($T_1$) and bottom ($T_2$) of the heat collector.

The table shows that there is very good correlation between the measured temperatures and losses and the simulated temperature and losses. For the given conditions, the maximum temperature rise in the structure is approximately 14.6°C and occurs when the load current is the highest having the lowest output voltage and highest input voltage. The experimental structure has a maximum loss at this point of 7.64W for the inductor volume of 5.7cm$^3$. This gives the inductor a maximum loss density of 1.34W/cm$^3$.

The inductor structure has a total surface area in contact with the heat collector of approximately 18.8cm$^2$ and dissipates a maximum of 7.64W in the inductor volume. The maximum average heat flux density flowing across the inductor's surface area into the heat collector is then equal to the total losses in the inductor divided by the heat collecting area. This gives an average heat flux density flowing out of the inductor of 0.4W/cm$^2$. However, the heat path to the thermal interface has a cross-sectional area of only 0.8cm$^2$ and since there are two heat paths each carries half of the inductor's losses. The heat flux density in the heat path is then approximately 4.75W/cm$^2$ which is 11.7 times larger than that flowing out of the inductor. The heat flux density coming out of the inductor is compressed into an area that is approximately 11.7 times smaller than the surface area it escapes from while resulting in a maximum temperature rise of 14.6°C and a nominal temperature rise of 11.2°C.

**Table 5.6. The measured and simulated losses and temperatures in the integrated heat sink**

| Terminal voltages (V) | | Measure temperatures (°C) | | | Simulated temperatures (°C) | | | | $V_{thermopile}$ | Power loss $Q_{measured}$ | Power loss $Q_{simulated}$ | Power loss error |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{42}$ | $V_{14}$ | $T_1$ | $T_2$ | $T_3$ | $T_1$ | $T_2$ | $T_3$ | $T_{max}$ | (mV) | (W) | (W) | (%) |
| 30 | 11 | 37 | 35.9 | 31.6 | 37.4 | 35.8 | 31.6 | 44.5 | 19.98 | 6.45 | 5.91 | 9.10 |
| 30 | 14 | 32 | 31.2 | 28.4 | 32.2 | 31.2 | 28.4 | 36.9 | 13.7 | 4.42 | 4.01 | 10.25 |
| 30 | 16 | 30.4 | 29.7 | 27.3 | 30.4 | 29.6 | 27.3 | 34.1 | 11.04 | 3.56 | 3.23 | 10.30 |
| 36 | 11 | 36.6 | 35.7 | 31.2 | 37.5 | 35.7 | 31.2 | 44.9 | 19.95 | 6.44 | 6.41 | 0.43 |
| 36 | 14 | 33.1 | 32.3 | 28.9 | 33.4 | 32.2 | 28.9 | 39 | 15.59 | 5.03 | 4.93 | 2.05 |
| 36 | 16 | 31.4 | 30.8 | 27.8 | 31.5 | 30.5 | 27.8 | 35.9 | 13.81 | 4.46 | 4.07 | 9.50 |
| 42 | 11 | 38.6 | 37.6 | 32.5 | 38.8 | 37.2 | 32.5 | 46.6 | 21.38 | 6.90 | 6.66 | 3.59 |
| 42 | 14 | 35.3 | 34.5 | 30.5 | 35.5 | 34.3 | 30.5 | 41.7 | 16.94 | 5.47 | 5.67 | -3.59 |
| 42 | 16 | 34.4 | 33.7 | 29.9 | 34.5 | 33.3 | 29.9 | 40 | 15.52 | 5.01 | 5.08 | -1.41 |
| 46 | 11 | 39.3 | 38.3 | 33 | 39.4 | 38.7 | 33 | 47.4 | 22.41 | 7.23 | 6.8 | 6.35 |
| 46 | 14 | 35.8 | 34.9 | 30.6 | 35.9 | 34.6 | 30.6 | 42.5 | 18.35 | 5.92 | 6.01 | -1.47 |
| 46 | 16 | 34.8 | 34 | 29.9 | 34.8 | 33.6 | 29.9 | 40.7 | 16.84 | 5.43 | 5.57 | -2.44 |
| 50 | 11 | 40.3 | 39.3 | 33.7 | 40.3 | 38.7 | 33.7 | 48.3 | 23.68 | 7.64 | 6.96 | 9.79 |
| 50 | 14 | 35.9 | 35.1 | 30.6 | 36 | 34.9 | 30.6 | 42.8 | 18.67 | 6.02 | 6.25 | -3.60 |
| 50 | 16 | 35.2 | 34.4 | 30 | 35.3 | 34.1 | 30 | 41.6 | 18.08 | 5.83 | 6.13 | -4.82 |

## 6. Summary

In this chapter a thermal management technique for components, specifically passive components, for application in the high power density ISM operating in a high temperature environment has been considered.

To operate in a high temperature environment, all the heat dissipated in the components must be minimised and removed from the components within the maximum allowed temperature drop between the component and the environment as discussed in section 2. In the case of the ISM, all the heat dissipated in the components within the module must be transported to the thermal interface using only thermal conduction. It is assumed that thermal radiation and convection do not contribute to the module's thermal management because the location and orientation of the module within the automotive environment are not known.

To implement the thermal management within the ISM, an integrated heat sink is defined in section 3 and practical implementation issues are considered in section 4. The integrated heat sink is a concept whereby all heat dissipated in a component is collected with a heat collector. The resulting heat flux density is compressed and then transported to the thermal interface via a heat path. The integrated heat sink structure brings the following advantages into play:

- The surface area that the passive component dissipating the heat requires on the thermal interface is reduced from the component's footsprint to the cross-sectional area of the heat path. This increases the surface area available to high loss density components on the thermal interface without increasing the thermal interface area.
- The passive component in the integrated heat sink structure can be implemented in the 3$^{rd}$ dimension above the thermal interface plane. This makes volume available on the thermal interface for high loss density components while still implementing the module with a high power density and within the allowed $\Delta T$.
- The maximum temperature of the component in the integrated heat sink structure can be manipulated relatively easy by changing the integrated heat sink structure geometry and/or thermal properties.
- The integrated heat sink can remove the heat dissipated in the passive components very effectively, making it possible to implement the passive components in a much smaller volume for an acceptable maximum temperature.

To illustrate the integrated heat sink concept, a case study is considered in section 5. The case study considered is an inductor that is implemented in a 14V/42V 500W single phase synchronous rectifier. An inductor is selected for the case study because it is relatively easy to produce an inductor in almost any shape and dimension desired, allowing more freedom in the design of the component and integrated heat sink structure combination. The inductor has a maximum average current of 45A and a volume of 5.7cm$^3$. All the material, geometrical properties and issues are discussed.

Since the inductor is implemented in such close proximity to another electrically conductive material, there is electromagnetic interaction between the inductor and the integrated heat sink. This affects the losses in the combined structure. The losses in the case study structure are presented in section 4.2 for the different terminal voltages of the topology the inductor is implemented in. The loss analysis can be found in Appendix C. Using the calculated losses, the temperature distribution in the inductor structure is simulated using a three-dimensional model of the structure. The thermal results are presented in section 5.4 for a variety of geometry dimensions.

To verify the calculated losses and temperatures, the inductor and integrated heat sink structure is implemented and experimentally verified in section 5.5. The measured results correspond well with the calculated losses and temperatures. The results show that the inductor structure operating at full load has a nominal temperature rise of 11.2°C and a maximum temperature rise of 14.6°C above the thermal interface temperature. This means that if the thermal interface has a maximum temperature of approximately 110°C, the maximum temperature in the inductor structure will be approximately 125°C.

The integrated heat sink structure allows the passive components required to realise a power converter to be implemented within the ISM without requiring additional thermal interface area and within the volume that is already available in the power module. Passive components can be realised with small volumes and high loss densities due to the effectiveness of the integrated heat sink structure. In addition, the advantage of being capable of placing the passive components almost anywhere within the module while meeting the thermal requirements of the components can contribute to significantly increasing the ISM's power density.

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# Chapter 6

## VOLUMETRIC AND SPATIAL OPTIMISATION

## 1. Introduction

In Chapter 3, interdependencies between the electrical, thermal and spatial designs were identified. Of these, the electrical design together with its trade-offs were considered in Chapter 4 and, similarly, the thermal design was discussed in Chapter 5. In this chapter, the last design, the spatial design which considers the volumetric and spatial optimisation within the ISM, is discussed.

The volumetric design of the ISM couples the electrical and thermal design to the real world through the geometry, volume and materials used to implement the ISM. In this chapter, the volumetric optimisation is considered on two levels, namely the component level and the system or assembly level. To minimise the volume of the ISM, the volume of both the components and assembly of components constituting the ISM system must be miniaturised.

Volumetric optimisation on the component level is considered first in section 3 of this chapter. The optimisation is defined and illustrated on the basis of a planar inductor together with its integrated thermal management structure as defined in Chapter 5. A relationship between the component's excitation, volume and temperature-rise is derived that can be used to determine the components minimum volume for a given $\Delta T$.

Volumetric optimisation on the system level is considered in section 4. This section considers the volumetric and geometric optimisation of an assembly of components making up a system. A figure of merit is defined to help evaluate different assembly structures and geometrical performance. The assembly of a phase arm is considered.

## 2. Volumetric and spatial optimisation within the ISM

The spatial design of the ISM with reference to the design interdependence identified in Chapter 3 is repeated in Figure 6.1. The figure shows that the spatial design is connected to the electrical design through the energy that must be stored and processed by the topology and to the thermal design through the volume required to establish the necessary thermal resistance. In addition there is a trade-off between the volume required for the storage of energy and volume required to establish the required thermal resistance. Minimising the energy storage requirements of the topology was addressed in Chapter 4 and methods for establishing the necessary thermal resistance were addressed in Chapter 5. The spatial design is then concerned with implementing and minimising both the volume required for energy storage and the volume required for thermal management within the ISM for the given set of specifications.

The spatial design of the ISM couples the functional design of the module to the physical world, making the design highly dependent on the operating environment and spatial specifications. In the following sections, the spatial and volumetric design of the ISM is considered on both a component and system level. On a component level, the relationship

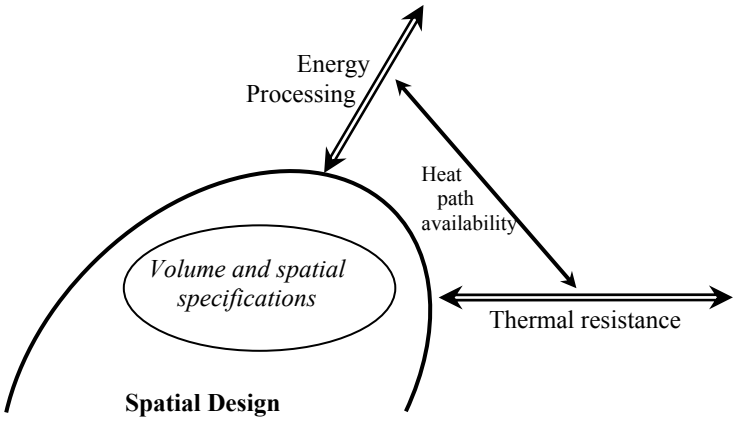



**Figure 6.1. The spatial design as defined in Chapter 3**

between the volume required for energy storage and volume required for thermal management is considered and manipulated to result in the smallest volume possible. On a system level, the volumetrically optimised components are placed together to form a functional circuit capable of meeting the required electrical specifications.

## 3. Volume reduction on a component level

Reducing the volume of the components within the ISM, specifically the passive components can lead to significant improvements in the ISM's power density. In this section of the chapter, the volume of a passive component and its thermal management structure as implemented in the Chapter 5 are considered together with a view to reducing the component's total volume. Only passive components are considered in this part of the chapter because the volume that they occupy in the module tends to be significantly more than that of the active components.

### 3.1 Volumetric optimisation of passive components within the ISM

The volume of any passive component within the ISM with an integrated heat sink structure can be represented as:

$$\psi_{component} = f(\psi_{energy\_storage}, \psi_{field\_establishment}, \psi_{thermal\_management}, \psi_{other}) \tag{6.1}$$

where $\psi_{component}$ is the total volume of the passive component [$m^3$],
$\psi_{energy\_storage}$ is the volume required to store the energy [$m^3$],
$\psi_{field\_establishment}$ is the volume required to establish and direct the magnetic or electric fields [$m^3$],
$\psi_{thermal\_management}$ is the volume of the integrated heat sink [$m^3$]
and $\psi_{other}$ is the volume required for electric isolation and thermal coupling [$m^3$].

Table 6.1 lists the volumetric breakdown for the most common passive components according to equation 6.1. It is assumed that all of the passive components in the ISM are implemented with an integrated heat sink in one form or another to remove the heat dissipated in the components and transport it to the thermal interface. The table also shows that some of the component parts contribute in more than one volume category. An example is the core of an inductor or transformer. The core contributes to both the volume required for energy storage and the volume required to establish and direct the magnetic fields.

**Table 6.1. The volumetric break down for common passive components implemented in the ISM with integrated heat sink**

| | $\psi_{energy\_storage}$ | $\psi_{field\_establishment}$ | $\psi_{thermal\_management}$ | $\psi_{other}$ |
|---|---|---|---|---|
| Inductor | Air-gap and core | Inductor winding and core | Integrated heat sink | Electrical isolation and thermal coupling |
| Transformer | Leakage field and core | Transformer windings and core | Integrated heat sink | Electrical isolation and thermal coupling |
| Capacitor | Dielectric | Capacitor plates | Integrated heat sink | Electrical isolation and thermal coupling |

In addition, the table also shows that only the integrated heat sink is considered for the thermal management volume of the component. It is true that ultimately all of the parts in a component contribute to the volume of the thermal management of the component but the integrated heat sink is the only part of the component that is purely dedicated to the thermal management of the component.

The volume required to store energy within the passive component, $\psi_{energy\_storage}$ is determined by the medium in which the energy is stored and by the energy storage requirements of the component [6-1]. For example, the energy in an inductor is stored primarily in an air-gap if one is present, with a very small percentage stored in the core, assuming a core material with a high permeability. However, if a core material with a low permeability is used, then the energy is stored primarily in the core material of the inductor. For a given construction, material technology and operating specifications, the volume required for energy storage is fixed and cannot be reduced.

The volume required to establish and direct the magnetic or electric fields associated with the stored energy, $\psi_{field\ establishment}$ is not necessarily directly related to the volume required to store the energy. This volume is required to create the magnetic or electric fields in the form of windings or plates respectively and in the case of the inductor or transformer, the core that directs the magnetic field. The volume of these component parts is limited only by the material properties and maximum operating temperature of the materials used. For example, the maximum magnetic flux density and operating frequency of an inductor core are limited by the core material's saturation flux density and loss density. The volume of the field establishment parts can be reduced within the limitations of the material's properties used to implement them.

The volume of the integrated heat sink structure, $\psi_{thermal\ management}$ is determined primarily by the amount of heat the structure must transport from the component to the thermal interface and the maximum allowed temperature drop between the component and thermal interface for a given material and geometry. The volume of the integrated heat sink structure and the volume of the field establishment parts can be traded off against each other for a given energy storage requirement since the first primarily represents the volume used to remove dissipated heat and the second represents the volume in which the heat is dissipated.

The final volume component, $\psi_{other}$ represents the volume required for the electrical isolation and the thermal coupling materials that are required in the practical implementation of any passive component together with the integrated heat sink. The volume required for these materials is determined by the construction of the component, and safety and reliability requirements. For example, an inductor implemented in the ISM requires a material between the inductor structure and the integrated heat sink structure that provides both electrical

isolation and thermal coupling. This material is vital in terms of heat transfer and for mechanical stress relief. The volume of material required is determined by the component's surface area in contact with the integrated heat sink. It is desirable to reduce the volume required by these materials within the reliability and safety margins since they do not contribute directly to the component's electromagnetic function.

In order to optimise the volume of a passive component, the total volume of the component must be minimised within the allowable operating temperature for the required energy storage. For a given construction technology, the volume of the medium in which the energy is stored cannot be significantly reduced without reducing the amount of energy being stored. This fixes $\psi_{energy\_storage}$. However, the volume required for establishing the required fields and thermal management can be manipulated to result in a component with the minimum volume for the given electrical and thermal specifications. This is illustrated in the following section.

## 3.2 Volumetric optimisation of a planar inductor with the integrated heat sink

To illustrate how the volume of a passive component together with the integrated heat sink can be minimised, the total volume of an inductor and integrated heat sink structure is minimised for a given energy storage requirement. The approach considered can be implemented on any passive component. The planar inductor is selected because the structure has already been introduced and considered in the previous chapter.

The combined inductor and integrated heat sink structure as implemented in the ISM is illustrated in Figure 6.2. This structure was introduced in Chapter 5 where it was experimentally evaluated. In this section, the combined volume of the inductor and integrated heat sink structure is minimised for a given energy storage requirement and maximum temperature-rise.

To reduce the volume of the inductor and integrated heat sink structure without reducing the amount of magnetic energy stored in the component, only the volume associated with the inductor winding structure can be manipulated. For the inductor structure this means that the volume of the winding structure will be reduced which requires an increase in the current density in the inductor windings. If the current density in the windings is increased for a fixed average current, then the volume of the core and windings can be reduced while maintaining the appropriate core cross-sectional area and energy storage volume [6-4].

### *3.2.1 Volume of the inductor as a function of the current density*

The minimum volume of the inductor and integrated heat sink structure can be determined in

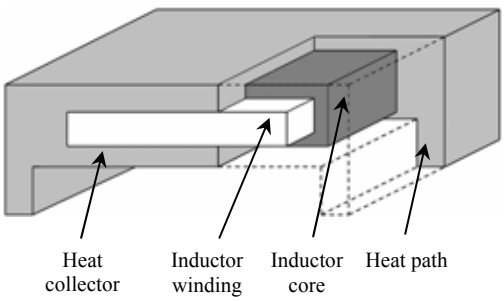



**Figure 6.2. The inductor and integrated heat sink structure to be volumetrically optimised**

terms of the component excitation parameters, such as maximum stored energy and maximum flux density, and geometrical parameters such as the cross-sectional area of the conductors and core all as a function of the current density.

Figure 6.3 shows a cross-section through the planar inductor structure, not including the integrated heat sink structure showing the two winding windows. In the figure the core cross-sectional area and the winding window area are identified with the shaded blocks. The variables are summarised in Table 6.2.

The inductor's volume (inductor core and winding) can be completely described with these variables.

In terms of the defined variables, the inductor core volume including the air-gap is:

$$\psi_{core} = \{(h_w + w_{cen}) \cdot (2w_{cen} + 2w_w) - 2A_w\} \cdot l_c \tag{6.2}$$

where $\psi_{core}$ is the volume of the inductor core [$m^3$].

The volume of the inductor winding can be determined by assuming the winding has the same cross-sectional area and shape outside the core as it does in the core, that the winding fills the winding window and that the winding closes the path outside the core with the minimum distance. Then the winding cross-sectional area and the core dimensions can be used to determine the winding's volume. The inductor winding volume is:

**Table 6.2. The variables defining the inductor structure**

| Variable | Description | | Variable | Description |
|---|---|---|---|---|
| $A_w$ | winding window area | | $A_c$ | core area |
| $w_{cen}$ | width of the centre member of the core | | $h_c$ | total height of the core |
| $l_c$ | length of the core | | $w_w$ | winding windows width |
| $h_w$ | winding windows height | | | |

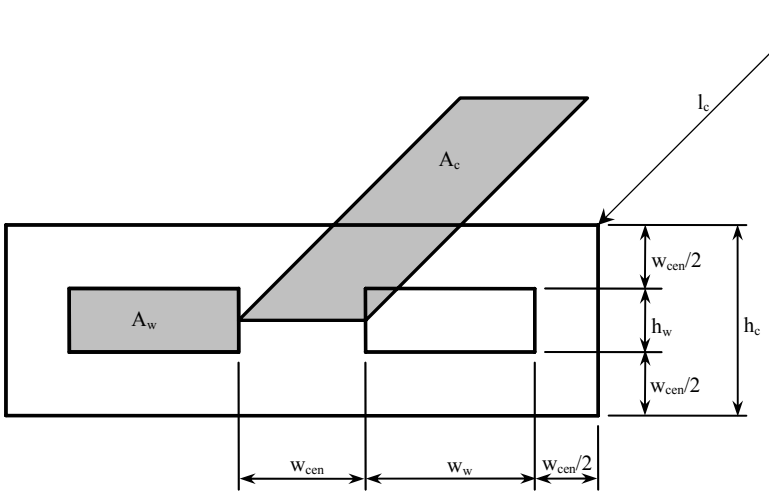



**Figure 6.3. Cross-section of a planar inductor structure**

$$\psi_{winding} = \left(2 \cdot A_w \cdot l_c\right) + 2\left(h_w \cdot w_w \cdot \left(2w_w + w_{cen}\right)\right) \tag{6.3}$$

where $\psi_{winding}$ is the volume of the inductor winding [$m^3$].

The volume of the inductor structure can then be determined by taking the sum of equations 6.2 and 6.3 and rearranging:

$$\psi_{inductor} = \left(2w_{cen} + 2w_w\right) \cdot \left(h_w + w_{cen}\right) \cdot l_c + 2 \cdot h_w \cdot w_w \cdot \left(w_{cen} + 2w_w\right) \tag{6.4}$$

To determine the inductor dimensions with respect to the inductor energy storage requirements, the energy that can be stored in the component must be related to the inductor dimensions and material properties. The energy stored in the component is given as [6-1][6-2]:

$$E_{inductor} = \tfrac{1}{2} \cdot L \cdot I^2 \tag{6.5}$$

where $E_{inductor}$ is the maximum energy to be stored in the inductor [J],
$L$ is the inductor's inductance [H]
and $I$ is the peak inductor current [A].

The energy stored in the inductor is assumed to be stored in an air-gap with the cross-sectional area of the core and a length of $l_g$ [6-1][6-2]:

$$E_{inductor} = \frac{1}{2} \frac{B^2 \cdot A_c \cdot l_g}{\mu_0} \tag{6.6}$$

where $B$ is the magnetic flux density in the core [T],
$l_g$ is the length of the air-gap [m]
and $\mu_0$ is the permittivity of air [H/m].

With the energy to be stored in the inductor known, the inductor area product can be used to couple the stored energy to the component dimensions [6-1][6-3]:

$$A_c \cdot A_w = \frac{2 \cdot E_{inductor}}{B \cdot J \cdot k_{fill}} \tag{6.7}$$

where $k_{fill}$ is the winding window fill factor and is defined as the ratio of copper in the winding window to the area of the winding window ($k_{fill} \leq 1$)
and $J$ is the current density in the copper conductors [$A/m^2$].

In order to determine the inductor volume, one of two possibilities exists. The first is to fix one of the main dimensions, the winding window width for example. Alternatively, two aspect ratios can be defined. The two aspects ratios are defined as:

$$k_w = \frac{h_w}{w_w} \tag{6.8}$$

and

$$k_c = \frac{w_{cen}}{l_c} \tag{6.9}$$

where $k_w$ is the winding window aspect ratio
and $k_c$ is the core aspect ratio.

Both aspect ratios are dimensionless.

Consider now the winding window. The relationship between the number of turns, the current and the current density is:

$$N_{turns} \cdot I = J \cdot k_{fill} \cdot A_w \tag{6.10}$$

but the winding window area is:

$$A_w = h_w \cdot w_w \tag{6.11}$$

Substituting equation 6.8 into equation 6.11 and the combined substitution into equation 6.10, the width of the winding window can be calculated:

$$w_w = \sqrt{\frac{N_{turns} \cdot I}{J \cdot k_{fill} \cdot k_w}} \tag{6.12}$$

With $w_w$ known, $h_w$ can be determined from equation 6.8. The area of the winding window, $A_w$ is then also known. Once the winding window area is known, the core cross-sectional area can be determined from equation 6.7 as:

$$A_c = \frac{2 \cdot E_{inductor}}{A_w \cdot B \cdot J \cdot k_{fill}} \tag{6.13}$$

Together with the aspect ratio in equation 6.9 and

$$A_c = w_{cen} \cdot l_c \tag{6.14}$$

the dimensions of the core cross-sectional area can be determined as:

$$l_c = \sqrt{\frac{A_c}{k_c}} \tag{6.15}$$

and

$$w_{cen} = k_c \cdot l_c \tag{6.16}$$

Alternatively, if the winding window width is fixed, then the winding window aspect ratio is not required and the winding height $h_w$ can be calculated directly as:

$$h_w = \frac{N_{turns} \cdot I}{J \cdot k_{fill} \cdot w_w} \tag{6.17}$$

The winding window width can be fixed in the case where the possibility of creating a completely custom core does not exist and an existing E-core is used but with the length of the three legs ground down to the required dimensions. In this case, $w_w$ is fixed but $h_w$ is variable and thus the area $A_w$ and the aspect ratio $k_w$ are also variable.

With all the dimensional parameters known in terms of the stored energy, which is a function of the current density, the volumetric behaviour as a function of the current density can be determined.

Assuming that the values for the materials and excitation parameters are as in Table 6.3 (based on the inductor structure presented in Chapter 5), the volume of the inductor can be calculated ignoring the volume of the integrated heat sink structure. This is plotted in Figure 6.4. The figure shows that the volume of the inductor can be significantly reduced by simply increasing the current density in the inductor winding. The figure also shows that increasing the current density indefinitely does not result in an infinitely small inductor. Furthermore, as the current density increases and the volume of the core and winding decrease, the volume required for energy storage, i.e. the air-gap, will become larger relative to the decreasing volume of the inductor core. A point will be reached where there is insufficient volume in the inductor core to implement the air-gap, for example when the length of the air-gap becomes longer than the height of the winding window (assuming this is where the air-gap is implemented). This will limit the maximum current density and volume reduction achievable with a specific

**Table 6.3. Parameters used to determine the inductor's volume**

| Parameter | Value | | Parameter | Value |
|---|---|---|---|---|
| L | 3.8μH | | I | 44.5A |
| $N_{turns}$ | 7 | | $k_{fill}$ | 0.695 |
| $k_c$ | 0.316 | | $k_w$ | 1.085 |
| $\mu_r$ | 1500 | | B | 300mT |

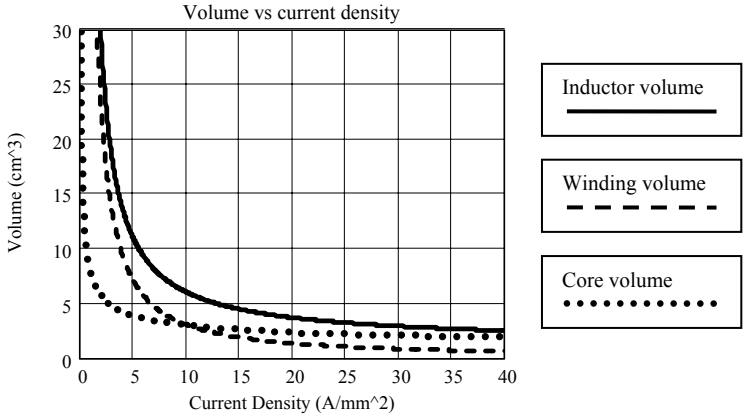



**Figure 6.4. The inductor volume as a function of the current density for the parameters in Table 6.3**

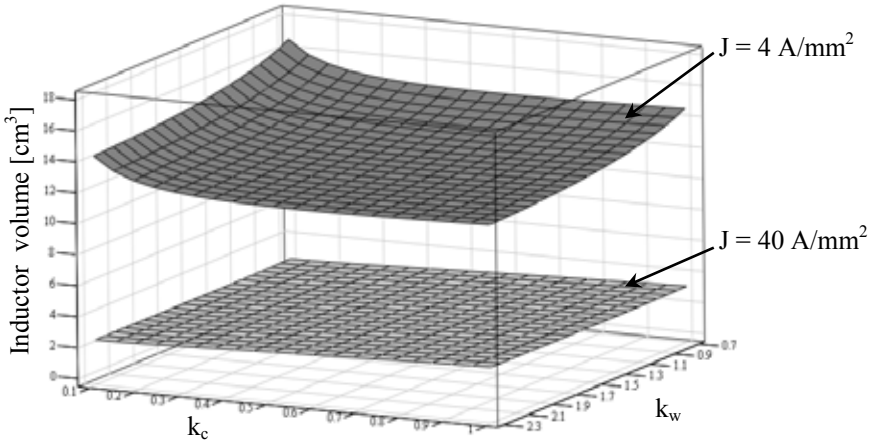



**Figure 6.5. The inductor (winding and core) volume as a function of the two aspect ratios for two current densities**

construction and air-gap implementation method. For Figure 6.4 the length of the split air-gap is limited to half of the winding window height.

The volume of the inductor structure can be defined as a function of the core area and winding window area aspect ratios. The volume of the complete inductor (winding and core) is plotted in Figure 6.5 as a function of both aspect ratios and for two inductor winding current densities, namely 4A/mm$^2$ and 40A/mm$^2$.

The figure shows that the two aspect ratios do not have a significant effect on the volume of the inductor. The volume of the inductor structure varies only marginally over the aspect ratio range ($0.1 \leq k_c \leq 1$, $0.7 \leq k_w \leq 2.3$) compared to the change in the component's volume when the current density is increased.

However, when the current density in the inductor winding is increased, it can be expected that the losses in the winding will increase accordingly, limiting the volume reduction achievable.

### *3.2.2 Increased losses in the inductor structure*

To determine the losses in the inductor and integrated heat sink structure, a finite element package can be employed (as was done in Chapter 5). Assuming that the inductor and integrated heat sink structure have a cross-section as given in Figure 5.13 in Chapter 5, and for the geometric and excitation parameters as given in Table 6.3, the losses in the structure are calculated and plotted in Figure 6.6 as a function of the current density in the winding.

The figure shows that the total losses in the inductor and integrated heat sink structure increase just less than threefold as the current density is increased from 4A/mm$^2$ to 40A/mm$^2$. The losses in the inductor winding increase almost linearly since the DC component of the winding losses is dominant and the DC conduction losses increase as the cross-sectional area of the winding decreases. The losses in the inductor core decrease with the decreasing core volume because the core excitation does not change as a function of the current density; thus the core loss density does not change. The losses in the integrated heat sink structure due to the induced eddy currents increase slightly as the current density increases. The increase in the induced losses is not significant because even through the current density increases, the surface area of the winding in close contact with the integrated heat sink decreases.

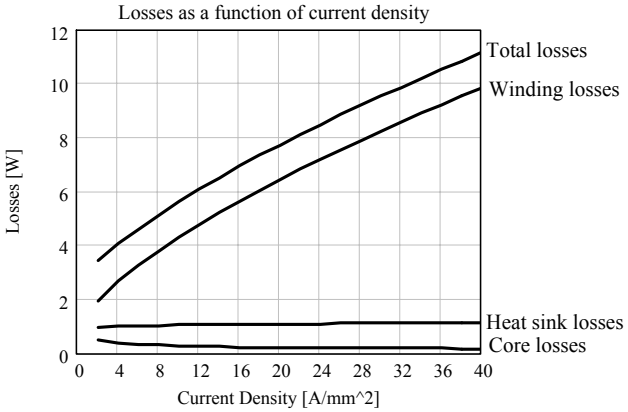



**Figure 6.6. The losses in the inductor structure as a function of the current density**

The losses in the inductor structure and the volume of the inductor without the integrated heat sink, both normalised to the losses and volume of an inductor structure with a current density of 4A/mm$^2$ are plotted in Figure 6.7. The figure shows that the losses increase almost linearly while the inductor volume decreases inversely proportionally to the current density. This implies that a small increase in the current density in the inductor winding, from 4A/mm$^2$ to 8A/mm$^2$ for example, reduces the inductor's volume by a half relative to the reference structure, while the losses increase by only about 25%. However, if the increase in the current density is larger, say from 4A/mm$^2$ to 16A/mm$^2$, the volume of the inductor will be reduced to approximately 30% of the reference structure while the losses increase by approximately 70%. The significantly increased losses will result in an increase in the integrated heat sink structure's volume for a desired maximum temperature, offsetting the reduction of the inductor's volume.

### *3.2.3 Integrated heat sink volume*

Assuming that the integrated heat sink structure and inductor are implemented as illustrated in Figure 6.8, the maximum temperature in the structure can be determined as a function of both the current density in the inductor winding and the geometry of the integrated heat sink. Assuming the inductor geometry remains as has been defined in Table 6.3 ($k_{fill}$ = 0.695, $k_w$=1.085, $k_c$=0.316 ), the volume of the integrated heat sink geometry can be defined in terms

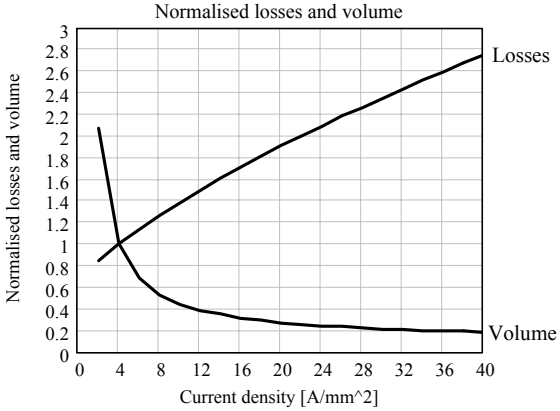



**Figure 6.7. The total inductor losses and inductor volume (without the integrated heat sink) normalised to that of an inductor structure with a current density of 4A/mm$^2$**

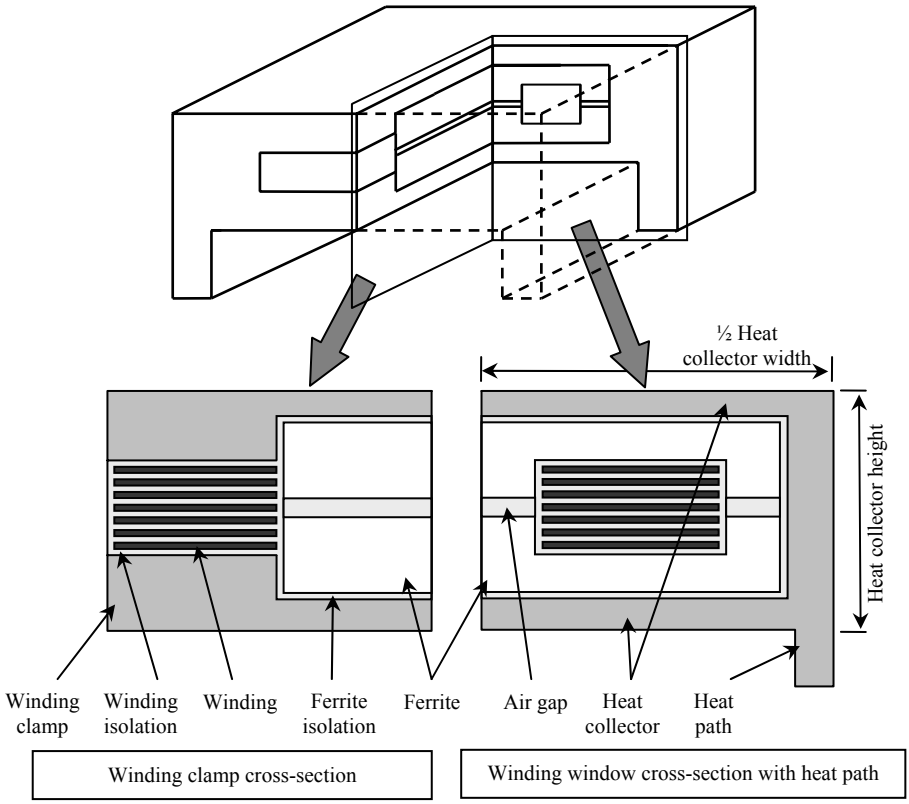



**Figure 6.8. The two inductor structure cross-sections used to calculate the conduction losses in the inductor windings and the integrated heat sink structure**

of the inductor dimensions by defining:

$$VRC = \frac{\psi_{heat\_collector}}{\psi_{inductor}} \tag{6.18}$$

where $\psi_{heat\_collector}$ is the volume of the heat collector structure excluding the heat paths [$m^3$],
$\psi_{inductor}$ is the volume of the complete inductor structure (core and winding) [$m^3$]
and *VRC* is a constant and is referred to as the *Volumetric Ratio Constant*.

It is assumed that the dimensions of the heat collector increase equally in all directions except the length of the structure as the VRC constant increases for a fixed inductor volume. The length of the integrated heat sink structure is fixed by the length of the inductor core and the width of the winding structure. The volume of the heat collector does not include the volume of the heat paths, which are fixed by the heat path's length and cross-sectional area. The increasing VRC is illustrated in Figure 6.9 for the inductor structure illustrated in Figure 6.8 with four different values of the VRC. The VRC has a minimum value which cannot be exceeded while being a realisable structure. This is also illustrated in Figure 6.9 where the integrated heat sink implements only the winding clamp and not a heat collector around the core. The minimum VRC is:

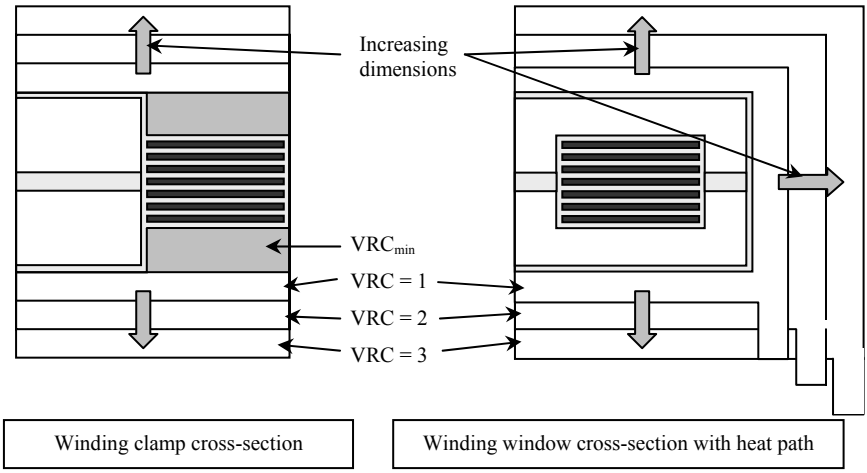



**Figure 6.9. The inductor structure with an increasing VRC**

$$VRC_{\min} = \frac{2w_w\left[\left(h_w + w_{cen}\right)\cdot\left(2w_w + 2w_{cen}\right) - h_w\left(w_{cen} + 2w_w\right)\right]}{\left(2w_{cen} + 2w_w\right)\cdot\left(h_w + w_{cen}\right)\cdot l_c + 2\cdot h_w \cdot w_w \cdot \left(w_{cen} + 2w_w\right)} \tag{6.19}$$

For the structure currently being considered, the absolute minimum VRC is 0.32, which represents a structure that is on the border of being physically realisable. A structure with a VRC equal to the $VRC_{min}$ requires a heat collector thickness of 0mm (see Figure 6.9). For practical purposes, a VRC value slightly larger than the $VRC_{min}$ is used as the smallest possible VRC for a given structure.

Assume that the heat path material and geometry are the same as the structure investigated in Chapter 5 (heat path length is 5.7mm, the heat path width is 3mm and the heat path depth is the same as the heat collector's depth as determined by the core and winding). The volume of the inductor structure and the integrated heat sink (heat collector and heat paths) is calculated for a range of current densities and VRC values. The result is plotted in Figure 6.10 for VRC = 0.5 and VRC = 2.2.

The maximum temperature-rise in the inductor and integrated heat sink structure is calculated

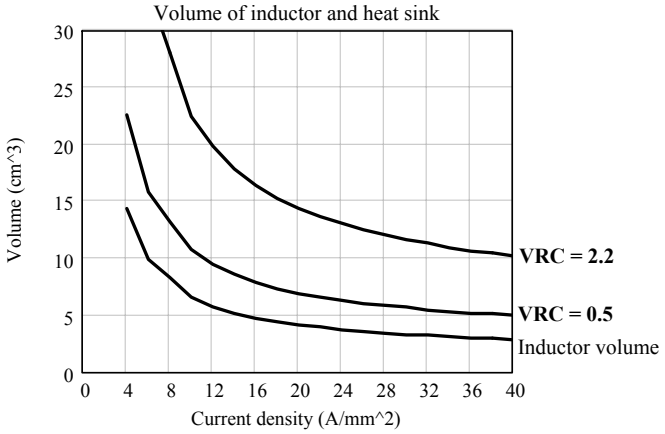



**Figure 6.10. Volume of the inductor and integrated heat sink as a function of the current density**

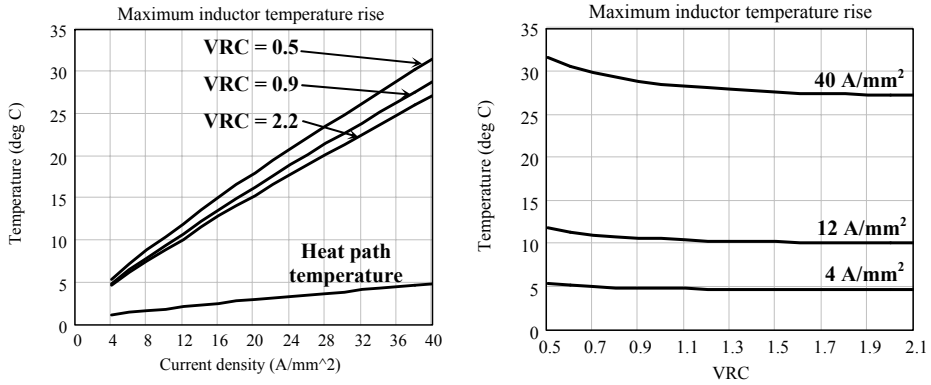



**Figure 6.11.The maximum temperature-rise in the combined inductor and integrated heat sink as a function of the current density and the VRC**

by the FEM package for the losses in Figure 6.6 as a function of the current density and over a range of VRC constants for the geometry in Figure 6.8. The results are plotted in Figure 6.11. The figure also shows the temperature drop over the heat path connecting the heat collector to the thermal interface. The results show that the maximum temperature-rise in the component is a strong function of the current density, varying near linearly with the current density while being a weak function of the heat collector volume. Moreover, the temperature drop over the heat path is significantly smaller than that between the heat path and the maximum temperature in the inductor (over the heat collector). These graphs can be used to trade off the maximum current density in the component and the volume of the inductor and integrated heat sink for a given maximum temperature-rise.

### *3.2.4 Optimum inductor and integrated heat sink volume*

The optimum volume of the inductor and integrated heat sink is the minimum combined volume of both the inductor and integrated heat sink for a given maximum allowed temperature drop and energy storage requirement. For the given geometrical structure, materials and excitation, the relationship between the maximum temperature-rise and total volume is plotted in Figure 6.12 as a function of the VRC. The direction of increasing current density is also identified.

The trade-off between volume and temperature-rise is made through the current density and thus losses in the inductor. For example, if the total volume of the inductor and integrated heat

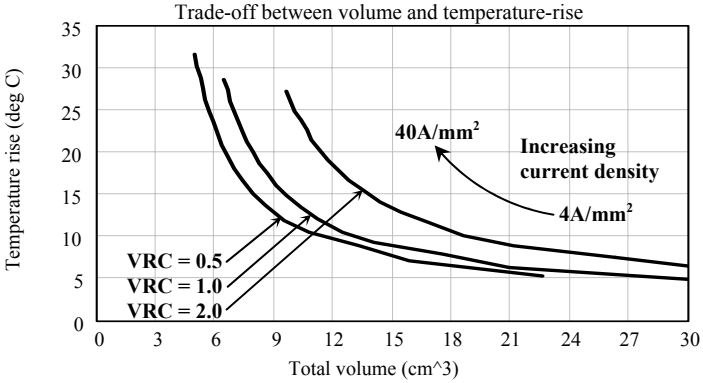



**Figure 6.12. The trade-off between the total inductor volume (inductor and integrated heat sink) and maximum temperature-rise for a constant $k_c$ and $k_w$ (For the given structure $VRC_{min}$ = 0.32)**

sink is limited to 15cm$^3$ (including heat paths), then for a VRC of 0.5, the maximum temperature-rise is approximately 7.5°C, while for a VRC of 2.0, the maximum temperature-rise is approximately 13°C. Since both components have the same total volume but different VRCs, the current density in the component with VRC = 2 must be larger (15A/mm$^2$ compared to 6A/mm$^2$) to store the same energy in the volume available for the inductor. The larger current density results in a much higher component loss (9.5W compared to 6W), which inadvertently results in a higher temperature-rise given the fixed total volume.

The volumetrically optimum inductor and integrated heat sink structure is a balance between the component's volume, the temperature-rise within the component and the losses in the component. The volume and temperature-rise within the component can be traded off by manipulating both the percentage of volume allocated to the inductor and integrated heat sink and the current density in the inductor winding. Figure 6.12 shows that for a fixed total volume, the component with the largest percentage heat sink volume does not necessary have the lowest temperature-rise but rather the component with a lower percentage heat sink volume and thus lower current density.

### 3.3 Practically implemented high current density inductor structures

To verify the relationship between the total inductor and integrated heat sink volume and the maximum temperature-rise, two experimental inductors based on the structure considered thus far were realised and experimentally evaluated. The two structures are illustrated in Figure 6.13 and are labelled as structure A and structure B. The parameters describing the two structures are tabulated in Table 6.4. Structure A is designed for a current density of 15A/mm$^3$ with a VRC of 0.86 while structure B is designed for 40A/mm$^3$ with a VRC of 1.24. Both structures have the same heat path geometries. The integrated heat sink structures are implemented with aluminium.

The two structures are realised using the same materials and specifications as the experimental inductor structure in Chapter 5. In addition, both inductors use the same inductor core but with

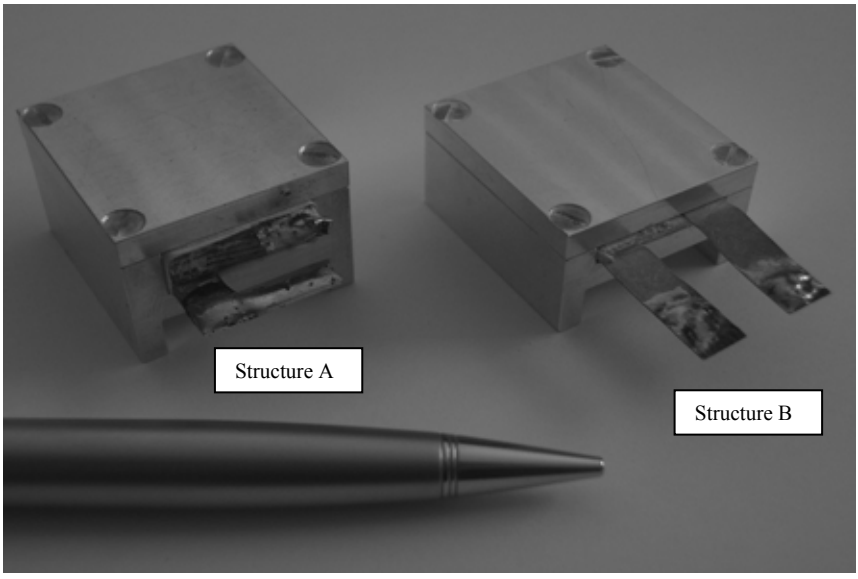



**Figure 6.13. Two experimental inductor and integrated heat sink structures (Left: J=15A/mm$^2$, VRC=0.86. Right: J=40A/mm$^2$, VRC=1.24)**

**Table 6.4. Geometrical parameters of the 2 experimental inductor and integrated heat sink structures**

| Structure A | | | Structure B | |
|---|---|---|---|---|
| Parameter | Value | | Parameter | Value |
| Current density: J | 15A/mm$^2$ | | Current density: J | 40A/mm$^2$ |
| VRC | 0.86 | | VRC | 1.24 |
| $I_{average}$ | 43.2A | | $I_{average}$ | 43.2A |
| L | 3.8µH | | L | 3.8µH |
| $k_c$ | 0.3164 | | $k_c$ | 0.3164 |
| $k_w$ | 1.084 | | $k_w$ | 0.4237 |
| $k_f$ | 0.51 | | $k_f$ | 0.51 |
| $h_w$ | 6.4mm | | $h_w$ | 2.5mm |
| $w_w$ | 5.9mm | | $w_w$ | 5.9mm |
| $w_{cen}$ | 5mm | | $w_{cen}$ | 5mm |
| $l_c$ | 15.8mm | | $l_c$ | 15.8mm |
| Heat collector height | 14.2mm | | Heat collector height | 10.35mm |
| Heat collector width | 25.4mm | | Heat collector width | 24.6mm |
| Heat collector length | 26.8mm | | Heat collector length | 27.1mm |
| Heat path length | 5.7mm | | Heat path length | 5.7mm |
| Heat path width | 3mm | | Heat path width | 3mm |
| | | | | |
| Heat path volume | 916.5mm$^3$ | | Heat path volume | 926.8mm$^3$ |
| Volume inductor | 5195.3mm$^3$ | | Volume inductor | 3078.9mm$^3$ |
| Volume heat collector | 4470.8mm$^3$ | | Volume heat collector | 3821.0mm$^3$ |
| Total volume | 10582.6mm$^3$ | | Total volume | 7826.7mm$^3$ |

different winding window heights. Consequently both structures have the same winding window width, core aspect ratios and core length.

The two inductor structures are excited with the 42V/14V DC/DC converter operating with the same specifications used to excite the inductor in Chapter 5. The losses and temperature-rise are also measured in the same way as for the inductor in Chapter 5. The experimental maximum temperature-rise for both structures is plotted on the graph in Figure 6.14 showing the maximum temperature-rise in the inductor versus the volume of the complete inductor and integrated heat sink structure for a VRC of 0.86 and 1.24.

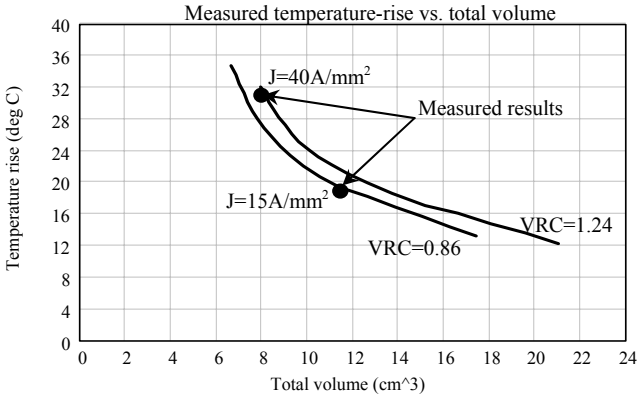



**Figure 6.14. The calculated and measured temperature-rise in the experimental inductor and integrated heat sink structures**

The measured results correspond well to the expected temperature rise for the given volumes. Structure B has a total volume that is only 70% of that of structure A. However, the volume reduction comes with significantly high losses. The inductor structure A has a total loss of approximately 8.1W, while structure B has approximately 18W for the same operating point. These two structures illustrate well the trade-off between the total component (inductor and integrated heat sink) volume and the losses in the component.

## 4. Volume reduction on a system level

Reducing the volume of a single passive component within the ISM can contribute towards but does not ensure an improvement in the power density of the ISM. This is because the ISM is a system of components and the volume of all the components within the ISM must be reduced simultaneously for the given specification and environment if the power density is to be increased. In this section of the chapter, attention is given to reducing the volume of the ISM on a system level considering two approaches, namely:

i. multifunctional parts and
ii. geometric optimisation.

The section on multifunctional parts considers how a single part can be used to implement several functions and the second section, on geometric optimisation, considers how to optimise the geometric construction to minimise the volume required to implement a given function.

### 4.1 Multifunctional parts

The ISM requires many different components and parts to realise a working structure that meets the given specifications in the given environment. All of these parts, be they electrical components, conductors or heat sinks, require volume within the ISM. In the best case scenario, assuming that there is absolutely no unused volume within the ISM, the absolute minimum volume that the ISM can have is the sum of the volumes of all the different components and parts. If the number of parts can be reduced, without significantly increasing the volume of the remaining parts, the volume of the ISM can be reduced while still meeting the specifications.

Since each part in the ISM is required to perform a certain function, no arbitrary part can be removed from the ISM without affecting the ISM's functionality. Thus the only way to reduce the number of parts required to implement the ISM is to have new parts that perform multiple functions [6-5][6-6][6-7]. These new parts reduce the number of parts required to implement the ISM while retaining the ISM's functionality and if selected and implemented appropriately, can have a smaller volume.

The most common example of implementing multiple functions with a single part is that of electromagnetic integration [6-6][6-8][6-9]. Electromagnetic integration combines the electromagnetic functionality of several discrete passive components into a single component that has the same electromagnetic functionality as a specific combination of the discrete components (over most of the operating frequency range). The electromagnetically integrated component can then replace the network of discrete components.

In the ISM, electromagnetic integration is not implemented but there are other opportunities within the module where a single part with multiple functions can be exploited to help reduce the module's volume. The integrated heat sink structure provides these opportunities. In the following section, the multifunctionality of the integrated heat sink will be considered with the

intention of reducing the ISM volume and thus increasing the power density.

### *4.1.1 Multiple heat collectors on a single heat path*

The first possible means of combining multiple parts with a single part is to combine the heat paths of several heat collectors into a single heat path connecting all the heat collectors to the thermal interface. This is illustrated conceptually in Figure 6.15, which shows four heat collectors, all with passive components dissipating heat, connected to the thermal interface through a single heat path.

The combined heat path can reduce the volume of the ISM by:

i. Significantly reducing the surface area on the thermal interface required for transferring the dissipated heat to the environment. However, this is also affected by the allowed temperature drop across the heat path.
ii. By combining the heat paths into a single structure, the layout of the high loss density components on the thermal interface can be simplified and possibly implemented with a lower profile because their design does not need to contend with making several areas available to implement heat paths on the thermal interface.
iii. Depending on the allowed temperature drop between the components dissipating the heat and the thermal interface, the single combined heat path will require less volume than all of the individual heat paths collectively.

The volume-saving attainable by combining the different heat paths into a single structure is highly dependent on the allowed temperature drop over both the heat path and the heat collector. For example, consider Figure 6.15, which shows the four heat collectors connected by a single heat path to the thermal interface. Below the thermal management structure is a figure of a possible temperature distribution between the various heat collectors, heat path and the thermal interface, given certain assumptions. The figure identifies two temperature drops, the first is the temperature drop over the heat collector, between the heat source and the heat paths, and the second temperature drop is over the heat path itself. The maximum temperature of the heat source is a combination of these two temperature drops.

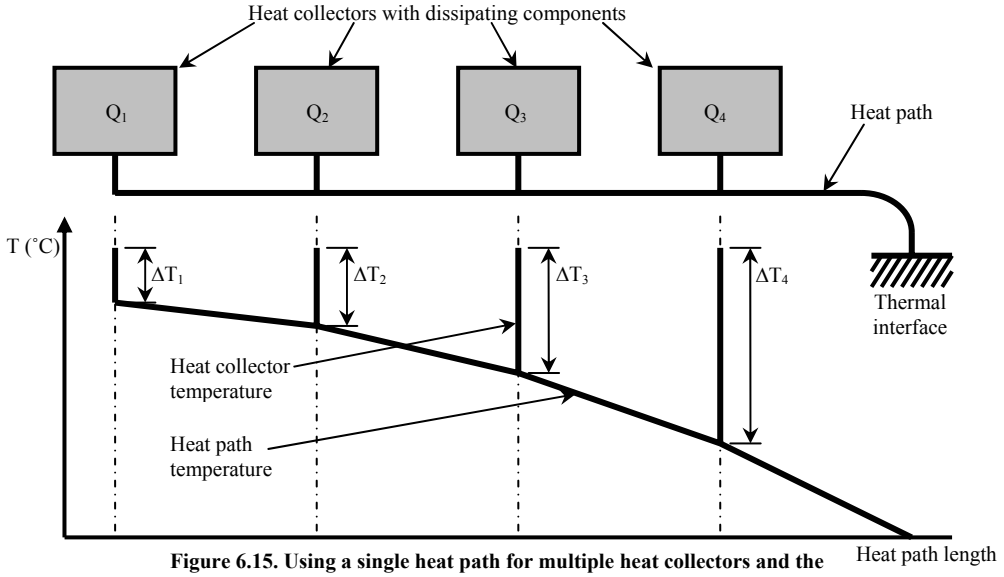



**Figure 6.15. Using a single heat path for multiple heat collectors and the temperature drop along the heat path**

If it can be assumed that the geometry or material properties of the heat path do not change with length, that the four heat sources dissipate similar amounts of heat and are evenly spaced along the heat path, then the temperature drop over the heat path will have the temperature profile as illustrated in the figure. With heat flowing in the heat path from left to right, the temperature drop over the heat path between heat sources will increase with each additional heat source. This means that the allowable temperature drop over the heat collector will also increase from left to right. Assuming similar components are implemented in the heat collectors, the relative volume of the heat collector can also decrease as the allowable temperature drop increases. This can help to further reduce the volume of the integrated heat sink structure.

A consequence of combining all the heat paths into a single heat path structure is that the design of the various components and the heat collectors along the heat path become even more dependent on each other. For example, the allowable temperature drop over the heat collector depends on the heat source's maximum temperature and the temperature of the heat path at the point of coupling. The temperature of the heat path at the point of coupling depends on the other heat sources that are coupled to the heat path between the heat collector of interest and the thermal interface.

### *4.1.2 Mechanical integrity*

The heat paths and heat collectors can be implemented with a variety of materials depending on their desired properties. However, if the material selected to implement the heat collectors and heat paths is solid and rigid, such as aluminium, then the heat paths and heat collectors can also be used to provide the components with a degree of mechanical integrity. In this context, mechanical integrity can be considered as the ability to keep the component intact so that it can perform its function while maintaining the component's spatial orientation. In other words, the heat paths and heat collectors can be used to replace the mechanical support the components would otherwise require to function while providing the required heat removal function.

In more conventional construction methodologies, circuit carriers such as PCB are normally used to provide not only electrical interconnection between components but also mechanical support for the components. In the ISM the circuit carrier is typically implemented with technologies such as DBC. These circuit carriers are generally limited in terms of providing mechanical support to passive components, especially components that are not implemented directly on the substrate. This means that the passive components that are implemented in the ISM above the thermal interface will need additional mechanical support which can be provided by the heat path and heat collector structures of the integrated heat sink.

The heat collectors can be used, in addition to collecting the heat dissipated in the component, to hold the components together in the case of components consisting of several parts, provided the appropriate electrical isolation and thermal coupling are included. The heat paths can then be used to locate the components with their heat collectors anywhere within the ISM volume. Not only does this provide a significant degree of freedom in the location of the component but it can also completely remove the need for additional mechanical support for the passive components such as that provided by plastic bobbins for inductors and transformers.

In the automotive ISM it is also important to ensure that the module is not sensitive to vibration or mechanical shock. In conventional circuit construction techniques, the connection between circuit carrier and the component leads or terminals is often the only form of mechanical support available for the passive components. An example is an electrolytic capacitor mounted

on a substrate. Any mechanical vibration or shock is transferred to the component through the component leads or terminals, weakening the electrical contact over time [6-10]. Using the heat paths and heat collectors in the ISM to provide mechanical support for the components can help avoid any problems due to interconnections failing as a consequence of mechanical vibration or shock. This is due to the fact that the component is securely fixed in the heat collector and vibrations or mechanical shocks are transferred to the component through the rugged integrated heat sink and not the passive component connection terminals.

When using the integrated heat sink structure to provide the required mechanical integrity to the components, care must be taken to avoid reliability issues that arise from the different coefficients of thermal expansion [6-10][6-11]. This has been addressed in Chapter 5, section 4.4, where it was seen that by placing a compressible interface material between the hard and irregular surfaces in the passive component and integrated heat sink structure, good thermal coupling and mechanical stress relief can be achieved.

### *4.1.3 Housing and protection*

A third possibility in extending the functionality of the integrated heat sink is to extend the integrated heat sink structure in such a way as to also implement the ISM housing. Implementing the ISM housing requires extending the integrated heat sink structure to form a sealable shell around the components within the ISM.

Using the integrated heat sink structure to implement a sealable shell around the ISM removes the requirement of an additional cover structure that must be attached to the ISM. This can help to reduce the ISM volume and increase the power density. The housing implemented with the integrated heat sink structure must provide the same functionality as a conventional cover, namely seal and protect the sensitive components within the ISM from the environment, whilst still implementing the thermal management function.

Additional benefits can also be obtained by using the integrated heat sink to implement the ISM cover. For example, if the integrated heat sink structure is implemented with aluminium, then the cover will also provide protection against EMI radiation, either escaping or entering the ISM. Since the cover is conductive and hermetically seals the ISM, electromagnetic radiation can neither enter nor escape the module.

### *4.1.4 The multifunctional integrated heat sink*

To maximise the volume reduction achievable by making the integrated heat sink multifunctional, as many functions should be implemented with the thermal management structure as practicably possible. An example of the integrated heat sink structure being used to implement all three of the above additional functions is illustrated in Figure 6.16.

The integrated heat sink forms a hermetically sealed housing by extending all around the components within the ISM. In addition, all of the passive components are implemented in their individual heat collector structures. The heat collector structures are part of the component's assemblies because they provide the components with mechanical support and integrity. Finally, all of the heat collectors in the ISM are located above the thermal interface and held in place by the combined heat paths. The heat paths are only connected to the thermal interface around the parameter of the ISM and all the heat collectors share common heat paths to both remove the heat collected by the heat collectors and hold the heat collectors in place. If the temperatures of the heat sources within the heat collectors are too high, they can be reduced

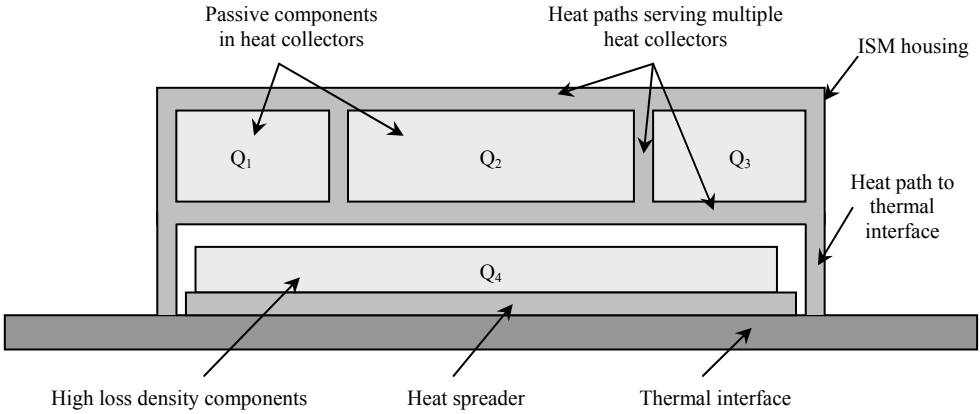



**Figure 6.16. An example of using the integrated heat sink to implement multiple functions to minimise the volume of the ISM**

by adding additional heat paths between the heat collectors and the thermal interface. Through the multifunctionality of the integrated heat sink structure, the volume of the ISM can be reduced, allowing higher power densities whilst still meeting the thermal specifications.

## 4.2 Geometric optimisation

In any power electronic system there is always unused volume contributing to the total system volume [6-12]. Removing or minimising this unused volume can contribute significantly to improving the system's power density. To remove or minimise the unused volume without changing the system's primary characteristics, the geometry and location of the components within the system must be considered. This can be achieved on at least two levels:

i. simply repacking the same components into a smaller volume with less wasted space between the various components [6-13] and
ii. considering the components geometrically and manipulating their individual shapes so that they complement each other.

The first of the two methods is currently the most popular when attempts are made to increase the power density, but has had limited success. The second method requires the shapes of the various components and their interaction with other components within the assembly to be considered and then manipulated to minimise the unused volume. This is a more a labour-intensive design but can significantly reduce the unused volume within the assembly.

The latter approach is considered in this part of the chapter.

### *4.2.1 Component interaction*

Component interaction in this context refers to the consequences that a component's geometry, shape and volume has for the other components in the assembly and on the assembly itself in terms of the assembly's volume and does not include electromagnetic interaction between the components. For example, a component with a dominating dimension (such as the height of an aluminium electrolytic capacitor) can force the complete assembly to have a height that is at least equal to that of the dominating dimension. This can result in an assembly with a large amount of unused volume, especially if the assembly has other components with much smaller dominating dimensions, as illustrated in Figure 6.17 showing a typical commercial power supply. The figure illustrates the effect that components with significantly different dimensions and non-complementing shapes can have on the power density of a system.

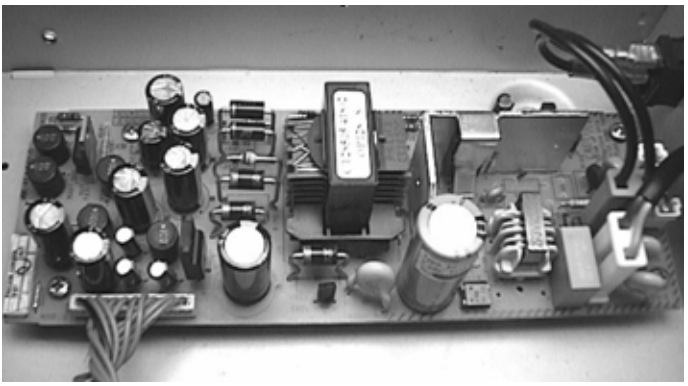


**Figure 6.17. An example of how a few components with non-conforming dimensions can result in large amounts of unused volume**

The geometric interactions between the various components in the assembly are driven primarily by their relative dimensions and geometries. The larger the difference between the relative and relevant dimensions is, the more geometrically incompatible the components are likely to be.

By manipulating the dimensions and shapes of the components in the ISM so that they are more compatible, significant volume savings can be made. Component compatibility can be achieved by:

i. using components with similar shapes, or similar footprints,
ii. using components or combinations of components with similar dimensions (specifically components with large volumes) and
iii. exploiting the third dimension for component placement.

This is briefly illustrated in Figure 6.18, which shows two hypothetical component assemblies of the passive components in a filter as well as the total volume each occupies. The more

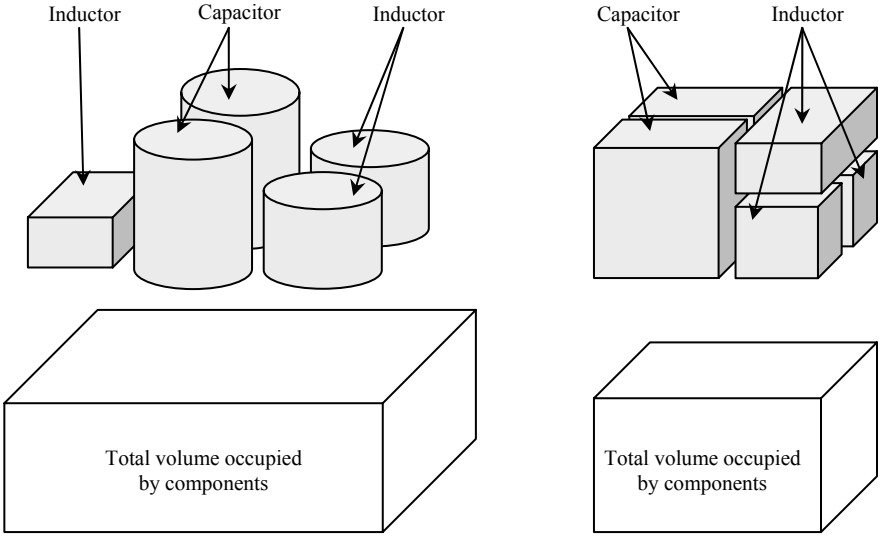



**Figure 6.18. Assemblies using geometrically incompatible (left) and geometrically compatible (right) components to implement a passive filter**

traditional arrangement on the left uses a variety of shapes with a range of dimensions, making it difficult to minimise the unused volume. However, the assembly on the right, having the same number of components and the components having the same volume as the assembly on the left, can have a significantly smaller total volume because the components are geometrically more compatible. Compatibility is achieved by having dimensions that are similar or multiples of each other and shapes that can be assembled together with the minimum unused volume. It should also be mentioned that implementing interconnections in the more traditional assembly on the left of Figure 6.18 is easier than implementing the same interconnections in the geometrically optimised assembly on the right.

To determine the optimum combination of component geometry and assembly configuration, many combinations have to be investigated. Determining the best solution can be done with the aid of a figure of merit, namely, the Relative Volume Utilisation and the total assembly volume. Based on the results of the figure of merit and total volume, the optimum geometric solution can be found.

The Relative Volume Utilisation is defined to assist in determining how well an assembly of components has been packaged into the assembly relative to the assembly volume and is defined as:

$$\varsigma_{relative} = \frac{\sum \psi_{component}}{\sum \psi_{component} + \psi_{unused}} = \frac{\sum \psi_{component}}{\psi_{total\_assembly}} \tag{6.20}$$

where $\zeta_{relative}$ is the Relative Volume Utilisation,
$\sum \psi_{component}$ is the total component volume in the assembly [$m^3$],
$\psi_{unused}$ is the total unused volume in the assembly [$m^3$]
and $\psi_{total\_assembly}$ is the total assembly volume [$m^3$].

The Relative Volume Utilisation is an indication of how well the assembly volume is being utilised to implement the components and parts thereof in and is desired to be as high as possible. It does however not give an indication if the total assembly volume is the smallest volume possible for the assembly.

Using the Relative Volume Utilisation figure of merit and the total assembly volume, a variety of different assembly configurations can be easily compared to each other and the most satisfactory solution can be found.

### *4.2.2 Exploiting the third dimension*

One of the principal means of reducing the assembly volume and improving the Relative Volume Utilisation of an assembly is to exploit the third dimension. This means to place components freely in all three dimensions instead of being restricted to the traditional two-dimensional construction approach. Smaller components can be geometrically arranged on top of each other so that they have similar dimensions to the dominating components within the assembly. This can help to significantly reduce the amount of unused volume in the assembly. This is also illustrated in Figure 6.18 on the right, which shows the assembly of components having a smaller total volume with some of the components placed in the third dimension.

The integrated heat sink is a key means of placing components, primarily passive components

in the third dimension in the ISM as discussed in the previous chapter. The integrated heat sink structure gives the freedom of placing passive components almost anywhere within the ISM volume while still being able to meet the component's thermal requirements.

### *4.2.3 Limitations on geometric optimisation*

The geometric optimisation of an assembly is subject to certain laws, constraints and considerations, namely:

i. System specifications
ii. Circuit theory laws
iii. Electromagnetic laws
iv. Thermal management considerations
v. Reliability considerations
vi. Mechanical capabilities.

These limitations maintain the assembly's electrical and thermal functionality and should be taken into consideration while the various geometrical assembly candidates are being considered. They limit the level of manipulation possible within the assembly while still achieving the desired electrical and thermal specification.

A typical example of these limitations is the relative location of the two switching devices in a totem pole phase arm configuration. From an electromagnetic point of view, the two switching devices must be located as close to each other as practicably possible to avoid extensive voltage overshoot and ringing, which increase the devices losses. This condition must be met in the assembly under consideration. Assembly candidates that do not meet this electromagnetic requirement are not suitable and cannot be used.

## *4.3 Volumetric and geometric optimisation of a phase arm*

To illustrate the volumetric and geometric optimisation of an assembly, a phase arm similar to that implemented in the ISM is considered in this section.

### *4.3.1 The phase arm*

The phase arm to be optimised is illustrated in Figure 6.19. The phase arm consists of two MOSFETs, including the freewheeling diodes ($SW_1$ and $SW_2$), one high frequency decoupling capacitor ($C_{42}$), one inductor ($L$) and one resistive shunt required for current measurement ($R$). The capacitor, $C_{42}$ in the figure, is not the complete bus capacitance required to meet the voltage ripple specification but is only the high frequency decoupling capacitor. If more than one phase is to be implemented then the bulk bus capacitor will be common to all the phases and as such is not packaged with the individual phases. The phase arm operates between the

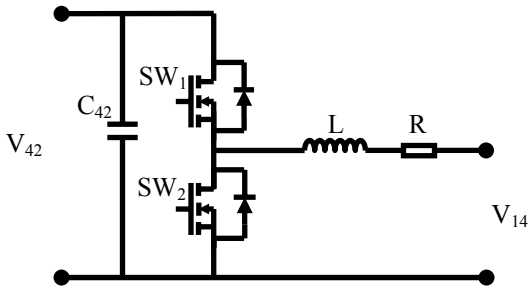



**Figure 6.19. The phase arm used to illustrate the volumetric and geometric optimisation of a phase arm**

**Table 6.5. The phase arms operating specifications**

| Parameter | Nominal Value | Range |
|---|---|---|
| P | 500W | |
| $V_{42}$ | 42V | 30V → 50V |
| $V_{14}$ | 14V | 11V → 16V |
| $I_{42}$ | 11.9A | 10A → 16.6A |
| $I_{14}$ | 35.7A | 31.25A → 44.45A |

**Table 6.6. The phase arm component values**

| Component | Value |
|---|---|
| $C_{42}$ | Ceramic 12.6μF |
| L | 3.8μH |
| R | 1mΩ |
| $SW_1$ and $SW_2$ | Open die MOSFETs |

nominally 42V and 14V bus voltages denoted by $V_{42}$ and $V_{14}$ respectively. The phase arm specifications are listed in Table 6.5 while the component specifications are listed in Table 6.6.

### *4.3.2 Energy storage requirements*

From Chapter 4, the energy stored in a single phase phase-arm inductor as illustrated in Figure 6.19 is given as:

$$E_{\max\_L} = \tfrac{1}{2} L \left[ \frac{P}{V_{14}} + \tfrac{1}{2} \Delta I_L \right]^2 \tag{6.21}$$

where
$$\Delta I_L = \frac{\left(V_{42} - V_{14}\right)\frac{V_{14}}{V_{42}} T_s}{L} \tag{6.22}$$

$E_{max\_L}$ is the maximum energy stored in the inductor [J],
$P$ is the power rating of the phase arm [W]
and $T_s$ is the switching period of the phase arm [s].

Assuming $1/T_s$ is 140kHz, the maximum energy that must be stored in the inductor is 0.46mJ.

Similarly, the maximum energy that must be stored in the decoupling capacitor is given as:

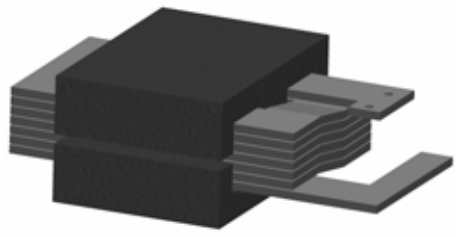
$$E_{\max\_C} = \tfrac{1}{2} C_{42} V_{42}^2 \tag{6.23}$$

where $E_{max\_C}$ is the maximum energy to be stored in the decoupling capacitor [J].

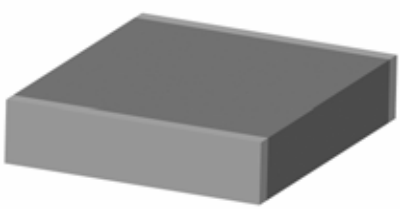
For the given capacitance and maximum bus voltage ($V_{42}$=50V), the maximum energy stored in the capacitor is 15mJ, significantly more than in the inductor.

### *4.3.3 The Selected components*

The components selected for implementing the phase arm are based on the energy requirements calculated previously and geometrical compatibility issues discussed in the previous section. There are infinitely many components available for the given specifications



The inductor without isolation



Ceramic capacitor

Open die MOSFET

Resistive shunt

**Figure 6.20. The components used to implement the phase arm**

**Table 6.7. The properties and volumes of the components selected for the phase arm**

| Component | Value | Volume [$mm^3$] |
|---|---|---|
| L (Ferrite, winding, isolation) | 3.8µH | 5714.4 |
| $C_{42}$ | 12.6µF | 1161.3 |
| R | 1mΩ | 52 |
| $SW_1$ and $SW_2$ open die devices | | 7.3 each |

but only one possible assembly solution is illustrated based on the selected components. The properties and volumes of the components selected for the phase arm are tabulated in Table 6.7.

The components listed in Table 6.7 are graphically illustrated in Figure 6.20. The phase arm inductor is illustrated in the upper left-hand corner with the electrical isolation between the winding and ferrite removed. The ceramic decoupling capacitor is illustrated in the upper right corner. The ceramic capacitor is large and its dimensions are selected to be similar to the footprint of the inductor's core. The reason for this will become clear in the following section. The open die MOSFETs and the resistive shunt are illustrated in the bottom left and right of the figure respectively. The footprints of these components are also selected to be similar to each other.

### *4.3.4 Example of assembly*

The phase arm assembly can be assembled in many different ways all with their own advantages and disadvantages. One possible assembly, taking into consideration the thermal constraint of the ISM, is illustrated in Figure 6.21a. The figure shows the complete assembly including bus bars and interconnections between the various components. In addition, the inductor is implemented in an integrated heat sink structure as described in Chapter 5.

The assembly is implemented as follows: the main circuitry, semi-conductors, shunt and decoupling capacitor are all implemented on DBC substrate that is attached directly to the thermal interface. The exact location of the semi-conductors and the decoupling capacitor can be seen more clearly in Figure 6.21b, which shows a cross-section through the structure. The dimensions of the ceramic capacitor are critical in the assembly because they determine the

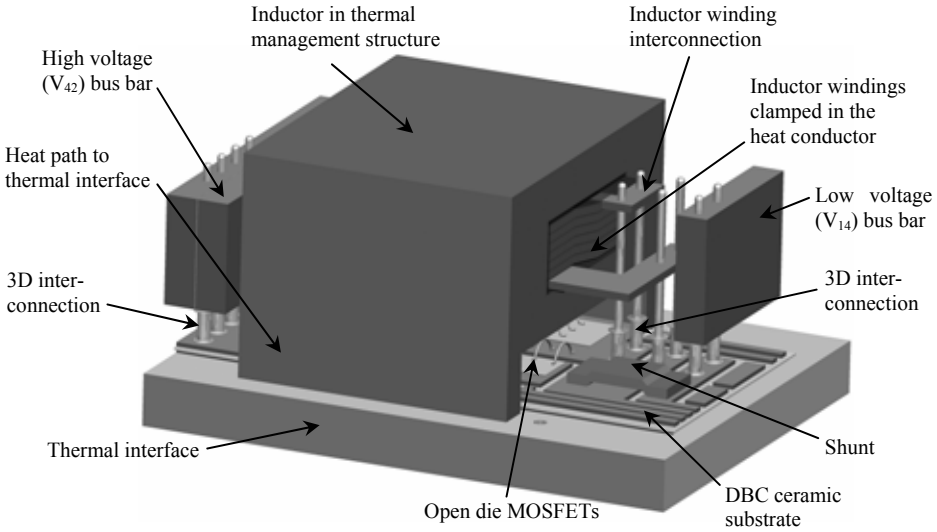



**Figure 6.21a. A possible assembly configuration for the phase-arm**

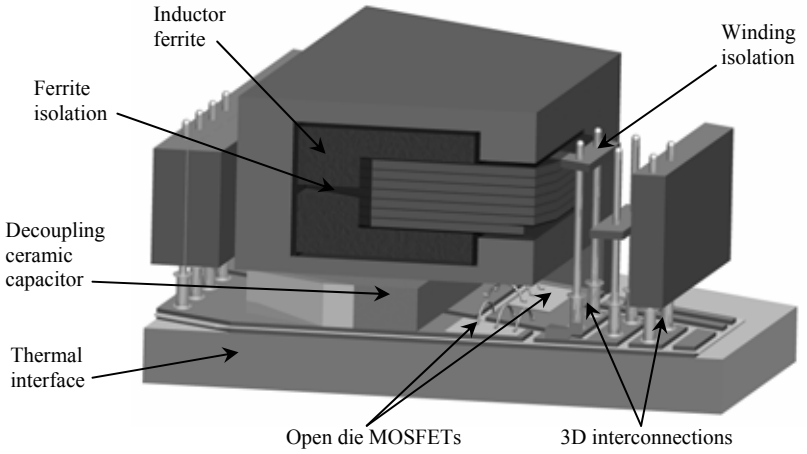



**Figure 6.21b. A section through the assembly**

width of the DBC substrate. Moreover, since the inductor structure is implemented with an integrated heat sink, placing the inductor in the third dimension above the capacitor, the height of the capacitor also determines the length of the heat paths between the inductor heat collector and the thermal interface. The width of the capacitor also fixes the width of the inductor structure. The integrated heat sink structure in which the inductor is mounted is also used to remove the heat dissipated in the ceramic decoupling capacitor. The inductor heat collector is dimensioned so that the bottom part of the inductor heat collector is in thermal contact (electrically isolated) with the top of the ceramic capacitor. Thus the heat collector of the integrated heat sink structure serves two components simultaneously. The inductor structure is also implemented so that it extends over the semi-conductors, resulting in a very short vertical electrical interconnection between the semi-conductors and the inductor. This is clearly visible in Figure 6.21b.

The bus bar structures are implemented vertically as illustrated in the figure, so as to reduce

**Table 6.8. The volumetric break down of the assembly**

| Parameter | Volume ($mm^3$) | Percentage (%) |
|---|---|---|
| Total assembly volume | 40162 | 100 |
| Total occupied volume | 23416 | 58.3 |
| Total unused volume | 16747 | 41.7 |
| | | |
| Inductor (without integrated heat sink) | 5714.4 | 14.24 |
| Decoupling capacitor | 1161.3 | 8.6 |
| MOSFETs | 7.3 each | 0.018 |
| Shunt | 52 | 0.12 |
| Bus bars | 3564 | 8.8 |
| Interconnections | 145.6 | 0.36 |
| DBC | 1089 | 2.7 |
| Integrated heat sink | 9087 | 22.6 |
| | | |
| Relative Volume Utilisation ($\zeta_{reltive}$) | | 58.3 |

their footprint on the thermal interface. The vertical implementation of the bus bars also allows the bus bars to have sufficient conduction cross-sectional area without requiring a large footprint on the thermal interface, thereby reducing their conduction losses. The bus bars are connected to the DBC through two-part pin and barrel structures. One part is soldered to the bus bar and the second to the DBC. The two parts are then press-fitted into each other. To avoid mechanical stresses in the interconnection structures they are designed to allow a small degree of vertical movement. The same pin structures are used to connect the inductor to the DBC. Several pins are used in parallel to achieve the required current rating.

In this structure, the dimensions of the ceramic decoupling capacitor are critical since all the remaining components together with their individual support structures are designed relative to the decoupling capacitor. This illustrates the impact a single component can have on the design and geometric arrangement of an assembly of components.

The volume of the components used to implement the assembly and the Relative Volume Utilisation are tabulated in Table 6.8. The table shows that only 58.3% of all the assembly volume is used to implement the components or parts thereof. Of the volume occupied, the largest portion is occupied by the integrated heat sink structure followed by that of the inductor and then the capacitor. The table also justifies the decision to disregard the semi-conductor devices in the volumetric optimisation of the assembly since the two devices together occupy less than 0.04% of the assembly volume.

The phase arm capable of processing 500W with a maximum output current of 44.45A is implemented in a volume measuring 46mm by 26.4mm by 33mm. Even though the assembly is arranged in such a way as to minimise wasted volume, a Relative Volume Utilisation of only 58.3% is achieved. This is relatively high for a power converter assembly. More conventionally implemented assemblies can have a Relative Volume Utilisation as low as 20% if not lower. In the presented structure, the majority of the wasted volume is due to the interconnections between the DBC substrate and the components in the third dimension such as the bus bars and the inductor.

This structure is revisited in Chapters 7 and 8 where it is experimentally implemented and evaluated.

## 5. Summary

This chapter considered the volumetric and spatial design interdependence within the ISM. Specifically it considered the relationship between the volume required to store or process a given amount of energy and the volume required to remove the heat dissipated in the process of manipulating the energy while minimising the total component or system volume. The volume miniaturisation is considered on two levels, namely on a component level and a system level.

On a component level, volume miniaturisation is possible by manipulating the volume of the parts of the component that do not contribute directly to the energy storage capability of the component. For example, in section 3.2, the volume of an inductor is reduced by increasing the current density in the winding. For a given maximum current rating, the winding volume decreases as the current density increases. If the cross-sectional area of the core is fixed, then the winding window area can be reduced, reducing the total volume of the core without increasing the magnetic flux density in the core. However, as the current density increases for a given rating, the losses in the component will also increase. For the structure considered, the relationship between the inductor's volume and losses is summarised in Figure 6.7.

To reduce the component's total volume, the volume of the integrated heat sink must also be considered. This is achieved by defining the VRC in equation 6.18 under certain assumptions. For the given structure and given excitation, the relationship between the total combined volume (inductor and integrated heat sink) and the maximum temperature drop between the component hotspot and thermal interface can be derived. This is highly dependent on the component design, materials and excitation. The relationship for this case is summarised in Figure 6.12, which shows the maximum temperature drop in the component for a given current density, total volume and VRC. This graph shows that acceptable temperature drops can be achieved in an inductor with very high current densities by manipulating and optimising the volume associated with the energy storage and the volume associated with heat removal structure. Two experimental structures were presented; the first structure has a current density of 15A/mm$^2$ and VRC of 0.86 and the second structure has a current density of 40A/mm$^2$ and a VRC of 1.24. The theoretical and measured maximum temperature drop versus volume and VRC is plotted in Figure 6.14.

Volume optimisation on a system level requires not only the volume of the components within the system to be miniaturised, but for the minimisation the volume required for the assembly of components forming the system. Two methods of achieving volume optimisation on a system level are considered. The first considers using a single part to perform multiple functions and the second considers the geometrical properties of the components and assembly. In both cases volume reduction is possible.

Reducing the volume of the ISM can be achieved by using the integrated heat sink structure to perform multiple functions. Examples include having several heat collectors on one heat path, using the integrated heat sink as the ISM housing structure and using the integrated heat sink as a means to hold the component assembles together and in the appropriate location. By combining all of these functions into one component or part, the number of components in the ISM is reduced and, if designed appropriately, the volume of the combined structure can be less than the sum of the volumes of the individual structures.

Lastly, the volume of the assembly of components can also be miniaturised through the geometrical optimisation of the components and assembly. Typically assemblies are

constructed without consideration being given to the components' geometry and the effect that this has on other components and on the assembly itself. By selecting and using component geometries that complement each other, the unused volume within an assembly can be significantly reduced. In addition, there are an infinite number of possible combinations of components within the assembly and even more so if the third dimension is also exploited. In order to be able to evaluate how well an assembly performs, a geometric figure of merit is required. Such a figure of merit is defined, namely the Relative Volume Utilisation, and is given by equation 6.20. The Relative Volume Utilisation represents the percentage of the total converter or assembly volume used to implement components in. Together with the assembly volume, the optimum assembly configuration can be found.

For the phase arm assembly considered in Figure 6.21, the Relative Volume Utilisation was approximately 58.3%. This indicates that even though the assembly is highly compact, there is still significant volume that is not being used. In the presented assembly, the interconnections between the DBC substrate and the components in the third dimension account for a large portion of the wasted volume.

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# Chapter 7

## DESIGN OF THE AUTOMOTIVE ISM

## 1. Introduction

In the previous four chapters, the interdependence between the electrical, thermal and spatial designs of the automotive integrated system module were considered. This interdependence was graphically defined in Chapter 3 and is repeated here in Figure 7.1. In this chapter, this relationship is used and exploited in the design of an experimental automotive ISM prototype to a given set of specifications. The purpose of this chapter is to illustrate how the interdependences that have been defined and explored in the previous three chapters can be used to implement a functional ISM, thereby closing the link between concept and practice.

The chapter begins by first presenting the specifications for the automotive ISM in the following section. These specifications define the boundary conditions in which the ISM prototype must be implemented and evaluated.

Once the specifications have been presented, an overview of the interdependent ISM design is given. The overview briefly describes how the design is performed. The complete design of the ISM cannot be presented in this chapter, so this section serves to highlight those parts of the design that are considered most critical.

In the following three sections, the electrical, thermal and spatial designs of the ISM are presented. The designs are based on the work presented in Chapters 4 to 6 respectively and the concepts used in these chapters are exploited in the ISM prototype. Only the significant design

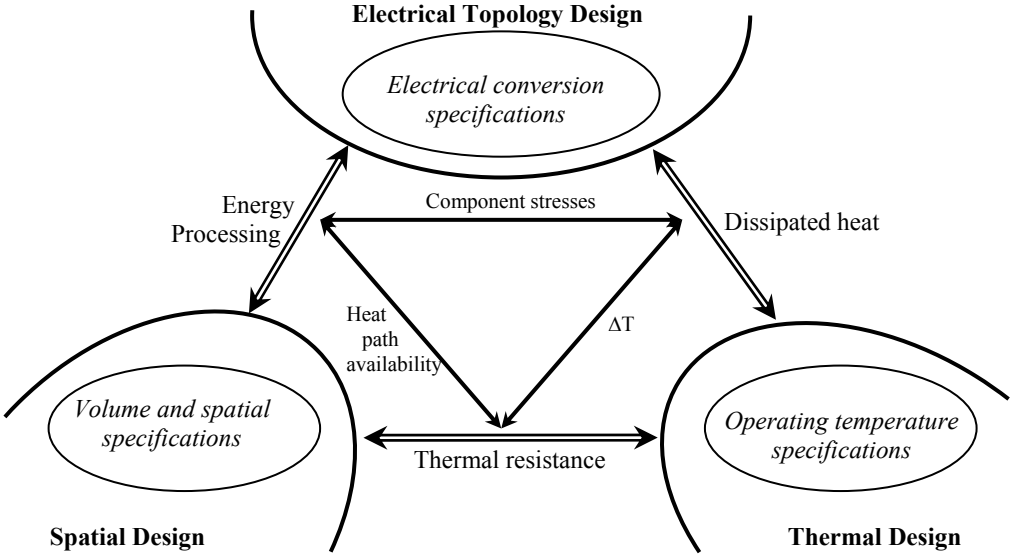


**Figure 7.1. The relationship between the electrical, thermal and spatial designs**

details are presented in these sections, with the supporting analysis in the appendixes.

## 2. Specifications

The specifications for the automotive ISM are tabulated in Table 7.1 as defined by a third party (Siemens CT, Munich) [7-1]. The specifications require a highly integrated module containing the complete system required for power conversion over a large working range, both thermally and electrically, while having a high power density. Also note that the specifications fix the phase switching frequency based on EMI constraints.

### 2.1 Control of the module

The converter control does not form a part of this thesis. However, in the interest of completeness it is briefly described.

**Table 7.1. The complete specification list for the experimental automotive ISM**

| Specification | Description | Requirement |
|---|---|---|
| Mechanical contents | | The converter includes: the bi-directional DC/DC converter, the DC bus capacitors, the gate drives, the control system, EMI filters and interconnections. |
| Volume | Length by width by depth | Minimum volume |

| Thermal specifications | Description | Requirement |
|---|---|---|
| Full power operating temperature | Minimum temperature<br>Nominal temperature<br>Maximum temperature | -40°C<br>+85°C<br>+110°C |
| Temperature de-rating | Power de-rating of 50% | +110°C → +125°C |
| Thermal limit | Thermal protection | +125°C |
| Coolant flow rate | Volume flow rate | 6.0 – 12.0 l/min |
| Coolant | Water – Glucose | 50% - 50% by volume |

| Electrical Specifications | Description | Requirement |
|---|---|---|
| Maximum power rating | Nominal voltage range<br>Buck mode : 30V-50V / 11V-16V<br>Boost mode : 11V-16V / 30V-50V | 2kW |
| Control power source | Power from the 14V terminal | Minimum voltage: 8V |
| Converter efficiency | At nominal temperature of 85°C | >90% |
| Switching frequency | Maximum per phase arm | 140kHz |

| Robustness | Description | Requirement |
|---|---|---|
| EMI | Measured at full thermal and electrical load | CISPR 25 |
| Transients | Transients due to switching load on the 42V net that the control loop must handle | 22V / 20ms |

| Control | Description | Requirement |
|---|---|---|
| Control system communication | BUS - system | CAN 2B |

The converter controller is divided into two parts – a high-level digital controller and a low-level analogue controller. The analogue controller implements current mode control in each phase but does not perform voltage control. The digital controller interfaces the analogue controller to the main system controller (the automobiles energy management system for example). It communicates the required current to be transported between the voltage busses depending on the measured voltage to the analogue controller, which adjusts the current accordingly. The required power command is given to the digital controller through a CAN interface from the main vehicle control system.

## 3. Overview of the ISM design

The design of the ISM is divided into three sections, namely, the electrical design, the thermal design and the spatial design. The aspects that are considered in each section are listed below:

i. Electrical design
   a. *Fixing the topology*. In this thesis the topology has been fixed to the synchronous rectifier presented in Chapter 4.
   b. *Find the optimum number of phases*. To find the optimum number of phases, the optimum phase arm inductance is determined. Then the optimum number of phases and the bus capacitance can be determined. This is based on the minimum stored energy and RMS current analysis in Chapter 4.
   c. *Decide on preliminary components*. This determines the technologies that are available.
   d. *Estimate component losses*.

ii. Thermal design
   a. *Define the thermal management concept.* The integrated heat sink is used to provide the necessary thermal management for the passive components. This structure was introduced in Chapter 5, where it was evaluated.
   b. *Miniaturise the components.* Use the integrated heat sink structure together with the reduced energy storage requirement to reduce the volume of the passive components.
   c. *Thermal simulations.* Use thermal simulations of the integrated heat sink together with the estimated losses in the component to determine the temperature-drop in the component, the heat collector and heat path.

iii. Spatial design
   a. *Define preliminary layout.* This is required for the spatial design.
   b. *Spatial design*. Perform a detailed spatial design determining exactly where and how the components are located in space. If necessary change the components' shapes to reduce the unused volume within the module. The geometric design is based on that presented in Chapter 6.
   c. *Define all materials*.
   d. *Evaluate and reiterate*. Evaluate the module and if necessary make changes to the design to meet the electrical, thermal and volumetric requirements.

In the following three sections, the above aspects are considered more closely for the automotive ISM given the specifications in Table 7.1.

## 4. The electrical design (based on Chapter 4)

In Chapter 4, the tools for optimising the electrical topology for a high power density and high operating temperature were considered. In this section of the chapter, they are used to help design the automotive ISM.

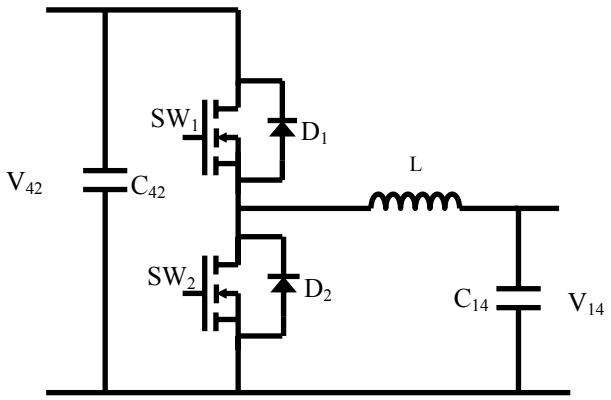


**Figure 7.2. The synchronous rectified bi-directional phase-arm**

## 4.1 The topology

The requirements for a topology to implement a high power density ISM in a high temperature environment were considered in Chapter 4. These included the topology having a relatively low component count, being a direct topology, having low component stresses, being easy to control and being relatively insensitive to temperature variations. The bi-directional synchronous rectifier was selected as the topology meeting most of these requirements. To reduce the RMS currents and component stresses in the topology, multiple phase are interleaved at the expense of some additional components. The bi-directional synchronous rectifier to be implemented in the ISM is illustrated in Figure 7.2, which shows a single phase.

The parameters for the passive components (inductance and capacitance) and the number of phases are determined as discussed in Chapter 4.

## 4.2 The optimum number of phases and component parameters

The RMS current and the energy that must be stored in the passive components is a function of the number of phases, the duty cycle and the phase inductance. To determine the RMS current and the energy storage requirement as a function of the number of phases, at least the phase arm inductance is required since the terminal voltage ranges are clearly specified.

### *4.2.1 The phase arm inductance*

To determine the phase arm inductance, the total energy to be stored in all the passive components and the RMS current in $C_{42}$ is calculated and plotted in Figure 7.3a and Figure 7.3b respectively for a duty cycle of 33% as a function of the phase arm inductance. Two assumptions are made in generating these graphs, namely the capacitor $C_{42}$ suffers the largest RMS currents between the two bus capacitors and, secondly, it is assumed that the voltage ripple over the two bus capacitors is in the order of 1% of the bus voltage. Note that the duty cycle of 33% is the nominal duty cycle but it must be remembered that the topology operates over a duty cycle range of at least 20% to 50%.

The two graphs show the energy to be stored in the passive components within the ISM and the RMS current in $C_{42}$ as a function of the number of phases and the phase arm inductance. Both graphs show that the influence of the phase inductance is limited once the inductance value has passed a certain value for a given number of phases. This is especially the case with the RMS current clearly showing the RMS current decreasing with the increasing inductance and then reaching a plateau value from which it does not change as the inductance is further increased.

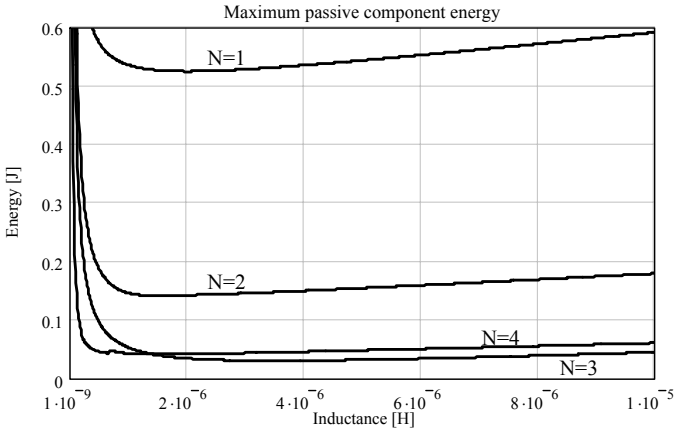


**Figure 7.3a. The energy stored in all the passive components assuming a 1% voltage ripple on the capacitors and a duty cycle of 33%**

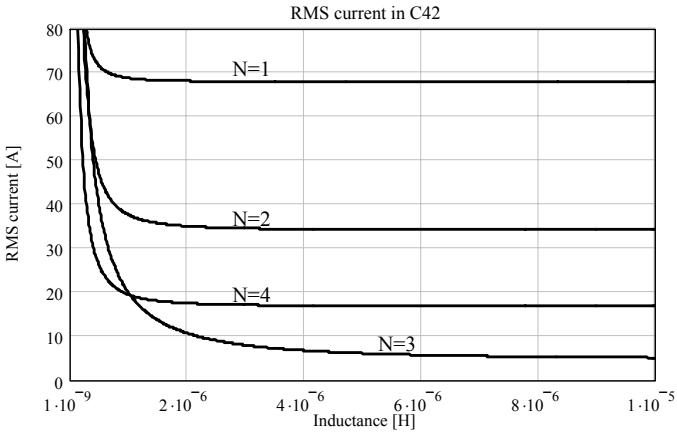


**Figure 7.3b. The RMS current in $C_{42}$ assuming a voltage ripple of 1% on the capacitors and a duty cycle of 33%**

In terms of the phase arm inductance, this means that a single value of inductance can be selected to be implemented in a topology with an unspecified number of phases. This also means that using an inductor with a large inductance does not have any advantages over an inductor with a significantly smaller inductance with reference to the RMS current in $C_{42}$. In terms of the energy stored in the passive components, a large inductance will result in more energy being stored than necessary. A smaller inductance value also has several advantages from a construction and thermal management point of view.

Based on the two graphs presented in Figure 7.3, a phase arm inductance of 3.8µH is selected.

### *4.2.2 The optimum number of phases*

With the phase arm inductance fixed, the energy to be stored and the RMS currents in the passive components can be calculated as done in Chapter 4. The RMS currents in the two bus capacitors and the phase arm inductor are plotted in Figure 7.4 as a function of the duty cycle and the number of phases. Figure 7.4a to Figure 7.4c shows the RMS currents in $C_{42}$, $C_{14}$ and $L$ respectively for one through to four phases. Figure 7.4b to Figure 7.4f, shows the RMS current in $C_{42}$, $C_{14}$ and $L$ respectively as a function of the terminal voltages for a 4-phase system.

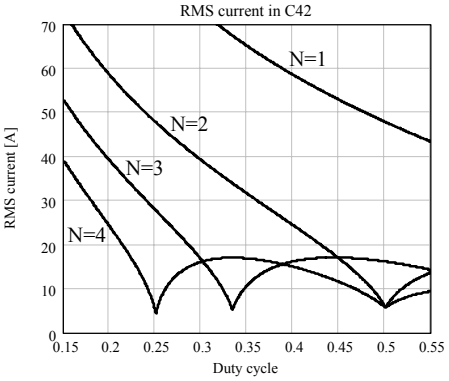


**Figure 7.4a. The RMS current in $C_{42}$ as a function of N**

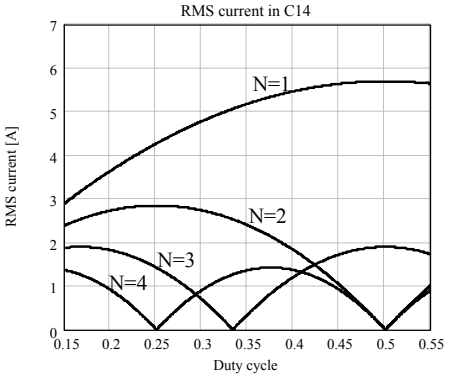


**Figure 7.4b. The RMS current in $C_{14}$ as a function of N**

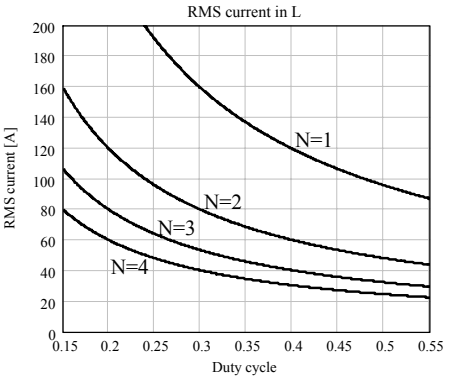


**Figure 7.4c. The RMS current in L as a function of N**

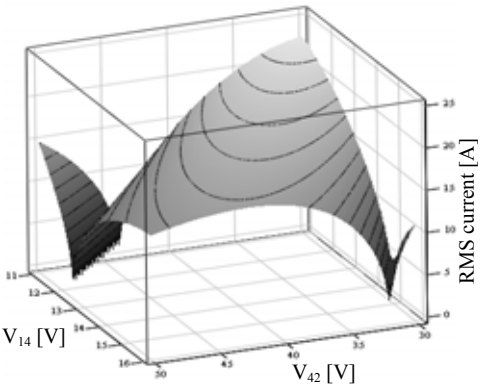


**Figure 7.4d. The RMS current in $C_{42}$ for 4 phases as a function of the terminal voltages**

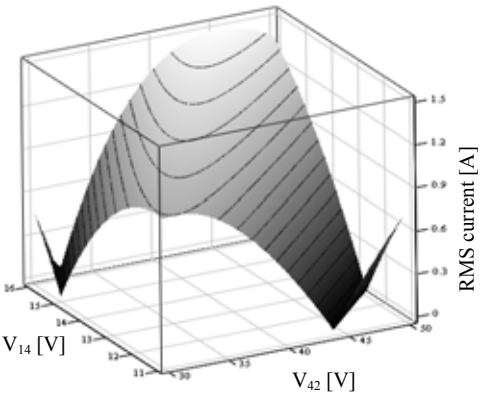


**Figure 7.4e. The RMS current in $C_{14}$ for 4 phases as a function of the terminal voltages**

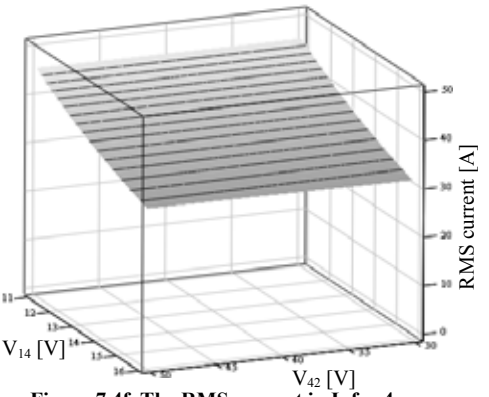


**Figure 7.4f. The RMS current in L for 4 phases as a function of the terminal voltages**

Considering the first three figures (Figure 7.4a, Figure 7.4b and Figure 7.4c) over the duty cycle range of 20% to 50%, it is clear that the 4-phase system has the lowest maximum RMS current. A higher number of phases will have still lower RMS current requirements, but it is decided not to exceed four phases in the prototype. If four phases is selected as the optimum

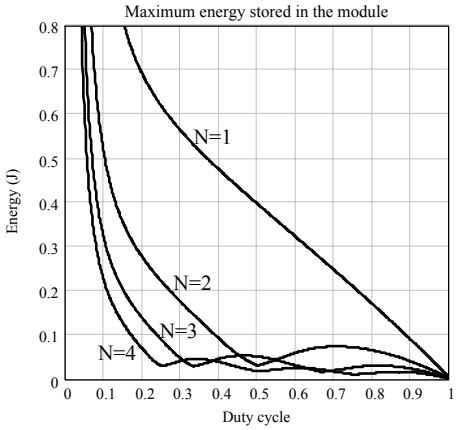


**Figure 7.5. The maximum energy stored in the passive components as a function of the number of phases**

number of phases based on the RMS current alone, the second set of figures (Figure 7.4d, Figure 7.4e and Figure 7.4f) show the maximum RMS currents in these components as the terminal voltages vary over the allowed working range at full load. These are the RMS currents that the components must be designed and rated for.

The total maximum energy that must be stored in the passive components is plotted in Figure 7.5 as a function of the number of phases and the duty cycle. If the duty cycle range is considered, the figure confirms that the 4-phase system has the lowest maximum energy storage requirement. The maximum requirement is found at a duty cycle of 20%.

Considering both the RMS currents and the energy that must be stored in the passive components over the given duty cycle range, the optimum number of phases is selected as 4.

### *4.2.3 The bus and decoupling capacitors*

The capacitance that is required for a given voltage ripple can be calculated from the energy that must be stored in the capacitors, as was discussed in Chapter 4. For the given specifications and a voltage ripple of 1%, the capacitance required for $C_{14}$ is only 10µF and the capacitance required for $C_{42}$ is 40µF for $V_{14}$ = 14V and $V_{42}$ = 42V. However, it must be noted that this assumes perfect current sharing between all four phases at all times and neglects the effect of reverse recovery on the capacitor currents, both of which will result in an increase of the minimum capacitance.

## 4.3 Preliminary components and technologies

The components that are selected to implement the ISM topology are briefly considered. The criteria for selecting the components and component materials are primarily the components' maximum operating temperature and RMS current rating where relevant.

### *4.3.1 Capacitors*

The capacitors in the topology are implemented with a combination of aluminium electrolytic capacitors and ceramic capacitor technologies. The aluminium electrolytic capacitors are required for implementing the bus capacitors providing the bulk energy storage and the ceramic capacitors provide decoupling for the high frequency switching devices.

The aluminium electrolytic capacitors pose a challenging problem since these components are

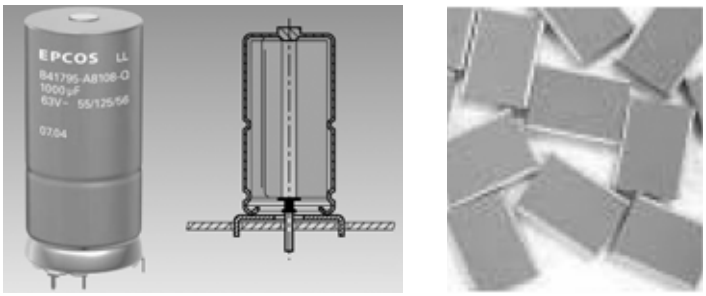


**Figure 7.6. The aluminium electrolytic (left) and the ceramic (right) capacitors used to implement the ISM bus and decoupling capacitors respectively**

normally not rated for high temperature applications. However, at the time of component sourcing, EPCOS had released their aluminium electrolytic capacitors for automotive applications; these capacitors have a maximum operating temperature of 150°C [7-2]. This capacitor in solder star casing is illustrated in Figure 7.6 on the left. These components are also specified to have a low ESR value.

The two bus capacitors were selected from the range of devices available from EPCOS based on the RMS current ratings of the components and the maximum allowed voltage. For safety reasons, the bus capacitor on the 14V bus must be able to safely handle 25V and on the 42V bus, 75V. Based on this, $C_{14}$ is selected as a single 1000µF capacitor (B41693A5108Q000) and $C_{42}$ is selected as a parallel combination of two 220µF capacitors (B41693A0227Q000). These values of capacitance are significantly more than what is required and will result in significantly more energy being stored in the ISM.

The decoupling capacitors are illustrated on the right-hand side of Figure 7.6. These capacitors are required on both the 14V and 42V terminals to provide capacitance for the higher frequency currents that are present during switching. The decoupling capacitors on the 42V bus are especially important for this function and should be placed as close to the switching devices as possible. When placed close to the switching devices, these components reduce the inductance in series with the switching devices, which in turn reduces the voltage overshoot during switching.

High temperature ceramic capacitors from Novacap are selected to implement the decoupling capacitors [7-3]. The capacitors selected have a maximum operating temperature rating of 160°C. The same voltage constraints are imposed on the selection of these components as on the aluminium electrolytic capacitors. The decoupling capacitors on the 42V bus comprise of the parallel combination of four (one for each phase) 100V 12µF ceramic capacitors (7565G126J101N). The decoupling capacitors on the 14V bus consists of the parallel combination of 3 25V 18µF ceramic capacitors (7565G186J250N).

Thus $C_{42}$ consists of a total capacitance of 448µF and $C_{14}$ consist of a total capacitance of 1054µF. This is significantly more that what is required which will result in more energy being stored in the module. However, this is unavoidable due to components and component technologies available.

### *4.3.2 Phase arm inductors*

The phase arm inductors are implemented with the same materials and technologies as the case studies presented in Chapters 5 and 6.

### 4.3.3 Switching devices

The switching devices are obtained from Infineon as bare die devices which can be attached to a custom designed DBC layout. Based on the current requirement of the devices, the switching frequency and a maximum blocking voltage of 75V, the MOSFET SPP80N08S2-07 device was selected.

This device has a maximum blocking voltage of 75V, a continuous drain current of 80A and a maximum on resistance of 7mΩ. In addition, this device has a maximum operating temperature of 175°C [7-5].

### 4.3.4 EMI filters

The EMI filters are implemented with planar transmission line filters that are primarily used to implement common mode filters. These filters are implemented with two copper conductors separated by a ceramic dielectric and inserted into a ferrite ring. The ferrite used to implement the planar filters is the 3E27 EMI ferrite manufactured by Ferroxcube. The material has a medium permeability with low losses and a relatively high maximum operating temperature of 150°C [7-4].

### 4.3.5 The implemented topology

The topology schematic including all the component values is presented in Figure 7.7. The figure shows the 4-phase topology with the relative location of the components. In addition, the resistive shunts in series with the inductors that are required to measure the inductor current for control are also included. The shunts are 1mΩ devices rated for a maximum of 3W.

## 4.4 Estimated losses

With the main components selected and with all the currents and voltages known, the losses in all of the components can be estimated. The estimated losses can then be used in the thermal design to determine the thermal management requirements.

In this section, the losses in all of the components are briefly presented. The loss calculation methods can be found in Appendixes C through to E.

### 4.4.1 Losses in the inductors

The phase arm inductor structure is implemented with the same structure, materials and configuration as the inductor structure presented in Chapter 5. The losses for this structure are presented in the same chapter and are repeated here in Table 7.2. These are the losses for a single inductor. There are four of these structures in the ISM, thus the total inductor losses will be four times that in Table 7.2.

A summary of the loss calculation for the inductor structure can be found in Appendix C.

**Table 7.2. The calculated losses for a single inductor**

| Inductor losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 5.91 | 6.351 | 6.589 | 6.66 | 6.8 | 6.96 |
| $V_{14}$=14V | 4.01 | 4.786 | 5.452 | 5.67 | 6.01 | 6.25 |
| $V_{14}$=16V | 3.23 | 3.898 | 4.771 | 5.08 | 5.57 | 6.13 |

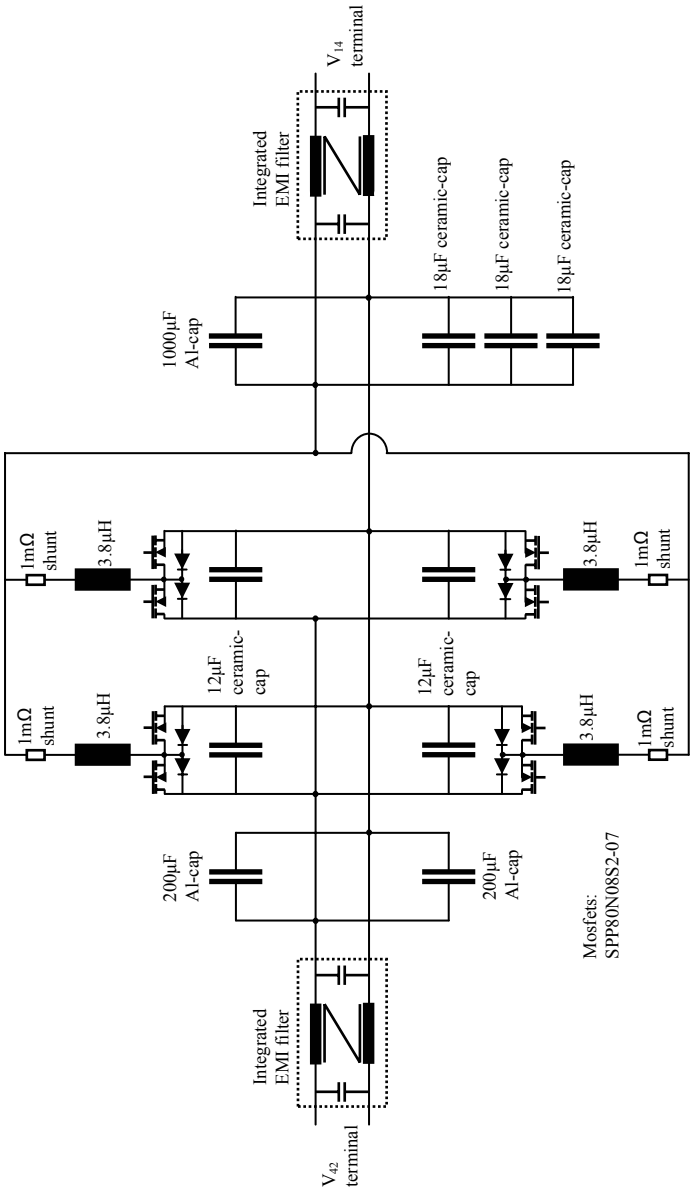


**Figure 7.7. The circuit schematic of the 4-phase interleaved bi-directional synchronous rectifier**

### *4.4.2 Losses in the capacitors*

The losses in both $C_{42}$ and $C_{14}$ are determined by measuring the capacitor impedance with an impedance analyser and then using the measured impedance in a mathematical model to determine the current distribution between the different capacitors when excited by the switching waveforms. Once the capacitor impedance and the capacitor currents are known, the apparent power in the component can also be determined. The real component of the apparent power gives the losses in the capacitor. The impedance measurement is performed at room temperature and uses small signal excitation to make the measurement.

**Table 7.3. The calculated losses in one of the two electrolytic capacitors implementing $C_{42}$**

| Electrolytic cap losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 0.06 | 0.06 | 0.05 | 0.03 | 0.02 | 0.06 |
| $V_{14}$=14V | 0.03 | 0.04 | 0.04 | 0.04 | 0.04 | 0.04 |
| $V_{14}$=16V | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 |

A detailed summary of the calculation can be found in Appendix D.

The losses in one of the two electrolytic capacitors comprising $C_{42}$ at full load are tabulated in Table 7.3 over the terminal voltage range. The losses shown are in the low milli-watt range. This is due to the significantly reduced RMS current in the component as a consequence of interleaving and the parallel ceramic capacitors. If the losses in the capacitor are calculated for the same parameters but for a single phase topology, the losses in the component are in the order of 25 to 50 times larger showing the advantages gained by interleaving. This calculation can be found in the same appendix.

The losses in one of the four ceramic capacitors comprising $C_{42}$ over the operating voltage range at full load are tabulated in Table 7.4. The losses in the ceramic capacitor are larger than those in the aluminium electrolytic capacitors since the component has a significantly higher RMS current. The higher current is due to the better frequency performance of the component (lower impedance over a large frequency range) and the fact that the ceramic capacitors are significantly closer to the switching devices than the electrolytic capacitors.

The total losses dissipated in all the capacitors comprising $C_{42}$ at full load are tabulated in Table 7.5. The table shows that the highest losses expected in the parallel combination of the capacitors are in the region of 4.35W for $V_{14}$ = 11V and $V_{42}$ = 50V and the lowest expected losses just above 1.74W for $V_{14}$ = 16V and $V_{42}$ = 45V. The trend in the losses is not very clear because with small changes in the terminal voltages, the capacitor current can have completely different waveforms and consequently different losses.

For the operating range of interest, the average ESR for the various 42V capacitors can be determined. These are tabulated in Table 7.6.

The losses in the 14V capacitors, $C_{14}$ are determined in a similar way as $C_{42}$. The calculation

**Table 7.4. The calculated losses in one of the four ceramic decoupling capacitors implementing $C_{42}$**

| Ceramic cap losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 0.84 | 0.82 | 0.89 | 0.89 | 0.93 | 1.18 |
| $V_{14}$=14V | 0.68 | 0.59 | 0.53 | 0.53 | 0.55 | 0.58 |
| $V_{14}$=16V | 0.53 | 0.53 | 0.47 | 0.45 | 0.43 | 0.44 |

**Table 7.5. The total calculated losses in $C_{42}$**

| Total $C_{42}$ Losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 3.40 | 3.39 | 3.50 | 3.42 | 3.46 | 4.35 |
| $V_{14}$=14V | 2.50 | 2.30 | 2.17 | 2.17 | 2.24 | 2.29 |
| $V_{14}$=16V | 1.93 | 1.96 | 1.83 | 1.78 | 1.74 | 1.77 |

**Table 7.6. The average ESR of the capacitors constituting $C_{42}$**

| Capacitor | ESR [Ω] |
|---|---|
| $C_{42}$ aluminium electric | 0.074 |
| $C_{42}$ ceramic capacitor | 0.015 |

**Table 7.7. The calculated losses in the electrolytic capacitor implementing $C_{14}$**

| Total $C_{42}$ losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 0.037 | 0.113 | 0.069 | 0.02 | 0.021 | 0.149 |
| $V_{14}$=14V | 0.059 | 0.06 | 0.078 | 0.117 | 0.204 | 0.149 |
| $V_{14}$=16V | 0.059 | 0.106 | 0.078 | 0.073 | 0.104 | 0.221 |

can also be found in Appendix D. The results of the calculation are tabulated in Table 7.7, which shows the total losses in the combined electrolytic and ceramic capacitors implementing $C_{14}$. The table shows that the losses are extremely low. This is due to the significantly reduced RMS current in the components as a consequence of interleaving.

### *4.4.3 Losses in the MOSFETs*

The losses in the MOSFETs are estimated on the basis of the topology waveforms and the data sheet information. The analysis can be found in Appendix E. Table 7.8 tabulates a summary of the losses in the MOSFETs for a single phase operating at nominal load ($P$=2kW, $V_{14}$=14V, $V_{42}$=42V) in buck mode and with a dead time of 100ns. The results show that the losses associated with the reverse recovery of the free-wheeling diode contribute the largest portion of the switching device losses followed by the switching losses of $SW_1$. In the implemented topology, the free-wheeling diodes are implemented with the body diodes of the MOSFETs. Replacing these diodes with alternative diodes such as schottky devices can significantly reduce the losses associated with reverse recover of the free-wheeling diode.

**Table 7.8. The loss distribution in the MOSFETs for a single phase**

| Switching losses | |
|---|---|
| $SW_1$ turn on losses | 3.9 W |
| $SW_1$ turn off losses | 8.3 W |

| Conduction losses | |
|---|---|
| $SW_1$ | 6.7 W |
| $SW_2$ | 6.1 W |

| Gate Charge losses | |
|---|---|
| $SW_1$ | 0.16 W |
| $SW_2$ | 0.16 W |

| Diode losses | |
|---|---|
| Conduction losses | 1.7 W |
| Reverse recovery losses | 17.5 W |

| Total device losses for a single phase | |
|---|---|
| $SW_1$ | 18 W |
| $SW_2$ | 26.1 W |

**Table 7.9. The calculated losses in the MOSFETs for all four phases**

| Total MOSFET losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 207.4 | 217.8 | 228.26 | 232.6 | 241.3 | 249.9 |
| $V_{14}$=14V | 157.8 | 166 | 174.4 | 177.8 | 184.8 | 191.8 |
| $V_{14}$=16V | 136.5 | 144.5 | 151.9 | 154.9 | 161.1 | 167.4 |

**Table 7.10. The estimated EMI filter losses**

| EMI filter losses [W] | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 18.65 | 17.65 | 17.00 | 16.80 | 16.48 | 16.24 |
| $V_{14}$=14V | 12.96 | 11.96 | 11.31 | 11.11 | 10.79 | 10.54 |
| $V_{14}$=16V | 10.81 | 9.81 | 9.16 | 8.96 | 8.64 | 8.39 |

The total MOSFET losses in all four phase arms are tabulated in Table 7.9 over the operating voltage range and at nominal power. The losses are calculated at room temperature.

### *4.4.4 Losses in the EMI filters*

The losses in the EMI filters are estimated by calculating the DC resistance of the expected EMI filter's structures. This calculation only gives an indication of the losses in the filters due to the large DC currents and can change depending on the requirements of the implemented EMI filters. The combined estimated losses in both the 14V and 42V EMI filters are tabulated in Table 7.10.

### *4.4.5 Losses in the resistive shunts*

The losses in the 4 1mΩ shunts in series with the inductors are also included in the loss estimation. The losses in these components based on the RMS current in the inductors are tabulated in Table 7.11. As much as 8.34W is dissipated in the 1mΩ shunts.

### *4.4.6 Projected efficiency*

The projected efficiency can be estimated by taking the sum of all the previously calculated losses. The estimated efficiency is tabulated in Table 7.12 for nominal operation at room temperature. The estimated efficiency at full load for the ISM varies between 86% and 92% depending on the terminal voltages and is expected to have an efficiency of approximately 90%

**Table 7.11. The calculated losses in the resistive shunts**

| Shunt losses [W] | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 8.32 | 8.33 | 8.33 | 8.34 | 8.34 | 8.34 |
| $V_{14}$=14V | 5.16 | 5.18 | 5.19 | 5.20 | 5.20 | 5.21 |
| $V_{14}$=16V | 3.97 | 3.99 | 4.00 | 4.01 | 4.02 | 4.03 |

**Table 7.12. The estimated ISM efficiency**

| ISM efficiency [%] | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 88.1 | 87.7 | 87.2 | 87.0 | 86.6 | 86.2 |
| $V_{14}$=14V | 90.7 | 90.5 | 90.1 | 89.9 | 89.6 | 89.2 |
| $V_{14}$=16V | 92.0 | 91.6 | 91.3 | 91.1 | 90.8 | 90.5 |

at nominal operation. It is also expected that as the ISM thermal interface temperature increases, the efficiency will decrease slightly. The decrease is due to the temperature dependence of some of the loss components.

## 5. The spatial and geometric design (based on Chapter 6)

The spatial design and the thermal design of the ISM are highly dependent on each other. In this, the design overview of the ISM prototype, the spatial design is presented before the thermal design because all the geometrical information that is considered in the spatial design is required for the thermal design and analysis. These designs (thermal and spatial) are normally iterative in nature with both the thermal design and volumetric design being adapted to meet the given specifications. However, in this chapter only the final design result is presented.

In this section an overview of the layout as well as a detailed description of the construction of the ISM prototype is presented. The structure has already undergone the iterative thermal design which is presented in section 6.

### 5.1 Layout overview

The preliminary layout of the four-phase bi-directional ISM is illustrated in Figure 7.8. The layout takes advantage of the highly symmetrical configuration of the topology. The layout is configured to have the four phase arms in the centre of the thermal interface, two on either side of the 42V bus bar distributing power to the phase arms. The decoupling capacitors are implemented with the phase arms. The bus capacitors for both terminal voltages are located alongside the phase arms perpendicular to the centre bus bar. The aluminium electrolytic capacitors are located in these structures. The EMI filters are located alongside the capacitor structures with the ISM terminals on the outside of the EMI filter structures. The control system can then be implemented on top of the ISM. The figure shows the different parts of the ISM separated slightly from each other to make the figure clear. In the implemented structure, all the components will be placed tightly alongside each other.

### 5.2 Geometric design

The ISM is implemented on a copper base plate that serves as the thermal interface and that is attached to the infinite heat sink. Figure 7.9 shows the base plate of the ISM measuring 137mm by 187mm by 5mm. The MOSFETs implementing the phase arms together with the ceramic

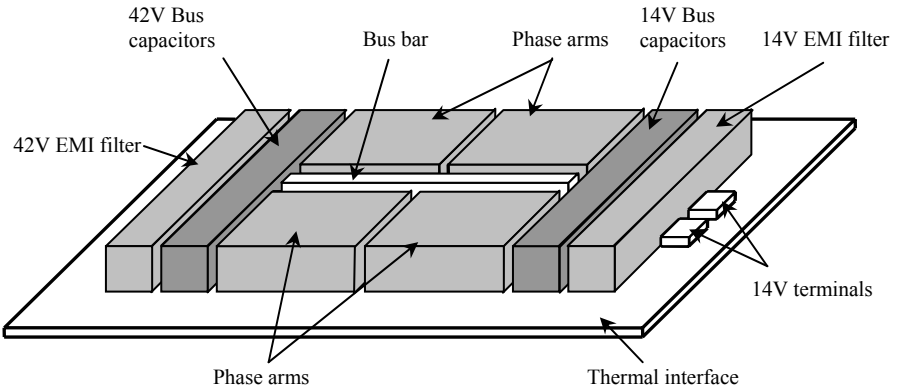


**Figure 7.8. The preliminary layout of the ISM**

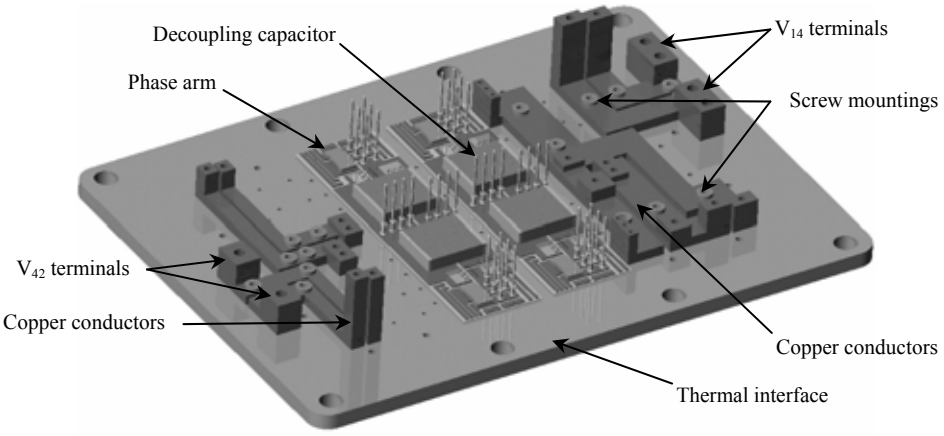


**Figure 7.9. The converter base plate with the DCB and base conductors**

decoupling capacitors are implemented on two separate DBC substrates together with the base copper conductors required to connect the ISM terminals to the EMI filters and to the bus bars. The copper conductors that carry the most current are located on the right of the figure. Due to the large currents and heat dissipated in the conductors, the conductors are mounted on the base plate, isolated by a layer of kapton and kept in place with screws.

Figure 7.10 shows a close up view of the implementation one of the four phases. The figure shows the two MOSFETs forming the phase arm mounted on the DBC substrate together with the wire bonding required to connect the two devices to the circuit. The current measuring shunt and six pins are mounted on the DBC in addition to the ceramic decoupling capacitor. There are an additional eight pins located behind the ceramic capacitor that are required to connect the DBC substrate to the 42V and ground bus bars. Additional connection points are included on the DBC substrate to connect the phase arm to the control circuit.

Figure 7.11 shows the ISM base plate with the three bus bar structures connecting the pins on the DBC substrates to the base copper conductors. The central vertically orientated bus bar is the 42V bus bar with the nearest conductor being the ground conductor. The eight pins located behind the ceramic decoupling capacitor are used to implement the interconnection between

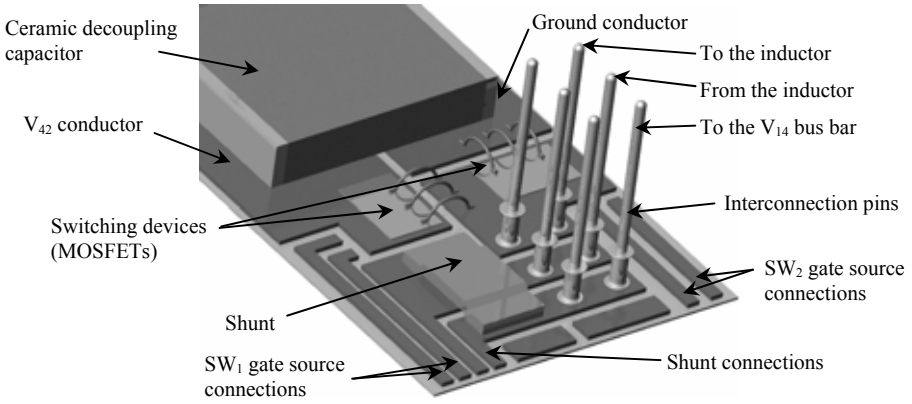


**Figure 7.10. Close up view of one of the four phases showing the switching devices, the decoupling capacitor and the pin structures used to connect to the inductor on the DBC substrate**

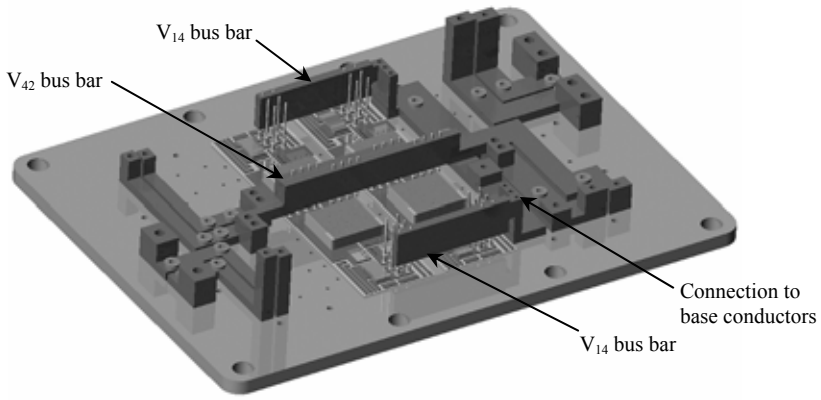


**Figure 7.11. The bus bars mounted over the DCB substrate**

the bus bar and the two DBC substrates. The two outer vertically orientated bus bars, one on either side of the ISM are the 14V bus bars. The current from the two alongside inductors are combined with the 14V bus bars. The electrical connection between the inductor structure and the 14V bus bar is made through the pins mounted on the DBC substrate. All of the bus bars are connected to the base copper conductors with screw interconnections. These are selected to allow the ISM prototype structure to be assembled and disassembled with relative ease.

Figure 7.12 shows the ISM base plate with the two inductor integrated heat sink structures mounted on the thermal interface. An integrated heat sink structures is located on either side of the 42V bus bar. The two integrated heat sink structures each support two inductors with only three heat paths between the heat collectors and the thermal interface. Three heat paths are used instead of four to reduce the surface area the inductors integrated heat sink structure requires on the thermal interface. In the figure, the foremost 14V bus bar has been removed to illustrate the electrical interconnection between the inductor terminals and the DCB substrate.

Figure 7.13 shows a close up view of two of the four inductors without the integrated heat sink structure. The electrical interconnection between the inductors and the DCB is implemented with the aid of the pin structures as illustrated in the figure. The figure also illustrates the second function of the integrated heat sink structure: the integrated heat sink physically holds

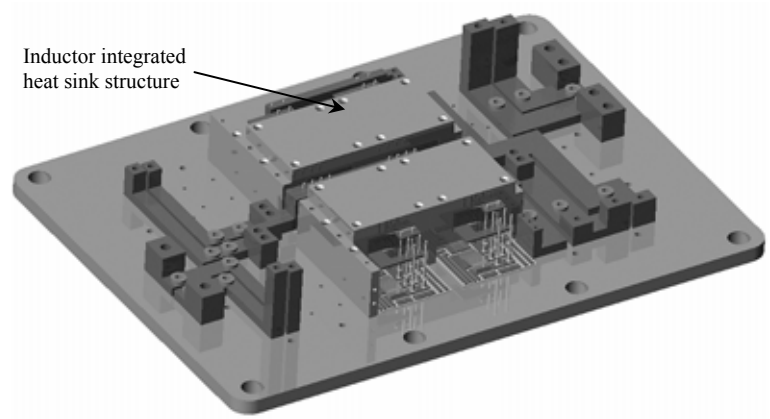


**Figure 7.12. The base plate with the four inductors mounted in two integrated heat sink structures**

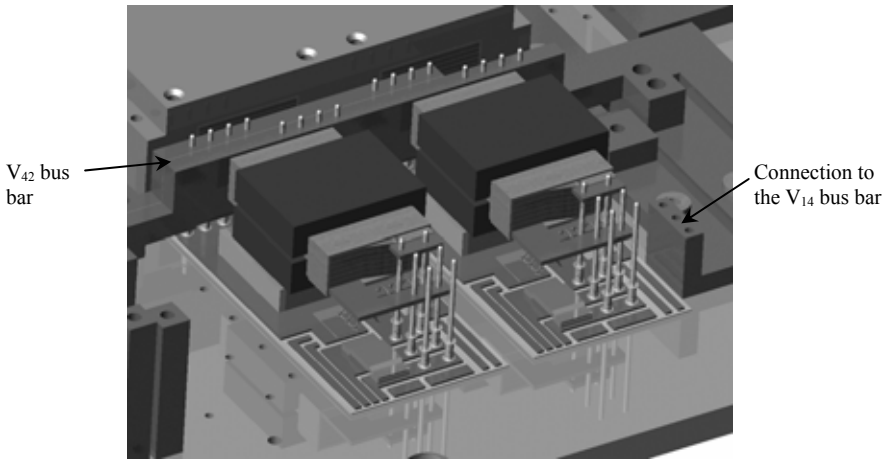


**Figure 7.13. A close up of two of the four inductors mounted without the thermal management structure to illustrate the electrical connection**

the inductors in place. The inductor integrated heat sink structure is also used to remove the heat dissipated in the ceramic decoupling capacitor over which the inductor structure is mounted. This is achieved by dimensioning the heat collector of the inductor integrated heat sink to be such that it is in thermal contact (electrically isolated) with the ceramic capacitor.

Figure 7.14 shows the placement of the two 42V aluminium electrolytic bus capacitors together with their integrated heat sink structures. The two electrolytic capacitors are mounted horizontally and very close to the base of the converter to minimise the thermal resistance between the capacitor and the thermal interface. Very good thermal management external to the capacitor is required due to the poor internal thermal properties of the capacitor. These poor thermal properties are due to the internal construction and material properties of the electrolytic capacitor. Heat is extracted from the electrolytic capacitors both radially and axially to maximise heat extraction.

Figure 7.15 shows a close-up view of one of the 42V electrolytic capacitors. Only one of the three available surfaces is not used to remove heat from the component since the component's electrical connections are implemented on this surface. The electrolytic capacitors are also

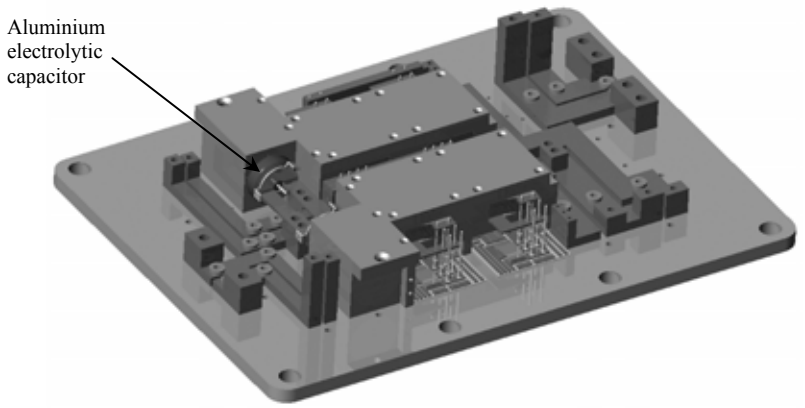


**Figure 7.14. The 42V bus capacitors mounted in their integrated heat sink structures**

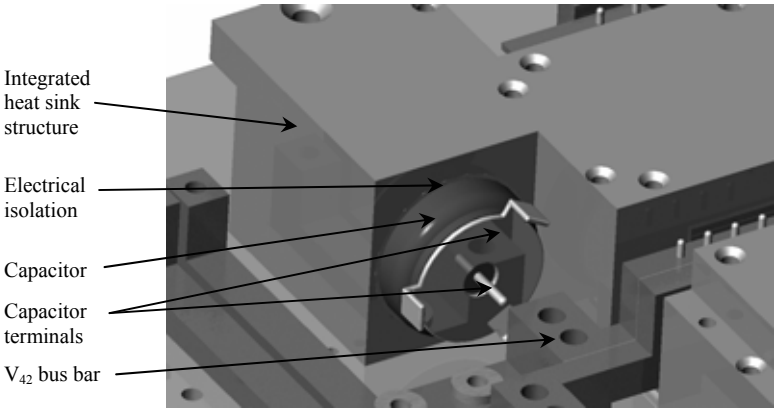


**Figure 7.15. A close up view of the 42V bus capacitor mounted in the integrated heat sink structure**

connected to the 42V and ground bus bar at this point. Making the electrical connection at this point reduces the number of required connections by one because one interconnection connects the bus bar to the capacitors and to the base conductors. It can also be seen that the capacitor is mounted very close to the converter's base. A thermally conductive, electrically isolating material is placed between the component and the integrated heat sink to provide thermal coupling and mechanical stress relief is also identified in the figure. The 14V electrolytic capacitor is implemented in a similar way to the 42V electrolytic capacitors.

The 14V ceramic capacitors together with their integrated heat sink structure are illustrated in Figure 7.16. The figure shows three ceramic capacitors connected in parallel and mounted directly on the base copper conductors. There is no direct heat path for the heat dissipated in the capacitors to escape other than through the high current conductors on which they are mounted. Thus to remove the heat from the capacitors, an integrated heat sink structure is included. The figure shows the heat collector of the integrated heat sink. The heat dissipated in the capacitors is removed through the heat collector placed above and in thermal contact with the capacitors. The heat is conducted up from the capacitors through the integrated heat sink heat collector and then down to the thermal interface through the converter outer wall, which functions as the heat path (not shown in the figure).

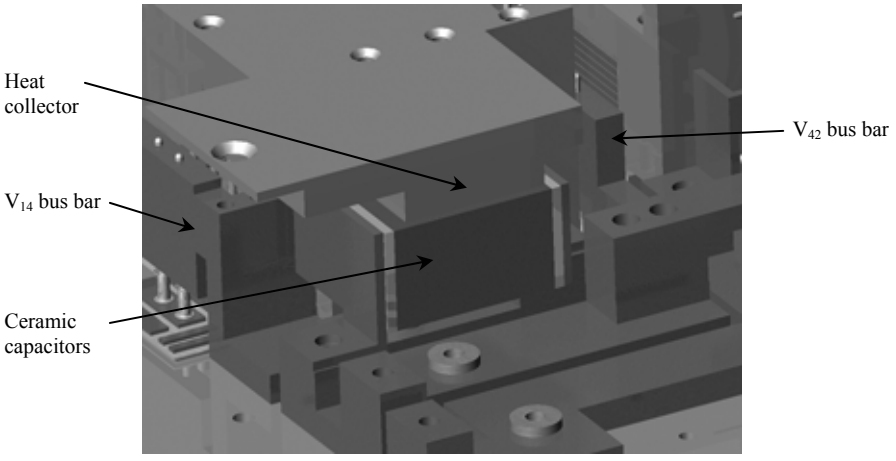


**Figure 7.16. The 14V ceramic capacitors together with their integrated heat sink structure**

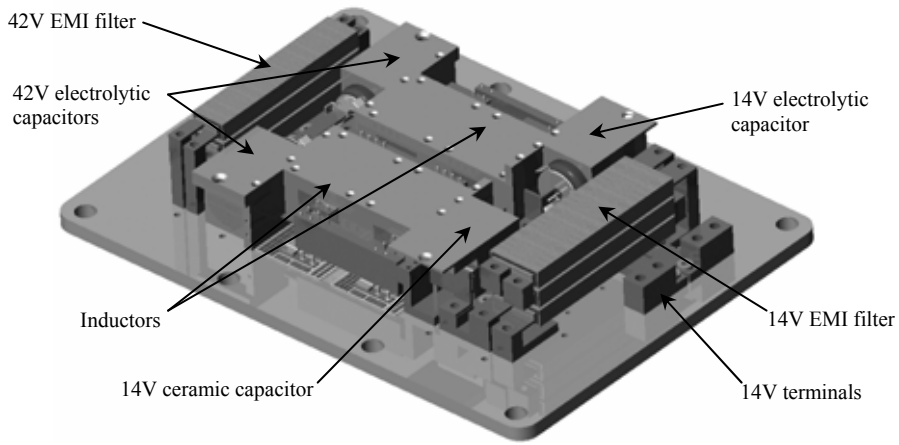


**Figure 7.17. The converter structure with the 42V and 14V EMI filter structures**

Figure 7.17 shows the ISM with all the capacitors and the two EMI filters, without their integrated heat sinks structures. In the figure, the 42V EMI filter is located in the top left corner and the 14V EMI filter in the lower right corner. Both EMI filters are implemented with a series combination of three integrated LC structures. The two EMI filters have different widths to accommodate the different DC current levels.

Figure 7.18 shows the ISM without the gate drives or control circuitry but with the complete integrated heat sink structure in place. By comparing Figure 7.17 and Figure 7.18 it can be seen that the ISM outer walls provide a significant part of the heat path to the thermal interface. The side walls complete the heat path for all of the electrolytic capacitors and the 14V ceramic capacitors. The ISM without the control circuits has a with of 98mm, a length of 145mm and a maximum height of 28mm. In the centre of the converter, at the lowest point, the module is 21mm high.

Figure 7.19 shows the complete ISM with the control circuitry in place. The gate drives are mounted vertically against the inside of converter outer housing and connected directly to the DBC substrates to drive the MOSFETs. The auxiliary power supply used to power the control circuit and gate drives is mounted in the indentation on top of the converter structure. The ISM

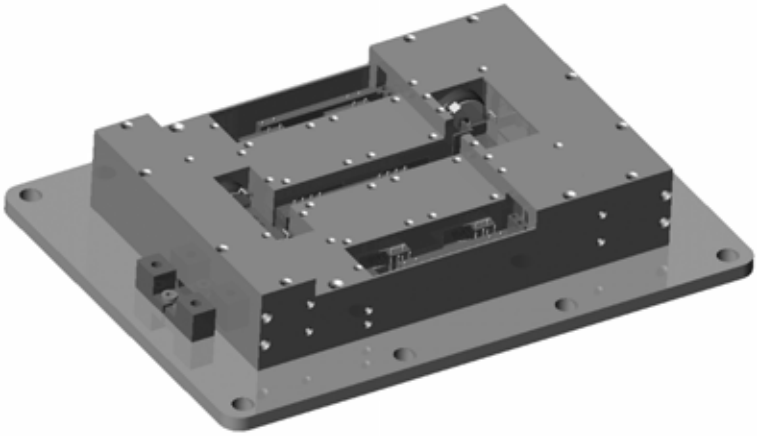

**Figure 7.18. The converter structure with the complete thermal management structure**

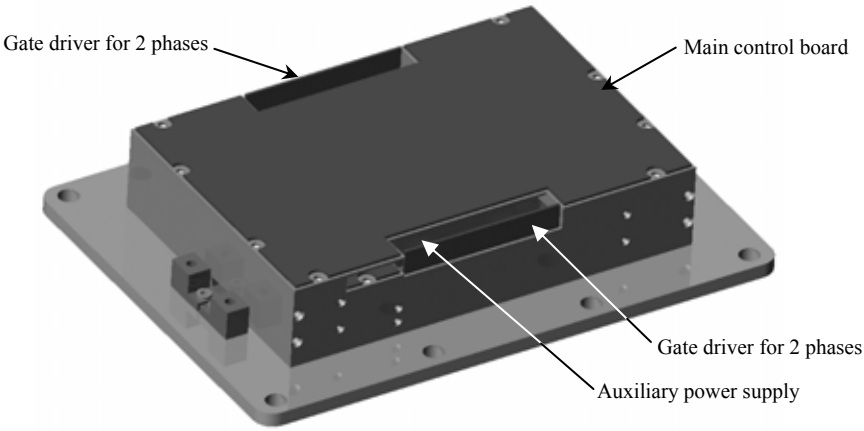


**Figure 7.19. The power converter together with the auxiliary power supply, the control circuit and the gate drivers**

main control circuit is then mounted on top of the converter and auxiliary power supply. The control circuit, the auxiliary power supply and the gate drives are all implemented on high temperature PCBs using high temperature components. The converter control system has a CAN bus interface to communicate with the automotive central control system.

Figure 7.20 shows the integrated system module with all of the integrated heat sink structure removed. The figure shows the high density placement of the components in all three dimensions.

### 5.3 Volume usage

The ISM uses the integrated heat sink structure to reduce the volume of the passive components while providing the necessary heat removal. Several of the techniques presented in Chapter 6 to further reduce the volume of the ISM are also implemented. These techniques

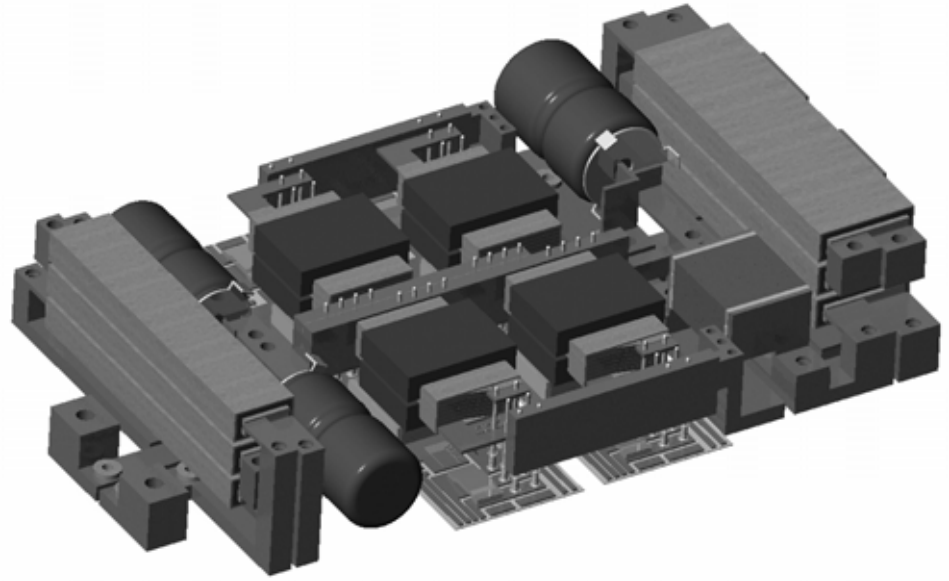

**Figure 7.20. The complete ISM with all of the integrated heat sink structure removed**

**Table 7.13. A summary of the volume distribution in the ISM**

| Component or material | Volume [mm$^3$] | Volume [%] |
|---|---|---|
| Total ISM volume | 350154 | 100 |
| Relative Volume Utilisation | 234835 | 67 |
| | | |
| Single Inductor* | 5714 | 1.63 |
| All the Electrolytic capacitors* | 18832 | 5.37 |
| All the Ceramic capacitors* | 8182 | 2.33 |
| All the EMI filters* | 35988 | 10.2 |
| Complete integrated heat sink | 111112 | 31.7 |

*** component only; excluding the integrated heat sink**

include the following:

- The heat collectors of the inductor structures that are alongside each other share common heat paths to the thermal interface. For the two inductors there are only three heat paths and the cross-sectional area of all three heat paths is the same.
- The outer wall of the ISM is a central part of the complete integrated heat sink structure since it completes the heat paths for almost all of the remaining passive components, the gate drivers and the control circuitry.
- The integrated heat sink provides mechanical support for all of the passive components, making the module physically durable.
- The integrated heat sink allows all of the passive components to be miniaturised by significantly improving the heat removal from the components.

The only technique discussed in Chapter 6 not implemented in the ISM module is the use of the integrated heat sink to provide a hermitically sealed housing for the module.

The volume of the different components is tabulated in Table 7.13. The table shows the total volume occupied by the ISM as well as the volume of all the components within the module. From this, the Relative Volume Utilisation, $\zeta_{relative}$ can be calculated as 67%, which is significantly higher than for conventional construction methods.

For the given volume and a power rating of 2kW, the projected power density of the ISM is just below 6kW/dm$^3$ (100W/in$^3$). The power density does not give any indication that this power density is achieved with a thermal interface temperature of 110°C.

If the EMI filters are neglected, the power density of the ISM can be increased to 8.5kW/dm$^3$ (140W/in$^3$) with the same thermal interface temperature.

## 6. The thermal design (based on Chapter 5)

In this section, the thermal design of the ISM is briefly presented. The geometry of the module is already known. Based on this and the estimated losses calculated in section 4 of this chapter, the temperature distribution in the different components can be calculated. The thermal calculations are primarily performed with ANSYS™, a finite element package. The materials used to implement the different components are also identified in this section where relevant.

### 6.2 Thermal management: Integrated heat sink

It has been seen in the previous section that the integrated heat sink structure is used extensively within the ISM to provide both mechanical integrity and to transport heat very

effectively from the heat source to the thermal interface. In this section the thermal resistance required for the different components is determined. The integrated heat sink must provide a thermal resistance between each component and the thermal interface that is at most equal to the maximum allowed thermal resistance.

### *6.2.1 The required thermal resistance*

Determining the maximum thermal resistance allowed for each component, assuming the components operate at their individual maximum temperature for both the nominal and worst case conditions, gives the upper limit to the thermal resistance that the integrated heat sink must achieve between the component's hot spot and the thermal interface. This calculation is performed for all the components in the ISM module and tabulated in Table 7.14. The table also gives the maximum temperature for the various components. In the table, the nominal load refers to the ISM operating at 2kW and a thermal interface temperature of 85°C with $V_{14}$ = 14V and $V_{42}$ = 42V. The worst case load refers to when then the ISM is operating at 2kW with $V_{14}$ = 11V and $V_{42}$ = 50V. Under these terminal conditions, the losses in all the components are at their highest. The situation can be further compounded if the thermal interface temperature is 110°C.

The thermal resistance for the worst case conditions is smaller for all the components compared to the nominal load and forms the upper limit on the maximum allowed thermal resistance. The table shows that the range in which the required thermal resistances falls is rather extensive – ranging between 1.6°C/W to 1625°C/W.

## 6.3 Thermal simulations

The different components together with their integrated heat sink structures are simulated using the finite element package Ansys™ to determine the temperature distribution within the components to ensure that the maximum component temperature's are not exceeded, under both nominal and worst-case load conditions. These simulations are used in the design process of the integrated heat sink to determine the most suited dimensions and geometries. The final simulation results for the various components are presented in this section to summarise the thermal design.

**Table 7.14. The calculated thermal resistance required for each component for both the worst-case load and nominal load conditions**

| Component | Maximum temperature [°C] | Thermal interface [°C] | Max losses [W] Nom losses [W] | Maximum $R_{t,max}$ [°C/W] Nominal $R_{t,nom}$ [°C/W] |
|---|---|---|---|---|
| MOSFET | 175 | 110 | 39.9 | 1.6 |
| | | 85 | 26.1 | 3.4 |
| Inductor | 280 | 110 | 6.9 | 24.6 |
| | | 85 | 5.7 | 34.8 |
| Electrolytic capacitor | 150 | 110 | 0.06 | 665 |
| | | 85 | 0.04 | 1625 |
| Ceramic capacitor | 160 | 110 | 1.2 | 41.6 |
| | | 85 | 0.5 | 150 |
| 14V EMI filter | 150 | 110 | 14.9 | 2.68 |
| | | 85 | 9.2 | 7 |
| 42V EMI filter | 150 | 110 | 3.8 | 10.5 |
| | | 85 | 1.9 | 34.2 |

**Table 7.15. Material properties for the materials implementing the inductor structure**

| Material | k (W/m·˚C) |
|---|---|
| Copper | 380 |
| Aluminium (Alloy 51ST 6082 ) | 120 |
| Ferrite (N92) | 3.5 |
| Isolation (BondPly, Chomerics) [7-6][7-7] | 0.9 |
| Winding: parallel to winding plane | 325 |
| Winding: perpendicular to winding plane | 4 |

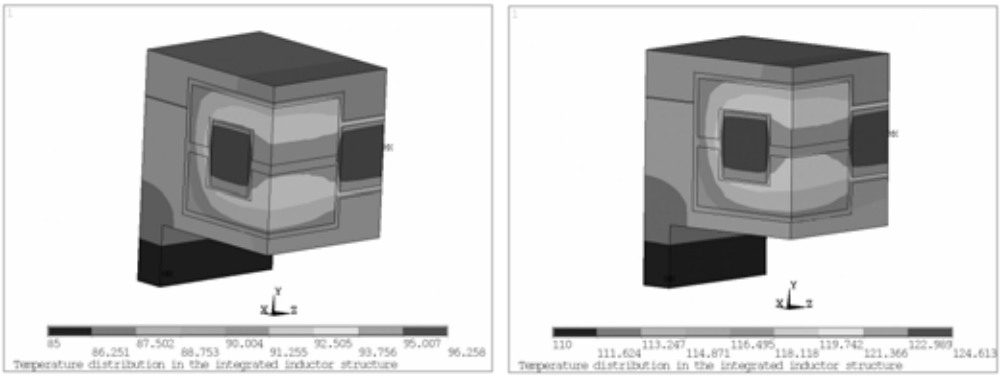


**Figure 7.21. The simulated temperature distribution in the phase arm inductor for nominal conditions (left), and worst-case conditions (right)**

### *6.3.1 The phase arm inductors*

The phase arm inductors are implemented with the same inductor geometry and materials as the inductor presented in Chapter 5. The only difference between the two inductor and integrated heat sink structures is that the integrated heat sink structure in the ISM supports two inductors alongside each other as illustrated in Figure 7.12.

The properties of the various materials used in the implementation of the inductor and integrated heat sink structure are tabulated in Table 7.15, which shows the materials' thermal conductivities. The thermal simulation for the nominal and worst-case conditions as tabulated in Table 7.14 is plotted in Figure 7.21 on the left and on the right of the figure respectively. For nominal operation, a temperature rise of approximately 11.3°C resulting in a maximum temperature of approximately 96.3°C is expected. For the worst-case conditions a maximum temperature of approximately 124.6°C is expected which corresponds to a temperature rise of about 14.6°C above a thermal interface temperature of 110˚C.

The low maximum temperature relative to the maximum allowable temperature of the inductor structure is an indication that the integrated heat sink is over-designed. The thermal resistance achieved by the integrated heat sink is approximately 2.1°C/W.

### *6.3.3 The decoupling capacitors*

Of the ceramic capacitors, the thermal model of only one of the 42V ceramic decoupling capacitors is presented.

Figure 7.22 shows a cross-section of the 42V ceramic decoupling capacitor mounted on the DBC beneath the phase arm inductor integrated heat sink. The capacitor is in thermal contact

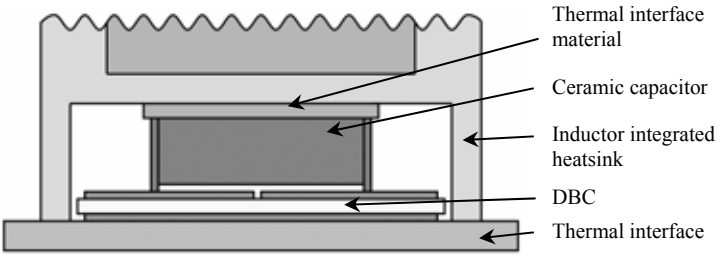


**Figure 7.22. Front view of the 42V ceramic decoupling capacitor mounted on the DBC below the inductor integrated heat sink**

with the underside of the integrated heat sink through a thermal interfacing material that is electrically isolating while being thermally conductive and is manufactured by Chomerics™ [7-7]. The heat in the component is transported through the integrated heat sink as well as through the DBC to the thermal interface. The thermal properties of the materials used to implement this structure are tabulated in Table 7.16.

To thermally model the structure, a 3D model is used to determine the temperature distribution for both the nominal and the worst-case load conditions. Using symmetry through the centre of the structure, only half of the capacitor and integrated heat sink structure is required for the simulation. A 3D model is used to include the effect of the large overhanging integrated heat sink directly above the capacitor.

**Table 7.16. Material properties for the materials implementing the 42V ceramic decoupling capacitor structure**

| Material | Thermal conductivity (W/m·°C) |
|---|---|
| Air | 0.03 |
| Thermal interface material | 0.9 |
| Ceramic capacitor [7-8][7-9] | 2.5 |
| Capacitor metallization | 10 |
| DBC ceramic substrate | 24 |
| Solder | 44 |
| Copper | 385 |
| Aluminium (Alloy 51ST 6082 ) | 120 |

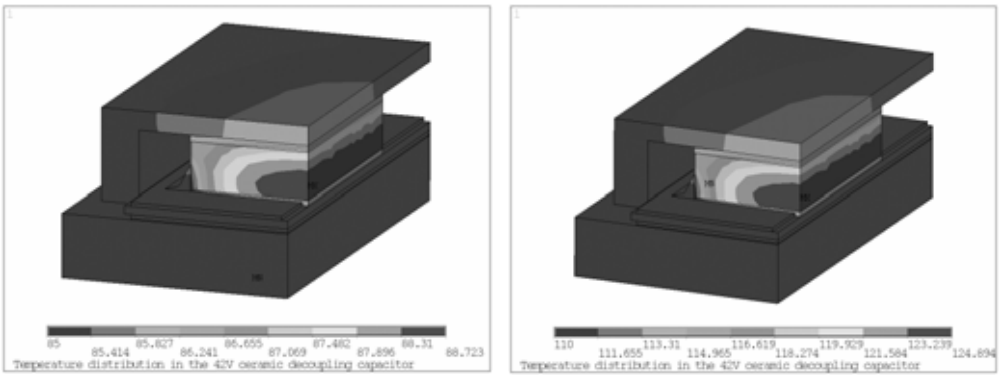


**Figure 7.23. The simulated temperature distribution in the 42V ceramic decoupling capacitor for nominal conditions (left), and worst-case conditions (right)**

The result of the thermal simulation for the nominal and the worst-case load conditions is plotted in Figure 7.23 on the left and right respectively. Under nominal load conditions, approximately 0.5W is dissipated in the capacitor resulting in a maximum temperature of just below 89°C, which corresponds to a temperature-rise of less than 4°C. Under the worst case load conditions, the temperature rise is approximately 15°C, with a maximum temperature just below 125°C for 1.2W loss. The resultant thermal resistance achieved for the capacitors is 12.5°C/W. The high thermal resistance is due to the low thermal resistance of the ceramic capacitor. It must also be noted that the model ignores any heating in the capacitor due to the losses dissipated in the inductor structure. This assumption is justifiable by noting that the thermal conductivity of the aluminium used to implement the integrated heat sink is very large compared to the thermal conductivity of the ceramic capacitor. The heat entering the integrated heat sink from the inductor will flow to the thermal interface through the heat paths and not the ceramic capacitor.

### *6.3.4 The MOSFETs*

The semi-conductors are implemented with open die devices on a DBC substrate as illustrated in Figure 7.10. A cross-section through the semi-conductor assembly is illustrated in Figure 7.24, which shows the various materials between the semi-conductors and the infinite heat sink. All of the layers are identified in the figure. The thermal properties and the thickness of the different materials are tabulated in Table 7.17.

The temperature distribution in the two MOSFETs per phase is determined with a two dimensional thermal simulation based on the material properties and dimensions in Table 7.17. The simulated temperature distribution in the semi-conductor structure for nominal and worst-case load conditions are illustrated in Figure 7.25 on the left and right of the figure respectively. In the simulation, the MOSFET on the left of the figure is $SW_1$ in Figure 7.2, and on the right is $SW_2$ in the same figure.

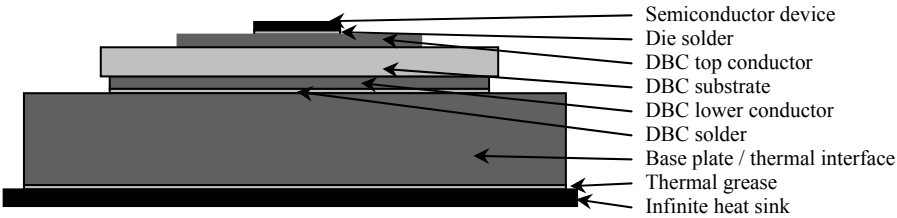


**Figure 7.24. A cross-section through the semi-conductor material stack**

**Table 7.17. Properties of the materials implementing the semi-conductor switching device structure**

| Layer description | Approximate thickness (μm) | Thermal conductivity (W/m·°C) |
|---|---|---|
| Active Device | ≈200 | 140 |
| Die Solder Layer | 60 | 44 |
| DBC Top Copper Layer | 300 | 385 |
| DBC Ceramic Layer | 635 | 24 |
| DBC Bottom Copper Layer | 300 | 385 |
| Substrate Solder Layer | 100 | 44 |
| Thermal interface | 5000 | 385 |
| Thermal Grease | ≈100 | 0.9 |

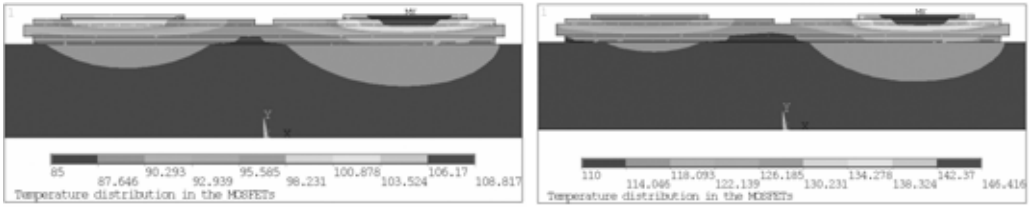


**Figure 7.25. The simulated temperature distribution in the semi-conductor devices for nominal conditions (left), and worst-case conditions (right)**

The simulations show that under nominal conditions, the maximum temperature rise in the MOSFETs is in $SW_2$ with a temperature rise of approximately 24°C, resulting in a maximum temperature of just under 109°C for 26.1W loss. The temperature rise for the worst-case load condition is approximately 37°C, resulting in a maximum temperature of just over 146°C for 39.9W loss. These temperatures are still well within the device maximum temperature of 175°C.

A thermal resistance to the environment of 0.9°C/W is expected for the switching devices.

### *6.3.5 The EMI filters*

Both the 14V and 42V EMI filters are implemented with a series combination of three planar filter structures as illustrated in Figure 7.26. The filter structure consists of two conductors placed parallel to each other but separated by a layer of ceramic. The ceramic and copper sandwich is then enclosed in a ferrite ring that is electrically isolated from the conductors with a compressible thermally conductive material [7-7]. The filter structure is then placed in the integrated heat sink structure that mounts the three filter structures above each other, again electrically isolated with the compressible thermally conductive material.

The materials for the filter structures are chosen so that the filter functions primarily as a common mode filter. The filters are considered further in the following chapter.

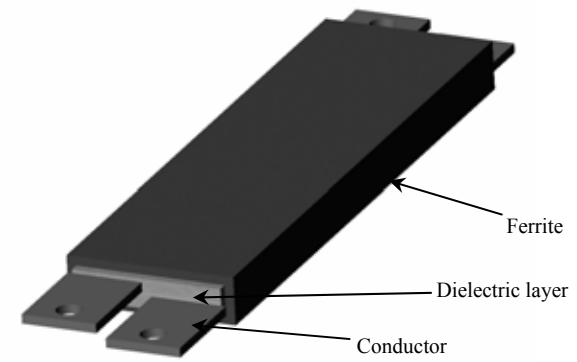


**Figure 7.26. One of the three 14V planar EMI filter structures**

**Table 7.18. Material properties for the materials implementing the planar EMI filter structure**

| Material | Thermal conductivity (W/m·°C) |
|---|---|
| Thermal interface material | 0.9 |
| Ceramic capacitor [7-8][7-9] | 2.5 |
| Copper | 385 |
| Aluminium (Alloy 51ST 6082 ) | 120 |
| Ferrite (3E27) | 5 |

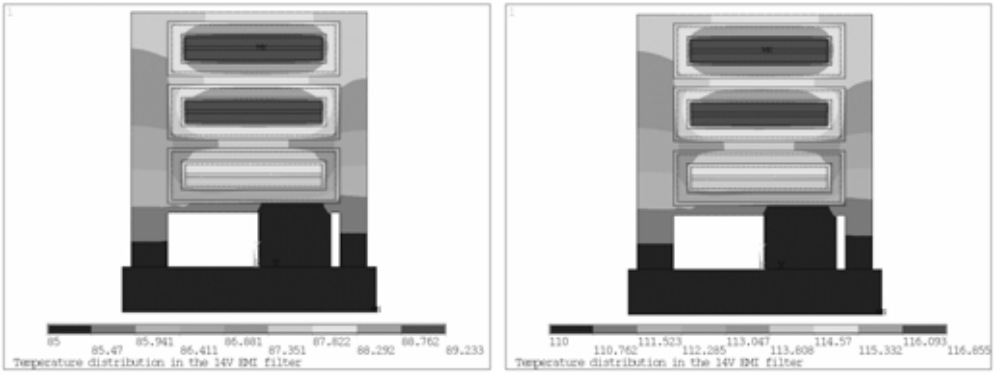


**Figure 7.27. The simulated temperature distribution in the EMI filter structure for nominal conditions (left), and worst-case conditions (right)**

The thermal properties of the materials used to implement the EMI filter structures are tabulated in Table 7.18.

Only the 14V EMI filter simulation is presented because the losses in this structure are significantly higher than those in the 42V filter due to the larger DC current. The temperature distribution of the EMI filter structure is simulated with a 2D model for both the nominal and the worst case load and the results are plotted in Figure 7.27 on the left and right respectively. The figure shows the three planar EMI filter structures mounted above each other in the integrated heat sink structure. There are three heat paths between the heat collectors and the thermal interface. Three heat paths are used to avoid overheating in the filter structures.

The simulations show that under nominal load conditions, approximately 9.2W is dissipated in the six copper conductors resulting in a temperature rise of just over 4°C, which corresponds to a maximum temperature in the structure of just over 89°C. Under the worst-case load conditions, the maximum temperature is just under 7°C above the thermal interface temperature of 110°C due to 14.9W of dissipated heat. The integrated heat sink structure realises a thermal resistance of 0.46°C/W for the $V_{14}$ EMI filter.

## 6.4. Realised thermal resistance

The realised thermal resistance for the four components presented in the previous section

**Table 7.19. Summary of the maximum allowable and realised thermal resistance together with the maximum temperature for the worst-case and nominal load conditions**

| Component | Maximum thermal resistance Worst / Nom [°C/W] | Implemented thermal resistance Worst / Nom [°C/W] | Losses Worst / Nom [W] | Maximum temperature Worst / Nom [°C] |
|---|---|---|---|---|
| MOSFET | 1.6 | 0.9 | 39.9 | 146.4 |
| | 3.4 | 0.9 | 26.1 | 108.8 |
| Inductor | 24.6 | 2.1 | 6.9 | 124.6 |
| | 34.8 | 2.1 | 5.7 | 96.3 |
| Ceramic capacitor | 41.6 | 12.5 | 1.2 | 124.9 |
| | 150 | 12.5 | 0.5 | 88.7 |
| 14V EMI filter | 2.68 | 0.46 | 14.9 | 116.8 |
| | 7 | 0.46 | 9.2 | 89.2 |

together with the maximum temperature in the component under nominal and worst-case load conditions is summarised in Table 7.19. The table also lists the maximum allowable thermal resistance for the various components. In all cases, the realised thermal resistance is at least an order smaller than that which is required.

## 7. Summary

This chapter presented an overview of the interdependent design of the automotive ISM prototype based on the work presented in the previous four chapters. The ISM is designed to a given set of specifications requiring a high power density module capable of operating with thermal interface temperatures of up to 110°C at full rating.

The overview of the ISM design is divided into thee sections. The first considers the electrical design, the second considers the spatial design and the last the thermal design. The three designs are presented in this order to simplify the design overview.

The electrical design considers the current and energy in the passive components to determine the optimum number of phases and the component parameters. The first component parameter that is determined is the phase arm inductance. It is seen that a small phase arm inductance can be used without significantly affecting the RMS current in the bus capacitors once a minimum inductance value is exceeded, as illustrated in Figure 7.3. A phase arm inductance of 3.8µH is selected. With the phase arm inductance fixed, determining the RMS current and stored energy as a function of the number of phases and duty cycle is possible. These are then used to determine the optimum number of phases. For the given specifications and phase arm inductance, the optimum number of phases is four. The remaining component parameters can then be determined.

Once the component parameters are known, preliminary components required to implement the topology can be identified. These components are selected primarily for their high temperature capability. With the components identified, the losses in the components can be estimated. The estimated losses are summarised in the chapter with the loss calculations presented in the appendixes.

Once all the components are identified, the result of the spatial design is presented. The spatial design uses the integrated heat sink concept presented in Chapter 5 to mount the components in the ISM as well as to remove the heat from the components. The ISM has a power density of approximately 6kW/dm$^3$ (100W/in$^3$) with a thermal interface temperature of 110°C. In addition, the ISM has a Relative Volume Utilisation of 67%. This value of the Relative Volume Utilisation is significantly higher than conventional converters of similar ratings.

Once the ISM geometry is known, an overview of the thermal design results is presented. The integrated heat sink concept is used to implement all the passive components in the ISM. The maximum thermal resistance that the integrated heat sink structure must achieve is identified. To evaluate the thermal design, thermal simulations are used. The results of the thermal simulations for four of the components are presented in the chapter.

The achieved thermal resistance can be determined for each component from the simulations. These values of the thermal resistance can then be compared to the maximum allowed thermal resistance. For all the components presented, the achieved thermal resistance is an order or more smaller than the maximum allowed thermal resistance. This means that all the

components will operate well within their maximum temperature ratings, but it is also an indication that the integrated heat sink structure is over-designed. An over-designed integrated heat sink structure occupies more volume that what is necessary for the components to operate within their allowed maximum temperature. The power density can be increased by further reducing the volume of the integrated heat sink.

## 8. References


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# Chapter 8

## EXPERIMENTAL EVALUATION OF THE AUTOMOTIVE ISM

## 1. Introduction

The automotive integrated system module presented in the previous chapter is built and experimentally evaluated in this chapter. The ISM is designed for a maximum output power of 2kW with a thermal interface temperature of up to 110°C and a de-rated output power of 1kW with a thermal interface temperature of up to 125°C. The theoretical power density of the module, including all passive components and EMI filters, is 6kW/dm$^3$ (100W/in$^3$).

The realisation of the experimental structure is presented first in the following section. A photographic record of the construction and implementation of the module is presented and discussed. The implementation of the EMI filters is also presented.

The ISM is experimentally evaluated in sections 3 and 4. Measured waveforms and the operating efficiency for different thermal interface temperatures are presented and discussed in section 3. The thermal measurements performed on the module under full electrical and thermal excitation are presented in section 4.

The achieved power density is discussed in section 5 and section 6 discusses some identified implementation issues.

## 2. Realisation of the experimental automotive ISM

The physical implementation of the converter structure is presented and discussed. The topology implemented is that in Figure 7.7 of Chapter 7.

### 2.1 Realisation of the module

Figure 8.1a shows the converter base (thermal interface) with two DBC substrates soldered to it. There are two phase arms implemented on each of the DBC substrates. The ceramic decoupling capacitors, the switching devices, the shunts and the connection pins are identified in the figure. The connection pins are used to connect the DBC conductors to the copper conductors that are located above the DBC substrate. Several wires can also be seen on either side of the DBC substrates. These wires provide the electrical connection between the DBC substrate and the converter control system.

Figure 8.1b shows the converter base (thermal interface) with the base copper conductors and the base of the integrated heat sinks for the three electrolytic capacitors. The copper conductors mounted on the base plate are electrically isolated from the base plate with a layer of high temperature kapton material, which has a high electrical breakdown voltage. The layer of kapton is also very thin, in the order of 100μm, thereby minimizing the additional thermal resistance being placed between the conductors and base plate. The capacitor mountings are

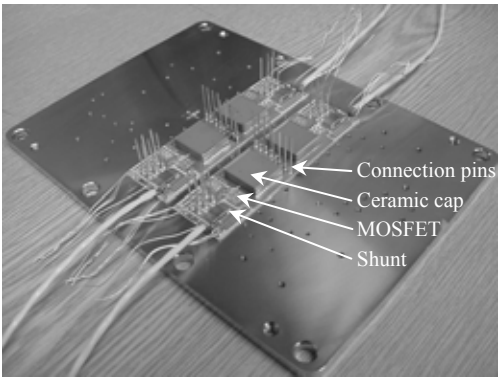



**Figure 8.1a. The converter base (thermal interface) with the two DCB substrates together with the connection pins**

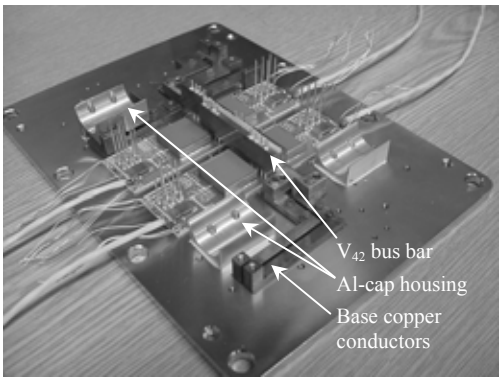



**Figure 8.1b. The converter base with the copper conductors and part of the three electrolytic capacitor thermal management structures**

mounted on the base plate with a thin layer of thermal grease to minimise the interface thermal resistance and fixed in place with small screws.

In Figure 8.1b the main $V_{42}$ bus bar connecting the base copper conductors to the DBC conductors is identified. The connection between the bus bar and the DBC conductors is achieved with the pins mounted on the DBC. The pins pass through holes in the bus bar conductors. Under normal circumstances, the connection would be fixed with a solder or wielding process. However, in the experimental converter, the electrical connection between the pins and the bus bar is made with a silver loaded conductive paste. To ensure a good electrical connection, the holes in the bus bar conductor are filled with the silver-loaded paste before the pins are inserted into the holes. The silver-loaded paste is then allowed to set. This gives the freedom of being able to easily construct and dismantle the module as required.

Figure 8.2a shows the converter thermal interface with the four inductors mounted in the integrated heat sink structures and electrically connected to the phase arms. Each of the two inductor structure houses two inductors. The connection between the inductors and the DBC conductors is made with pins that are soldered to the inductor conductors. A solder connection is used because the available connection area between the pins and the inductor conductors is relatively easy to access and the contact area is smaller.

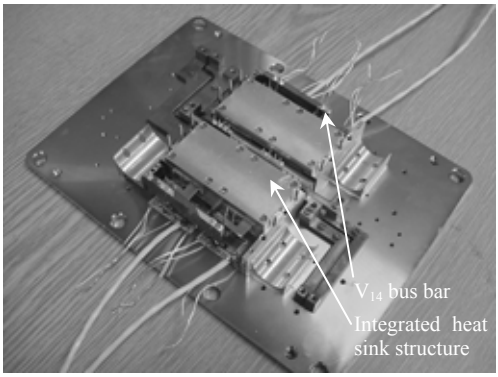



**Figure 8.2a. The converter base with the two inductor structures mounted**

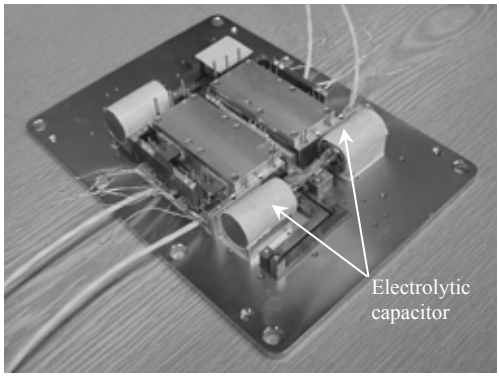



**Figure 8.2b. The converter base with the three electrolytic capacitors and the 14V ceramic capacitors mounted**

The inductor integrated heat sink structures are also used to conduct heat away from the ceramic capacitors shown in Figure 8.1b. To prevent an electrical short circuit, a layer of kapton is placed on the underside of the inductor integrated heat sink structure. Then to minimize the thermal resistance between the ceramic capacitors and the inductor integrated heat sink structure, a layer of Chomerics™ compressible thermal interfacing material is used. As the integrated heat sink structure is mounted above the capacitor structure and fixed in place, the thermal interface material between the inductor structure and the capacitor is placed under pressure thereby reducing the interface thermal resistance.

Figure 8.2a also shows the two 14V bus bars on either side of the two inductor integrated heat sink structures. The electrical connection between the two 14V bus bars and the DBC are made in the same way as with the bus bar illustrated in Figure 8.1b, with pins and silver-loaded paste. The 14V bus bars are connected to the base copper conductors with three screws each.

Figure 8.2b shows the thermal interface of the ISM with the three electrolytic capacitors and the 14V ceramic capacitors mounted. The three electrolytic capacitors all have a layer of kapton around the capacitors covering the entire surface apart from the face with the electrical connections. The kapton is required to maintain electrical isolation. A layer of thermal interface material is also placed around the capacitors. The thermal interface material reduces the interface thermal resistance and also compensates for the thermal expansion between the different materials. The thermal interface material is also placed on top of the 14V ceramic capacitors.

The electrical connection between the electrolytic capacitors and the base conductors is made at the point where the 42V bus bar connects to the base conductors. This reduces the number of necessary interconnections. The connection itself is made with a litz wire isolated with high temperature silicon isolation.

Figure 8.3a shows the ISM base with the top part of the electrolytic and ceramic capacitor integrated heat sink structures in place. All four of these integrated heat sink structures are physically attached to the inductor integrated heat sink structure to minimise the number of heat paths required. Figure 8.3b shows the ISM structure with the two sidewalls included. The top of the inductor integrated heat sink structure and the sidewalls complete the thermal management structure for the electrolytic and 14V ceramic capacitors. The sidewalls function as heat paths for all of the passive components except for the inductors. The heat dissipated in

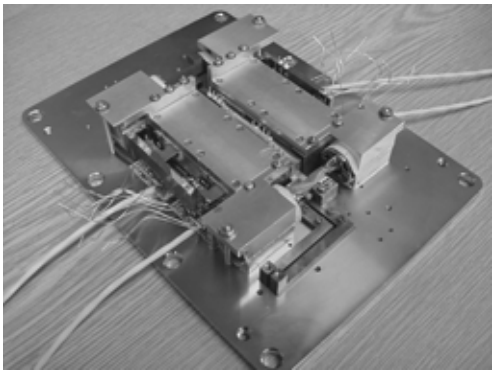


**Figure 8.3a. The converter base with the remainder of the capacitor heat collector structures mounted**

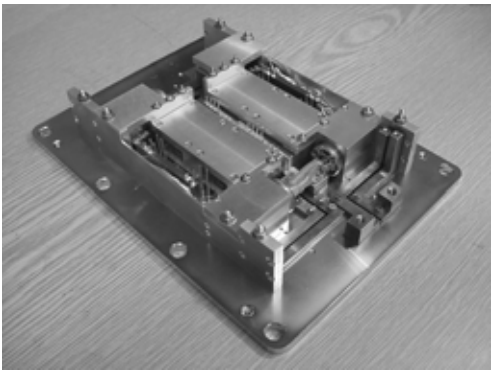


**Figure 8.3b. The converter base with the converter walls mounted completing the capacitor thermal management structure**

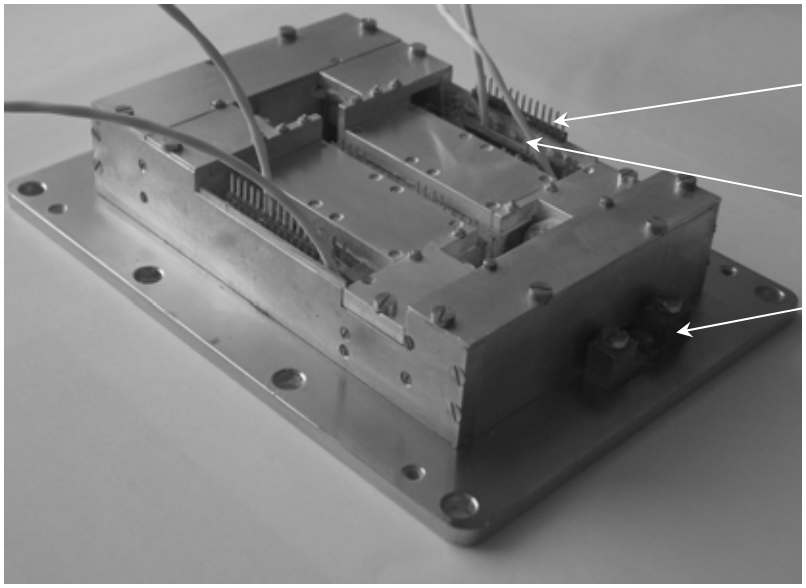



**Figure 8.4. The complete automotive ISM (without auxiliary power supply and control circuit)**

the electrolytic capacitors is removed radially and axially into the surrounding integrated heat sink structure and conducted down to the thermal interface.

The complete automotive ISM without the auxiliary power supply and control circuit is illustrated in Figure 8.4. For the purpose of the experimental evaluation, the auxiliary power supply and the control circuit are kept separate from the power module to maintain measurement accessibility.

The figure shows the ISM module complete with the both the 14V and the 42V EMI filter structures in place. The EMI filters are also implemented in integrated heat sink structures. The connection to the integrated gate drivers is identified in the figure as well as the connection between the control and the current measuring shunt.

## 2.2 Realisation of the EMI filters

The EMI filters are implemented with integrated LC structures. The internal parts of these filters are illustrated in Figure 8.5. Figure 8.5a shows one of the three conductors forming the 14V filter with ceramic tiles placed on the conductor. The ceramic tiles are used to implement the desired capacitance between the two conductors. Multiple small tiles are used instead of one large tile to avoid the tiles breaking due to uneven surfaces or thermal expansion. Each ceramic tile used to implement the 14V filter is rated for 500V and has a capacitance of 8nF. The twenty tiles results in a capacitance of just under 160nF.

The tiles are attached to the copper conductor with a very small amount of conductive silver paste. Conductive paste is used instead of an adhesive to allow a small degree of relative movement between the tiles and the conductors to alleviate any stresses between the different parts. Once the second copper conductor is placed in the filter, also connected to the ceramic tiles with the conductive paste, the conductors are wrapped in a thermally conductive adhesive tape. The tape keeps the conductors in place relative to each other and ensures that the ceramic tiles cannot move out from between the conductors. This is illustrated in Figure 8.5b. Figure

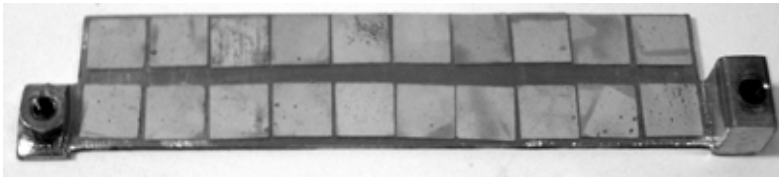


**Figure 8.5a. The ceramic tiles placed between the two copper conductors forming the dielectric layer (14V filter – high current)**

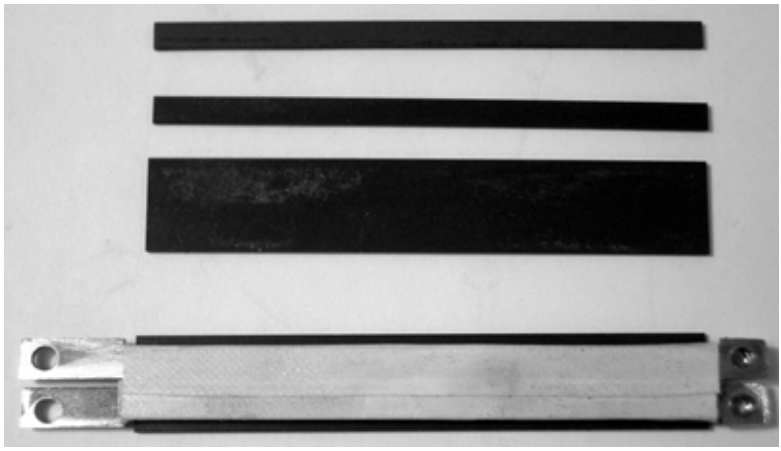


**Figure 8.5b. The conductors with the ceramic tiles isolated with thermally conductive material and the ferrite tiles that enclose the conductors**

8.5b shows the ceramic tiles sandwiched between the copper conductors placed on one of the ferrite tiles that makes up the ferrite encasing. The combined conductors and ferrite ring are then implemented in an integrated heat sink in the ISM in series with two more filter structures that makes up the complete EMI filter. Both the 42V and the 14V EMI filters are implemented with this structure.

The EMI filter primarily functions as a common mode filter due to the ferrite ring and long length. However, there is a small amount of leakage inductance that together with the high capacitance between the conductors implement a differential mode filter. Impedance measurements for the EMI filters are presented in the following section.

## 3. Experimental evaluation

To evaluate the performance of the automotive ISM, several parameters of the module are measured under a variety of operating conditions. In this section the experimental work performed on the ISM is presented.

The experimental setup is presented first. Using the experimental setup, the ISM efficiency is measured for a variety of loads and thermal interface temperatures. Measured waveforms are also presented.

### 3.1 Experimental setup

The experimental setup used to evaluate the ISM's electrical and thermal performance is shown in Figure 8.6. The figure shows the ISM mounted on an infinite heat sink with the additional circuitry required for the module to function. The infinite heat sink can maintain a

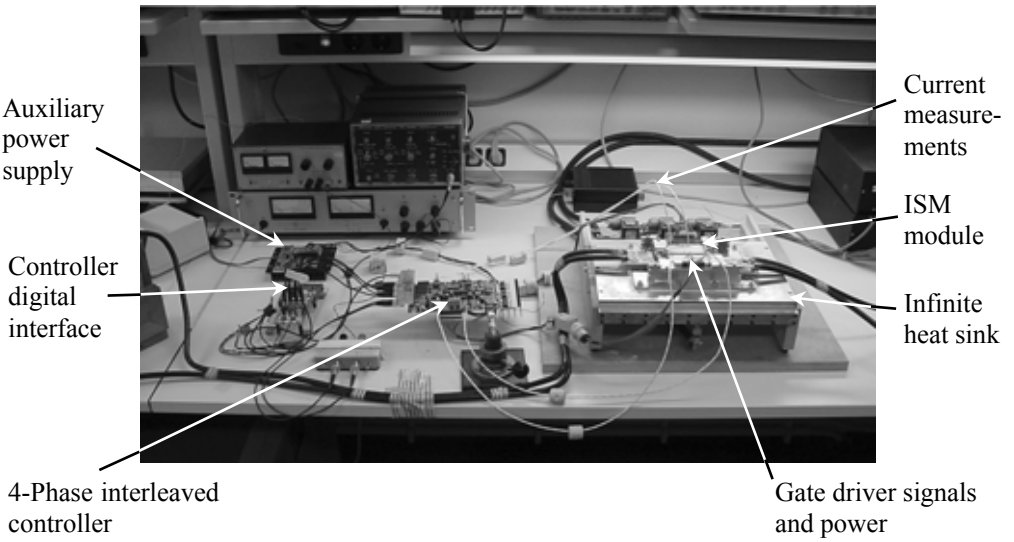



**Figure 8.6. The experimental setup used to determine the ISM efficiency**

constant thermal interface temperature irrespective of the amount of heat being dissipated in it (within the heat sink's limits). The infinite heat sink is actively controlled. The ISM's control system is shown on the left side of the figure.

The control system consists of the four-phase interleaved controller, the controller auxiliary power supply and the digital interface. The four-phase interleaved controller provides the current mode control for the four phases. The current is measured with the aid of a shunt in the inductor current path. This signal is used to maintain the current in the converter at the value specified by the digital interface. In the figure, long wires are used to measure the very small feedback signal. This works only if the measurement cable is a twisted pair, is shielded and the shield is grounded at a single common point. Under this condition the feedback signal is less sensitive to the surrounding electromagnetic noise. The auxiliary power supply is used to provide the ISM control system with the different isolated voltage levels required. Isolated voltages are required to help improve the systems noise immunity. The auxiliary power supply is supplied from the $V_{14}$ terminals and requires a voltage between 8V and 16V.

Under normal operating conditions, the converter control system is very close to the converter module and the long wires between the control system and the converter system are very short. However, in the experimental setup the converter temperatures must be measured. Thus the system is assembled in a more open fashion. However, since the complete system is more open, it is also sensitive to surrounding noise. This problem is handled with the common mode filters that can be seen in the figure. Some of the common mode filters are already implemented in the converter control design but are insufficient for the open layout. These filters will be removed once the control is integrated into the integrated system module.

### 3.2 Efficiency as a function of the thermal interface temperature

The ISM efficiency as a function of the output power and the thermal interface temperature is measured as a performance indicator of the module. The measured efficiency for the module operating over the complete power range with $V_{14}$ = 14V and $V_{42}$ = 42V is plotted in Figure 8.7 for the module operating in buck mode over the full thermal range.

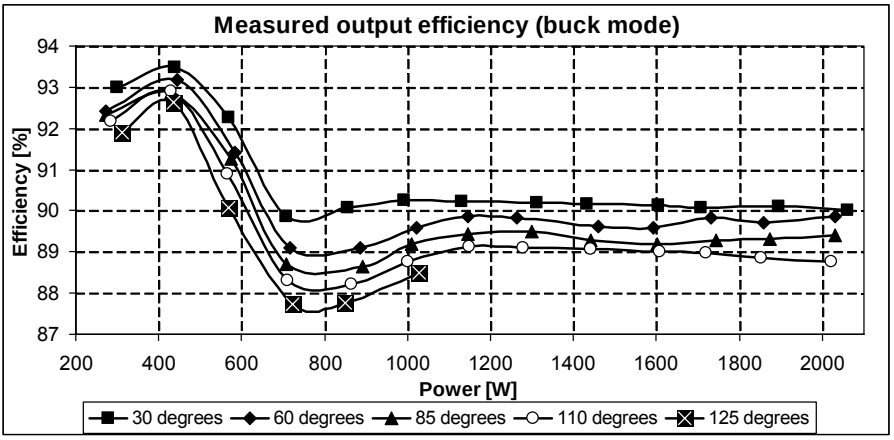



**Figure 8.7. The measured ISM efficiency for $V_{14}$ = 14V, $V_{42}$ = 42V, buck mode**

The measured efficiency shows that for a thermal interface temperature of 30°C and at full electrical load, the efficiency is just over 90%. As the thermal interface temperature increases, the efficiency over the full power range decreases. The module efficiency for a thermal interface temperature of 85°C and at full electrical load is approximately 89.5%, while it decreases to just under 89% as the thermal interface temperature increases to 110˚C. Over the measured temperature range (30˚C to 110˚C) the efficiency drops by approximately 1%, which corresponds to an increase in the measured losses of 20W.

The measured efficiency for a thermal interface temperature of 125˚C with a de-rated output power of 1kW, for the same operating conditions, is approximately 88.5%.

The measured results also show that there is a large drop in the efficiency at around 500W where the efficiency decreases from around 95% to just below 90% for a thermal interface temperature of 30°C. The large drop in the efficiency is due to the reverse recovery in the freewheeling diodes.

For an output power of less than 500W, the four phases operate with inductor currents that become negative during each switching period – ZCCM. If the inductor current becomes negative, then the diode $D_2$ does not conduct just before $SW_1$ is turned on in buck mode. Thus the freewheeling diode does not experience reverse recover losses and there is no reverse recovery current to flow through $SW_1$. However, as the output power increases, the average inductor current increases and a point is reached where the inductor current is no longer negative during the switching period – CCM. When this happens, the freewheeling diode starts to experience reverse recovery increasing the diode losses. The reverse recovery current also flows through $SW_1$ increasing the device's switching losses significantly. Thus, as the phases start experiencing reverse recovery, the losses in the switching devices increase significantly.

### 3.3 Measured waveforms

To verify the operation of the ISM, several electrical measurements are made. The most critical of these measurements include the phase arm currents and the voltage ripple at the terminals of the module. These are presented in this section.

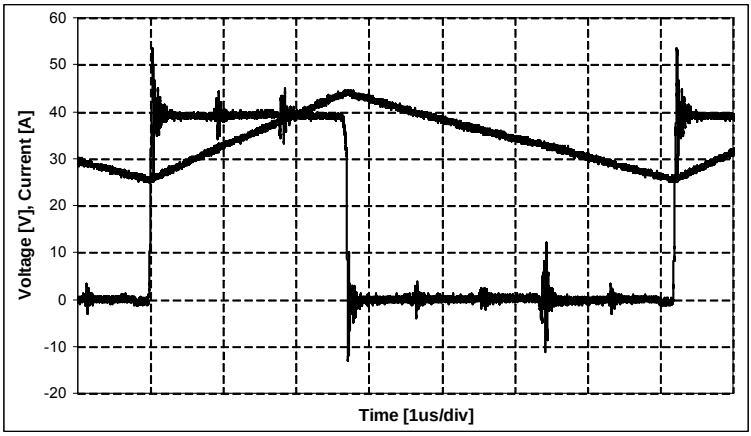



**Figure 8.8. The measured inductor current and the drain source voltage over $SW_2$ for full electrical load**

### *3.3.1 Phase arm measurements*

The voltage measured over the drain source of $SW_2$, the lower device in the phase arm and the inductor current measured with a current probe in the same phase is illustrated in Figure 8.8. The measurement is taken for the module operating at full electrical load in buck mode ($I_{14}$ = $I_{load}$ = 140A, $V_{14}$ = 14V) and with a thermal interface temperature of 30°C

The voltage measurement is noisy. The noise on the measurement is primarily due to the large measurement loop created when measuring the waveform. The large measurement loop is a consequence of the highly integrated nature of the module, which makes it difficult to access the optimum measurement points. It is physically not possible to place the measurement probe very close to the device, and this results in the measurement being more susceptible to noise. The noise bursts occur at the time of switching in the remaining phases.

### *3.3.2 Phase currents*

The measured inductor currents in the four phases are illustrated in Figure 8.9. The measurement is taken for the module operating with 2kW output power in buck mode with $V_{14}$ = 14V and $V_{42}$ = 42V. The figure shows that there is an imbalance between the four inductor currents.

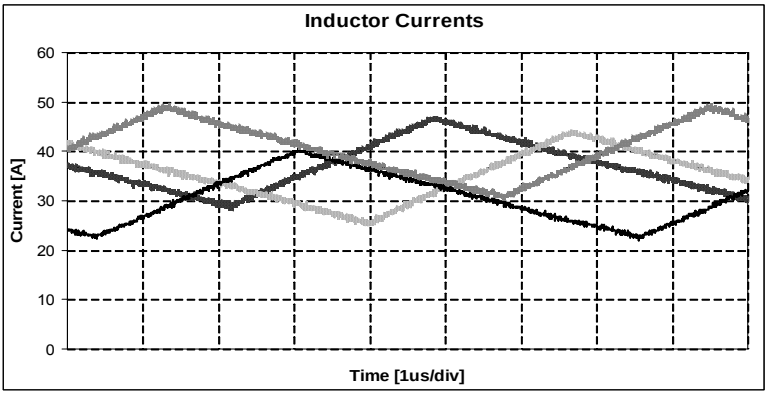



**Figure 8.9. The inductor currents for all four phases operating at full electrical load with P = 2kW, $V_{14}$ = 14V, $V_{42}$ = 42V and $I_{14}$ = 140A in buck mode**

The imbalance between the inductor currents is attributed to the imbalances in the control circuit, the long measurement wires and the very small feedback signal (1mV/A). It is expected that when the control circuit is integrated into the module, the measurement wires will be significantly shorter and the current imbalances should also be smaller.

### *3.3.3 Terminal voltages with and without the integrated EMI filters*

The module terminal voltages are measured to determine the differential mode voltage ripple with and without the integrated EMI filter structures. This is done on both of the module terminals for the module operating at full electrical power, in buck mode and with $V_{14}$ = 14V and $V_{42}$ = 42V. The measurements presented are not EMI compliance measurements but instead give a very good indication of how well the integrated EMI filters function. The EMI compliance measurements require both the terminal voltages and currents to be measured in common and differential mode as a function of frequency under defined physical and load conditions. This is described in the EMI standard. The measurements presented show the voltage ripple reduction achieved by the filter structures in the time domain.

The voltage ripple on the $V_{42}$ terminals with and without the EMI filter structures is measured and plotted in Figure 8.10. Figure 8.10a shows the voltage ripple on the terminals without the EMI filter structure in place and without the DC component. The peak to peak voltage ripple is in the order of 1.8V. The same measurement is performed but with the EMI filters installed and again without the DC component. The result is plotted in Figure 8.10b, which shows a peak to

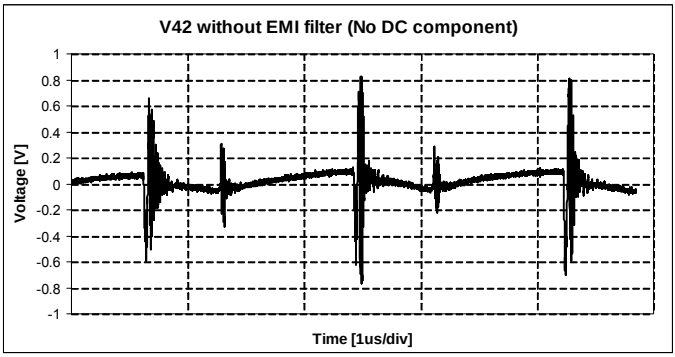



**Figure 8.10a. Measured differential voltage ripple on the $V_{42}$ terminals without the EMI filters and without the DC component**

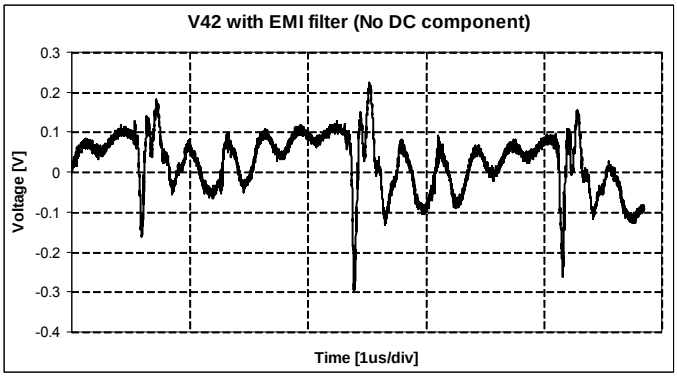



**Figure 8.10b. Measured differential voltage ripple on the $V_{42}$ terminals with the EMI filters and without the DC component**

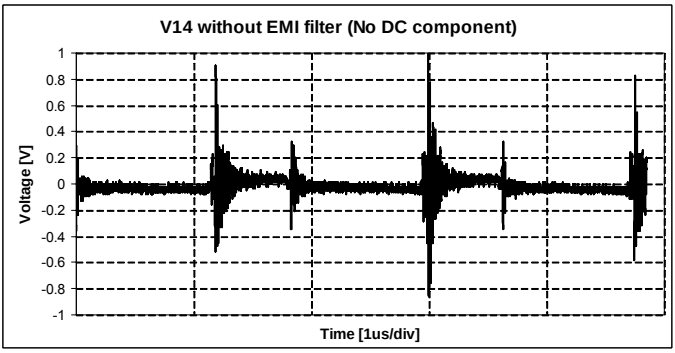



**Figure 8.11a. Measured differential voltage ripple on the $V_{14}$ terminals without the EMI filters and without the DC component**

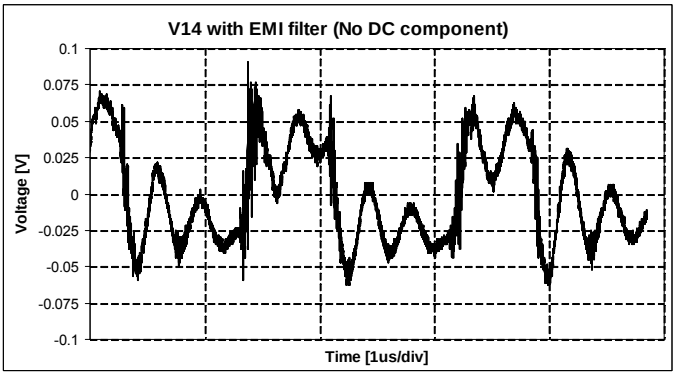



**Figure 8.11b. Measured differential voltage ripple on the $V_{14}$ terminals with the EMI filters and without the DC component**

peak voltage ripple in the order of 500mV. The maximum allowed voltage ripple at this operating point is 420mV.

The same measurement is performed on the $V_{14}$ terminals with the module operating with the same parameters as in the previous case. The measured differential voltage, without the DC component, with and without the EMI filters is plotted in Figure 8.11.

The measured voltage ripple without the EMI filter, for the module operating in buck mode with full electrical load is plotted in Figure 8.11a, which shows a peak to peak voltage ripple of approximately 2V. With the EMI filter installed, the peak to peak voltage ripple is reduced to 150mV and is plotted in Figure 8.12b. The maximum allowed voltage ripple is 140mV. For both terminals, the peak to peak voltage ripple is very close to that allowed when the filters are installed.

The impedance of the filter structures is measured for both common mode and differential mode as a function of frequency. Only one of the three series structures is measured for each terminal filter. The impedance is measured using an impedance analyser and the measurements are plotted in Figure 8.12 for the $V_{14}$ filter structure. Figure 8.12a shows the measured differential mode impedance and Figure 8.12b shows the measured common mode impedance.

The differential mode impedance is measured by measuring the input impedance of the filter structure with the output terminal short-circuited and the common mode impedance is

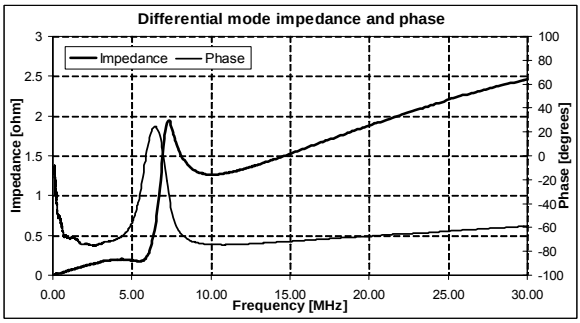



**Figure 8.12a. The measured differential mode impedance of one third (one integrated LC structure) of the 14V EMI filter**

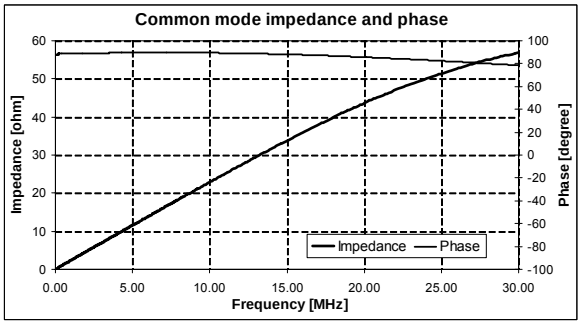



**Figure 8.12b. The measured common mode impedance of one third (one integrated LC structure) of the 14V EMI filter**

measured by measuring the impedance between the input and output of the filter structure when both the input and output terminals are short-circuited.

The measurements show that in differential mode the maximum impedance of the single $V_{14}$ filter structure is approximately 2.5Ω at 30MHz. This means that the maximum impedance for the three filter structures in series making up a single EMI filter is in the order of 7.5Ω. For common mode, the impedance of a single structure has a maximum impedance of approximately 55Ω, resulting in a maximum common mode impedance of 165Ω at 30MHz.

### *3.3.4 Switching between buck and boost mode*

An important specification for the automotive ISM is the bi-directional transfer of energy. It must be possible to redirect the direction of energy flow at any instant in time. Figure 8.13

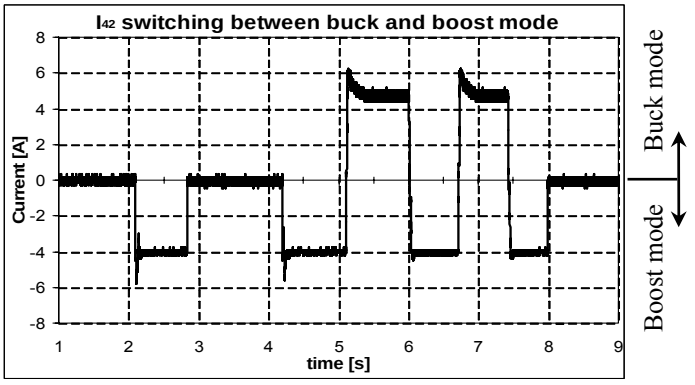



**Figure 8.13. The ISM turning on and changing between buck and boost mode**

shows the measured $I_{42}$ current for the module operating at approximately 200W output power. In buck mode $I_{42}$ is the supply current and in boost mode, is the load current. The figure shows the current $I_{42}$ being switched from zero to -4A and then from -4A to +5A and back again. As the current direction changes so does the energy flowing through the module.

# 4. Thermal evaluation

To evaluate the ISM thermally, the temperature of the module is measured under various electrical loads and thermal interface temperatures. To measure the surface temperature of the module or parts thereof, a thermal imaging camera is used.

The module is evaluated thermally first in an open configuration and then in a closed configuration. The open configuration requires the module to be tested to the full electrical rating but with the module constructed in such as way that it is possible to make thermal measurements of the components within the module. These measurements are required to ensure the module can function at the desired power levels.

The module is then reassembled into the highly compact integrated form that is the ISM. The module is re-evaluated under both full electrical and thermal loads.

## 4.1 Thermal measurements of the open module

To be able to measure the phase arm MOSFETs and decoupling capacitor temperatures with the thermal camera, they must be visually accessible while the components are being electrically excited. To achieve this the functional ISM is constructed in an open fashion – illustrated in Figure 8.15. This is achieved by removing the integrated heat sink structure for the inductors and parts of the integrated heat sink structures for the remaining passive components. The inductors are implemented alongside the module base and connected to the module via extension wires that are identified in the figure. Under these conditions the module can be excited to the full electrical load as long as none of the passive components that depend on the integrated heat sink overheat. This can be assisted by forcing the thermal interface temperature to 30°C.

Figure 8.15 shows the opened module identifying all of the components as used for the thermal measurement. The thermal measurement for the module operating with the rated output power of 2kW with $V_{14}$ = 14V, $V_{42}$ = 42V is shown in Figure 8.14. The module has an output current of 140A in buck mode and a thermal interface temperature of 30°C. The view in Figure 8.14 corresponds exactly to that in Figure 8.15, making it possible to identify all of the components on the module thermal interface.

The thermal measurement shows that the component with the highest temperature is the interconnection between the pins used to connect to the inductors and the inductor extension cables. The interconnection point has a temperature in excess of 90°C and limits the allowable thermal interface temperature.

In the figure it is easy to identify the MOSFETs, the decoupling capacitors, the bus bar structures and the gate drivers. The maximum temperature on these components is found on the MOSFETs, with a maximum temperature-rise of approximately 25°C. The thermal measurement is used to determine the temperature-rise on the MOSFETs as a function of the load current when operating in buck mode. The maximum temperature-rise for all eight

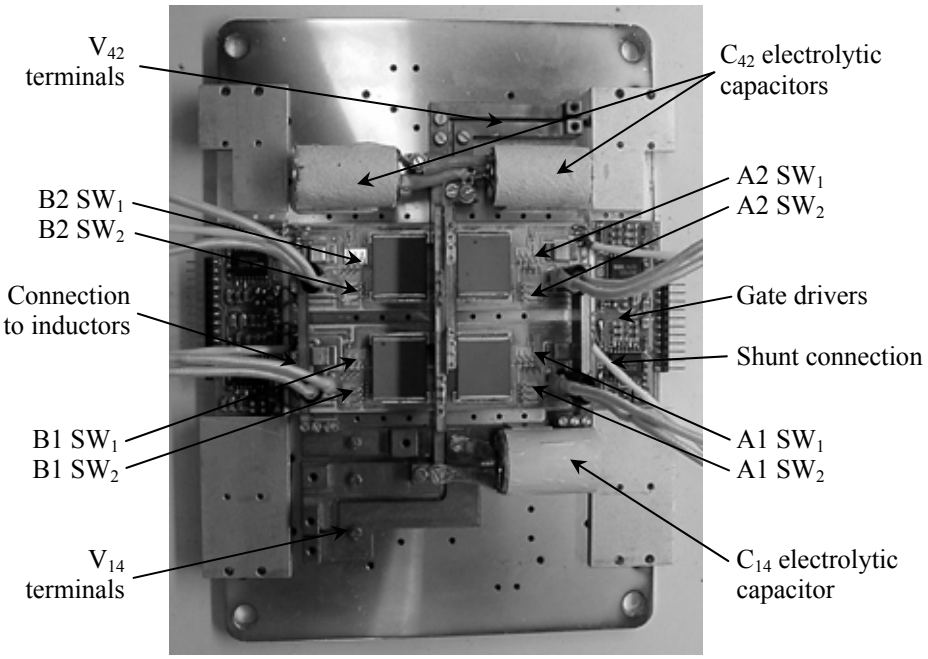



**Figure 8.15. Top view of the base of the ISM with the inductor integrated heat sink structures removed as used to measure the MOSFET operating temperatures**

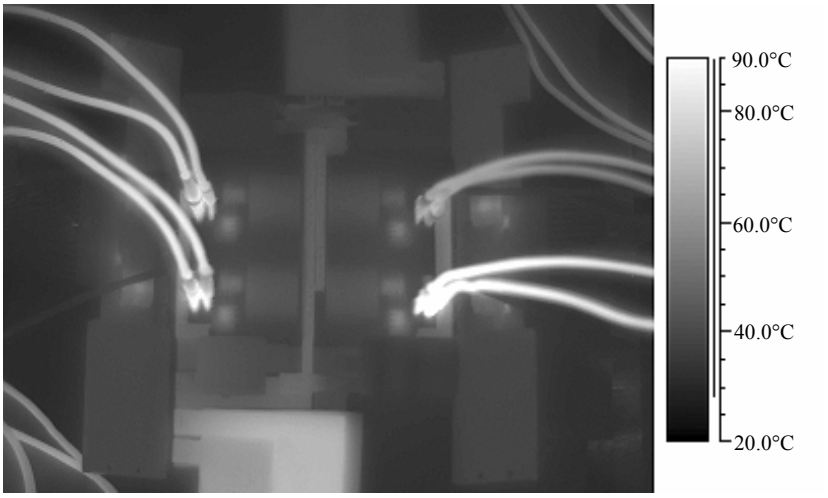



**Figure 8.14. The measured surface temperature of the base of the ISM for a thermal interface temperature of 30°C, $V_{14}$ = 14V, $V_{42}$ = 42V, P = 2kW and a load current of 140A in buck mode**

MOSFETs is recorded and tabulated in Table 8.1 as a function of the load current. In buck mode, the load current is four times the average phase inductor current.

Table 8.1 shows that the maximum temperature-rise on the MOSFETs is in the order of 25°C for a load current of $I_{14}$ = 143A. The table also shows that the maximum MOSFET temperatures are slightly different for each phase. The difference in the temperature is due to the current imbalance between the phases. For example, phase A1 carries the highest average current, resulting in more losses and a higher temperature. This is also evident in Figure 8.14.

**Table 8.1. The measured temperature-rise on the MOSFETs as a function of the load current (V14 = 14V, V42 = 42V, buck mode)**

| $I_{14}$ | ΔTa2 A2 $SW_1$ | ΔTa2 A2 $SW_2$ | ΔTa1 A1 $SW_1$ | ΔTa1 A1 $SW_2$ | ΔTb2 B2 $SW_1$ | ΔTb2 B2 $SW_2$ | ΔTb1 B1 $SW_1$ | ΔTb1 B1 $SW_2$ |
|---|---|---|---|---|---|---|---|---|
| 20.3 | 1.6 | 0.9 | 1.4 | 0.8 | 1.3 | 0.9 | 1.3 | 0.8 |
| 30.3 | 2 | 1.1 | 2.1 | 1 | 2 | 1.6 | 1.9 | 1.9 |
| 39.7 | 4.9 | 8 | 4.7 | 7.3 | 3.5 | 6.4 | 4.5 | 7.5 |
| 50.1 | 6.2 | 11.2 | 6.7 | 10.1 | 5 | 8.8 | 5.8 | 9.5 |
| 60.1 | 6.9 | 12.5 | 7.6 | 10.6 | 6 | 10.1 | 6.8 | 11 |
| 70.2 | 7.8 | 13.9 | 8.6 | 13.2 | 7 | 11.5 | 8.1 | 12.7 |
| 80.1 | 8.5 | 15 | 9.6 | 14.4 | 7.7 | 12.3 | 8.8 | 13.5 |
| 90.2 | 9.5 | 16.3 | 10.9 | 16 | 8.8 | 13.9 | 10.3 | 15 |
| 102.1 | 11 | 17.9 | 13.1 | 18.4 | 9.7 | 15.8 | 11.4 | 17.1 |
| 110.8 | 10.7 | 17.8 | 13.7 | 19 | 10.4 | 16.4 | 12.2 | 17.7 |
| 121.1 | 11.8 | 19.2 | 15.2 | 20.8 | 11.4 | 17.9 | 13.5 | 19.5 |
| 132.8 | 12.3 | 19.9 | 17 | 22.5 | 12.4 | 18.8 | 14.9 | 20.8 |
| 143.0 | 13.3 | 20.5 | 18.8 | 24.8 | 13.3 | 20.7 | 15.9 | 22.4 |

## 4.2 Thermal measurements of the ISM module

The surface temperature of the assembled ISM module, without the EMI filters is measured for full electrical and thermal load. The assembled ISM module is illustrated in Figure 8.16. The figure shows the top view of the assembled module including the structure used to connect the test terminals to the module. The EMI filters are not installed for this measurement. The view in Figure 8.16 corresponds to the view of the thermal measurements.

The thermal measurements are plotted in Figure 8.17. Figure 8.17a shows the thermal measurement for the structure in Figure 8.16 with a thermal interface temperature of 110°C, operating in buck mode, delivering 2kW output power with $V_{14}$ = 14V and $V_{42}$ = 42V. The maximum surface temperature in the measurement is on the interconnection between the

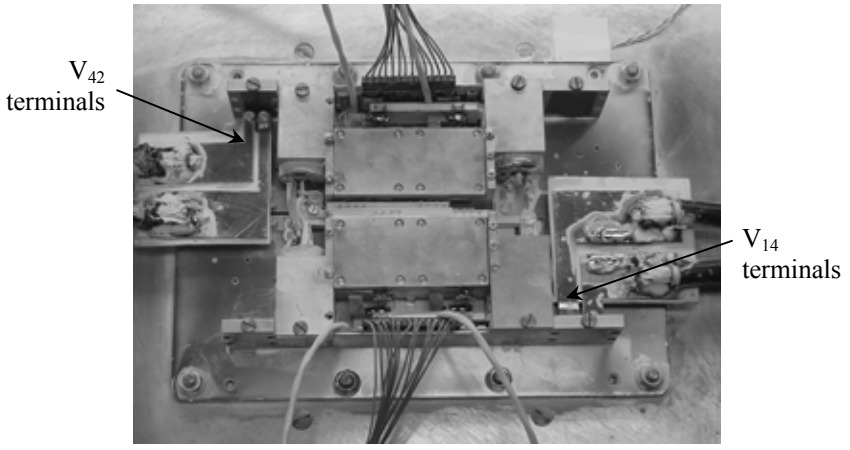



**Figure 8.16. Top view of the assembled ISM module including all the passive components, without the EMI filters, used to measure the modules surface temperature**

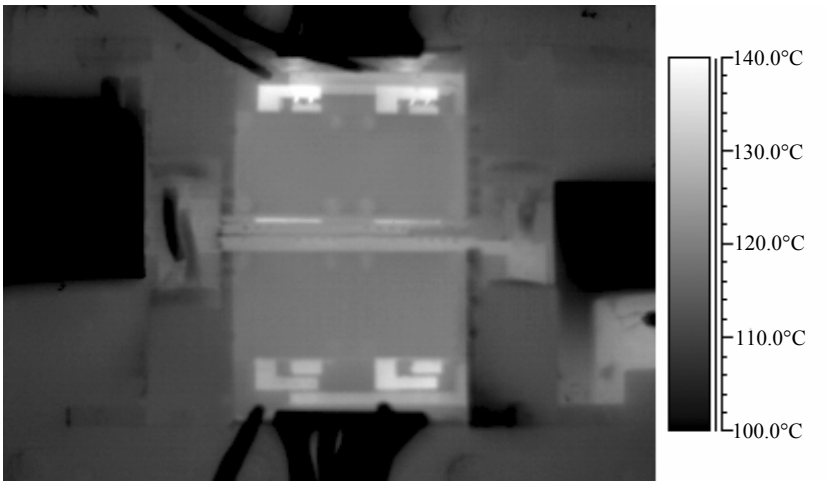



**Figure 8.17a. Thermal measurement of the ISM module, without EMI filters for a thermal interface temperature of 110°C, P = 2kW, $V_{14}$ = 14V, $V_{42}$ = 42V and a load current of 140A in buck mode**

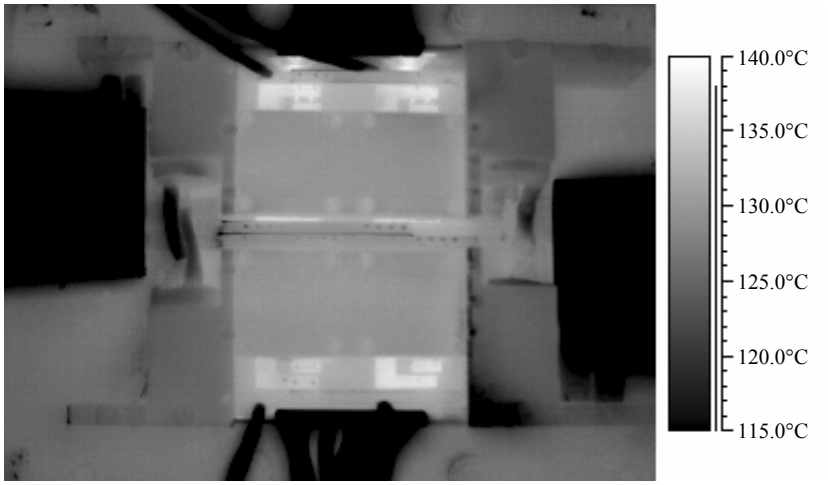



**Figure 8.17b. Thermal measurement of the ISM module, without EMI filters for a thermal interface temperature of 125°C, P = 1kW, $V_{14}$ = 14V, $V_{42}$ = 42V and a load current of 70A in buck mode**

inductor conductors and the pins leading to the DBC below the inductors. The highest temperature measured at this point is just over 140°C, which corresponds to a temperature-rise of 30˚C. The figure shows that the temperature measured on the inductor interconnection is different for the four inductors. This is due to the non-ideal current sharing between the phases. The figure also shows that the temperature-rise on the electrolytic capacitors is not significantly high: indeed, it is difficult to distinguish the capacitors from the background temperature.

Figure 8.17b shows the same measurement but for the module operating with an output power of 1kW and a thermal interface temperature of 125°C. Under these conditions, the maximum temperature measured on the modules surface is approximately 138°C, which is less than that measured for when the thermal interface temperature is 110°C with 2kW output power.

Figure 8.18a shows the completely assembled automotive integrated system module including

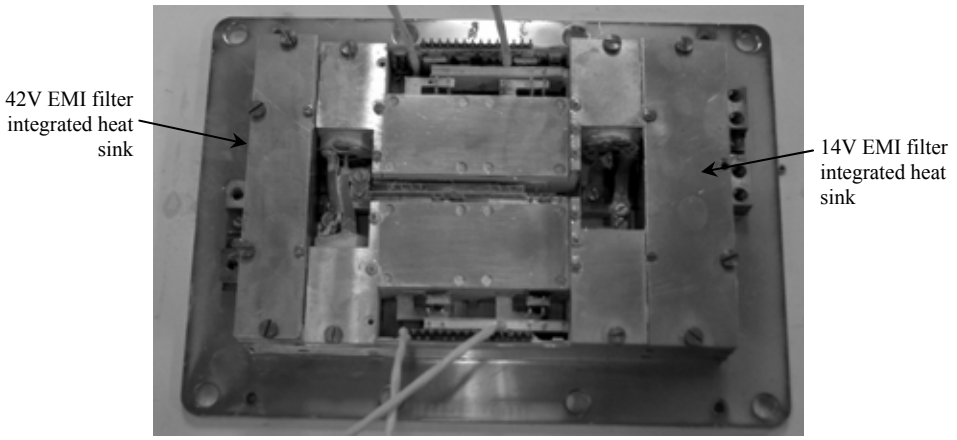



**Figure 8.18a. Top view of the completely assembled ISM module**

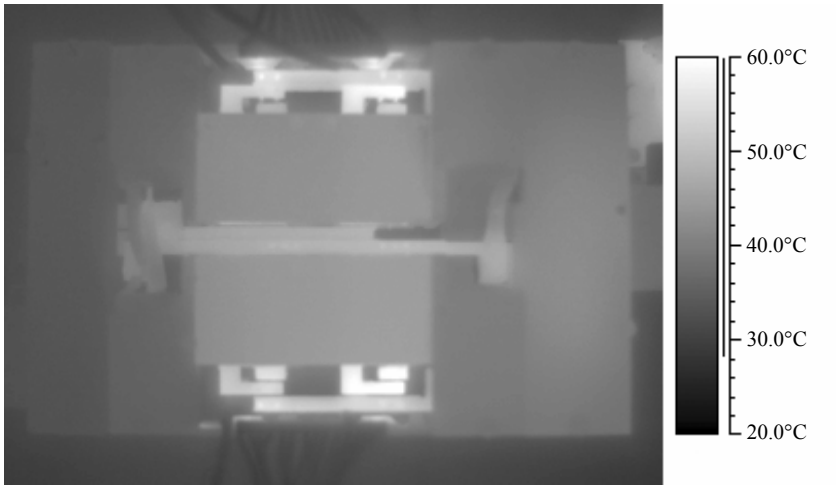



**Figure 8.18b. Thermal measurement of the complete ISM module, including the EMI filters for a thermal interface temperature of 30°C, output power of 2kW, $V_{14}$ = 14V, $V_{42}$ = 42V operating in buck mode with a load current of 140A**

the EMI filters. The control circuit and auxiliary power supply are not included. The 14V EMI filter is located on the right of the module while the 42V filter is located on the left. The module terminals can also be seen on the sides of the integrated heat sink structure.

The thermal measurement for the module in Figure 8.18a operated with 2kW output power in buck mode is plotted in Figure 8.18b for a thermal interface temperature of 30°C. The measurement shows that the surface temperature of the EMI filters is approximately 10°C higher that the thermal interface temperature for the 14V EMI filter.

### 4.3 Loss distribution within the module

The thermal measurements of the four phase arms in the ISM module can be used to determine the losses in the eight MOSFETs. The losses in each device are calculated from the experimentally determined losses and the experimentally verified loss models of the passive components.

**Table 8.2. A summary of the measured losses in the Integrated System Module without the EMI filters**

| 4-Phase ISM Measured Terminal Parameters with Thermal Interface Temperature of 30°C | | | | Total ISM Losses [W] | Total Inductor Losses [W] | Total Shunt Losses [W] | Conduction Losses [W] | Total Capacitor Losses [W] | Total MOSFET Losses [W] | MOSFET Losses[W] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{42}$ [V] | $V_{14}$ [V] | $P_{14}$ [W] | Eff [%] | | | | | | | A2 Sw1 | A2 Sw2 | A1 Sw1 | A1 Sw2 | B2 Sw1 | B2 Sw2 | B1 Sw1 | B1 Sw2 |
| 42.7 | 14.6 | 298.5 | 93.0 | 25.4 | 0.4 | 0.1 | 0.1 | 0.2 | 24.6 | 4.4 | 2.5 | 3.8 | 2.2 | 3.6 | 2.5 | 3.6 | 2.2 |
| 42.8 | 14.3 | 439.2 | 93.5 | 31.9 | 0.9 | 0.2 | 0.2 | 0.2 | 30.3 | 4.5 | 2.5 | 4.7 | 2.2 | 4.5 | 3.6 | 4.2 | 4.2 |
| 42.8 | 14.1 | 567.7 | 92.3 | 70.5 | 1.7 | 0.4 | 0.3 | 0.3 | 67.8 | 7.1 | 11.6 | 6.8 | 10.6 | 5.1 | 9.3 | 6.5 | 10.9 |
| 42.7 | 14.1 | 706.7 | 89.9 | 86.8 | 2.6 | 0.6 | 0.4 | 0.5 | 82.7 | 8.1 | 14.6 | 8.8 | 13.2 | 6.5 | 11.5 | 7.6 | 12.4 |
| 42.7 | 14.3 | 856.4 | 90.1 | 104.7 | 3.8 | 0.9 | 0.6 | 0.6 | 98.8 | 9.5 | 17.3 | 10.5 | 14.6 | 8.3 | 14.0 | 9.4 | 15.2 |
| 42.7 | 14.2 | 991.5 | 90.3 | 122.0 | 5.2 | 1.2 | 0.9 | 0.7 | 114.0 | 10.7 | 19.1 | 11.8 | 18.2 | 9.6 | 15.8 | 11.2 | 17.5 |
| 42.7 | 14.1 | 1131.1 | 90.2 | 138.7 | 6.9 | 1.6 | 1.1 | 0.8 | 128.2 | 12.1 | 21.4 | 13.7 | 20.6 | 11.0 | 17.6 | 12.6 | 19.3 |
| 42.7 | 14.3 | 1310.2 | 90.2 | 147.1 | 8.8 | 2.1 | 1.5 | 1.0 | 133.8 | 12.6 | 21.7 | 14.5 | 21.3 | 11.7 | 18.5 | 13.7 | 19.9 |
| 42.7 | 14.3 | 1431.3 | 90.2 | 162.5 | 11.3 | 2.6 | 1.9 | 1.3 | 145.5 | 14.0 | 22.8 | 16.7 | 23.4 | 12.3 | 20.1 | 14.5 | 21.7 |
| 42.7 | 14.4 | 1603.6 | 90.1 | 185.9 | 13.2 | 3.1 | 2.2 | 1.5 | 165.9 | 15.1 | 25.0 | 19.3 | 26.7 | 14.6 | 23.1 | 17.2 | 24.9 |
| 42.6 | 14.1 | 1707.5 | 90.1 | 197.8 | 16.0 | 3.7 | 2.6 | 1.7 | 173.8 | 15.9 | 25.8 | 20.4 | 28.0 | 15.3 | 24.1 | 18.1 | 26.2 |
| 42.7 | 14.5 | 1895.3 | 90.1 | 217.2 | 19.1 | 4.5 | 3.1 | 2.0 | 188.5 | 16.7 | 27.1 | 23.1 | 30.6 | 16.9 | 25.6 | 20.3 | 28.3 |
| 42.6 | 14.6 | 2060.5 | 90.0 | 224.4 | 22.2 | 5.2 | 3.7 | 2.3 | 191.1 | 17.0 | 26.2 | 24.0 | 31.7 | 17.0 | 26.4 | 20.3 | 28.6 |

A summary of the losses in all of the passive components (without the EMI filters) and in the MOSFETs as a function of the power delivered to the load in buck mode with a thermal interface temperature of 30°C is tabulated in Table 8.2. The total losses in the ISM are calculated from the difference of the measured input and output power. The various passive component loss models are used to calculate the losses in the passive components for the measured operating point. The total losses in all of the MOSFETs are calculated as the difference of the total losses in the ISM less the total passive component losses (including conductor conduction and shunt resistor losses). The measured temperature can then be used to determine the individual MOSFET losses, assuming all of the devices have the same thermal resistance. The EMI filters are not included in the measurement or calculation. The calculation method can be found in Appendix E.

The table shows that approximately 85% of all the losses in the ISM are located in the eight MOSFETs. Of the losses in the passive components, 66% is located in the four inductors.

## 5. Power density

The power density of the integrated system module is determined by considering the total volume of the module and the maximum output power.

The ISM has a total volume of 350cm$^3$ (21.3in$^3$) and the maximum measured output power processed by the converter with a thermal interface of 110°C is 2.14kW. For the given volume the converter's power density is 6.11kW/dm$^3$ (100.5W/in$^3$). This power density is achieved with a maximum temperature-rise in the ISM of less than 30˚C.

The power density includes the converter's bus capacitors and the EMI filters, both of which contribute significantly to the converter's volume. If the EMI filters are neglected, the power density is 9.1kW/dm$^3$ (149W/in$^3$).

## 6. Implementation issues

Some of the implementation issues encountered during the design and implementation of the experimental ISM are identified and discussed.

### 6.1 Electrical interconnections

The electrical interconnections, especially the interconnections between the DBC and components in the integrated heat sink above the DBC, presented severe limitations in the implementation of the ISM prototype. The interconnection between the DBC and the components in the integrated heat sink have to be capable of high currents with high thermal interface temperatures, be rugged, reliable and require relatively little volume.

In the experimental ISM, these interconnections were implemented with pins that are soldered or otherwise electrically connected to the component terminals above the DBC and then press-fitted into barrels that are soldered onto the DBC. The press-fit allows a small amount of relative movement between the pins and the barrels that helps to alleviate thermally induced stresses. However, this interconnection is fragile and cannot support very high current densities because of excessive heating. The highest temperatures measured in the experimental ISM module were located on the interconnections between the DBC and the inductor windings, which are implemented with the pin and barrel structures.

Alternative methods for implementing these electrical interconnections are required. One

possibility is to implement the electrical interconnections with pressure contacts. The electrical interconnection is established by the two conductors being in physical contact with each other and the interconnection is maintained by pressure exerted on the conductors. The source of the pressure could be either stresses internal to the conductors due to their shape (like a spring) or from an external structure (like a pressure plate). Implementing such interconnections in the ISM will have significant consequences for the design of the module. For example, the thermal interface and the combined integrated heat sink and passive component structure could be constructed as two separate parts. When these two parts are brought together and fixed to each other, the pressure-based interconnections built into the integrated heat sink structure could establish and maintain all the necessary electrical interconnections. This type of electrical interconnection does not require any solder or wielding process to maintain the interconnection and can easily be dimensioned for the desired current levels.

## 6.2 The integrated heat sink

The integrated heat sink structure is a critical component in the ISM. However, the integrated heat sink also brings with it its own set of implementation issues. In the experimental ISM, one of the main issues concerning the integrated heat sink is that it consists of many parts all of which are custom-machined into the shape and dimensions required for the specific set of components selected to implement the electrical topology. Any change to almost any parameter, such as using a different component or changing the dimensions of a heat collector has significant consequences for all the remaining components and could result in all the integrated heat sink parts having to be re-machined. Further, all of the parts making up the complete integrated heat sink structure must be assembled by hand with small screws. The integrated heat sink in the experimental ISM consists of 25 different parts with at least 50 screws.

Having to assemble the integrated heat sink with screws had significant consequences for the design of the integrated heat sink. The diameter of the screws used (M2 and M2.5) defines the smallest dimensions in many of the integrated heat sink components. For example, the heat paths are fixed to the thermal interface with M2.5 screws. This means that the smallest width that can be used for the heat paths is 3mm. For most of the heat paths a width in the order of 1mm would of have been sufficient. This results in an over-design of the integrated heat sink.

To improve the manufacturability of the integrated heat sink structure in the ISM, the integrated heat sink must consist of only a few parts which are easy to assemble and possibly flexible to minor changes. This can be achieved in one of two possible ways. The first is to manufacture the integrated heat sink structure with the minimum number of parts, which should ideally be two. One part forms the combined heat paths and part of the heat collectors while the second part forms the remainder of the heat collector structures. Placing all the passive components between the two integrated heat sink parts and then fixing them to each other results in the equivalent and final integrated heat sink structure. Due to the highly complex shape of the integrated heat sink structure, a moulding process can be used to realise the two parts. This can simplify the manufacture and implementation of the integrated heat sink structure.

The second possibility is to implement the integrated heat sink structure with a different material that is highly flexible. An example could be a thermally conductive epoxy. Such a material will have a significantly lower thermal conductivity but because the integrated heat sink structure can be moulded into very complex shapes with relative ease, this could result in a very effective way of realising the integrated heat sink structure. Further, if the epoxy

selected can absorb or withstand the thermally induced stresses, the passive components can be moulded into the integrated heat sink structure during the moulding process. Since no electrical isolation is required between the heat sink structure and the passive components, good thermal coupling can be achieved. The lower thermal conductivity will require the epoxy integrated heat sink to have more heat paths to the thermal interface and shorter heat path lengths.

## 7. Summary

The experimental implementation and evaluation of the automotive integrated ISM designed in Chapter 7 is presented in this chapter. The module is evaluated under full electrical and thermal loads. Both electrical and thermal results are presented. The experimental ISM meets all the given electrical, thermal and volumetric specifications.

A photographic description of the module is presented in the first section of the chapter. The figures show the module as the module is being assembled. The final ISM without the auxiliary power supply and control board is illustrated in Figure 8.4. The figure does show the extended measurement wires used to sense the voltage over the current measuring shuts. The wires are long so that the control system can be implemented a small distance away from the module allowing access to the module for experimental evaluation.

The module is electrically evaluated over the full electrical load range. The ISM efficiency is the first evaluation result presented, which shows the measured efficiency over the full electrical and thermal operating range. The result shows that the IMS achieves an efficiency of 90% at rated electrical power and with a thermal interface of 30°C. As the thermal interface temperature increases to 110°C, the ISM efficiency at full electrical load drops to approximately 89%. The results show only a 1% drop in the efficiency as the thermal interface temperature increases over the full electrical load range. The measurement also shows the measured efficiency for the ISM operating with a thermal interface temperature of 125°C and with 1kW output power.

Additional electrical waveform measurements are also presented to confirm the operation of the ISM. Among the electrical waveforms presented is the measured differential voltage ripple on the module $V_{14}$ and $V_{42}$ terminals with and without the integrated EMI filters. The measurements show that significant attenuation in the voltage ripple is achieved with the filters and in both cases the measured maximum voltage ripple is just larger than the specified 1% of the nominal terminal voltage.

The ISM is also evaluated thermally and the results are presented. The module is first evaluated in a semi-assembled state. The module is assembled in such a way so that the four phase arms are visually accessible, allowing the temperatures of the components of the four phase arms to be measured with the thermal camera. These measurements are used to ensure the switching devices do not exceed their thermal limit.

The completely assembled ISM is excited over the full electrical load and thermal interface temperature range. The surface temperature of the module is measured and presented for a thermal interface temperature of 110°C with 2kW output power and for a thermal interface temperature of 125°C with 1kW output power. Both measurements show that the maximum surface temperature of the module does not exceed 140°C.

# Chapter 9

## CONCLUSIONS AND RECOMMENDATIONS

## 1. Introduction

As discussed in Chapter 1, this thesis deals with the integral electrical, thermal and spatial design required to implement a power electronic converter in a state of the art power electronic module with a high power density for harsh thermal environments. An automotive power converter for the dual voltage network operating in the passenger vehicle engine compartment is chosen as the demonstrator for the study due to the stringent volume and thermal requirements that must be satisfied.

Chapter 2 investigates and classifies the state of the art in power electronic modules. The **I**ntegrated **S**ystem **M**odule (ISM) is defined as a power electronic module that contains the complete energy conversion system, including filters, in a single module. The ISM is selected as the power electronic module technology base in which to implement the automotive power converter.

The requirements on the ISM design to achieve a high power density and operate in a high temperature environment simultaneously are considered in Chapter 3. To achieve these requirements the interdependences that exist between the electrical, thermal and spatial designs are identified. The interdependencies and trade-offs between the three design domains can be used to manipulate the ISM design, making it possible to satisfy the electrical, thermal and volumetric specifications of the ISM. The interdependencies between the three design domains are considered further in Chapters 4 to 6.

Chapter 4 considers the optimisation of the electrical topology to minimise both the energy that must be stored in the module and the RMS currents in the passive components. This optimisation can be done largely on the basis of only the topology waveforms and with little or no knowledge of the physical components used to implement the topology.

The thermal management required within the ISM for operating in a high temperature environment is considered in Chapter 5. To ensure that the maximum operating temperatures of the various components within the ISM do not exceed their allowed limits, an integrated heat sink structure is defined. The integrated heat sink structure transports the heat dissipated in the various components to the environment without placing restriction on where the components can be implemented within the module.

The volumetric and spatial optimisation of the ISM is considered in Chapter 6 on both a component and system level. On the component level, the volumetric optimisation considers the trade-off between the volume of the integrated heat sink and the volume of the component and finds the minimum combined volume for a given set of excitation parameters and the maximum temperature rise. On the system level, the geometry of the various components is considered in order to minimise the total volume of the assembly of components that is required to implement the ISM.

An overview of the integral electrical, thermal and spatial design of the experimental automotive ISM for a set of given specifications is presented in Chapter 7. The experimental ISM is experimentally evaluated in Chapter 8. The experimental automotive ISM achieves a power density of 6.11kW/dm$^3$ with a thermal interface temperature of 110°C and an efficiency of 89% for 2kW output power. An efficiency of 88.5% is achieved for a thermal interface temperature of 125°C and an output power of 1kW.

# 2. Conclusions

The conclusions drawn from the work presented in this thesis can be grouped into four categories corresponding to the thesis objectives presented in Chapter 1. These objectives were:

i. *To investigate the possibility of implement the complete automotive converter in a state of the art power electronic module.*

ii. *To analyse the interdependencies that exist between the electrical, the thermal and the spatial design of the power electronic module.*

iii. *To develop techniques for a multi-objective design so that the power electronic module can meet all the given specifications.*

iv. *To design and construct a high power density, 3D integrated power electronic module prototype for the automotive environment.*

## 2.1 Power electronic modules

The automotive power converter is to be implemented in a power electronic module that contains the complete power processing system while meeting the high power density and high operating temperature specifications. However, power electronic modules or integrated power electronic modules are terms loosely used to describe a variety of modules and module-based solutions, and this makes it difficult to clearly specify the desired packaging solution. To this end power electronic modules are classified according to their level of functionality. The classification is:

i. *Power module (PM).* A power module is a structure that contains one or more power devices in a single structure.
ii. *Intelligent power module (IPM).* An IPM is a power module with additional functionality integrated into it. An IPM typically contains the power devices, the gate drivers, protection, current sensing and temperature sensing.
iii. *Integrated intelligent power module (I$^2$PM).* An I$^2$PM is a power module with additional intelligence integrated into the power module structure. The typical I$^2$PM consists of the power devices, the gate drivers, protection, current and temperature sensing, power supply, isolation, signal conditioning and possibly a micro-processor.
iv. *Integrated system module (ISM).* The ISM is a complete power conversion system in a single structure. The module is self-contained, self-protecting and self-driven. No additional components are required to implement a working system (with the possible exception of EMI filters).

The integrated system module (ISM) is a new term given to a group of emerging highly intelligent, highly functional power electronic modules containing the complete power processing system for a given application. The current trend in the development of power

electronic modules suggests that the ISM is going to become the central focus for the future development of power electronic modules. High power densities, high operating temperatures, high levels of functionality and intelligence make the ISM a viable and attractive solution for a wide range of power electronic applications and power levels.

It is concluded that the automotive power converter can be implemented in a power electronic module in the form of a futuristic ISM. The current state of the art ISMs do not meet the power requirements or the thermal requirements imposed on the module by the automotive specifications and environment. The level of integration and functionality of these ISMs must be increased to successfully implement the automotive converter.

## 2.2 The interdependent electrical, thermal and spatial design

The ISM requirements are seemingly contradictory in nature. A high power density requires small components with large levels of excitation inherent to higher losses while a high operating temperature requires reduced losses normally achieved with low levels of excitation and consequently larger component volumes. The only way to satisfy both the high power density and high operating temperature specification simultaneously and in the same volume is by understanding and manipulating the interdependencies between the electrical, thermal and spatial design domains. For modern ISMs this is a necessity if specifications are to be met.

The interdependencies and trade-offs between the three design domains are considered in Chapter 3 and repeated in Figure 9.1. Through manipulating the identified design interdependencies and the trade-offs, it is possible to satisfy the seemingly contradictory specifications.

The interdependent electrical, thermal and spatial design must achieve the following:

- The electrical topology is the source of the volume required for energy storage and indirectly the source of the volume required for heat transfer to the environment through the thermal design. Thus the energy storage requirements of the topology as well as the heat dissipated in the topology must be minimised.

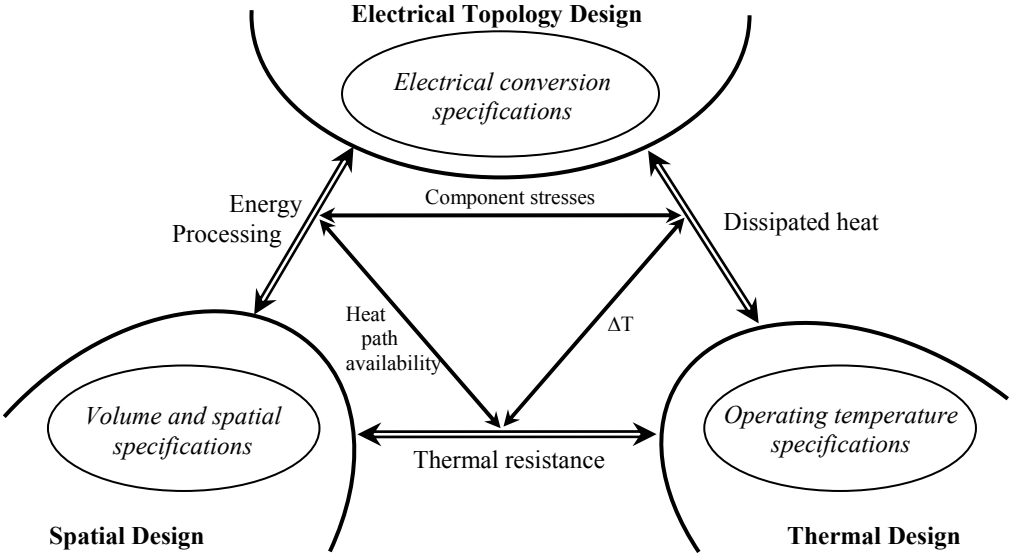



**Figure 9.1. The relationship between the electrical, thermal and spatial design domains**

- The temperature rise in the components is determined by the amount of heat that must be transferred to the environment and how the heat is transferred to the environment. To increase the module's operating temperature the heat dissipated in the components must be minimised and the temperature drop between the components and the environment must be such that the sum of the environment temperature and the temperature drop between the components and the environment is less that the component's maximum allowed operating temperature.
- To minimise the volume required to implement the module in, the combined volume of that required for energy processing and the volume required for the transfer of heat to the environment must be minimised.

## 2.3 Techniques for a multi-objective design

In Chapters 4 to 6 several techniques for manipulating the design interdependencies are considered. The conclusions that can be drawn in these chapters are summarised.

### *2.3.1 Topology optimisation*

The topology optimisation considers how to reduce both the energy that must be stored and the RMS current in the passive components that are implemented in the ISM. The conclusions that can be drawn are:

- Given the high power density and high operating temperature requirements of the ISM, the appropriate topology must be selected. The selected topology should show at least some of the following characteristics:
    - low or reduced number of passive components,
    - a direct topology,
    - low or reducible component stresses,
    - high efficiency,
    - temperature insensitive and
    - ease of control.

  The bi-directional synchronous rectifier is selected for the automotive ISM.
- The RMS currents and the maximum energy that must be stored in the passive components in the ISM can be significantly reduced by interleaving more than one phase of the synchronous rectifier in time. The exact reduction in the RMS current and energy stored in the passive components is a strong function of the number of implemented phases, the phase arm inductance and the duty cycle.
- Randomly increasing the number of implemented synchronous rectifier phases above two does not guarantee a reduction in either the RMS current or energy stored in the passive components. For the same topology parameters (inductance, supply voltage, power rating) the minimum in both the RMS current and energy stored in the passive components is highly dependent on the duty cycle. For example it is possible for a two-phase topology to have lower RMS currents in the bus capacitors than the equivalent three-phase configuration for a duty cycle of 50%. However, if the duty cycle is either larger than ≈55% or smaller than ≈45%, then the three-phase topology has lower RMS currents in the same components for the same topology parameters.
- Operating the synchronous rectifier topology in ZCCM (continuous conduction mode but with the inductor current crossing zero) is a popular technique to reduce the switching losses in the topology. However, both the RMS currents and the energy stored in all of the passive components are significantly increased. As a result the passive components' volume must be increased, reducing the achievable power density. In a high power density power module it is better to minimise the RMS currents and energy stored in the passive

components to reduce their volumes at the cost of the increased switching losses. This is due to the very low thermal resistance that can easily be achieved for the switching devices in state of the art power electronic modules.

- Making the phase arm inductance infinitely large does not reduce the RMS current or energy storage requirements of $C_{42}$ as it does for $C_{14}$. The RMS current and energy stored in $C_{42}$ both have minimums for a relatively small value of phase arm inductance. Moreover, this minimum does not change significantly as the phase arm inductance increases. The result is that a relatively small value of inductance results in a minimum in the RMS current and energy stored in the capacitor for a given duty cycle.

### *2.3.2 Thermal management optimisation*

The thermal management optimisation deals with minimising the temperature-drop between the components within the ISM and the environment. The conclusions that can be drawn are:

- The integrated heat sink structure is a thermal management structure used to collect the heat dissipated in a component and then transport that heat to the thermal interface where it is transferred to the environment. The integrated heat sink allows a passive component's loss density to be significantly increased without the penalty of a large thermal management volume or large temperature-drop.
- The length of the heat path can be adjusted according to the amount of heat being conducted, the heat path geometry and material properties. The heat path can be dimensioned so that the component in the heat collector can be placed almost anywhere with the ISM volume without the component overheating. This gives the ISM the freedom to utilise the height of the module to implement the desired topology in, allowing the ISM design to break away from the traditionally two-dimensional construction.
- The integrated heat sink structure allows the heat dissipated in the passive component to be transferred to the thermal interface through an area on the thermal interface that is significantly smaller than the footprint of the passive component. The area required on the thermal interface for the component is only the cross-sectional area of the heat path connecting the heat collector to the thermal interface. This results in more surface area on the thermal interface for other components that have significantly higher loss densities, such as semi-conductor devices.
- The integrated heat sink structure requires that the loss distribution in the passive component implemented within it be rethought. When a passive component is implemented together with an integrated heat sink structure, it is possible to redistribute the losses within the component in such a way that the maximum temperature rise in the component is limited. In an inductor, for example, the losses can be redistributed so that they are mostly located in the winding. Due to the shape of the component and heat collector, it is relatively easy to create a very low thermal impedance between the inductor winding and the heat collector by way of a winding clamp. This removes the heat from the winding very effectively, allowing a much higher loss density in the winding.
- The integrated heat sink structure is experimentally evaluated. The predicted and measured losses and temperature distribution correlate well, verifying the loss and temperature distribution modelling.

### *2.3.3 Volumetric and spatial optimisation*

The volumetric and spatial optimisation deals with finding the minimum volume in which the components in the ISM can be implemented. The following conclusions can be drawn:

- The combined volume of a passive component and integrated heat sink can be reduced by reducing the volume of the field establishing part of the component and still meet the energy storage requirements. For example, the current density in an inductor's winding can be increased without changing the energy storage volume (assuming the energy is stored in an air-gap), resulting in a smaller component volume for the same energy storage requirements. The component loss density will increase resulting in a higher temperature-drop over the integrated heat sink if the integrated heat sink geometry or material properties are not significantly changed.
- The optimum volume of the inductor in an integrated heat sink structure is the minimum combined volume for a given temperature rise. The combined volume and temperature rise in the component are functions of the VRC and current density. For a fixed maximum temperature rise, the lowest combined volume is not found with the structure having the highest VRC but instead with a structure having a relatively small VRC. This is because the lower VRC results in a larger volume being available for the inductor and consequently the current density in the winding is reduced, resulting in smaller losses.
- The volume of the ISM can be reduced by implementing several functions with a single part. An example is using the integrated heat sink structure, in addition to removing the dissipated heat from the components to provide several other functions. Examples include providing the passive components with mechanical integrity, keeping them located in their positions within the module, using the integrated heat sink as the housing of the module and combining several heat collectors on a single heat path. All of these functions must be performed in the module if it is to function. If they are all implemented with a single part then the ISM volume can be reduced.
- The volume of an assembly of components can be reduced by using geometrically complementary shapes for the components. A significant portion of an assembly volume is unused because the shapes of the various components do not fit together in the optimum way. By changing the shapes of the components a significant reduction in the volume can be achieved. This is especially the case when the third dimension is accessible for implementing components in.
- A very high current density inductor ($J$ = 40A/mm$^2$, $I_{ave}$ = 43.2A) is modelled and experimentally implemented in an integrated heat sink with a total combined volume of only 7.8cm$^3$ and a maximum temperature rise of 31.8°C. The predictions and experimental results correlate well. This verifies the volumetric optimisation modelling.

### 2.4 The experimental automotive ISM

The integral electrical, thermal and spatial design of the ISM is implemented in the design of the experimental automotive ISM for the given specifications. The conclusions that can be drawn are:

- The experimental automotive ISM meets the given electrical, thermal and spatial specifications simultaneously and in the same volume. The ISM achieves a power density of 6.11kW/dm$^3$ with a thermal interface temperature of 110°C and an efficiency of 89% for 2kW output power. An efficiency of 88.5% is achieved for a thermal interface temperature of 125°C and an output power of 1kW.
- The maximum temperature rise in the experimental ISM is only 30°C. This implies that a higher power density can be achieved by forcing the thermal interface to a low temperature and operating the ISM with a higher internal temperature drop within the maximum ratings of the components.

- Several limiting factors were encountered during the implementation of the experimental ISM. Among the most severe of these are the high current density, high temperature three-dimensional interconnections. These must be overcome for further advancement to take place.

### 2.5 Thesis contribution

The main scientific contributions of this thesis can be summarised as:

- The integral electrical, thermal and spatial design as used for implementing a complete power electronic converter in a power electronic module. The integral design in itself is not new but in this thesis the relationships between the designs are considered and manipulated to make it possible to implement a complete power converter, including filters and bulk energy storage in a power electronic module with a high power density and capable of operating in high temperature environments.
- Several techniques were considered for manipulating the interdependencies and trade-offs between the design domains. Examples include interleaving, the integrated heat sink structure and complementary geometries. None of these concepts in itself are new, but combining all of them through the integral design is unique. These techniques through the integral design make it possible for the experimental automotive ISM to meet the given electrical, thermal and spatial specifications even though they are seemingly contradictory in nature.
- In the literature there are several examples of inverters and a few DC/DC converters being implemented as ISMs. However, the power rating of these ISMs, and specifically that of the DC/DC converters, is relatively low and all of these modules have a limited maximum thermal interface temperature (normally between 85°C and 100˚C, limited by the passive components) and are severely de-rated as the thermal interface temperature increases. The experimental DC/DC ISM presented in this thesis achieves both a higher power rating (2kW) and a higher maximum thermal interface temperature (up to 125°C) without the use of special high temperature components.

## 3. Recommendations for further research

The following recommendations for further research can be made.

Concerning the integral electrical, thermal and spatial design:

- The integral electrical, thermal and spatial design of the ISM, though already a necessity in meeting the high power density and high operating temperature specifications, can be further improved on by expanding on the design domains and interdependencies. For example, the current interdependent design considered in this thesis has three design domains. These can be expanded to five design domains by including the EMI and reliability design domains. Interdependencies between the five design domains can be defined and manipulated to meet the given specifications, including EMI and reliability specifications. The two new design domains have the following design interdependencies with the current design domains:
  - The EMI design domain has design interdependencies with the electrical and the spatial designs through the component high frequency behaviour and spatial parasitics.
  - The reliability design has interdependencies with the electrical, thermal and spatial designs through material properties, thermal cycling and thermally induced stresses.

- The development of easy to use and fast multi-disciplinary 3D modelling and simulation software tools in which the integral design can be implemented, will be of great benefit. Currently all of the design domains are analysed in a single simulation tool that is most suited to that specific design domain, with the minimum in cross-coupling between design domains. This makes coupling the different designs to each other a cumbersome and time-consuming task. The development of a single software tool that can perform all the necessary multi-disciplinary analysis and couple the different design domains through the design interdependencies can help to reduce the design time while still resulting in the optimum solution for the ISM.

Concerning the interdependence manipulation techniques:

- In this thesis a few techniques for manipulating the design interdependencies and trade-offs were presented and discussed. These techniques are based on the topology used and the integrated heat sink structure. If a different topology were used it can be expected that different interdependencies and trade-off manipulation techniques would be required. It could be an interesting investigation to find more such techniques and determine each one's strengths and weaknesses.
- The RMS currents and the energy stored in the passive components in Chapter 4 are based on the topology's ideal voltage and current waveforms. The information in these waveforms is sufficient to get a good idea of the RMS currents and stored energy in the components. To improve on these calculations the non-ideal behaviour of the components could also be included. For example, the reverse recovery of the freewheeling diodes should also be included because this increases both the RMS currents and energy storage requirements of the passive components, in particular $C_{42}$. Furthermore, including the switching characteristics or approximated switching losses can also be helpful in determining the optimum number of phases in a multi-phase topology.
- The integrated heat sink is a necessity for the passive components to function correctly with the high thermal interface temperature and high loss densities. However, using aluminium for the implementation of the integrated heat sink requires very detailed design of the component and integrated heat sink structure and can be difficult to manufacture. Investigating the use of different materials and production methods for the implementation of the integrated heat sink can have some benefits, especially in terms of ease of manufacture and cost. One possible alternative material could be metal-loaded epoxy which together with the component can simply be moulded into the desired shape. However, this will come at the cost of a much lower thermal conductivity. Various combinations of materials and composites could be interesting to investigate for use as an integrated heat sink.

Concerning the experimental ISM:

- The complete integrated heat sink structure in the experimental ISM consists of many parts that all had to be manufactured, machined and then installed by hand. For the integrated heat sink to be more implementation-friendly, alternative methods for implementing the integrated heat sink are required. These could include using different materials that can be moulded, for example, or manufacturing the complete integrated heat sink with the minimum number of parts.
- Three-dimensional interconnections were one of the largest issues in the experimental ISM. High current density and high operating temperature interconnections between the DBC on the thermal interface and the components implemented in

the integrated heat sink in the third dimension present serious and restricting limitations on the ISM design. These interconnections are difficult to make, are generally not very reliable or robust and result in localised heating. The highest temperatures recorded in the experimental ISM were on the interconnections. This issue must be addressed for the future for 3D integration in power electronic modules to be successful. Alternative interconnection techniques, such as pressure contacts or flexible interconnections, are interesting possibilities.

# Appendix A

## ENERGY STORAGE IN THE SYNCHRONOUS RECTIFIER

## 1. Introduction

In this appendix, the maximum energy that must be stored in the passive components of the synchronous rectifier and the total energy passing through the passive components in one switching period is calculated for each component.

## 2. Energy stored in L as a function of the number of phases

The main waveforms for a single inductor in a system of *N*-phases are plotted in Figure A.1 for buck operation. For the analysis also to hold for boost mode, the current convention in Chapter 4 must simply be reversed. Considering buck mode, the inductor has only two possible waveforms irrespective of the number of phases and average current. The first is illustrated in the top of Figure A.1 for CCM and the second is illustrated in the bottom for ZCCM with ZCCM[a] as defined in Chapter 4. As the number of phases change, the average inductor current changes accordingly while the current ripple, $\Delta I_L$ remains the same for a given inductance, duty cycle and topology specifications.

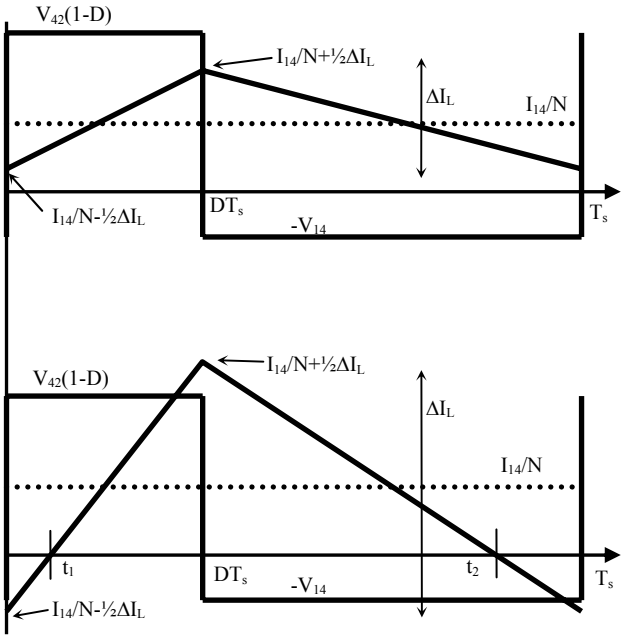



**Figure A.1. The inductor waveforms for an arbitrary number of phases (Top - CCM, Bottom - ZCCM)**

[a] ZCCM is continuous conduction mode with zero crossing. The inductor current always keeps its triangular shape irrespective of the average inductor current and never goes into true DCM.

The border between CCM and ZCCM can be found by determining when the inductor current becomes negative. Thus the boundary condition that must be satisfied to be in CCM is:

$$\frac{|I_{14}|}{N} \geq \tfrac{1}{2}\Delta I_L \tag{A.1}$$

where $N$ is the number of phases,
$|I_{14}|$ is the absolute value of the current flowing into or out of the topology at the 14V terminals[a] [A]
and $\frac{|I_{14}|}{N}$ is the average inductor current implemented in an $N$-phase topology.

The peak energy that is stored in the inductor is given by:

$$E_{\max\_L} = \tfrac{1}{2} L I_{\max}^2 \tag{A.2}$$

where $I_{max}$ is the maximum current in the inductor [A],
$L$ is the inductance [H]
and $E_{max\_L}$ is the energy that is stored in the inductor [J].

In both CCM and ZCCM the maximum current is given as:

$$I_{\max} = \frac{|I_{14}|}{N} + \tfrac{1}{2}\Delta I_L \tag{A.3}$$

where $\Delta I_L$ is the peak to peak current ripple in the inductor [A] and is given by:

$$\Delta I_L = \frac{V_{42}(1-D)DT_s}{L} \tag{A.4}$$

where $T_s$ is the switching period [s].

Thus the maximum energy that the inductor must be capable of storing in both CCM and ZCCM is:

$$E_{\max\_L} = \tfrac{1}{2} L \left( \frac{|I_{14}|}{N} + \tfrac{1}{2}\Delta I_L \right)^2 \tag{A.5}$$

To find the inductance that will result in the minimum energy being stored in the inductor, equation A.5 must be differentiated and the result made equal to zero. Solving this equation for the inductance will give the inductance resulting in the minimum energy being stored in the $N$-phase topology inductor.

[a] The absolute value of the current is used to make the analysis independent of the topology operating in either buck or boost mode. The analysis for both modes is exactly the same with the only difference being the direction of the currents through the topology. The absolute function removes this dependency.

Differentiating equation A.5 and making the result equal to zero:

$$\frac{dE_{\max\_L}}{dL} = \tfrac{1}{2}\left(\frac{I_{14}}{N} + \tfrac{1}{2}\Delta I_L\right)^2 - \tfrac{1}{2}\left(\frac{I_{14}}{N} + \tfrac{1}{2}\Delta I_L\right)\Delta I_L = 0 \tag{A.6}$$

Solving for the inductance:

$$L_{\min\_energy} = \tfrac{1}{2}\frac{NV_{42}^2(1-D)D^2T_s}{P} \tag{A.7}$$

where $L_{min\_energy}$ is the inductance for an $N$-phase system resulting in the lowest energy stored in the inductors [J].

To determine the energy that is processed by the inductor in one switching period, the inductor current must be considered for both conduction modes.

In CCM, the energy that is processed by the inductor is the maximum energy in the inductor, given by equation A.2 less the energy in the inductor at the beginning of the charging period. Thus the energy processed by the inductor is:

$$E_{processed\_L} = \tfrac{1}{2}LI_{\max}^2 - \tfrac{1}{2}LI_{\min}^2 \tag{A.8}$$

where $E_{processed\_L}$ is the energy processed by the inductor in one switching period [J],
$I_{max}$ is as previously defined [A]
and $I_{min}$ is the inductor current at the beginning of the charging period [A]:

$$I_{\min} = \frac{|I_{14}|}{N} - \tfrac{1}{2}\Delta I_L \tag{A.9}$$

Substituting equations A.3 and A.9 into equation A.8 yields the energy processed by the inductor in CCM:

$$E_{processed\_L} = \tfrac{1}{2}L\left(\left(\frac{|I_{14}|}{N} + \tfrac{1}{2}\Delta I_L\right)^2 - \left(\frac{|I_{14}|}{N} - \tfrac{1}{2}\Delta I_L\right)^2\right) \tag{A.10}$$

which can be reduced to:

$$E_{processed\_L} = L\Delta I_L\frac{|I_{14}|}{N} \qquad if\ \frac{|I_{14}|}{N} \geq \tfrac{1}{2}\Delta I_L \tag{A.11}$$

In ZCCM, there are two periods when energy is flowing into the inductor and two periods when energy is flowing out of the inductor. The first period when energy is flowing into the inductor is $t_1 < t \leq DT_s$ and the second period is $t_2 < t \leq T_s$. In buck mode, the first charging period represents energy that comes from the source at the $V_{42}$ terminals while the second

charging period represents energy the is taken from the $V_{14}$ terminals that must first be removed from the inductor before energy can be transferred from the $V_{42}$ source again.

The energy processed by the inductor in ZCCM is the sum of the energy stored in the two intervals and can be calculated similarly as in CCM. However, in ZCCM, for both charging intervals the inductor current starts from zero implying the initial energy stored in the inductor at the beginning of each charging cycle is zero. Thus the energy stored in the inductor in ZCCM is:

$$E_{processed\_L} = \tfrac{1}{2} L I^2_{\max,period\,1} + \tfrac{1}{2} L I^2_{\max,period\,2} \tag{A.12}$$

where $I_{max,period\,1}$ is the maximum current at the end of the first charging period [A]
and $I_{max,period\,2}$ is the maximum current at the end of the second charging period [A].

Considering Figure A.1 for ZCCM:

$$I_{\max,period\,1} = \frac{|I_{14}|}{N} + \tfrac{1}{2}\Delta I_L \tag{A.13}$$

and

$$I_{\max,period\,2} = \frac{|I_{14}|}{N} - \tfrac{1}{2}\Delta I_L \tag{A.14}$$

Substituting equations A.13 and A.14 into equation A.12:

$$E_{processed\_L} = \tfrac{1}{2} L \left( \left( \frac{|I_{14}|}{N} + \tfrac{1}{2}\Delta I_L \right)^2 + \left( \frac{|I_{14}|}{N} - \tfrac{1}{2}\Delta I_L \right)^2 \right) \tag{A.15}$$

which can be simplified to:

$$E_{processed\_L} = L \left( \left( \frac{|I_{14}|}{N} \right)^2 + \tfrac{1}{4}\Delta I_L^2 \right) \qquad if\ \frac{|I_{14}|}{N} < \tfrac{1}{2}\Delta I_L \tag{A.16}$$

The energy processed by the inductor in one switching period depends on the mode of operation and is summarised as:

$$E_{processed\_L} = \begin{cases} L\Delta I_L \dfrac{|I_{14}|}{N} & if\ \dfrac{|I_{14}|}{N} \geq \tfrac{1}{2}\Delta I_L \\ L\left( \left( \dfrac{|I_{14}|}{N} \right)^2 + \tfrac{1}{4}\Delta I_L^2 \right) & if\ \dfrac{|I_{14}|}{N} < \tfrac{1}{2}\Delta I_L \end{cases} \tag{A.17}$$

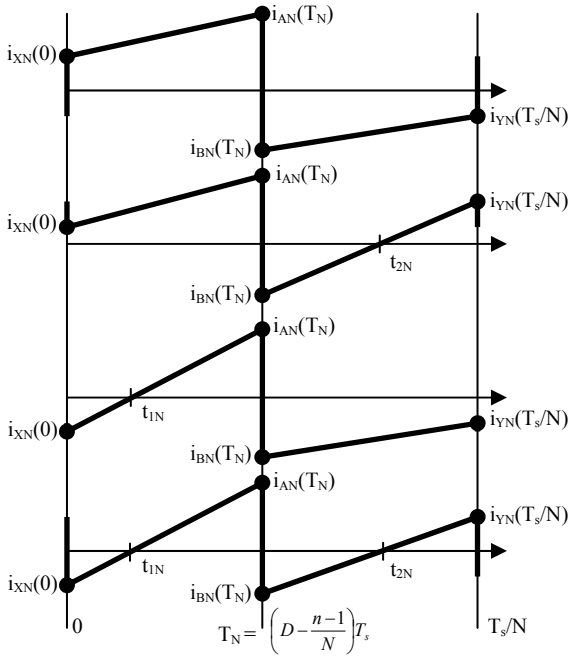



**Figure A.2. The 4 basic current waveforms present in $C_{42}$ as a function of the number of phases**

## 3. Energy stored in $C_{42}$ as a function of the number of phases

To determine the energy that is both stored in the capacitor and that is processed by the capacitor, the charge that the capacitor must store and process per switching cycle must first be calculated. Once the charge that the capacitor must accommodate is known, the required capacitance for a specific voltage ripple in the input and output bus voltages can be determined. With the capacitance know, the energy that the capacitor must be capable of storing can be determined.

The charge stored in the capacitor as a function of the number of phases is considered first. The current waveform in $C_{42}$ can be completely described by the 4 waveforms in Figure A.2. The waveform is repeated every $\frac{T_s}{N}$ seconds and is divided into two linear periods. The division takes place at $\left(D - \frac{n-1}{N}\right)T_s$ where *n=1* for an *N=1* system, *n=1, 2* for an *N=2* system and so on. The waveform has four possibilities based on whether the current is positive or negative at the beginning and end of each linear period. To full describe the waveforms, general expressions are required for $i_{XN(0)}$, $i_{YN(T_s/N)}$, $i_{AN(T_N)}$, $i_{BN(T_N)}$, $t_{1N}$ and $t_{2N}$ where $T_N = \left(D - \frac{n-1}{N}\right)T_s$ . With these six pointes in the capacitor current, the charge in the capacitor can be calculated for any number of phases and operating point.

To determine the general expressions, the 6 points are calculated for a 1-phase system, a 2-phase system and a 3-phase system. With this information, the general equations for the 6 points can be extrapolated.

The current in $C_{42}$ for a single phase system can be fully described as:

| 1-phase<br>$0 \le D \le 1$<br>$n = 1, N = 1$ |
|---|
| $i_{XN}(0) = I_{14}(1-D) - \frac{1}{2}\Delta I_L$ |
| $i_{YN}(T_s) = I_{14}D$ |
| $i_{AN}(DT_s) = I_{14}(1-D) + \frac{1}{2}\Delta I_L$ |
| $i_{BN}(DT_s) = I_{14}D$ |
| $t_1 = \frac{1}{2}DT_s - \frac{I_{14}}{\Delta I_L}(1-D)DT_s$ |

The current in $C_{42}$ for a 2-phase system can be fully described as:

| 2-phase<br>$0 \le D \le \frac{1}{2}$<br>$n = 1, N = 2$ | 2-phase<br>$\frac{1}{2} < D \le 1$<br>$n = 2, N = 2$ |
|---|---|
| $i_{XN}(0) = I_{14}\left(\frac{1}{2}-D\right) - \frac{1}{2}\Delta I_L$ | $i_{XN}(0) = I_{14}(1-D) - \frac{1}{D}\Delta I_L\left(D-\frac{1}{2}\right)$ |
| $i_{YN}\left(\frac{T_s}{2}\right) = I_{14}D$ | $i_{YN}\left(\frac{T_s}{2}\right) = I_{14}\left(\frac{1}{2}-D\right) + \frac{1}{2D}\Delta I_L(1-D)$ |
| $i_{AN}(DT_s) = I_{14}\left(\frac{1}{2}-D\right) + \frac{1}{2}\Delta I_L$ | $i_{AN}\left(\left(D-\frac{1}{2}\right)T_s\right) = I_{14}(1-D) + \frac{1}{D}\Delta I_L\left(D-\frac{1}{2}\right)$ |
| $i_{BN}(DT_s) = I_{14}D$ | $i_{BN}\left(\left(D-\frac{1}{2}\right)T_s\right) = I_{14}\left(\frac{1}{2}-D\right) - \frac{1}{2D}\Delta I_L(1-D)$ |
| $t_1 = \frac{1}{2}DT_s - \frac{I_{14}}{\Delta I_L}\left(\frac{1}{2}-D\right)DT_s$ | $t_1 = \frac{1}{2}\left(D-\frac{1}{2}\right)T_s - \frac{I_{14}}{\Delta I_L}(1-D)DT_s$ |
| | $t_2 = \frac{1}{2}DT_s - \frac{I_{14}}{\Delta I_L}\left(\frac{1}{2}-D\right)DT_s$ |

The current in $C_{42}$ for a 3-phase system can be fully described as:

| 3-phase<br>$0 \le D \le \frac{1}{3}$<br>$n = 1, N = 3$ | 3-phase<br>$\frac{1}{3} < D \le \frac{2}{3}$<br>$n = 2, N = 3$ |
|---|---|
| $i_{XN}(0) = I_{14}\left(\frac{1}{3}-D\right) - \frac{1}{2}\Delta I_L$ | $i_{XN}(0) = I_{14}\left(\frac{2}{3}-D\right) - \frac{1}{D}\Delta I_L\left(D-\frac{1}{3}\right)$ |
| $i_{YN}\left(\frac{T_s}{3}\right) = I_{14}D$ | $i_{YN}\left(\frac{T_s}{3}\right) = I_{14}\left(\frac{1}{3}-D\right) + \frac{1}{2D}\Delta I_L\left(\frac{2}{3}-D\right)$ |
| $i_{AN}(DT_s) = I_{14}\left(\frac{1}{3}-D\right) + \frac{1}{2}\Delta I_L$ | $i_{AN}\left(\left(D-\frac{1}{3}\right)T_s\right) = I_{14}\left(\frac{2}{3}-D\right) + \frac{1}{D}\Delta I_L\left(D-\frac{1}{3}\right)$ |
| $i_{BN}(DT_s) = I_{14}D$ | $i_{BN}\left(\left(D-\frac{1}{3}\right)T_s\right) = I_{14}\left(\frac{1}{3}-D\right) - \frac{1}{2D}\Delta I_L\left(\frac{2}{3}-D\right)$ |
| $t_1 = \frac{1}{2}DT_s - \frac{I_{14}}{\Delta I_L}\left(\frac{1}{3}-D\right)DT_s$ | $t_1 = \frac{1}{2}\left(D-\frac{1}{3}\right)T_s - \frac{1}{2}\frac{I_{14}}{\Delta I_L}\left(\frac{2}{3}-D\right)DT_s$ |
| | $t_2 = \frac{1}{2}DT_s - \frac{I_{14}}{\Delta I_L}\left(\frac{1}{3}-D\right)DT_s$ |

| 3-phase<br>$\frac{2}{3} < D \leq 1$<br>$n$ =3, $N$ = 3 |
|---|
| $i_{XN}(0) = I_{14}(1-D) - \frac{3}{2}\frac{1}{D}\Delta I_L\left(D-\frac{2}{3}\right)$ |
| $i_{YN}\left(\frac{T_s}{3}\right) = I_{14}\left(\frac{2}{3}-D\right) + \frac{1}{D}\Delta I_L(1-D)$ |
| $i_{AN}\left(\left(D-\frac{2}{3}\right)T_s\right) = I_{14}(1-D) + \frac{3}{2}\frac{1}{D}\Delta I_L\left(D-\frac{2}{3}\right)$ |
| $i_{BN}\left(\left(D-\frac{2}{3}\right)T_s\right) = I_{14}\left(\frac{2}{3}-D\right) - \frac{1}{D}\Delta I_L(1-D)$ |
| $t_1 = \frac{1}{2}\left(D-\frac{2}{3}\right)T_s - \frac{1}{3}\frac{I_{14}}{\Delta I_L}(1-D)DT_s$ |
| $t_2 = \frac{1}{2}\left(D-\frac{1}{3}\right)T_s - \frac{1}{2}\frac{I_{14}}{\Delta I_L}\left(\frac{2}{3}-D\right)DT_s$ |

Considering the above equations, the general equations can be determined using the variables $n$ and $N$. $N$ is the number of phases and $n$ is an integer who's value depends on the number of phases and the duty cycle.

For $N$-phases, the 6 equations can be written as:

$$i_{XN}(0) = I_{14}\left(\frac{n}{N}-D\right) - \frac{n}{2D}\Delta I_L\left(D-\frac{n-1}{N}\right) \tag{A.18}$$

$$i_{YN}\left(\frac{T_s}{N}\right) = I_{14}\left(\frac{n-1}{N}-D\right) - \frac{n-1}{2D}\Delta I_L\left(D-\frac{n}{N}\right) \tag{A.19}$$

$$i_{AN}\left(\left(D-\frac{n-1}{N}\right)T_s\right) = I_{14}\left(\frac{n}{N}-D\right) + \frac{n}{2D}\Delta I_L\left(D-\frac{n-1}{N}\right) \tag{A.20}$$

$$i_{BN}\left(\left(D-\frac{n-1}{N}\right)T_s\right) = I_{14}\left(\frac{n-1}{N}-D\right) + \frac{n-1}{2D}\Delta I_L\left(D-\frac{n}{N}\right) \tag{A.21}$$

$$t_{1N} = \frac{1}{2}\left(D-\frac{n-1}{N}\right)T_s - \frac{1}{n}\frac{I_{14}}{\Delta I_L}\left(\frac{n}{N}-D\right)DT_s \tag{A.22}$$

$$t_{2N} = \frac{1}{2}\left(D-\frac{n-2}{N}\right)T_s - \frac{1}{n-1}\frac{I_{14}}{\Delta I_L}\left(\frac{n-1}{N}-D\right)DT_s \tag{A.23}$$

where $n$=*1,2,..,N* and $\frac{n-1}{N} < D \leq \frac{n}{N}$.

Using Figure A.2 and equations A.18 to A.23, the maximum charge that must be stored in the capacitor, and the total charge being processed by the capacitor can be calculated. In Figure

A.2, there are 4 different waveforms, thus the charge calculations will also have 4 equations. Different equations will be used over the duty cycle range depending on the capacitor current waveform. Two points in Figure A.2 can be used to determine in which mode the current waveform is. Let these two points be point $i_{XN}(0)$ and point $i_{YN}(T_S/N)$.

If $\boldsymbol{i_{XN}(0) \geq 0}$ **and** $\boldsymbol{i_{YN}(T_S/N) \leq 0}$, then the charge can be calculated as the area under the current when the current is flowing into the capacitor:

$$Q_{\max\_C_{42}} = \left( i_{XN}(0) + \tfrac{1}{2}\left( i_{AN}\left( \left( D - \frac{n-1}{N} \right) T_s \right) - i_{XN}(0) \right) \right) \left( D - \frac{n-1}{N} \right) T_s \tag{A.24}$$

which simplifies to:

$$Q_{\max\_C_{42}} = I_{14} T_s \left( \frac{n}{N} - D \right) \left( D - \frac{n-1}{N} \right) \tag{A.25}$$

The total charge processed by the capacitor in one switching period in this mode is $N$ times that being stored:

$$Q_{processed\_C_{42}} = N I_{14} T_s \left( \frac{n}{N} - D \right) \left( D - \frac{n-1}{N} \right) \tag{A.26}$$

If $\boldsymbol{i_{XN}(0) \geq 0}$ and $\boldsymbol{i_{YN}(T_S/N) > 0}$, then the charge can be calculated as the area under the current when the current is flowing out of the capacitor (this area is chosen because it is easier to calculate and over one period the charge flowing into the capacitor is equal to the charge flowing out):

$$Q_{\max\_C_{42}} = \tfrac{1}{2} i_{BN} \left( \left( D - \frac{n-1}{N} \right) T_s \right) \cdot \left( t_{2N} - \left( D - \frac{n-1}{N} \right) T_s \right) \tag{A.27}$$

which simplifies to:

$$Q_{\max\_C_{42}} = \tfrac{1}{2} T_s \left[ I_{14} \left( \tfrac{n}{N} - D \right) \left( D - \tfrac{n-1}{N} \right) + \tfrac{n-1}{4D} \Delta I_L \left( D - \tfrac{n}{N} \right)^2 + \tfrac{D}{n-1} \tfrac{I_{14}^2}{\Delta I_L} \left( D - \tfrac{n-1}{N} \right)^2 \right] \tag{A.28}$$

The total charge processed by the capacitor in one switching period in this mode is $N$ times that being stored:

$$Q_{processed\_C_{42}} = \tfrac{1}{2} N T_s \left[ I_{14} \left( \tfrac{n}{N} - D \right) \left( D - \tfrac{n-1}{N} \right) + \tfrac{n-1}{4D} \Delta I_L \left( D - \tfrac{n}{N} \right)^2 + \tfrac{D}{n-1} \tfrac{I_{14}^2}{\Delta I_L} \left( D - \tfrac{n-1}{N} \right)^2 \right] \tag{A.29}$$

If $\boldsymbol{i_{XN}(0) < 0}$ and $\boldsymbol{i_{YN}(T_S/N) \leq 0}$, then the charge can be calculated as the area under the current waveform when the current is flowing into the capacitor:

$$Q_{\max\_C_{42}} = \tfrac{1}{2} i_{AN} \left( \left( D - \frac{n-1}{N} \right) T_s \right) \cdot \left( \left( D - \frac{n-1}{N} \right) T_s - t_{1N} \right) \tag{A.30}$$

which simplifies to:

$$Q_{\max\_C_{42}} = \tfrac{1}{2} T_s \left[ I_{14} \left( \frac{n}{N} - D \right) \left( D - \frac{n-1}{N} \right) + \frac{n}{4D} \Delta I_L \left( D - \frac{n-1}{N} \right)^2 + \frac{D}{n} \frac{I_{14}^2}{\Delta I_L} \left( D - \frac{n}{N} \right)^2 \right] \tag{A.31}$$

The total charge processed by the capacitor in this particular mode is $N$ times that being stored:

$$Q_{processed\_C_{42}} = \tfrac{1}{2} N T_s \left[ I_{14} \left( \frac{n}{N} - D \right) \left( D - \frac{n-1}{N} \right) + \frac{n}{4D} \Delta I_L \left( D - \frac{n-1}{N} \right)^2 + \frac{D}{n} \frac{I_{14}^2}{\Delta I_L} \left( D - \frac{n}{N} \right)^2 \right] \tag{A.32}$$

And lastly, if $\boldsymbol{i_{XN}(0) < 0}$ and $\boldsymbol{i_{YN}(T_S/N) > 0}$, then the charge is stored in the capacitor over two periods. The charge is each period can be calculated as:

$$Q_{\max C_{42}\_period1} = \tfrac{1}{2} i_{AN} \left( \left( D - \frac{n-1}{N} \right) T_s \right) \cdot \left( \left( D - \frac{n-1}{N} \right) T_s - t_{1N} \right) \tag{A.33}$$

and

$$Q_{\max\_C_{42}\_period2} = \tfrac{1}{2} i_{YN} \left( \frac{T_n}{N} \right) \cdot \left( \frac{T_n}{N} - \left( D - \frac{n-1}{N} \right) T_s \right) \tag{A.34}$$

The maximum of the two stored charges is taken as the maximum charge that must be stored in the capacitor:

$$Q_{\max\_C_{42}} = \max \begin{cases} \tfrac{1}{2} T_s \left[ I_{14} \left( \frac{n}{N} - D \right) \left( D - \frac{n-1}{N} \right) + \frac{n}{4D} \Delta I_L \left( D - \frac{n-1}{N} \right)^2 + \frac{D}{n} \frac{I_{14}^2}{\Delta I_L} \left( D - \frac{n}{N} \right)^2 \right] \\ \tfrac{1}{2} T_s \left[ I_{14} \left( \frac{n}{N} - D \right) \left( \frac{n-1}{N} - D \right) + \frac{n-1}{4D} \Delta I_L \left( D - \frac{n}{N} \right)^2 + \frac{D}{n-1} \frac{I_{14}^2}{\Delta I_L} \left( D - \frac{n-1}{N} \right)^2 \right] \end{cases} \tag{A.35}$$

The total charge processed by the capacitor in this particular mode is $N$ times the sum of the charge in the two intervals:

$$Q_{processed\_C_{42}} = \tfrac{1}{2} N T_s \left[ \frac{\Delta I_L}{4D} \left( n \left( D - \frac{n-1}{N} \right)^2 + (n-1) \left( D - \frac{n}{N} \right)^2 \right) + \frac{I_{14}^2 D}{\Delta I_L} \left( \frac{1}{n} \left( D - \frac{n}{N} \right)^2 + \left( \frac{1}{n-1} \right) \left( D - \frac{n-1}{N} \right)^2 \right) \right] \tag{A.36}$$

To complete the charge analysis, the conditions that must be met for $i_{XN}(0)$ and $i_{YN}(T_s/N)$ must be determined.

Considering the general expression for $i_{XN}(0)$, $i_{XN}(0)$ is larger than zero if:

$$I_{14}\left(\tfrac{n}{N}-D\right)\geq \tfrac{n}{2D}\Delta I_L\left(D-\tfrac{n-1}{N}\right) \tag{A.37}$$

and $i_{YN}(T_s/N)$ is smaller than zero if:

$$I_{14}\left(\tfrac{n-1}{N}-D\right)\leq \tfrac{n-1}{2D}\Delta I_L\left(D-\tfrac{n}{N}\right) \tag{A.38}$$

The complete equation describing the maximum charge stored in $C_{42}$ is:

$$Q_{\max\_C_{42}}=\begin{cases} if\, I_{14}\left(\tfrac{n}{N}-D\right)\geq \tfrac{n}{2D}\Delta I_L\left(D-\tfrac{n-1}{N}\right) & \\ \quad \begin{cases} I_{14}T_s\left(\tfrac{n}{N}-D\right)\left(D-\tfrac{n-1}{N}\right) & if\ I_{14}\left(\tfrac{n-1}{N}-D\right)\leq \tfrac{n-1}{2D}\Delta I_L\left(D-\tfrac{n}{N}\right) \\ \tfrac{1}{2}T_s\left[I_{14}\left(\tfrac{n}{N}-D\right)\left(D-\tfrac{n-1}{N}\right)+\tfrac{n-1}{4D}\Delta I_L\left(D-\tfrac{n}{N}\right)^2+\tfrac{1}{n-1}\tfrac{I_{14}^2}{\Delta I_L}\left(D-\tfrac{n-1}{N}\right)^2D\right] & otherwise \end{cases} \\ if\, I_{14}\left(\tfrac{n}{N}-D\right)<\tfrac{n}{2D}\Delta I_L\left(D-\tfrac{n-1}{N}\right) & \\ \quad \begin{cases} \tfrac{1}{2}T_s\left[I_{14}\left(\tfrac{n}{N}-D\right)\left(D-\tfrac{n-1}{N}\right)+\tfrac{n}{4D}\Delta I_L\left(D-\tfrac{n-1}{N}\right)^2+\tfrac{1}{n}\tfrac{I_{14}^2}{\Delta I_L}\left(D-\tfrac{n}{N}\right)^2D\right] & if\ I_{14}\left(\tfrac{n-1}{N}-D\right)\leq \tfrac{n-1}{2D}\Delta I_L\left(D-\tfrac{n}{N}\right) \\ \max\left\{\begin{array}{l}\tfrac{1}{2}T_s\left[I_{14}\left(\tfrac{n}{N}-D\right)\left(D-\tfrac{n-1}{N}\right)+\tfrac{n}{4D}\Delta I_L\left(D-\tfrac{n-1}{N}\right)^2+\tfrac{1}{n}\tfrac{I_{14}^2}{\Delta I_L}\left(D-\tfrac{n}{N}\right)^2D\right] \\ \tfrac{1}{2}T_s\left[I_{14}\left(\tfrac{n}{N}-D\right)\left(\tfrac{n-1}{N}-D\right)+\tfrac{n-1}{4D}\Delta I_L\left(D-\tfrac{n}{N}\right)^2+\tfrac{1}{n-1}\tfrac{I_{14}^2}{\Delta I_L}\left(D-\tfrac{n-1}{N}\right)^2D\right]\end{array}\right\} & otherwise \end{cases} \end{cases} \tag{A.39}$$

where $Q_{max\_C42}$ is the maximum charge that must be stored in $C_{42}$ [C]
and where $n=1,2,..,N$ and $\tfrac{n-1}{N}<D\leq\tfrac{n}{N}$.

The total charge that is processed by the capacitor is:

$$Q_{processed\_C_{42}}=\begin{cases} if\ I_{14}\left(\tfrac{n}{N}-D\right)\geq \tfrac{n}{2D}\Delta I_L\left(D-\tfrac{n-1}{N}\right) & \\ \quad \begin{cases} NI_{14}T_s\left(\tfrac{n}{N}-D\right)\left(D-\tfrac{n-1}{N}\right) & if\ \ I_{14}\left(\tfrac{n-1}{N}-D\right)\leq \tfrac{n-1}{2D}\Delta I_L\left(D-\tfrac{n}{N}\right) \\ \tfrac{1}{2}NT_s\left[I_{14}\left(\tfrac{n}{N}-D\right)\left(D-\tfrac{n-1}{N}\right)+\tfrac{n-1}{4D}\Delta I_L\left(D-\tfrac{n}{N}\right)^2+\tfrac{1}{n-1}\tfrac{I_{14}^2}{\Delta I_L}\left(D-\tfrac{n-1}{N}\right)^2D\right] & otherwise \end{cases} \\ if\ I_{14}\left(\tfrac{n}{N}-D\right)<\tfrac{n}{2D}\Delta I_L\left(D-\tfrac{n-1}{N}\right) & \\ \quad \begin{cases} \tfrac{1}{2}NT_s\left[I_{14}\left(\tfrac{n}{N}-D\right)\left(D-\tfrac{n-1}{N}\right)+\tfrac{n}{4D}\Delta I_L\left(D-\tfrac{n-1}{N}\right)^2+\tfrac{1}{n}\tfrac{I_{14}^2}{\Delta I_L}\left(D-\tfrac{n}{N}\right)^2D\right] & if\ \ I_{14}\left(\tfrac{n-1}{N}-D\right)\leq \tfrac{n-1}{2D}\Delta I_L\left(D-\tfrac{n}{N}\right) \\ \tfrac{1}{2}NT_s\left[\tfrac{1}{4D}\Delta I_L\left(n\left(D-\tfrac{n-1}{N}\right)^2+(n-1)\left(D-\tfrac{n}{N}\right)^2\right)+\tfrac{I_{14}^2}{\Delta I_L}\left(\tfrac{1}{n}\left(D-\tfrac{n}{N}\right)^2+\left(\tfrac{1}{n-1}\right)\left(D-\tfrac{n-1}{N}\right)^2\right)D\right] & otherwise \end{cases} \end{cases} \tag{A.40}$$

where $Q_{processed\_C42}$ is the total charge processed by $C_{42}$ in one switching period [C]
and where $n=1,2,..,N$ and $\tfrac{n-1}{N}<D\leq\tfrac{n}{N}$.

To determine the maximum energy in the capacitor, the capacitance for a given voltage ripple must be determined as a function of the number of phases and duty cycle. Defining the allowable voltage ripple as:

$$\Delta V_{42}=0.01V_{42} \tag{A.41}$$

where $\Delta V_{42}$ is the allowable voltage ripple on the bus voltage [V].

The capacitance required for the given voltage ripple is then:

$$C = \frac{Q_{\max\_C_{42}}}{\Delta V_{42}} \tag{A.42}$$

where $C$ is the required capacitance [F].

The maximum energy that must be stored in the capacitor is then given as:

$$E_{\max\_C_{42}} = \frac{1}{2}\frac{Q_{N\_C_{42}}}{\Delta V_{42}} V_{42}^2 \tag{A.43}$$

where $E_{max\_C42}$ is the maximum energy stored in the capacitor [J],
$\Delta V_{42}$ is the required voltage ripple [V]
and $V_{42}$ is the voltage across the capacitor [V].

The energy processed by the capacitor is determined from the charge that is processed by the capacitor. The energy processed by the capacitor is determined from the product of the voltage across the capacitor and the charge flowing through the capacitor in one switching cycle:

$$E_{processed\_C_{42}} = V_{42} \cdot Q_{processed\_C_{42}} \tag{A.44}$$

where $E_{processed\_C42}$ is the energy processed by the capacitor in one switching period [J],
$Q_{processed\_C42}$ is the charge processed by the capacitor [C]
and $V_{42}$ is the voltage across the capacitor [V].

## 4. Energy stored in $C_{14}$ as a function of the number of phases

The energy stored and processed by $C_{14}$ can be determined in a similar way as for $C_{42}$ from Figure A.3. The current waveform is used to determine the charge stored and processed by the capacitor. For a given voltage ripple, the required capacitance can be found and finally the energy stored in the capacitor can be determined. The current waveform in the capacitor is repeated every $T_s/N$ seconds and the waveform always has the same shape. Only the amplitude of the waveforms will change as the duty cycle changes for a given number of phases.

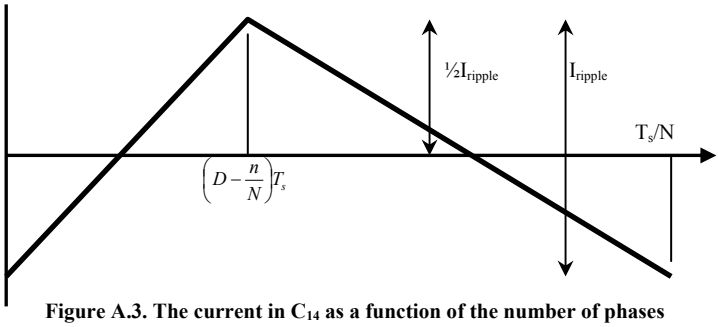



**Figure A.3. The current in $C_{14}$ as a function of the number of phases**

The charge stored in the capacitor is determined from the area under the current waveform when the current is positive. The capacitor stores charge when the current is positive and returns charge when the current is negative. To determine the time that the current is positive for it is noted that the average current in the capacitor must be zero. Thus the current waveform is positive for half of the period and negative for the other half of the period. Thus the charge stored in the capacitor is:

$$Q_{\max\_C_{14}} = \frac{1}{8}\frac{T_s}{N} I_{ripple} \tag{A.45}$$

where $Q_{max\_C14}$ is the charge stored in the capacitor [C]
and $I_{ripple}$ is the current ripple in $C_{14}$ and is:

$$I_{ripple} = \frac{NV_{42}T_s}{L}\left(D - \frac{n-1}{N}\right)\left(\frac{n}{N} - D\right) \qquad \frac{n-1}{N} < D \le \frac{n}{N} \tag{A.46}$$

which can be reduced to:

$$Q_{\max\_C_{14}} = \frac{V_{42}T_s^2}{8L}\left(D - \frac{n-1}{N}\right)\left(\frac{n}{N} - D\right) \qquad \frac{n-1}{N} < D \le \frac{n}{N} \tag{A.47}$$

where $L$ is the inductance [H]
$N$ is the number of phases,
and where $n=1,2,..,N$ and $\frac{n-1}{N} < D \le \frac{n}{N}$.

To determine the maximum energy in the capacitor, the capacitance for a given voltage ripple must be determined as a function of the number of phases and duty cycle. Defining the allowable voltage ripple as:

$$\Delta V_{14} = 0.01 V_{14} \tag{A.48}$$

where $\Delta V_{14}$ is the allowable voltage ripple on the bus voltage [V].

The capacitance required for the given voltage ripple is then:

$$C = \frac{Q_{N\_C_{14}}}{\Delta V_{14}} \tag{A.49}$$

where $C$ is the required capacitance [F].

The maximum energy that must be stored in the capacitor is then given as:

$$E_{\max\_C_{14}} = \frac{1}{2}\frac{Q_{\max\_C_{14}}}{\Delta V_{14}} V_{14}^2 \tag{A.50}$$

where $E_{max\_C14}$ is the maximum energy stored in the capacitor [J],

$\Delta V_{14}$ is the required voltage ripple [V]
and $V_{14}$ is the voltage across the capacitor [V].

The charge processed by the capacitor over one switching cycle is $N$ times the charge stored in the capacitor because the capacitor current has a frequency $N$ times higher that that of the phase switching frequency. The energy processed by the capacitor is then determined from the product of the voltage across the capacitor and the charge flowing through the capacitor in one switching cycle:

$$E_{processed\_C_{14}} = V_{14} \cdot N \cdot Q_{\max\_C_{14}} \tag{A.51}$$

which can be rewritten as:

$$E_{processed\_C_{14}} = \frac{NDV_{42}^2 T_s^2}{8L}\left(D - \frac{n-1}{N}\right)\left(\frac{n}{N} - D\right) \qquad \frac{n-1}{N} < D \le \frac{n}{N} \tag{A.52}$$

where $E_{processed\_C14}$ is the energy processed by the capacitor in one switching period [J]
and where $n=1,2,..,N$ and $\frac{n-1}{N} < D \le \frac{n}{N}$.

# Appendix B

## RMS CURRENTS IN THE SYNCHRONOUS RECTIFIER

## 1. Introduction

In this appendix, the RMS current in the passive components is calculated as function of the number of implemented phases. This is accomplished by calculating the RMS currents in the passive components for 1-, 2- and 3-phases and then generalising the equations for *N*-phases.

## 2. RMS current in $C_{42}$

The RMS current in $C_{42}$ is considered first.

### 2.1 RMS current in $C_{42}$ for a single-phase

Figure B.1 shows the current in the 42V capacitor, $i_{C42}(t)$. This current has the same shape as the current in $SW_1$ but has an off-set of $-I_{42}$. Further, let $T_s$ be the switching period, $D$ the duty cycle varying between 0 and 1 and let $\Delta I_L$ be the current ripple defined by the inductance, $L$. Then the current in the capacitor can be represented piecewise as:

$$i_{C42}(t) = \begin{cases} \dfrac{I_{42}}{D} + \dfrac{V_{42}(1-D)}{L}\left(t - \frac{1}{2}DT_s\right) & 0 < t \le DT_s \\ -I_{42} & DT_s < t \le T_s \end{cases} \tag{B.1}$$

The RMS current can be calculated as:

$$I^2_{C_{42}\_RMS} = \frac{1}{T_s}\left[\int_0^{DT_s}\left(\frac{I_{42}}{D} + \frac{V_{42}(1-D)}{L}\left(t - \frac{1}{2}DT_s\right)\right)^2 dt + \int_{DT_s}^{T_s}(-I_{42})^2 dt\right] \tag{B.2}$$

Performing the integration:

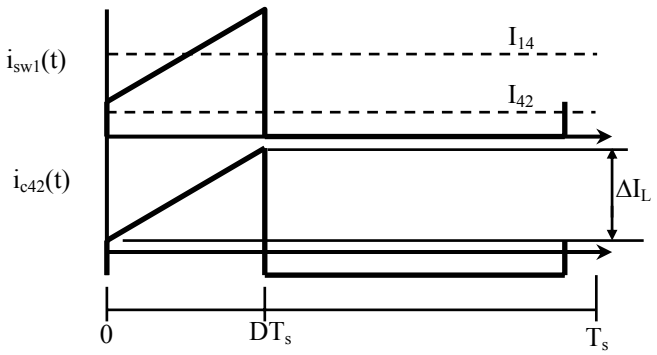



**Figure B.1. The current in $C_{42}$ for a single-phase topology**

$$I_{C_{42}\_RMS} = \sqrt{I_{42}^2 \frac{1-D}{D} + \left(\frac{V_{42}(1-D)DT_s}{L}\right)^2 \frac{D}{12}} \qquad \text{for } 0 < D \le 1 \qquad \text{(B.3)}$$

where $I_{C42\_RMS}$ is the RMS current in $C_{42}$ for a single phase [A].

### 2.2 RMS current in $C_{42}$ for two-phases

The RMS current in $C_{42}$ for two-phases is calculated in two separate intervals because the current in the capacitor has different waveforms for the duty cycle above and below 50%.

#### *2.2.1 $C_{42}$ RMS current for D<0.5*

Figure B.2 shows the current in the MOSFET $SW_1$ for both phases. These two currents combine to form the capacitor current.

The current in $C_{42}$ can be represented as:

$$i_{C_{42}}(t) = \begin{cases} \frac{I_{42}(1-2D)}{2D} + \frac{V_{42}(1-D)}{L}\left(t - \frac{1}{2}DT_s\right) & 0 < t \le DT_s \\ -I_{42} & DT_s < t \le \frac{1}{2}T_s \end{cases} \qquad \text{(B.4)}$$

The RMS current can be calculated from:

$$I_{C_{42}\_RMS}^2 = \frac{2}{T_s}\left[\int_0^{DT_s}\left(\frac{I_{42}(1-2D)}{2D} + \frac{V_{42}(1-D)}{L}\left(t - \frac{1}{2}DT_s\right)\right)^2 dt + \int_{DT_s}^{\frac{1}{2}T_s}(-I_{42})^2 dt\right] \qquad \text{(B.5)}$$

Performing the integration yields:

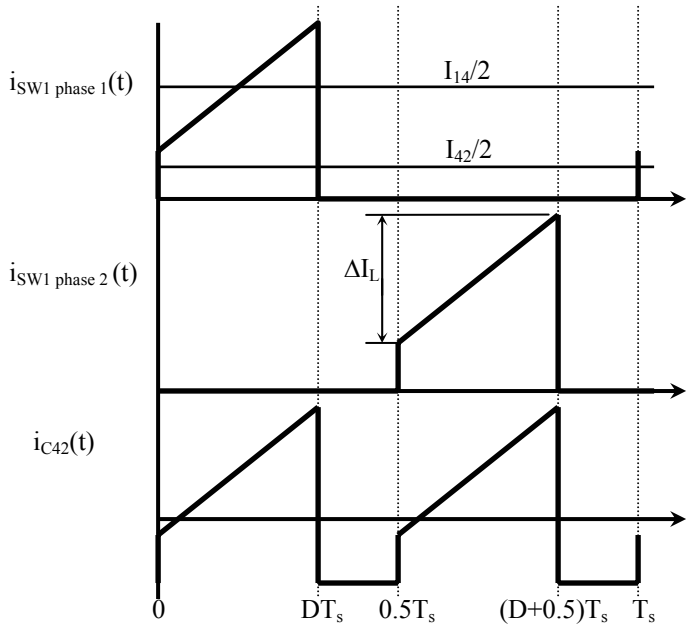



**Figure B.2. The current in $SW_1$ for both phases and the resulting current in $C_{42}$ for D<0.5**

$$I_{C_{42}\_RMS} = \sqrt{I_{42}^2 \frac{\frac{1}{2}-D}{D} + \frac{2D}{12}\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2} \qquad \text{for } 0 < D < \frac{1}{2} \tag{B.6}$$

### 2.2.2 $C_{42}$ RMS current for D≥0.5

Figure B.3 shows the current in $SW_1$ for both phases and the current in $C_{42}$ for a duty cycle larger than 50%.

The current in the capacitor can be described piecewise as:

$$i_{C_{42}}(t) = \begin{cases} I_{42}\frac{1-D}{D} + \frac{V_{42}(1-D)}{L}\left(2t + \left(\frac{1}{2}-D\right)T_s\right) & \text{for } 0 < t \le \left(D-\frac{1}{2}\right)T_s \\ I_{42}\frac{\frac{1}{2}-D}{D} + \frac{V_{42}(1-D)}{L}\left(t - \left(D-\frac{1}{2}\right)T_s\right) & \text{for } \left(D-\frac{1}{2}\right)T_s < t \le \frac{T_s}{2} \end{cases} \tag{B.7}$$

The RMS current is calculated from:

$$I_{C_{42}\_RMS}^2 = \frac{2}{T_s}\left[\begin{array}{l} \left\{\int_0^{\left(D-\frac{1}{2}\right)T_s}\left(\frac{I_{42}(1-D)}{D} + \frac{V_{42}(1-D)}{L}\left(2t + \left(\frac{1}{2}-D\right)T_s\right)\right)^2 dt\right\} + \\ \left\{\int_{\left(D-\frac{1}{2}\right)T_s}^{\frac{T_s}{2}}\left(\frac{I_{42}\left(\frac{1}{2}-D\right)}{D} + \frac{V_{42}(1-D)}{L}\left(t - \left(D-\frac{1}{2}\right)T_s\right)\right)^2 dt\right\} \end{array}\right] \tag{B.8}$$

which reduces to:

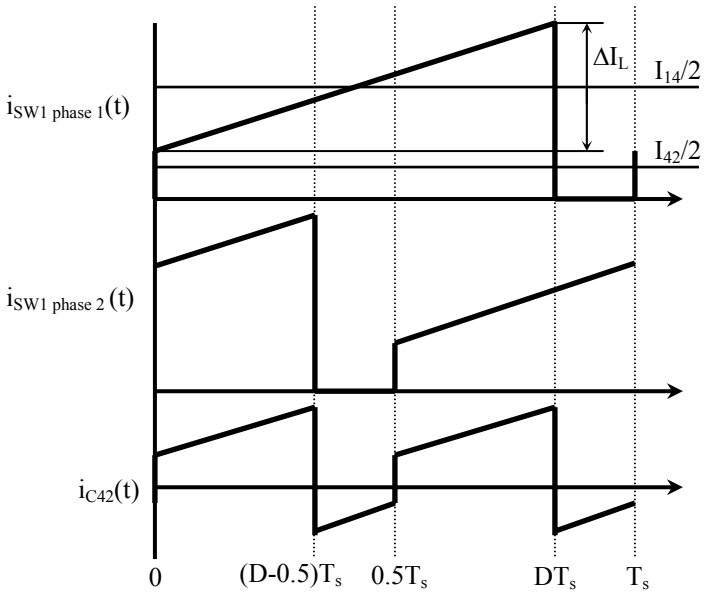



**Figure B.3. The current in $SW_1$ for both phases and the resulting current in $C_{42}$ for D≥0.5**

$$I_{C_{42}\_RMS} = \sqrt{I_{42}^2\left(\frac{D-\frac{1}{2}}{D}\right)\left(\frac{1-D}{D}\right)+\left(\frac{V_{42}(1-D)T_s}{L}\right)^2\frac{2}{12}\left(4\left(D-\frac{1}{2}\right)^3+(1-D)^3\right)} \quad \text{(B.9)}$$

for $0.5 > D \geq 1$.

### 2.3 RMS current in $C_{42}$ for three-phases

The RMS current in $C_{42}$ for three-phases is calculated in three separate intervals because the current in the capacitor has different waveforms for $0 < D \leq \frac{1}{3}$, $\frac{1}{3} < D \leq \frac{2}{3}$ and $\frac{2}{3} < D \leq 1$.

#### *2.3.1 $C_{42}$ RMS current for D≤1/3*

Figure B.4 shows the currents in $SW_1$ for the three phases and the resulting current in the 42V capacitor for the three phase system.

The current in the capacitor can be described piecewise as:

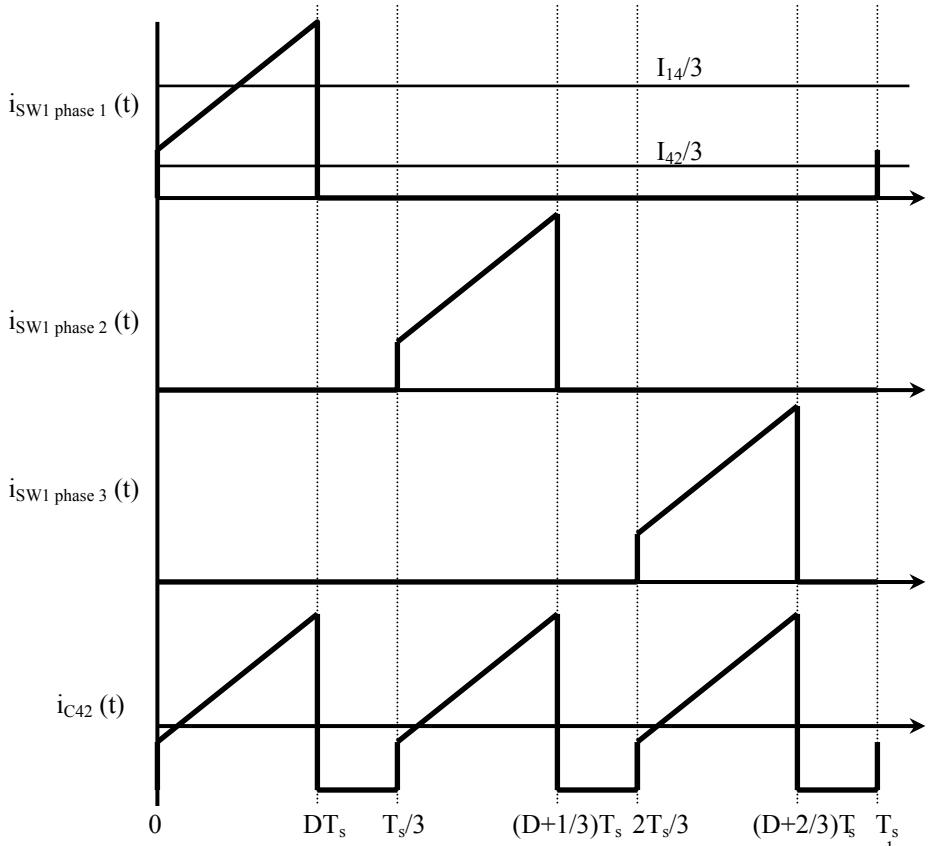



**Figure B.4. The current in $SW_1$ for both phases and the resulting current in $C_{42}$ for $0 < D \leq \frac{1}{3}$**

$$i_{C_{42}}(t)=\begin{cases} I_{42}\left(\dfrac{1-3D}{3D}\right)+\dfrac{V_{42}(1-D)}{L}\left(t-\dfrac{1}{2}DT_s\right) & \text{for } 0<t\le DT_s \\ -I_{42} & \text{for } DT_s<t\le \dfrac{1}{3}T_s \end{cases} \qquad \text{(B.10)}$$

Taking the RMS:

$$I^2_{C_{42}\_RMS}=\frac{3}{T_s}\left[\int_0^{DT_s}\left(\frac{I_{42}(1-3D)}{3D}+\frac{V_{42}(1-D)}{L}\left(t-\tfrac{1}{2}DT_s\right)\right)^2 dt+\int_{DT_s}^{\frac{1}{2}T_s}(-I_{42})^2\,dt\right] \qquad \text{(B.11)}$$

performing the integration yields:

$$I_{C_{42}\_RMS}=\sqrt{I^2_{42}\left(\frac{\frac{1}{3}-D}{D}\right)+\left(\frac{V_{42}(1-D)DT_2}{L}\right)^2\frac{3D}{12}} \qquad \text{for } 0<D\le\frac{1}{3} \qquad \text{(B.12)}$$

### *2.3.2 $C_{42}$ RMS current for 1/3<D≤2/3*

Figure B.5 shows the $SW_1$ and capacitor currents for a three-phase system for $\frac{1}{3}<D\le\frac{2}{3}$.

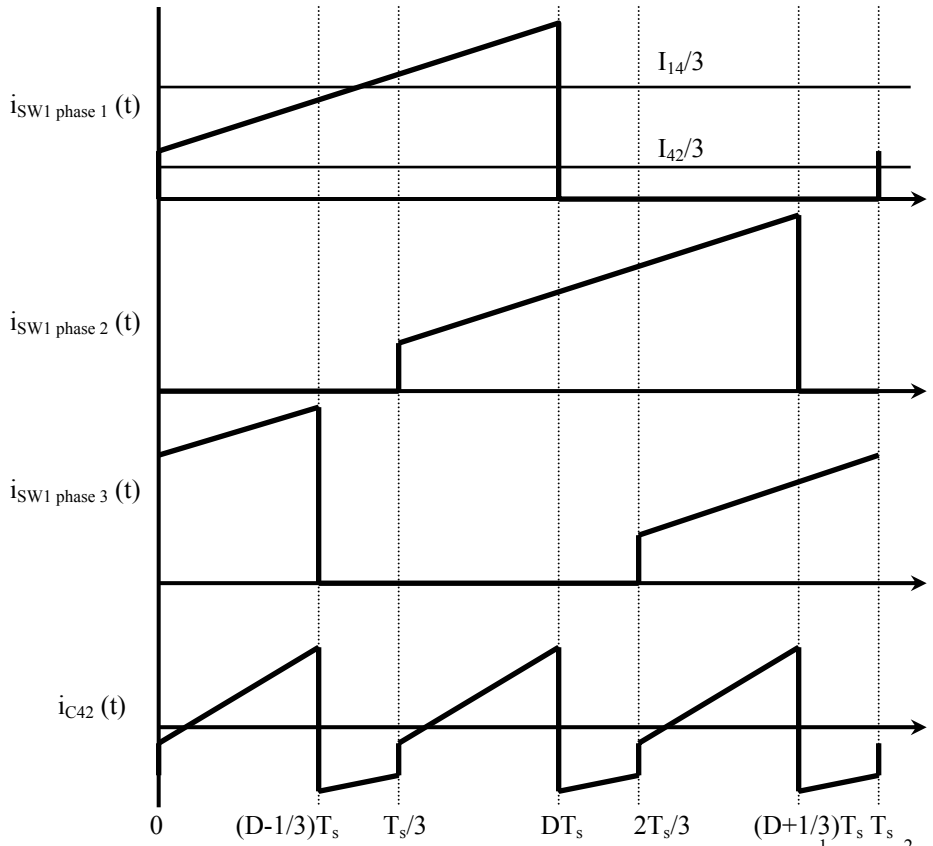



**Figure B.5 The currents in $SW_1$ and the 42V capacitor for a three-phase system with $\frac{1}{3}<D\le\frac{2}{3}$**

The current in the capacitor can be described as:

$$i_{C_{42}}(t)=\begin{cases} I_{42}\left(\frac{2-3D}{3D}\right)+\frac{V_{42}(1-D)}{L}\left(2t+\left(\frac{1}{3}-D\right)T_s\right) & \text{for } 0<t\le\left(D-\frac{1}{3}\right)T_s \\ I_{42}\left(\frac{1-3D}{3D}\right)+\frac{V_{42}(1-D)}{L}\left(\frac{1}{2}\left(D-\frac{2}{3}\right)T_s+\left(t-\left(D-\frac{1}{3}\right)T_s\right)\right) & \text{for } \left(D-\frac{1}{3}\right)T_s<t\le\frac{1}{3}T_s \end{cases} \quad \text{(B.13)}$$

The RMS current is calculated from:

$$I^2_{C_{42}\_RMS}=\frac{3}{T_s}\left[\begin{array}{l}\left\{\int_0^{\left(D-\frac{1}{3}\right)T_s}\left(I_{42}\left(\frac{2-3D}{3D}\right)+\frac{V_{42}(1-D)}{L}\left(2t+\left(\frac{1}{3}-D\right)T_s\right)\right)^2 dt\right\}+ \\ \left\{\int_{\left(D-\frac{1}{3}\right)T_s}^{\frac{T_s}{3}}\left(I_{42}\left(\frac{1-3D}{3D}\right)+\frac{V_{42}(1-D)}{L}\left(\frac{1}{2}\left(D-\frac{2}{3}\right)T_s+\left(t-\left(D-\frac{1}{3}\right)T_s\right)\right)\right)^2 dt\right\}\end{array}\right] \quad \text{(B.14)}$$

which can be simplified to:

$$I_{C_{42}\_RMS}=\sqrt{I^2_{42}\left(\frac{\frac{2}{3}-D}{D}\right)\left(\frac{D-\frac{1}{3}}{D}\right)+\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2\frac{3}{12}\left[\left(\frac{2}{3}-D\right)^3+4\left(D-\frac{1}{3}\right)^3\right]} \quad \text{for } \frac{1}{3}<D\le\frac{2}{3} \quad \text{(B.15)}$$

### *2.3.3 $C_{42}$ RMS current for 2/3>D≥1*

Figure B.6 shows the currents in $SW_1$ and the resulting current in the capacitor for a three-phase system.

The current in the capacitor can be described piecewise as:

$$i_{C_{42}}(t)=\begin{cases} I_{42}\left(\frac{1-D}{D}\right)+\frac{V_{42}(1-D)}{L}\left(3t+\frac{3}{2}\left(\frac{2}{3}-D\right)T_s\right) & \text{for } 0<t\le\left(D-\frac{2}{3}\right)T_s \\ I_{42}\left(\frac{\frac{2}{3}-D}{D}\right)+\frac{V_{42}(1-D)}{L}\left(2\left(t-\left(D-\frac{2}{3}\right)T_s\right)+(D-1)T_s\right) & \text{for } \left(D-\frac{2}{3}\right)T_s<t\le\frac{1}{3}T_s \end{cases} \quad \text{(B.16)}$$

The RMS current is calculated from:

$$I^2_{C_{42}\_RMS}=\frac{3}{T_s}\left[\begin{array}{l}\left\{\int_0^{\left(D-\frac{1}{3}\right)T_s}\left(I_{42}\left(\frac{1-D}{D}\right)+\frac{V_{42}(1-D)}{L}\left(3t+\frac{3}{2}\left(\frac{2}{3}-D\right)T_s\right)\right)^2 dt\right\}+ \\ \left\{\int_{\left(D-\frac{1}{3}\right)T_s}^{\frac{T_s}{3}}\left(I_{42}\left(\frac{\frac{2}{3}-D}{D}\right)+\frac{V_{42}(1-D)}{L}\left(2\left(t-\left(D-\frac{2}{3}\right)T_s\right)+(D-1)T_s\right)\right)^2 dt\right\}\end{array}\right] \quad \text{(B.17)}$$

which can be simplified to:

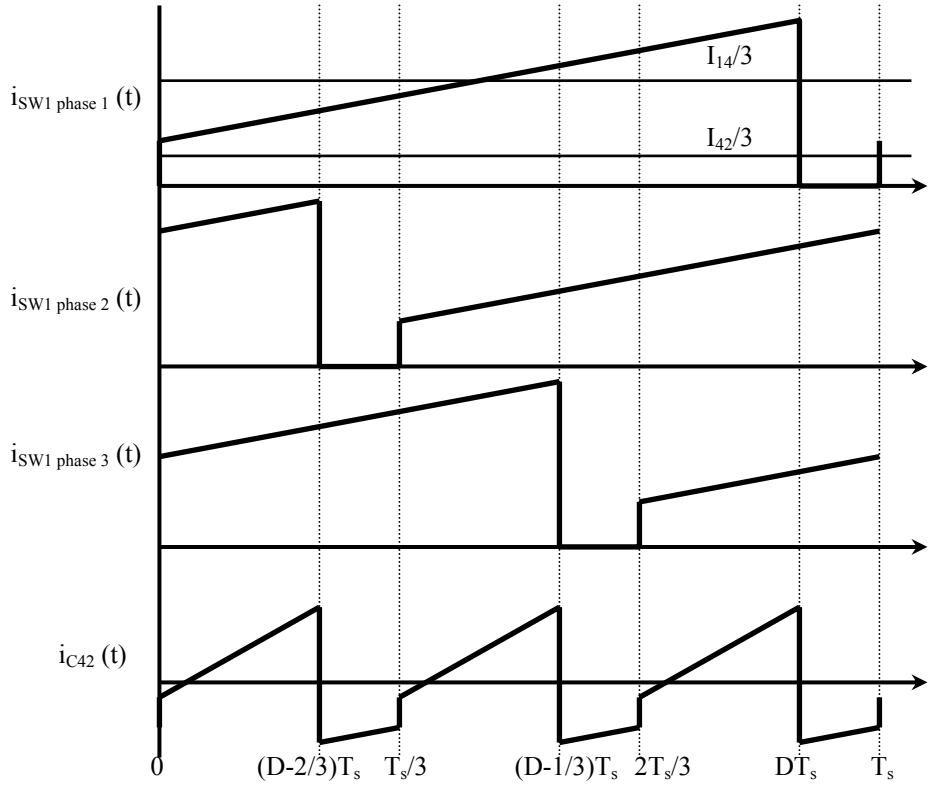



**Figure B.6. The currents in $SW_1$ and the 42V capacitor for a three-phase system with 2/3<D≤1**

$$I_{C_{42}\_RMS} = \sqrt{I_{42}^2\left(\frac{1-D}{D}\right)\left(\frac{D-\frac{2}{3}}{D}\right)+\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2 \frac{3}{12}\left[9\left(D-\frac{2}{3}\right)^3+4(1-D)^3\right]} \quad \text{for } \frac{2}{3} < D \le 1 \tag{B.18}$$

## 2.4 RMS current in $C_{42}$ for N-phases

To determine the RMS current in $C_{42}$ for an $N$-phase system, the RMS currents that have been derived for the one- to three-phase systems are rewritten and the general equation is determined by observation

The RMS currents for the 42V capacitor are rewritten and repeated for $N = 1, 2, 3$ and $n=1, 2, 3\ldots,N$

$N=1, n=1$:

$$I_{C_{42}\_RMS}=\sqrt{\frac{I_{42}^2}{D^2}(D-0)(1-D)+\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2 \frac{1}{12}\left[0^2(1-D)^3+1(D-0)^3\right]} \qquad \text{for } 0 < D \le 1 \tag{B.19}$$

$N=2, n=1$:

$$I_{C_{42}\_RMS} = \sqrt{\frac{I_{42}^2}{D^2}(D-0)\left(\frac{1}{2}-D\right)+\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2 \frac{2}{12}\left[0^2\left(\frac{1}{2}-D\right)^3+1^2(D-0)^3\right]} \qquad \text{for } 0 < D \le \frac{1}{2} \tag{B.20}$$

*N=2, n=2*:

$$I_{C_{42}\_RMS}=\sqrt{\frac{I_{42}^2}{D^2}\left(D-\frac{1}{2}\right)\left(\frac{2}{2}-D\right)+\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2\frac{2}{12}\left[1^2\left(\frac{1}{2}-D\right)^3+2^2\left(D-\frac{1}{2}\right)^3\right]} \quad \text{for } \frac{1}{2}<D\le 1 \tag{B.21}$$

*N=3, n=1*:

$$I_{C_{42}\_RMS}=\sqrt{\frac{I_{42}^2}{D^2}(D-0)\left(\frac{1}{3}-D\right)+\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2\frac{3}{12}\left[0^2\left(\frac{1}{3}-D\right)^3+1^2\left(D-\frac{0}{3}\right)^3\right]} \quad \text{for } 0<D\le\frac{1}{3} \tag{B.22}$$

*N=3, n=2*:

$$I_{C_{42}\_RMS}=\sqrt{\frac{I_{42}^2}{D^2}\left(D-\frac{1}{3}\right)\left(\frac{2}{3}-D\right)+\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2\frac{3}{12}\left[1^2\left(\frac{2}{3}-D\right)^3+2^2\left(D-\frac{1}{3}\right)^3\right]} \quad \text{for } \frac{1}{3}<D\le\frac{2}{3} \tag{B.23}$$

*N=3, n=3*:

$$I_{C_{42}\_RMS}=\sqrt{\frac{I_{42}^2}{D^2}\left(D-\frac{2}{3}\right)\left(\frac{3}{3}-D\right)+\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2\frac{3}{12}\left[2^2\left(\frac{3}{3}-D\right)^3+3^2\left(D-\frac{2}{3}\right)^3\right]} \quad \text{for } \frac{2}{3}<D\le 1 \tag{B.24}$$

Considering the above equations and rewriting them in terms of *n* and *N*, the following generic equation can be extracted:

$$I_{C_{42}\_RMS}=\sqrt{\frac{I_{42}^2}{D^2}\left(D-\frac{n-1}{N}\right)\left(\frac{n}{N}-D\right)+\left(\frac{V_{42}(1-D)DT_s}{L}\right)^2\frac{N}{12}\left[(n-1)^2\left(\frac{n}{N}-D\right)^3+n^2\left(D-\frac{n-1}{N}\right)^3\right]} \text{ for } \frac{n-1}{N}<D\le\frac{n}{N} \tag{B.25}$$

where $I_{C42\_RMS}$ is the RMS current in $C_{42}$ [A],
$N$ is the number of phases
and $n=1,2,3\ldots N$ and depend on the duty cycle

The above equation describes the RMS current in the 42V capacitor, $C_{42}$, as a function of the circuit parameters and the number of phases. The equation has been derived taking only continuous conduction into consideration, but because the considered circuit is a synchronous rectifier circuit, the average current in the inductor can be both positive and negative covering the entire possible working range of the converter.

## 3. RMS current in $C_{14}$

The RMS current in $C_{14}$ for *N*-phases is calculated in the same way as for $C_{42}$.

### 3.1 RMS current in $C_{14}$ for a single-phase

Figure B.7 shows the current flowing in the 14V bus capacitor. Further, let $T_s$ be the switching

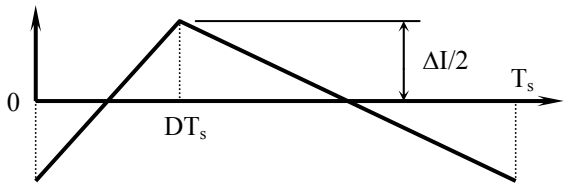



**Figure B.7. The current in $C_{14}$**

period, $D$ the duty cycle varying between 0 and 1 and let $\Delta I_L$ be the current ripple defined by the inductance, $L$.

Then the piecewise currents describing the current in the capacitor can be calculated as:

$$i_{C_{14}}(t)=\begin{cases}\dfrac{V_{42}(1-D)}{L}\left(t-\frac{1}{2}DT_s\right) & 0<t\le DT_s\\ \dfrac{V_{42}(D)}{L}\left(\frac{1}{2}(1+D)T_s-t\right) & DT<t\le T_s\end{cases} \tag{B.26}$$

The RMS current can be calculated as:

$$I^2_{C_{14}\_RMS}=\frac{1}{T_s}\left[\int_0^{DT_s}\left(\frac{V_{42}(1-D)}{L}\left(t-\frac{1}{2}DT_s\right)\right)^2 dt+\int_{DT_s}^{T_s}\left(\frac{V_{42}D}{L}\left(\frac{1}{2}(1+D)T_s-t\right)\right)^2 dt\right] \tag{B.27}$$

Performing the integration yields:

$$I_{C_{14}\_RMS}=\frac{V_{42}(1-D)DT_s}{\sqrt{12}L} \tag{B.28}$$

Where $I_{C14\_RMS}$ is the RMS current in $C_{14}$ [A].

### 3.2 RMS current in $C_{14}$ for two-phases

When more than one-phase is operational, the waveforms undergo a significant change when the duty cycle is equal to the inverse of the number of phases or any integer multiple there of with the result smaller than one, i.e., $D=n/N$, with n=1,2,…,$N$. This means that for a two-phase system, the currents must be considered separately for $D<0.5$ and $D\geq 0.5$.

#### *3.2.1 $C_{14}$ RMS current for D<0.5*

Consider Figure B.8. The figure shows the current in the 14V capacitor, $i_{C14}(t)$, as well as the current in the two inductors, $i_{L\_phase1}(t)$ and $i_{L\_phase2}(t)$. The current in the capacitor is the

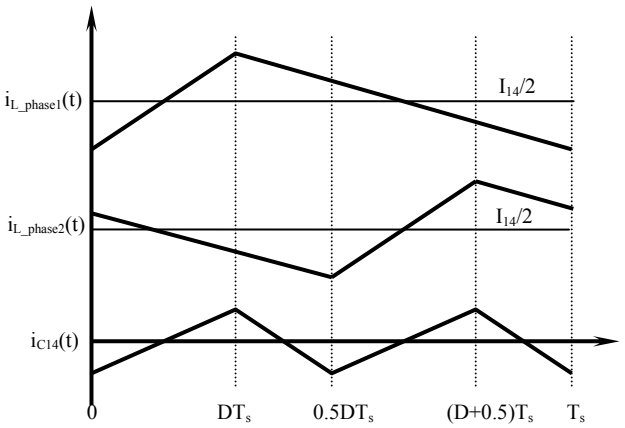



**Figure B.8. The capacitor current in $C_{14}$ for a two-phase system with D<0.5**

instantaneous sum of the two inductor currents less the average load current. The current in $C_{14}$ can be represented as:

$$i_{C_{14}}(t)=\begin{cases}\dfrac{V_{42}(1-2D)}{L}\left(t-\frac{1}{2}DT_s\right) & 0<t\le DT_s\\ \dfrac{V_{42}(D)}{L}\left(\left(\frac{1}{2}-D\right)T_s-2t\right) & DT<t\le\frac{1}{2}T_s\end{cases} \tag{B.29}$$

The RMS current can be calculated as:

$$I^2_{C_{14}\_RMS}=\frac{1}{T_s}\left[\int_0^{DT_s}\left(\frac{V_{42}(1-2D)}{L}\left(t-\frac{1}{2}DT_s\right)\right)^2dt+\int_{DT_s}^{\frac{1}{2}T_s}\left(\frac{V_{42}(D)}{L}\left(\left(\frac{1}{2}-D\right)T_s-2t\right)\right)^2dt\right] \tag{B.30}$$

Performing the integration yields:

$$I_{C_{14}\_RMS}=\frac{V_{42}(1-2D)DT_s}{\sqrt{12}L}\qquad \text{for } 0<D\le\frac{1}{2} \tag{B.31}$$

### *2.2.3 $C_{14}$ RMS current for D≥0.5*

Consider Figure B.9. The figure shows the current in the two inductors and the 14V capacitor for a duty cycle larger than 50%.

The current in $C_{14}$ can be represented as:

$$i_{C_{14}}(t)=\begin{cases}\dfrac{V_{42}(1-D)}{L}\left(\left(\frac{1}{2}-D\right)T_s+2t\right) & \frac{1}{2}T_s<t\le DT_s\\ \dfrac{V_{42}(1-2D)}{L}\left(t-\left(\frac{1}{2}-D\right)T_s\right) & DT_s<t\le T_s\end{cases} \tag{B.32}$$

The RMS current can be calculated as:

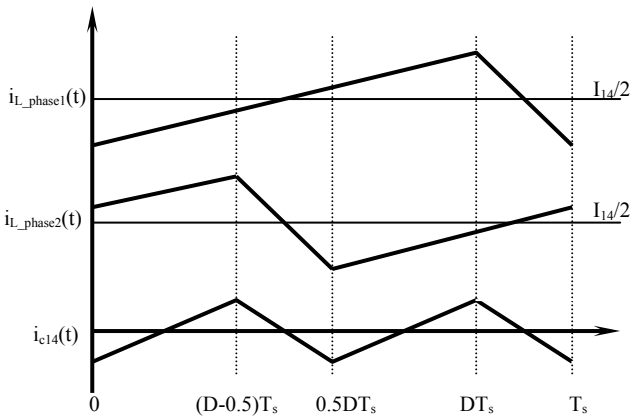



**Figure B.9. The current in the inductors and $C_{14}$ for D≥0.5**

$$I^2_{C_{14}\_RMS} = \frac{1}{T_s}\left[\int_{\frac{1}{2}T_s}^{DT_s}\left(\frac{V_{42}(1-D)}{L}\left(\left(\frac{1}{2}-D\right)T_s+2t\right)\right)^2 dt + \int_{DT_s}^{T_s}\left(\frac{V_{42}(1-2D)}{L}\left(t-\left(\frac{1}{2}-D\right)T_s\right)\right)^2 dt\right] \quad (B.33)$$

Performing the integration yields:

$$I_{C_{14}\_RMS} = \frac{V_{42}(D-1)(1-2D)T_s}{\sqrt{12}L} \qquad \text{for } \frac{1}{2} < D \le 1 \quad (B.34)$$

### 3.3 RMS current in $C_{14}$ for three-phases

The three-phase system needs to be considered over three intervals, namely $0 < D \le 1/3$, $1/3 < D \le 2/3$ and $2/3 < D \le 1$. In each of the three intervals, the waveforms are different and thus treated separately.

#### *3.3.1 $C_{14}$ RMS current for D≤1/3*

The current in the capacitor is determined from the sum of the currents in the inductors, less the average current in the load as illustrated in Figure B.10. The capacitor current, for a duty cycle of less than 1/3 can be described by:

$$i_{C_{14}}(t) = \begin{cases} \frac{V_{42}}{2L}(3D-1)(DT_s - t) & \text{for } 0 < t \le \frac{1}{3}T_s \\ \frac{V_{42}D}{L}\left(\frac{1}{2}(1-3D)T_s - 3(t-DT_s)\right) & \text{for } DT < t \le \frac{1}{3}T_s \end{cases} \quad (B.35)$$

The RMS current is calculated as:

$$I^2_{C_{14}\_RMS} = \frac{3}{T_s}\left[\int_0^{DT_s}\left(\frac{V_{42}}{2L}(3D-1)(DT_s-t)\right)^2 dt + \int_0^{\left(\frac{1}{3}-D\right)T_s}\left(\frac{V_{42}D}{L}\left(\frac{1}{2}(1-3D)T_s-3t\right)\right)^2 dt\right] \quad (B.36)$$

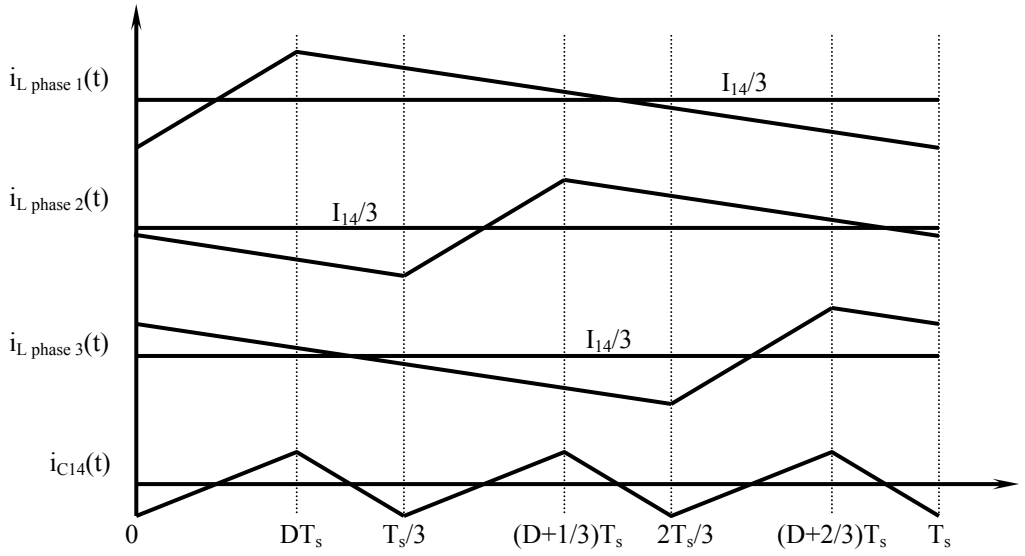



**Figure B.10. The current in the three inductors and the resulting current in $C_{14}$ for $0 < D \le 1/3$**

which can be reduced to:

$$I_{C_{14}\_RMS} = \frac{V_{42} D T_s}{\sqrt{12} L}(1-3D) \qquad \text{for } 0 < D \le \frac{1}{3} \tag{B.37}$$

### *3.3.2 $C_{14}$ RMS current for 1/3<D≤2/3*

Figure B.11 shows the current in the three inductors together with the current in the 14V capacitor. The three inductor currents summate together, less the total average to produce the capacitor current.

The current in the capacitor can be described piecewise as:

$$i_{C_{14}}(t) = \begin{cases} \frac{V_{42}}{L}\left(1-\frac{3}{2}D\right)\left(2t+\frac{1}{3}[1-3D]T_s\right) & \text{for } 0 < t \le \left(D-\frac{1}{3}\right)T_s \\ \frac{V_{42}}{L}\left(\frac{3}{2}D-\frac{1}{2}\right)\left(\frac{1}{3}[2-3D]T_s - 2\left(t-\left(D-\frac{1}{3}\right)T_s\right)\right) & \text{for } \left(D-\frac{1}{3}\right)T_s < t \le \frac{1}{3}T_s \end{cases} \tag{B.38}$$

The RMS current is:

$$I^2_{C_{14}\_RMS} = \frac{3}{T_s}\left[\begin{array}{l} \left\{\int_0^{\left(D-\frac{1}{3}\right)T_s}\left(\frac{V_{42}}{L}\left(1-\frac{3}{2}D\right)\left(2t+\frac{1}{3}[1-3D]T_s\right)\right)^2 dt\right\} + \\ \left\{\int_{\left(D-\frac{1}{3}\right)T_s}^{\frac{T}{3}}\left(\frac{V_{42}}{L}\left(\frac{3}{2}D-\frac{1}{2}\right)\left(\frac{1}{3}[2-3D]T_s - 2\left(t-\left(D-\frac{1}{3}\right)T_s\right)\right)\right)^2 dt\right\} \end{array}\right] \tag{B.39}$$

which can be simplified to:

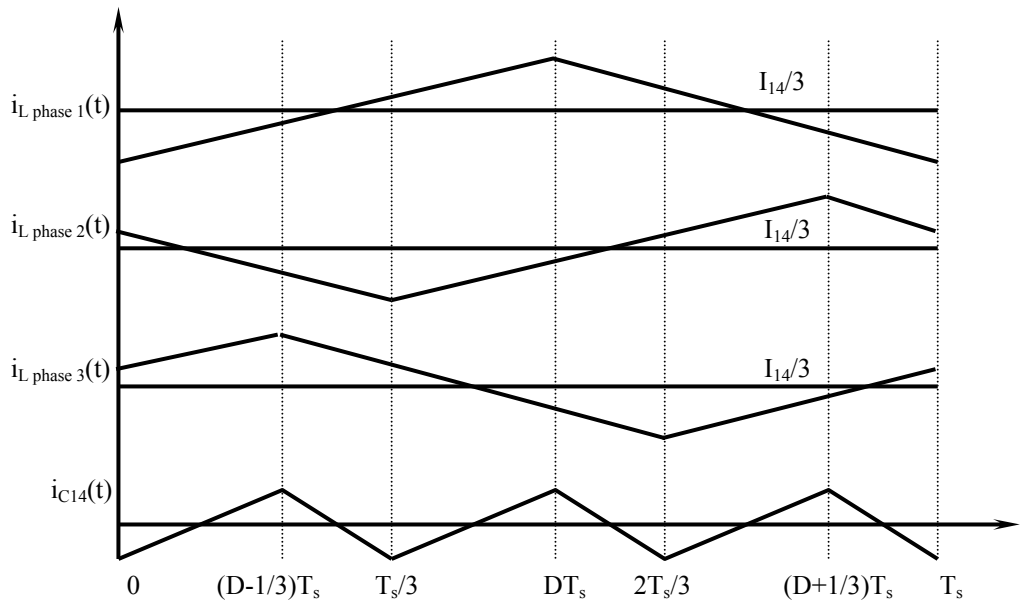



**Figure B.11. The currents in the three inductors and $C_{14}$ for 1/3 < D ≤ 2/3**

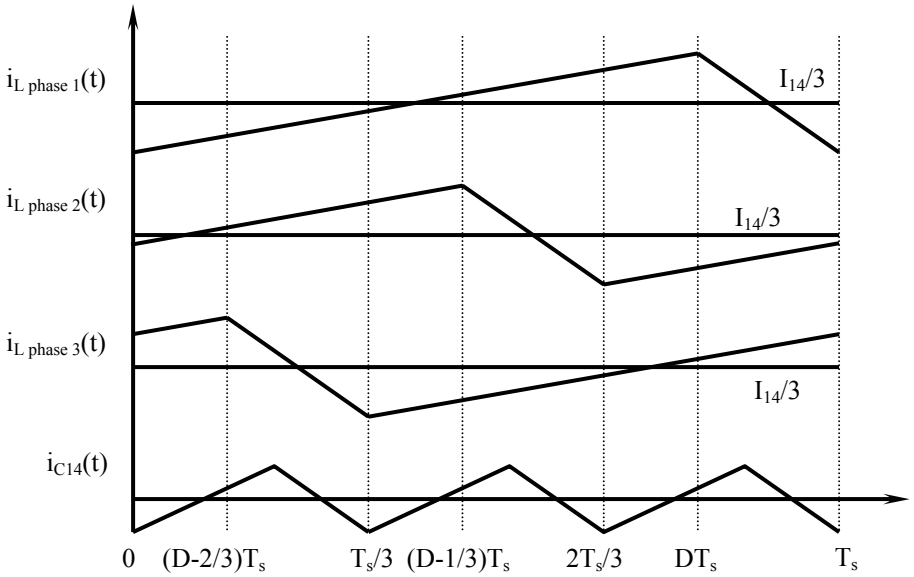



**Figure B.12 The inductor and $C_{14}$ currents for a duty cycle of 2/3 < D ≤ 1**

$$I_{C_{14}\_RMS} = \frac{V_{42}T_s}{\sqrt{12}L}(1-3D)\left(D-\frac{2}{3}\right) \qquad \text{for } \frac{1}{3} < D \le \frac{2}{3} \tag{B.40}$$

### *3.3.3 $C_{14}$ RMS current for 2/3>D≥1*

Figure B.12 shows the currents in the three inductors and the 14V capacitor. The three inductor currents sum together, less the average to produce the capacitor current.

The currents waveforms plotted in Figure B.12 are similar to the current waveforms plotted in Figure B.10. The currents in Figure B.10 are the mirror of the currents in Figure B.12. This allows the RMS current to be determined by making a substitution of $D = 1 - D$ in equation B.37. Doing this yields:

$$\begin{aligned} I_{C_{14}\_RMS} &= \frac{V_{42}(1-D)T_s}{\sqrt{12}L}(1-3(1-D)) \\ &= \frac{V_{42}T_s}{\sqrt{12}L}\left(D-\frac{2}{3}\right)(3-3D) \quad \text{for } \tfrac{2}{3} < D \le 1 \end{aligned} \tag{B.41}$$

## 3.4 RMS current in $C_{14}$ for N-phases

The generic equations for $C_{14}$ are determined by comparing the one-, two- and three-phase equations to each other and visually extracting the universal equation in terms of the number of phases.

The RMS currents for the 14V capacitor are rewritten for $N = 1, 2, 3$ and $n = 1, 2, n$.

$N=1, n=1$:

$$I_{C_{14}\_RMS} = \frac{V_{42}T_s}{\sqrt{12}L}(D-0)\left(\frac{1}{1}-D\right) \qquad \text{for } 0 < D \le 1 \tag{B.42}$$

*N=2, n=1*:

$$I_{C_{14}\_RMS} = \frac{V_{42}T_s}{\sqrt{12}L}(2D-0)\left(\frac{1}{2}-D\right) \qquad \text{for } 0 < D < \tfrac{1}{2} \tag{B.43}$$

*N=2, n=2*:

$$I_{C_{14}\_RMS} = \frac{V_{42}T_s}{\sqrt{12}L}(2D-1)\left(\frac{2}{2}-1D\right) \qquad \text{for } \tfrac{1}{2} < D \le 1 \tag{B.44}$$

*N=3, n=1*:

$$I_{C_{14}\_RMS} = \frac{V_{42}T_s}{\sqrt{12}L}(3D-0)\left(\frac{1}{3}-D\right) \qquad \text{for } 0 < D \le \tfrac{1}{3} \tag{B.45}$$

*N=3, n=2*:

$$I_{C_{14}\_RMS} = \frac{V_{42}T_s}{\sqrt{12}L}(3D-1)\left(\frac{2}{3}-D\right) \qquad \text{for } \tfrac{1}{3} < D \le \tfrac{2}{3} \tag{B.46}$$

*N=3, n=3*:

$$I_{C_{14}\_RMS} = \frac{V_{42}T_s}{\sqrt{12}L}(3D-2)\left(\frac{3}{3}-D\right) \qquad \text{for } \tfrac{2}{3} < D \le 1 \tag{B.47}$$

The RMS current in the 14V capacitor can be described in terms of *N* and *n* by:

$$I_{C_{14}\_RMS} = \frac{V_{42}T_s}{\sqrt{12}L}[ND-(n-1)]\left[\frac{n}{N}-D\right] \qquad \text{for } \frac{n-1}{N} < D \le \frac{n}{N} \tag{B.48}$$

where $I_{C14\_RMS}$ is the RMS current in $C_{14}$ [A],
$N$ is the number of phases
and $n=1,2,3\ldots N$ and depends on the duty cycle.

## 4. RMS current in L

The RMS current in the inductor for any number of phases can be calculated from Figure B.13. Only the average current of the inductor changes as the number of phases change. The period of the inductor current remains unchanged as the number of phases vary. Thus the inductor current can be described piecewise for any number of phases as:

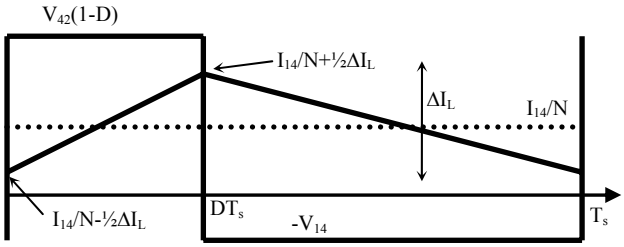



**Figure B.13. The inductor waveforms for an arbitrary number of phases**

$$i_L(t) = \begin{cases} \frac{I_{42}}{ND} + \Delta I_L\left(\frac{t}{DT_s} - \frac{1}{2}\right) & \text{for } 0 < t \le DT_s \\ \frac{I_{42}}{ND} + \Delta I_L\left(\frac{1}{2} - \frac{t}{(1-D)T_s}\right) & \text{for } DT_s < t \le 1 \end{cases} \quad \text{(B.49)}$$

where $i_L(t)$ is the current in the inductor [A],
$\Delta I_L$ is the current ripple in the inductor current given as:

$$\Delta I_L = \frac{V_{42}(1-D)DT_s}{L} \quad \text{(B.50)}$$

The RMS current in the inductor can be calculated as:

$$I_{L\_RMS}^2 = \frac{1}{T_s}\left[\int_0^{DT_s}\left(\frac{I_{42}}{ND} + \Delta I_L\left(\frac{t}{DT_s} - \frac{1}{2}\right)\right)^2 dt + \int_{DT_s}^{T_s}\left(\frac{I_{42}}{ND} + \Delta I_L\left(\frac{1}{2} - \frac{t}{(1-D)T_s}\right)\right)^2 dt\right] \quad \text{(B.51)}$$

The RMS current in the inductor as a function of the number of phases can then be calculated to be:

$$I_{L\_RMS} = \sqrt{\left(\frac{I_{42}}{ND}\right)^2 + \frac{1}{12}\Delta I_L^2} \quad \text{(B.52)}$$

where $I_{L\_RMS}$ is the RMS current in a single inductor in an $N$-phase system [A]
and $N$ is the number of phases.

# Appendix C

## LOSSES IN THE INTEGRATED HEAT SINK AND INDUCTOR STRUCTURE

## 1. Introduction

The inductor loss analysis comprises of calculating the losses in the conductors, heat sink and in the ferrite for the given excitation range (single phase synchronous converter operating at 500W) as described in Chapter 5.

In the following section, the core losses are considered first followed by the conduction losses in the structure. The core losses are considered analytically while the conduction losses are simulated.

## 2. Inductor core losses

The core losses in the inductor are approximated with the aid of a relative core losses versus frequency curve found in the data sheets for the magnetic material N92. To approximate the losses, the peak to peak change in the magnetic flux density is calculated. This value of the magnetic flux density is used to read off the losses per volume from the graph.

This method does not have a very high accuracy but does provide sufficient indication of the core losses.

### 2.1 The magnetic flux density components

Table C.1 tabulates the change in the magnetic flux density, $\Delta B$, the average magnetic flux density, $B_{ave}$, and the maximum magnetic flux density, $B_{max}$, based on the inductor current and core geometry. To approximate the core losses, $\Delta B$ is of interest.

It can be noticed that the value of $\Delta B$ does not have a large range with a minimum and maximum values corresponding to about 90mT and 140mT respectively. To accommodate reading the loss value off of the data sheet graphs, an average value of $\Delta B$ is used. The average value is about 115mT.

Reading the volume loss density off the graph, a volume loss density of 100kW/m$^3$ can be expected for the core operating with a core temperature of 100°C. The cores used in the inductor structure have a volume of 2540mm$^3$. The corresponding loss in the inductor core is therefore approximately 250mW. The very low value of core losses compared to the excitation justifies not calculating the core losses more accurately.

## 3. Winding conduction losses (FEM based)

Finite element loss analysis is required to obtain a more realistic value of the losses within the inductor winding structure by taking into account the two dimensional effects of the magnetic

**Table C.1. The magnetic flux density in the inductor as a function of the excitation range**

| $V_{14}$ | $V_{42}$ | $\Delta B$ | $B_{ave}$ | $B_{max}$ |
|---|---|---|---|---|
| 11 | 30 | 0.089985 | 0.312346 | 0.357339 |
| 14 | 30 | 0.096444 | 0.245415 | 0.293636 |
| 16 | 30 | 0.096444 | 0.214738 | 0.26296 |
| 11 | 36 | 0.098668 | 0.312346 | 0.36168 |
| 14 | 36 | 0.110508 | 0.245415 | 0.300669 |
| 16 | 36 | 0.114814 | 0.214738 | 0.272145 |
| 11 | 42 | 0.10487 | 0.312346 | 0.364781 |
| 14 | 42 | 0.120555 | 0.245415 | 0.305692 |
| 16 | 42 | 0.127935 | 0.214738 | 0.278706 |
| 11 | 46 | 0.108106 | 0.312346 | 0.366399 |
| 14 | 46 | 0.125796 | 0.245415 | 0.308313 |
| 16 | 46 | 0.134781 | 0.214738 | 0.282129 |
| 11 | 50 | 0.110824 | 0.312346 | 0.367758 |
| 14 | 50 | 0.130199 | 0.245415 | 0.310514 |
| 16 | 50 | 0.140532 | 0.214738 | 0.285004 |

flux density distribution. The copper losses are calculated by considering the spatial distribution of the current within the copper conductor(s) and calculated as:

$$P_{cu} = \int_{vol} \rho\{\overline{J(t)} \bullet \overline{J(t)}\}dv \tag{C.1}$$

where $P_{cu}$ are the losses in the conductor [W]

$\overline{J(t)}$ is the current density [A/m$^2$]

and $\rho$ is the electrical resistivity [Ωm].

From the properties of the dot product, the above can be simplified to:

$$P_{cu} = \int_{vol} \rho\{J^2\}dv \tag{C.2}$$

since the dot product of a vector with itself is the square of its amplitude.

### 3.1 Calculating the total power loss

The current density is typically not sinusoidal in time. This complicates the calculation of the total power losses. To calculate the conduction losses in the winding, the excitation current must be reduced to its Fourier components and then the losses can be calculated.

Let the current density in the inductor windings be defined as:

$$J(t) = J_0 + \sum_{h=1}^{\infty} J_h Cos(h\omega t + \phi_h) \tag{C.3}$$

where $J_0$ is the DC component of the current density [A/m$^2$],
$J_h$ is the $h^{th}$ component of the Fourier series of the current density [A/m$^2$],
$\phi_h$ is the phase shift of the $h^{th}$ component of the current density [rad]
and $h$ is the harmonic number.

Squaring the current density:

$$J^2(t) = J_0^2 + 2J_0\sum_{h=1}^{\infty} J_h Cos(h\omega t + \phi_h) + \underbrace{\sum_{h=1}^{\infty}\sum_{m=1}^{\infty} J_h J_m Cos(h\omega t + \phi_h)Cos(m\omega t) + \phi_m)...}_{h\neq m} + \sum_{h=1}^{\infty} J_h^2 Cos^2(h\omega t + \phi_h) \tag{C.4}$$

The instantaneous power is calculated as:

$$p(t) = \rho \int_{vol} J^2(t)dv \tag{C.5}$$

Substituting equation C.4 into equation C.5:

$$p(t) = \rho\left[\int_{vol} J_0^2 dv + \int_{vol} 2J_0\sum_{h=1}^{\infty} J_h Cos(h\omega t + \phi_h)dv + \int_{vol}\sum_{h=1}^{\infty} J_h^2 Cos^2(h\omega t + \phi_h)dv... + \underbrace{\int_{vol}\sum_{h=1}^{\infty}\sum_{m=1}^{\infty} J_h J_m Cos(h\omega t + \phi_h)Cos(m\omega t) + \phi_m)dv}_{h\neq m}\right] \tag{C.6}$$

The power dissipated in the conductors can then be determined from:

$$P_{cu} = \frac{1}{T}\int_T p(t)dt \tag{C.7}$$

Substituting equation C.6 into C.7 yields:

$$P_{cu} = \frac{\rho}{T}\left[\int_T\int_{vol} J_0^2\, dv\, dt + \int_T\int_{vol} 2J_0\sum_{h=1}^{\infty} J_h Cos\,(h\omega t + \phi_h)dvdt\ .... + \underbrace{\int_T\int_{vol}\sum_{h=1}^{\infty}\sum_{m=1}^{\infty} J_h J_m Cos\,(h\omega t + \phi_h)Cos\,(m\omega t + \phi_m)dvdt\ ....}_{h\neq m} + \int_T\int_{vol}\sum_{h=1}^{\infty} J_h^2 Cos^2(h\omega t + \phi_h)dvdt\right] \tag{C.8}$$

Equation C.8 is the power lost in the copper conductors due to the current distribution within the conductors. The expression can be simplified by noting that:

$$\sum_{n=1}^{\infty}\int_{T} Cos(n\omega t+\phi_n)dt = 0 \tag{C.9}$$

and

$$\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\int_{T} Cos(n\omega t+\phi_n)Cos(m\omega t+\phi_m)dt = 0 \qquad if\ n \neq m \tag{C.10}$$

which is known as the orthogonal property of cosine.

Substituting equations C.9 and C.10 into C.8:

$$P_{cu} = \frac{\rho}{T}\left[\int_{T}\int_{vol} J_0^2 dvdt + \int_{T}\int_{vol}\sum_{h=1}^{\infty} J_h^2 Cos^2(h\omega t+\phi_h)dvdt\right] \tag{C.11}$$

Performing the time integration:

$$P_{cu} = \frac{\rho}{T}\left[T\int_{vol} J_0^2 dv + T\sum_{h=1}^{\infty}\frac{1}{2}\int_{vol} J_h^2 dv\right] \tag{C.12}$$

The summation and integration symbols can be interchanged if the current density is linear piece wise over time. This is the case for the current waveform. Finally:

$$P_{cu} = P_{DC} + \sum_{h=1}^{\infty} P_h \tag{C.13}$$

Equation C.13 shows that the total power loss in the copper conductors is the sum of the losses in the conductors for all of the Fourier's components of the inductor's current. Thus to determine the total copper losses, the losses at each harmonic frequency must be calculated and then summed to give the total power loss.

The losses induced in the heat sink due to induced eddy currents can be determined in exactly the same way.

### 3.2 Determining the inductor conduction losses

To determine the conduction losses in the inductor structure with the aid of ANSYS™, two cross-sections through the inductor are considered. The sections are illustrated in Figure C.1. The figure in the bottom left corner shows a cross-section of the inductor winding clamped in the heat sink structure. This section is found outside of the ferrite. The winding is clamped in the heat sink to minimise the thermal resistance between the inductor winding and the thermal

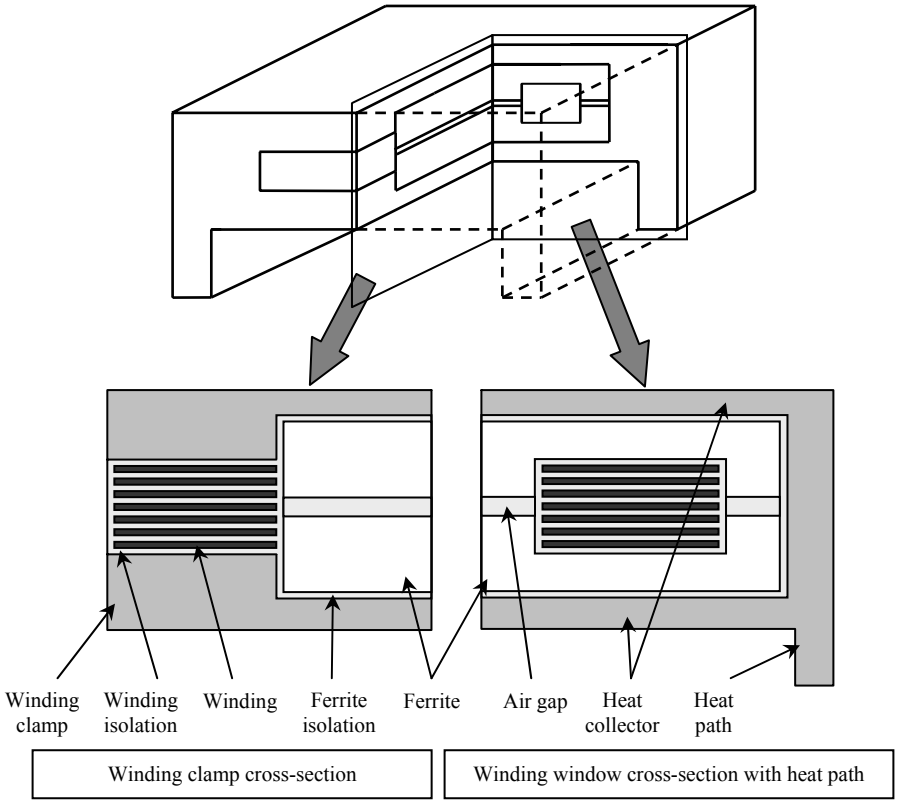



**Figure C.1. The two inductor structure cross-sections used to calculate the conduction losses in the inductor windings and the integrated heat sink structure**

interface. The figure in the bottom right corner shows the cross-section of the inductor winding window. The ferrite is also clamped in the heat sink structure as shown in the figure. This aids in the heat removal from the inductor structure.

The two cross-sections are electromagnetically simulated with ANSYS$^{TM}$ and the current density distribution in both the copper conductors and the aluminium heat sink are determined. The losses in the two components are then determined as discussed in the previous section.

The losses are determined for 15 combinations of the converter terminal voltage range. This is done to determine the inductor losses over the full inductor operating range. The terminal voltage combinations can be seen in Table C.1. For each voltage combination, the first 4 harmonics of the inductor current are determined and used to excite the simulations to determine the losses in the copper conductors and aluminium heat sink.

The simulation determines the losses for each harmonic frequency. The DC losses are calculated separately and added to the harmonic losses as in equation C.13.

### *3.2.1. Simulation results for the winding window cross-section*

Before the losses for the inductor structure are considered, the results of the simulation for nominal operation ($V_{14}$ = 14V and $V_{42}$ = 42V) for both cross-sections are presented and discussed. This will illustrate the electromagnetic interaction between the inductor and the heat sink structure.

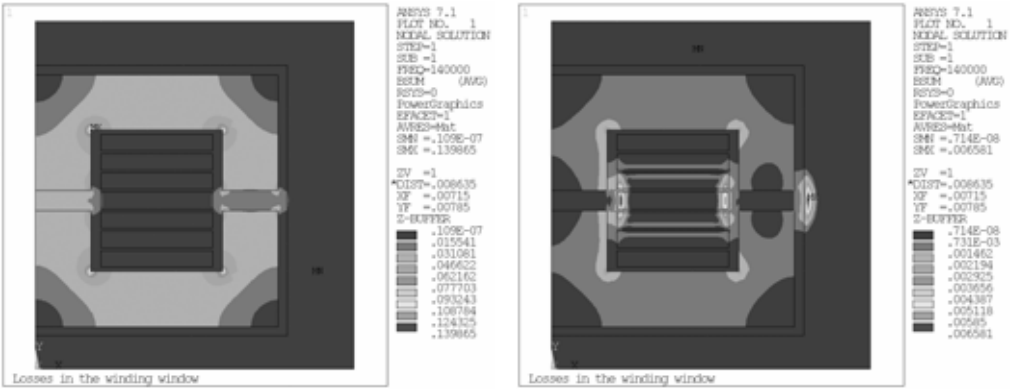



**Figure C.2. The real (left) and imaginary (right) components of the magnetic flux density**

The magnetic flux density and current density are calculated for the first four harmonics of the excitation current for the cross-section taken through the winding window of the inductor structure. The results for each simulation are plotted below.

### *3.2.1.1 Harmonic 1: Frequency =140kHz with I=-5.98+3.45j A*

Figure C.2 plots the magnetic flux density distribution for half of the winding window of the inductor clamped in the heat sink. Both the real and imaginary components are plotted on the left and right of the figure respectively. The magnetic flux density fringing around the air gap is evident in both figures. The magnetic flux density leaking into the copper conductors and heat sink will result in induced currents increasing the joule losses of the structure. The current distribution in both the copper conductors and the surrounding heat sink structure can be seen in Figure C.3 and Figure C.4 respectively.

Figure C.3 shows the current density distribution in both its real and imaginary components for the copper conductors. The effect of the leaking magnetic flux density into the windings is evident by the large currents in the region local to the air gap. The same effect can be seen in the heat sink as illustrated in Figure C.4.

The joule heat loss can be determined for the two metals for this harmonic. The conductors have a loss of 35.4W/m and the heat sink has an induced loss of 16.3W/m. These loss values are only valid this harmonic frequency.

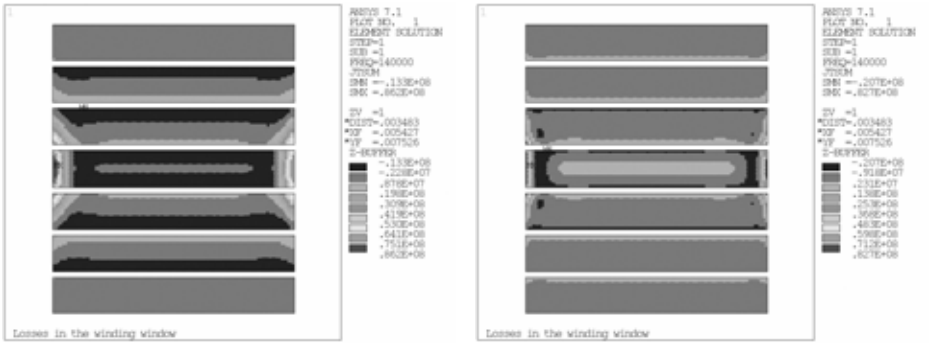



**Figure C.3. The real (left) and imaginary (right) components of the current density distribution in the copper conductors**

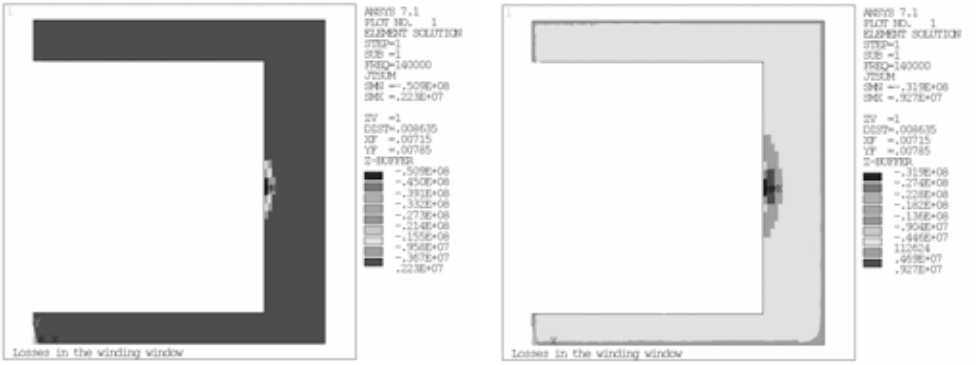



**Figure C.4. The real (left) and imaginary (right) components of the current density distribution in the aluminium heat sink**

### *3.2.1.2 Harmonic 2: Frequency =280kHz with I=-1.49-0.86j A*

Figure C.5 plots the real and imaginary components of the current density in the copper conductors for the second harmonic. The effect of the fringing magnetic flux density is once again evident on the current density distribution in both the real and imaginary components.

The current density distribution for the aluminium heat sink is plotted in Figure C.6. The

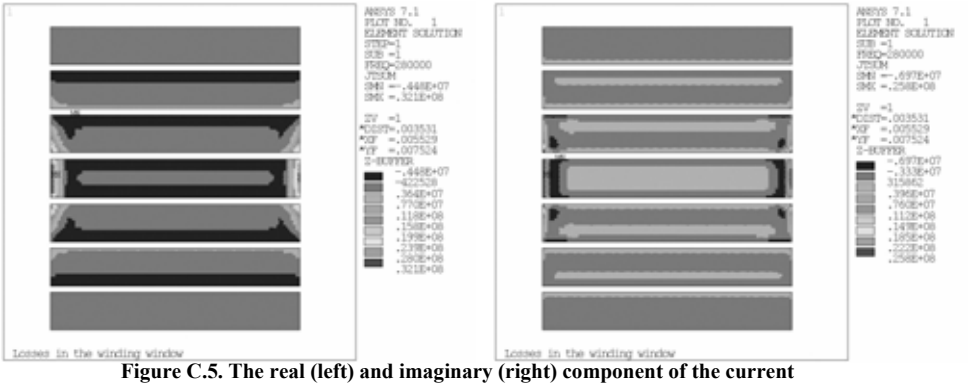



**Figure C.5. The real (left) and imaginary (right) component of the current density in the copper conductors**


**Figure C.6. The real (left) and imaginary (right) component of the current density in the aluminium heat sink**

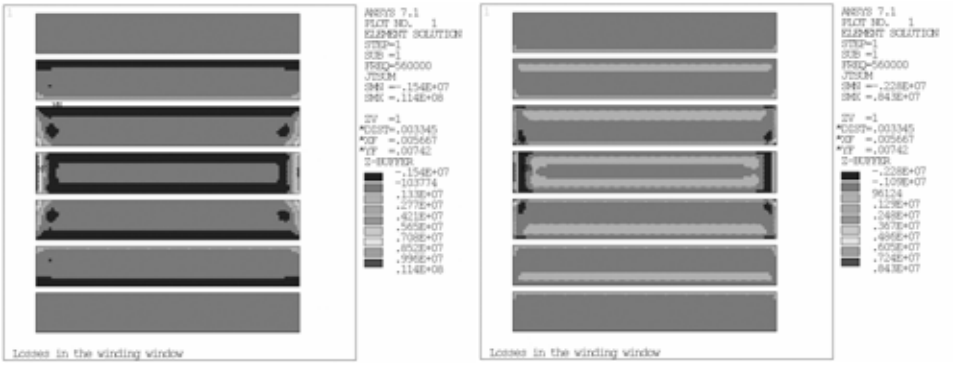



**Figure C.7. The real (left) and imaginary (right) component of the current density in the copper conductors**

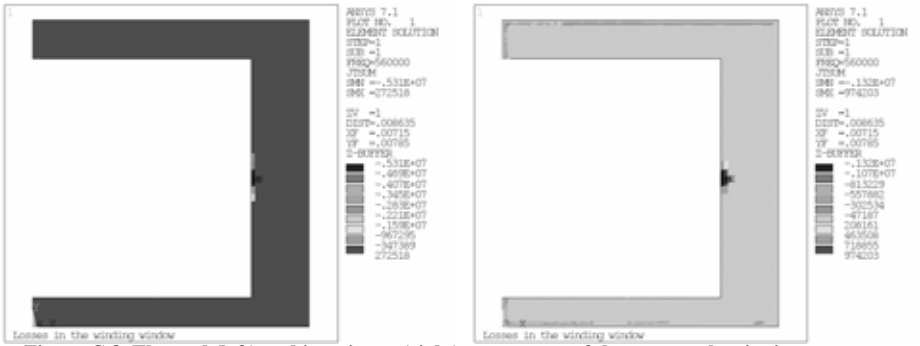



**Figure C.8. The real (left) and imaginary (right) component of the current density in the aluminium heat sink**

induced eddy currents result in a power loss of approximately 1.4W/m in the heat sink and 3.3W/m in the copper conductors.

#### *3.2.1.3 Harmonic 3: Frequency =420kHz with I=0+0j A*

The third harmonic of the excitation current is zero and consequently does not contribute to the losses.

#### *3.2.1.4 Harmonic 4: Frequency =560kHz with I=-0.37-0.22j A*

Figure C.7 shows the real and imaginary components of the current density in the copper conductors and Figure C.8 shows the same for the heat sink material for the fourth harmonic. The effects of the fringing magnetic flux density are still present but is decreasing. The reason for the decreasing disturbance in current density is because the current has a lower value and can't penetrate as deep as the previous cases.

For the fourth harmonic, the losses in the copper conductors are approximately 0.3W/m and for the heatsink, 0.13W/m.

### *3.2.2. Simulation results for the clamped winding section*

The magnetic flux density distribution together with the current density distribution is also calculated for the section taken through the winding passing outside of the ferrite core and clamed in the heat sink structure.

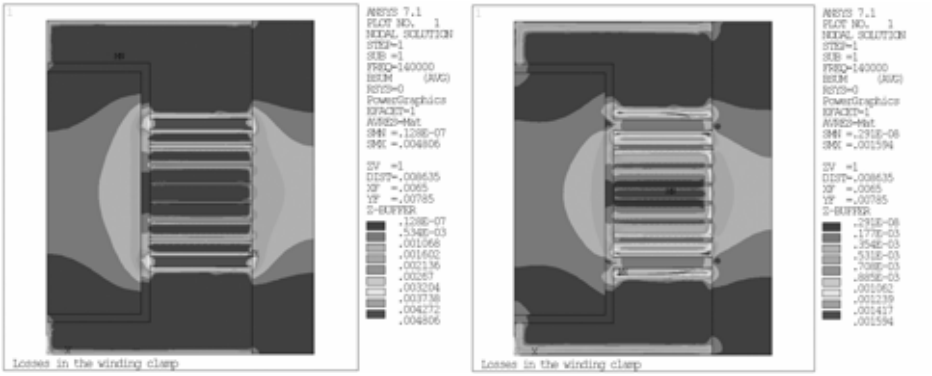



**Figure C.9. The real (left) and imaginary (right) components for the magnetic flux density distribution for the clamped winding section**

### *3.2.2.1 Harmonic 1: Frequency =140kHz with I=-5.98+3.45j A*

Figure C.9 shows the magnetic flux density distribution in its real and imaginary components for the section taken through the winding clamp. In both components it is clear that the magnetic flux density interacts with the heat sink clamping the copper conductors.

The current density distribution in the copper conductors is plotted in Figure C.10 and for the heat sink in Figure C.11. The current density distribution is mostly uniform across the width of

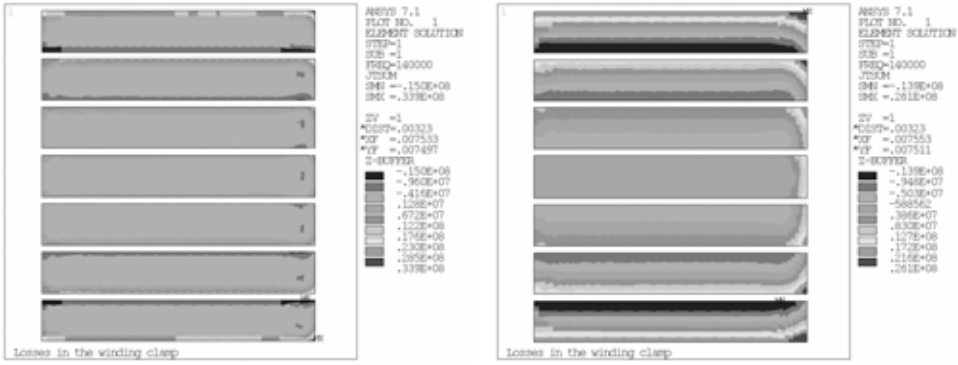



**Figure C.10. The real (left) and imaginary (right) component of the current density in the copper conductors**

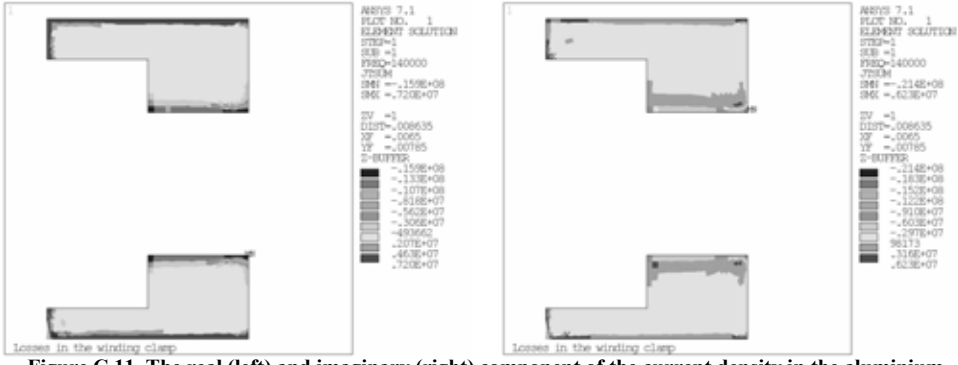



**Figure C.11. The real (left) and imaginary (right) component of the current density in the aluminium heat sink**

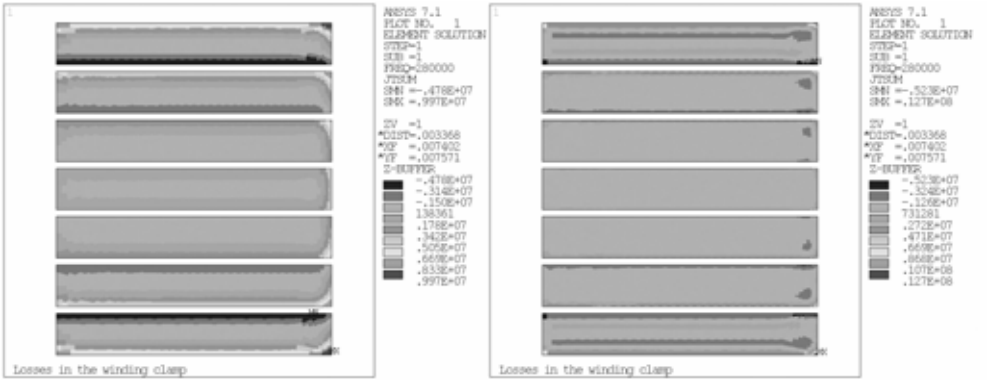



**Figure C.12. The real (left) and imaginary (right) component of the current density in the copper conductors**

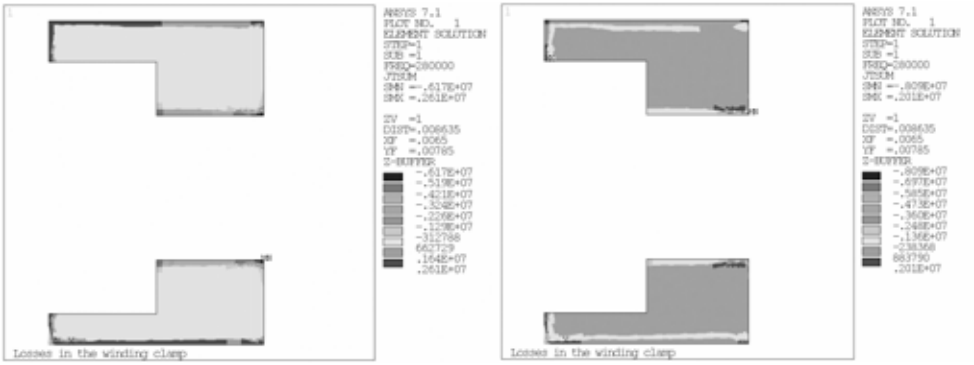



**Figure C.13. The real (left) and imaginary (right) component of the current density in the aluminium heat sink**

the copper conductors as expected from the magnetic flux density distribution. The close proximity of the copper conductors and the heat sink results in eddy currents being induced in the heat sink all along the width of the conductors. This induced current is largely responsible for the uniform current distribution along the width of the conductor.

The copper losses correspond to a loss of approximately 19.4W/m while the loss in the heat sink corresponds to about 14.6W/m for the given excitation conditions.

#### *3.2.2.2 Harmonic 2: Frequency =280kHz with I=-1.49-0.86j A*

The current density distribution in the copper conductors is plotted in Figure C.12 and in the heat sink in Figure C.13 for the second harmonic. The current density distribution is once again very uniform over the width of the conductors. The copper loss for this harmonic is approximately 1.7W/m and for the aluminium heat sink, 1.3W/m.

#### *3.2.2.3 Harmonic 3: Frequency =420kHz with I=0+0j A*

The third harmonic of the excitation current is zero and consequently does not contribute to the losses.

#### *3.2.2.4 Harmonic 4: Frequency =560kHz with I=-0.37-0.22j A*

Figure C.14 plots the current density distribution in the copper conductors for an excitation frequency of 560kHz and Figure C.15 plots the same in the aluminium heat sink. In the copper

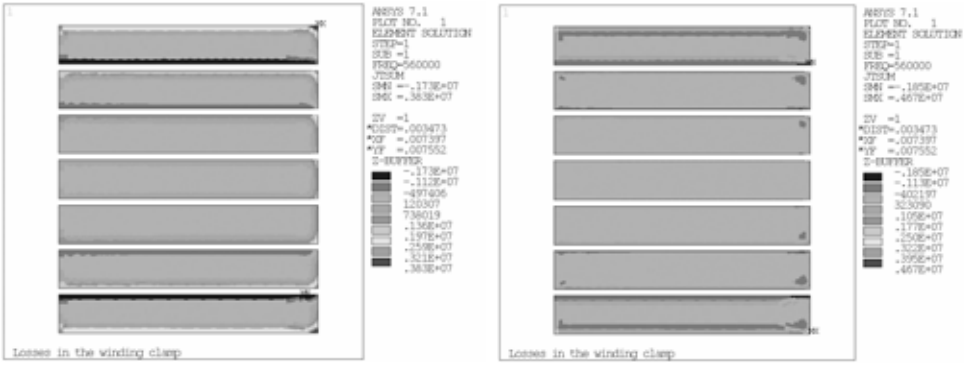



**Figure C.14. The real (left) and imaginary (right) component of the current density in the copper conductors**

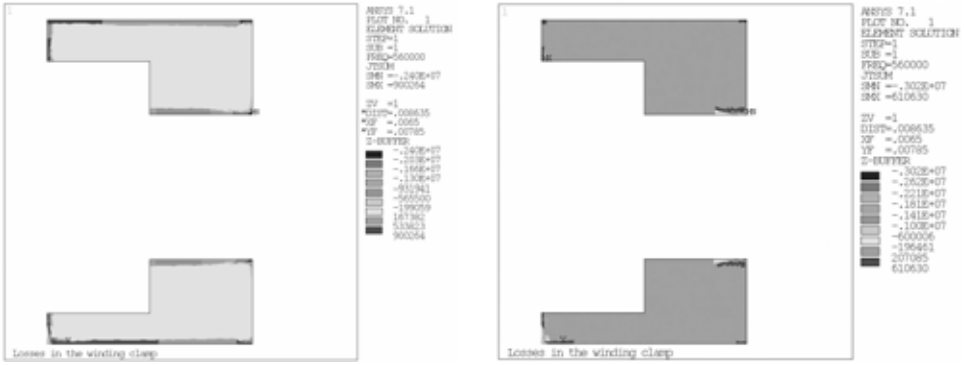



**Figure C.15. The real (left) and imaginary (right) component of the current density in the aluminium heat sink**

conductors the current density is still uniformly distributed across the width of the conductors. For this excitation, the copper losses correspond to about 3.3W/m and the losses induced in the heatsink correspond to about 2.6W/m.

## 4. Losses in the inductor structure

The conduction losses in the inductor structure due to the harmonics are determined by summating the conduction losses in the copper conductors and aluminium heat sink in the two cross-sections for the 4 harmonic frequencies. This is repeated for the 15 different excitation conditions covering the operating range of the inductor. The losses due to the harmonics are tabulated in Table C.2. The DC losses and the core losses have not been included as of yet.

Table C.2 shows that a considerable portion of the losses in the inductor structure are induced in the heat sink structure. It can also be noticed that the losses in the copper conductors in the winding clamp are always significantly less than that in the winding window for approximately the same conductor lengths. For the geometrical configuration and material properties considered, one third of the harmonic induced losses in the copper conductors are located within the winding clamp and the remaining two thirds in the winding window.

### 4.1 Total Inductor Losses

The total inductor losses are determined from the sum of the previously approximated core losses, the above calculated conduction losses and the DC conduction losses in the copper

**Table C.2. Summary of the conduction losses in the inductor at 100°C**

| Terminal voltages (V) | | Conduction losses in the winding window (W) | | Conduction losses in the winding clamp (W) | | Total Cu conduction losses (W) | Total Al conduction losses (W) | Total inductor conduction losses (W) |
|---|---|---|---|---|---|---|---|---|
| $V_{14}$ | $V_{42}$ | Cu | Al | Cu | Al | Excluding the DC component | | |
| 11 | 30 | 0.62 | 0.28 | 0.31 | 0.23 | 0.93 | 0.51 | 1.43 |
| 14 | 30 | 0.50 | 0.22 | 0.25 | 0.18 | 0.74 | 0.41 | 1.15 |
| 16 | 30 | 0.43 | 0.19 | 0.21 | 0.15 | 0.64 | 0.35 | 0.98 |
| 11 | 36 | 0.84 | 0.37 | 0.42 | 0.31 | 1.25 | 0.68 | 1.93 |
| 14 | 36 | 0.89 | 0.40 | 0.45 | 0.33 | 1.34 | 0.73 | 2.07 |
| 16 | 36 | 0.78 | 0.35 | 0.39 | 0.29 | 1.18 | 0.64 | 1.82 |
| 11 | 42 | 0.94 | 0.42 | 0.47 | 0.35 | 1.41 | 0.77 | 2.18 |
| 14 | 42 | 1.21 | 0.54 | 0.60 | 0.45 | 1.82 | 0.99 | 2.81 |
| 16 | 42 | 1.22 | 0.55 | 0.61 | 0.45 | 1.83 | 1.00 | 2.83 |
| 11 | 46 | 1.00 | 0.45 | 0.50 | 0.37 | 1.50 | 0.82 | 2.32 |
| 14 | 46 | 1.36 | 0.61 | 0.68 | 0.50 | 2.04 | 1.11 | 3.15 |
| 16 | 46 | 1.48 | 0.61 | 0.74 | 0.50 | 2.21 | 1.11 | 3.32 |
| 11 | 50 | 1.07 | 0.48 | 0.53 | 0.39 | 1.60 | 0.87 | 2.48 |
| 14 | 50 | 1.46 | 0.66 | 0.73 | 0.54 | 2.19 | 1.19 | 3.39 |
| 16 | 50 | 1.68 | 0.75 | 0.84 | 0.62 | 2.51 | 1.37 | 3.88 |

conductors. The total inductor and integrated heat sink losses are tabulated in Table C.3 for 15 combinations of terminal voltages.

Table C.3 tabulates the three primary loss components for 15 terminal voltage conditions. The

**Table C.3. Summary of the total losses in the inductor structure**

| Terminal voltages (V) | | DC current (A) | DC losses (W) | Total harmonic conduction losses (W) | Core losses (W) | Total losses (W) |
|---|---|---|---|---|---|---|
| $V_{14}$ | $V_{42}$ | | | | | |
| 11 | 30 | 45.45 | 4.23 | 1.43 | 0.25 | 5.91 |
| 14 | 30 | 35.71 | 2.61 | 1.15 | 0.25 | 4.01 |
| 16 | 30 | 31.25 | 2.00 | 0.98 | 0.25 | 3.23 |
| 11 | 36 | 45.45 | 4.23 | 1.93 | 0.25 | 6.41 |
| 14 | 36 | 35.71 | 2.61 | 2.07 | 0.25 | 4.93 |
| 16 | 36 | 31.25 | 2.00 | 1.82 | 0.25 | 4.07 |
| 11 | 42 | 45.45 | 4.23 | 2.18 | 0.25 | 6.66 |
| 14 | 42 | 35.71 | 2.61 | 2.81 | 0.25 | 5.67 |
| 16 | 42 | 31.25 | 2.00 | 2.83 | 0.25 | 5.08 |
| 11 | 46 | 45.45 | 4.23 | 2.32 | 0.25 | 6.80 |
| 14 | 46 | 35.71 | 2.61 | 3.15 | 0.25 | 6.01 |
| 16 | 46 | 31.25 | 2.00 | 3.32 | 0.25 | 5.57 |
| 11 | 50 | 45.45 | 4.23 | 2.48 | 0.25 | 6.96 |
| 14 | 50 | 35.71 | 2.61 | 3.39 | 0.25 | 6.25 |
| 16 | 50 | 31.25 | 2.00 | 3.88 | 0.25 | 6.13 |

**Table C.4. The total inductor losses operating at full load**

| Inductor losses (W) | $V_{14}$ = 11V | $V_{14}$ = 14V | $V_{14}$ = 16V |
|---|---|---|---|
| $V_{42}$ = 30V | 5.91 | 4.01 | 3.23 |
| $V_{42}$ = 36V | 6.41 | 4.93 | 4.07 |
| $V_{42}$ = 42V | 6.66 | 5.67 | 5.08 |
| $V_{42}$ = 46V | 6.80 | 6.01 | 5.57 |
| $V_{42}$ = 50V | 6.96 | 6.25 | 6.13 |

values in the table also justify the core loss approximation. Notice that the core losses are significantly less than the copper losses and do not contribute significantly to the total inductor and integrated heat sink losses.

Table C.4 summarises the total inductor and integrated heat sink losses over the complete excitation range for operating at a temperature of 100°C.

# Appendix D

## LOSSES IN THE CAPACITORS

## 1. Introduction

The capacitor losses can be estimated with the capacitor RMS current multiplied by the ESR of the capacitor. This approach is sufficient if the full RMS current flows in the capacitor as assumed. However, the capacitance on the 42V side of the converter is implemented with the parallel combination of 6 different capacitors, 2 aluminium electrolytes and 4 ceramic capacitors distributed in space. The spatial distribution of the capacitors implies the capacitors are connected together with impedances which will redistribute the current in the capacitors. The total sum of the current in the different capacitors is still equal to the originally calculated current. The same is true on the 14V side of the converter where the capacitance is implemented with the parallel combination of one electrolytic and three ceramic capacitors.

To estimate the current distribution between the capacitors it can be assumed that the impedances interconnecting the capacitors can be neglected. However, for a more accurate estimation, these should be included. In this appendix, the current distribution between the capacitors is determined by including the impedance of the interconnecting conductors. This requires a full knowledge of the ISM structure which is presented in Chapter 7.

## 2. Calculating the currents in the $C_{42}$ capacitors

Since the current distribution between the various capacitors is of interest, the impedance of the capacitors can be measured instead of approximated with models to account for differences in the capacitors that the models would over look. Further, the impedance of the various conductors of the converter structure can be determined by calculating the conductors self-inductance, mutual-inductance and capacitance. With the impedance of the various capacitors and the structure known, mesh currents can be determined and solved for various forms of excitation. The losses in the capacitors can then be determined. This process is expanded on extensively in the following section.

### 2.1 The $C_{42}$ capacitor current model

Figure D.1 shows a simplified schematic of the converter structure true to the spatial layout of the various components. Capacitors $C_A$, $C_B$, $C_1$ to $C_4$ implement the bus capacitance and the decoupling capacitance respectively on the 42V side of the converter. Similarly, $C_D$ to $C_G$ implement the capacitance on the 14V side of the converter.

The currents in the 42V capacitors are considered first due to the significantly larger currents compared to their 14V counterparts. To simplify the model, it can be assumed that the MOSFETs can be replaced with a current source that reproduces the currents in the top MOSFETs interleaved in time. The current sources need only to provide the current that the 42V side of the converter sees, thereby allowing the 42V and the 14V side of the converter to be decoupled. The reduced model is illustrated in Figure D.2.

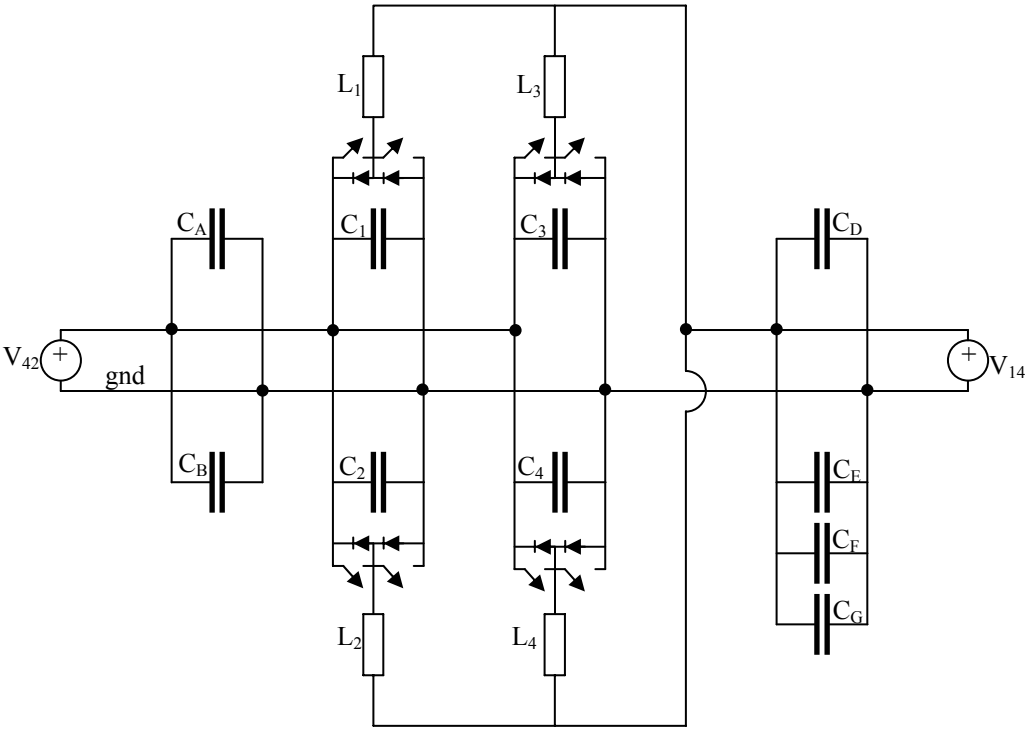



**Figure D.1. A simplified schematic of the ISM structure**

The capacitor current can be solved for using the reduced model in Figure D.2 using the currents in Figure D.3.

As mentioned previously, the impedance of the electrolytic and ceramic capacitors are measured as a function of frequency. This is done on an impedance analyser. However, the

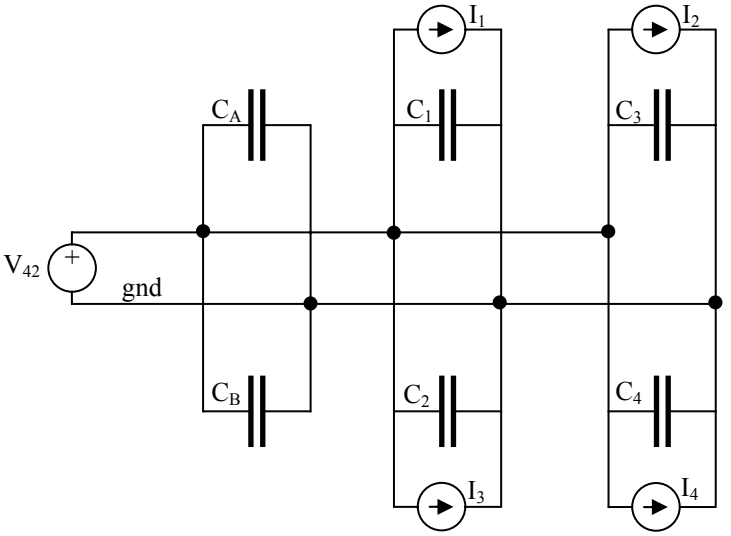



**Figure D.2. The simplified circuit used to calculate the capacitor currents**

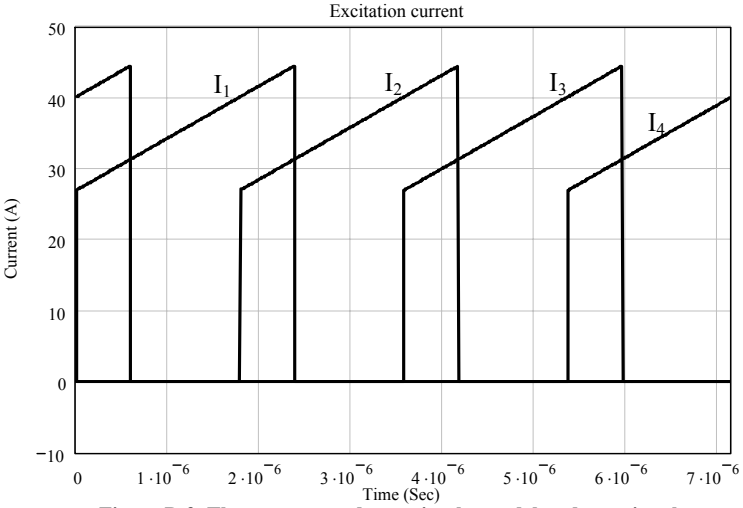



**Figure D.3. The current used to excite the model to determine the capacitor currents**

impedance analyser measures the impedance under small signal excitation. This implies that the measured impedance can only be considered as an approximation but is still considered to be better than a pure analytical model of the impedance.

The impedance is measured for the one of the two bus capacitors and for one of the four ceramic capacitors for at room temperature between the frequencies of 40Hz and 40.6Mhz. The measured impedance and phase for both the electrolytic and ceramic capacitor are plotted in Figure D.4.

There is a clear difference between the measured impedance for the ceramic and electrolytic capacitors. This is evident in both the amplitude and phase measurements. This is also expected because the ceramic capacitor has better high frequency properties than the electrolytic capacitors.

## 2.2 Determining the converter structure impedances

To determine the impedance of the various conductors the self-inductance, the mutual-inductance and the capacitance between the various conductors must be determined.

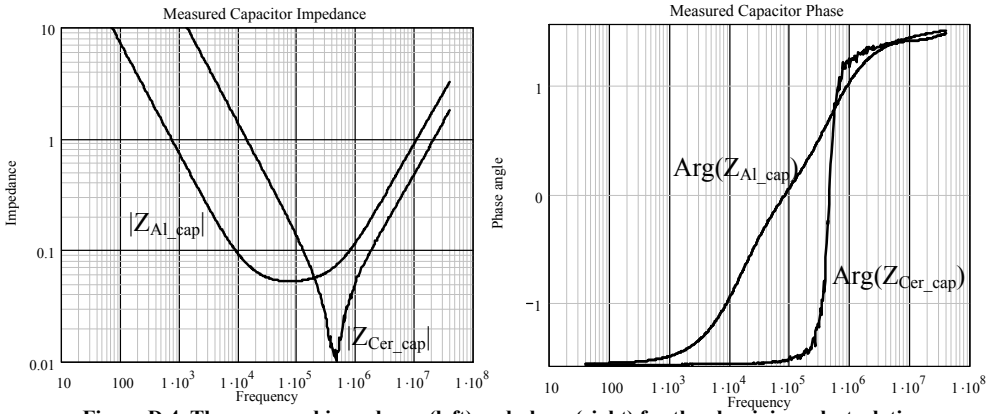



**Figure D.4. The measured impedance (left) and phase (right) for the aluminium electrolytic and ceramic capacitors**

### 2.2.1 Self-inductance of a straight conductor

The self-inductance of a single straight conductor is given by [D-1]:

$$L = 2l \cdot \left[ Ln\left(\frac{2l}{GMD}\right) - 1.25 + \frac{AMD}{l} + \frac{\mu Y}{4} \right] \quad \text{(D.1)}$$

where $L$ is the self-inductance in nano-henry (nH),
$l$ is the length of the conductors centre line,
$GMD$ is the geometric mean distance,
$AMD$ is the arithmetic mean distance,
$\mu$ is the conductors relative permeability
and $Y$ is a frequency compensation factor that varies between 1 at DC and 0 at f $\rightarrow\infty$.

The GMD of a conductor cross-section is the distance between 2 imaginary filaments normal to the cross-section, whose mutual inductance is equal to the self inductance of the conductor.

For a round conductor with a radius of $r$ the GMD is [D-1]:

$$GMD = 0.7788 \cdot r \quad \text{(D.2)}$$

For a rectangular conductor with a width of $a$ and a thickness of $b$, the GMD is:

$$GMD = 0.2232(a + b) \quad \text{(D.3)}$$

The AMD is the average of all the distances between the points of one conductor and the points of another. For a single conductor, the AMD is the average of all the possible distances within the cross-section [D-1].

For a circular conductor, the AMD is equal to the radius.

For a rectangular cross-section with a width of $a$ and a thickness of $b$, the AMD is [D-1]:

$$AMD = \frac{a + b}{3} \quad \text{(D.4)}$$

The self-inductance of a straight conductor with a radius $r$ can be determined by substituting equation D.2 into equation D. and using AMD=$r$ [D-1]:

$$L = 2l \cdot \left[ Ln\left(\frac{2l}{r}\right) - 0.75 \right] \quad \text{(D.5)}$$

assuming that $\mu=1$ and that frequencies where the inductance is calculated are relatively low making $Y \approx 1$. The radius is measured in centimeters [cm]

For a rectangular conductor, with a width of $a$ and a thickness of $b$, the self-inductance is given by:

$$L = 2l \cdot \left[ Ln\left(\frac{2l}{a+b}\right) - 0.25049 + \frac{a+b}{3l} + \frac{\mu Y}{4} \right] \tag{D.6}$$

where $a$ and $b$ are both in cm.

### *2.2.2 The mutual-inductance between parallel conductors*

The mutual inductance between two parallel conductors of the same length is given as [D-1]:

$$M = 2lQ_m \tag{D.7}$$

where $M$ is the mutual inductance between two conductors [nH],
$l$ is the length of the two conductors [cm]
and $Q_m$ is the mutual inductance parameter that is given as [1/cm]:

$$Q_m = Ln\left\{\frac{l}{GMD} + \sqrt{1 + \frac{l^2}{GMD^2}}\right\} - \sqrt{1 + \frac{l^2}{GMD^2}} + \frac{GMD}{l} \tag{D.8}$$

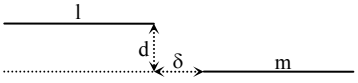
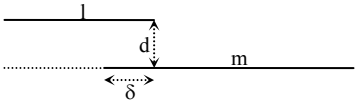
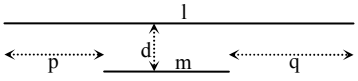
where the GMD is that between the two conductors and can be calculated as:

$$Ln\left(GMD\right) = Ln\left(d\right) - \left[ \frac{1}{12\left(\frac{d}{w}\right)^2} + \frac{1}{60\left(\frac{d}{w}\right)^4} + \frac{1}{168\left(\frac{d}{w}\right)^6} + \frac{1}{360\left(\frac{d}{w}\right)^8} + \frac{1}{660\left(\frac{d}{w}\right)^{10}} + \cdots \right] \tag{D.9}$$

where $d$ is the distance between the centre lines of the two conductors [cm],
and $w$ is the width of the conductor [cm].

If the conductors are not of equal length, then the mutual-inductance calculation must be modified as illustrated in Table D.1.

**Table D.1. The mutual inductance for overlapping conductors [D-2]**

| | |
|---|---|
| Non-overlapping   | $M = \frac{1}{2}\left[\left(M_{l+m+\delta} + M_{\delta}\right) - \left(M_{l+\delta} + M_{m+\delta}\right)\right]$ |
| Partly overlapping   | $M = \frac{1}{2}\left[\left(M_{l+m-\delta} + M_{\delta}\right) - \left(M_{l-\delta} + M_{m-\delta}\right)\right]$ |
| Fully overlapping   | $M = \frac{1}{2}\left[\left(M_{m+p} + M_{m+q}\right) - \left(M_{p} + M_{q}\right)\right]$ |

### 2.2.3 Total inductance

The total inductance of a set of conductors is determined by the sum of the self-inductance of each conductor and the mutual-inductance, both positive and negative. The mutual-inductance between two conductors is positive when the current flows in the same direction in both conductors and is negative when the current flows in the opposite direction. The total inductance can be summarised as:

$$L_T = L_0 + \sum M_+ + \sum M_- \tag{D.10}$$

where $L_T$ is the total inductance [H],
$L_o$ is the total self-inductance of the straight conductors [H],
$M_+$ is the positive mutual-inductance [H]
and $M_-$ is the negative mutual-inductance [H].

### 2.2.4 Structure capacitance

The structure capacitance can be determined by considering the structure illustrated in Figure D.5. The figure shows two copper conductors mounted on the base heat sink isolated by a very thin layer of Kapton™ material. Due to the large area of the copper conductors, and the capacitive properties of the isolation material, a relatively large capacitance exists between the conductor and the heat sink. This is true for each conductor. There is also a smaller capacitance between the two conductors through the air separating the conductors.

The capacitance is given as [D-3]:

$$C = \frac{\varepsilon A}{d} \tag{D.11}$$

where $\varepsilon = \varepsilon_0 \cdot \varepsilon_r$ is the permittivity of the dielectric material with $\varepsilon_r$ being the relative permittivity [F/m],
$A$ is the area of the dielectric [$m^2$]
and $d$ is the distance between the two conductors [m].

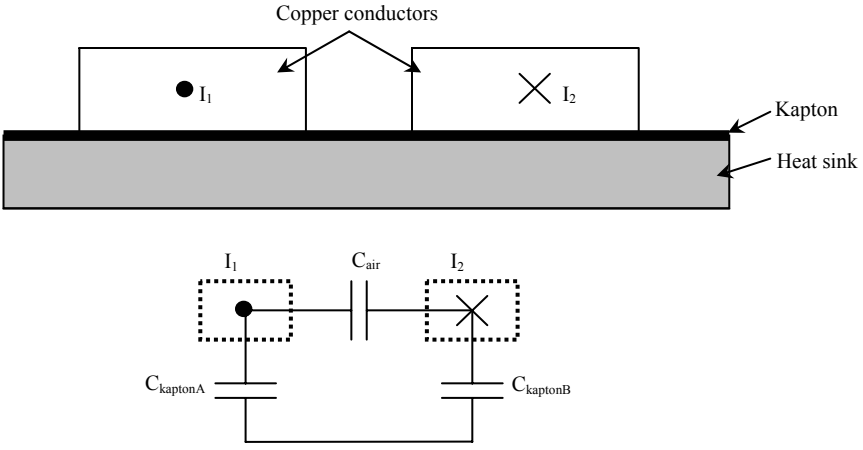



**Figure D.5. A cross-section through 2 conductors showing the three main coupling capacitors**

In Figure D.5, the dielectric is either the air between the two conductors, or the kapton isolation material.

The total capacitance between the two conductors is given as:

$$C_{total} = C_{air} + \frac{C_{kaptonA} \cdot C_{kaptonB}}{C_{kaptonA} + C_{kaptonB}} \tag{D.12}$$

### *2.2.5 The converter structure impedances*

Figure D.6 shows the a simplified schematic of the converter structure connecting the 6 capacitors and the current sources representing the MOSFETs. The figure also identifies 10 impedances that need to be defined to determine the current sharing between the capacitors. An additional impedance, labelled $Z_{Lcon}$ is also included in series with the $V_{42}$ power supply. This impedance decouples the capacitor currents from the supply currents. In reality, the impedance represents the cable impedance connecting the converter to the supply.

Figure D.7 shows the same circuit diagram as in Figure D.6, but in terms of the structure impedances. With all of the impedances known, 27 mesh currents can be defined and solved simultaneously to determine the currents in each of the capacitors.

The impedances are listed in Table D.2.

## 2.3 Calculating the $C_{42}$ capacitor currents

Using the impedances given in Table D.2 and in Figure D.4, the capacitor currents can be solved for. However, the impedance is a function of frequency so it is simplest to solve for the capacitor currents in the frequency domain. To do this, the excitation current is transferred into the frequency domain where the harmonic components are calculated for integer multiples of the switching frequency of 140kHz. The current harmonics amplitude and phase for nominal

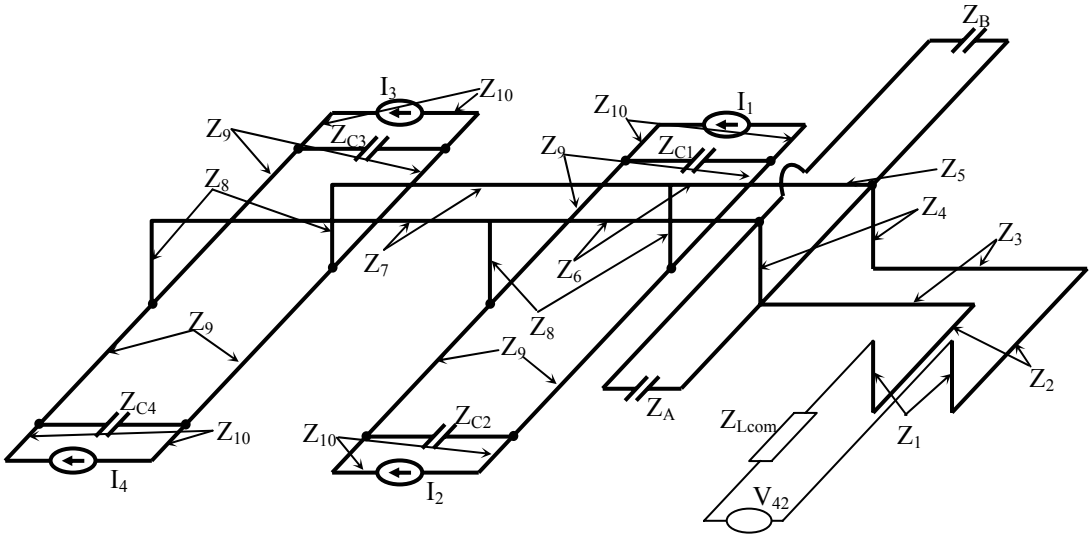



**Figure D.6. The spatial connection and definition of the impedances connecting the 6 capacitors together**

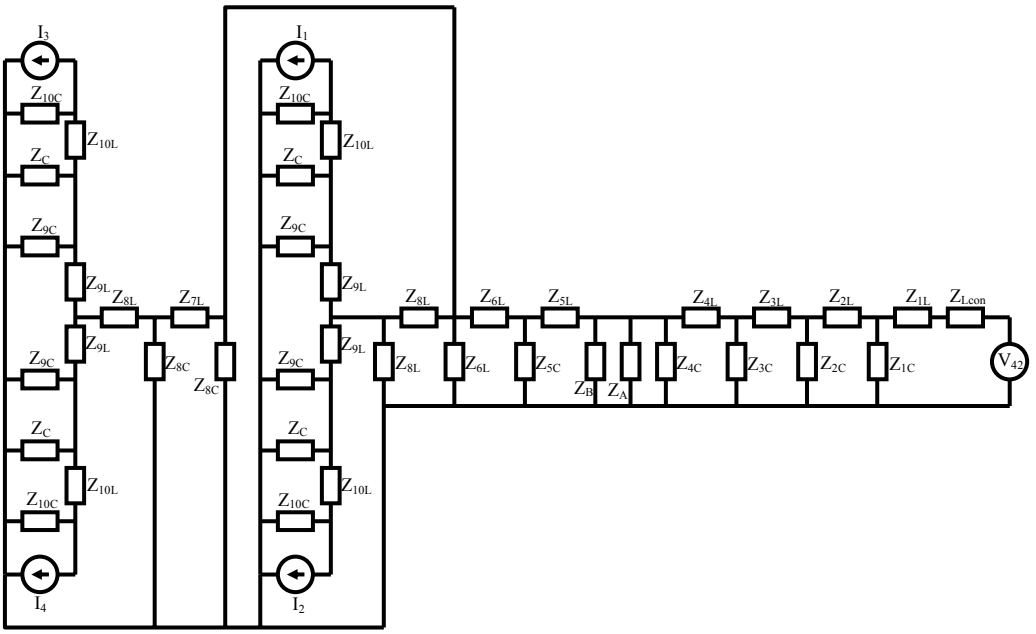



**Figure D.7. The equivalent circuit diagram in terms of the structure inductive and capacitive impedances**

**Table D.2. The calculated impedances for the structure shown in Figure D.6 and Figure D.7**

| Inductive impedance [Ω] | | Capacitive impedance [Ω] | | Inductive impedance [Ω] | | Capacitive impedance [Ω] | |
|---|---|---|---|---|---|---|---|
| $Z_{1L}$ | $1.7\cdot10^{-5}+j\omega2.5\cdot10^{-9}$ | $Z_{1C}$ | $-j\omega8.3\cdot10^{-14}$ | $Z_{6L}$ | $5\cdot10^{-5}+j\omega8.14\cdot10^{-9}$ | $Z_{6C}$ | $-j\omega1.5\cdot10^{-9}$ |
| $Z_{2L}$ | $9.7\cdot10^{-5}+j\omega18.9\cdot10^{-9}$ | $Z_{2C}$ | $-j\omega3\cdot10^{-11}$ | $Z_{7L}$ | $5\cdot10^{-5}+j\omega2.5\cdot10^{-9}$ | $Z_{7C}$ | $-j\omega1.5\cdot10^{-9}$ |
| $Z_{3L}$ | $4\cdot10^{-5}+j\omega11.2\cdot10^{-9}$ | $Z_{3C}$ | $-j\omega2.3\cdot10^{-11}$ | $Z_{8L}$ | $5\cdot10^{-5}+j\omega1.1\cdot10^{-9}$ | $Z_{8C}$ | $-j\omega3.9\cdot10^{-13}$ |
| $Z_{4L}$ | $5.17\cdot10^{-6}+j\omega3.1\cdot10^{-9}$ | $Z_{4C}$ | $-j\omega1\cdot10^{-11}$ | $Z_{9L}$ | $1.24\cdot10^{-4}+j\omega5.5\cdot10^{-9}$ | $Z_{9C}$ | $-j\omega9.7\cdot10^{-12}$ |
| $Z_{5L}$ | $3.5\cdot10^{-5}+j\omega5.18\cdot10^{-9}$ | $Z_{5C}$ | $-j\omega1.1\cdot10^{-11}$ | $Z_{10L}$ | $8\cdot10^{-5}+j\omega7\cdot10^{-9}$ | $Z_{10C}$ | $-j\omega1.1\cdot10^{-11}$ |

operation of 42V to 14V volts are plotted in Figure D.8a and Figure D.8b respectively.

The analysis uses the first 290 harmonics of the MOSFET current to determine the capacitor currents. The first 290 harmonics are used due to the limited impedance measurement of the capacitor impedances. The highest harmonic is 290·140kHz = 40.6MHz.

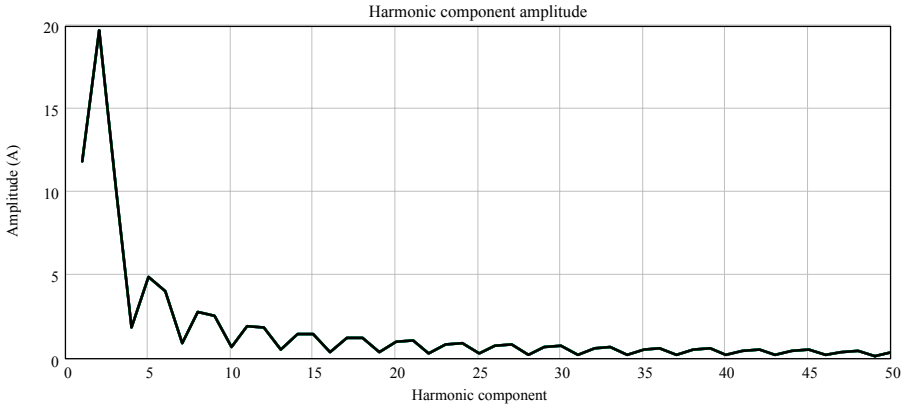



**Figure D.8a. The excitation current amplitude for the first 50 harmonics**

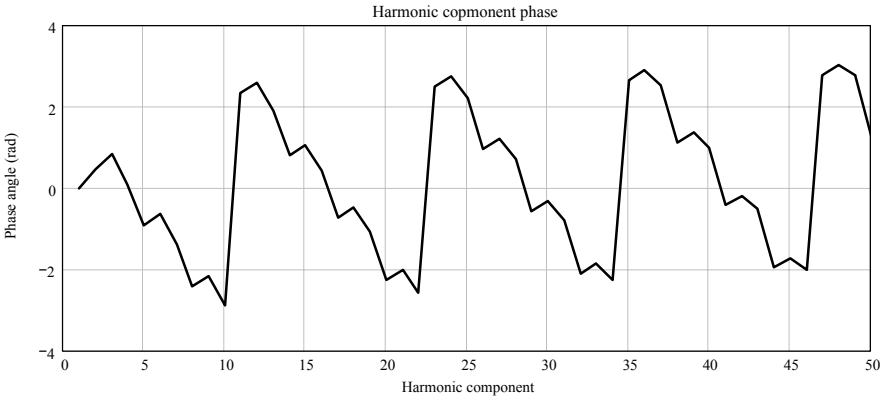



**Figure D.8b. The phase of the first 50 harmonics for $I_1$**

### *2.3.1 The calculated currents in the $C_{42}$ capacitors*

The calculated current in one of two the electrolytic capacitors is plotted in Figure D.9. From the figure it can be seen that the amplitude of the current in the capacitors is not very high. The small difference in the amplitude of the peak currents flowing into and out of the capacitors are due to the distance between the capacitors and the 4 phase arms.

Figure D.10 shows the calculated current in two of the 4 ceramic capacitors (capacitor $C_1$ and $C_3$ in Figure D.1). The 4 capacitor currents all show similar behaviour. The ceramic capacitors support each other during every switching event distributing the current between them thereby reducing the RMS currents in the capacitors. The difference in the amplitude of the currents depends on how far the capacitor is from the phase arm that needs the current. The difference is due to the impedance between the current sources and the capacitors.

To ensure that the calculated currents are correct, an instantaneous sum of the 6 capacitor currents can be taken and compared to the theoretical capacitor current for an ideal capacitor

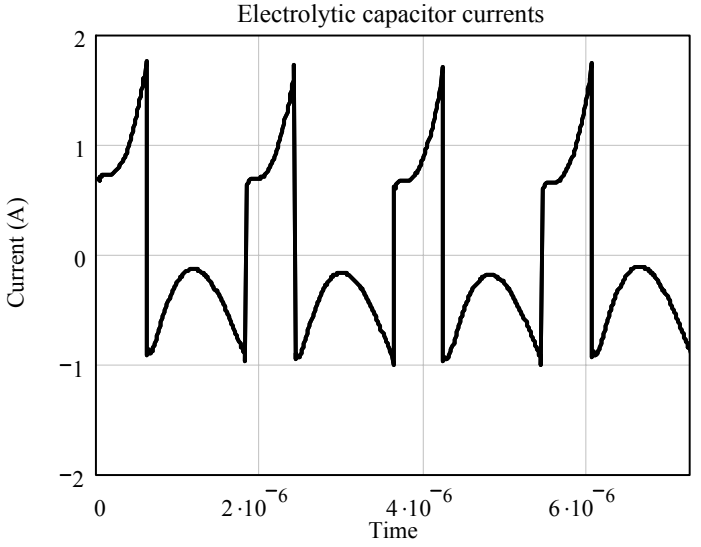



**Figure D.9. The calculated current in the electrolytic capacitors**

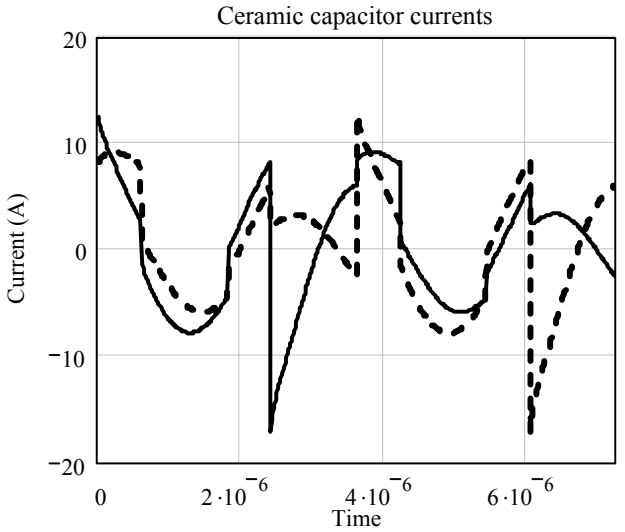



**Figure D.10. The calculated current flowing in 2 of the 4 ceramic capacitors ($C_1$ – solid, $C_3$ - dashed)**

taking into consideration the interleaving between the phases. This result is plotted in Figure D.11 showing the sum of the capacitor currents superimposed on the theoretical interleaved capacitor current. The calculated and theoretical current correlate very well.

The RMS currents in the 6 capacitors as well as for the ideal capacitor waveform are calculated and tabulated in Table D.3. The table also shows that there is a difference in the RMS currents in $C_{1,2}$ and $C_{3,4}$, with the latter being larger. This is because $C_3$ and $C_4$ are physically further away from the electrolytics than $C_1$ and $C_2$. This means that they are not as well supported and need to provide more current to the switching devices. The larger current is basically due to the geometrical distance between the ceramic and the electrolytic capacitors.

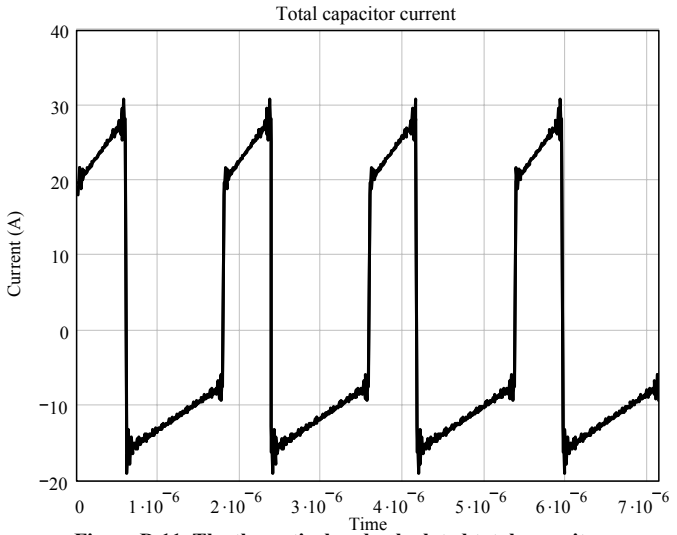



**Figure D.11. The theoretical and calculated total capacitor current superimposed on each other**

**Table D.3. The calculated RMS currents in the capacitors forming $C_{42}$**

| RMS current | Ampere (A) | | RMS current | Ampere (A) |
|---|---|---|---|---|
| $I_{RMS\_C42}$ ideal waveform | 17.031 | | $I_{RMS\_A}$ | 0.713 |
| $I_{RMS\_C42}$ harmonic limited | 17.018 | | $I_{RMS\_B}$ | 0.713 |
| $I_{RMS\_C1}$ | 5.7 | | $I_{RMS\_C3}$ | 5.8 |
| $I_{RMS\_C2}$ | 5.7 | | $I_{RMS\_C4}$ | 5.8 |

## 2.4 Calculated losses in the $C_{42}$ capacitors

Using the measured impedance, the losses in the capacitors can be approximated now that the current distribution between the capacitors is known. The total capacitor losses are tabulated in Table D.4 as a function of the converter terminal voltages for the converter operating with all 4 phases and ideal current sharing between the phases. The capacitor losses vary between just over 1.7W to just under 4.4W.

Table D.5 tabulates the losses in $C_1$, one of the 4 ceramic capacitors. The loss distribution between the 4 ceramic capacitors is not ideal with the capacitors $C_3$ and $C_4$ having higher losses that $C_1$ and $C_2$. The increase in the losses is due to the ceramic capacitors $C_3$ and $C_4$ being physically further away from the electrolytic capacitors than $C_1$ and $C_2$.

Table D.6 tabulates the losses in one of the two aluminium electrolytic capacitors. The losses in the two capacitors are identical. As can be seen from the table, the losses in the capacitors are significantly low. This is due to the interleaving of the four phases that has reduced the RMS currents in the capacitors significantly.

**Table D.4. The total calculated losses in $C_{42}$ for 4-phase operation**

| Total $C_{42}$ Losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 3.40 | 3.39 | 3.50 | 3.42 | 3.46 | 4.35 |
| $V_{14}$=14V | 2.50 | 2.30 | 2.17 | 2.17 | 2.24 | 2.29 |
| $V_{14}$=16V | 1.93 | 1.96 | 1.83 | 1.78 | 1.74 | 1.77 |

**Table D.5. The calculated losses in $C_1$, one of the 4 ceramic decoupling capacitors implementing $C_{42}$ for 4-phase operation**

| Ceramic cap losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 0.84 | 0.82 | 0.89 | 0.89 | 0.93 | 1.18 |
| $V_{14}$=14V | 0.68 | 0.59 | 0.53 | 0.53 | 0.55 | 0.58 |
| $V_{14}$=16V | 0.53 | 0.53 | 0.47 | 0.45 | 0.43 | 0.44 |

**Table D.6. The calculated losses in one of the two electrolytic capacitors implementing $C_{42}$ for 4-phase operation**

| Electrolytic cap losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 0.06 | 0.06 | 0.05 | 0.03 | 0.02 | 0.05 |
| $V_{14}$=14V | 0.03 | 0.04 | 0.04 | 0.04 | 0.04 | 0.03 |
| $V_{14}$=16V | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 |

**Table D.7. The total calculated losses in $C_{42}$ for 1-phase operation**

| Total $C_{42}$ Losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 6.78 | 6.06 | 5.42 | 5.18 | 4.87 | 4.43 |
| $V_{14}$=14V | 4.80 | 4.48 | 4.10 | 3.97 | 3.76 | 3.46 |
| $V_{14}$=16V | 3.72 | 3.71 | 3.48 | 3.38 | 3.24 | 2.99 |

**Table D.8. The calculated losses in $C_3$, one of the 4 ceramic decoupling capacitors implementing $C_{42}$ for 1-phase operation**

| Ceramic cap losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 0.74 | 0.72 | 0.78 | 0.81 | 0.85 | 0.92 |
| $V_{14}$=14V | 0.59 | 0.51 | 0.46 | 0.46 | 0.47 | 0.50 |
| $V_{14}$=16V | 0.46 | 0.46 | 0.41 | 0.39 | 0.38 | 0.38 |

**Table D.9. The calculated losses in one of the two electrolytic capacitors implementing $C_{42}$ for 1-phase operation**

| Electrolytic cap losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 2.62 | 2.22 | 1.86 | 1.73 | 1.56 | 1.33 |
| $V_{14}$=14V | 1.91 | 1.75 | 1.55 | 1.48 | 1.36 | 1.19 |
| $V_{14}$=16V | 1.48 | 1.47 | 1.35 | 1.30 | 1.22 | 1.08 |

To illustrate the effect that interleaving has on the RMS currents and thus losses on the capacitors, the capacitor loss model can be used to determine the losses in the capacitors if only one of the 4 phases were operated at a rated power of 500W. That is to say, if only one of the four phases operates at its rated power. The result of the calculation is tabulated in Table D.7 through to Table D.9 for the phase with $C_3$ being excited.

Table D.7 shows the total losses in all the capacitors that make up $C_{42}$ when the topology is operated with only one phase. Comparing Table D.7 to Table D.4 it can be seen that the total losses are larger with single phase excitation compared to the four phases excitation. For a single phase topology to have the same rated power of 2kW, the capacitor losses are going to be significantly larger requiring larger components.

Table D.8 tabulates the losses in $C_3$, the ceramic capacitor in the phase being excited. The losses in this capacitor are significantly higher than in the remaining three ceramic capacitors. The remaining three capacitors do support $C_3$ but because of the impedances between the capacitors, the switching current is primarily limited to $C_3$.

The losses in one of the two aluminium electrolytic capacitors is tabulated in Table D.9 for single phase operation. Comparing Table D.6 to Table D.9 it can be seen that the losses in exactly the same aluminium electrolytic capacitor are between 25 to 50 times greater for single phase operation compared to 4-phase operation. This clearly illustrates the advantages achieved through interleaving.

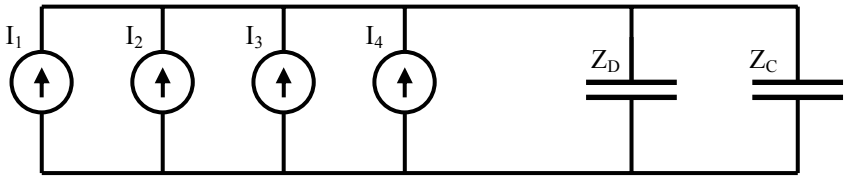



**Figure D.12. The simplified model used to calculate the current in the 14V capacitors**

## 3. Losses in the $C_{14}$ capacitors

Following a similar procedure the currents and losses for the 14V bus electrolytic and decoupling capacitors can be calculated. However, since the current in these capacitors are considerably smaller than that in $C_{42}$, the current calculation can be simplified. For example, since the capacitors are very close to each other, it is not necessary to take the converter's structure surrounding the capacitors into account. A very simple model, consisting of a parallel combination of the measured impedances excited by the parallel combination of 4 current sources can be used to calculate the currents in the capacitors.

The model used to calculate the current in the bus and decoupling capacitor is illustrated in Figure D.12. The 4 current sources model the inductor currents that are interleaved in time. The current sources do not include the DC components since ideally, the DC current does not affected the capacitors. In Figure D.12 $Z_D$ is the aluminium electrolytic bus capacitor impedance corresponding to $C_D$ in Figure D.1 and $Z_C$ be the combined impedance of the ceramic capacitors $C_{E\text{-}F\text{-}G}$ in the same figure.

As in the case of the 42V capacitors, the capacitors are excited by the Fourier components of the excitation current. The current in the capacitors are determined for a range of frequencies. The currents in the capacitors can then be reconstructed and the RMS and losses can be determined.

### 3.1 The currents in the $C_{14}$ capacitors

The current in the two capacitors at the various harmonic frequencies can be determined with the current divider rule. The currents in the two capacitors are:

$$I_{D_h} = \frac{Z_{C_h}}{Z_{C_h} + Z_{D_h}} \cdot \left( I_{1_h} + I_{2_h} + I_{3_h} + I_{4_h} \right) \tag{D.13}$$

and

$$I_{C_h} = \frac{Z_{D_h}}{Z_{C_h} + Z_{D_h}} \cdot \left( I_{1_h} + I_{2_h} + I_{3_h} + I_{4_h} \right) \tag{D.14}$$

where $I_D$ is the current in the bus capacitor for the $h^{th}$ harmonic,
$I_C$ is the current in the decoupling capacitor for the $h^{th}$ harmonic,
and $I_1$ to $I_2$ are the $h^{th}$ harmonic of the excitation current.

**Table D.10. The losses in the $C_{14}$ aluminium electrolytic capacitor**

| Total $C_{14}$ Losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 0.016 | 0.054 | 0.034 | 0.01 | 0.01 | 0.073 |
| $V_{14}$=14V | 0.029 | 0.027 | 0.035 | 0.055 | 0.099 | 0.073 |
| $V_{14}$=16V | 0.029 | 0.052 | 0.035 | 0.032 | 0.047 | 0.106 |

**Table D.11. The losses in the $C_{14}$ Ceramic capacitors**

| Ceramic cap losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 0.021 | 0.059 | 0.035 | 0.01 | 0.011 | 0.021 |
| $V_{14}$=14V | 0.03 | 0.033 | 0.043 | 0.062 | 0.105 | 0.03 |
| $V_{14}$=16V | 0.03 | 0.054 | 0.043 | 0.041 | 0.057 | 0.03 |

### 3.2 The calculated losses in the 14V capacitors

The losses in the 14V capacitors can be calculated with the capacitor impedance and currents. The calculated losses in the aluminium electrolytic capacitor are tabulated in Table D.10 and for the ceramic capacitors in Table D.11. The tables shows that the losses in the 14V capacitors are almost negligible. This is because the current ripple in the capacitor's current are very small.

## 4. Experimental evaluation

To evaluate the capacitor RMS current and loss model, the model is used to calculate the losses in the capacitors and then the losses are experimentally measured and compared to that predicted.

Comparing Table D.4 to Table D.6 and Table D.7 to Table D.9 it can be noticed that the aluminium electrolytic capacitors, when excited with a single phase show the largest losses. Due to the largest losses being in the aluminium electrolytic capacitors and the structure of the experimental realisation of the 4-phase ISM, it is decided to measure the combined losses in the two aluminium electrolytic capacitors under single phase excitation. The model can be excited under the same conditions and the predicted losses in the aluminium electrolytic capacitors can be compared to the measured values.

The losses in the two capacitors are measured in the same way as the inductor losses in Chapter 5. The two capacitors, in their integrated heat sink structures are placed on a heat spreader with known dimensions. A heat flux sensor is placed between the heat spreader and the infinite heat sink. The capacitor structures are then thermally isolated from the surrounding environment with isolation material as illustrated in Figure 5.19. The capacitors are then excited by the ISM. The output voltage of the heat flux sensor (the thermopile) is then compared to a calibration curve created with a known heat source on the same heat spreader. The losses in the ceramic capacitors are not measured because these devices are soldered very close to the MOSFETs and is not possible to de-solder them to remake the connection with them thermally isolated.

The two aluminium electrolytic capacitors are excited with a single phase. The phase selected to excite the capacitors is the phases in parallel with $C_3$, also referred to as B1 in Chapter 8. This phases is selected because it is one of the two phases furthest from the electrolytic

**Table D.12. The measured and calculated RMS current and losses in the two aluminium electrolytic capacitors for excitation for only one phase**

| $V_{42}$ [V] | $I_{42}$ [A] | $V_{14}$ [V] | $I_{14}$ [A] | $P_{14}$ [W] | Eff [%] | Capacitor Losses | | | RMS current | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Meas [W] | Model [W] | Error [%] | Meas [A] | Model [A] | Error [%] |
| 50.2 | 11.2 | 16.3 | 31.3 | 508.5 | 90.5 | 2.33 | 2.20 | -6.25 | 4.50 | 4.54 | 0.88 |
| 50.2 | 11.6 | 14.5 | 35.4 | 513.5 | 88.6 | 2.58 | 2.43 | -6.40 | 4.86 | 4.77 | -1.80 |
| 50.2 | 11.9 | 11.3 | 45.3 | 511.2 | 85.6 | 2.98 | 2.74 | -9.04 | 5.40 | 5.07 | -6.59 |
| 45.3 | 12.7 | 16.3 | 32.2 | 524.2 | 91.6 | 2.67 | 2.62 | -1.73 | 4.95 | 4.96 | 0.26 |
| 45.3 | 12.5 | 14.4 | 35.3 | 508.3 | 89.8 | 2.87 | 2.72 | -5.55 | 5.17 | 5.05 | -2.38 |
| 45.3 | 12.9 | 11.2 | 45.2 | 504.4 | 86.4 | 3.32 | 3.12 | -6.46 | 5.77 | 5.41 | -6.73 |
| 42.3 | 13.7 | 16.4 | 32.5 | 530.9 | 91.6 | 2.76 | 2.61 | -5.72 | 5.20 | 4.95 | -5.01 |
| 42.3 | 13.1 | 14.2 | 35.8 | 508.1 | 92.1 | 2.98 | 2.97 | -0.12 | 5.43 | 5.28 | -2.84 |
| 42.3 | 13.9 | 11.1 | 45.8 | 508.0 | 86.4 | 3.66 | 3.50 | -4.48 | 6.00 | 5.73 | -4.71 |
| 40.8 | 13.3 | 16.1 | 31.0 | 500.4 | 92.3 | 2.62 | 2.65 | 1.06 | 4.80 | 4.98 | 3.61 |
| 40.8 | 13.7 | 14.4 | 35.2 | 505.6 | 90.6 | 3.09 | 3.03 | -1.83 | 5.32 | 5.34 | 0.32 |
| 40.8 | 14.2 | 11.2 | 45.2 | 505.0 | 87.3 | 3.70 | 3.65 | -1.21 | 6.13 | 5.85 | -4.71 |
| 35.1 | 15.3 | 16.1 | 31.6 | 508.3 | 94.9 | 2.79 | 2.99 | 6.88 | 5.27 | 5.30 | 0.60 |
| 35.1 | 15.7 | 14.4 | 35.2 | 507.1 | 92.1 | 3.21 | 3.43 | 6.27 | 5.90 | 5.72 | -3.15 |
| 35.7 | 16.0 | 11.2 | 45.1 | 505.1 | 88.5 | 4.10 | 4.32 | 5.10 | 6.75 | 6.37 | -5.98 |
| 30.2 | 17.9 | 16.2 | 31.4 | 507.7 | 93.9 | 2.63 | 2.96 | 11.08 | 4.89 | 5.28 | 7.28 |
| 30.2 | 19.1 | 14.9 | 35.5 | 527.8 | 91.5 | 3.41 | 3.81 | 10.46 | 5.65 | 5.98 | 5.53 |
| 30.4 | 18.8 | 11.1 | 45.0 | 500.1 | 87.6 | 4.58 | 5.12 | 10.47 | 7.03 | 6.94 | -1.36 |

capacitors and thus will experience the greatest effect of the impedance of the conductors between the phase and the electrolytic capacitors.

The measured combined losses in the two electrolytic capacitors and the measured RMS current in one electrolytic capacitor are tabulated in Table D.12. The table also tabulates the terminal voltages, currents and output power for each measurement. These parameters are used to excite the analytical model.

The table shows good correlation between the measured and modelled losses and RMS currents in the capacitors with all the trends agreeing. The difference between the modelled and measure losses varies between -9% and +10% while for the RMS current, the difference varies between -7% and +7%.

The variation in the measured and modelled losses is acceptable considering the losses in the capacitors are calculated based on the small signal impedance measurement and the model ignores the effects of reverse recovery.

## 5. References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# Appendix E

## LOSSES IN THE MOSFETS

## 1. Introduction

In this appendix, the losses in the two MOSFETs that make up a phase arm are identified and calculated. The topology in which the MOSFETs are implemented is illustrated in Figure E.1. The losses in the devices must be known so that the operating temperature of the devices for a given construction can be determined. In this appendix, the various losses in the MOSFETs are identified and calculated. The loss derivation is then used to determine the losses in the phase arm under nominal operating conditions.

## 2. Semi-conductor losses

The losses in the two MOSFETs can be grouped into four categories as listed below [E-1][E-2][E-3][E-4]:

1. switching losses,
2. conduction losses,
3. gate charge losses, and
4. diode losses.

The diode losses further consist of diode conduction losses and reverse recovery losses. Each of these are considered in detail in this appendix.

### 2.1 Switching losses including the effects of reverse recovery

The switching losses consist of both turn on and turn off losses. $SW_1$ is a hard-switching device but $SW_2$ is switched under zero voltage conditions because the device's body diode conducts both immediately before the device is turned on and after the device is turned off. Thus, $SW_1$ is the only contributor to the switching losses, both turning on and off.

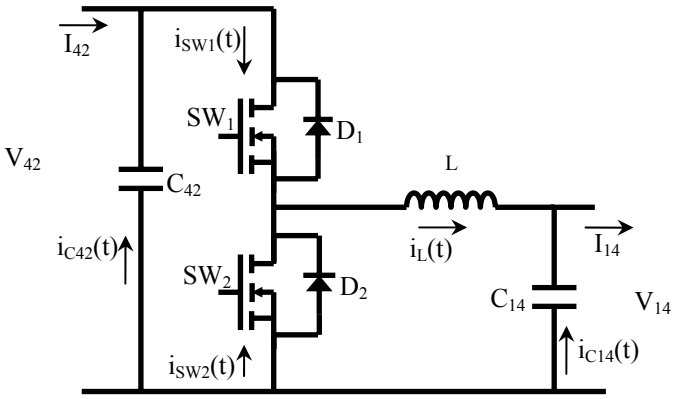


**Figure E.1. The synchronous rectified bi-directional phase arm**

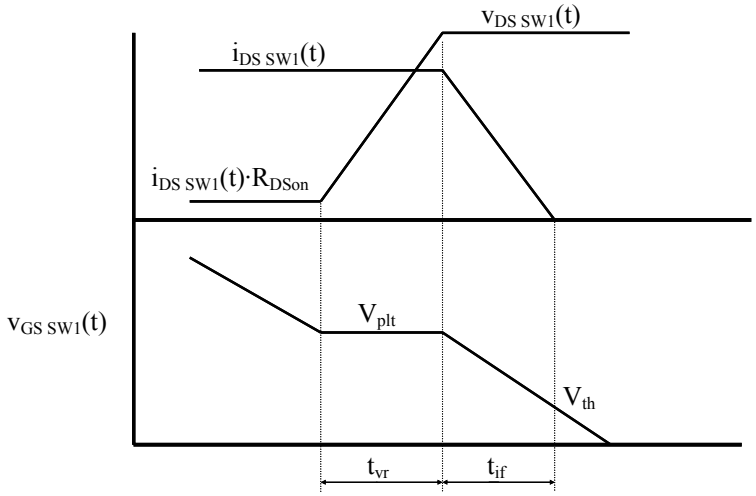


**Figure E.2. The turn off transition of $SW_1$**

To include the effects of the diode, $D_2$, reverse recovery, the turn on and turn off transitions are considered separately.

### *2.1.1 $SW_1$ Turn Off losses*

The losses in $SW_2$ during the device turn off based on Figure E.2 are given by [E-1][E-2] [E-3][E-4]:

$$P_{SW1(off)} = \frac{I_d V_s \left(t_{if} + t_{vr}\right)}{2} f_s \tag{E.1}$$

where $P_{SW1(off)}$ is the turn off losses in $SW_1$ [W],
$f_s$ is the switching frequency [Hz],
$t_{ir}$ and $t_{vf}$ are the current rise time and voltage fall time respectively [s]
and $V_s$ is the supply voltage [V]

The time intervals $t_{if}$ and $t_{vr}$ must be determined and can not be used directly from the device data sheet because the values given in the data sheet are for specific conditions which are not the same as in the converter. The time intervals are illustrated in Figure E.2.

The time intervals can be calculated be considering the time taken to discharge the gate charge. The time taken for the voltage to rise to the supply voltage is calculated as [E-4]:

$$t_{vr} = \frac{Q_{gd}}{I_{gate\_driver}} = \frac{Q_{gd}}{\dfrac{V_{plt}}{R_{gate} + R_{gate\_driver}}} \tag{E.2}$$

where $Q_{gd}$ is the gate drain charge from the MOSFET's data sheet [C],
$I_{gate\ driver}$ is the current the gate driver can sink to discharge the gate charge [A],
$V_{plt}$ is the plateau voltage of the gate voltage, also taken from the data sheet [V],
$R_{gate}$ is the additional gate resistance in series with the gate [Ω]
and $R_{gate\ driver}$ is the internal resistance of the gate driver [Ω].

The current fall time can be calculated by considering the time taken for the $C_{gs}$ capacitor to discharge exponentially from $V_{plt}$ to $V_{th}$. The gate source capacitance can be read from the data sheet as $C_{iss}$ [E-4]. The current fall time is calculated as:

$$t_{if} = \left(R_{gate\_driver} + R_{gate}\right) \cdot C_{iss} \cdot Ln\left(\frac{V_{th} - V_{gate}}{V_{plt} - V_{gate}}\right) \tag{E.3}$$

where $C_{iss}$ is the gate source capacitance [C],
$V_{th}$ is the gate threshold voltage [V]
And $V_{gate}$ is the gate voltage [V].

### 2.1.2 $SW_1$ Turn on losses including reverse recovery effects

When $SW_1$ turns on, the diode $D_2$, experiences reverse recovery. The reverse recovery current flows through $D_2$ as well as the drain source of $SW_1$ increasing the switching losses. Additionally, the revere recovery current significantly effects the total turn on time of $SW_1$. Consider Figure E.3. When the gate voltage is applied, the gate source voltage increases exponentially from zero to the gate source voltage required for the sum of the drain source current and the reverse recovery current [E-4]. The time taken for this interval can be considered in two parts, first $t_{ir}$, the time taken for the gate source voltage to rise from the threshold voltage to the plateau voltage for the drain source current without the reveres recovery current. This time interval is calculated as in the case of the device turn off:

$$t_{ir} = \left(R_{gate\_driver} + R_{gate}\right) \cdot C_{iss} \cdot Ln\left(\frac{V_{th} - V_{gate}}{V_{plt} - V_{gate}}\right) \tag{E.4}$$

The second time interval, $t_{rr1}$ is the first time interval of the reverse recovery current. This time interval is approximated assuming that the current rise *di/dt* remains constant as the current increases to the sum of the drain source current and the reverse recovery current [E-2]. The time interval can then be determined if the reverse recovery current is known. The time interval

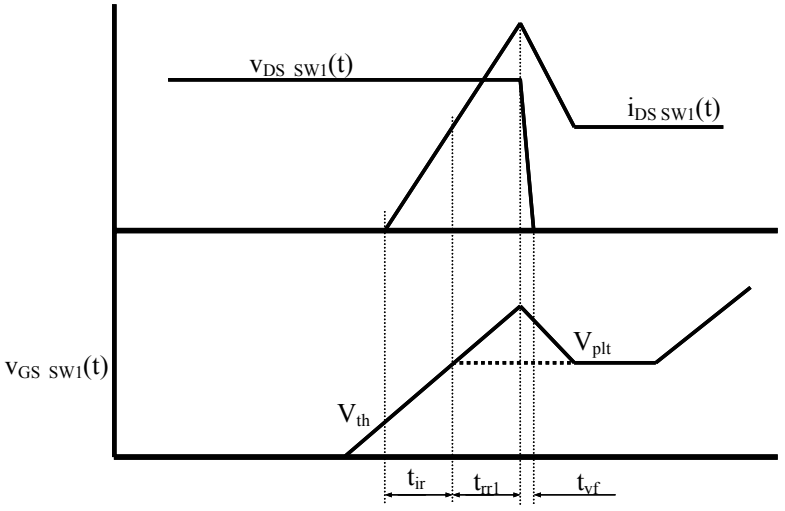


**Figure E.3. The turn on transition of $SW_1$ including reverse recovery**

can be approximated as:

$$t_{rr1} = \frac{I_{rr}}{\frac{I_{DS\_SW1}}{t_{ir}}} \tag{E.5}$$

where $I_{rr}$ is the peak revere recovery current [A],
$I_{DS\_SW1}$ is the turn on drain source current [A],
$t_{ir}$ is the current rise time [s]
and $t_{rr1}$ is the first interval of the diode reverse recovery current [s].

This approach requires that the diode reverse recovery current is known. This can be determined experimentally.

Once the current in $SW_1$ has reached its peak value, the diode reverse recovery current decreases to zero quickly, resulting in the current in $SW_1$ to return to the inductor current value. This fast drop in the drain source current results in the corresponding drop in the gate voltage to the plateau voltage required for the inductor current. However, the diode reverse recovery current assists the gate driver during this interval helping to further discharge the gate drain capacitance. The result is that the drain source voltage drops very quickly. The voltage fall time can be approximated as:

$$t_{vf} = \frac{Q_{gd}}{I_{gate\_driver} + I_{rr}} = \frac{Q_{gd}}{\frac{V_{gate} - V_{plt}}{R_{gate} + R_{gate\_driver}} + I_{rr}} \tag{E.6}$$

The turn on losses in $SW_1$ can then be determined as [E-3]:

$$P_{SW1(on)} = \frac{(I_d + I_{rr})V_s(t_{ir} + t_{vf} + t_{rr1})}{2} f_s \tag{E.7}$$

where $t_{if}$ and $t_{vr}$ are the current fall time and voltage rise time respectively [s].

It might be necessary to adjust the voltage in equation E.7 if the inductance in series with the device is significant. When the current increases, the di/dt is significant and will result in a voltage drop over any series inductance. The voltage over the switching device is then the supply voltage less the voltage drop across the series inductance.

The total switching losses in $SW_1$ can then be determined by taking the sum of equations E.1 and E.7.

### 2.2 Conduction losses

The conduction losses for the two devices depend on the current in the device and the on resistance of the device. The total conduction losses will be obtained from the sum of the conduction losses of the two devices. The conduction losses can be determined from:

$$P_{conduction(SW1)} = I_L^2 R_{DS\_on} D \tag{E.8}$$

and

$$P_{conduction(SW2)} = I_L^2 R_{DS\_on}(1-D) \tag{E.9}$$

where $D$ is the duty cycle of $SW_1$
and $I_L$ is the average inductor current [A].

It must also be remembered that the on resistance of the MOSFET channel is a function of the channel temperature. The conduction losses can increase as the device temperature increases.

### 2.3 Gate charge losses

The gate charge losses are determined with the aid of the gate charge curve in the data sheets of the devices. The total gate charge losses will again be the sum of the gate charge losses for each device. The gate charge losses can be determined as follows:

$$P_{gate(SW1)} = Q_{gate} V_{gate} f_s \tag{E.10}$$

and

$$P_{gate(SW2)} = Q_{gate} V_{gate} f_s \tag{E.11}$$

where $V_{gate}$ is the voltage applied to the gate of the device [V].

### 2.4 Diode losses

The diode only conducts during the transition of the two switches. Thus, the diode losses will consist of both conduction losses and reverse recovery losses. Reverse recovery will occur only when $SW_1$ is turned on. Reverse recovery does not occur when $SW_2$ is turned on because the voltage over the diode does not force the diode off, but rather the current is simply redirected into the device channel due to the lower on voltage.

The reverse recovery losses for the diode can be determined as [E-3]:

$$P_{rr} = \frac{1}{2} Q_{rr} V_s f_s \tag{E.12}$$

where $Q_{rr}$ is the reverse recovery charge [C].

The reverse recovery charge can be taken from the data sheet but this is a poor approximation since the test conditions under which the reverse recovery charge is determined is not true to the operation of the device in a switch mode converter. Thus a more realistic value of the reverse recovery should be determined.

During the turn on interval of $SW_1$, the peak reverse recovery current was required and was determined experimentally. Either the reverse recovery charge can be determined experimentally too or it can be calculated.

The first time interval of the reverse recovery current has been determined as $t_{rr1}$. The second

time interval of the reverse recovery current can be calculated from the snappy factor of the body diode [E-2]. The snappy factor is defined as:

$$S = \frac{t_{rr2}}{t_{rr1}} \tag{E.13}$$

where $t_{rr1} + t_{rr2} = t_{rr}$,
$t_{rr}$ is the diode reverse recovery current [s]
and $S$ is the snappy factor.

The reverse recovery charge can then be approximated as:

$$Q_{rr} = \frac{1}{2} I_{rr} t_{rr} \tag{E.14}$$

The conduction losses of the diode will be a function of the time the diode conducts. The conduction time of the diode will be affected by the dead time between the two MOSFETs. The conduction losses can be determined as:

$$P_{cond} = I_{diode} V_{fw} t_{con} f_s \tag{E.15}$$

where $V_{fw}$ is the forward voltage of the diode [V],
$I_{diode}$ is the average diode current [A],
and $t_{con}$ is the total conduction time of the diode consisting of two conducting periods [s].

**Table E.1. The data sheet characteristics for the SSP80N08S2-07 and the converter circuit parameters**

| Property | Typical value | Unit |
|---|---|---|
| Converter Power level | 2000 | W |
| $V_{42}$ | 42 | V |
| $V_{14}$ | 14 | V |
| Number of phases | 4 | |
| $SW_1$ duty cycle: D | $V_{14}/V_{42} = 1/3$ | |
| MOSFET drain current | $P/(N \cdot V_{14}) = 35.7$ | A |
| MOSFET drain current at turn on | 27.4 | A |
| MOSFET drain current at turn off | 44.1 | A |
| $V_{gate}$ | 12 | V |
| Dead time | 100 | ns |
| $f_s$ | 140 | kHz |
| L | 3.8 | µH |
| | | |
| Turn on delay | 200 | ns |
| Turn off delay | 60 | ns |
| On resistance | 7.1 | mΩ |
| Gate charge | 95 | nC |
| Diode on voltage | 1.1 | V |

## 3. Theoretical device losses

The MOSFETs used for the converter are the SSP80N08S2-07 MOSFETs from Infineon. The MOSFETs are implemented on a DCB substrate without any packaging. The data sheet characteristics as well as the circuit parameters needed to estimate the device losses are tabulated in Table E.1.

It must be remembered that the losses using the data sheets information is at best an approximation.

Using equations E.1 to E.15, the semi-conductor losses are approximated and tabulated in Table E.2. The results in the table are for one of the four phases. The total semiconductor switching losses are tabulated in Table E.3.

The results in the two tables show that the losses in $SW_1$ of each phase are smaller than the losses in $SW_2$ for the same phases. The primary contributors to the losses in $SW_1$ are the turning on and turning off losses. The lower device, $SW_2$ is turned on and off under zero voltage conditions but the reverse recovery losses are significant resulting in the large losses in

**Table E.2. The semi-conductor switching times and losses**

| | |
|---|---|
| **$SW_1$ Turn on time ($t_{vf}$, $t_{rr1}$, $t_{ir}$)** | 2ns, 75ns, 30ns<br>total = 107ns |
| **$SW_1$ Turn off time ($t_{vr}$, $t_{if}$)** | 34ns, 30ns<br>total = 64ns |
| **Parasitic inductance in series with MOSFETs** | ≈20nH |
| **$Q_{rr}$** | 5.8μC |
| **S** | 1.3 |

| **Calculated losses** | |
|---|---|
| **Switching losses** | |
| $SW_1$ turn on losses | 6.6 W |
| $SW_1$ turn off losses | 8.2 W |

| **Conduction losses** | |
|---|---|
| $SW_1$ | 3.1 W |
| $SW_2$ | 6.4 W |

| **Gate Charge losses** | |
|---|---|
| $SW_1$ | 0.2 W |
| $SW_2$ | 0.2 W |

| **Diode losses** | |
|---|---|
| Conduction losses | 1.7 W |
| Reverse recovery losses | 18.1 W |

| **Total device losses for a single phase** | |
|---|---|
| $SW_1$ | 18.1 W |
| $SW_2$ | 26.4 W |

**Table E.3. The total semiconductor losses**

| | |
|---|---|
| **Total $SW_1$ losses for all 4 phases** | 72.7 W |
| **Total $SW_2$ losses for all 4 phases** | 107.2 W |

| | |
|---|---|
| **Total semiconductor losses** | 177.8W |

the lower device. The switching losses in $SW_1$ can only be reduced by improving the turn on and off speed of the device and in $SW_2$, by reducing the reverse recovery current and time.

The total losses in Table E.2 and Table E.3 are for operation with the nominal voltages of $V_{42}$ = 42V and $V_{14}$ = 14V and an output power of 2kW. As these voltages vary, the losses in the devices will also vary because the drain current in and the voltage across the MOSFETs will change. The total MOSFET losses for a single phase is tabulated in Table E.4 showing the total losses vary between 34.4W and 62.5W as a function of the excitation voltage. The variation in the losses in $SW_1$ and $SW_2$ over the operating voltage range is tabulated in Table E.5 and Table E.6 respectively.

The maximum switching losses in both devices corresponds with the terminal voltages where the largest drain currents flow through the device. Under these operating conditions the losses in $SW_1$ can reach approximately 23.4W while the losses in $SW_2$ can reach values as high as 40.2W

## 4. Experimental evaluation of the MOSFET losses

The losses in the MOSFETs can be estimated with the aid of the thermal measurements performed in Chapter 8. If the total losses in the MOSFETs can be determined, then using the measured temperature of the individual devices and assuming the thermal resistance of all the devices is the same, the losses in the individual MOSFETs can be determined.

**Table E.4. The calculated losses in the MOSFETs in a single phase**

| Total MOSFET losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 51.8 | 54.4 | 57.1 | 58.2 | 59.8 | 62.5 |
| $V_{14}$=14V | 39.5 | 41.5 | 43.6 | 44.5 | 45.8 | 47.9 |
| $V_{14}$=16V | 34.4 | 36.1 | 38.0 | 38.8 | 39.9 | 41.9 |

**Table E.5. The calculated losses in SW1 in a single phase**

| SW1 losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 23.4 | 22.8 | 22.5 | 22.5 | 22.4 | 22.3 |
| $V_{14}$=14V | 18.8 | 18.4 | 18.2 | 18.1 | 18.2 | 18.2 |
| $V_{14}$=16V | 16.8 | 16.4 | 16.3 | 16.3 | 16.3 | 16.4 |

**Table E.6. The calculated losses in SW2 in a single phase**

| SW2 losses (W) | $V_{42}$=30V | $V_{42}$=35V | $V_{42}$=40V | $V_{42}$=42V | $V_{42}$=45V | $V_{42}$=50V |
|---|---|---|---|---|---|---|
| $V_{14}$=11V | 28.5 | 31.6 | 34.6 | 35.7 | 37.4 | 40.2 |
| $V_{14}$=14V | 20.6 | 23.1 | 25.4 | 26.4 | 27.6 | 29.7 |
| $V_{14}$=16V | 17.6 | 19.7 | 21.7 | 22.5 | 23.6 | 25.5 |

The MOSFETs losses are determined by measuring the converters losses and then subtracting the sum of the losses in the bus capacitors, the inductors, the shunts and the copper conductors.

Consider the following for a single phase:

It is known that the temperature rise in a medium is the product of the dissipated power and the thermal resistance:

$$\Delta T = R_t \cdot P_{lost} \tag{E.16}$$

where $\Delta T$ is the temperature rise in the medium [˚C],
$R_t$ is the thermal resistance [˚C/W],
and $P_{lost}$ is the dissipated power [W].

Thus, for each device:

$$\begin{aligned} \Delta T_{SW1} &= R_t \cdot P_{SW1} \\ \Delta T_{SW2} &= R_t \cdot P_{SW2} \end{aligned} \tag{E.17}$$

and

$$P_{lost\_total} = P_{SW1} + P_{SW2} \tag{E.18}$$

with $P_{SW1}$ is the power dissipated in SW1 [W],
$P_{SW2}$ is the power dissipated in SW2 [W],
and $P_{lost\_total}$ is the total power dissipated in the phase arm MOSFETs [W].

The total power lost in terms of the power lost in each device can be obtained by making $P_{SW1}$ and $P_{SW2}$ the subject of equation E.16 and substituting it into equation E.18. The result is:

$$P_{lost\_total} = \frac{\Delta T_{SW1} + \Delta T_{SW2}}{R_t} \tag{E.19}$$

The thermal resistance is still unknown but can be removed from the equation by rewriting equation E.17 in terms of the thermal resistance and equating the thermal resistance of the two devices. Thus

$$\frac{\Delta T_{SW1}}{P_{SW1}} = \frac{\Delta T_{SW2}}{P_{SW2}} \tag{E.20}$$

Equation E.20 can then be substituted into equation E.19 to obtain the power loss in each device from the device temperature:

$$P_{SW1} = \frac{P_{lost\_total} \cdot \Delta T_{SW1}}{\Delta T_{SW1} + \Delta T_{SW2}} \tag{E.21}$$

$$P_{SW2} = \frac{P_{lost\_total} \cdot \Delta T_{SW2}}{\Delta T_{SW1} + \Delta T_{SW2}} \tag{E.22}$$

Equations E.21 and E.22 determine the power loss in the two devices considering the total loss between the two devices and the maximum temperature of the devices assuming the two devices have the same thermal resistance. To determine the losses in all 8 of the MOSFETs equations E.21 and E.22 can be expanded to include any number of MOSFETs:

$$P_{SWN} = \frac{P_{lost\_total} \cdot \Delta T_{SWN}}{\Delta T_{SW1} + \Delta T_{SW2} + \ldots + \Delta T_{SWN}} \tag{E.23}$$

where $P_{SWN}$ is the power dissipated in MOSFETs $N$ [W],
$\Delta T_{SWN}$ is the temperature rise of MOSFETs $N$ [˚C]
and $P_{lost\_total}$ is the total losses in all $N$ MOSFETs [W].

Table E.8 tabulates the results of the calculation to determine the losses in the MOSFETs based on the temperature and losses measured and recorded in Table E.7 and Table E.8. The total ISM losses without the EMI filters are measured as a function of the load current. The models developed in the previous sections are used to determine the losses in the inductor structures, in the capacitor structures, in the shunts and in the copper conductors. These losses are summed together and subtracted from the total measured losses leaving the losses dissipated in the 8 MOSFETs. Using equation E.23 the loss distribution between the MOSFETs can be determined as listed.

The table shows that the under full electrical excitation and with a thermal interface temperature of 30°C, the maximum heat dissipated in the MOSFETs is just under 31.7W for $SW_2$ and 24W for $SW_1$. The difference in the switching loss distribution between the devices is a consequence of the non-ideal current sharing in the phases.

**Table E.7. The measured temperature rise on the MOSFETs as a function of the load current (V14 = 14V, V42 = 42V, buck mode)**

| $I_{14}$ | ΔTa2 A2 $SW_1$ | ΔTa2 A2 $SW_2$ | ΔTa1 A1 $SW_1$ | ΔTa1 A1 $SW_2$ | ΔTb2 B2 $SW_1$ | ΔTb2 B2 $SW_2$ | ΔTb1 B1 $SW_1$ | ΔTb1 B1 $SW_2$ |
|---|---|---|---|---|---|---|---|---|
| 20.3 | 1.6 | 0.9 | 1.4 | 0.8 | 1.3 | 0.9 | 1.3 | 0.8 |
| 30.3 | 2 | 1.1 | 2.1 | 1 | 2 | 1.6 | 1.9 | 1.9 |
| 39.7 | 4.9 | 8 | 4.7 | 7.3 | 3.5 | 6.4 | 4.5 | 7.5 |
| 50.1 | 6.2 | 11.2 | 6.7 | 10.1 | 5 | 8.8 | 5.8 | 9.5 |
| 60.1 | 6.9 | 12.5 | 7.6 | 10.6 | 6 | 10.1 | 6.8 | 11 |
| 70.2 | 7.8 | 13.9 | 8.6 | 13.2 | 7 | 11.5 | 8.1 | 12.7 |
| 80.1 | 8.5 | 15 | 9.6 | 14.4 | 7.7 | 12.3 | 8.8 | 13.5 |
| 90.2 | 9.5 | 16.3 | 10.9 | 16 | 8.8 | 13.9 | 10.3 | 15 |
| 102.1 | 11 | 17.9 | 13.1 | 18.4 | 9.7 | 15.8 | 11.4 | 17.1 |
| 110.8 | 10.7 | 17.8 | 13.7 | 19 | 10.4 | 16.4 | 12.2 | 17.7 |
| 121.1 | 11.8 | 19.2 | 15.2 | 20.8 | 11.4 | 17.9 | 13.5 | 19.5 |
| 132.8 | 12.3 | 19.9 | 17 | 22.5 | 12.4 | 18.8 | 14.9 | 20.8 |
| 143.0 | 13.3 | 20.5 | 18.8 | 24.8 | 13.3 | 20.7 | 15.9 | 22.4 |

**Table E.8. A summary of the measured losses in the Integrated System Module without the EMI filters**

| 4-Phase ISM Measured Terminal Parameters with Thermal Interface Temperature of 30°C | | | | Total ISM Losses [W] | Total Inductor Losses [W] | Total Shunt Losses [W] | Conduction Losses [W] | Total Capacitor Losses [W] | Total MOSFET Losses [W] | MOSFET Losses[W] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{42}$ [V] | $V_{14}$ [V] | $P_{14}$ [W] | Effi [%] | | | | | | | A2 Sw1 | A2 Sw2 | A1 Sw1 | A1 Sw2 | B2 Sw1 | B2 Sw2 | B1 Sw1 | B1 Sw2 |
| 42.7 | 14.6 | 298.5 | 93.0 | 25.4 | 0.4 | 0.1 | 0.1 | 0.2 | 24.6 | 4.4 | 2.5 | 3.8 | 2.2 | 3.6 | 2.5 | 3.6 | 2.2 |
| 42.8 | 14.3 | 439.2 | 93.5 | 31.9 | 0.9 | 0.2 | 0.2 | 0.2 | 30.3 | 4.5 | 2.5 | 4.7 | 2.2 | 4.5 | 3.6 | 4.2 | 4.2 |
| 42.8 | 14.1 | 567.7 | 92.3 | 70.5 | 1.7 | 0.4 | 0.3 | 0.3 | 67.8 | 7.1 | 11.6 | 6.8 | 10.6 | 5.1 | 9.3 | 6.5 | 10.9 |
| 42.7 | 14.1 | 706.7 | 89.9 | 86.8 | 2.6 | 0.6 | 0.4 | 0.5 | 82.7 | 8.1 | 14.6 | 8.8 | 13.2 | 6.5 | 11.5 | 7.6 | 12.4 |
| 42.7 | 14.3 | 856.4 | 90.1 | 104.7 | 3.8 | 0.9 | 0.6 | 0.6 | 98.8 | 9.5 | 17.3 | 10.5 | 14.6 | 8.3 | 14.0 | 9.4 | 15.2 |
| 42.7 | 14.2 | 991.5 | 90.3 | 122.0 | 5.2 | 1.2 | 0.9 | 0.7 | 114.0 | 10.7 | 19.1 | 11.8 | 18.2 | 9.6 | 15.8 | 11.2 | 17.5 |
| 42.7 | 14.1 | 1131.1 | 90.2 | 138.7 | 6.9 | 1.6 | 1.1 | 0.8 | 128.2 | 12.1 | 21.4 | 13.7 | 20.6 | 11.0 | 17.6 | 12.6 | 19.3 |
| 42.7 | 14.3 | 1310.2 | 90.2 | 147.1 | 8.8 | 2.1 | 1.5 | 1.0 | 133.8 | 12.6 | 21.7 | 14.5 | 21.3 | 11.7 | 18.5 | 13.7 | 19.9 |
| 42.7 | 14.3 | 1431.3 | 90.2 | 162.5 | 11.3 | 2.6 | 1.9 | 1.3 | 145.5 | 14.0 | 22.8 | 16.7 | 23.4 | 12.3 | 20.1 | 14.5 | 21.7 |
| 42.7 | 14.4 | 1603.6 | 90.1 | 185.9 | 13.2 | 3.1 | 2.2 | 1.5 | 165.9 | 15.1 | 25.0 | 19.3 | 26.7 | 14.6 | 23.1 | 17.2 | 24.9 |
| 42.6 | 14.1 | 1707.5 | 90.1 | 197.8 | 16.0 | 3.7 | 2.6 | 1.7 | 173.8 | 15.9 | 25.8 | 20.4 | 28.0 | 15.3 | 24.1 | 18.1 | 26.2 |
| 42.7 | 14.5 | 1895.3 | 90.1 | 217.2 | 19.1 | 4.5 | 3.1 | 2.0 | 188.5 | 16.7 | 27.1 | 23.1 | 30.6 | 16.9 | 25.6 | 20.3 | 28.3 |
| 42.6 | 14.6 | 2060.5 | 90.0 | 224.4 | 22.2 | 5.2 | 3.7 | 2.3 | 191.1 | 17.0 | 26.2 | 24.0 | 31.7 | 17.0 | 26.4 | 20.3 | 28.6 |

The losses predicted for the two devices is 18.1W for $SW_1$ and 26.4W for $SW_2$ assuming ideal current sharing. For the two phases where the average current is the same as in the model, the losses in $SW_1$ are17W and 26.2W in $SW_2$ showing very good correlation with the model.

## 5. Estimating the device thermal resistance

In the previous section, the losses in the MOSFETs have been determined from the thermal measurement and the module efficiency measurement. The MOSFETs temperature rise can be plotted against the losses in the device to determine the device thermal resistance. This is plotted in Figure E.4 for the top MOSFETs ($SW_1$) in each of the 4 phase and in Figure E.5 for the bottom MOSFETs ($SW_2$) in each of the 4 phases. Both graphs plot a linear relationship between the device temperature increase and the losses dissipated in the device. Since the temperature rise is taken as the device temperature less the thermal interface temperature, the gradient of the relationship between the temperature rise and the dissipated heat represent the thermal resistance between the device and the thermal interface.

The thermal resistance is determined by plotting a trend line through the measured data in Figure E.4 and Figure E.5. The equation representing the trend lines are plotted in the figures.

The measured MOSFETs thermal resistance is 0.74 C°/W.

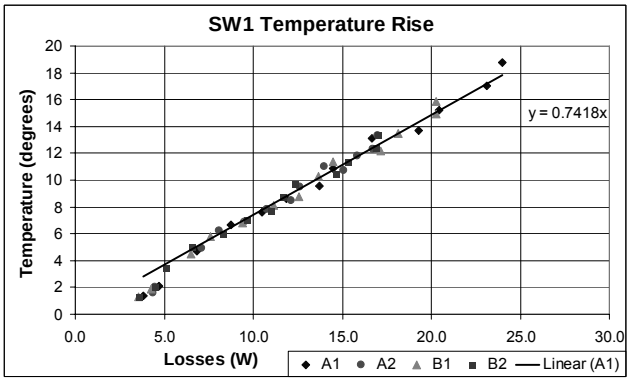


**Figure E.4. The temperature rise of the $SW_1$ MOSFETs of the 4 phases as a function of the switching losses**

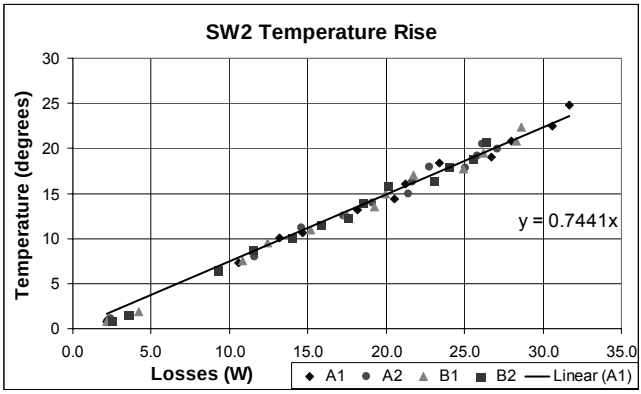


**Figure E.5. The temperature rise of the $SW_2$ MOSFETs of the 4 phases as a function of the switching losses**

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# SUMMARY

## The Electrical, Thermal and Spatial Integration of a Converter in a Power Electronic Module

Ph.D. Thesis
by Mark Benjamin Gerber

**Power electronics in the automotive environment**

Electronic systems have been implemented in passenger vehicles almost since the passenger vehicles inception. Over time, the functionality and sheer quantity of these systems in the passenger vehicle have increased and this has meant that more electrical power has been required. In response to this, the voltage level of the automotive power distribution network was increased from 6V to 12V in the 1950s. History is about to repeat itself again with the voltage level being increased to 42V in response to the explosion of electrical systems being implemented in modern passenger vehicles.

The conversion from the current 14V[a] system to the new "42V PowerNet Bus" is not as simple as the conversion in the 1950s was. Almost every component in an automobile is highly optimised and changing a parameter that is as fundamental to the complete system as the supply voltage will be a lengthy and complicated process. As a compromise, both the 14V and 42V power distribution networks will be implemented in a transitional period of approximately 10 to 15 years to minimise the conversion cost.

The higher bus voltage opens the doors to many new and exciting possibilities most of which have power electronics at their core. However, for these systems to be implemented they must first function in the automotive environment. The automotive environment is electrically and thermally harsh, with temperatures ranging between -40˚C to 150˚C, and severe volumetric restrictions being placed on any system implemented within the vehicle.

This thesis is concerned with the design and implementation of a power electronic system (14/42V DC/DC converter) that is implemented in the automotive environment, specifically the engine compartment. The power electronic system must have a high power density while operating in a high temperature environment.

**Power electronic modules**

Power electronic modules are considered the technology base in which to implement the automotive converter. The evolution of power electronic modules is considered and the power electronic modules are classified according to their level of functionality.

[a] 14V is the engine on voltage of the automotive power distribution network with a 12V battery.

Of the power electronic modules considered, the Integrated System Module (ISM) is proposed for the automotive application. The ISM is a power electronic module that not only includes the power semi-conductor devices, but also contains all the additional passive components required for energy storage and if required, EMI filters. The module also contains the circuitry required for control and diagnostics. Thus the ISM is a completely self-contained, self-driven, self-protecting power conversion system implemented in a high power density power electronic module.

**Interdependent design of a power converter in a power module**

To design the automotive power converter with a high power density and the capacity to operate in a high temperature environment, the electrical design of the topology, the thermal design of the module and the spatial and volumetric design of the physical module and components must all be optimised simultaneously. This can only be achieved by considering the interdependencies and trade-offs between the various designs and manipulating the interdependencies to simultaneously optimise all of the relevant parameters such as the power density and operating temperature. The interdependencies and the manipulation of these interdependences form the core of this thesis.

**Manipulating design interdependencies**

Several techniques for manipulating the design interdependencies and trade-offs between the various designs are considered in the thesis. For the synchronous rectifier topology considered for the automotive converter, the most important manipulation techniques include interleaving and the integrated heat sink structure.

*Interleaving* is a technique used to optimise the electrical topology design. Through interleaving multiple phases, the energy that must be stored in the various passive components and the RMS currents in the same components can be significantly reduced. By choosing the appropriate number of phases for a given set of operating parameters, the energy and RMS currents in the various passive components can be minimised on the basis of only the topology waveforms. This can help minimise both the losses in the components and the volume required for energy storage.

The *integrated heat sink* structure is a thermal management technique used to extract and transport the heat dissipated in the various components in the ISM to the environment with a very small $\Delta T$ between the heat source and the environment. This is critical for high temperature operation because the maximum allowed $\Delta T$ can be relatively small. The integrated heat sink allows the volume of a passive component located anywhere within the ISM to be significantly decreased for a given excitation while limiting the maximum temperature rise in the component. This makes it possible to implement the various passive components in the power electronic module without increasing the power electronic module's volume.

**The experimental Integrated System Module**

The interdependent electrical, thermal and spatial design presented in the thesis is used to design and implement the experimental automotive ISM. The specifications for the ISM are 2kW, bi-directional energy transfer between the 14V and 42V power nets and the module is cooled with the passenger vehicle's engine coolant that has a nominal temperature of 85˚C and a maximum temperature of 125˚C.

The experimental ISM implements a bi-directional 4-phase synchronous rectifier topology including all the passive components required by the topology (bus capacitors, decoupling capacitors and EMI filters). The ISM has a measured power density of 6.11kW/dm$^3$ (110.5W/in$^3$) and an efficiency of 89% with a coolant temperature of 110˚C. At 125˚C, the efficiency drops to 88.5%. The maximum temperature-rise in the IMS at full electrical power is only 30˚C. This is the maximum temperature-rise on the switching semi-conductors.

**Conclusions**

The most important conclusions drawn in the thesis can be summarised by the thesis objectives:

i. *To investigate the possibility of implementing a complete automotive converter in a state of the art power electronic module.*
The automotive converter is implemented in a state of the art Integrated System Module (ISM), which is a power electronic module containing the complete power conversion system including all the necessary passive components. Current ISM implementations do not meet the power or the thermal requirements imposed on the module by the automotive environment and specifications.

ii. *To analyse the interdependencies that exist between the electrical, the thermal and the spatial design of the power electronic module.*
The interdependencies and trade-offs between the electrical, thermal and spatial aspects of the ISM design are identified in the thesis. These interdependencies and trade-offs are manipulated so that all of the given specifications can be satisfied simultaneously and in the same volume.

iii. *To develop techniques for a multi-objective design so that the power electronic module can meet all the given specifications.*
Techniques for manipulating the design interdependencies and trade-offs are considered for each of the three designs. For the topology considered, the most important of these techniques include interleaving and the integrated heat sink. Various other techniques are also considered.

iv. *To design and construct a high power density, 3D integrated power electronic module prototype for the automotive environment.*
The experimental automotive ISM design documented in the thesis is based on the integral electrical, thermal and spatial design and meets the given electrical, thermal and spatial specifications simultaneously and in the same volume. The module achieves a high power density while operating with a high temperature coolant. The maximum temperature-rise in the ISM is only 30˚C and the module contains the complete power conversion system.

# SAMENVATTING

## De Elektrische, Thermische en Ruimtelijke Integratie van een Omvormer in een Vermogenselektronische Module

Proefschrift
van Mark Benjamin Gerber

**Vermogenselektronica in de automobiel omgeving**

Sinds het onstaan van passagiersvoertuigen zijn er elektronische systemen in toegepast. In de loop der jaren is de functionaliteit van deze systemen toegenomen. Dit betekende dat er steeds meer elektrische energie nodig was. In reactie hierop is het spanningsniveau van het vermogensdistributienetwerk in auto's in de jaren '50 gestegen van 6V naar 12V. De geschiedenis staat op het punt zichzelf te herhalen nu het spanningsniveau verhoogd wordt naar 42V, in reactie op de enorme toename van het aantal elektrische systemen dat in moderne passagiersvoertuigen wordt toegepast.

De omschakeling van het huidige 14V system naar de nieuwe "42V PowerNet Bus" is niet zo eenvoudig als de omschakelijk in de jaren '50 was. Bijna alle componenten in een auto zijn sterk geoptimaliseerd en het veranderen van een fundamentele parameter zoals de spanning zal een langdurig en ingewikkeld proces worden. Als compromis zullen gedurende een overgangstijd van 10 tot 15 jaar zowel 14V als 42V distributienetwerken geïmplementeerd worden om de de kosten van de omschakeling zo klein mogelijk te houden.

De hogere busspanning biedt de mogelijkheid tot vele nieuwe en interessante mogelijkheden, welke veelal gebaseerd zijn op vermogenselektronica. Voordat deze systemen echter geïmplementeerd kunnen worden moeten ze eerst kunnen functioneren in een auto. De elektrische en thermische eisen zijn hier zwaar. De omgevingstemperatuur kan varieren tussen -40˚C en 150˚C. Verder worden er strenge eisen gesteld aan het volume van elk systeem dat geïmplementeerd wordt in het voertuig.

Dit proefschrift gaat over het ontwerp en de implementatie van een vermogenselektronisch systeem (14/42V DC/DC omvormer) dat geïmplementeerd is in het motorcompartiment van een auto. Het vermogenselektronisch systeem moet een hoge vermogensdichtheid hebben, terwijl het moet werken bij een hoge omgevingstemperatuur.

**Vermogenselektronische modules**

Vermogenselektronische modules worden beschouwd als de basistechniek voor omvormers voor automobieltoepassingen. De evolutie van deze modules is nagegaan en de modules zijn geclassificeerd op basis van het aantal functionaliteiten.

Van de beschouwde modules wordt de *Integrated System Module* (ISM) voorgesteld voor toepassing in auto's. De ISM bevat niet alleen de vermogenshalfgeleiders, maar ook de aanvullende componenten die nodig zijn voor energieopslag en, indien nodig, de EMI filters. Verder bevat de module de elektronica die nodig is voor regeling en diagnostiek. De ISM is dus een compleet zelfstandig, (zelfsturend en zelfbeveiligend) systeem voor vermogensomzetting, dat geïmplementeerd is in een module met een hoge vermogensdichtheid.

**Onderling afhankelijk ontwerp van een vermogensomvormer in een vermogensmodule**

Het doel is om een omvormer met hoge vermogensdichtheid te ontwerpen die toegepast wordt in auto's en die kan werken bij een hoge omgevingstemperatuur. Daarvoor is het nodig het elektrisch ontwerp van de topologie, het thermische ontwerp van de module en het ruimtelijke ontwerp en de afmetingen van de fysieke module en alle componenten gelijktijdig te optimaliseren. Dit kan alleen bereikt worden door de onderlinge afhankelijkheden en *trade-offs* tussen de diverse ontwerpen na te gaan en de onderlinge afhankelijkheden te manipuleren om gelijktijdig alle relevante parameters, zoals de vermogensdichtheid en bedrijfstemperatuur, te optimaliseren. De onderlinge afhankelijkheden en het manipuleren daarvan vormen de kern van dit proefschrift.

**Het manipuleren van de onderlinge afhankelijkheden van het ontwerp**

In dit proefschrift zijn de verschillende technieken voor het manipuleren van de onderlinge afhankelijkheden en de *trade-offs* tussen de verschillende ontwerpen beschouwd. Voor de synchrone gelijkrichter topologie, die in aanmerking komt voor de omvormer voor automobieltoepassingen, zijn *interleaving* en de *integrated heat sink structure* de belangrijkste manipulatietechnieken.

*Interleaving* is een techniek die gebruikt wordt om het ontwerp van de elektrische topologie te optimaliseren. De energie die opgeslagen moet worden in de verschillende passieve componenten en de RMS stromen door diezelfde componenten kunnen door *interleaving* van meerder fasen behoorlijk gereduceerd worden. Door het juiste aantal fasen te kiezen voor een gegeven set operationele parameters, zijn alleen maar de golfvormen van de topologie nodig om de energie en de RMS stromen in de verschillende passieve componenten te kunnen minimaliseren. Dit kan helpen om zowel de verliezen in de componenten als het volume dat nodig is voor energieopslag te minimaliseren.

De *integrated heat sink structure* is een methode voor warmtehuishouding die gebruikt wordt om, bij een hele kleine $\Delta T$ tussen de warmtebron en de omgeving, de warmte die gedissipeerd wordt in de verschillende componenten van de ISM te onttrekken en naar de omgeving te transporteren. Dit is erg belangrijk voor de werking bij een hoge temperatuur omdat de maximaal toegestane $\Delta T$ relatief klein kan zijn. De *integrated heat sink* maakt het mogelijk om, voor een gegeven excitatie, het volume van passieve componenten behoorlijk te laten afnemen, onafhankelijk van waar die componenten zich in de ISM bevinden. De maximale temperatuurtoename in de component blijft hierbij beperkt. Dit maakt het mogelijk om de verschillende passieve componenten te implementeren in de vermogenselektronische module zonder dat het volume van de module toeneemt.

**De experimentele *Integrated System Module***

Het onderling afhankelijke elektrische, thermische en ruimtelijke ontwerp dat in dit proefschrift

gepresenteerd is, is gebruikt om een experimentele ISM voor automobieltoepassingen te ontwerpen en implementeren. De belangrijkste specificaties voor de ISM zijn een vermogen van 2kW en een bi-directioneel energietransport tussen de vermogensnetten van 14V en 42V. De module wordt gekoeld met het koelwater van de motor. Dit heeft een nominale temperatuur van 85˚C en een maximale temperatuur van 125˚C.

De experimentele ISM bevat een bi-directionele 4-fasige synchrone gelijkrichter inclusief alle passieve componenten die gebruikt worden door de topologie (tussenkringcondensatoren, ontkoppelingscondensatoren en EMI filters). De ISM heeft een gemeten vermogensdichtheid van 6.11kW/dm$^3$ (110.5W/in$^3$) en een rendement van 89% bij een koelwatertemperatuur van 110˚C. Bij 125˚C zakt het rendement naar 88.5%. De maximale temperatuurtoename van de schakelende halfgeleiders in de ISM is slechts 30˚C.

**Conclusies**

De belangrijkste conclusies die in dit proefschrift getrokken zijn kunnen samengevat worden aan de hand van de doelstellingen van het proefschrift:

i. *Onderzoek of het mogelijk is om een complete omvormer voor automobieltoepassingen te implementeren in een state of the art vermogenselektronische module.*
De omvormer voor automobieltoepassingen is geïmplementeerd in een *state of the art Integrated System Module* (ISM). Dit is een vermogenselektronische module die het complete vermogensconversie systeem bevat, inclusief al de noodzakelijke passieve componenten. De huidige ISM implementaties voldoen niet aan de eisen met betrekking tot vermogen en temperatuur, die de automobielomgeving en de specificaties stellen.

ii. *Analyseer de onderlinge afhankelijkheden die bestaan tussen het elektrische, het thermische en het ruimtelijke ontwerp van een vermogenselektronische module.*
De onderlinge afhankelijkheden en de *trade-offs* tussen de elektrische, thermische en ruimtelijke aspecten van het ISM ontwerp zijn in dit proefschrift geïdentificeerd. Deze onderlinge afhankelijkheden en *trade-offs* zijn gemanipuleerd om, binnen hetzelfde volume, gelijktijdig aan al de gegeven specificaties te kunnen voldoen.

iii. *Ontwikkel technieken voor een multi-objective ontwerp zodat de vermogenselektronische module kan voldoen aan al de gegeven specificaties.*
Voor elk van de drie ontwerpen zijn technieken beschouwd die kunnen worden gebruikt om de onderlinge afhankelijkheden en trade-offs te manipuleren. De meest belangrijke technieken voor de beschouwde omvormer zijn *interleaving* en de *integrated heat sink*. Daarnaast zijn er nog verschillende andere technieken beschouwd.

iv. *Ontwerp en bouw een 3D geïntegreerde vermogenselektronische module met hoge vermogensdichtheid, voor toepassing in een automobielomgeving.*
Het experimentele ISM ontwerp voor automobieltoepassingen dat in dit proefschrift beschreven is, is gebaseerd op een integraal elektrisch, thermisch en ruimtelijk ontwerp. Het voldoet aan de gegeven elektrische, thermische en ruimtelijke specificaties. De module heeft een hoge vermogensdichtheid, terwijl hij werkt met

koelwater van hoge temperatuur. De maximale temperatuurtoename in de ISM is slechts 30˚C. De module bevat het complete vermogensconversie systeem.

# ZUSAMMENFASSNG

## Elektrische, thermische und räumliche Integration eines Spannungswandlers in ein Leistungselektronik-Modul

Dissertation
von Mark Benjamin Gerber

### Leistungselektronik für die Automobileechnik

Von Beginn an haben elektrische/elektronische Systeme im Personenkraftfahrzeug Einzug gehalten. Mit der Zeit stieg die Funktionalität und der Gesamtanteil dieser Systeme und damit verbunden der elektrische Leistungsbedarf. Durch die Umstellung der Bordnetzspannung von 6V auf 12V hat man dieser Entwicklung Rechnung getragen. Eine ähnliche Tendenz ist heute zu beobachten mit dem Ziel, den großen Leistungsbedarfs durch eine Bordnetzspannung von 42 V decken zu können.

Der Übergang von 14V[a] auf 42V ist aber nicht mehr so einfach wie die Konversion von 6V auf 12V in den fünfziger Jahren. Beinahe jede Komponente im Kraftfahrzeug ist optimiert und jede Änderung eines Parameters hat große Konsequenzen für das Gesamtsystem. Insbesondere die Erhöhung der Bordnetzspannung bedingt daher einen längeren und komplexeren Konversionsprozess. Es sind daher Systeme mit einer dualen Bordnetzspannung von 14V und 42V für diese Übergangsperiode von 10-15 Jahre vorgesehen, um die Kosten während der Umstellung möglichst gering zu halten.

Höhere Bordnetzspannungen erlauben eine Vielzahl neuer Möglichkeiten und Applikationen, wo besonders die Leistungselektronik herausgefordert wird. Zu beachten sind zudem die harten Einsatz- und Umgebungsbedingungen in elektrischer und thermischer Hinsicht, mit einem Temperaturbereich von -40°C…150°C. Hinzu kommen starke Forderungen bezüglich des Volumens der Elektronik, das durch die engen Vorgaben der Einbauplätze zu minimieren ist.

Im Rahmen dieser Dissertation wurde ein Leistungselektroniksystem (14V/42V DC/DC-Wandler) für den Einsatz im Motorraum eines Fahrzeuges entworfen und entwickelt, mit dem Ziel einer hohen Leistungsdichte bei gleichzeitigem Einsatz bei hohen Umgebungstemperaturen.

### Leistungselektronische Module

Als Technologiebasis für den DC/DC-Wandler dient die heutige Modultechnik. Die technologische Entwicklung der Modultechnik wird hinsichtlich der eingebauten Funktionalität betrachtet. Hierbei wird ein Integrated System Module (ISM) vorgeschlagen, das nicht nur die

[a] 14V ist die Bordnetzsspannung bei einer 12V Batterie-Versorgung

Leistungshalbleiter enthält, sondern darüber hinaus zusätzlich passive Bauelemente für Energiespeicherung und, falls benötigt, für EMV-Filterung. Das Modul enthält des weiteren die komplette Elektronik für Regelung und Diagnostik. Das ISM ist daher ein in sich geschlossener, selbsttätiger, abgesicherter Leistungswandler, der in einem Leistungsmodul mit hoher Leistungsdichte realisiert wurde.

**Abhängiger Entwurf eines Leistungswandlers in einem Leistungsmodul**

Der Entwurf eines solchen kompakten leistungselektronischen Systems für den Einsatz bei hohen Temperaturen erfordert gleichzeitig die Auslegung des elektrischen Systems, das thermische Design und die räumliche und volumetrische Anordnung der Komponenten. Dies gelingt nur bei Beachtung der Abhängigkeiten dieser Entwürfe voneinander und gegenseitiger Abstimmung dieser Abhängigkeiten, um letztendlich zu einem optimierten Entwurf bezüglich Leistungsdichte und Hochtemperaturtauglichkeit zu gelangen. Die Abhängigkeiten der Entwürfe und deren Beeinflussung bilden den Schwerpunkt der Dissertation.

**Beeinflussung der Abhängigkeiten im Entwurfsprozess**

Verschiedene Techniken zur Beeinflussung und Abstimmung der Freiheitsgrade beim Entwurfsprozess werden in vorliegender Arbeit untersucht. Für die vorgeschlagene Topologie eines Synchrongleichrichters sind dies vor allem die Mehrphasigkeit und die integrierte Kühlkörperstruktur.

Die Mehrphasigkeit dient der Optimierung des elektrischen Entwurfes. Durch einen mehrphasigen Aufbau sinken die in den passiven Bauelementen gespeicherten Energien und Strombelastungen. Die Wahl der Anzahl der Phasen erlaubt bei bestimmten Randbedingungen eine optimale Nutzung der Energiespeicherung in Form von minimaler Anzahl an passiven Komponenten. Dies unterstützt den Entwurf hinsichtlich der Verluste in den Komponenten und deren Volumen.

Eine integrierte Kühlkörperstruktur dient dem thermischen Management in Bezug auf Wärmetransport von den verschiedenen verlustbehafteten Bauelementen im ISM zur Umgebung mit einem kleinen DT zwischen Wärmequelle und –senke. Dieser Wärmepfad ist kritisch für Hochtemperaturanwendungen, da hier üblicherweise das DT relativ klein ist. Die integrierte Kühlkörperstruktur erlaubt kleinere Volumina von passiven Komponenten innerhalb des ISM bei gleicher Anregung und Limitierung des Temperaturanstieges. Dadurch können passive Bauelemente in das Modul integriert werden, ohne das Volumen desselben signifikant zu erhöhen.

**Experimentelles ISM**

Ein voneinander abhängiger elektrischer, thermischer und räumlicher Entwurf wird für ein experimentelles ISM vorgestellt. Die Spezifikationen für das ISM sind 2kW, bidirektionaler Energietransfer zwischen 14V und 42V-Bordnetzen und Nutzung des Motorkühlkreislaufs mit einer Kühlwassertemperatur von 85°C bis maximal 125°C.

Das experimentelle ISM besteht aus einer 4-phasigen bi-direktionalen Synchrongleichrichter-Topologie mit passiven Komponenten (Stützkondensatoren, Entkopplungskondensatoren und EMV-Filter). Das ISM zeigt eine Leistungsdichte von 6.11kW/dm$^3$ (110.5W/in$^3$) und einen Wirkungsgrad von 89% bei einer Kühlwassertemperatur von 85°C. Bei 125°C sinkt der

Wirkungsgrad auf 88.5%. Der maximale Temperaturanstieg im gesamten IMS beträgt nur 30K und tritt an den Leistungshalbleitern auf.

**Schlussfolgerungen**

Folgende Schlussfolgerungen können aus der Aufgabenstellung der Dissertation gezogen werden.

i. *Untersuchung einer Integration eines Wandlers für Automobilanwendungen in ein State-of-the-art Leistungsmodul.*
Der Wandler ist in ein ISM integriert, das neben den aktiven Komponenten auch alle passiven Komponenten beinhaltet. Gängige Leistungsmodule erfüllen nicht die Leistungs- bzw. Temperaturspezifikationen der Automobilindustrie.

*ii.* *Analyse der Abhängigkeiten bei einem elektrischen, thermischen und räumlichen Entwurf eines Leistungsmoduls.*
Diese Abhängigkeiten und Abstimmungen der Freiheitsgrade bei einem solchen Entwurf werden analysiert und deren Beeinflussung dargestellt.

iii. *Entwicklung eines komplexen Entwurfprozesses zur Erfüllung der Spezifikationen.*
Verschiedene Techniken für einen solch einen komplexen Entwurf werden analysiert. Für die gestellte Aufgabe sind dies insbesondere die Mehrphasigkeit und die integrierte Kühlkörperstrukutr.

iv. *Entwurf, Konstruktion eines hochintegrierten 3-D ISM Prototypen.*
Der Prototyp wurde gemäß des optimierten Entwurfsprozesses entwickelt und gestestet. Die geforderten Spezifikationen hinsichtlich Leistungsdichte und Hochtemperatureinsatz konnten experimentell bestätigt werden.

# CURRICULUM VITAE

Mark Benjamin Gerber was born in Johannesburg, South-Africa, in 1977. He received his Bachelors and Masters in Electronic and Electrical Engineering (B. Eng. and M. Eng.), both cum laude, from the Rand Afrikaans University, Johannesburg, South-Africa, in 1999 and 2001 respectively.

He started working towards the Ph.D. degree in April 2002 at the Delft University of Technology in the Netherlands in the field of high power density packaging of power electronic systems. His Ph.D. research was sponsored by Siemens CT. in München, Germany and the research was done in the research group Electrical Power Processing of the Faculty of Electrical Engineering, Mathematics and Informatics, at the Delft University of Technology in the Netherlands. This thesis is the result of this research.

His current research interests include packaging and high power density packaging of power electronic systems, thermal management in power electronic systems and topologies for DC/DC converters and inverters.