M.Sc. thesis in Electrical Power Engineering

Microinverter for Residential PV Systems

Rohan Shailesh Deshmukh

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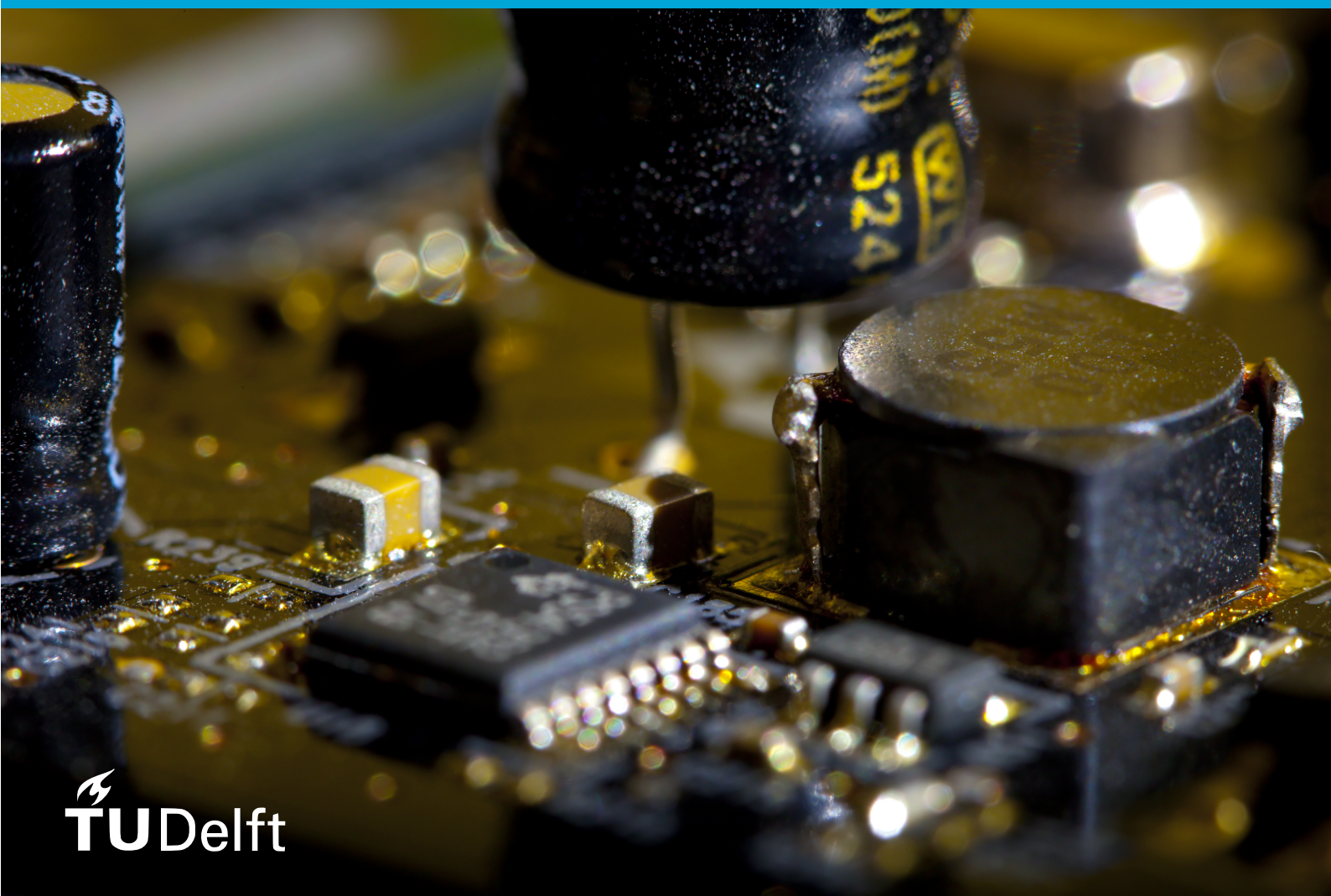

TU Delft

Microinverter for Residential PV Systems

by

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Abstract

Up to 5 kW PV installations microinverters are common alternatives for the typical string solar inverters. The main draw back of the technology is the slight higher initial cost, however, a more efficient energy generation can be achieved if one of the PV modules are operated optimally at the maximum power point. This work shows that converters employed using low voltage Si-MOSFETS can exhibit excellent loss performance. Power efficiency above 97 % is possible yielding to much lower total cost of ownership. This thesis emphasizes on the investigation of microinverter technology in residential PV systems. A small scale prototype is developed to evaluate the performance of the selected topology. The advantage of the designed circuit are flexibility in expanding the system, redundant switching states and, less number of semi-conductor switches per PV module.

Acknowledgement

This thesis would have not been possible without the support of the below mentioned important persons, I would first and foremost take this opportunity to sincerely thank my supervisor Dr. Thiago Batista Soeiro for his patience, motivation, knowledge sharing and guidance. I would like to thank Dr. Aditya Shekhar for his valuable feedback and advise in context of the research methodology.

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Rohan Shailesh Deshmukh
Delft, July, 2021

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Nomenclature

$\% \, i_{\text{ripple}}$	% Current Ripple
ω	Angular Frequency
ω_{g}	Angular Grid Frequency
i_{c}	Capacitor Current
ΔI	Change in Current
ΔP	Change in Power
ΔV	Change in Voltage
T_{d}	Controller Delay
i_{inv}	Current injected
C_{dc}	DC link capacitance per cell
V_{dc}	DC Link Voltage per cell
$V_{\text{dc(ref)}}$	DC Link Voltage Reference
R_{dc}	DC Resistance
d_{bare}	Diameter of the bare conductor
C_{DS}	Drain-Source Capacitance
V_{drv}	Driver Supply Voltage
$f_{\text{sw(eff)}}$	Effective Switching Frequency
L_{f}	Filter inductance
C_{GD}	Gate-Drain Capacitance
C_{GS}	Gate-Source Capacitance
V_{GS}	Gate-Source Voltage
θ_{g}	Grid Angle
$i_{\text{g(ref)}}$	Grid Current Reference
f_{g}	Grid Frequency
i_{dc}	Input DC Current
P_{dc}	Input DC Power
$X(s)$	Input Transfer Function
K_{Iv}	Integral Gain of the DC link voltage controller
$\Delta i_{\text{L(max)}}$	Maximum current ripple

$V_{\text{g(max)}}$ Maximum grid voltage for converter design

V_{MPP} Maximum Power Point Voltage

$V_{\text{dc(meas)}}$ Measured average DC link voltage per cell

$V_{\text{(miller)}}$ Miller Voltage

m_{a} Modulation Index

N_{carrier} Number of Carrier Signals

N_{cell} Number of cells

V_{op} Operating PV Voltage

$Y(s)$ Output Transfer Function

C_{PW} Parasitic capacitance between the windings

C_{P} Parasitic Capacitance of PV module

$\hat{i}_{\text{drv}}$ Peak Driving Current

$\hat{i}_{\text{g}}$ Peak Grid Current

$\hat{V}_{\text{t}}$ Peak Terminal Voltage of the converter

ϕ_{m} Phase margin

ω_{i} PI Current Controller Bandwidth

ω_{v} PI DC link voltage controller Bandwidth

P_{drv} Power Dissipation in Gate Driver

P_{c} Power injected into the Capacitor

P_{inv} Power injected into the grid

K_{Pv} Proportional Gain of the DC link voltage controller

S_{rated} Rated Apparent Power

R_{L} Resistance of the filter

$V_{\text{g(rms)}}$ RMS Grid Voltage

f_{s} Sampling Frequency

T_{s} Sampling Period

f_{sw} Switching Frequency

T_{sw} Switching Period

T_{PSPWM} Time Delay between 2 carrier signals

C_{DC} Total DC Link Capacitance

ΔV_{DC} Total DC Link Voltage Ripple

V_{DC} Total DC Link Voltage

Acronyms

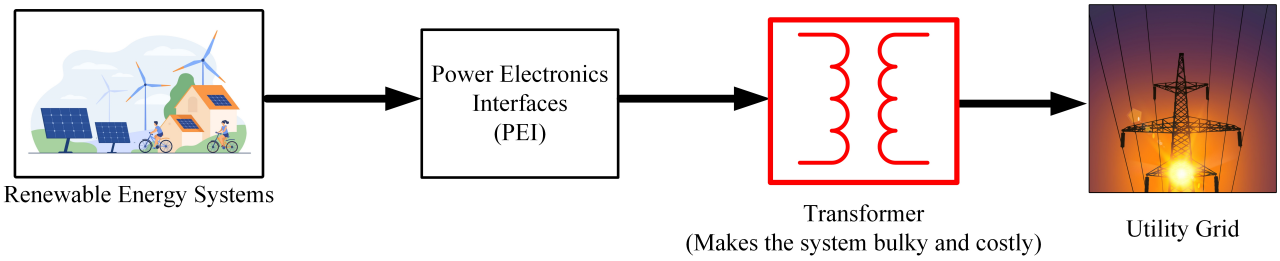
PV	Photovoltaic
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
GMPP	Global Maximum Power Point
LMPP	Local Maximum Power Point
AC	Alternating Current
DC	Direct Current
THD	Total Harmonic Distortion
CHB	Cascaded H-Bridge
HERIC	Highly Efficient and Reliable Inverter Concept
MLC	Multi Level Converter
PWM	Pulse Width Modulation
HV	High Voltage
RMS	Root Mean Square
HCPWM	Hybrid-Carrier Pulse Width Modulation
PDPWM	Phase Disposition Pulse Width Modulation
LCRPWM	Leakage Current Reduction Pulse Width Modulation
PSPWM	Phase Shifted Pulse Width Modulation
KVL	Kirchhoff's Voltage Law
RES	Renewable Energy System
EMI	Electromagnetic Interference

Chapter 1

Introduction

1.1 Motivation

Up to 5 kW PV installations, microinverters are common alternatives for the typical string solar inverters. The demerit of this technology is the slightly initial cost. However, the merits offered by this technology outweigh the demerits such as independent operation of each PV module allowing efficient energy generation. Renewable energy systems utilize power electronic interfaces for connecting them with the grid. It should be noted that although it is important to provide galvanic isolation between the grid and the renewable energy system, the addition of transformers makes the system bulky and costly. Moreover, in residential PV systems, some of the PV configurations prevents each PV module from operating indepedently which has a detrimental effect on the system efficiency. Therefore, there is a need to design a microinverter that can help in minimizing these problems.



1.2 Research Questions

The focus of this thesis is to develop a microinverter for residential PV systems. This thesis answers the following research questions:

- What are the benefits of utilizing a microinverter in contrast to utilizing string and centralized inverter configurations for residential PV systems?
- What are the various features offered by state of the art microinverter topologies? How can the benchmarking of the right microinverter solution be carried out among the investigated topologies?
- How can the design, modelling and control of such a microinverter be carried out? What are the approaches utilized for controlling the grid current in such converters? How are they different from each other?
- How can the hardware design of such a microinverter be carried out? How to test and evaluate the performance of such a prototype?

Although being out of the scope of the research questions, several MPPT techniques were also investigated along with a comparative analysis.

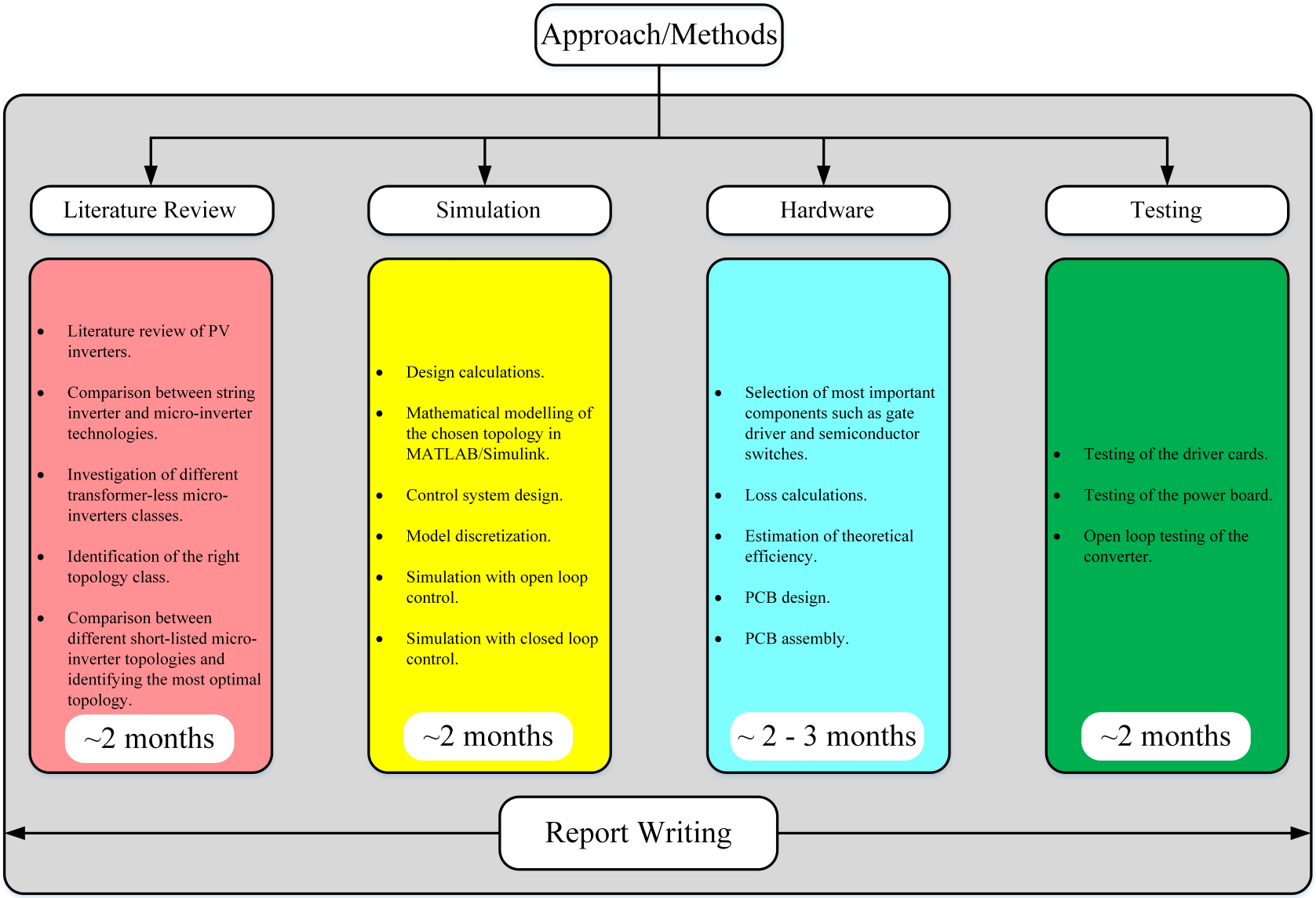


Figure 1.1: Approach/Methods

1.3 Thesis Organization

This thesis is divided into **9** chapters:

- **Chapter-2**: The literature review of transformerless PV inverters with the focus on string and microinverters is carried out. A general comparison between both types of PV inverters has been performed. Several topologies have been studied in both the categories. A comparative analysis was performed on these short-listed topologies on the basis of certain criteria essential for the application and the best topology for this application has been selected.
- **Chapter-3**: The design calculations are performed for the chosen topology.
- **Chapter-4**: The mathematical modelling of the microinverter and the control system design was carried out.
- **Chapter-5**: The simulation results are provided here.
- **Chapter-6**: The component selection for the microinverter under design has been carried out. Loss calculations have been performed for the semiconductor switches and, gate driver in a systematic manner. The theoretical efficiency of the microinverter has been estimated.
- **Chapter-7**: The design of the hardware prototype begins, a general PCB structure of the prototype is made. General remarks for each section of the prototype have been provided. Furthermore, the PCB design of the hardware prototype, fabricated PCB boards as well as the complete assembly of the prototype has been illustrated.
- **Chapter-8**: The results obtained during hardware tests are shown. The open-loop efficiency has been determined here.
- **Chapter-9**: The conclusions and scope for future work have been provided here.

1.4 Limitations

- The simulation is based on a mathematical model of the converter.
- The design of the filter inductance is carried out using the current ripple method.
- The DC/DC conversion stage has not been studied.

1.5 Conclusion

In this chapter, the motivation behind conducting this thesis has been provided along with the research objectives. Approach/methods utilized for this thesis have been illustrated along with an approximate timeline. This was followed by giving a brief description regarding the organization of this thesis. This chapter is then concluded with limitations faced during this thesis.

Chapter 2

Background Knowledge

2.1 Classification of PV Inverters

Photovoltaic inverters can be classified on the basis of PV panel arrangement. Literature indicates that the most commonly used configurations are as follows:

- Centralized Inverters
- String Inverters
- Micro Inverters (MI)

2.1.1 Centralized Inverters

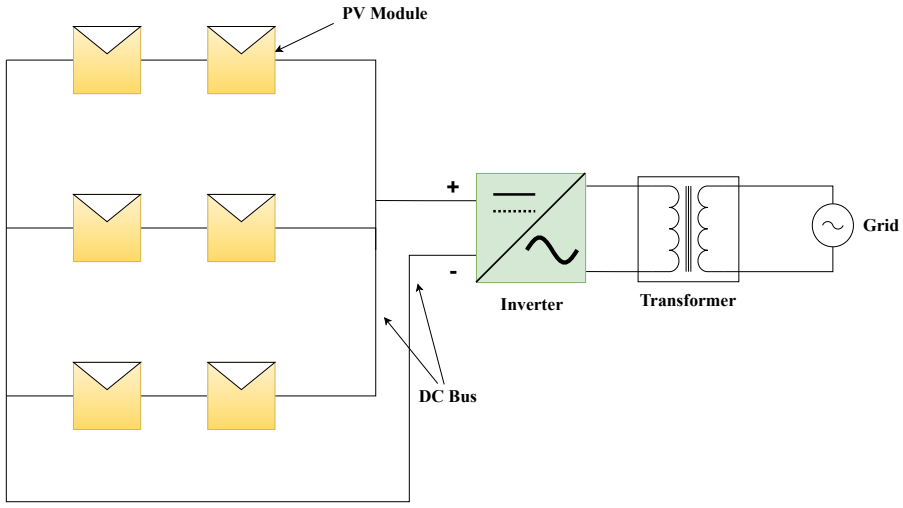


Figure 2.1: Centralized inverter configuration

Centralized inverters are an old technology. They are usually used in medium-high voltage applications. The configuration involves the entire PV system connected to the central inverter, hence, the name centralized inverter. Figure 2.1 shows a schematic representation of centralized inverter configuration of a PV system.

Advantages

Inverters used in such configurations, are rated for higher power and thus exhibit higher efficiency. Since, a single inverter is required to accomplish the task of power conversion, the overall capital cost is also small [1].

Disadvantages

In PV systems, diodes are installed at the end of PV string to ensure that the flow power is unidirectional, i.e. from PV panel to inverter. These diodes are required to withstand the voltage and the current generated by the complete string. As a result, with time, these diodes start contributing to the overall power losses in the system [1]. As mentioned earlier, centralized inverter configuration is employed in large PV systems. This means that the installation complexity is high. Moreover, PV systems of such configuration face the problem of partial shading which leads to mismatch losses. As a result, MPPT algorithm implemented for the string, does not guarantee that each PV module operates at its MPP [2]. If the PV panels are spread over a wide geographical region, the length of the DC cable required to connect the panel and the inverter would be very long. This results in additional power losses in the cable.

2.1.2 String Inverters

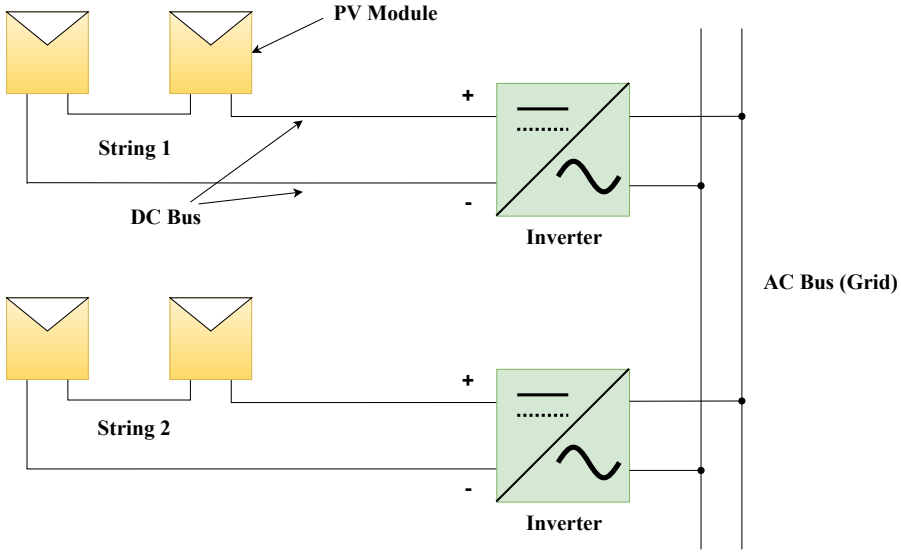


Figure 2.2: String inverter configuration

A refined version of the centralized inverter configuration. In this configuration, the PV system is divided into several series connected PV panel groups known as strings. Each string is connected to an inverter which later on interfaces them with the grid as shown in Figure 2.2.

Advantages

When PV panels are installed on rooftops and positioned on a non-uniform area, installation with the same orientation is therefore not possible and as a result, they are exposed to different shading conditions during the day [3]. By using this type of configuration, the problem of orientation is not only eliminated but, also it allows MPPT of each string independently thereby, improving the overall efficiency compared to centralized inverters. Moreover, the length of cable required per string configuration is also less compared to the centralized inverter configuration.

Disadvantages

Similar to centralized inverters, this configuration also suffers from the effect of partial shading. Since, one string is connected to one inverter. This increases the initial capital cost of the system as the number of inverters required would be equal to the number of strings in the system.

2.1.3 Microinverters

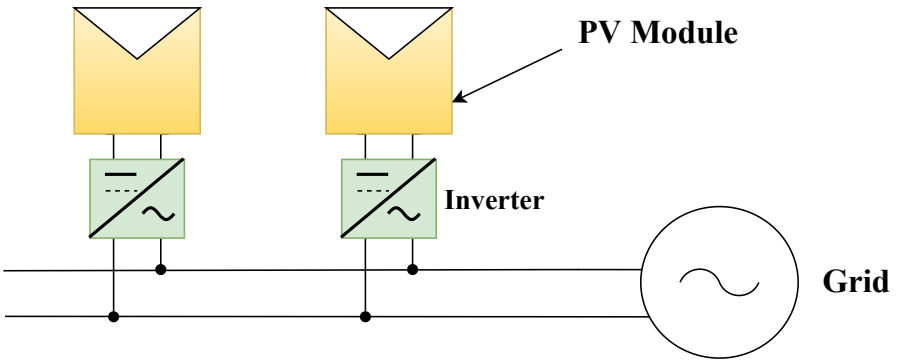


Figure 2.3: Micro Inverter configuration

Figure 2.3 shows 2 microinverters interfacing 2 PV modules to the grid. Microinverters, also known as module integrated converters or AC module can be considered to be derived from string inverters, however, the implementation is at the module level rather than the string level. In this type of configuration, each PV module is integrated with an inverter.

Advantages

Eliminates the issue of partial shading/mismatch losses between the PV modules. This is because each PV module operates independently in this case. Microinverters are designed for the best power density allowing them to be placed behind the PV modules. This configuration exhibits redundancy or no single point of failure in the system. For instance, if a PV module is under influence of partial shading or if there is failure of one of the microinverters, it does not hamper the overall operation of the system and hence, the efficiency of the system does not reduce significantly.

Disadvantages

1. A microinverter is attached to the PV module, hence, it is subjected to unforgiving environmental conditions like humidity, temperature, lightning, etc. This degrades the Mean Time to Failure (MTTF) [4].

2. Although, MI systems have a lower cost, yet, for large PV systems the cost per watt exceeds that of a string inverter for the same size [4]. Faults in the system may increase the maintenance complexity as inverters are difficult to access [5].

3. MI systems are designed for good power density which would imply a compact design of the inverter. This means that it has to house a lot of components in a compact space. This indicates that each and every component is a potential point of failure [6].

2.2 Comparison between String Inverters and MicroInverters

1. **Partial Shading/Mismatch between PV panels**
   The effect of partial shading on PV systems employing microinverters are minimal or none. This is because, each module has its own inverter. As a result, if some modules are not able to deliver the required PV power at MPP due to partial shading, other panels can still operate at MPP without hampering the system efficiency. On the other hand, partial shading is a difficult problem to deal when utilizing PV systems with string inverters. There are 2 reasons:

   (a) A string inverter does the role of power conversion for the entire string and hence, MPPT algorithm will determine MPP with respect to the entire string [1].

   (b) Since the PV panels are connected in series, string MPP will be limited to the PV panel that has the smallest MPP (the panel which is subjected to partial shading) [5]. This leads to decrease in the overall output of the system.

2. **Scalability**
   Microinverter based configurations allow "plug and play" applications. System can be expanded with ease by simply adding more PV modules integrated with inverters without redesigning the entire system [5]. On the other hand, a new string inverter having a different power rating would be required depending on how many additional PV modules are added to the string.

3. **Reliability**
   Since the inverter is the most important component of the PV system, it is important for it to have a strong robust design such that it can withstand faults thereby, prolonging its lifetime. As a result, reliability distinguishes both string and microinverter systems.
   Single phase inverters utilize energy storing components such as capacitors for power decoupling. Electrolytic capacitors are the weakest components of an inverter [7]. The failure rate of a capacitor is directly proportional to its capacitance, operating voltage and temperature [8]. Since, string inverters are rated for a higher power compared to microinverters, they are most likely to fail much earlier compared to microinverters.

4. **Redundancy**
   As discussed previously, in microinverter PV systems, each PV panel operates independently and hence, there is no single point of failure. This means that, if one of the microinverters fail, it will not affect the operation of the whole system. On the other hand, in string inverter PV systems, since a single inverter takes up the responsibility of power conversion for the entire string, failure of the same would lead to shutting down of the entire PV string.

5. **Safety**
   Safety is a very important factor when it comes to PV systems. Safety in PV systems can be at risk due to the following reasons [9]:

   (a) Shock Hazards.

   (b) Arc Faults.

   In string inverter configuration, the system voltage can be as high as 600 V DC which is fatal. On the other hand, the DC voltage level associated with microinverters can be as high as 40 V DC [9].
   Arc Faults are also common in large PV systems. In string inverters, the system is spread over a large area. PV panels are connected in series-parallel combination thereby, amplifying both voltage and current levels. Portion of the DC cables is exposed for connection purposes. As a result, there is a high probability that arcing may occur between 2 neighboring exposed conductors of the cables. On the other hand, in the microinverter PV systems, the DC voltage can be between 18 V up to 40 V. At this voltage level, it is difficult to maintain an arc. As mentioned before, since microinverters are attached at the back of the PV module, the DC wiring is minimal. This also reduces the chances of fires and arcing as discussed previously [1], [9].

The above comparative study of both string and microinverters on the basis of several factors gives an insight that microinverters prove to be a promising technology in the future as compared to string inverters.

2.3 Classification of PV Microinverters

Literature indicates that PV microinverters can be classified as follows:

1. Number of power conversion stages

   (a) Single stage.

   (b) Double stage/Multi-stage.

2. Ability to provide galvanic isolation

   (a) Isolated.

   (b) Non-Isolated.

2.3.1 Single Stage PV Microinverters

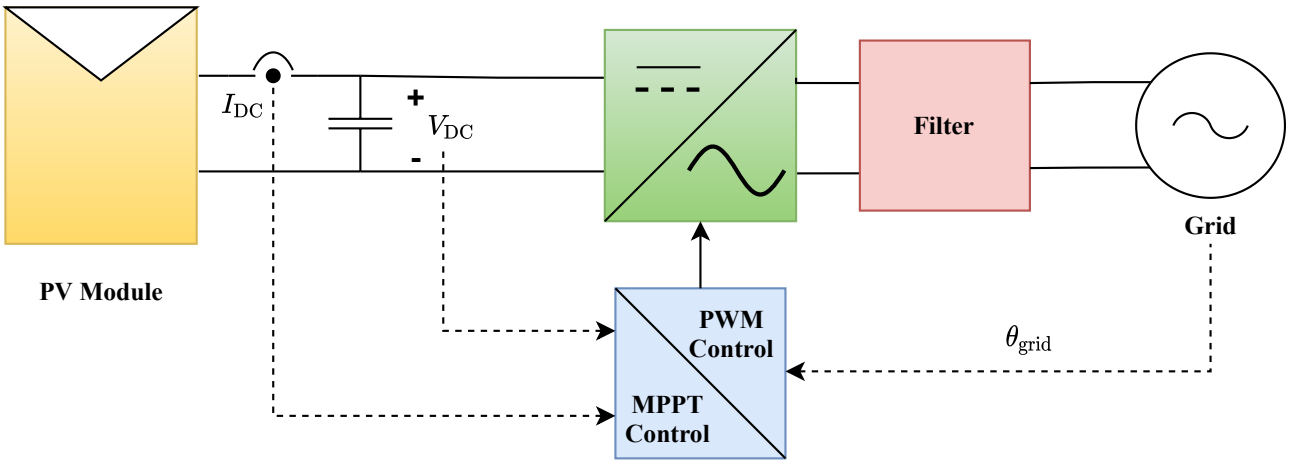


Figure 2.4: Single Stage PV Microinverter

Figure 2.4 shows a block diagram representation of a single stage PV microinverter. A single stage microinverter steps up the DC voltage of the PV module such that the PV module operates at MPP and then converts this DC power to AC power in a single stage [2]. In such configuration, the DC decoupling capacitor is installed between the PV module and the converter. The converter performs both MPPT and rectified sine current shaping operations. In such configurations, the DC link is known as a pseudo DC-link [1].

Advantages

1. Requires a single controller that ensures MPPT and current injection into the utility grid while maintaining an optimum power factor and THD as per grid standards.
2. Smaller component count.
3. Compact design.
4. Conversion efficiency is very high since, both DC-DC and DC-AC conversion occurs in a single stage.

Disadvantages

1. The presence of double frequency ripple in the voltage requires a very large value of electrolytic decoupling capacitors.
2. MI are attached at the back of the PV module. As a result, they are subjected to extreme temperatures, which increases the probability of failure of the electrolytic capacitor thereby, decreasing the lifetime to less than 25 years.
3. Frequent failures would require replacement, and hence, would lead to increase in maintenance cost.

2.3.2 Double-Stage Microinverters

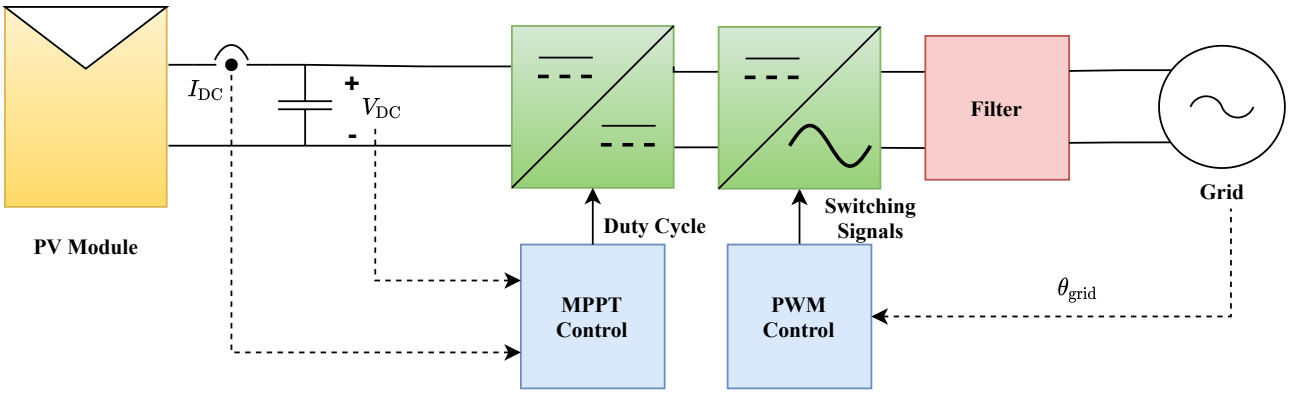


Figure 2.5: Double Stage Microinverter

Figure 2.5 shows a block diagram representation of a double stage PV microinverter. A double stage microinverter performs power conversion in 2 stages:

- The first stage consists of a DC-DC converter that regulates the voltage of the PV module to a sufficient level for the second stage, followed by extraction of maximum power from the PV module.
- The second stage performs the DC-AC conversion.

The power decoupling capacitor in such configurations are installed between the DC-DC converter and the DC-AC converter. As a result, this configuration is also known as microinverters with DC link [1].

Advantages

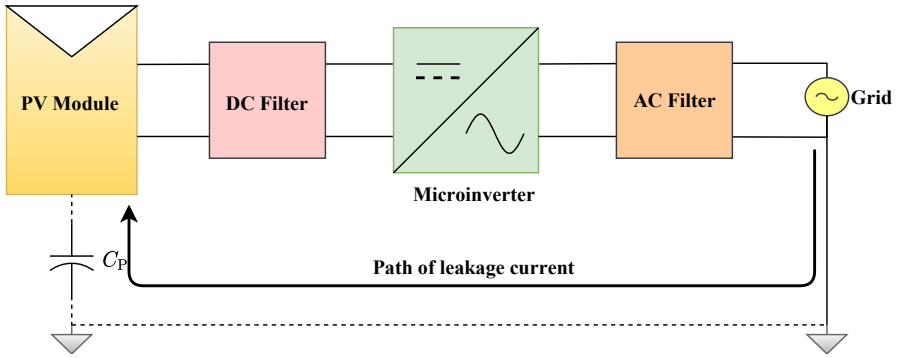
1. Each power conversion stage is controlled by 2 separate controllers. This reduces control system complexity as compared to single stage inverters. More importantly, control strategies of both stages can be different so as to optimize the efficiency of the inverter [1].
2. Since, the decoupling capacitor is located between the DC-DC converter and DC-AC converter, the DC link is at a higher voltage level compared to the PV side. As a result, a small decoupling capacitor can be used. This improves the reliability of the inverter.

Disadvantages

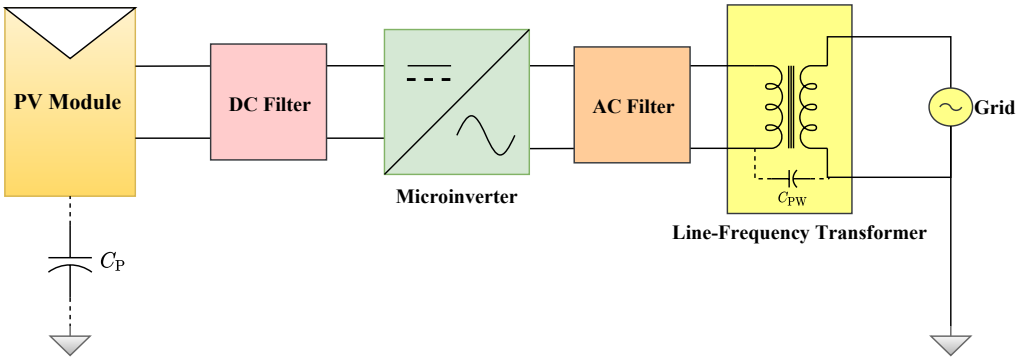
1. Due to the presence of 2 conversion stages, the component count is considerably higher compared to the single stage configurations.
2. Smaller decoupling capacitor value does not eliminate the issue of extreme temperatures.
3. The presence of 2 power conversion stages, leads to a decrease in the conversion efficiency.

Non-Isolated PV microinverters are microinverters where the circuit topology does not incorporate a galvanic isolation between PV module and the grid. Isolated PV microinverters on the other hand, incorporate galvanic isolation between the PV module and the grid.

2.3.3 Significance of galvanic isolation in microinverters



(a) Microinverter without galvanic isolation



(b) Microinverter with galvanic isolation

Figure 2.6: Significance of galvanic isolation

Figures 2.6a and 2.6b illustrate microinverters without galvanic isolation and with galvanic isolation respectively. The chassis of the PV module and the ground act as 2 plates of a capacitor with air as the dielectric medium. In both arrangements, this capacitor is represented by C_P. The value of this parasitic capacitance depends on several factors such as temperature, moisture content, humidity, etc. In case of microinverters without galvanic isolation, a return path for the current exists between ground of the grid and the parasitic capacitance. As a result, the parasitic capacitor, DC and AC filters as well as the grid impedance interact with each other to form a common mode resonance circuit. A varying common mode voltage across the terminal voltage of the microinverter can cause the excitation of this resonant circuit thereby generating common mode currents also known as leakage currents. This leakage current circulates in the direction shown in Figure 2.6a and thus, reaches the PV module [10].

On the other hand, in the case of microinverters with galvanic isolation, a line frequency transformer is utilized. Between the isolated primary and secondary windings of the transformer, there exists a parasitic capacitance, C_{PW}. The value of C_{PW} is much smaller than C_P and hence, the equivalent common mode impedance seen by the leakage currents is significantly higher. Therefore, leakage currents are minimized to some extent in such an arrangement.

At the same time, it is important to note that addition of line frequency transformer would not only make the system bulky but, also increases the overall cost of the system. Hence, the focus of this thesis would be to implement a non-isolated high power density microinverter.

2.4 Non-isolated Double Stage PV Microinverters

Based on the literature studied, non-isolated double stage microinverter topologies containing a cascaded DC/AC topology such as the cascaded H-bridge (CHB), H5 and HERIC proposed in [11]–[13] have no split capacitor arrangement whereas, topologies such as diode clamped MLC and flying capacitor proposed in [11], contain split capacitor arrangements.

It has been observed that the split capacitor arrangement in cascaded variants serves the purpose of splitting up the DC link voltage for obtaining the required number of voltage levels at the output. Most of the non-cascaded topologies found in the literature [10], [14]–[17] have implemented a split capacitor arrangement. However in this case the split capacitor arrangement serves 2 functions:

- It splits up the DC link voltage equally.
- It helps in clamping of the terminal voltage to half the DC link voltage as part of the passive clamping circuit during the freewheeling period.

In a nutshell, non-cascaded topologies have been designed from the perspective of mitigating common mode leakage currents which is the biggest issue due to the absence of galvanic isolation. A PV system with non-cascaded microinverters may help in mitigating leakage currents however, it also introduces other problems in the system.
For better harmonic performance, microinverters are operated on the principle of Pulse Width Modulation (PWM) to push the harmonics at the output to higher orders. Higher the switching frequency, higher the order of harmonics, smaller the size of the low pass filter but, at the cost of increased switching losses. This degrades the overall efficiency of the system significantly since each converter is operating independently. Moreover, reliability takes a big hit, as HV electrolytic capacitors are utilized for the split capacitor arrangement.

On the other hand, we have cascaded topologies, consider a PV system consisting of several microinverters connected in cascaded fashion.

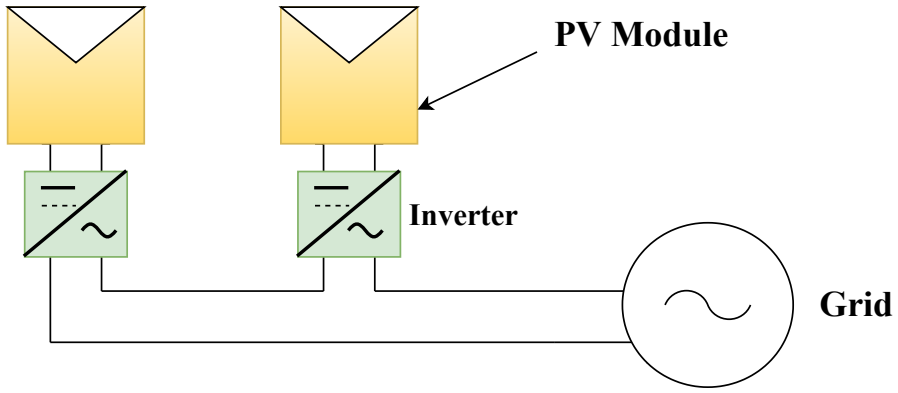


Figure 2.7: Concept of cascaded microinverters

Cascaded connection provides the following benefits:

- Higher number of levels can be achieved at the output voltage of the converter.
- Higher the number of levels, better will be the harmonic performance of the system.
- A very unique advantage that the cascaded microinverters have to offer is the ability to select a smaller switching frequency and yet, effectively push harmonics to higher orders. This is because the effective switching frequency of the system is directly proportional to the number of cascaded microinverters. Smaller effective switching frequency leads to smaller switching losses thereby, leading to smaller filter size and significant improvement in efficiency. The reduction in filter size however, increases the common mode leakage currents which is undesirable.

However, due to its popularity, several modulation strategies have been proposed which focus on mitigating the leakage currents in the converter without utilizing any additional passive components [12], [18]–[21]. These strategies are based on yet another inherent feature of cascaded microinverter, redundant switching states. By developing the modulation strategies that turn on the semiconductor switches in such a manner that the common

mode voltage remains constant, the leakage currents can be minimized.

While the total grid leakage current gets minimized, the inter-module leakage currents still exist and are difficult to mitigate even with galvanic isolation. Kumar et al. [22] has proposed a method to minimize the inter module leakage currents in cascaded H-bridge grid connected PV inverters however, this method requires usage of additional passive components as well as a modified PWM strategy which is not desirable from the point of view of size, cost and control complexity. However, it should be noted that they do not interact with the utility grid and remain within the system only.

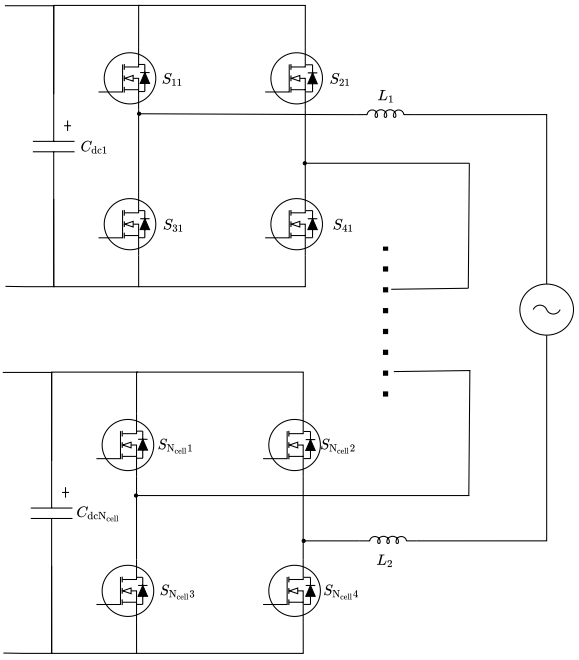
With these insights, it was concluded that the selection process for the DC-AC topology would be made for the cascaded microinverters.

2.4.1 Criteria for topology selection

The following criteria were decided for selecting an optimal topology for the DC-AC conversion:

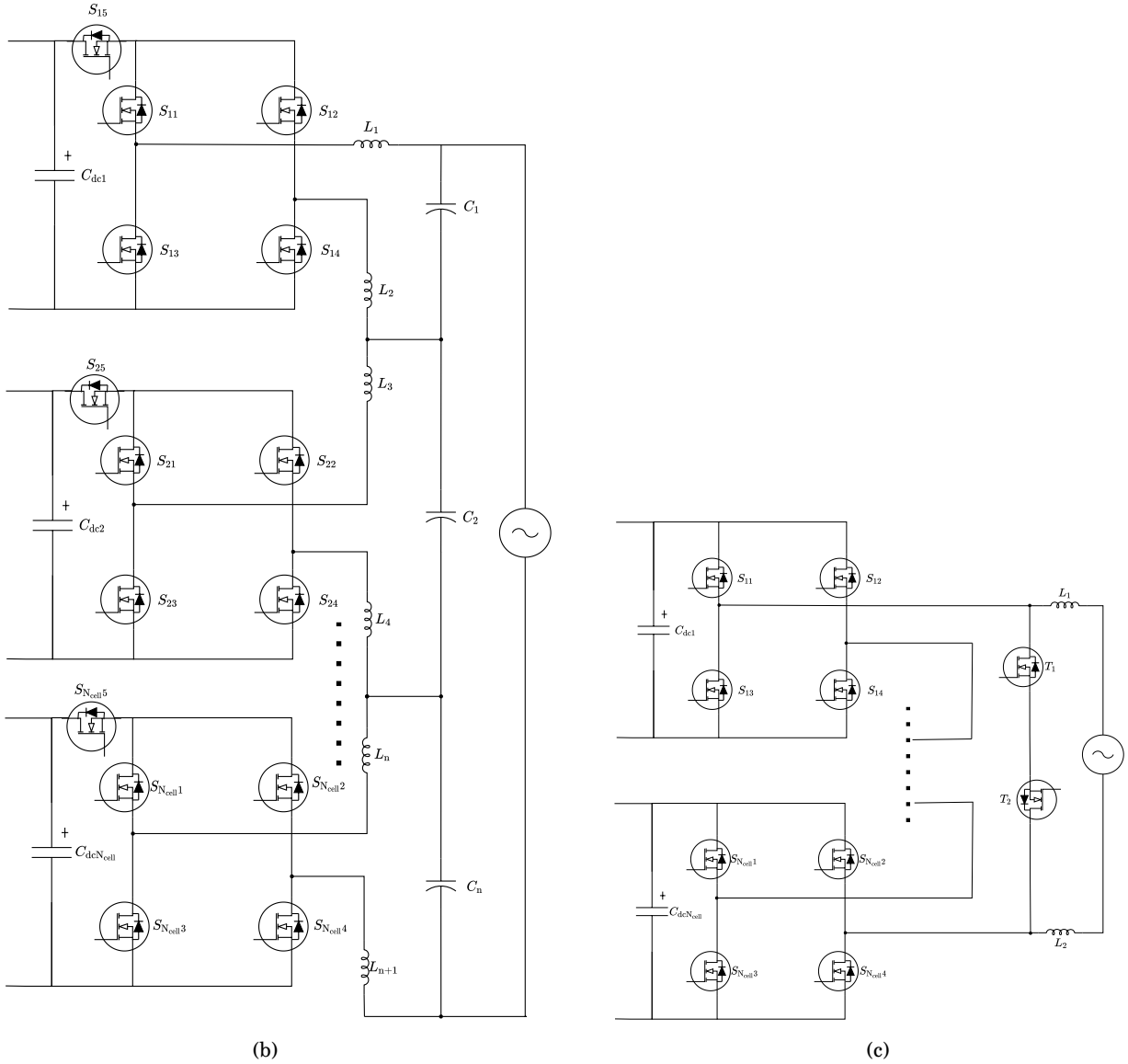
- **Total Harmonic Distortion (THD)**
  According to the IEEE 1547 Grid Standards, THD < 5% [23].
- **Efficiency**, $\eta \geq 95\%$.
- **Leakage current suppression**
  According to the VDE0126-1-1 German Standard, the leakage current must be less than 300 mA peak [24].
- **Modularity**
- **Scalability**

Based on these 6 criteria, 3 topologies were short listed. These topologies are illustrated in Figure 2.8.



(a)

Figure 2.8: Short-listed topologies for DC-AC conversion stage



(b) (c)

Figure 2.8: Short-listed topologies for DC-AC conversion stage (Continued)

Table 2.1 shows a comparative study between these short-listed topologies.

Topology	Component Count	Number of switches	Features	Drawbacks	Leakage Current	Efficiency	THD
Cascaded H4 Topology [11]	5	4	• Simple structure. • Can be used to integrate multiple PV panels independently. • Control is simple. Switching redundancies exists. Cascade connection inherently introduces more redundancies [11].	• Due to the presence of independent DC sources (PV modules), there are multiple common mode paths and loops for the leakage current [25].	• 240 mA peak (70 mA RMS) as indicated in [18] for a 5-level CH4 topology utilizing HC-PWM. • 1.33 mA RMS as indicated in [19] for a 5-level CH4 topology utilizing modified PD-PWM. • 24 mA RMS as indicated in [21] for a 9-level CH4 topology utilizing LCRPWM.	98.8% as indicated in [19]	• 4.25% [18] • 4.88 % [19] • 1.72% [21]
Cascaded H5 Topology [12]	6	5	• An additional switch is added on the +ve DC bus for decoupling the PV side from the grid. • MC-PWM has been used for the converter switches. • This topology effectively suppresses leakage currents when operating in both symmetrical and asymmetrical operation.	• The output filter arrangement has been made using split inductors and capacitors. • A mid-point has to be established between every 2 H5 cells. This will increase the circuit complexity and wiring when dealing with more than 2 PV panels. • The modulation strategy implemented leads to a high leakage current value in the upper cell compared to the lower cell of the converter [12].	• Symmetrical Operation – Upper cell: 12.2 mA RMS – Lower cell: 9.76 mA RMS • Asymmetrical Operation – Upper cell: 19.1 mA RMS – Lower cell: 18.6 mA RMS	-	-
Cascaded HERIC [13]	7	6	• It is basically a cascaded H4 topology. However, 2 AC switches have been added across its output terminals. Hence, overall structure resembles that of a cascaded HERIC. • Utilizes the redundant switching states of CH4 topology and the freewheeling feature of the HERIC topology.	-	264 mA peak (20.2 mA RMS)	-	4.65%

Table 2.1: Comparative study of short-listed topologies

2.5 Maximum Power Point Tracking

In this chapter, several algorithms proposed in literature for tracking the maximum power point (MPP) have been discussed. Two MPPT categories have been studied. Algorithms of both the categories have the same objective but, may or may not have the same approach.

2.5.1 Classification of MPPT Techniques

Bollipo et al. in [26] presents a review of over 23 MPPT techniques found in the literature. The MPPT Techniques/algorithms can be classified into 3 categories:

1. Classical Techniques.
2. Intelligent Techniques.
3. Optimization Techniques.

Classical MPPT techniques are preferred for locations receiving uniform solar irradiation annually. As a result, such techniques focus on achieving a single maximum power point in PV curve. Intelligent and Optimization based MPPT techniques are preferred when the solar irradiation is non-uniform especially during partial shading conditions. Such techniques need to consider 2 types of maximum power points in a PV curve, a global maximum power point (GMPP) and a local maximum power points (LMPP). The objective of MPPT techniques falling under intelligent and optimization categories is to identify GMPP out of all LMPPs.

For this study, only classical and intelligent MPPT techniques have been considered. 2 techniques in both the categories have been chosen for the study.

2.5.2 Classical MPPT Techniques

Perturb and Observe Algorithm (P&O)

Perturb and Observe algorithm (P&O) is the most popular algorithms implemented for MPPT. The voltage of the PV panel is chosen as the perturbation variable. The algorithm computes the difference between 2 points in a PV curve and determines the position of the operating point of the PV panel. Based on this operating point, the algorithm updates the reference voltage for the DC-DC converter in order to effectively track MPP.

Conditions	Operating Voltage	Duty Cycle
$\frac{\Delta P}{\Delta V} > 0$	$V_{op} < V_{MPP}$	Increase
$\frac{\Delta P}{\Delta V} < 0$	$V_{op} > V_{MPP}$	Decrease
$\frac{\Delta P}{\Delta V} = 0$	$V_{op} = V_{MPP}$	Maintain

Table 2.2: Conditions encountered in P&O algorithm

Table 2.2 tabulates the conditions that the algorithm needs to consider for while updating the reference voltage. The drawback of this algorithm is that it is never able to achieve the exact MPP. It oscillates around the MPP point. Moreover, it is capable of tracking only GMPP which makes it unfavorable under partial shading conditions (PSC).

Improved P&O Technique

Sai et al. proposed an improved P&O tracking algorithm in [27]. This approach requires 4 quantities, voltage, current, irradiance and array temperature. The algorithm is divided into 2 operating modes:

1. Global Maximum Detection Mode.
2. Voltage Search Mode.

The global maximum detection mode performs calculation, sorting of peak voltages across the PV module and sets the initial value of the duty cycle. On the other hand, the voltage search mode acquires the sorted peak voltage values and utilizes the conventional algorithm to identify the global maximum power point among them.

Kollimalla and Mishra proposed a novel adaptive P&O algorithm. In this algorithm, the PV current is chosen as the perturbation variable in contrast to the voltage variable in the conventional P&O algorithm. A brief explanation about the significance of selecting current as the perturbation variable rather than the voltage is given in their paper [28]. The algorithm is divided into 2 sub-algorithms:

1. Current Perturbation Algorithm (CPA).
2. Adaptive Control Algorithm (ACA).

The CPA consists of the conventional P&O algorithm with current perturbation. On the other hand, the ACA has been implemented to mitigate the effects of PSC on the system. It ensures that the operating point stays in the vicinity of the MPP and therefore, the search window is reduced which reduces the effort taken by the controller in tracking the MPP. The governing equations, converter and controller design can be found in their paper.

Incremental Conductance Algorithm (INC)

The incremental conductance method is based on the same approach as the P&O algorithm. However, for tracking purposes it utilizes the slope of the I-V curve.

Conditions	Operating Voltage	Duty Cycle
$\frac{\Delta I}{\Delta V} > -\frac{I}{V}$	$V_{\text{op}} < V_{\text{MPP}}$	Increase
$\frac{\Delta I}{\Delta V} < -\frac{I}{V}$	$V_{\text{op}} > V_{\text{MPP}}$	Decrease
$\frac{\Delta I}{\Delta V} = -\frac{I}{V}$	$V_{\text{op}} = V_{\text{MPP}}$	Maintain

Table 2.3: Conditions encountered in INC algorithm

Table 2.3 tabulates the conditions that the algorithm needs to consider before making the decision where $\frac{\Delta I}{\Delta V}$ represents the incremental conductance and $\frac{I}{V}$ represents the instantaneous conductance [29]. The algorithm performs better compared to P&O. Tracking efficiency can be enhanced by increasing the step size of perturbation variable, but, at the cost of more oscillations around MPP.

2.5.3 Improved INC

Chauhan et al. proposed an improved INC method in [30]. The method utilizes the conventional INC algorithm to generate the required reference voltage. This reference voltage is fed to a PID controller whose gains are optimized using the Grey Wolf Optimization algorithm for effectively controlling the duty cycle of the converter.

Tey and Mekhilef proposed an algorithm that not only took partial shading under consideration but, also took the load variations that occur in the system [31]. The authors have tested their algorithms for 3 cases and have also provided detailed explanations about the flow in the algorithm for each of the cases. The algorithm was integrated within the control of SEPIC converter. Steady state oscillations around MPP are completely eliminated.

2.5.4 Intelligent MPPT Techniques

Artificial Neural Networks (ANN)

"Artificial Neural Networks (ANN) can be viewed as parallel and distributed data processing systems that consists of a numerous processing elements called neurons" [32]. ANN can be represented by a network consisting of nodes and edges which can be considered to be analogous to the brain's neurons connected to each other via synapses.

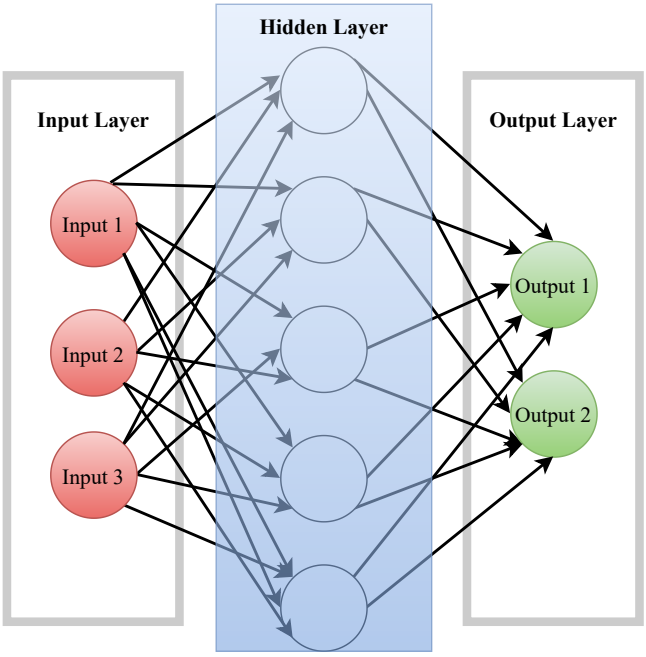


Figure 2.9: Typical structure of an artificial neural network [26]

Figure 2.9 shows a typical diagram of an ANN. A neural network in general consists of 3 layers. The input layer, hidden layer and the output layers. With reference to MPPT, the input layers will consist of either PV power and PV voltage or irradiance and temperature or a combination of both as the input variables and the output layer will consist of either V_{MPP} or GMPP as the output variables [26]. The decision making of selecting the best possible value for the output variable is performed in the hidden layers. After an ANN is developed, training data is fed to the network to assess its performance and also to get the neural network arrive at the right decisions. The quantity of training data fed to the ANN is directly proportional to the probability that it will track MPP effectively [26].

A simulation study was performed by Younis et al. who proposed an improved P&O MPPT algorithm driven by ANN in [33]. The ANN in the proposed system, consisted of 5 input variables, irradiation, ambient temperature, and the temperature coefficients of voltage and current. The output variable was chosen to be V_{MPP}. Data consisting of over 1500 values was used to train, validate and test the network. Out of the 1500 values, 1300 values were used for training purpose. A comparison between the values of V_{MPP} obtained by conventional P&O algorithm and the values predicted by the ANN was made. Simulation results indicate that the ANN predicted values nearly follow the values identified by the conventional algorithm [33].

Divyasharon et al. proposed ANN based MPP for PV systems under varying climatic conditions in [32]. A simulation study was conducted by the authors and the algorithm was tested on a Cuk converter. The results of the Cuk converter were compared with that of a boost converter. The algorithm was tested for 5 different conditions. Simulations results indicate that the proposed ANN based MPPT algorithm worked significantly better with a Cuk converter compared to the boost converter for all the 5 test conditions.

Fuzzy Logic Technique

Fuzzy logic is a unique approach for MPPT. Figure 2.10 shows a block diagram representing different stages in a Fuzzy logic technique.

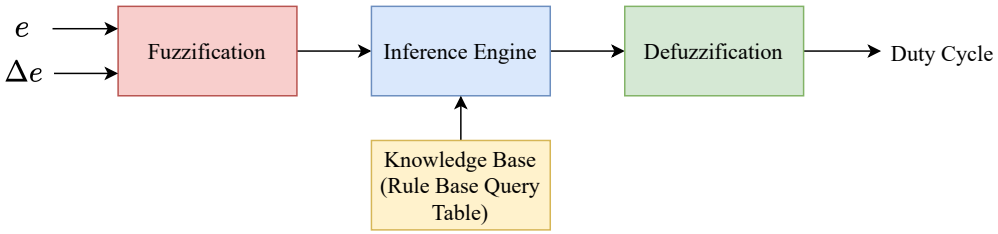


Figure 2.10: Block Diagram representation of Fuzzy Logic stages [34]

A fuzzy logic consists of 3 stages:

1. Fuzzification
2. Rule Base Query Table, also known as Fuzzy rules
3. Defuzzification.

Literature indicates that 2 of the most commonly used classical techniques, P&O and INC have been implemented using fuzzy logic [34], [35].

Ozdemir et al. presented a fuzzy logic based MPPT controller designed for a quadratic boost converter in [35]. The fuzzy logic controller (FLC) consists of PV power and voltage as the input variables and duty cycle as the output variable.

Another fuzzy logic implementation was carried out Zainuri et al. in [34]. The proposed controller has both the simplicity of P&O as well as the intelligence of FLC. The controller was implemented to modulate the duty cycle of a boost converter. The proposed approach was compared with the conventional P&O method and the standard FLC method. Simulation and experimental results indicate that the proposed method had out-performed the other 2 methods. One unique result found by the authors was that the proposed method performed much better in low irradiance scenarios.

2.6 Selection Criteria for MPPT Algorithms

There are many criteria on the basis of which a MPPT algorithm can be judged. However, there is no single criteria that is considered to be the best for selecting the right algorithm. For this study, the following criteria have been considered:

1. Number of Sensors
2. Control Complexity
3. Tracking Speed
4. Tracking Accuracy
5. Efficiency

Algorithm	Number of sensors	Control Complexity	Tracking Speed	Tracking Accuracy	Efficiency
P&O	2	Simple	Slow	Medium	97.6%[36]
INC	2	Simple	Slow	Medium	98.5%[36]
Improved P&O [27]	4	Medium	Very fast	High	-
Improved P&O [28]	3	Medium	Fast	High	-
Improved INC [30]	2	Medium	Fast	High	97.6%
Improved INC [31]	2	Medium	Fast	High	-
ANN MPPT [32]	2	High	Very fast	Very High	>99%
P&O with ANN [33]	2	High	Medium	Medium	94-95%
P&O with FLC [35]	2	Medium	Fast	High	99.10%
INC with FLC [34]	2	Medium	Fast	High	>99%

Table 2.4: Comparison between the different MPPT algorithms under study

Table 2.4 compares the various MPPT techniques that have been considered in this study.

2.7 Conclusion

- The cascaded H4 topology proposed in [11] allows fault tolerant operation as the system expands. Moreover, due to its level of popularity compared to its competitors as well as due to lower component count, many modulation strategies have been proposed in the literature which allows more flexibility in its control.
- The cascaded H5 topology proposed in [12] eliminates the drawback of multiple leakage current loops found in cascaded H4 topology. By introducing an additional switch at the DC bus, decoupling between the PV side and the grid is achieved, but, at the cost of increased number of switches per cell compared to the cascaded H4 topology for the same number of voltage levels. While, the modulation strategy proposed does help in mitigating leakage current in both symmetrical and asymmetrical conditions, the circuit complexity increases as the system expands.
- The topology proposed in [13] is based on the cascaded H4 topology however, by adding two AC switches across the terminals of the converter, the overall structure resembles that of a cascaded HERIC. Requires 2 additional switches compared to the cascaded H4 topology for the same number of voltage levels. The leakage current can be freewheeled using the 2 AC switches in accordance to the half cycle of the grid. Based on the comparative analysis conducted in Table 2.1, it was found that the cascaded H4 topology [11] proves to be a suitable candidate for the DC-AC conversion stage of the microinverter.
- In case of the MPPT techniques, the number of sensors utilized by the methods under study range from 2 up to 4.

- Among the classical methods, the conventional P&O as well as the INC algorithm utilize less number of sensors as well as deliver efficiencies greater than 97% however, lag behind the tracking speed compared to its competitors whereas, on the other hand, the improved variants of both these methods proposed in [27], [28], [30], [31] offer significant improvements in tracking speed as well as accuracy however, the control complexity involved as well as the number of sensors utilized is greater compared to the conventional variants.
- In case of intelligent methods, ANN and FLC based techniques proposed in [32]–[35] are superior compared to its competitors in terms of the sensors utilized, tracking speed, accuracy as well as efficiency. However, they lack the simplicity offered by the classical methods. ANN needs to be trained before implementing it on the field and hence, requires a lot of training data to be able to make the right decisions during MPPT. On the other hand, FLC requires knowledge about the system and the ability to convert this into a set of rules that can be interpreted by the controller.
- The microinverter that will be designed as the product of this thesis would be used for residential applications and hence, utilizing classical methods would be optimal as they would achieve the objective of MPPT tracking with a lower control complexity compared to intelligent methods.
- On the basis of the comparison made in Table 2.4, the conventional INC method can be used as an MPPT algorithm for the DC-DC conversion stage. The method proposed offers the best of both the worlds, i.e. utilization of only 2 sensors with faster tracking speed and simple control design but, at the cost of medium tracking accuracy.

Chapter 3

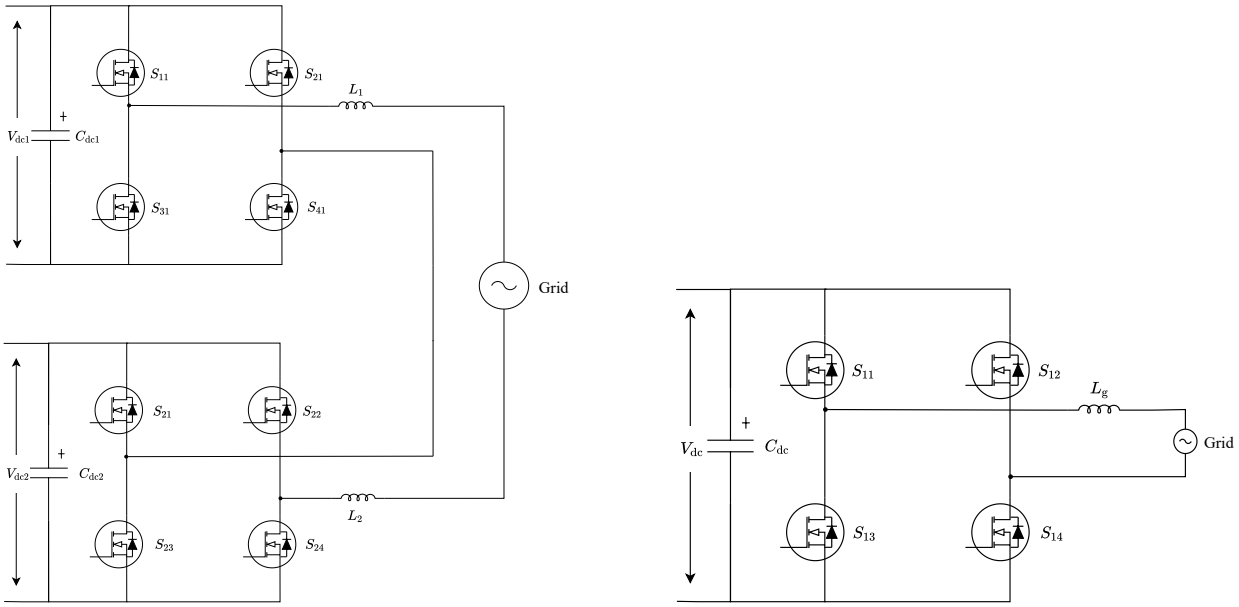
Design of CHB converter

3.1 Introduction

The CHB converter consists of several components such as semiconductor switches, DC link capacitors, low pass AC filters. For the modelling of converters, the components chosen cannot have arbitrary values because they affect the nature and performance of the converter. Moreover, the control system also depends on these values to achieve the required goals. In this chapter, the structure and working principle of CHB converter has been discussed. Guidelines for selecting the DC link voltage, DC link capacitance, number of cells, switching frequency, AC filter as well as semiconductor switches have been discussed. The chapter is concluded with the complete specifications of the CHB converter.

3.2 Structure and Working principle

CHB converters are multilevel converters formed by series connection of 2 or more single phase H-bridge converters. Figures 3.1a and 3.1b show structures of a CHB converter as well as its building block, the H-bridge converter.



(a) Cascaded H-bridge Converter

(b) H-Bridge Converter

Figure 3.1: Structure of CHB

Unlike the H-bridge converter that can only generate 3 voltage levels, the CHB converter can generate more number of voltage levels depending on the number of series connected H-bridge cells and modulation strategy.

3.3 Selection of DC link Voltage and number of cells

Parameters	Values
S_{rated}	2.25 kVA
$V_{\text{g(rms)}}$	230 V rms
f_{g}	50 Hz

(a) Large-Scale-Prototype

Parameters	Values
S_{rated}	500 VA
$V_{\text{g(rms)}}$	57.5 V rms
f_{g}	50 Hz

(b) Lab-Scale Prototype

Table 3.1: Known converter specifications

Table 3.1a and Table 3.1b show the known converter specifications.
For the sake of simplicity, the design calculations are carried out for the large scale prototype. The design steps essentially remains the same for the lab-scale prototype.

The permissible fluctuations in the grid voltage are in the range of **±15%** of the nominal value. Therefore,

$$V_{\text{g(max)}} = 1.15 \cdot \sqrt{2} \cdot V_{\text{g}}$$
$$\boxed{V_{\text{g(max)}} = 373.75 \text{ V}}$$

This means that the converter should be capable of delivering a peak terminal voltage greater than 373.75 V. As mentioned previously the building blocks of a CHB converter is a H-bridge converter, therefore, the terminal voltage can be expressed as [37],

$$\hat{V}_{\text{t}} \leq m_{\text{a}} V_{\text{DC}} \tag{3.1}$$

Therefore, considering that $m_{\text{a}} = 1$, the effective DC link voltage must be chosen such that,

$$\hat{V}_{\text{t}} \leq V_{\text{g(max)}} \leq V_{\text{DC}} \tag{3.2}$$

The DC link voltage must be sufficiently large enough for proper operation of the converter, under both steady-state and dynamic conditions [38].

$$\boxed{V_{\text{DC}} = 450 \text{ V}}$$

However, it should be noted that the DC link voltage must not be very high as it would lead to higher switching losses.
Based on the effective DC link voltage and the semiconductor switch ratings, the cell DC link voltage can be determined. For a switch having a voltage rating of 60 V, each cell can share a DC link voltage of

$$\boxed{V_{\text{dc}} = 50 \text{ V}}$$

Therefore, the number of cells are given by,

$$N_{\text{cell}} = \frac{V_{\text{DC}}}{V_{\text{dc}}} \tag{3.3}$$

$$\boxed{N_{\text{cell}} = 9}$$

3.4 DC link

The DC link serves as an important interface between the DC side and the converter side. The DC link capacitor serves the following functions:

- Ensures a constant DC voltage across the converter.
- Suppresses the ripples present in the DC voltage.
- Provides the necessary compensation in power caused as a result of differences between power injected by the DC source and the power injected into the grid.

In case of CHB converter, each H-bridge will have it's own DC link. Therefore, the determination of the DC link capacitance depends on the voltage and power for which each H-bridge has been designed as well as the permissible voltage ripple.

In [39], the expression for the DC link voltage ripple has been derived and is given by,

$$\Delta V_{\mathrm{dc}} = \frac{P_{\mathrm{dc}}}{2 \cdot \omega_{\mathrm{g}} \cdot C_{\mathrm{dc}} \cdot V_{\mathrm{dc}}} \tag{3.4}$$

Therefore, restructuring Equation 3.4, the expression for the DC link capacitance is given by,

$$\boxed{C_{\mathrm{dc}} = \frac{P_{\mathrm{dc}}}{2 \cdot \omega_{\mathrm{g}} \cdot \Delta V_{\mathrm{dc}} \cdot V_{\mathrm{dc}}}} \tag{3.5}$$

Note, that this is the minimum DC link capacitance. The minimum DC link capacitance for a 2 V ripple for the converter under design was found to be,

$$\boxed{C_{\mathrm{dc}} \geq 4 \text{ mF}}$$

3.5 Selection of Modulation Strategy

With the advent of multilevel converters, several modulation strategies have been proposed in the literature depending on the application and the converter topology. The modulation schemes can be classified based on the average switching frequency. For CHB converters, it was found that the Phase Shifted Carrier Pulse Width Modulation (PSPWM) strategy is the best [11].

The number of voltage levels generated by the converter utilizing PSPWM are $2N_{\mathrm{cell}} + 1$ with the maximum converter output voltage of $N_{\mathrm{cell}} V_{\mathrm{dc}}$.

3.6 Selection of Switching Frequency

3.6.1 Switching losses

For the same number of voltage levels, higher the switching frequency, higher will be the switching losses, however, smaller would be stress imposed on the semiconductor switches. On the other hand, having a smaller switching frequency would lead to distorted current due to presence of harmonics.

3.6.2 Modulation Strategy

The modulation strategy influences the overall switching frequency of the converter. For PSPWM [11], the effective switching frequency is directly proportional to the number of cells and hence, is given by,

$$\boxed{f_{\mathrm{sw(eff)}} = N_{\mathrm{cell}} \cdot f_{\mathrm{sw}}} \tag{3.6}$$

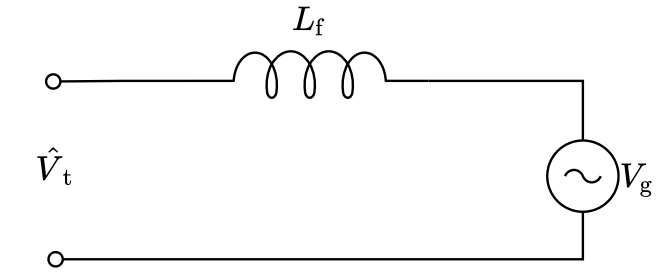
Therefore, a higher effective switching frequency can be achieved for the same number of voltage levels and at the same time, achieve better harmonic performance and lower switching losses [11].

A switching frequency of $\boldsymbol{f_{\mathrm{sw}}}$ **= 48 kHz** was selected for the lab-scale model, whereas a switching frequency of $\boldsymbol{f_{\mathrm{sw}}}$ **= 16 kHz** was selected for the large-scale model.

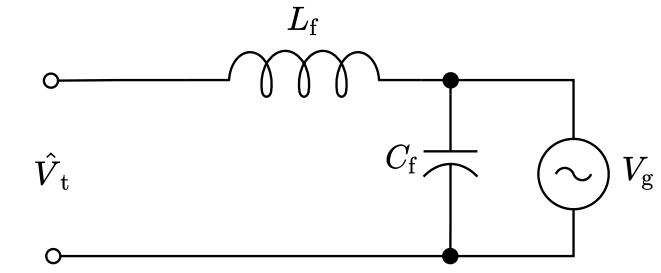
3.7 Power Conditioning

For interfacing an inverter with the grid, it is important to ensure that the residual harmonic content must be mitigated/filtered out to inject an optimum sinusoidal current. In such a scenario, low pass filters are used to interface an inverter with the grid.

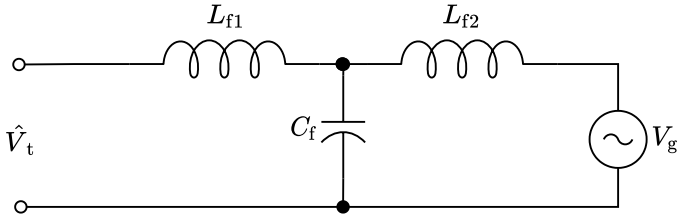
Several filter topologies have been discussed in the literature. The most popular topologies used are the L , LC and the LCL filter. L filter employs only a single inductor and is simple, however, more comparative studies as well as design guidelines have been made for LCL filters [40]–[42]. LCL filters are found to be widely used for interfacing purposes due to their small size and better attenuation when compared to an LC filter for the same inductor value [41]. Table 3.2, summarizes the key points that have been identified in the literature for the 3 considered passive filter topologies[40]–[43].



(a) L Filter



(b) LC Filter



(c) LCL Filter

Figure 3.2: Filters used for grid tie inverters

L filter	LC filter	LCL filter
• Size depends on the switching frequency. • First order filter. • 20 dB/decade attenuation at all frequencies [40]. • Offers a very large gain at all frequencies [40].	• Smaller size compared to L filter • Second order filter • Provides 12 dB/octave attenuation after cut-off frequency [40]. • Offers no gain before cut-off frequency [40] • Delivers a peak at the resonant frequency. Damping techniques can be implemented [41]. • Resonant frequency varies with grid impedance.	• Smallest size compared to L and LC filter. • Third order filter • Provides 60 dB/decade attenuation after cut-off frequency. [40]. • Offers no gain before cut-off frequency. • Better current ripple attenuation even with small inductance values. • Prone to resonance and also magnifies side-bands of the cut-off frequency [40]. • Offers better decoupling between the filter and the grid impedance [43]. • Selection of capacitor is a trade off between reactive power in the capacitor and inductor[42].

Table 3.2: Key points of studied passive filters

Based on the comparison, it was found that a simple L filter would serve as an optimum choice as an interface between the converter and the grid. The value of inductance can be calculated using the following equations stated in [44],

$$\boxed{L_{\mathrm{f}} = \frac{1}{16} \cdot \frac{V_{\mathrm{dc}}}{f_{\mathrm{sw}} \cdot \Delta i_{\mathrm{L(max)}}}} \tag{3.7}$$

where, $\Delta i_{\mathrm{L(max)}}$ is the maximum permissible current ripple.

$$\Delta i_{\mathrm{L(max)}} = \%\ i_{\mathrm{ripple}} \cdot \hat{i}_{\mathrm{g}} \tag{3.8}$$

$$\hat{i}_{\mathrm{g}} = \frac{2 \cdot N_{\mathrm{cell}} \cdot P_{\mathrm{dc}}}{V_{\mathrm{g(max)}}} \tag{3.9}$$

3.8 Conclusion

This chapter is concluded with updating Table 3.1a & Table 3.1b to Table 3.3a and Table 3.3b showing the calculated values of different parameters for the converter under design for both the cases.

Parameter	**Symbol**	**Value**
Rated Apparent Power	S_{rated}	2.25 kVA
Grid Voltage (rms)	$V_{\text{g(rms)}}$	230 V
Grid Frequency	f_{g}	50 Hz
Number of cells	N_{cell}	9
Effective DC link Voltage	V_{DC}	450 V
DC Link Voltage Ripple	ΔV_{dc}	2 V
DC link capacitance	C_{dc}	6.6 mF
Nominal Current	$\hat{i}_{\text{g}}$	13.834 A
Current Ripple	$\Delta i_{\text{L(max)}}$	10.37 A
Filter Inductance	L_{f}	2×60 μH
Switching Frequency	f_{sw}	16 kHz

(a) Large Scale Prototype

Parameter	**Symbol**	**Value**
Rated Apparent Power	S_{rated}	500 VA
Grid Voltage (rms)	$V_{\text{g(rms)}}$	57.5 V
Grid Frequency	f_{g}	50 Hz
Number of cells	N_{cell}	2
Effective DC link Voltage	V_{DC}	100 V
DC Link Voltage Ripple	ΔV_{dc}	2 V
DC link capacitance	C_{dc}	6.6 mF
Nominal Current	$\hat{i}_{\text{g}}$	12.29 A
Current Ripple	$\Delta i_{\text{L(max)}}$	2.45 A
Filter Inductance	L_{f}	75 μH
Switching Frequency	f_{sw}	48 kHz

(b) Lab-Scale Prototype

Table 3.3: Complete Converter Specifications

Chapter 4

Modelling & Control

4.1 Introduction

For designing the control systems, it is important to derive a mathematical model of the system. The mathematical model as well as control system design for both converter designs has been carried out in this chapter.

4.2 Modelling of the converter

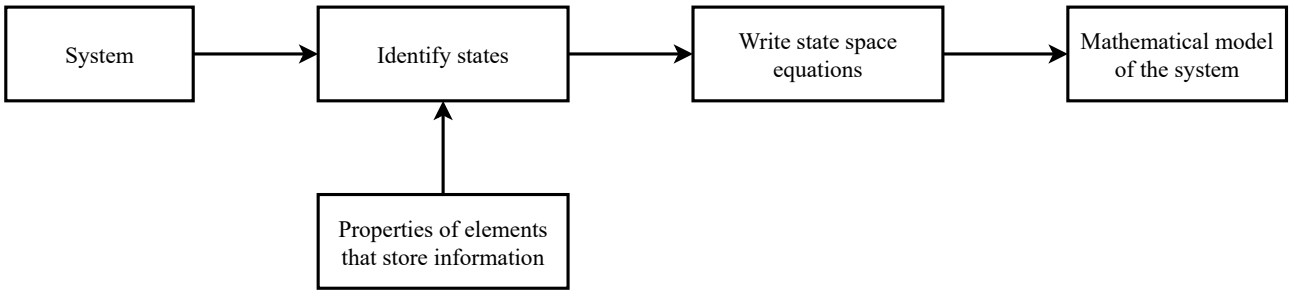


Figure 4.1: Concept of mathematical modelling

4.2.1 Assumptions

1. The switches are considered to be ideal. This means that the switching losses and the on-state resistance are not considered in the modelling process.
2. Dead-time between the semiconductor switching signals has been neglected and hence, switching occurs instantaneously.
3. The voltage across the capacitors are considered to be stable and equal in all the cells. Practically, this is not true as there is always a presence of 2^{nd} harmonic ripple present in the voltage across the capacitors. But, this can be minimized by natural selection of large DC-link capacitors.
4. The grid is considered to be rigid. As a result, the current injection by the converter does not influence the grid parameters.

4.2.2 Modelling of PSPWM

As discussed in the previous chapter, the Phase Shifted Pulse Width Modulation strategy is the best for a CHB converter. Figure 4.2 shows the scheme applied for 5-level converter. A phase shift is introduced between the carrier signals of the series connected cells, producing a phase-shifted switching pattern between them. The benefits of utilizing this strategy is its ability to uniformly distribute the power losses among the semiconductor switches.

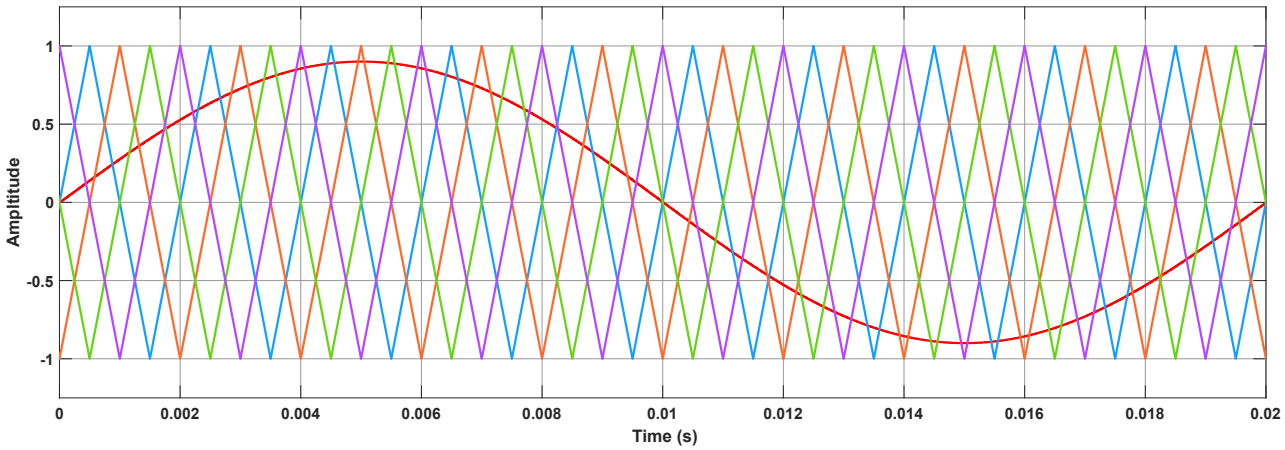


Figure 4.2: Phase shifted pulse width modulation technique for a 5-level CHB

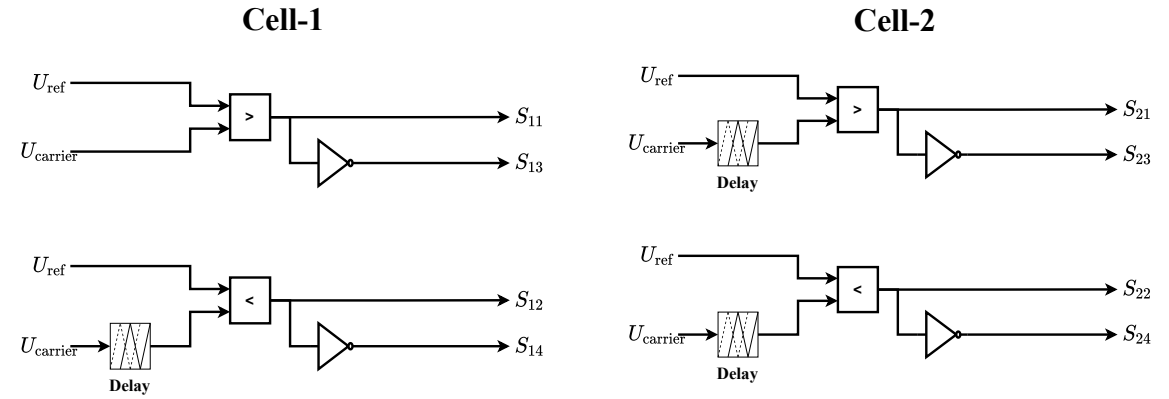
It can be noted that, the number of carrier signals required can be determined by the number of levels [11]. For a m-level CHB,

$$\boxed{N_{\text{carrier}} = m - 1} \tag{4.1}$$

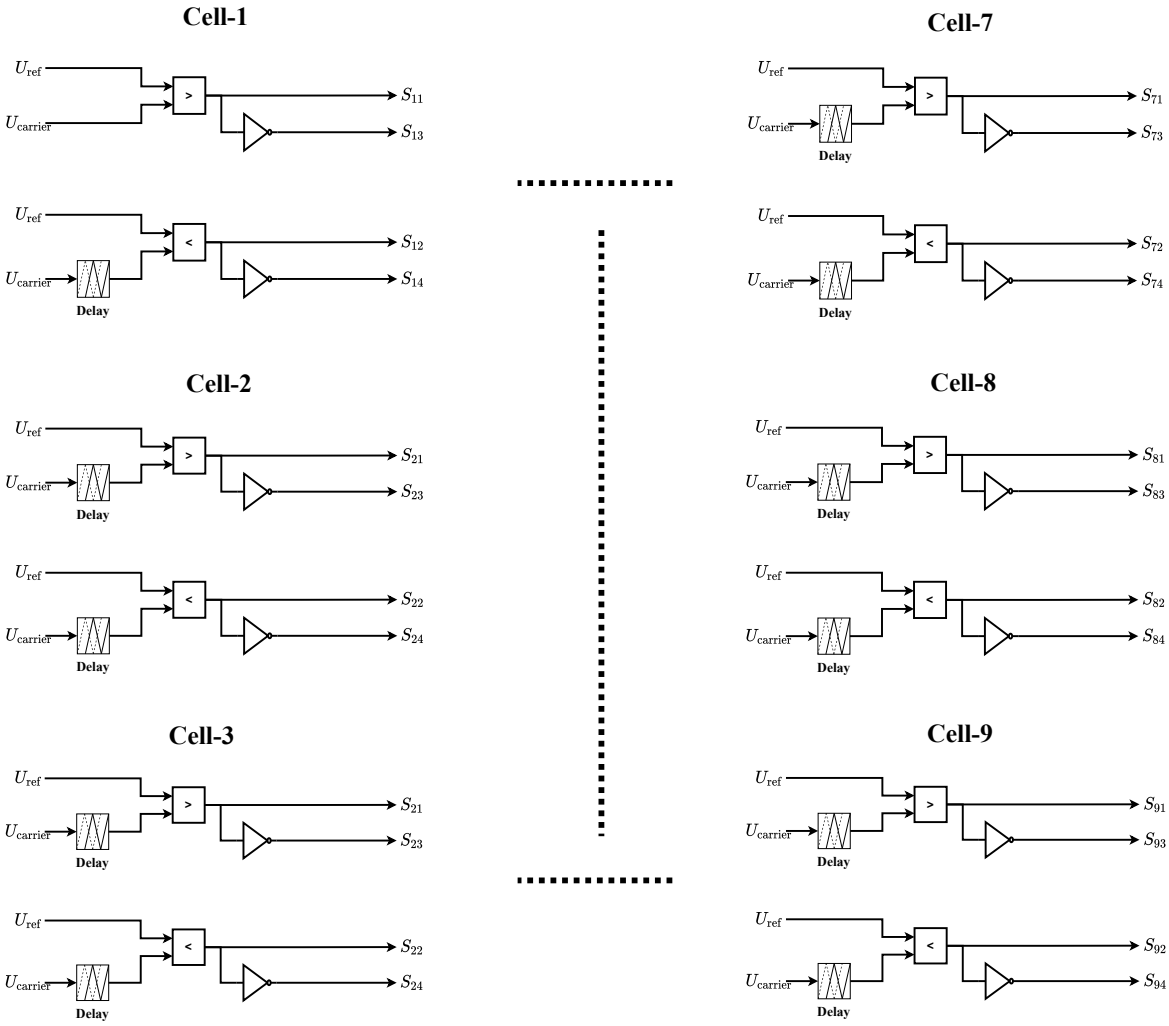
where, number of levels, $m = 2N_{\text{cell}} + 1$
The phase shift in seconds between each carrier signal can be determined as follows,

$$\boxed{T_{\text{PSPWM}} = \frac{T_{\text{sw}}}{2 \cdot N_{\text{cell}}}} \tag{4.2}$$

where, T_{sw} is the time period corresponding to the switching frequency.



(a) 5-level



(b) 19-level

Figure 4.3: Synthesis of Discrete Switching States

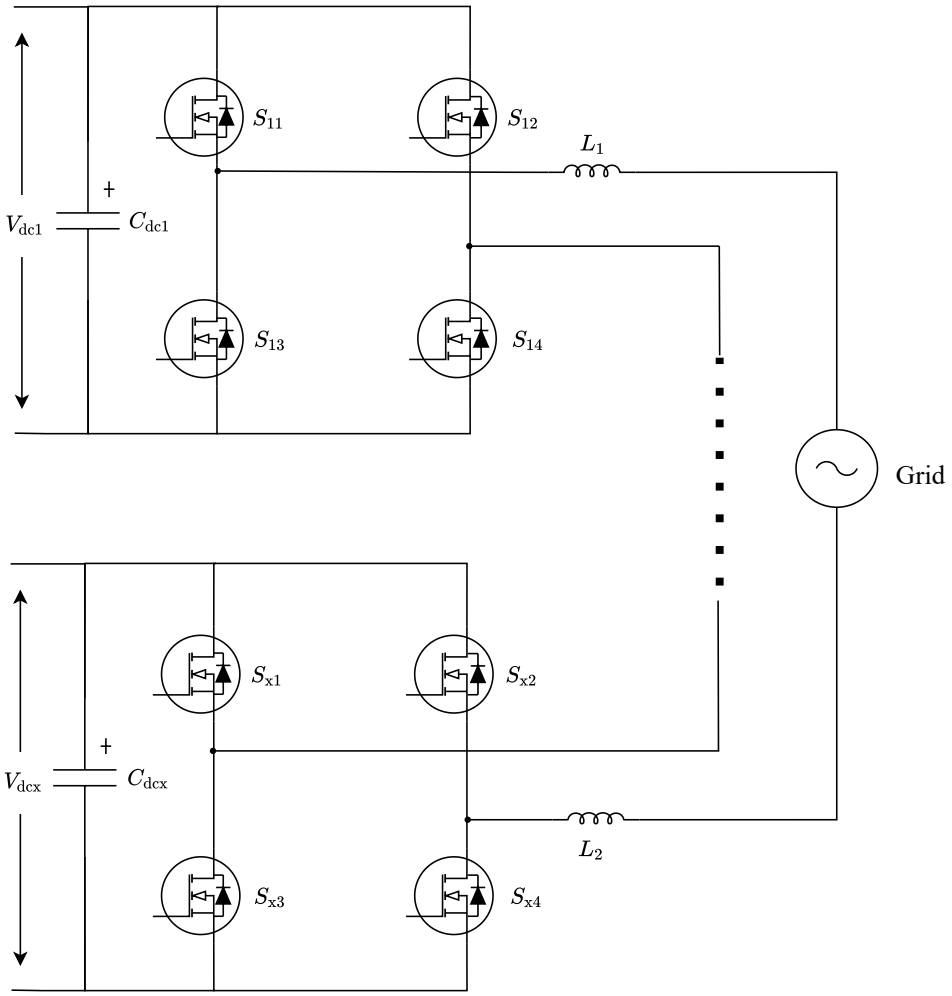


Figure 4.4: N-cell CHB Converter

Figure 4.4, shows the generalized structure of a CHB converter.
Let, x represent the cell number.
Switching states of S_{x1}, S_{x3} must be complimentary to those of S_{x2}, S_{x4} to avoid cross conduction in the H-bridge. However, these switching states hold discrete values,

$$S_{xy} = \left\{ \begin{array}{ll} 0 & , \text{OFF} \\ 1 & , \text{ON} \end{array} \right\}$$

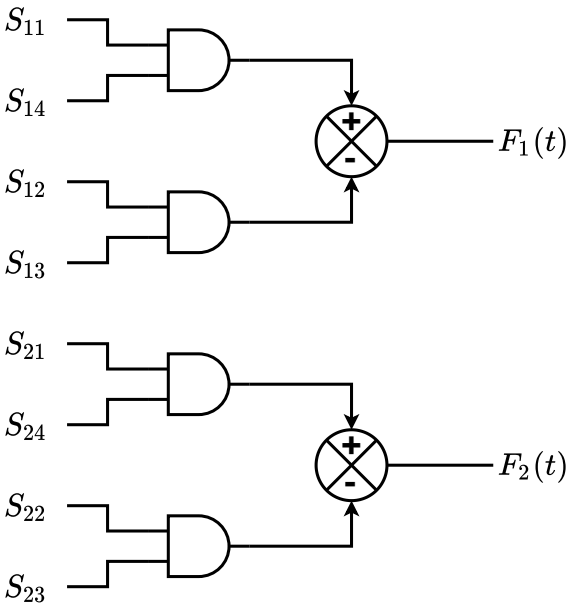
where, y = 1, 2, 3, 4.

In order to utilize a modulation technique, these discrete switching states need to be transformed into continuous switching functions. Using these switching states, generalized switching functions for a N-cell CHB can be derived as follows [45]:

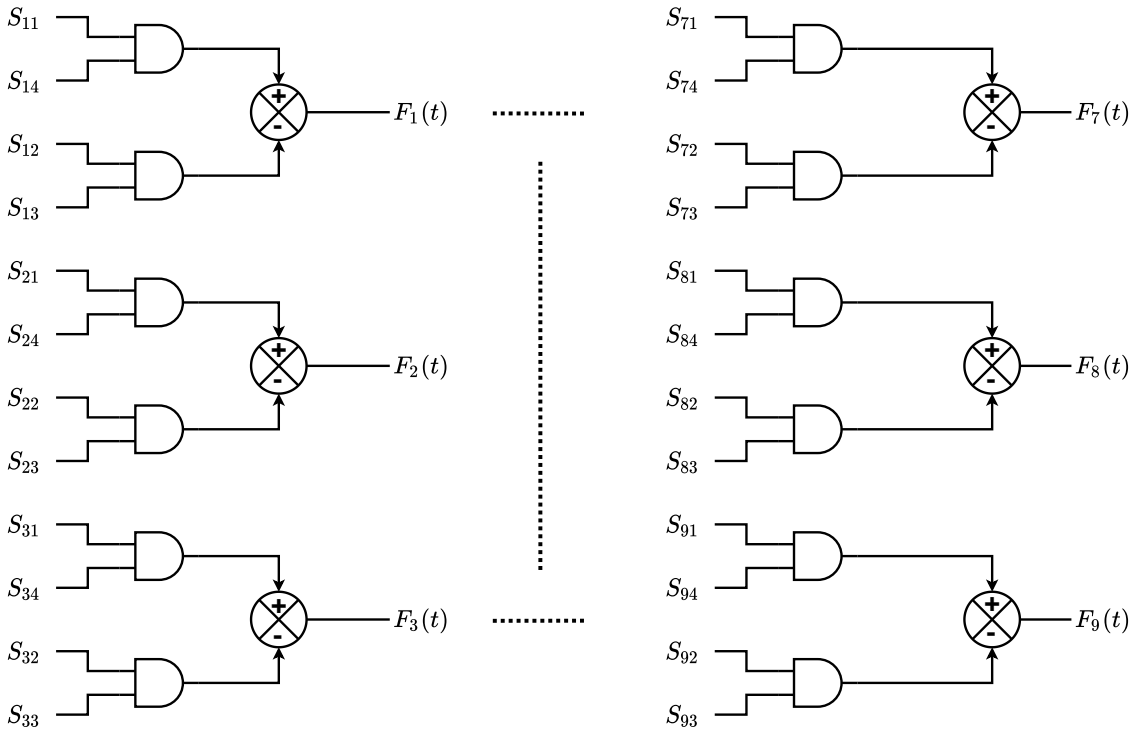
$$F_1(t) = S_{11}S_{14} - S_{12}S_{13} \tag{4.3}$$
$$F_x(t) = S_{x1}S_{x4} - S_{x2}S_{x3} \tag{4.4}$$

where,
$x \in 1, 2, 3, \ldots N_{cell}$ and,

F_x, the continuous switching function of the x^{th} cell.



(a) 5-level



(b) 19-level

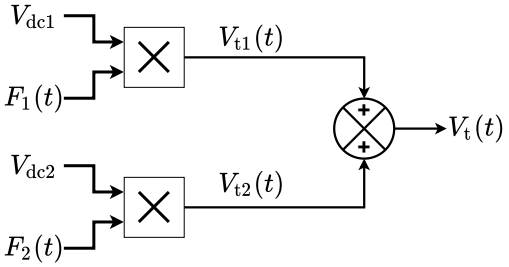
Figure 4.5: Synthesis of Continuous Switching Functions

4.2.3 CHB Model

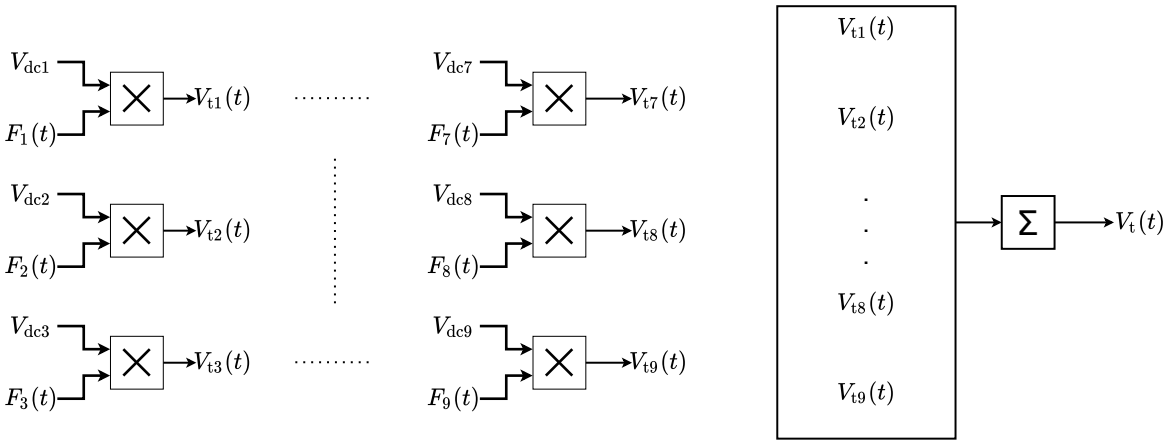
Now, in order to synthesize the terminal voltage of converter, the continuous switching functions need to be multiplied with its respective cell DC link voltage. Therefore, the terminal voltage of the converter under design can be expressed as,

$$\boxed{V_{\mathrm{t}} = \sum_{i=1}^{N_{\mathrm{cell}}} F_{\mathrm{i}}(t) \cdot V_{\mathrm{dc}i}} \tag{4.5}$$

Note, that based on the assumptions made during the beginning of the modelling process, the DC link voltages have been kept constant. Equation 4.5 can be modelled in SIMULINK as shown below:



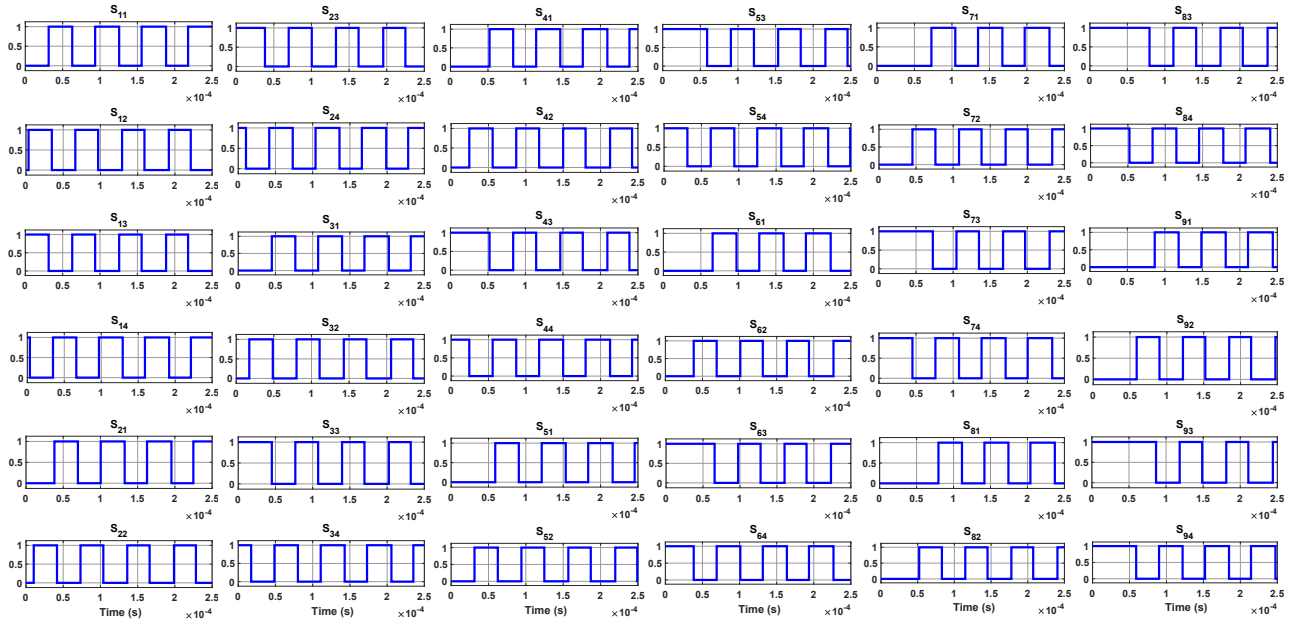
(a) 5-level CHB Model



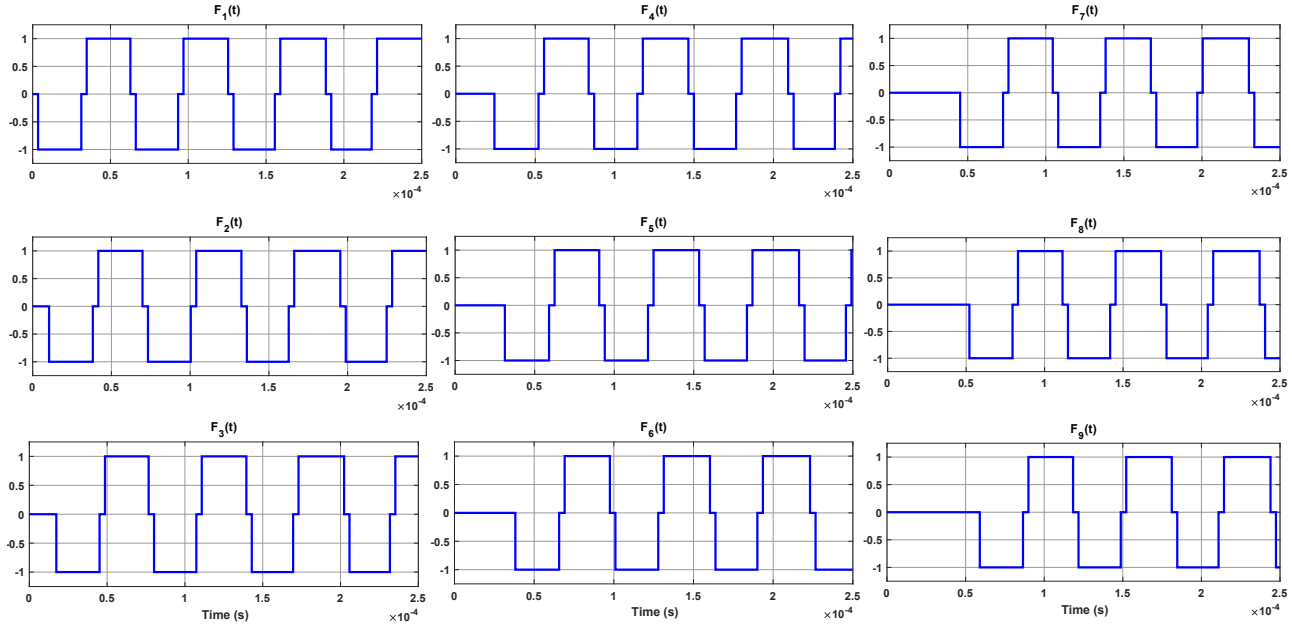
(b) 19-Level CHB Model

Figure 4.6: CHB model using continuous switching functions

4.2.4 Simulation Results of the model

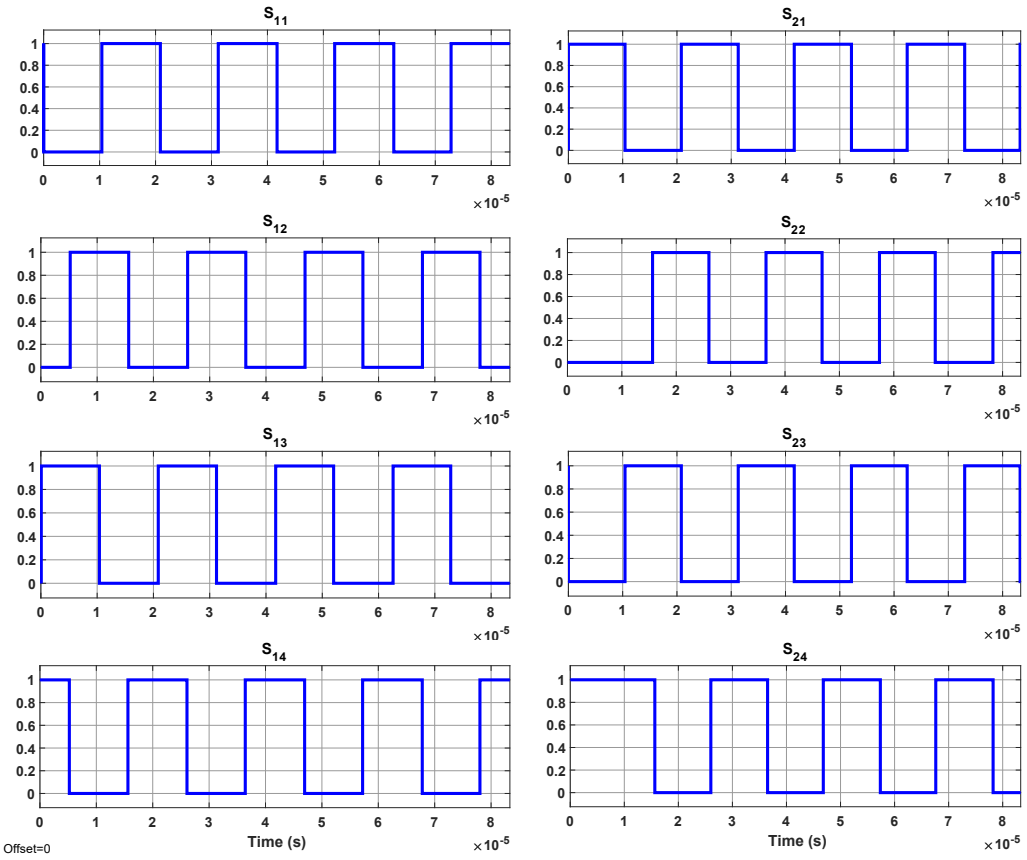


(a) Discrete Switching Functions

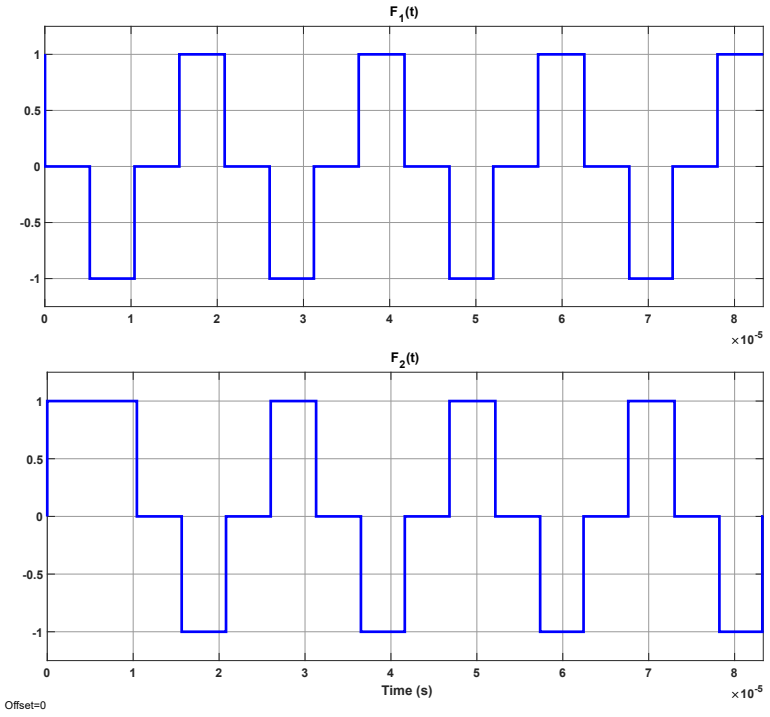


(b) Continuous Switching Functions

Figure 4.7: Simulation Results of Pulse Width Modulation Scheme for the 19-level converter, $T = 4 \cdot T_{\text{sw}}$

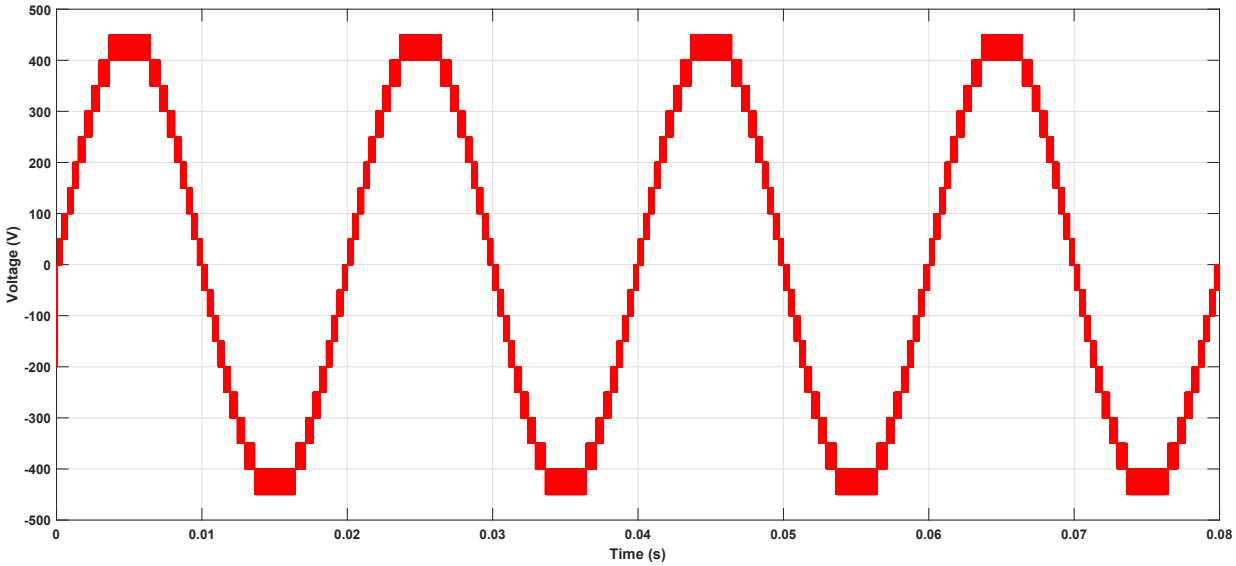


(a) Discrete Switching Functions

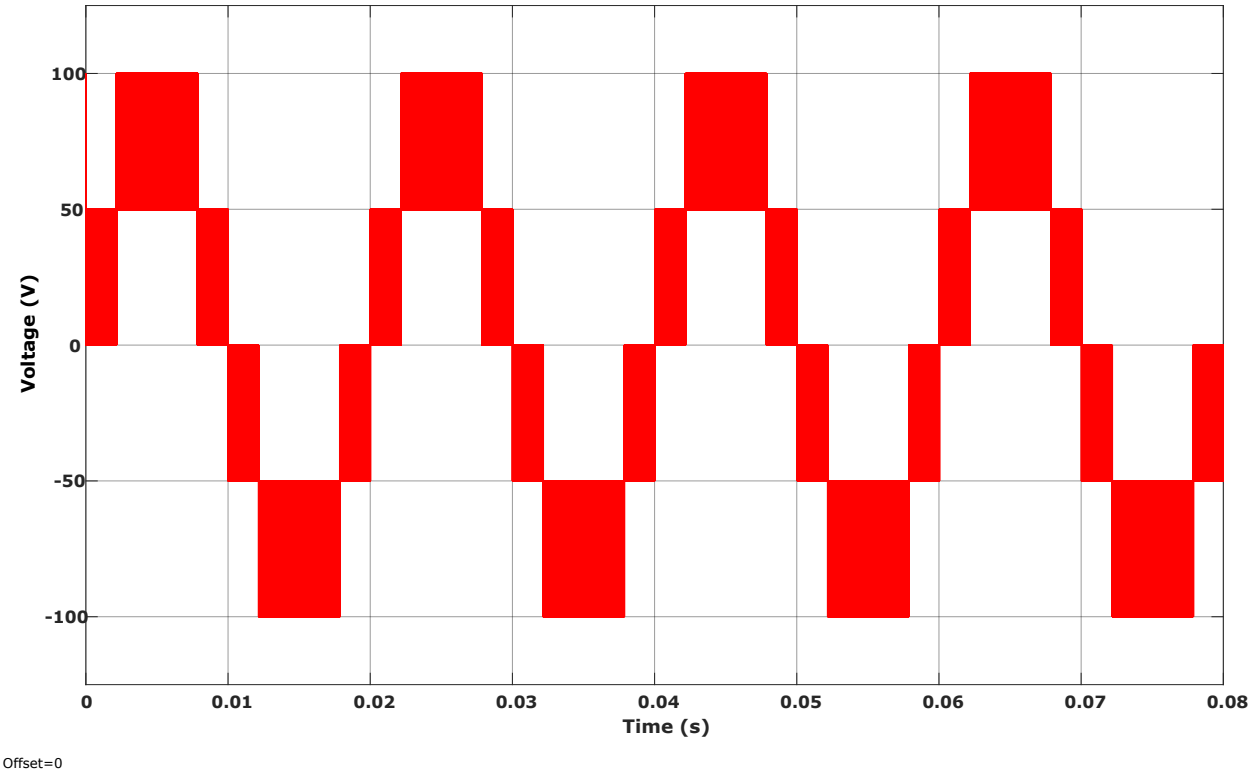


(b) Continuous Switching Functions

Figure 4.8: Simulation Results of Pulse Width Modulation Scheme for the 5-level converter, $T = 4 \cdot T_{\text{sw}}$



(a) 19-level



(b) 5-level

Figure 4.9: Terminal Voltage, $T = \frac{4}{f_g}$

4.3 Control of CHB converter

4.3.1 Control structure of CHB

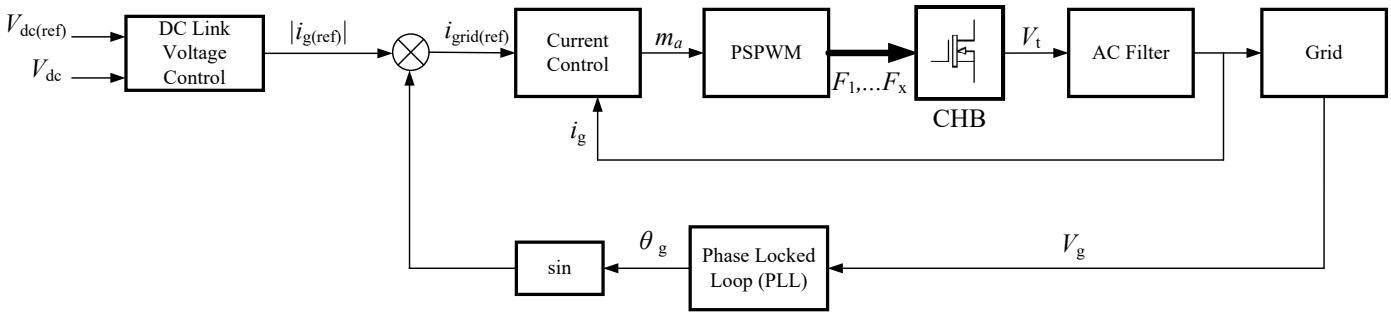


Figure 4.10: Typical control structure of voltage source converter

The control structure of a grid-connected converter is shown in Figure 4.10. It can be divided into 2 levels:

1. High level control
2. Low level control

High level control includes the DC link voltage control, reactive power control and the PLL. On the other hand, low level control consists of the current control, and the pulse width modulator. In case of PV systems, reactive power control will not be present due to unity power factor operation of the converter.

- **DC Link Voltage Control**
  The DC link voltage control can be implemented in 2 ways:
  - Generate the magnitude of the grid current reference.
  - Generate the active power reference required to be injected into the grid.

  Since the DC source in this grid connected system is a PV module, the converter can no longer control the active power. Therefore, the controller needs to be designed for generating the amplitude of the grid current reference. This means, that the controller would generate the amplitude of grid current reference such that the DC link voltage per cell remains constant.

- **Current Control**
  - The heart of the converter control system.
  - Generates the required reference modulating signal for the pulse width modulator.
  - Provides overload protection to the converter.
  - Robust against variations in parameters of the converter and the grid, superior dynamic performance, and higher control precision [38].

- **PSPWM**
  Based on the modulating signal reference generated by the current controller, the modulator generates gate signals for the semiconductor switches of the converter.

- **PLL**
  Phase Locked Loops (PLL) are an integral component of any grid connected system. It tracks the grid voltage angle and locks onto it thereby ensuring that the grid current reference always remains in phase with the grid voltage.

4.4 Current Control

4.4.1 The L filter model

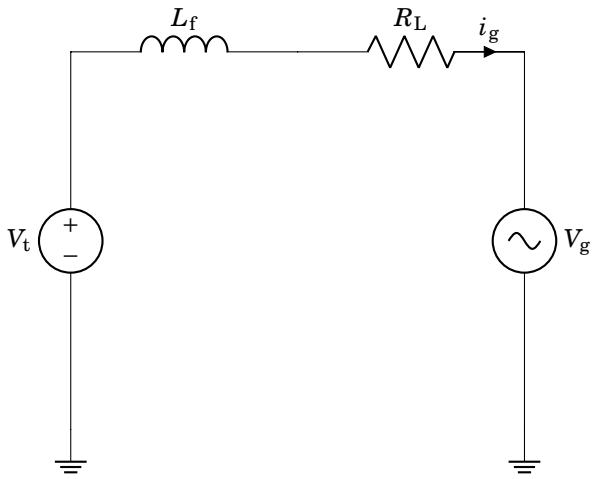


Figure 4.11: The L filter as an interface between the converter and the grid

The mathematical model for the L filter can be expressed by applying KVL on the circuit shown in Figure 4.11:

$$\boxed{V_t = V_g + L_f \frac{di_g}{dt} + i_g R_L} \tag{4.6}$$

Assuming that, $V_g = 0$, and taking the Laplace transform of Equation 4.6, the transfer function of the L filter can therefore be expressed as,

$$\boxed{\frac{i_g(s)}{V_t(s)} = \frac{1}{sL_f + R_L}} \tag{4.7}$$

4.4.2 Controller Selection

When it comes to controller selection, the Proportional Integral Derivative Controller (PID) is by far the most common controller. However, for good enough performance, a simple PI controller can also be implemented.
In this case, since the grid current needs to be controlled, the plant is basically the inductor transfer function expressed by Equation 4.7. This is a first order plant model and therefore, the implementation of a PI controller is straightforward. However, it will be observed in the forthcoming sections that a PI controller for sinusoidal reference tracking may not be the best option.

4.4.3 PI Controller

A PI controller can be represented by the following block diagram:

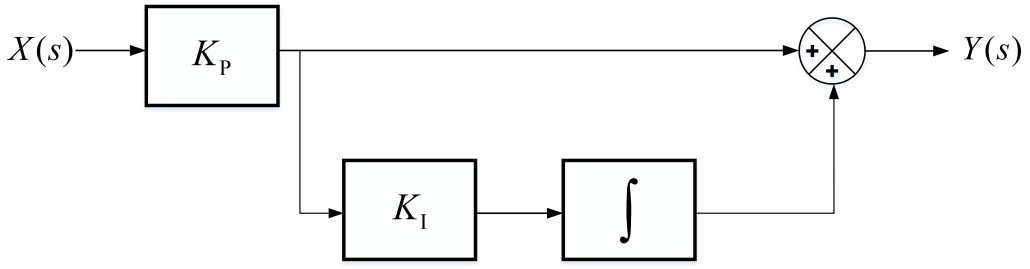


Figure 4.12: Block Diagram of PI Controller

The transfer function associated with the PI controller can be expressed as:

$$\frac{Y(s)}{X(s)} = K_{\mathrm{P}}\left(1 + \frac{K_{\mathrm{I}}}{s}\right) \tag{4.8}$$

where,
K_{P} and K_{I} are proportional and integral gains of the controller.

Plant Model

For grid current control, a simple plant model with the PI controller is shown below:

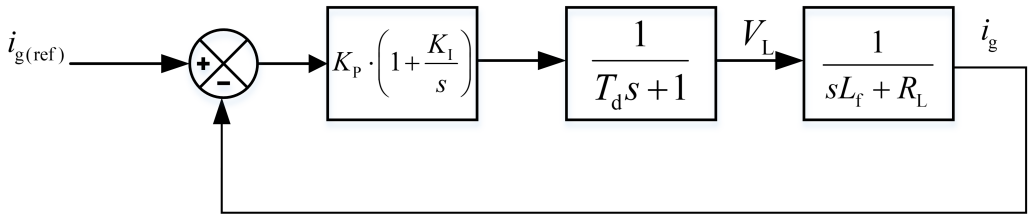


Figure 4.13: Plant model for PI controller based Grid Current Control

Controller Gains

Note, that for determination of controller gains, the controller delay has not been taken into account.
The open loop transfer function of the plant model can be expressed as :

$$G_{\mathrm{o}}(s) = K_{\mathrm{P}} \cdot \left(1 + \frac{K_{\mathrm{I}}}{s}\right) \cdot \left(\frac{1}{sL_{\mathrm{f}} + R}\right) \tag{4.9}$$

Simplifying further we have,

$$G_{\mathrm{o}}(s) = K_{\mathrm{P}} \cdot \left(\frac{s + K_{\mathrm{I}}}{s}\right) \cdot \left(\frac{1}{L_{\mathrm{f}}\left(s + \frac{R_{\mathrm{L}}}{L_{\mathrm{f}}}\right)}\right) \tag{4.10}$$

By closely having a look at Equation 4.10, we can notice that if the value of the integral gain, $K_{\mathrm{I}} = \frac{R_{\mathrm{L}}}{L_{\mathrm{f}}}$, it results in a pole-zero cancellation of the system. Equation 4.10 can be simplified to the following form,

$$\boxed{G_{\mathrm{o}}(s) = \frac{K_{\mathrm{P}}}{sL_{\mathrm{f}} + K_{\mathrm{P}}}} \tag{4.11}$$

The closed loop transfer function of the plant model can therefore be expressed as:

$$G_{\mathrm{c}}(s) = \frac{G_{\mathrm{o}}(s)}{1 + G_{\mathrm{o}}(s)} \tag{4.12}$$

$$G_{\mathrm{c}}(s) = \frac{1}{\left(\frac{L_{\mathrm{f}}}{K_{\mathrm{P}}}\right)s + 1} \tag{4.13}$$

Therefore, the controller gains for a RL circuit can be calculated as follows:

$$\boxed{K_{\mathrm{I}} = \frac{R_{\mathrm{L}}}{L_{\mathrm{f}}}} \tag{4.14}$$

$$\boxed{K_{\mathrm{P}} = L_{\mathrm{f}} \cdot \omega_{\mathrm{i}}} \tag{4.15}$$

where,
ω_{i} is the bandwidth of the controller.
As a rule of thumb, the bandwidth of the current controller should be at least 10 times smaller than the switching frequency.

4.4.4 Simulation of the PI based current controller

For this purpose, we utilize the parameters presented in Table 3.3a.

Parameters	Value
ω_{i}	3 kHz
K_{P}	7.083 Ω
K_{I}	404.25 s^{-1}
T_{d}	$1.5{\cdot}T_{\mathrm{sw}}$

Table 4.1: PI controller parameters

A sinusoidal current reference corresponding to the nominal value of current is applied and the controller response is noted.

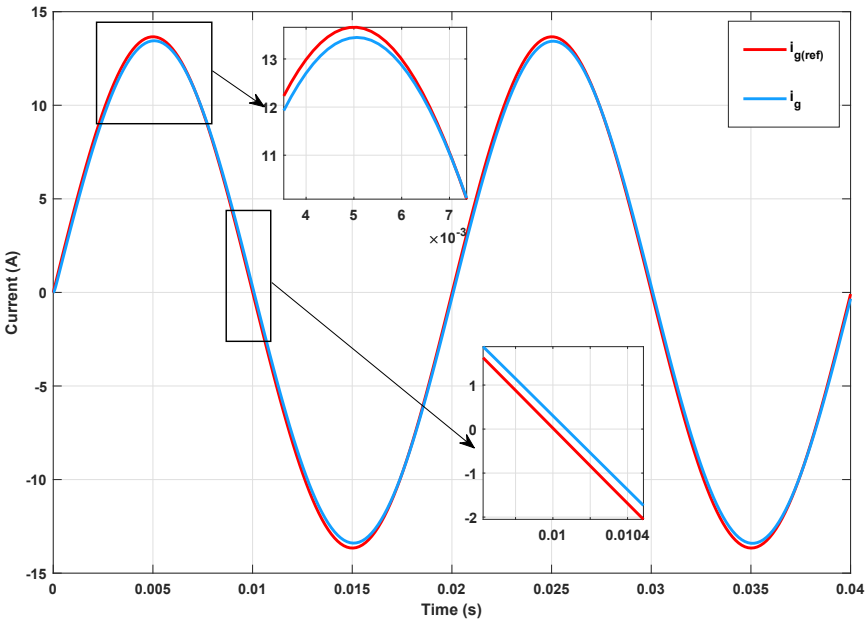


Figure 4.14: PI Controller Response

It is evident from the simulation results that the controller is not able to track the reference signal correctly and therefore, introduces amplitude and phase errors in the grid current. This is an inherent problem of the controller and therefore, is not an optimal choice for tracking sinusoidal references [38], [46].

4.4.5 PR controller

To eliminate the effects of amplitude and phase errors observed in a PI controller, a new class of controllers known as Proportional Resonant Controllers can be utilized. A PR controller delivers superior performance compared to a conventional PI controller due to the following features [47]:

- Provides very high gain at the specified resonant frequency. This is useful when tracking an AC signal of a specific frequency.
- No reference frame transformations required. A PR controller can track signals while being in the stationary reference frame thereby reducing the computational burden and control complexity compared to the conventional PI controller based algorithms especially in grid connected systems.
- The ability to track a specific resonant frequency allows a PR controller to behave as a selective harmonic compensator. This can be achieved by connecting several resonant sections in parallel, each section tuned for compensating the required harmonic order.

A PR controller can be represented by the following block diagram:

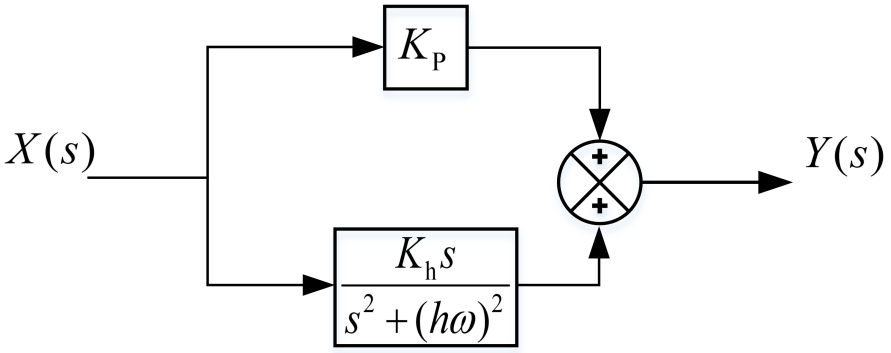


Figure 4.15: Block Diagram of PR Controller

A PR controller can be expressed by the following transfer function:

$$\frac{Y(s)}{X(s)} = K_P + \sum_{h=1}^{\infty} K_h \cdot \left(\frac{s}{s^2+(h\omega)^2}\right) \tag{4.16}$$

where,
h = order of the harmonic

Plant Model

The plant model for a PR controller based grid current control is shown below:

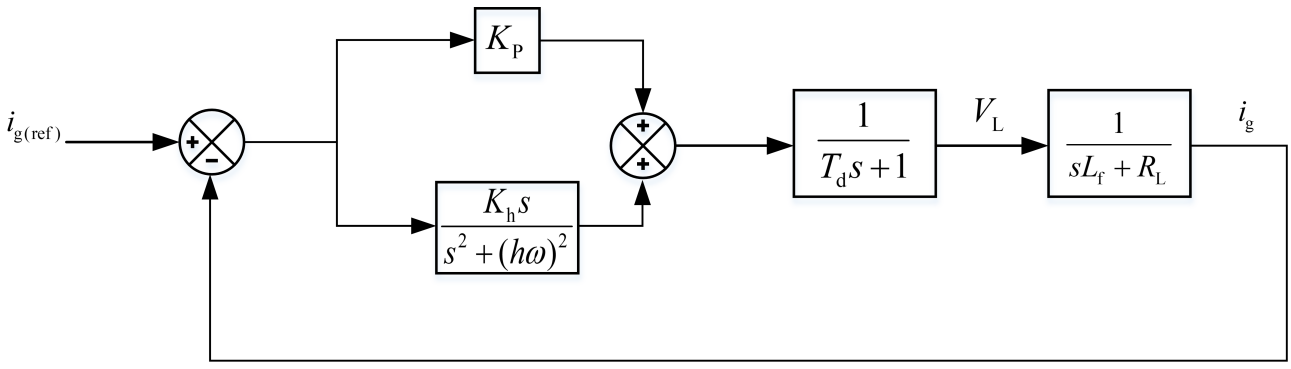


Figure 4.16: Plant model for PR controller based Grid Current Control

Controller Gains

Note, that for determination of controller gains, the controller delay has not been taken into account.
To determine the controller gains, K_P and K_h, 2 parameters need to be selected:

- Closed Loop Bandwidth.
- Resonant Bandwidth.

"The closed loop bandwidth, α_c is an important parameter, as it determines the exponential convergence rate for closed loop system transients. The total time delay, T_d is not generally negligible and hence there is an upper limit for α_c that must be observed for the closed loop system to remain stable with large enough margins" [46].

$$\boxed{\alpha_c \leq \frac{\omega_s}{10}} \tag{4.17}$$

where, $\omega_s = \frac{2\pi}{T_s}$ is the angular sampling frequency.

The resonant bandwidth, α_h [46] must be selected such that,

$$\boxed{\alpha_h < \omega_1} \tag{4.18}$$

Once, the closed loop and the resonant bandwidths have been defined, the controller gains can then be calculated [46].

$$\boxed{K_P = \alpha_c \cdot L_f} \tag{4.19}$$

$$\boxed{K_h = 2 \cdot K_P \cdot \alpha_h} \tag{4.20}$$

4.4.6 Simulation of the PR based current controller

For this purpose, we utilize the parameters presented in 3.3a. The closed loop bandwidth and resonant bandwidth chosen are as follows:

Parameters	Value
α_c	3.14 krad/s
α_h	282.74 rad/s
K_P	0.376 Ω
K_1	212.81 Ω·rad/s
T_d	$1.5 \cdot T_{sw}$

Table 4.2: PR controller parameters

A sinusoidal current reference corresponding to the nominal value of current is applied and the controller response is noted.

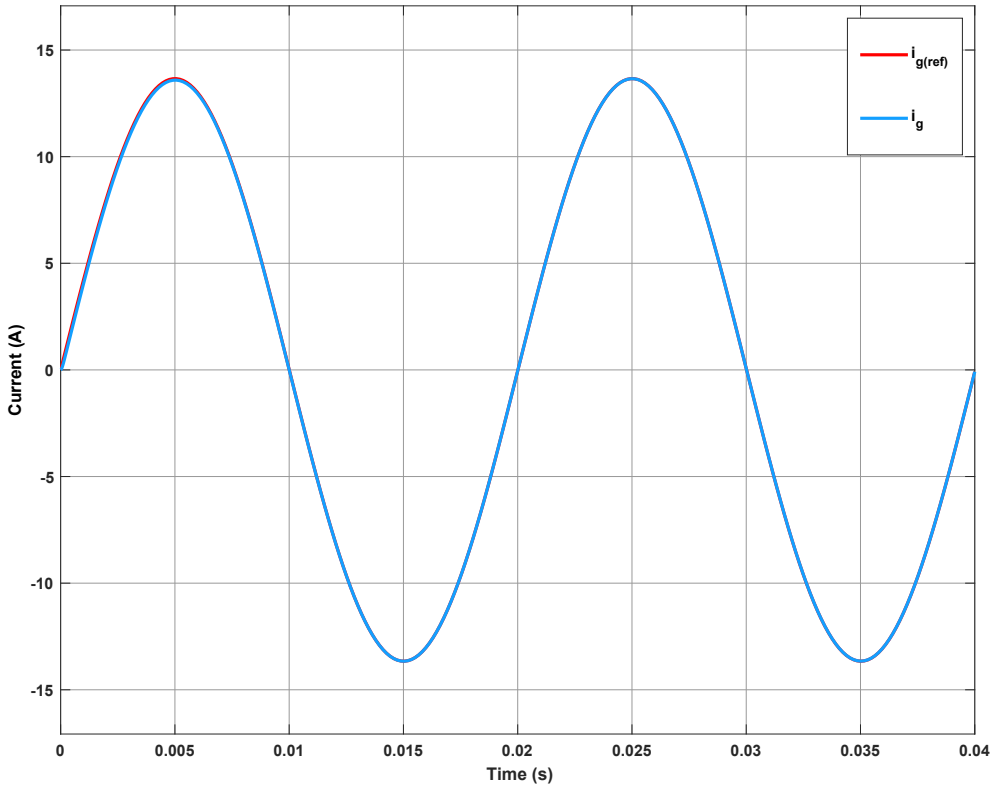


Figure 4.17: PR Controller Response

It is evident from the simulation results shown in Figure 4.17 that the PR controller is able to effectively track the sinusoidal signal with negligible amplitude and phase error. The controller is able to track the signal correctly in **less than 10 ms** which is very fast. Therefore, comparing Figure 4.14 with Figure 4.17, it is clearly noticeable that PR controller proves to be a suitable candidate for the current control in the CHB converter.

The PR controller parameters for the current control of the 5-level converter are tabulated below:

Parameters	**Value**
α_c	18.85 krad/s
α_h	282.74 rad/s
K_P	1.411 Ω
K_1	798.05 Ω·rad/s
T_d	$1.5 \cdot T_{sw}$

Table 4.3: PR controller parameters

4.5 DC Link Voltage Control

4.5.1 DC Link Mathematical Model

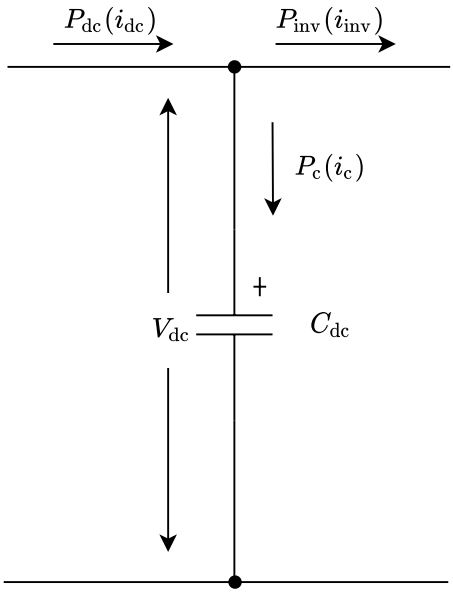


Figure 4.18: DC link model showing the power flow in a single cell as a function of current

Using power balance we have,

$$P_{dc} = P_c + P_{inv} \tag{4.21}$$

$$i_c = \frac{P_{dc} - P_{inv}}{V_{dc}}$$

$$\boxed{C_{dc}\frac{dV_{dc}}{dt} = \frac{P_{dc} - P_{inv}}{V_{dc}}} \tag{4.22}$$

$$\boxed{C_{dc}\frac{dV_{dc}}{dt} = \frac{1}{2}\cdot\left(\frac{2P_{dc} - \hat{V}_g\hat{i}_g}{V_{dc}}\right)} \tag{4.23}$$

Equation 4.22 can be used to mathematically represent the DC link in SIMULINK as shown in Figure 4.19. Note, that there is an additional gain of $\frac{1}{N}$ applied for the power injected into the grid. This means that the total power injected into the grid is contributed equally by all the cells.

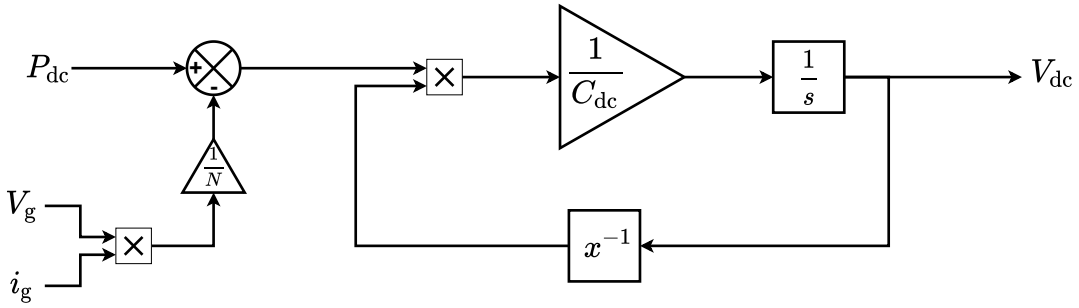


Figure 4.19: DC Link Model for a single cell

4.5.2 DC link Plant Model

Equation 4.23 indicates that the model of the DC link is non-linear. In order to linearize the model, the Taylor series expansion is used. The non-linear model described in Equation 4.23 needs to be linearized around equilibrium points. In this case, the equilibrium points are the reference DC link voltage and the nominal current.

$$C_{\mathrm{dc}}\frac{\mathrm{dV_{dc}}}{\mathrm{d}t} = f(V_{\mathrm{dc}}, \hat{i}_{\mathrm{g}}) \tag{4.24}$$

$$C_{\mathrm{dc}}\frac{\mathrm{dV_{dc}}}{\mathrm{d}t} = \Delta V_{\mathrm{dc}}\left(\frac{\partial f}{\partial V_{\mathrm{dc}}}\right)\Bigg|_{\hat{i}_{\mathrm{g}}=\hat{i}_{\mathrm{g}}} + \Delta\hat{i}_{\mathrm{g}}\left(\frac{\partial f}{\partial \hat{i}_{\mathrm{g}}}\right)\Bigg|_{V_{\mathrm{dc}}=V_{\mathrm{dc}}} \tag{4.25}$$

$$C_{\mathrm{dc}}\frac{\mathrm{dV_{dc}}}{\mathrm{d}t} = \underbrace{-\frac{1}{2}\cdot\left(\frac{2P_{\mathrm{dc}} - \hat{V}_{\mathrm{g}}\hat{i}_{\mathrm{g}}}{V_{\mathrm{dc}}^2}\right)\cdot\Delta V_{\mathrm{dc}}}_{\text{Higher Order Terms}} - \frac{1}{2}\left(\frac{\hat{V}_{\mathrm{g}}}{V_{\mathrm{dc}}}\right)\cdot\Delta\hat{i}_{\mathrm{g}} \tag{4.26}$$

Neglecting the higher order terms we have the linearized model of the DC link,

$$\boxed{C_{\mathrm{dc}}\frac{\mathrm{dV_{dc}}}{\mathrm{d}t} = -\frac{1}{2}\left(\frac{\hat{V}_{\mathrm{g}}}{V_{\mathrm{dc}}}\right)\cdot\Delta\hat{i}_{\mathrm{g}}} \tag{4.27}$$

Taking Laplace transform on both sides of Equation 4.27 we have,

$$sC_{\mathrm{dc}}V_{\mathrm{dc}}(s) = -\frac{1}{2}\left(\frac{\hat{V}_{\mathrm{g}}}{V_{\mathrm{dc}}}\right)\cdot\Delta\hat{i}_{\mathrm{g}}(s)$$

$$\boxed{\frac{V_{\mathrm{dc}}(s)}{\hat{i}_{\mathrm{g}}(s)} = -\frac{1}{2}\left(\frac{\hat{V}_{\mathrm{g}}}{sC_{\mathrm{dc}}V_{\mathrm{dc}}}\right)} \tag{4.28}$$

4.5.3 Controller Tuning

A simple PI controller has been utilized for the control of the DC link voltage. The plant model for the PI based DC link voltage control is illustrated below:

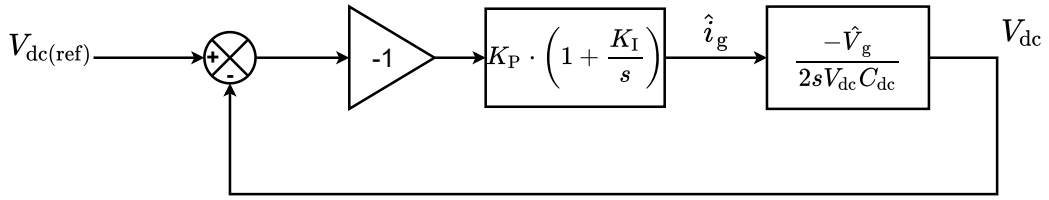


Figure 4.20: PI based DC link Voltage controller

To avoid the influence of current controller, the bandwidth of the voltage controller must be at least 10 times smaller than the bandwidth of the current controller. For this design, a sufficient margin has been alloted and the bandwidth of the voltage controller was chosen to be 60 rad/s.
To identify the controller gains, the **PID Tuner** feature of MATLAB has been utilized. The controller parameters are tabulated below:

Parameters	Value
ω_{v}	60 rad/s
K_{Pv}	0.483
K_{Iv}	7.367
T_{d}	$1.5{\cdot}T_{\mathrm{sw}}$
ϕ_{m}	83°

Table 4.4: DC link voltage controller parameters

4.5.4 Simulation Results

A step reference of 50 V with a step time of 1 ms is applied to the plant model for tuning the PI controller.

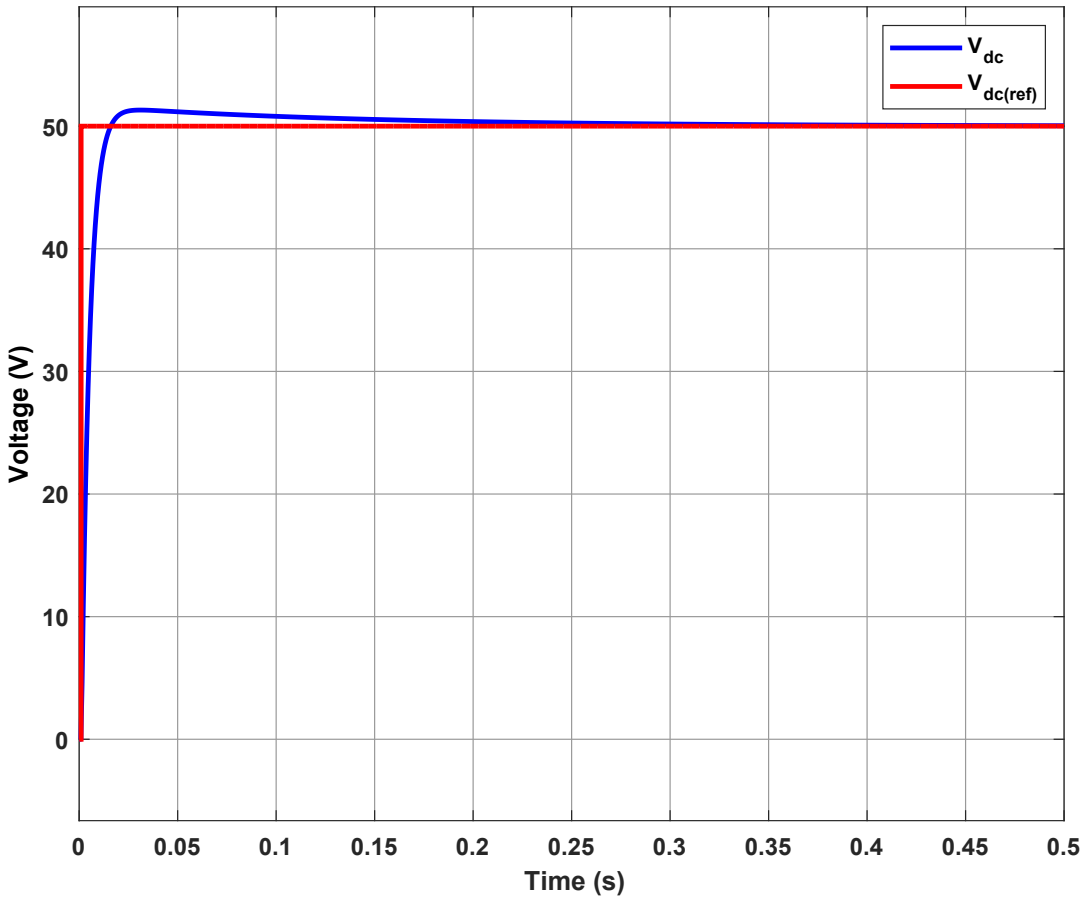


Figure 4.21: DC Link Voltage Controller Plant Response

It is evident from the plant response, that the controller gains are tuned correctly with sufficient phase margin.

4.6 Significance of Digital Control

Power electronics and digital control theory have a very strong relationship. The application of digital control techniques to power electronic converters has always been considered very intriguing. Digital controllers offer several advantages [48]:

- Advanced control laws can be implemented. This is difficult or impossible to implement analogically.
- Exhibits inherent flexibility. Allows the designer to redesign the control strategy without making significant modifications in the hardware.
- Resistant towards signal noise.
- Complete absence of aging effects or thermal drifts.

4.7 Zero-Order Hold

A zero order hold or ZOH is essentially a digital to analog converter (DAC) which converts a signal sampled at a particular frequency to its equivalent continuous domain signal by holding the value of the latest sample. Figure 4.22 illustrates the working principle of the ZOH.

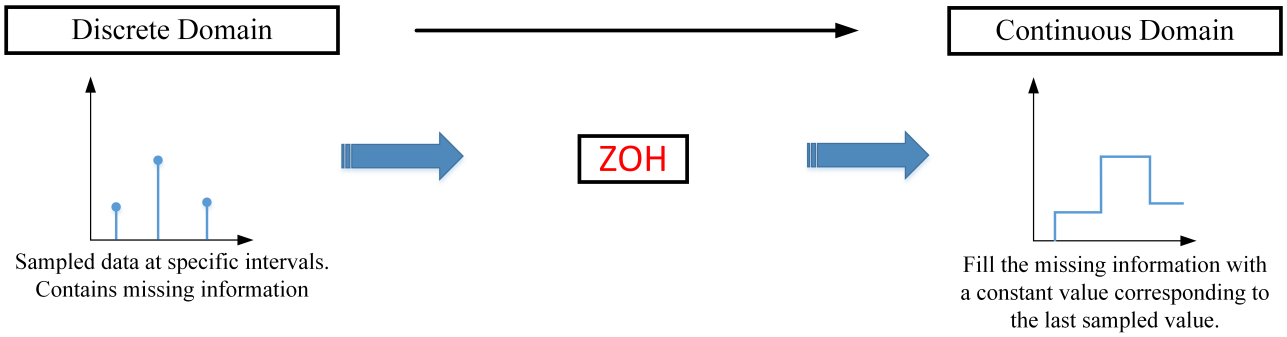


Figure 4.22: Principle of Zero Order Hold

To illustrate the difference between a continuous signal and a ZOH signal, Consider, the following transfer function,

$$G(s) = \frac{1}{(s+1)}$$

To convert a continuous transfer function into a discrete transfer function, the MATLAB command "**c2d**" is used. The discretization method is set to ZOH with a sampling frequency of 10 Hz. The corresponding discrete transfer function obtained as a consequence of applying the ZOH method is expressed as,

$$G(z) = \frac{0.09516}{(z-0.9048)}$$

The step response of this transfer function as well as its continuous variant is plotted.

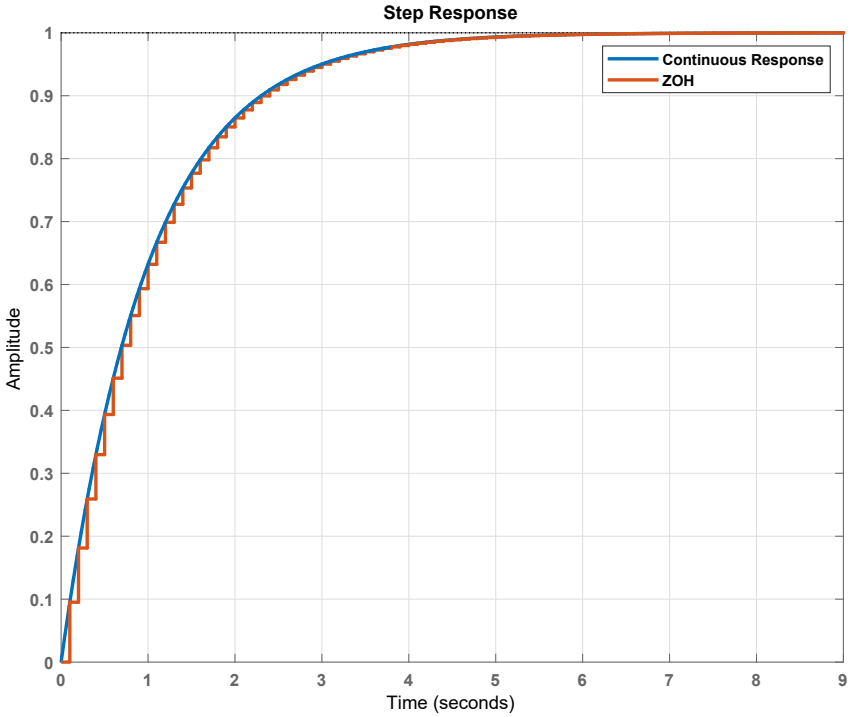


Figure 4.23: Step-response for $G(s)$ & $G(z)$

It is evident from the step response that the ZOH response closely follows the continuous response. The instant at which the ZOH touches the continuous response corresponds to the instant at which the next sampled value was found in the discrete domain.
Plant models illustrated in Figures 4.16, 4.20 have been discretized with the help of "**Model Discretizer**". This is a feature in MATLAB, that detects all continuous time blocks, and converts them into discrete blocks sampled at the user specified sampling frequency as well as discretization method.

4.7.1 Performance Comparison

Figures 4.24 and 4.25 show the comparison of the discretized plant models with their continuous variant.

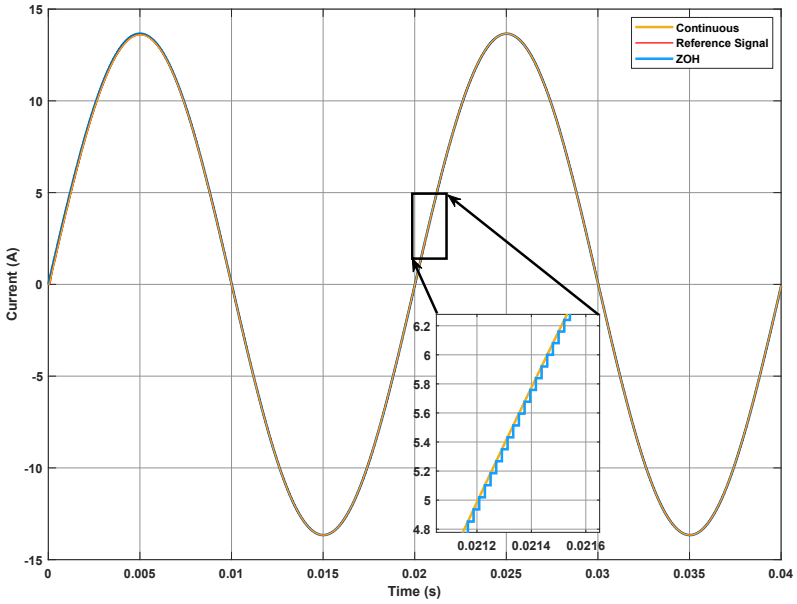


Figure 4.24: Current Controller Performance

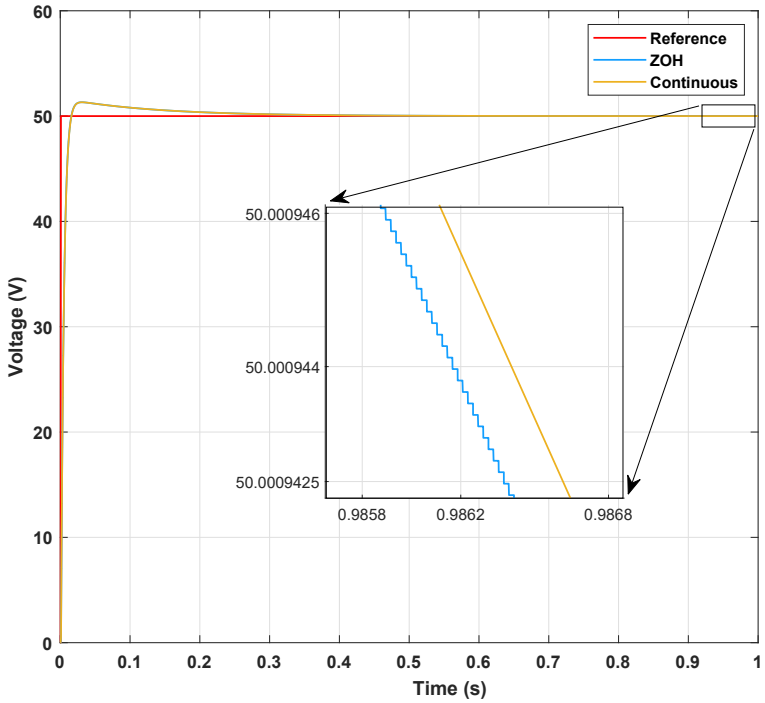


Figure 4.25: DC Link Voltage Controller Performance

Observations

- By comparing the controller responses, it is evident that the zero-order hold discretization method is able to effectively produce the corresponding continuous signal in the form of a stair-case.
- It can be noted from both, digital current and voltage controller that, discretization leads to loss of information. Accuracy of the controller can be increased by increasing the sampling frequency, however, this requires more processing power by the micro-controller/DSP. On the other hand, a smaller sampling frequency reduces computing power, however, leads to inaccuracies.
- Digital controllers introduce delay. This reduces the upper limit of the controller bandwidth. Since, the bandwidths selected for this design do not lie in the neighborhood of this upper limit, there was no need of altering the controller gains.

4.8 Conclusion

In this chapter, the modelling of the converter components as well as the design of control system has been carried out. Guidelines for tuning the current controllers as well as the difference in response between the PI and the PR controller have been illustrated. The DC link model was developed which was followed by the tuning of the DC link voltage controller using PID tuner feature of MATLAB. Significance of digital control as well as synthesis of discretized plant models for both the controllers with the help of ZOH has been discussed along with performance comparisons.

Chapter 5

Simulation Results

5.1 Introduction

In the previous chapter, the mathematical model as well as the design of the control system for the CHB was carried out. In this chapter, all the subsystems of the simulation model are connected together to form the complete grid connected CHB simulation model and the response is studied. Before, testing the complete model, it is important to ensure that the control system is functioning normally. Therefore, testing of all the controllers is carried out first. This is done in a systematic manner. Once, all the controllers are confirmed to work properly, the next step would be to check the response of the system for unity power factor operation.

5.2 The Complete System

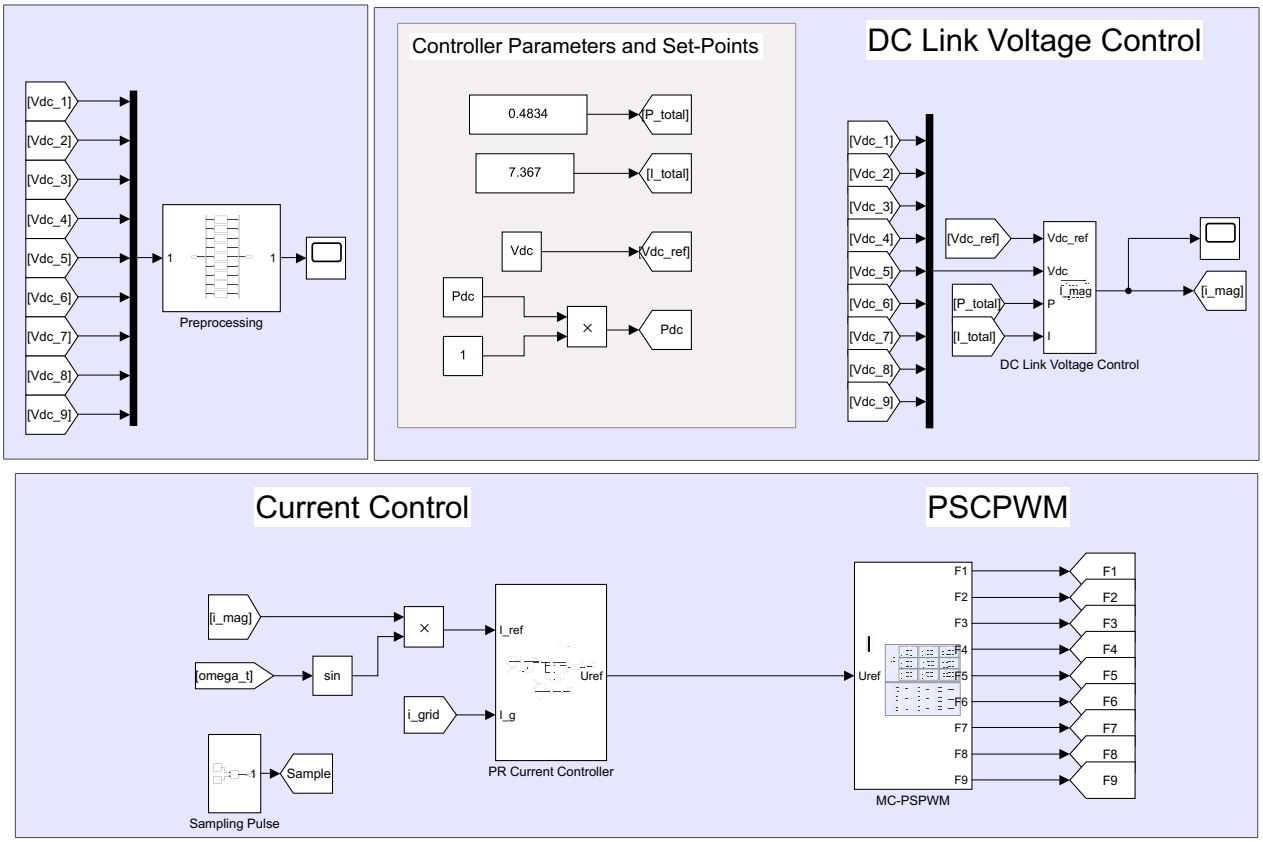


Figure 5.1: Control System of the 19-level Converter

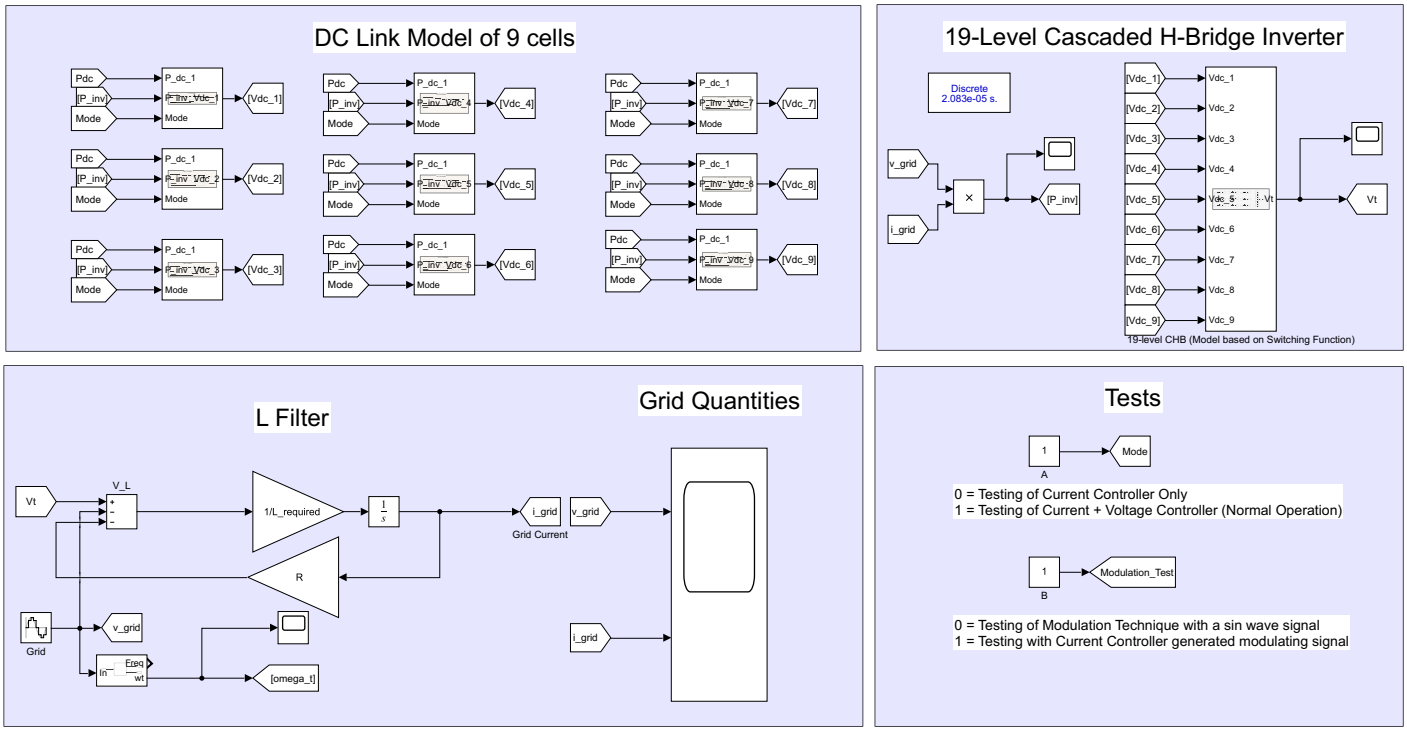


Figure 5.2: 19-level Converter

5.2.1 Additional Changes

1. **Testing**
   In Figures 5.2, a testing functionality for the simulation model has been implemented. This is implemented so as to make the testing procedure simple and without modifying the system.

   Table 5.1 explains the modes of testing for different values of variables "**A**" and "**B**":

A	B	Mode of Operation
0	1	Testing of current controller with a defined sinusoidal reference and DC link voltage.
1	1	Testing of both DC link and current controller (Normal Operation).
0	0	Testing of the Modulation scheme (Open Loop Testing).

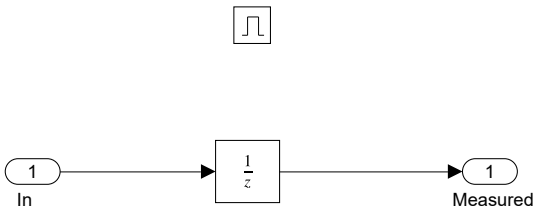
   Table 5.1: Different modes of testing available

2. **Measurement of DC link voltage**
   As stated in Chapter 4, the capacitor voltages per cell are never constant but, contain a 2^{nd} harmonic component of the fundamental frequency. The presence of this component in DC link voltage may cause the DC link controller to operate incorrectly. Thus, it is important to reject this component for measurement purposes.
   To achieve this, a filter is designed to specifically suppress only the 2^{nd} harmonic component of the DC link voltage. The generalized transfer function for the filter can be expressed as follows:

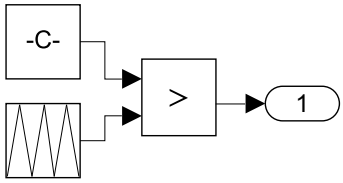
$$\frac{V_{dc(meas)}(s)}{V_{dc}(s)} = \frac{s^2 + (h\omega_1)^2}{s^2 + 2h\omega_1 + (h\omega_1)^2} \tag{5.1}$$

It will be realized in the forthcoming chapter that there is a significant difference in the measured DC link voltage with and without this filter.

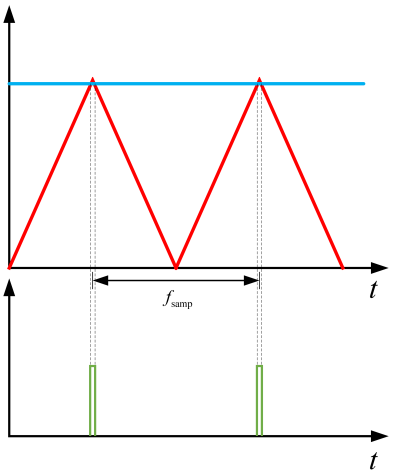
3. **DC Link Voltage and Grid Current Measurement Subsystems**



(a) Sampler



(b) Logic for triggering the sampler



(c) Generation of triggers for the measurement subsystem

Figure 5.3: Measurement of DC link voltage and grid current

Figure 5.3a shows a triggered sampler that can be used for measurement of DC link voltage and grid current. It utilizes a unit delay which operates on the same principle as ZOH however, operates only in the discrete domain.

This sampler is triggered based on the logic developed in Figure 5.3b and 5.3c. The grid current contains ripples which have a triangular shape. Therefore, to obtain the instantaneous value of the current, it is important to ensure that the sampling occurs as close as possible at the mid-point of this triangle, i.e. the peak of the triangle. After sampling, the unit delay holds the value until, the next peak is encountered and the process is repeated.

5.3 Current Controller

5.3.1 Testing of current controller

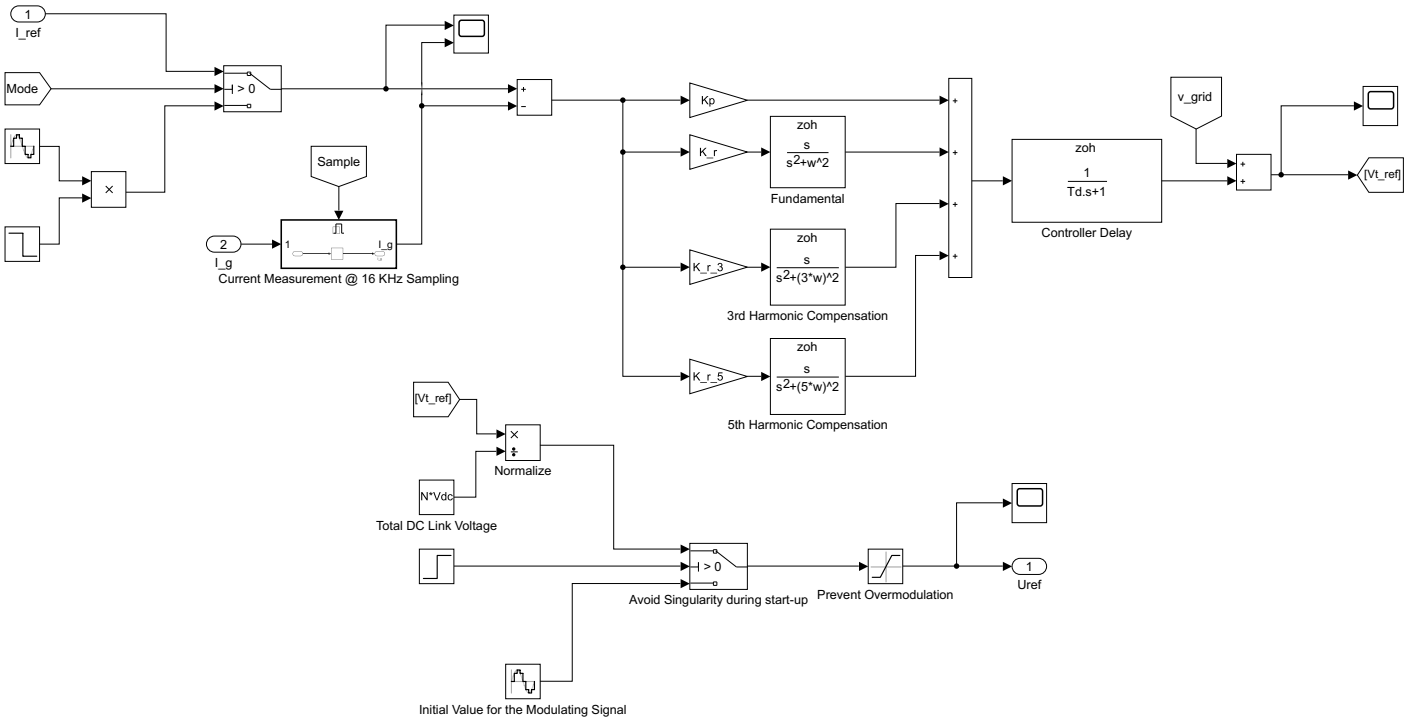


Figure 5.4: Current Controller

- In order to test the current controller only, the variables "A" and "B" are modified according to Table 5.1.

- A constant DC link voltage is applied to the converter and a pre-defined sinusoidal reference corresponding to the nominal current is applied to the controller. The simulation period is **0.1 s**.
- The controller shown in Figure 5.4 includes 2 additional resonant components for compensating the 3^{rd}, and 5^{th} harmonics. The significance of this compensation will be explained in the forthcoming sections.
- Moreover, an additional logic has been added at the end of the controller. This is provided so as to avoid singularity errors in the simulation during start-up. During start-up, a pre-defined reference modulating signal having a very small amplitude is provided for a period of 0.1 ms, after which, the current controller takes over.

5.3.2 Simulation Results

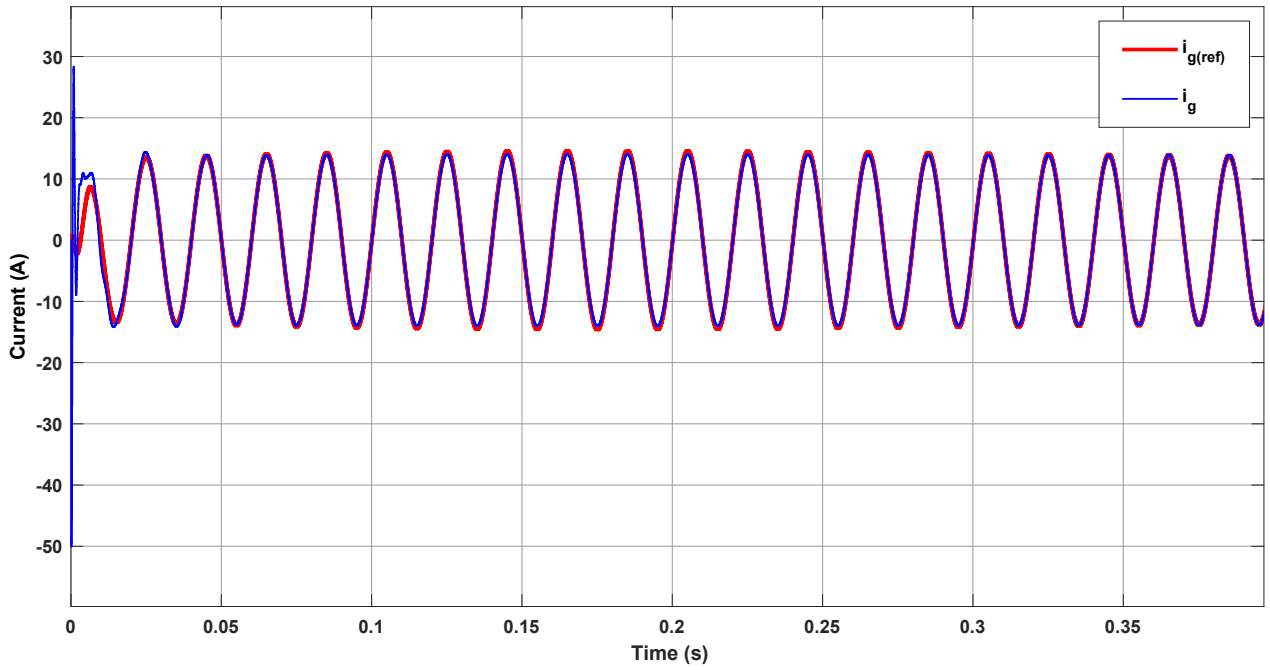


Figure 5.5: Response of the current controller

Observations

- From Figure 5.5, it is evident that the current controller has been tuned correctly.
- The controller is able to track the reference signal in approximately 2 cycles of the fundamental frequency.

5.4 Testing of the DC Link Voltage Controller

In order to test the DC link voltage controller, the variables "A" and "B" are modified according to Table 5.1. In this test, DC link voltage reference per cell is set to 50 V. The DC link voltage controller is shown below:

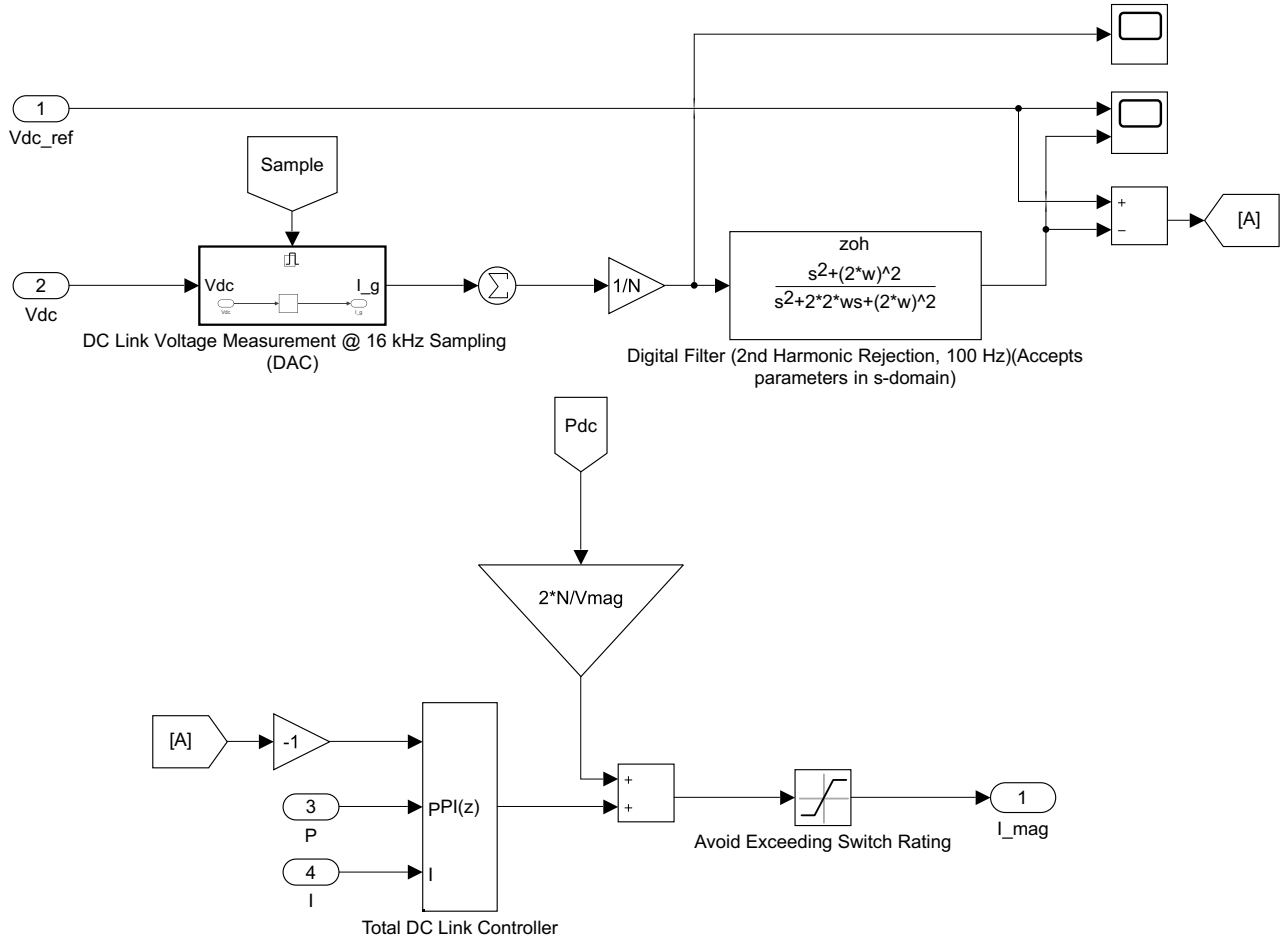


Figure 5.6: DC Link Voltage Controller

As can be observed in the controller structure, the DC link voltages per cell are measured at a sampling frequency of 16 kHz, followed by computing the average DC link voltage. In the previous chapter, it was mentioned that the measured DC link voltage will be passed through a 2^{nd} harmonic rejection digital filter. This is an important component for the measurement and can be justified by the responses shown in Figure 5.7.

5.4.1 Simulation Results

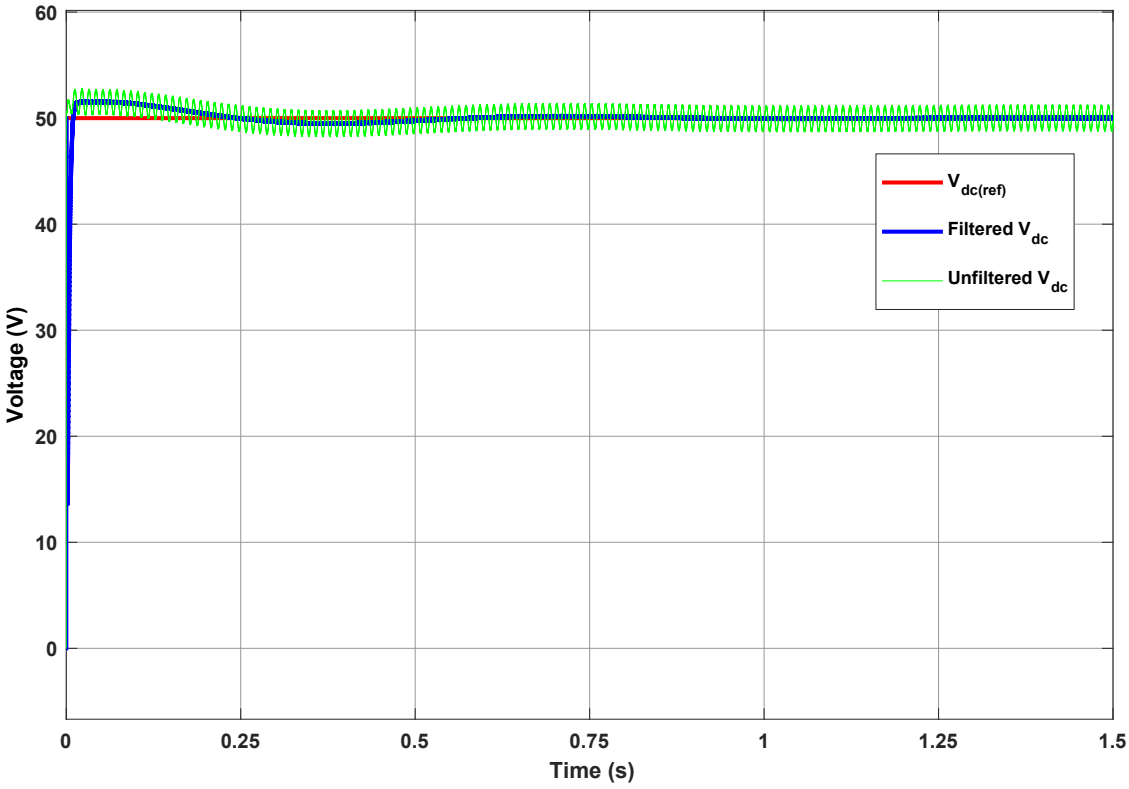


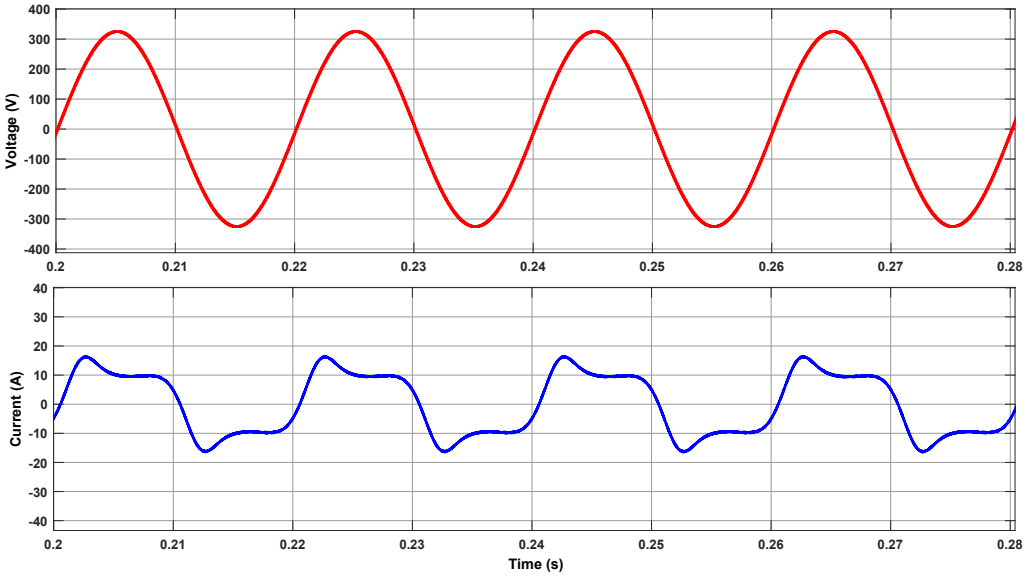
Figure 5.7: Significance of implementing a harmonic rejection filter for DC link voltage measurement

- It is evident from Figure 5.7, that the measurement of DC link voltage with the filter is superior compared to the measurement without it.
- The addition of filter allows a smoother DC link voltage response which is essential for the controller to converge to the required magnitude of the grid current as well as have a minimum distortion in the grid current.

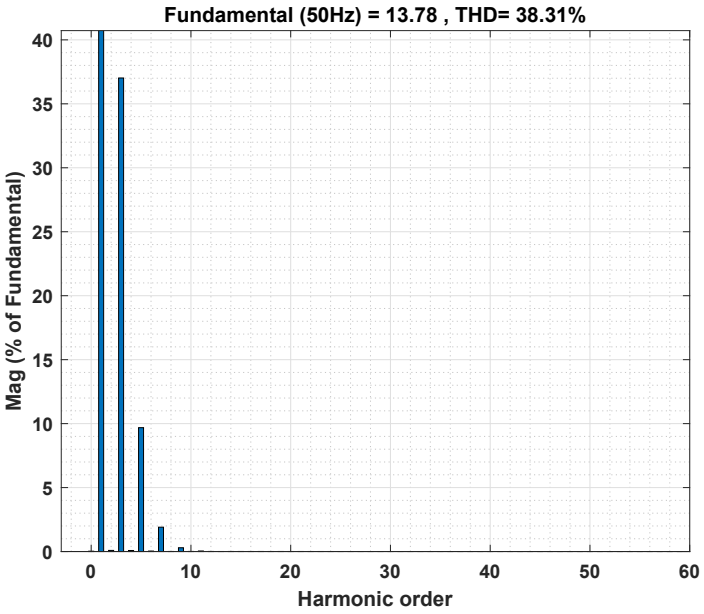
5.5 Nominal Operation

5.5.1 Without Harmonic Compensation

Now, that both the DC link voltage controller and PR current controller have been tested and verified. The converter is ready for its nominal operation. Since, the converter is used for integrating a PV system with the grid, the converter can only operate at unity power factor.
During nominal operation, the grid currents and voltage are noted along with its harmonic performance. Figure 5.8 shows the response of the converter with a standard PR current controller.



(a) Grid Voltage and Current



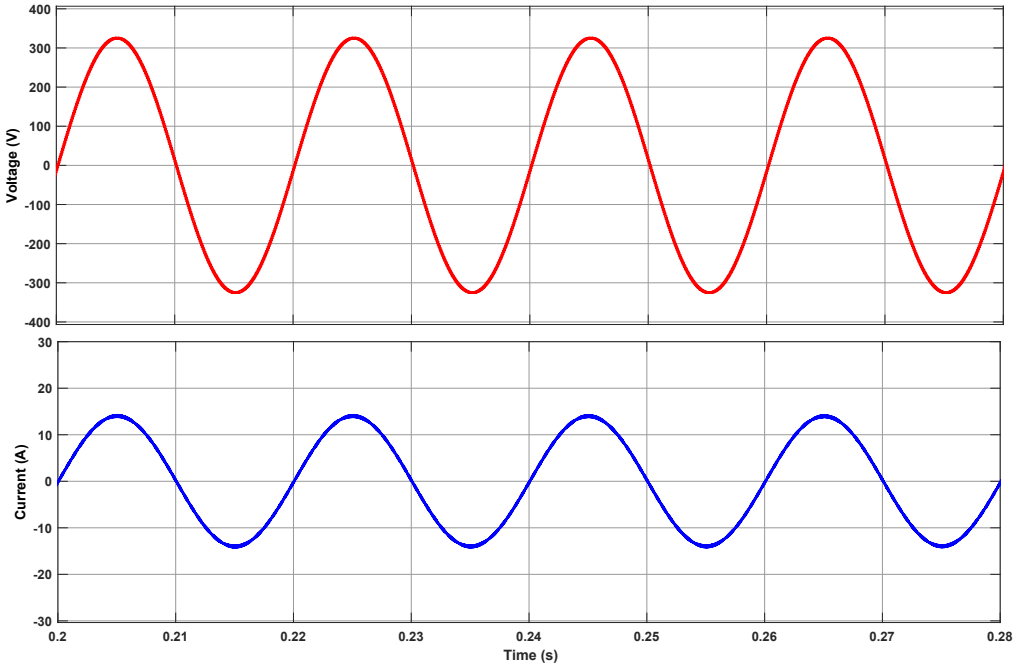
(b) THD of grid current

Figure 5.8: Harmonic performance of the converter without 3^{rd} & 5^{th} harmonic compensation

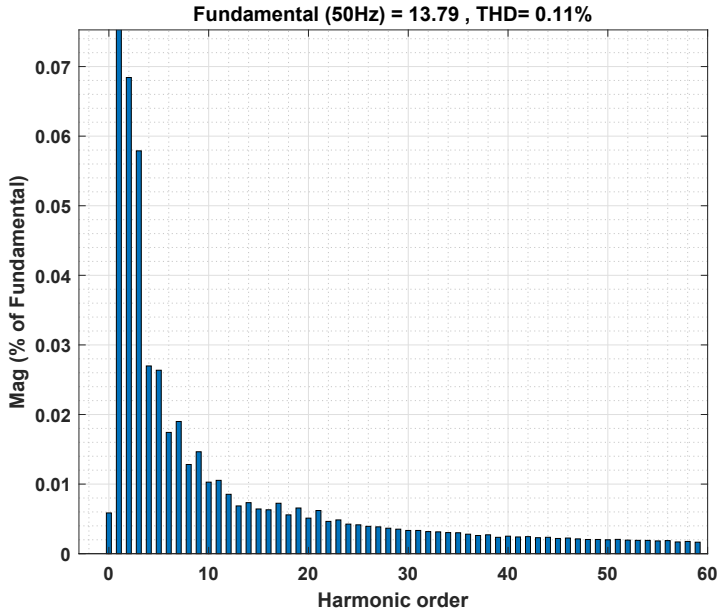
In Figure 5.8b, the FFT analysis of the grid current is shown, the THD of the grid current was found to be 38.31% with major contribution by the 3^{rd} harmonic component (37%) and 5^{th} harmonic component (9.5%).

5.5.2 With Harmonic Compensation

It was explained in Chapter 4, that current controllers employed using PR controllers, can be modified to compensate a specific harmonic component. Therefore, utilizing the resonant component of Equation 4.16, the 3^{rd} and 5^{th} harmonic compensator was added to the standard PR controller.
The grid current and voltage along with the harmonic performance of the grid current are shown in Figure 5.9.



(a) Grid Voltage and Current



(b) THD of grid current

Figure 5.9: Harmonic performance of the converter with 3^{rd} & 5^{th} harmonic compensation

In Figure 5.9b, the FFT analysis of the grid current is shown, the THD of the grid current was found to be **0.11**% with the 3^{rd} harmonic component contributing less than 0.06% and the 5^{th} harmonic component contributing less than 0.03 %.

5.6 Conclusion

In this chapter, the simulation results of the converter model were illustrated. Controllers were tested and their responses were verified. To test the complete system, the results for the nominal operation of the converter have been illustrated. Significance of implementing a PR based current controller has been illustrated by compensating the 3^{rd} and 5^{th} harmonics present in the grid current.

Chapter 6

Component Selection and Loss Calculation

6.1 Introduction

In the previous chapter, the simulation results for the complete system were illustrated. The response of the system gave a clear indication that the control system is working correctly. Before initiating the design of the hardware prototype, it is important to select the right components that are suited for this application. In this chapter, the selection of the most important components such as the MOSFET and the gate driver has been carried out. To determine the theoretical efficiency of the converter, loss calculation is performed under worse case scenario.

6.2 MOSFET

6.2.1 Selection Criteria

The selection of a MOSFET depends mainly on the following criteria [49]:

1. **Voltage rating**

   The rated drain-source voltage, V_{DS} of the MOSFET must be greater than the applied voltage. Failing to do so, would result in an avalanche break-down leading to the destruction of the switch. Moreover, selection must be done in such a manner that there must be a sufficient margin between the rated drain-source voltage of the switch and the applied voltage across the switch. This is important to safeguard the lifetime of the switch.

2. **Current rating**

   The selection of MOSFET with regards to the current rating is done differently. The current ratings given in the data sheets mostly refer to the value when the case temperature of the switch corresponds to the ambient temperature i.e. 25 °C. However, this is not true because losses will vary this temperature according to the cooling apparatus and ambient temperature.
   For instance, converters installed at the back of a PV panel will be subjected to an ambient temperature that would exceed 40 °C. In this case, the on-state resistance of the switch would increase thereby leading to a decrease in the current rating of the switch for that specific ambient temperature. Therefore, a switch rated to handle sufficiently high currents is required.

3. **On-state resistance**

   The on-state resistance of a MOSFET is governed by the following equation:

   $$R_{\mathrm{DS(on)}} \propto V_{\mathrm{DS}}^{2.5 \text{ to } 2.7} \tag{6.1}$$

   Therefore, selecting an over rated switch in terms of break-down voltage would increase the on-state resistance leading to a significant increase in the conduction loss.

4. **Gate threshold voltage**

   The gate threshold voltage is an important parameter that determines the range of gate driving voltage. The gate drive voltage must be sufficiently larger than the gate threshold voltage. Data sheets define the limits of the gate voltage. Setting a higher gate voltage minimizes the on-state resistance of the switch for a given load. However, it increases the driver loss.

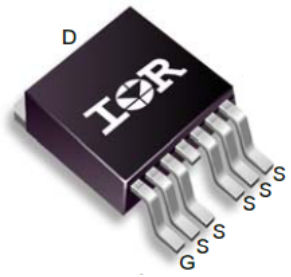
5. **Switching speed**

   Depending on the application, it is important to take note of the switching times of the MOSFET. Note, that for high frequency applications such as the CHB converter, switching losses account for a significant portion of the total power dissipation of the switch. Therefore, a high speed MOSFET should be utilized for reducing the switching loss.

Taking the following criteria under considerations, the following MOSFET was chosen for the CHB converter:

Model No.		**IRFS3006-7PPbF**
Package		**D^{2}PAK 7 Pin**
Parameter		**Value**
Drain-Source Breakdown Voltage	V_{DS}	60 V
Continuous Drain Current (25 °C)	I_D	240 A
On-state Resistance	$R_{DS(on)}$	2.1 mΩ
Internal Gate resistance	$R_{G(int)}$	2.1 Ω
Gate-Source Voltage	V_{GS}	±20 V
Gate Threshold Voltage	V_{th}	2 V
Total Gate Charge	Q_G	300 nC
Turn on delay	$t_{d(on)}$	14 ns
Rise Time	t_r	61 ns
Turn off delay	$t_{d(off)}$	118 ns
Fall time	t_f	69 ns

(a) Data sheet parameters



(b) D^{2}PAK 7 pin package

Table 6.1: IRFS3006-7PPbF 60 V N-Channel MOSFET [50]

6.2.2 Power Dissipation

The power losses in the switch can be divided into 3 parts:

1. Conduction losses
2. Switching losses
3. Blocking (Leakage) losses, normally being neglected.

A systematic approach to calculating the MOSFET losses has been provided in [51]. This method will be utilized for determining the losses in the selected MOSFET.

MOSFET Conduction Losses

Step-1: Determining the On-State Resistance, $R_{\mathrm{DS(on)}}$

According to the data sheet parameters mentioned in Table 6.1, the maximum ON-state resistance of the MOSFET is 2.1 mΩ. However, this value has been calculated for a junction temperature of 25°C.

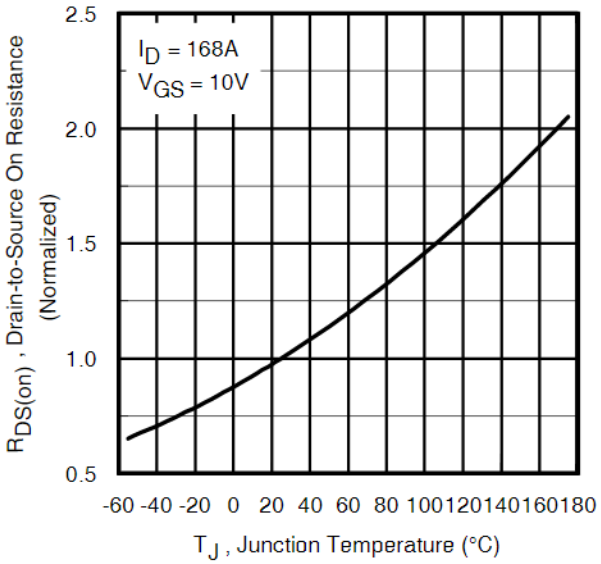


Figure 6.1: Normalized ON-state Resistance vs. Junction Temperature [50]

Figure 6.1 shows the variation of of the on-state resistance with change in the junction temperature. For the worse case scenario, a junction temperature of 140 °C has been considered for the calculation.
The resulting on-state resistance is obtained as,

$$R^{140^\circ C}_{\mathrm{DS(on)}} = 1.75 \cdot R^{25^\circ C}_{\mathrm{DS(on)}}$$

$$\boxed{R^{140^\circ C}_{\mathrm{DS(on)}} = 3.7\ \mathrm{m\Omega}}$$

Step-2: Determine RMS Switch Current

For sinusoidal pulse width modulation, the duty cycle for the top switch is given by,

$$D_{\mathrm{u}}(\omega t) = \frac{1}{2} + \frac{m}{2}\sin\omega t \tag{6.2}$$

and for the lower switch,

$$D_{\mathrm{l}}(\omega t) = 1 - D_{\mathrm{u}}(\omega t) \tag{6.3}$$

The grid current can be expressed by the following expression,

$$i_{\mathrm{g}}(\omega t) = \hat{i}_{\mathrm{g}} \cdot \sin(\omega t - \phi) \tag{6.4}$$

where, ϕ is the power factor angle defined as the phase-shift angle between the grid voltage and current. The RMS current is given by,

$$\boxed{I_{\mathrm{D(rms)}} = \sqrt{\frac{1}{2\pi} \cdot \int_{\phi}^{2\pi+\phi} D_{\mathrm{u}}(\omega t) \cdot i_{\mathrm{g}}^2(\omega t) \cdot d\omega t}} \tag{6.5}$$

Step-3: Calculate conduction loss

The conduction losses of the MOSFET is given by,

$$\boxed{P_{\mathrm{CM}} = I_{\mathrm{D(rms)}}^2 \cdot R_{\mathrm{DS(on)}}^{140^{\circ}C}} \tag{6.6}$$

MOSFET Switching Losses

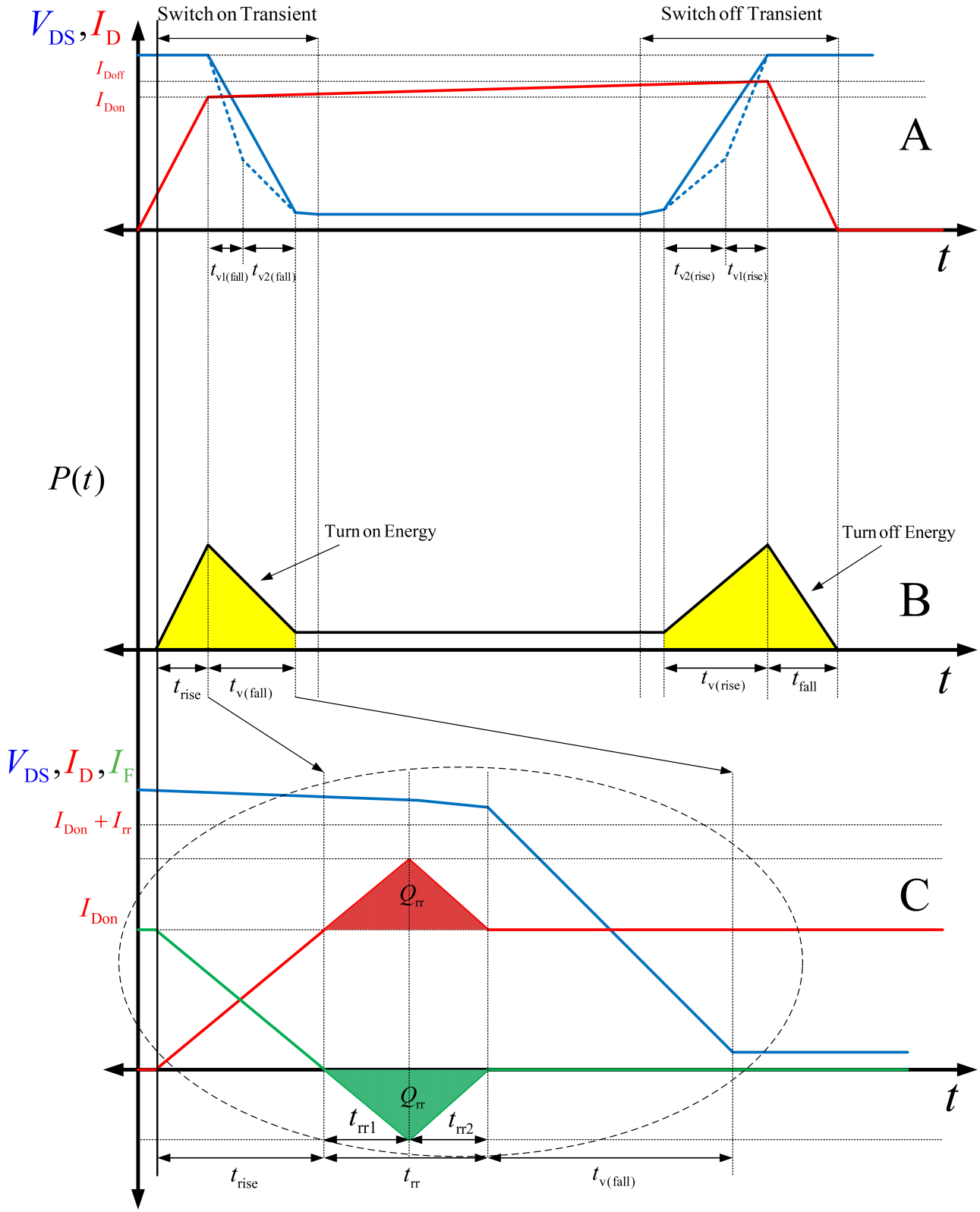


Figure 6.2: Typical switching characteristics of a MOSFET

Step - 1 Calculating the voltage fall-time and rise-time

To accurately calculate the voltage fall-time, the non-linearity of the gate-drain capacitance, C_{GD} needs to be taken into account.
For this, a 2-point approximation has been utilized [51], the approximation has been carried out as follows:

- If $V_{DS} \in \left[\frac{V_{DS}}{2}, V_{DS}\right]$ then, $C_{GD1} = C_{GD}(V_{DS})$.
- If $V_{DS} \in \left[0, \frac{V_{DS}}{2}\right]$ then, $C_{GD2} = C_{GD}(R_{DS(on)} \cdot I_D)$.

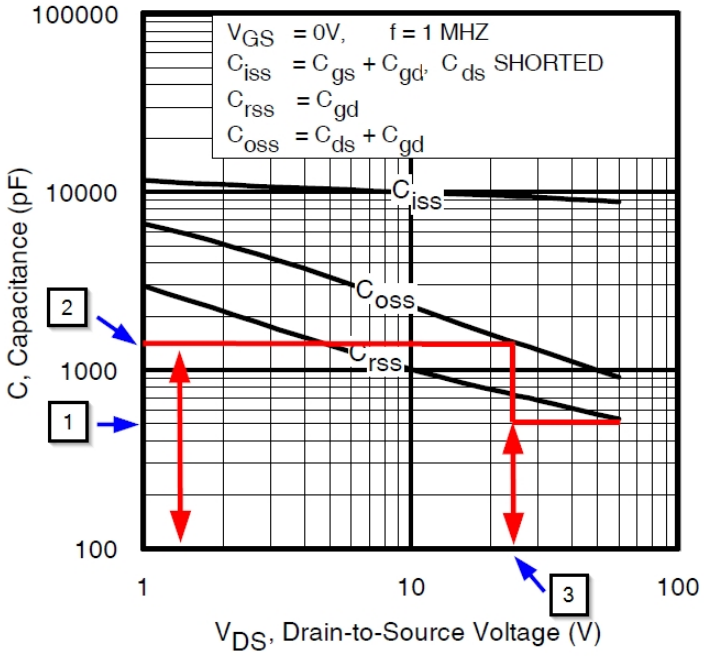


Figure 6.3: Gate-Drain Capacitance vs. Drain-Source Voltage [50]

The values of these gate-drain capacitances have been indicated in Figure 6.3 as **1** and **2** respectively. On the other hand, **3** represents the point at which the drain-source voltage is 50% of the applied voltage across the switch.

The voltage fall time during switch on transient can thus, be calculated as follows:

$$t_{v(fall)} = \frac{t_{v1(fall)} + t_{v2(fall)}}{2} \tag{6.7}$$

where,

$$t_{v1(fall)} = \left(V_{DS} - R_{DS(on)} \cdot I_{D(on)}\right) \cdot R_G \cdot \frac{C_{GD1}}{\left(V_{drv} - V_{((miller))}\right)} \tag{6.8}$$

$$t_{v2(fall)} = \left(V_{DS} - R_{DS(on)} \cdot I_{D(on)}\right) \cdot R_G \cdot \frac{C_{GD2}}{\left(V_{drv} - V_{((miller))}\right)} \tag{6.9}$$

Similarly, the voltage rise time during switch off transient can be calculated as follows:

$$t_{\text{v(rise)}} = \frac{t_{\text{v2(rise)}} + t_{\text{v2(rise)}}}{2} \tag{6.10}$$

where,

$$t_{\text{v1(rise)}} = \left(V_{\text{DS}} - R_{\text{DS(on)}} \cdot I_{\text{D(on)}}\right) \cdot R_{\text{G}} \cdot \frac{C_{\text{GD1}}}{V_{\text{(miller)}}} \tag{6.11}$$

$$t_{\text{v2(rise)}} = \left(V_{\text{DS}} - R_{\text{DS(on)}} \cdot I_{\text{D(on)}}\right) \cdot R_{\text{G}} \cdot \frac{C_{\text{GD2}}}{V_{\text{(miller)}}} \tag{6.12}$$

Step - 2 Calculate switching energies

The worse case turn-on energy losses in the MOSFET can be calculated as follows:

$$E_{\text{onM}} = E_{\text{on}} + E_{\text{on(rr)}} \tag{6.13}$$

where,
E_{on} is the turn on energy loss without taking account the reverse recovery process of the diode given by,

$$E_{\text{on}} = \frac{(t_{\text{rise}} + t_{\text{v(fall)}})}{2} \cdot V_{\text{DS}} \cdot I_{\text{D(on)}} \tag{6.14}$$

and,
$E_{\text{on(rr)}}$ is the turn on energy loss taking account the reverse recovery process of the diode. This has been considered 0 due to unity power factor operation. The turn off energy loss of the MOSFET is therefore given by,

$$E_{\text{offM}} = \frac{t_{\text{v(rise)}}}{2} \cdot V_{\text{DS}} \cdot I_{\text{D(off)}} \tag{6.15}$$

Step-3 Calculating switching losses

The switching losses for MOSFET can be calculated as follows:

$$\boxed{P_{\text{SWM}} = (E_{\text{onM}} + E_{\text{offM}}) \cdot f_{\text{sw}}} \tag{6.16}$$

(6.17)

6.2.3 Total Power Dissipation

The total power dissipation in each MOSFET can be determined as the sum of the conduction losses and the switching losses.

$$\boxed{P_{\text{lossM}} = P_{\text{CM}} + P_{\text{SWM}}} \tag{6.18}$$

6.3 MOSFET Gate Driver

Gate drivers are an integral part of a converter. They serve as an interface between the control signals (digital or analog controllers) and power switches. They help in reducing design complexity as well as to make compact PCB boards.

6.3.1 Selection Criteria

The following criteria have been considered for selecting the MOSFET gate driver [52]:

1. **Isolation type and barrier**
   There are mainly 3 types of isolation found in most of the gate drivers. Each type utilizes a different principle through which the signals are transferred from the low voltage side to the high voltage side of the system without an electrical connection.

   - Optical
   - Magnetic
   - Capacitive

   Table 6.2 summarizes the difference between these 3 isolation in terms of current draw, reliability and noise immunity.

Isolation Type	Current Draw	Reliability	Noise immunity
Optical	High	Medium	Low
Magnetic	High	Medium	Low
Capacitive	Low	High	High

Table 6.2: Comparison between the available isolation technologies

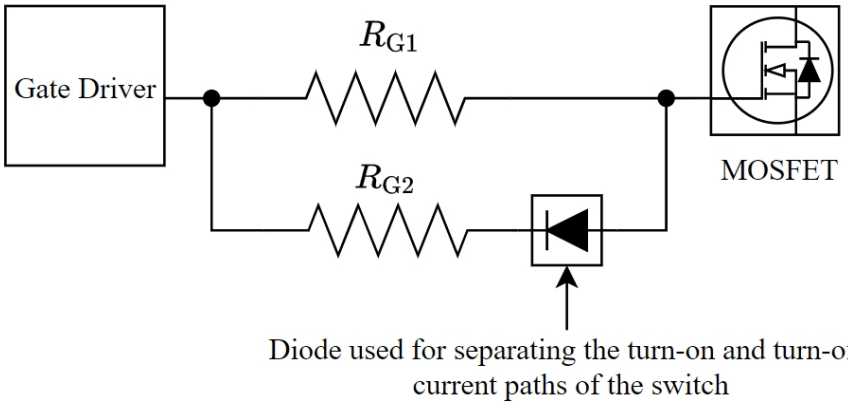
   On the other hand, isolation barriers ensure that the low and high voltage circuits remain electrically isolated from each other. There are mainly 3 types of isolation barriers:

   - Functional isolation, ensures nominal operation, however, fails to protect against electric shock.
   - Basic isolation, provides protection against electric shocks as long as isolation barrier does not undergo breakdown.
   - Reinforced isolation, utilizes double the basic isolation barrier, to provide redundancy.

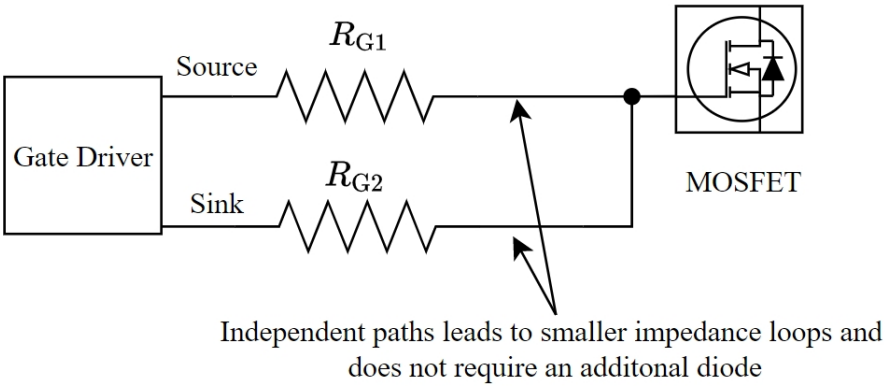
2. **Drive Strength**
   The drive strength refers to the source and sink capabilities of the driver. The driving current is related to the total gate charge of the MOSFET as well as the application. If the gate current required by the switch is greater than the peak driving current of the gate driver then, an additional gate resistor is required to limit the amount of current. Therefore, to inject the same amount of charge into the gate capacitance, the switching characteristics of the MOSFET would change.

3. **Propagation delay**
   Propagation delay of the driver is defined as the time it takes from 50% of the input to 50% of the output. This is an important parameter in high frequency applications where the dead time between the switches is limited. It is important to select a driver with low propagation delay.

4. **Split Outputs**



(a) Single Output



(b) Split Outputs

Figure 6.4: Single Output vs. Split Outputs for independent control of turn-on and turn off of the MOSFET

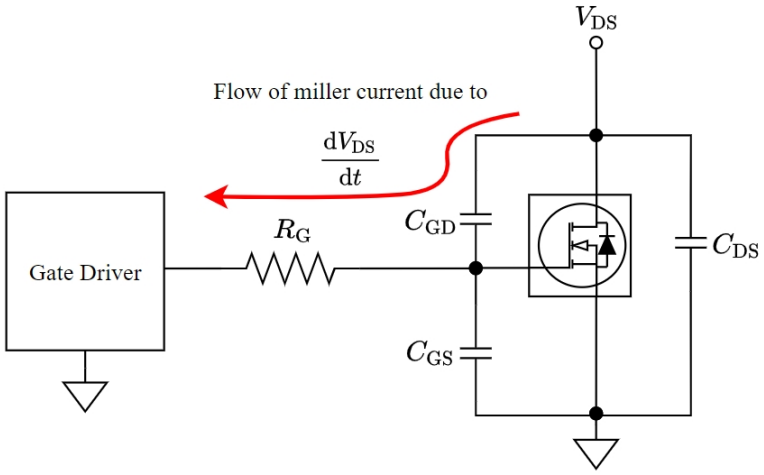
The gate driver sources and sinks current at the gate of the MOSFET to turn it on and off. The rise time, fall time and delays between turn on and turn off are different and therefore, require separate consideration.

- During turn off, large voltage overshoot may occur due to $\frac{\mathrm{d}i}{\mathrm{d}t}$, therefore, it is important that the switch needs to be turned off slowly.
- On the other hand, during turn on, it is important to turn on the switch faster so as to reduce the rise time of the voltage and reduce the switching losses.

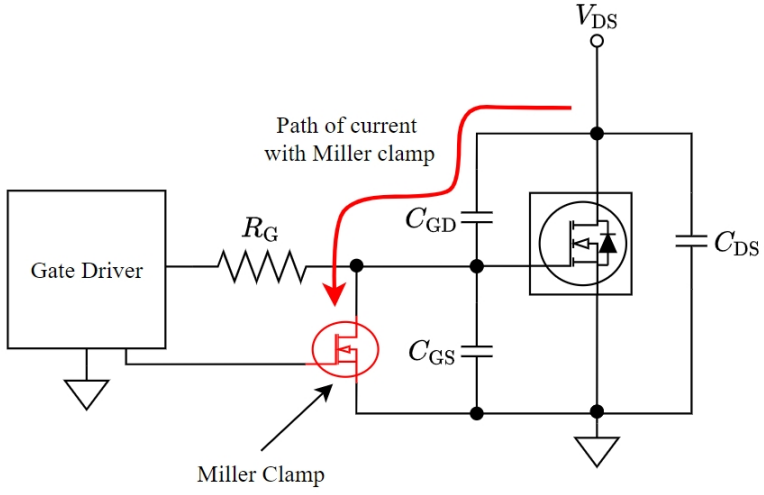
In order to implement such flexibility in the switching operation, drivers with split outputs prove to be a suitable candidate as they provide separate paths for source and sink currents to flow.

5. **Common Mode Transient Immunity (CMTI)**
   CMTI is the maximum acceptable rate of rise or fall of the common mode voltage, applied between two isolated circuits. In high power applications, the voltage and the current of the switches change within hundreds of nanoseconds. This generates very large voltage transients (≈>100 V/ns). The gate driver experiences these voltage swings, and therefore, it is important for the driver to be able to withstand CMTI above the rate level to prevent noise injection in the low voltage side and to prevent failure of isolation barrier.

6. **Miller Clamp**
   $\frac{dV}{dt}$ during switching, interacts with the parasitic Miller capacitance. This leads to a current flow through the gate causing the switch to falsely turn on. To prevent this problem, Miller clamps are provided to reroute the current without affecting switching efficiency.
   A Miller clamp is basically, a low impedance switch. It keeps the switch in the off-state by either connecting the gate of the MOSFET to the ground or connecting it to the negative voltage rail.



(a) Without Miller Clamp



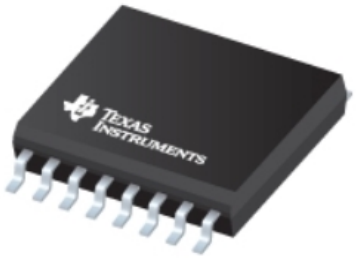
(b) With Miller Clamp

Figure 6.5: Importance of Miller Clamps

Based on the above criteria, the Texas Instruments **ISO5852S DWR** MOSFET Driver was chosen. Some of the important parameters of the driver have been tabulated in Table 6.3a.

Model No.		**ISO5852S-DWR**		
Package		**SOIC 16 Pin**		
Parameter		**Minimum**	**Nominal**	**Maximum**
Input Supply Voltage	V_{CC1}	2.25 V		5.5 V
Positive Supply Voltage	V_{CC2}	15 V		30 V
Negative Supply Voltage	V_{EE2}	-15 V		0 V
Operating Temperature	T_a	-40 °C		125 °C
Source Current	I_{OUTH}		2.5 A	
Sink Current	I_{OUTL}		5 A	
Maximum Power Dissipation	P_d			251 mW
Type of Isolation			Capacitive	
Type of Isolation Barrier			Reinforced	

(a) Data sheet Parameters of ISO5852S-DWR [53]



(b) SOIC-16 Pin Package

Table 6.3: ISO5852S-DWR MOSFET Driver

6.3.2 Power Dissipation

Step-1 Determining the total gate capacitance

Using data sheet parameters of the MOSFET in Table 6.1, we have the total gate charge, Q_G = 300 nC. However, this is for specific test conditions.
In order to get the right gate charge value, the relationship between the gate-source voltage and the total gate charge must be studied.

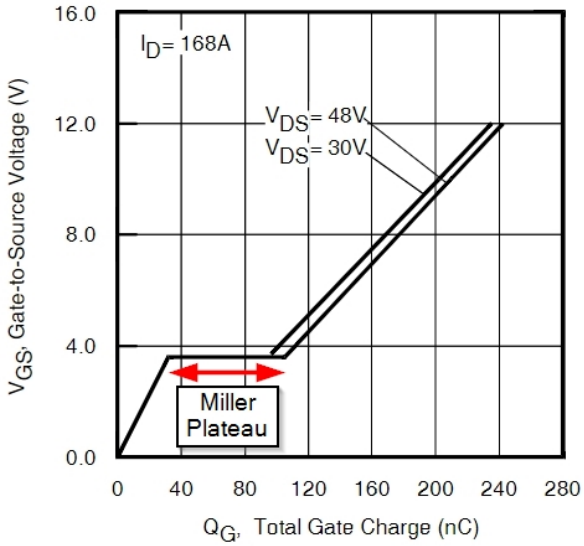


Figure 6.6: Gate Charge vs Gate-Source Voltage [50]

Figure 6.6 shows the variation of total gate charge with gate-source voltage. For this application, a gate-source voltage of 15 V has been considered for driving the MOSFET. Each switch has to block 50 V. Therefore, the curve corresponding to the V_{DS} = 48 V can be utilized for the sake of simplicity.

By determining the slope of the curve after the Miller plateau, the total gate charge corresponding to a gate-source voltage, V_{GS} = 15 V can be identified. This was found to be **285 nC**. Therefore,

$$\boxed{Q_G = 285 \text{ nC}}$$

Now, the total gate capacitance is given by,

$$C_G = \frac{Q_G}{V_{GS}} \tag{6.19}$$

$$\boxed{C_G = 19 \text{ nF}}$$

Step-2 Calculating power dissipation in the gate driver

The power dissipation in the gate driver can be calculated as follows [54]:

$$P_{Drv} = C_G \cdot V_{GS}^2 \cdot f_{sw} \tag{6.20}$$

For a 5-level converter,

$$\boxed{P_{Drv} = 205.2 \text{ mW}}$$

Similarly, for a 19-level converter,

$$\boxed{P_{Drv} = 68.4 \text{ mW}}$$

6.3.3 Gate Resistance

The speed at which a MOSFET can be turned on and off depends on charge/discharge rate of the gate capacitance of the MOSFET.
According to the data sheet parameters in Table 6.1, the total turn on time of the MOSFET can be determined as the sum of the turn on delay time, and the rise time.

$$t_{on} = t_{d(on)} + t_r \tag{6.21}$$

$$\boxed{t_{on} = 75 \text{ ns}}$$

In the previous section, the total gate charge was determined. Therefore, the amount of drive current required to pump this charge into the gate capacitance can be determined as follows,

$$\hat{I}_{drv} = \frac{Q_G}{t_{on}} \tag{6.22}$$

$$\boxed{\hat{I}_{drv} = 3.8 \text{ A}}$$

This gives an indication that a driver having a peak driving current of at least **4 A** would be a suitable candidate for serving the driving needs of the chosen MOSFET. However, the chosen driver, **ISO5852S DWR** can deliver only up to **2.5 A** source and **5 A** sink currents.
There is a requirement to reduce the amount of current by introducing an external gate resistance. As a result, to pump the same amount of charge into the gate capacitance, the switching characteristics of the MOSFET would change. This is a tradeoff.

From Table 6.1, the internal gate resistance of the MOSFET is **2.1 Ω**. The corresponding driving current for a gate-source voltage of 15 V, would be **10 A**, which is very high.

An additional external gate resistance is therefore, introduced to limit the driving current. Therefore, based on the source current of 2.5 A, an external gate resistance of **5.6 Ω** can be utilized for this purpose. Therefore, the total gate resistance is,

$$R_G = R_{G(ext)} + R_{G(int)}$$

$$\boxed{R_G = 7.7 \ \Omega}$$

Therefore, for the total gate resistance, the driving current is reduced to **1.94 A**, which can be delivered by the chosen gate driver.

6.3.4 Verification of the selected gate resistance

From Table 6.1, the gate threshold voltage of the chosen MOSFET is **2 V**. This is a very small value, and may cause the MOSFET to falsely turn on if the driver is utilizing a unipolar power supply. Therefore, to ensure that the gate capacitance is completely discharged, a bipolar power supply is necessary. For this design, the following bipolar power supply has been chosen,

$$V_{CC2} = +15 \text{ V}$$

$$V_{EE2} = -5 \text{ V}$$

The inclusion of an external gate resistance although helps in avoiding the reselection of driver, yet, it also means that more power would be dissipated in the driver circuit. Therefore, it is important to ensure that the output power under load of the gate driver does not exceed the permissible maximum power dissipation of the driver for a given gate resistance. The maximum power dissipation, according to Table 6.3a is **251 mW**.

The power consumption can be decomposed into 3 parts [53]:

1. Total Input Power, P_{id} given by,

$$P_{\text{id}} = V_{\text{CC1(max)}} \cdot I_{\text{CC1(max)}} \tag{6.23}$$

2. Total Output Power, P_{od} given by,

$$P_{\text{od}} = (V_{\text{CC2}} - V_{\text{EE2}}) \cdot I_{\text{CC2(max)}} \tag{6.24}$$

3. Output Power Under Load, P_{ol} given by,

$$P_{\text{ol}} = P_{\text{d}} - P_{\text{id}} - P_{\text{od}} \tag{6.25}$$

where, $I_{\text{CC1(max)}}$ & $I_{\text{CC2(max)}}$ are the maximum input and output supply quiescent currents given in the data sheet [53].
Using Equations 6.23, 6.24 and 6.25 we have,

$$\boxed{P_{\text{id}} = 24.7 \text{ mW}}$$
$$\boxed{P_{\text{od}} = 120 \text{ mW}}$$
$$\boxed{P_{\text{ol}} = 106.3 \text{ mW}}$$

Therefore, the dynamic output power consumption under worse case condition can expressed as [53],

$$P_{\text{ol-wc}} = 0.5 \times f_{\text{sw}} \times Q_{\text{G}} \times (V_{\text{CC2}} - V_{\text{EE2}}) \times \left(\frac{r_{\text{on-max}}}{r_{\text{on-max}} + R_{\text{G}}} + \frac{r_{\text{off-max}}}{r_{\text{off-max}} + R_{\text{G}}} \right) \tag{6.26}$$

where,
$r_{\text{on-max}}$ = 4 Ω and,
$r_{\text{off-max}}$ = 2.5 Ω
are the worse case output resistance in the on-state and off-state respectively.

The condition that must be obeyed for the chosen gate resistance, is as follows:

$$\boxed{P_{\text{ol-wc}} < P_{\text{ol}}} \tag{6.27}$$

For the 5-level converter,

$$\boxed{P_{\text{ol-wc}} = 60.2 \text{ mW}}$$

Similarly, for the 19-level converter,

$$\boxed{P_{\text{ol-wc}} = 20.1 \text{ mW}}$$

The output power consumption under worse conditions for both the converters obeys the constraint defined by Equation 6.27. Therefore, the chosen value of gate resistance is acceptable.

6.4 Filter Inductor

6.4.1 Specifications

Parameter		5-level	19-level
Inductance	L_f	75 μH	2 × 60 μH
Number of turns	N	14	15
Current Ripple	$\Delta\, i_{\mathrm{L(max)}}$	2.45 A	10.37 A
Switching Frequency	f_sw	48 kHz	16 kHz

Table 6.4: Electrical specifications of the filter

Parameter		Value
Core Size		ETD54
Core Cross-sectional Area	A_c	280 mm^2
Magnetic Length	l_m	127 mm
Mean Length Turn	MLT	97 mm
Window Area	A_w	315.6 mm^2
Effective Volume	V_v	35600 mm^3

(a) Core Specifications [55]

Parameter		Value
Core Material		3C90
Saturation Flux Density	B_sat	380 mT
Relative Permeability	μ_r	2000
Core Loss	P_v	80 kW/m^3

(b) Core Material Specifications [56]

Table 6.5: Filter Inductor Specifications

The determination of electrical specifications are shown in Appendix A.1.

6.4.2 Core Loss

From Table 6.5b, the core loss per unit volume as well as the volume of the core can be used to calculate the core losses.

$$P_\mathrm{c} = P_\mathrm{v} \cdot V_\mathrm{c} \tag{6.28}$$

$$\boxed{P_\mathrm{c} = 2.8\ \mathrm{mW}}$$

6.4.3 Winding Loss

Winding loss in inductors are introduced due to 2 effects:

- **Proximity Effect**
  In some of the inductor and transformer designs, the presence of layering introduces proximity effect and thus, needs to be taken into account. The contribution of this effect to winding losses is significant, and hence, it is important to ensure that the number of winding layers are kept minimum.

- **Skin Effect**
  On the other hand, skin effect is observed in application where the frequency in the range of kHz and above. This reduces the effective cross-sectional area of the conductors thereby increasing the resistance.

Detailed procedure for calculating the winding losses while taking both proximity effect and skin effect into account is provided in [57].
The penetration depth due to the skin effect is given by,

$$D_{\text{pen}} = \frac{65}{\sqrt{f_{\text{sw}}}} \text{ mm} \tag{6.29}$$

Using the penetration depth, the effective AC resistance, due to skin effect is given by,

$$R_{\text{ac,skin}} = \frac{d_{\text{bare}}}{D_{\text{pen}}} \cdot R_{\text{dc}} \tag{6.30}$$

Therefore, the effective power loss in layer m, due to proximity and skin effect is given by,

$$P_{\text{w}} = I_{\text{rms}}^2 \cdot \left[(m-1)^2 + m^2\right] \cdot R_{\text{ac,skin}} \tag{6.31}$$

6.4.4 Total Losses

The total losses in the filter inductance can be obtained as the sum of the core losses and the winding losses due to skin effect and proximity effect.

$$P_{\text{f}} = P_{\text{c}} + P_{\text{w}} \tag{6.32}$$

6.5 Theoretical Efficiency

To estimate the theoretical efficiency, losses described in the previous sections have been calculated, at different operating conditions. Note, that the filter losses have not been considered. The load of the converter is increased from 5% to the full load and the losses are calculated at 7 unique points of interest.

% Load	Input Power, P_{in}(W)	Output Power, P_{out}(W)	Total Switch Loss (W)	Efficiency, η
5%	25 W	22.26 W	2.74 W	89.04%
10%	50 W	45.69 W	4.31 W	91.38%
20%	100 W	92.55 W	7.45 W	92.55%
30%	150 W	139.38 W	10.62 W	92.92%
50%	250 W	232.99 W	17.01 W	93.2%
75%	375 W	349.87 W	25.13 W	93.3%
100%	500 W	466.62 W	33.38 W	93.32%

Table 6.6: Theoretical efficiencies for 5-level CHB converter

% Load	Input Power, P_{in}(W)	Output Power, P_{out}(W)	Total Switch Losses (W)	Efficiency, η
5%	112.5 W	108.06 W	4.44 W	96%
10%	225 W	217.86 W	7.14 W	97.8%
20%	450 W	437.38 W	12.62 W	97.2%
30%	675 W	656.77 W	18.23 W	97.3%
50%	1125 W	1095.18 W	29.82 W	97.3%
75%	1687.5 W	1642.48 W	45.02 W	97.3%
100%	2250 W	2188.99 W	61.01 W	97.2%

Table 6.7: Theoretical efficiencies for 19-level CHB converter

6.5.1 Observations

- Figure 6.7 shows the efficiency curves for the 5-level and the 19-level CHB converter. It is evident from both the trends that there is significant difference in the efficiencies of both the converters.
- This difference in the efficiency trend is due to 2 reasons:
  - As mentioned earlier, the switching losses depend on the switching frequency which, in turn depends on the number of voltage levels. A converter generating 19 voltage levels can operate at a much lower switching frequency as compared to a converter generating 5 voltage levels. As a result, switching losses are much more dominant in the 5-level CHB as compared to the 19-level CHB converter for the same semi-conductor switch.
  - For calculating losses in the semi-conductor switch, most of the parameters are obtained from the data sheet. Each parameter is calculated based on a certain test conditions which are also provided by the manufacturer. These test conditions do not correspond to the test conditions set in this case. This leads to over-estimation of losses.

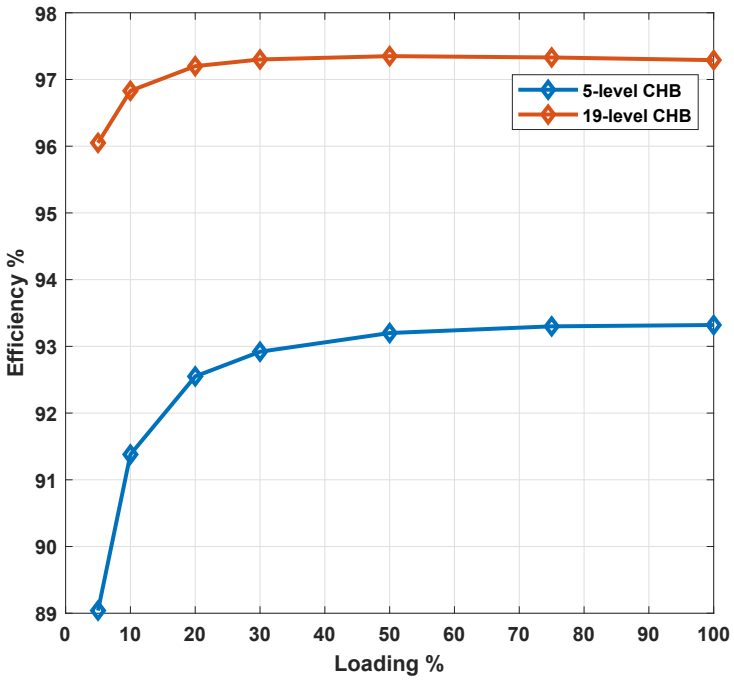


Figure 6.7: Comparison of performance of both converters

6.5.2 Euro & CEC Efficiency

"Power electronic converters do not operate always at their maximum efficiency, but according to an efficiency profile as function of power" [58]. This necessitates to compute the Euro and CEC weighted efficiencies as they measure the performance of the converter across the range of the converter's capacity. 7 efficiency points are required which have been calculated in Table 6.6 & 6.7.

The Euro efficiency and CEC efficiency is given by [58],

$$\eta_{\text{Euro}} = 0.03 \times \eta_{5\%} + 0.06 \times \eta_{10\%} + 0.13 \times \eta_{20\%} + 0.1 \times \eta_{30\%} + 0.48 \times \eta_{50\%} + 0.2 \times \eta_{100\%} \tag{6.33}$$

$$\eta_{\text{CEC}} = 0.04 \times \eta_{10\%} + 0.05 \times \eta_{20\%} + 0.12 \times \eta_{30\%} + 0.21 \times \eta_{50\%} + 0.53 \times \eta_{75\%} + 0.05 \times \eta_{100\%} \tag{6.34}$$

where, $\eta_{X\%}$ indicates efficiency of the converter at X % load.

From Table 6.6, the Euro and CEC efficiency of the 5-level CHB converter was found to be,

$$\boxed{\eta_{\text{Euro}} = 93\%} \qquad \boxed{\eta_{\text{CEC}} = 93\%}$$

Similarly from Table 6.7, the Euro and CEC efficiency of the 19-level CHB converter was found to be,

$$\boxed{\eta_{\text{Euro}} = 97\%} \qquad \boxed{\eta_{\text{CEC}} = 97\%}$$

6.6 Conclusion

In this chapter, the selection of crucial components such as the semiconductor switch and the gate driver was carried out. Before finalizing the component, they were judged on the basis of several important criteria. After finalizing the components, power dissipation in these components was computed for both the 5-level and the 19-level CHB converter. A systematic procedure for calculating the conduction and switching losses of the semiconductor switch as well as the power dissipation in the driver has been provided. This was followed by computing the theoretical efficiency. The performance of both CHB converters was evaluated by computing the CEC and European efficiencies.

Chapter 7

Design of hardware prototype

7.1 Introduction

In the previous chapter, it was concluded that the chosen gate driver, MOSFET as well as the filter inductance were acceptable based on Euro and CEC efficiencies. The next step, would be to design a hardware prototype of the H-bridge sub module, the building blocks of the CHB converter. The chapter begins with the general layout for the prototype. Apart from the gate driver and MOSFET, there are several other circuits and components that are essential and have been added to the prototype, details of which have been provided in this chapter. The chapter concludes with the assembly of one of the H-bridge cells.

7.2 General Structure of PCB

The hardware prototype under design must be modular as well as compact. The following PCB layout has been adopted for the prototype:

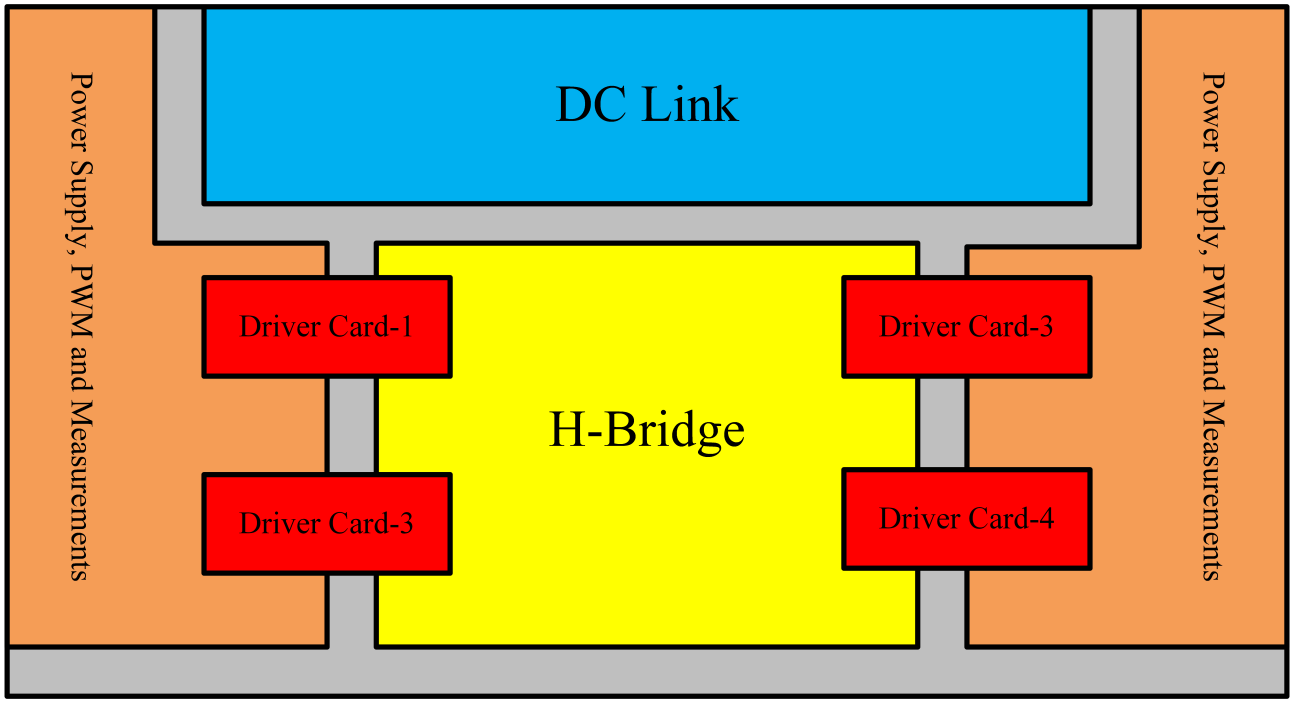


Figure 7.1: General Layout of the sub module

As shown in Figure 7.1, the hardware prototype can be divided into 2 parts:

- Driver Card.
- Power Board.

The power board will contain the H-bridge as well as other circuits essential for proper operation of the converter. On the other hand, driver cards will be mounted on the power board.

7.3 Gate Driver Card

7.3.1 Gate Driver IC

As discussed in Chapter 6, the **ISO5852S DWR** by Texas Instruments was chosen for this prototype. Some of the important protection features offered by the driver IC are as follows [53]:

1. 5.7 kV_{rms}, reinforced isolation.
2. Internal Active Miller Clamp.
3. DESAT Protection.
4. Fault alarm upon DESAT detection.
5. Soft turn-off during short-circuit.
6. I/O under voltage lockout (UVLO).

Pin Description

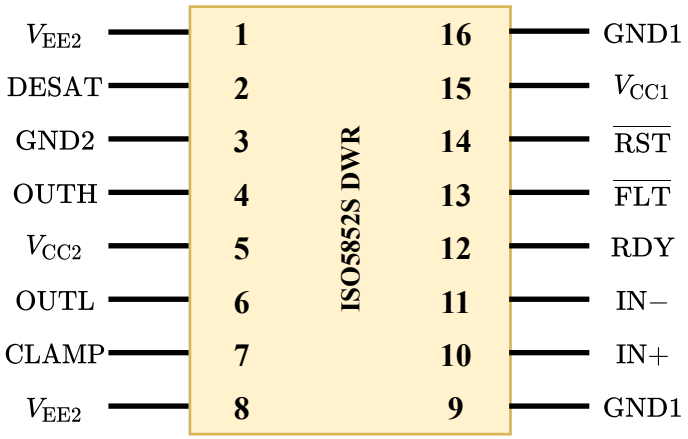


Figure 7.2: ISO5852SDWR Pins

Name	Pin No.	I/O	Description
DESAT	2	I	Desaturation voltage input
OUTH	4	O	Positive gate drive voltage output (Source)
OUTL	6	O	Negative gate drive voltage output (Sink)
CLAMP	7	O	Miller clamp output
IN+	10	I	Non-inverting gate drive voltage control input
IN-	11	I	Inverting gate drive voltage control input
RDY	12	O	Power-good output, active high
$\overline{FLT}$	13	O	Fault output, active low
$\overline{RST}$	14	I	Reset input
V_{EE2}	1, 8	N.A	Gate drive output negative supply
GND2	3	N.A	Gate drive supply ground
V_{CC2}	5	N.A	Gate drive output positive supply
GND1	9, 16	N.A	Input ground
V_{CC1}	15	N.A	Logic supply

Table 7.1: Pin Description [53]

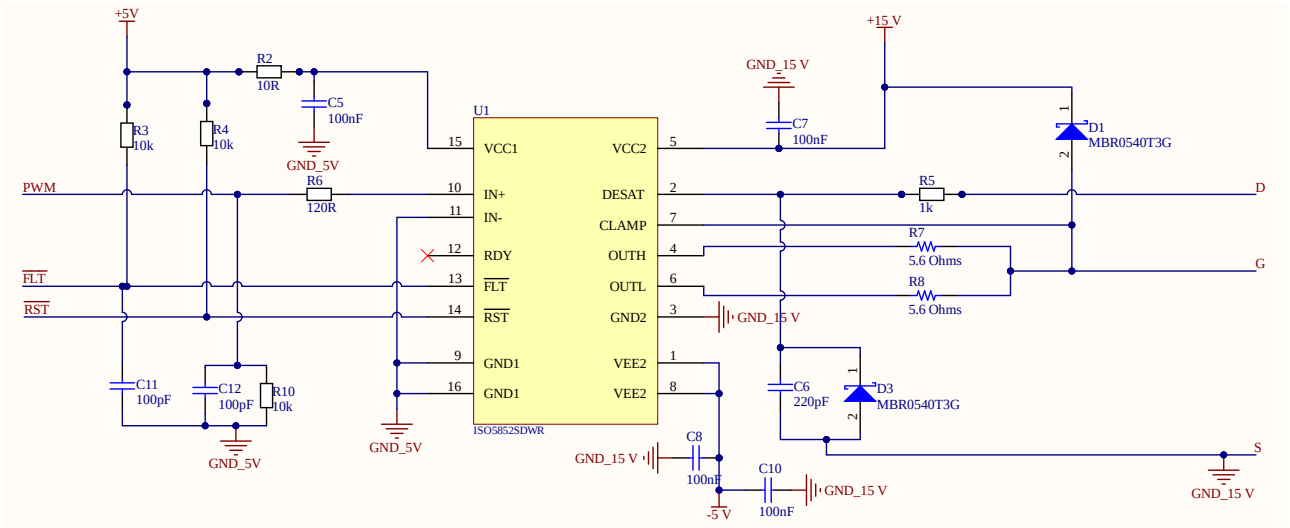


Figure 7.3: Gate Driver Circuit

Figure 7.3 shows a typical gate driver circuit utilized for driving a MOSFET using the chosen driver IC.

Remarks:

- C5, C7 and C8 are decoupling capacitors which are recommended by the manufacturer to be placed on the input supply pin (Pin: 15) as well as the output supply pin of the gate driver IC (Pin No. 1, 5 and 8).
- R6 is a current limiting resistor connected to pin 10. Additionally, an RC filter has been implemented with the help of R10 and C12 on pin 10, to suppress unwanted noise in the PWM signal.
- R7 and R8 are gate resistors connected on pins 4 and 6.
- Resistor R5 is recommended at pin 2 for protection purposes. C6 is a blanking capacitor has been implemented to disable the DESAT detection during the off-to-on transition of the semiconductor switch. Note, that the DESAT diode has not been included on the driver card, but, has been added on the power board. The DESAT diode is responsible for conducting the forward current, allowing sensing of the saturated drain to source voltage of the MOSFET as well as to withstand high voltage.
- D1 and D3 are zener diodes. D1 ensures that the gate voltage is clamped to V_{CC2} and therefore, prevents voltage spikes. On the other hand, D3 clamps the voltage across the blanking capacitor C6.

7.3.2 Isolated Gate Driver Supply

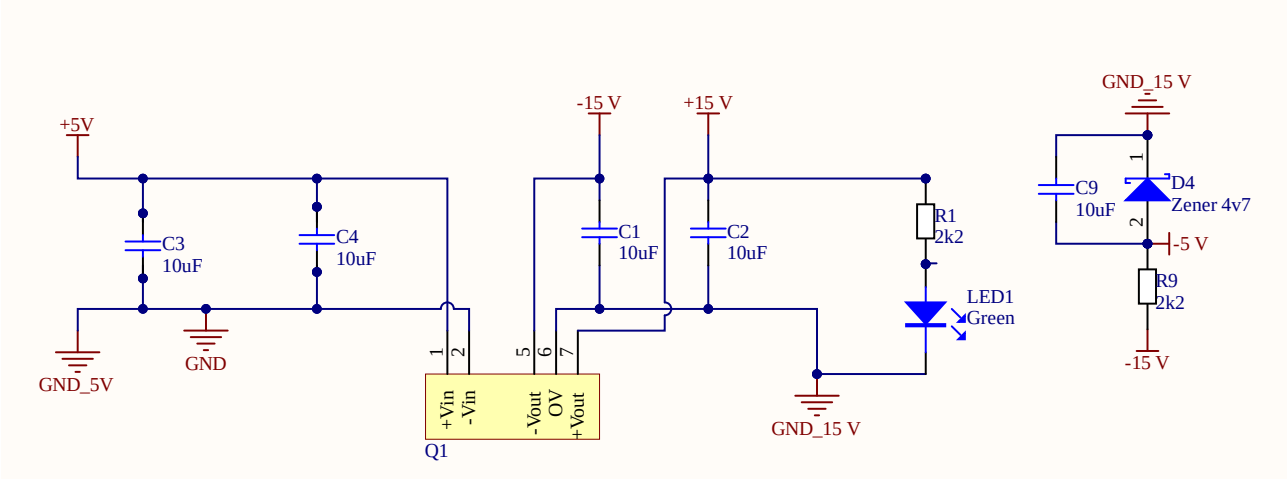


Figure 7.4: MEV1D0515SC based isolated gate driver bipolar supply

Figure 7.4 shows the gate driver supply utilized for the driver IC. It is based on MEV1D0515SC, a dual output 3 kV DC isolated DC-DC converter. This converter can deliver an output voltage of ±15 V at an input voltage of 5 V.

Remarks:

- C1, C2, C3, C4 and C9 are decoupling capacitors. Additionally, an LED has been added for indication purpose.
- It was mentioned earlier, that the gate driver would utilize a bipolar supply. The gate driver IC is capable of having a maximum bipolar supply voltage of ±15 V. However, for this application, a +15 V/-5 V is sufficient. To incorporate this, an additional zener diode based circuit was added on pin 5 of the DC-DC converter. D4 is a 4.7 V zener diode added to ensure that the voltage across pin 5 and ground was clamped to the required -ve voltage.
- This type of arrangement allows a lot of flexibility for bipolar driver supply. For instance, if -10 V was required for the semiconductor switch, then the existing diode needs to be replaced with a 10 V zener diode.

7.3.3 I/O Headers

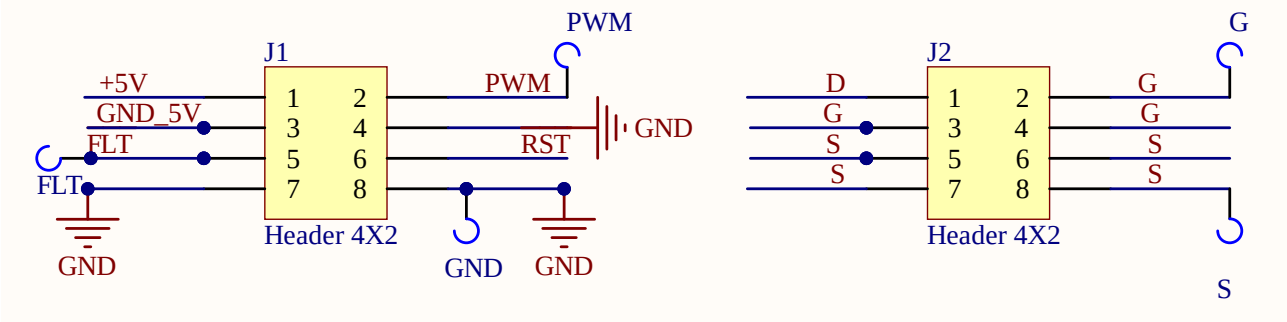


Figure 7.5: I/O Headers for the driver card

Figure 7.5 shows the I/O connectors for the gate driver cards. Depending on the number of connections required, a 4 X 2 male header needs to be added on the driver cards. Note, that while each pin of the header serves different function for input side header, the pins located on the output header, are combined together to allow even distribution of gate current and prevent hot spots.

7.4 Power Board

7.4.1 Fiber Optic Connectors

Interfacing the controller with the converter using cables, introduces issues in the signals transmitted and received such as attenuation due to the resistance of the conductor as well as the ringing phenomenon due to parasitic inductances of the wire. Moreover, if the controller is located far away from the converter, both these problems have a significant impact. To eliminate these problems, fiber optic technology has been utilized.

7.4.2 H-Bridge

- As mentioned earlier, DESAT diodes are placed on the power board rather than the driver card.
- Capacitors have been connected across both the arms of the H-bridge. These capacitors are known as snubber capacitors.
- PCB traces inherently contain parasitic inductances. During commutation, the MOSFET has to withstand voltage spikes, due to $\frac{\mathrm{d}i}{\mathrm{d}t}$ across these parasitic inductances. If this voltage spike exceeds the ratings of the switch, then this can lead to the failure of the switch. This is where snubber capacitors come into play.
- It is important that these capacitors need to be placed as close as possible to the semiconductor switches, so as to reduce the parasitic inductance. The surge suppression effect is greater for a smaller number of parallel groups and for larger total capacitance [59].
- In this design, 5 parallel connected capacitors have been utilized for serving this purpose.

7.4.3 DC Link

- In Chapter 4, the DC link capacitance was determined. According to Table 3.3b, a DC link capacitance of 6.6 mF per sub module is required.
- The DC link voltage per sub module is 50 V. Therefore, the voltage rating of the capacitor needs to be sufficiently higher than the applied DC link voltage. A voltage rating of 70 V was thus chosen for the DC link capacitor. There are 2 ways to approach the design:
  1. Connect a single capacitor of 6.6 mF, 70 V.
  2. Connect a series-parallel combination of smaller capacitors to form the required amount of equivalent capacitance.
- The first approach, does not effectively utilize the PCB board leaving a lot of unused space. On the other hand, the second approach, effectively utilizes the board space. Moreover, the DC link is more reliable as low voltage capacitors with small capacitances are utilized for obtaining the required amount of DC link capacitance.
- For this design, 6 series parallel combination has been utilized. $C_{\mathrm{dX}+}$ and $C_{\mathrm{dX}-}$ (X = 1, 2, ... 6) are 35 V, 2200 μF capacitors. The equivalent capacitance can therefore, be calculated as follows:

$$C_{\mathrm{DC}} = 6 \times (C_{\mathrm{dX}+} \,||\, C_{\mathrm{dX}-})$$

$$C_{\mathrm{DC}} = 6 \times 1.1 \text{ mF}$$

$$\boxed{C_{\mathrm{DC}} = 6.6 \text{ mF}}$$

7.4.4 DC Link Voltage Measurement

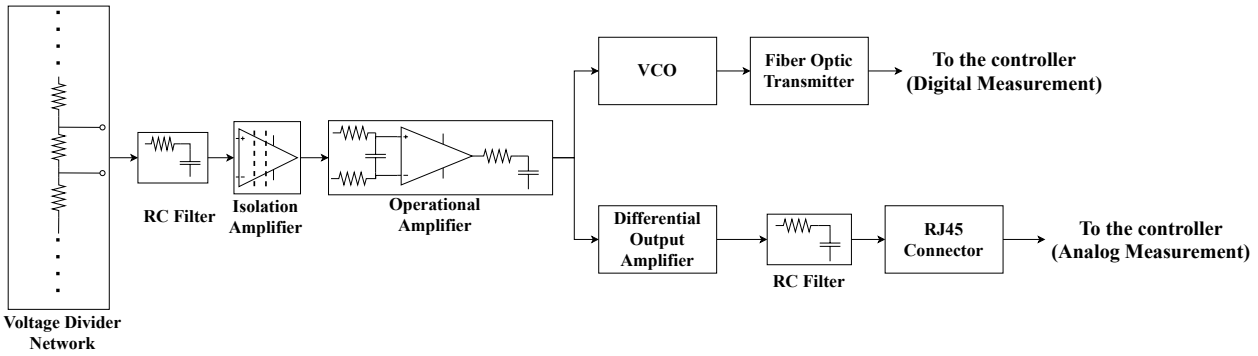


Figure 7.6: DC Link Voltage Measurement

- To measure the DC link voltage, a voltage divider network is utilized. The voltage divider network consists of 10 x 1 MΩ resistors and a 50 kΩ resistor. The voltage across the 50 kΩ is utilized for measurement purposes.
- To suppress unwanted high frequency noise, RC filters have been implemented at various locations in the circuit. The filtered differential signal is then passed through an isolation amplifier.
- An isolation amplifier behaves as an electronic transformer by providing sufficient isolation between the high voltage and the low voltage side. The isolation amplifier utilized for this design requires that the input differential signal must be in range of ±250 mV. Therefore, it is important to ensure, that the resistance across which the differential signal has been measured is selected such that it does not exceed the input differential range of the isolation amplifier. The amplifier selected for this design has an intrinsic gain of 8.2 V/V.
- The amplified differential signal is then passed through an OP-AMP with unity gain. At this point, the differential measurement obtained earlier is lost.
- The measurement of the DC link voltage can be done in 2 ways:
  - Analog Measurement
  - Digital Measurement

  The analog measurement method has been chosen.
- For measuring the DC link voltage analogically, the signal obtained from the unity-gain OP-AMP is passed through a differential output amplifier. This helps to obtain a high impedance differential measurement with sufficient noise suppression.
- To interface the measurement circuit with the OPAL-RT controller, a RJ45 connector has been utilized. This is because OPAL-RT controllers communicate very well through ethernet connections.

7.4.5 Grid Current Measurement

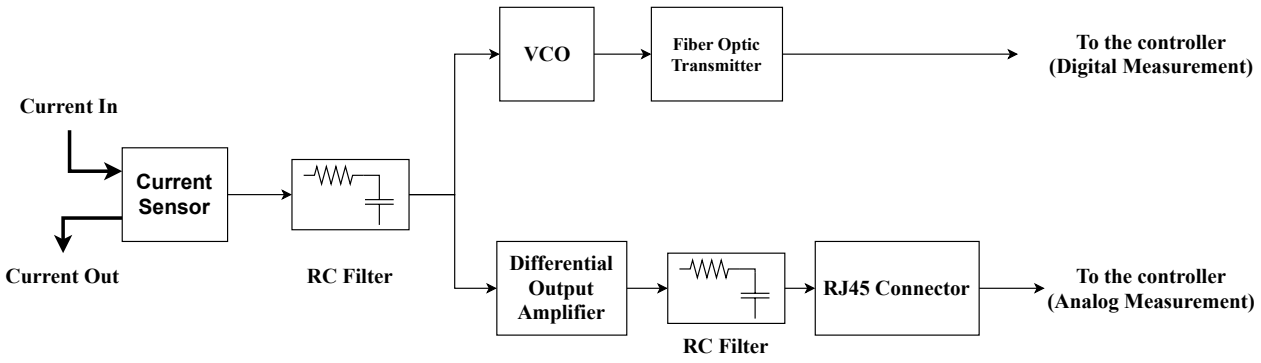


Figure 7.7: Current sensor for measuring the grid current

- The current measurement circuit is similar to the DC link voltage measurement circuit. A coreless hall-effect based current sensor has been utilized for this design. It is capable of measuring currents up to 30 A.
- The output of this current sensor is as follows:
  - 5 V, if current flowing through the sensor is 30 A.
  - 2.5 V, if no current is flowing through the sensor.
  - -5 V, if current flowing through the sensor has been reversed (30 A)

  Similar to the DC link voltage measurement method, the analog measurement has been chosen with the differential output amplifier and RJ-45 connector.

7.4.6 Global Shutdown and Enable

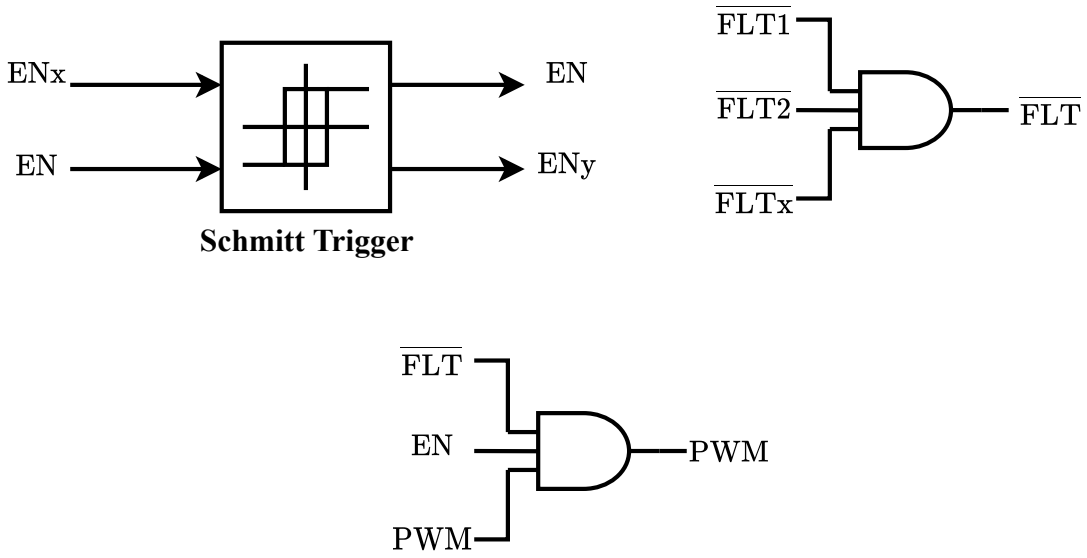


Figure 7.8: Logic for implementing global shutdown and enable functionality

- As mentioned before, the MOSFET gate driver IC, is equipped with an $\overline{\text{FLT}}$ pin.
- Each sub module consists of 4 independent $\overline{\text{FLT}}$ pins. In this design, $\overline{\text{FLT}}$ pins of the gate drivers of a single half bridge are tied together. These are represented by signals $\overline{\text{FLT1}}$ and $\overline{\text{FLT2}}$, indicating $\overline{\text{FLT}}$ signals of the left half bridge and right half bridge respectively. An additional enable signal, EN has been added to provide blocking functionality for PWM signals.
- The fault signals are fed to a 3 input positive AND gate that generates the resultant $\overline{\text{FLT}}$ signal for the sub module where, signal $\overline{\text{FLTx}}$ is the resultant $\overline{\text{FLT}}$ signal obtained from the previous sub module.
- This resultant $\overline{\text{FLT}}$ signal along with the EN signal is associated with every PWM signal with the help of AND gates.
- To transmit $\overline{\text{FLT}}$ and EN to other sub modules, two 3 x 1 male headers are provided on the board. One of the headers is utilized for acquiring signals from the previous sub module, while, the other is utilized to send the signals to the next sub module. ENx represents the enable signal obtained from the previous sub module while, ENy represents the enable signal sent to the next sub module.

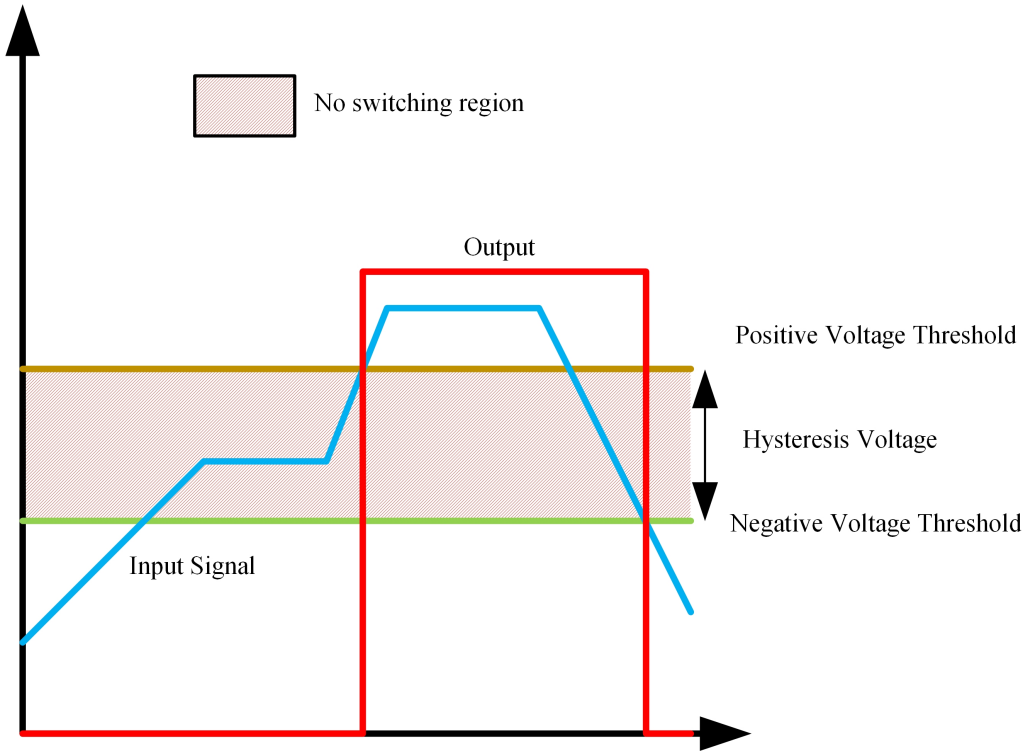


Figure 7.9: Working of a non-inverting Schmitt trigger

- Note, that the enable signals that are being sent and received are first fed to a non-inverting Schmitt trigger. A Schmitt trigger introduces a voltage hysteresis enveloped by the positive threshold voltage and the negative threshold voltage as shown in Figure 7.9.
- The function of this Schmitt trigger is to avoid oscillations in the signals caused due to noise. This is achieved by the hysteresis voltage region where no switching occurs.
- For a supply voltage of 5.5 V, the Schmitt trigger chosen for this design has a positive threshold voltage of 2.88 V and a negative threshold voltage of 1.68 V. This means that if the voltage of the EN signal falls from 5 V to 2 V, it will retain its previous output until, the voltage drops below 1.68 V. This avoids false blocking of PWM signals.

7.5 PCB design and assembly

The PCB are designed on Altium Designer 21. The gate driver board has been designed on a 2 layer PCB while, the power board has been designed on a 4-layer PCB.

7.5.1 Gate Driver Card

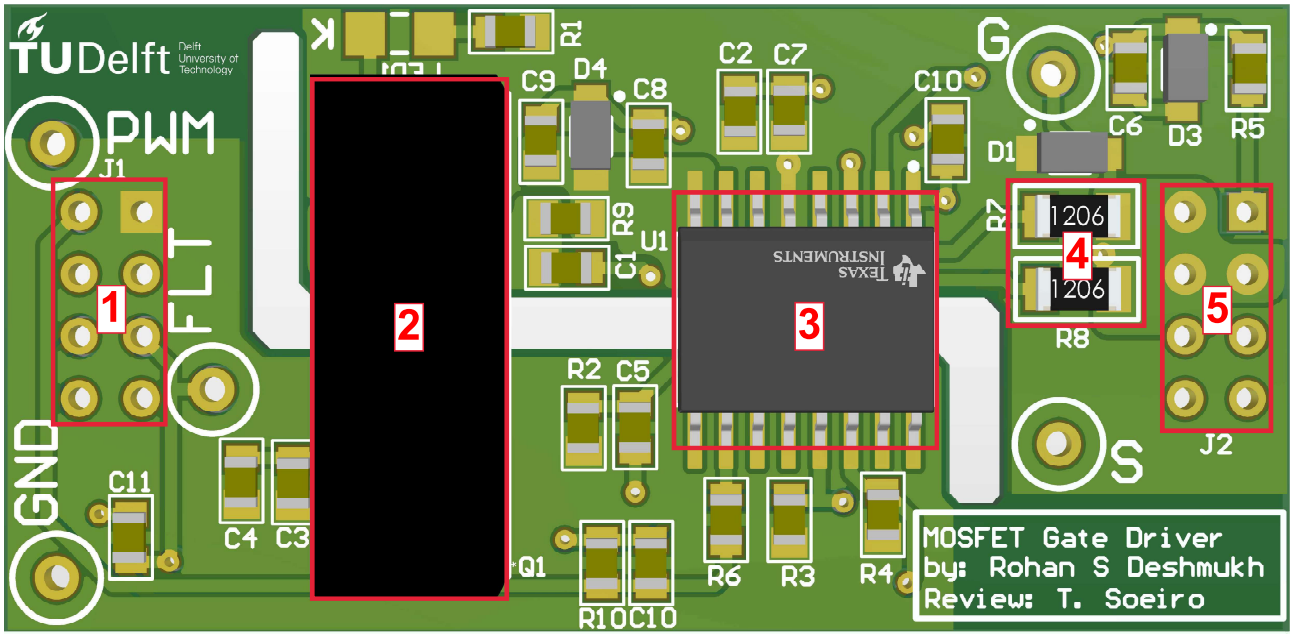


Figure 7.10: 3D view of the driver card

With reference to the annotations provided in Figure 7.10,

1. I/P stage of the driver card.
2. Isolated DC/DC converter 5 V/±15 V.
3. Gate driver IC, ISO5852S DWR.
4. Gate resistors.
5. O/P stage of the driver card.

7.5.2 Power Board

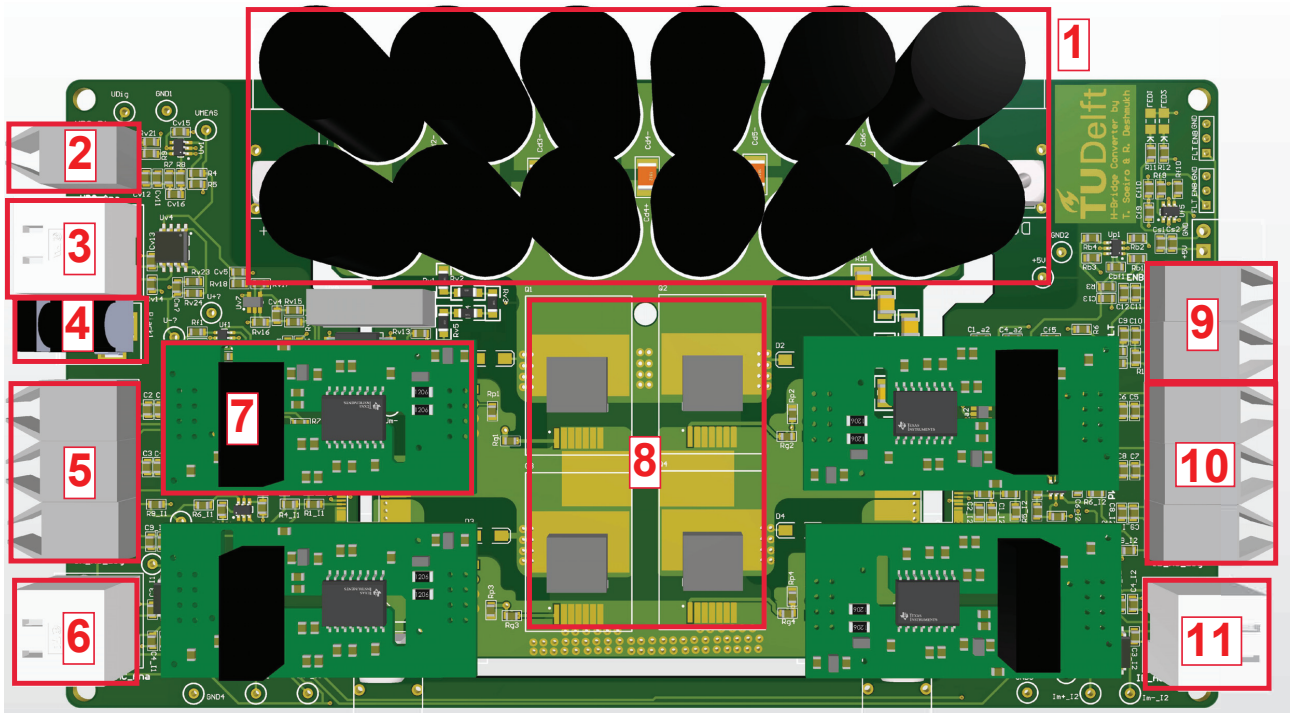


Figure 7.11: 3D View (Top View)

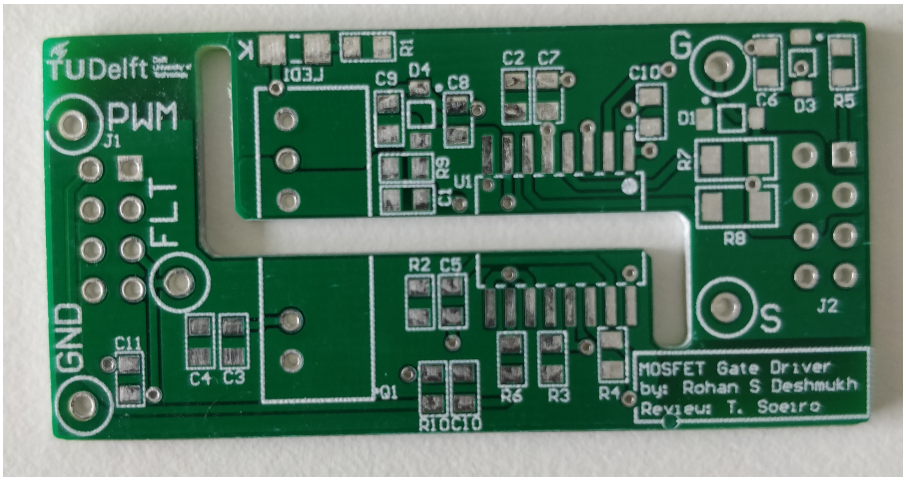
With reference to the annotations provided in Figure 7.11,

1. DC link (Positive DC bus on the left).
2. Optic transmitters for digital DC link voltage measurement.
3. Analog DC link voltage measurement.
4. Global 5 V power supply.
5. Optic receivers for PWM inputs of left H-bridge, and optic transmitter for digital grid current measurement.
6. Analog grid current measurement.
7. Gate driver card.
8. H-bridge
9. Optic transmitters for acquiring global $\overline{\text{FLT}}$ and $\overline{\text{RST}}$ signals from the gate drivers.
10. Optic receivers for PWM inputs of right H-bridge, and optic transmitter for digital grid current measurement (optional).
11. Analog grid current measurement (optional)

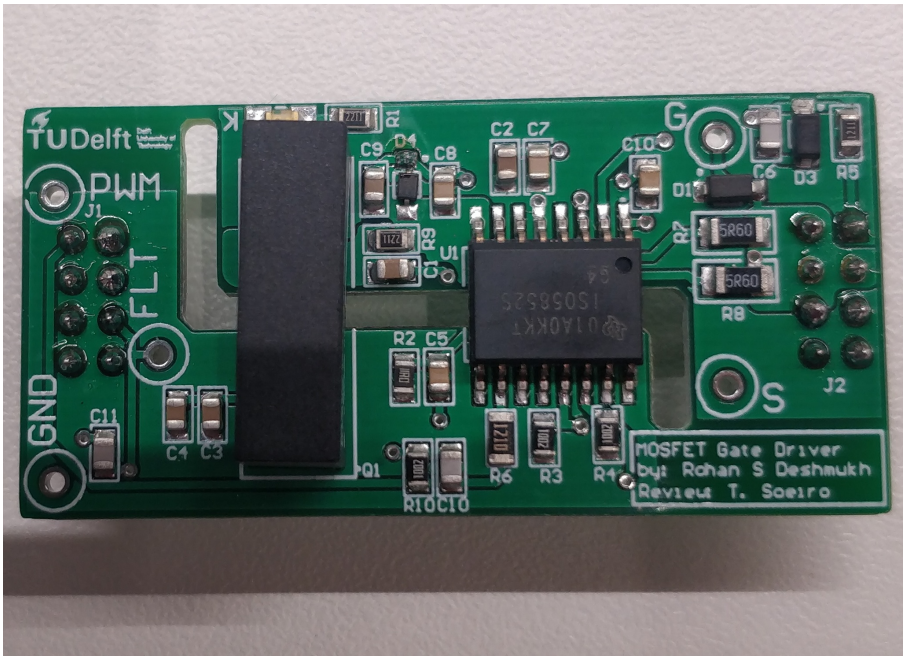
7.6 PCB Assembly

- Majority of the components selected for the prototype are surface mount components. As a result, a PCB stencil printer was used. Stencils of both the PCB boards were designed and were utilized to place the soldering paste on the pads of the SMD components.
- The soldering process begins with the careful placement of the surface mount components. After successfully placement of all SMD components, they were soldered with the help of hot air. This is followed by soldering of through-hole components.
- After soldering all the relevant components of the prototype, an inspection of the PCB was carried out. This is done so as to check for pads that have not been soldered properly to the component or there is short between 2 pads due to excess solder paste. Potential areas of problems were fixed with hand-soldering

7.6.1 Gate Driver Card



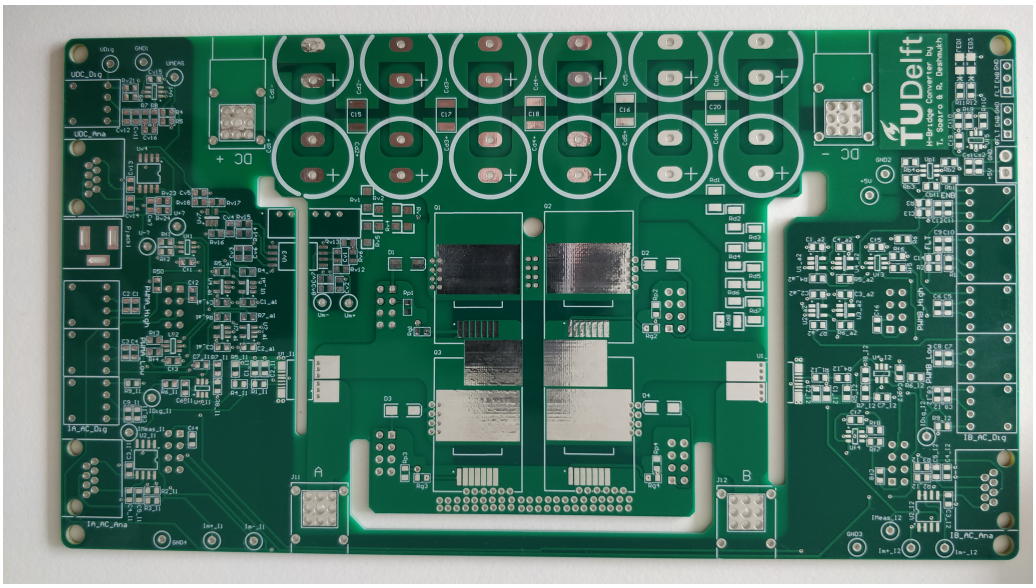
(a) Fabricated Driver Card PCB



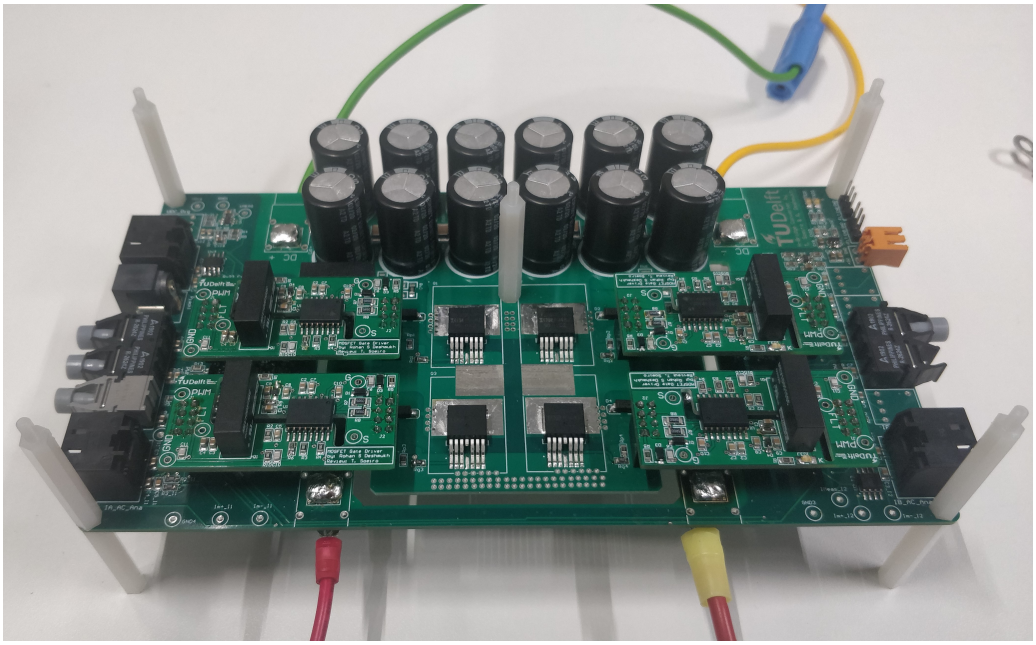
(b) Assembled Driver Card PCB

Figure 7.12: Driver Card

7.6.2 Power Board



(a) Fabricated Power Board



(b) Assembled Power Board

Figure 7.13: Power Board

7.7 Conclusion

In this chapter, the design of the hardware prototype was carried out. This was initiated by creating a general layout of the prototype. Implementation of modularity in the prototype was carried out by dividing the prototype into 2 PCB boards: Driver Card and Power Board. The design of the gate driver card was carried out first. Important remarks for the PCB design of each component of the gate driver card are provided with the schematics. Similarly, several sections which form the power board PCB have been explained in brief along with general block diagrams for the sake of simplicity. The gate driver and power board are fabricated followed by assembly of relevant components.

Chapter 8

Hardware Tests and Results

8.1 Introduction

In the previous chapter, the PCB design and assembly of the hardware prototype was carried out. This chapter has been divided into 2 parts. In the first part, the testing of the driver card and the power board was carried out. This was followed by computation of the converter efficiency. The results obtained are validated with the theoretical results.

8.2 The Gate Driver Setup

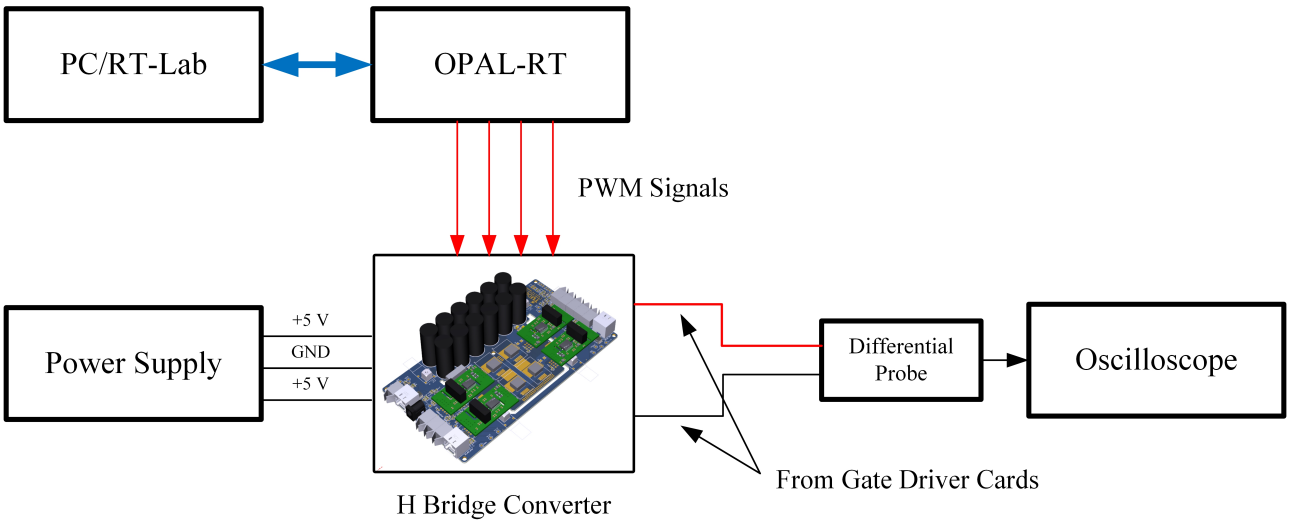


Figure 8.1: Gate Driver Test Setup

The test setup is as follows:

1. The gate driver cards are mounted on the power board.
2. The board is energized with 5 V with the help of adjustable lab bench power supply. Note, that only the low voltage section of the board has been energized here.
3. The powering up of the gate driver cards has been indicated with the help of an LED present on each card.
4. As mentioned in Chapter 7, the converter is equipped with Global Shutdown and Enable Logic. Since, only a single H-bridge is tested, they need to be bypassed. In order to achieve this, the $\overline{\text{FLT}}$ and EN pins of the board are energized with 5 V.
5. The OPAL-RT is programmed with the help of RT-LAB and MATLAB. The generation of reference modulating signal is based on Equation 6.2. It is connected to the PWM OUT block provided by the RT-LAB Simulink Package.

6. The function of this block is to generate the required PWM signals as a function of the duty ratio (I/P).

7. The following parameters were configured for the block:

Parameter	**Value**
Number of PWM Signals	2
Polarity	Active High
Carrier Wave Mode	Symmetric
Output Complementary Channels?	Yes
Carrier Delay	[0 0]
Dead Time	200 ns

Table 8.1: PWM OUT block configured parameters

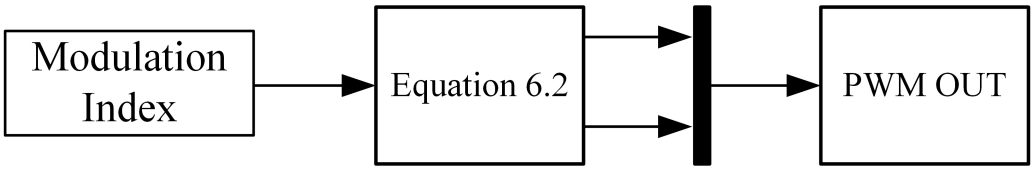


Figure 8.2: Simulink model for gate driver test using OPAL-RT Blocks.

8. As mentioned earlier, the prototype acquires PWM signals with the help of fiber optic receivers. The PWM signals are fed to the Digital Out Port located behind the controller. To convert these signals into fiber optic signals, an interface card has been utilized as shown in Figure 8.3a. This interface card converts the digital PWM signals obtained from the controller into light with the help of optic fiber transmitters located on the interface card. These PWM signals are then transmitted to the prototype with the help of fiber optic cables.

9. To enable real time operation of the controller, RT-LAB has to perform the following 3 steps:

   (a) Build

   (b) Load

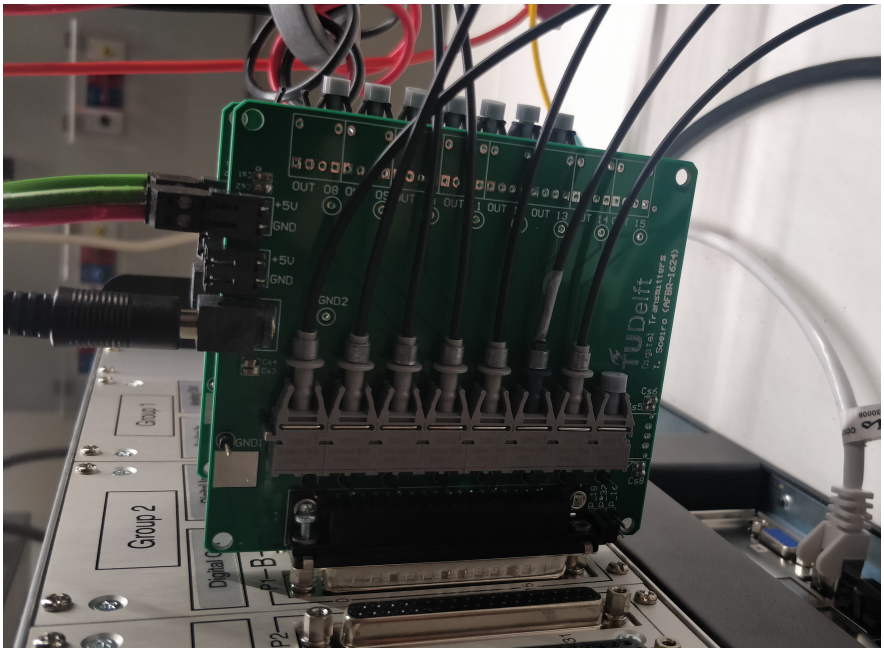
   (c) Execute

10. OPAL-RT controllers have their independent operating systems. They work either on Linux or Windows. The controller utilized here is based on the Linux Operating System.

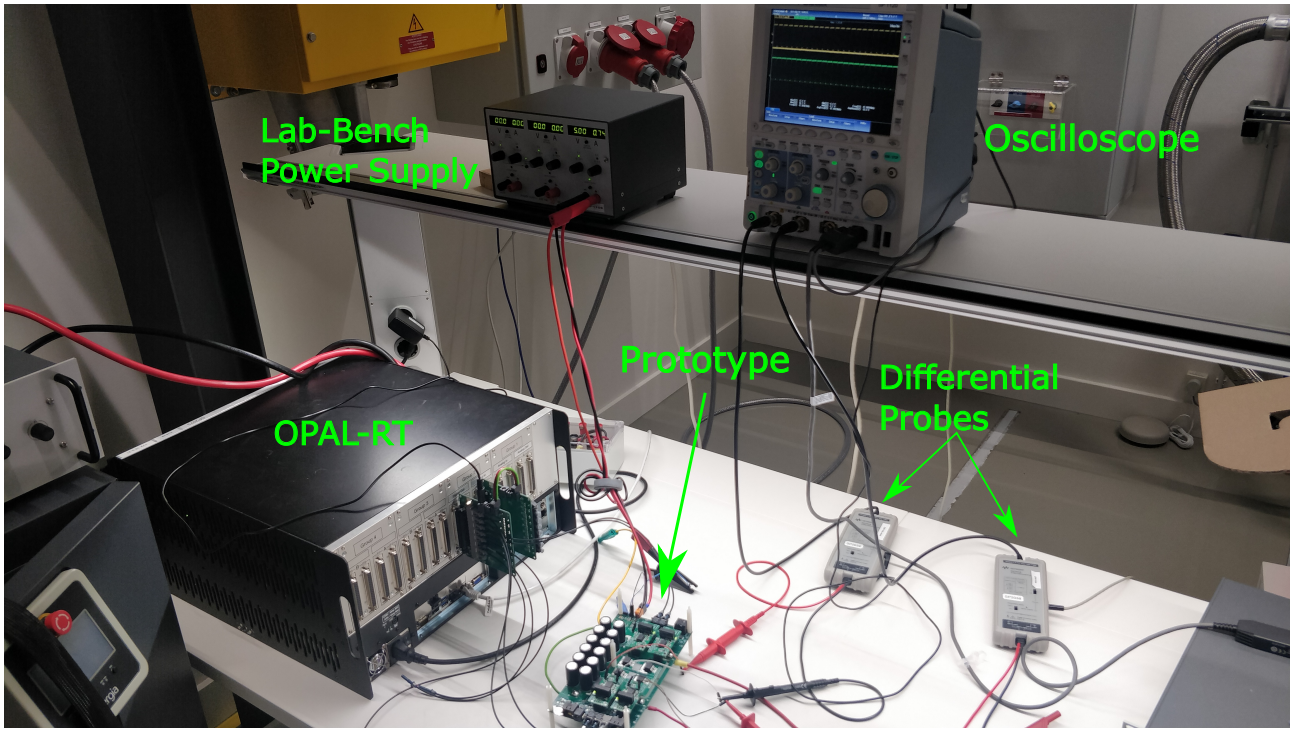
11. The **Build** command, essentially, utilizes Simulink's Code Generation functionality to convert the model into a Linux executable. The **Load** command, as the name suggests, loads the generated Linux executable of the model onto the controller. Here, the bit stream file is flashed on the controller for giving the information regarding the I/O that have been utilized by the application. At the end of this process, RT-LAB makes the controller ready for real-time operation. The final command, **Execute** activates the real-time operation of the controller allowing it to send PWM signals at the required Digital Out Port.

12. Each gate driver card has testing points for measuring the gate-source voltage. This voltage is measured with the help of differential probes and studied with the help of an oscilloscope.

13. The complete setup has been shown in Figure 8.3b.



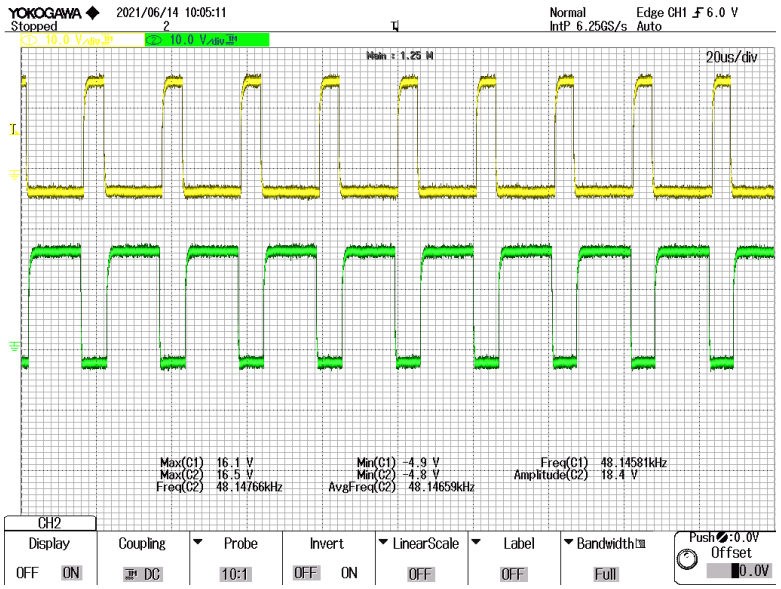
(a) Optic Fiber Interface Card for OPAL-RT



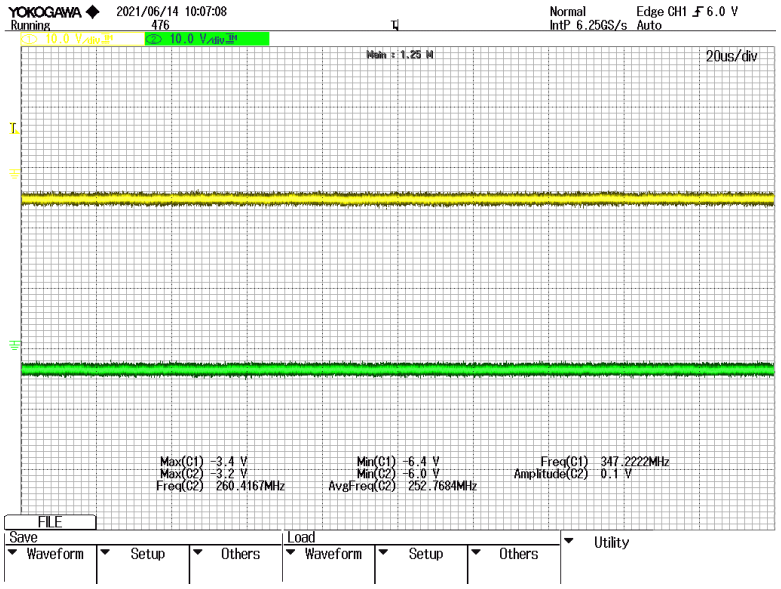
(b) The Complete Setup

Figure 8.3: Gate Driver Test Setup

8.2.1 Gate Driver Test Results



(a) Nominal Operation



(b) Triggering of Fault Logic

Figure 8.4: Gate Driver Test Results

Observations

- Figure 8.4 shows the gate-source voltages of one of the half-bridges. It is evident from Figure 8.4a, that both PWM signals are complementary.
- The usage of bipolar driver supply is evident from the maximum and minimum values of the gate-source voltage, i.e. 16.1 V and -4.9 V.
- Upon closer inspection, the dead time between the PWM signals has been detected which corresponds to approximately 200 ns as defined in the PWM Out Block in the Simulink model.
- To verify the Global Shutdown and Enable Logic, the $\overline{\text{FLT}}$ signal was grounded indicating that a fault has occurred. The response is shown in Figure 8.4b. It is evident from this response that the logic is working correctly where the gate-source voltage is brought down to -4.9 V ensuring that all the semiconductor switches remain OFF.

8.3 Open Loop Efficiency Test

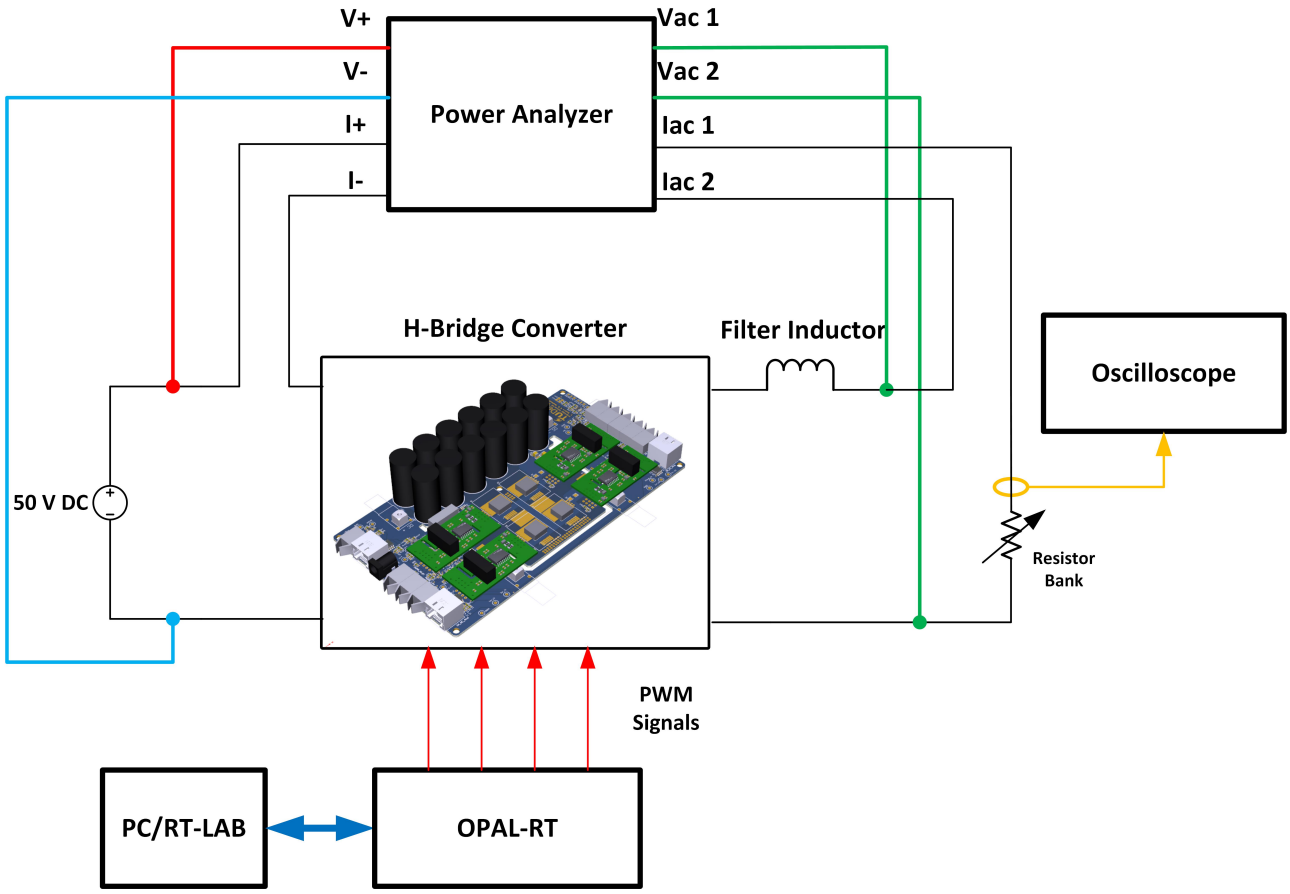


Figure 8.5: Setup for open-loop efficiency test

The test setup is as follows:

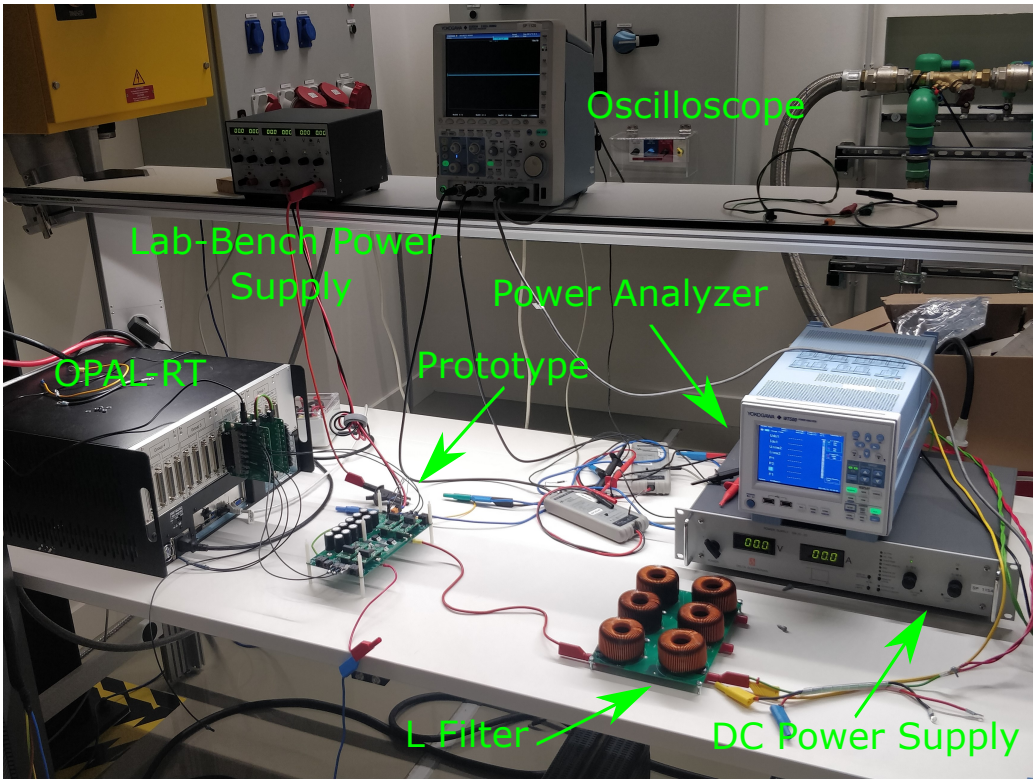
1. The previous setup for testing the gate driver illustrated in Figure 8.1 is retained. However, the energization of the power circuit is required in this test and therefore, Figure 8.5 shows the additional connections that need to be made. The DC link is energized by an adjustable DC Power Supply which is capable of delivering up to 70 V and 22 A. In this setup, it has been set to 50 V with the current limited to 5 A.

2. A power analyzer has been utilized for this test. It is a tool that helps in accurately measuring the voltage and current at the I/P and O/P stages of the converter so as to calculate the efficiency. In this setup, the DC link voltage and the DC link current is measured at the I/P stage.

3. The terminals of the converter are connected to an L filter having an inductance of 740 μH. This is followed by connecting it to the power analyzer for measuring the load voltage and current.

4. The load utilized for this test is a resistor bank consisting of 2 rheostats capable of providing a resistance up to 70 Ω and rated for 5.2 A. The load current is acquired with the help of current probe respectively and are studied with the help of an oscilloscope.

5. To calculate the filter losses, the resistive component of the filter needs to be determined. This is done with the help of an impedance analyzer. At fundamental frequency, the resistance of the filter was found to be 92.53 mΩ.



(a) The Complete Setup

(b) Load

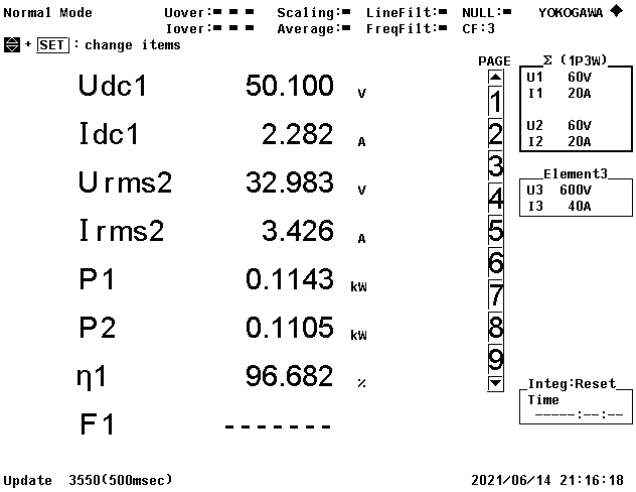
Figure 8.6: Open-Loop Efficiency Test Setup

The converter is operated at 3 unique operating points. The load is varied such that the required operating point is achieved by the converter. To measure the efficiency of the converter, it needs to be operated at the highest possible modulation index, i.e. $m_a = 0.99$. This results in a terminal voltage of 49.5 V. Table 8.2 shows the required value of resistance along with the load current for attaining different operating points.

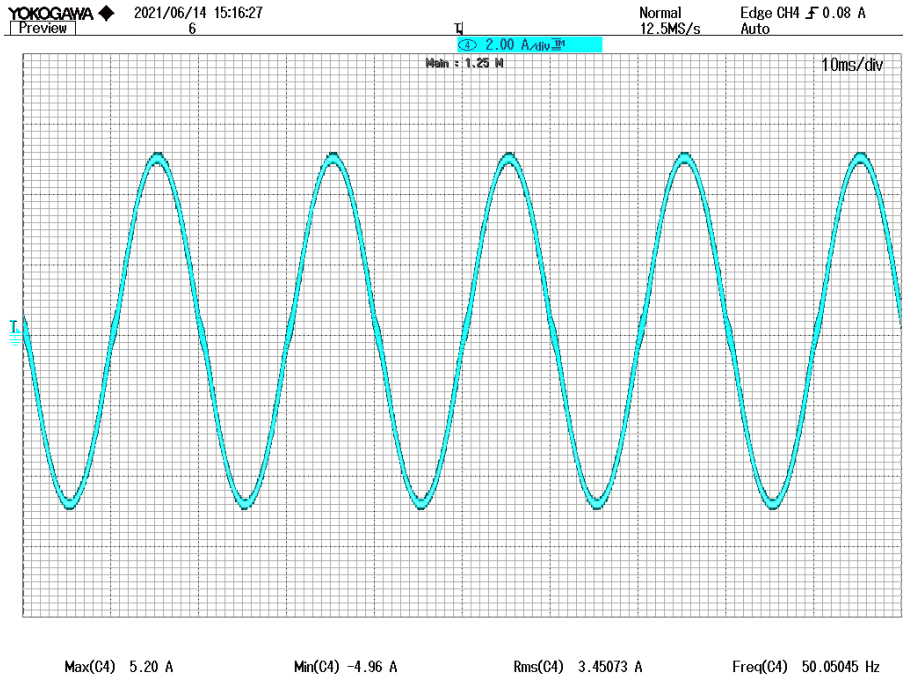
% Loading	Load Current	Resistance
50 %	5.05 A	10 Ω
75 %	7.58 A	7 Ω
100 %	10.1 A	5 Ω

Table 8.2: Load Values for Open-Loop Efficiency Test

8.3.1 Open-Loop Efficiency Test Results

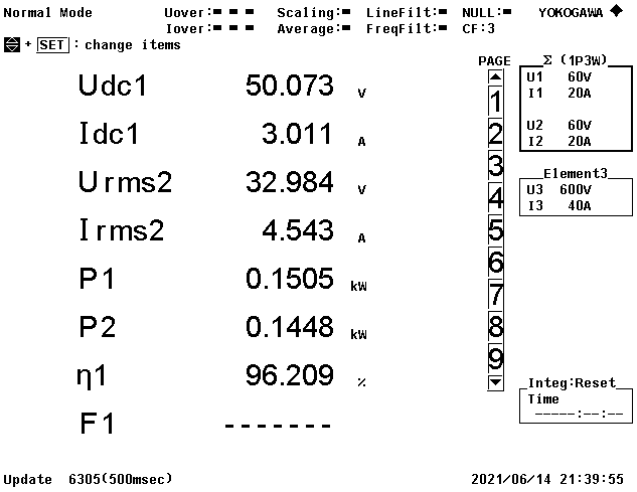


(a) Power Analyzer Results

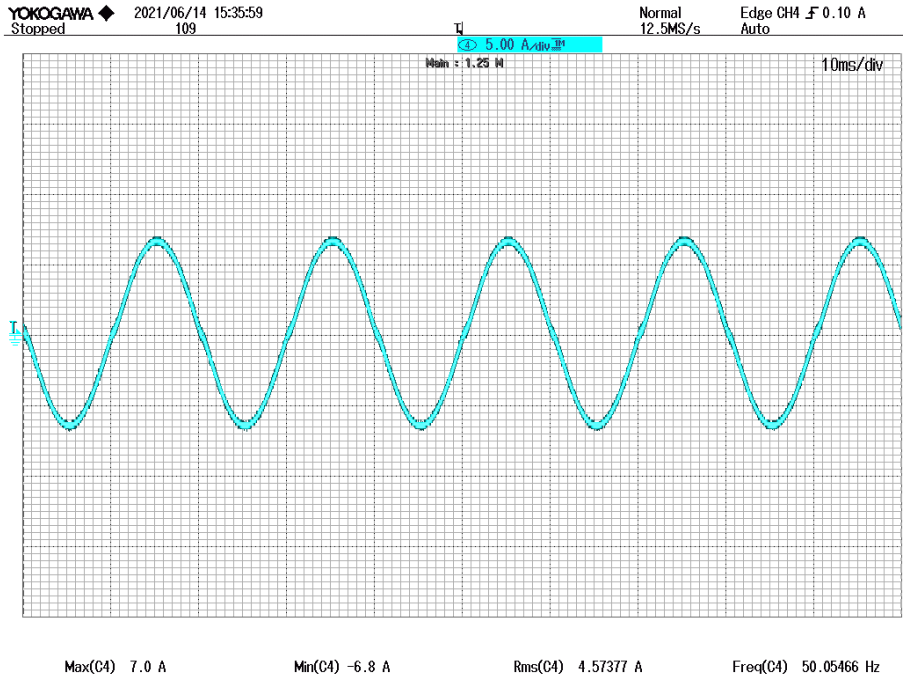


(b) Load Current

Figure 8.7: 50 % Loading

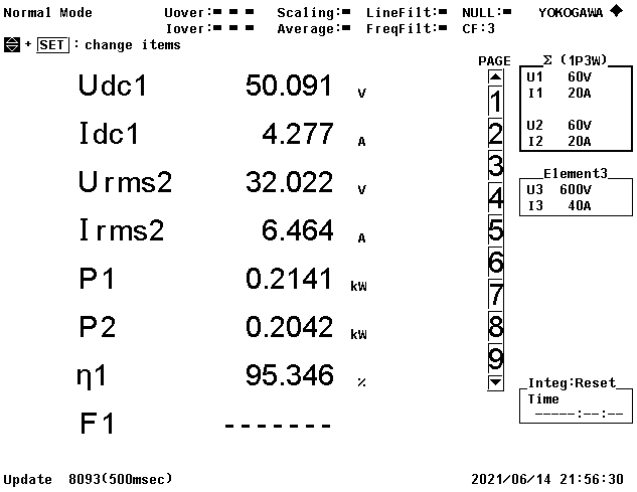


(a) Power Analyzer Results

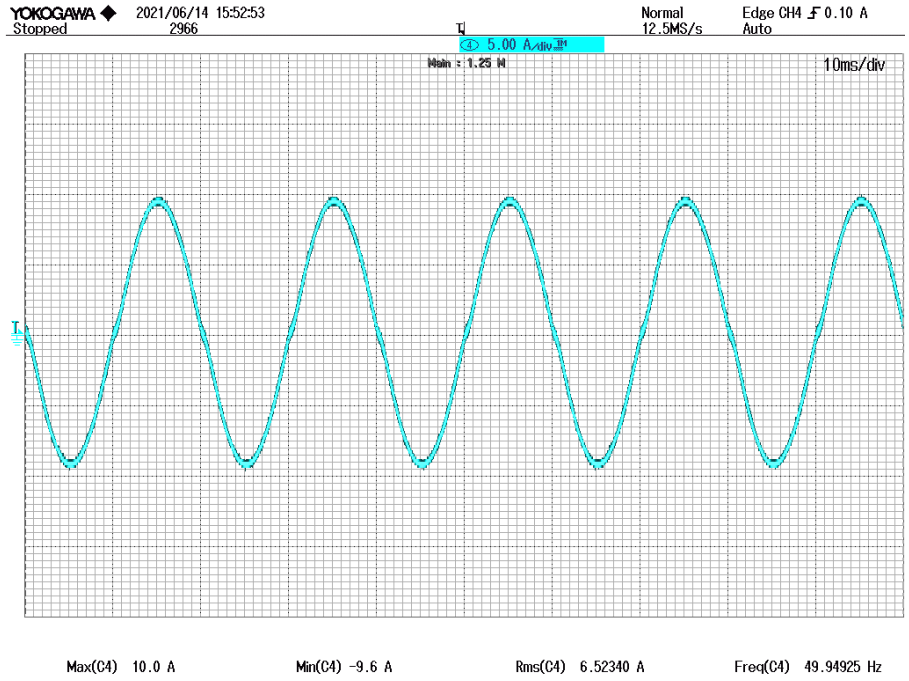


(b) Load Current

Figure 8.8: 75 % Loading



(a) Power Analyzer Results



(b) Load Current

Figure 8.9: 100 % Loading

Observations

- Figures 8.7, 8.8 and 8.9 shows the open-loop efficiencies measured by the power analyzer and load currents at 3 operating points of interest.
- The peak values of load currents of the converter obtained at different operating points are in accordance to the theoretically calculated load currents shown in Table 8.2 with minor differences. Similarly, the terminal voltage of the converter remains constant at all 3 operating points and also corresponds to the RMS terminal voltage of 35 V at m_a = 0.99.
- On the other hand, the efficiencies determined by the power analyzer, also takes into account the filter losses. Therefore, we need to recalculate the efficiencies without taking the filter losses into account. From the perspective of harmonic performance, the currents are sinusoidal and contain no additional harmonics.

- The theoretical efficiency and the hardware efficiencies were calculated without taking the filter losses into consideration. Table 8.3 and Table 8.4 provides efficiencies calculated for both the cases.

% Load	Input Power, P_{in}(W)	Output Power, P_{out}(W)	Efficiency, η
50%	125 W	118.52 W	94.8%
75%	187.5 W	177.72 W	94.8%
100%	250 W	236.86 W	94.7%

Table 8.3: Theoretical Efficiency of the prototype

% Load	Input Power, P_{in}(W)	Output Power, P_{out}(W)	Efficiency, η
50%	114.3 W	111.58 W	97.62%
75%	150.5 W	146.70 W	97.48%
100%	214 W	208.06 W	97.18%

Table 8.4: Practical efficiency of the prototype

- Figure 8.10 shows the trends of both theoretical and hardware efficiencies of the converter. It is evident from the trend that the theoretically calculated losses have been over-estimated due to the fact that certain parameters which are crucial for calculating the switching losses such as:
  - Turn on delay time.
  - Rise time.
  - Turn off delay time.
  - Fall time.

  are obtained at test conditions mentioned by the manufacturer in the data sheet. These conditions do not correspond with the conditions set during this experimental test. This causes a difference in the efficiency by approximately 2.5 % at full load.

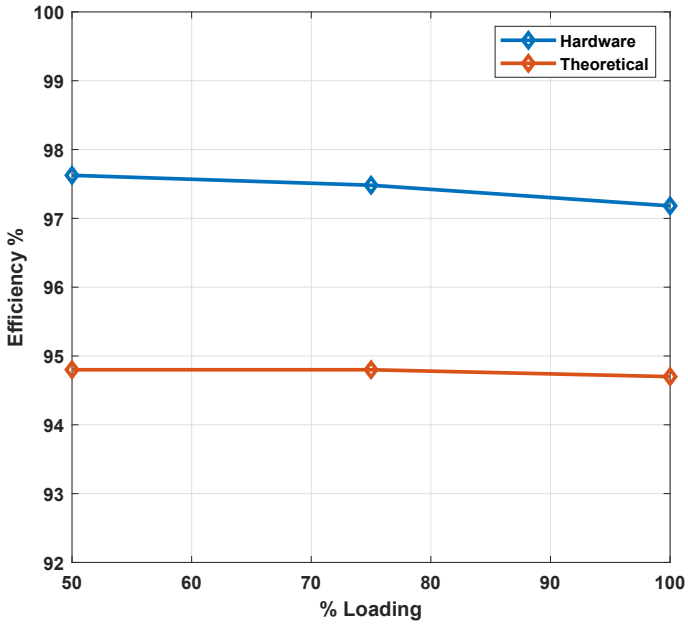


Figure 8.10: Comparison of Theoretical and Practical efficiency of the prototype

Chapter 9

Conclusions and Future Work

9.1 Conclusions

With reference to the research questions provided in Section 1.2,

1. **What are the benefits of utilizing a microinverter in contrast to utilizing string and centralized inverter configurations for residential PV systems?**

    - The most commonly used PV inverters were the string and centralized inverters. However, they presented lot of challenges with regards to system efficiency such as partial mismatch and, higher capital cost. However, microinverters prove to be a suitable candidate for the application as they allow each PV panel to operate independently and eliminate the problems of partial mismatch offered by string and centralized inverters.
    - Microinverters were classified on the basis of number of power conversion stages and galvanic isolation. Single stage microinverters offered compact design and high conversion efficiency, however, lead to an increase in the control complexity. On the other hand, double/multi-stage microinverters, allowed independent control of the conversion stages leading to simpler control design. Microinverters with galvanic isolation offered protection against leakage currents which need to be investigated for a transformerless topology. However, addition of a line-frequency transformer would not only make the system bulky but, also would increase the cost of the system. Therefore, it was evident that a non-isolated double stage topology would be selected with the focus on the DC/AC conversion stage.

2. **What are the various features offered by state of the art microinverter topologies? How can the benchmarking of the right microinverter solution be carried out among the investigated topologies?**

    - Several non-isolated double stage topologies contained split capacitor arrangements to mitigate the effects of leakage currents. However, this would require usage of HV capacitors and a higher switching frequency. On the other hand, some of the topologies incorporated additional switches in order to freewheel the leakage current thereby preventing it from interacting with the PV module. At this stage, the cascaded topologies of microinverters were investigated.
    - Cascaded topologies offered several advantages such as redundant switching states, lower switching frequency and better efficiency. At this stage, it was decided that a non-isolated double stage microinverter will have a cascaded DC/AC topology. 3 cascaded topologies were shortlisted and were judged on the basis of 5 criteria: THD, efficiency, leakage current suppression, modularity and scalability. At the end of this analysis, it was found that the cascaded H-bridge topology proves to be a suitable candidate for this application.

3. **How can the design, modelling and control of such a microinverter be carried out? What are the approaches utilized for controlling the grid current in such converter? How are they different from each other?**

   - The next phase was to initiate the design of CHB converter by determining important parameters such as minimum DC link voltage, number of cells, DC link capacitance, power conditioning and switching frequency. The designing was carried out for 2 variants: Lab-scale model and the Large-scale model. This was followed by developing a mathematical model and control system design of the converter. The modelling of the converter was carried out by utilizing the state-space approach and the concept of switching functions. The usage of mathematical model served 2 merits:
     - The model was very fast compared to the model containing the semi-conductor switch models.
     - To allow controller tuning faster.
   - The verification of the converter mathematical model was followed by the control system design. Current controllers were studied with 2 approaches i.e. PI and PR controllers. It was proved through simulations that a PI controller was inherent to amplitude and phase errors and therefore, PR controllers delivered superior performance with the ability to provide harmonic compensation. The DC link voltage controller was studied with the help of state-space approach, by developing the DC link model. Both controller responses were tested and verified with the help of the plant model. The controllers were discretized using the ZOH approximation.
   - The next phase involved the simulation of the complete system. The current controller was tested independently followed by addition of the DC link voltage controller. This was followed by the nominal operation of the system, at unity power factor. Harmonic performance of the system indicated that 3^{rd}, and 5^{th} harmonics need to be compensated and therefore, resonant compensators were added to the PR controller. This resulted in a THD of 0.11 %.
   - After successful verification of the control system with simulations, the selection of components and loss calculation was carried out. The semiconductor switch and the gate driver were selected on the basis of certain criteria. A systematic approach for calculating the losses in both these components was followed. The theoretical efficiencies of the system was computed for the chosen switch and gate driver for 7 unique operating points. These operating points were used for computing the Euro efficiency and the CEC efficiency.

4. **How can the hardware design of such a microinverter be carried out? How to test and evaluate the performance of such a prototype?**

   - Acceptable efficiencies of the system allowed to initiate the design of the hardware prototype. A general layout indicating the positions of different sections of the prototype was made. The prototype was divided into 2 parts: Driver Card and Power Board. The design of the gate driver card was carried out first. Important remarks about the design were discussed in detail. After acceptable positioning of all the components on the PCB, the design files were submitted for fabrication. The PCB boards were first applied with the solder paste by utilizing a PCB printer for placing the surface mount components which were soldered with the help of hot-air. A thorough inspection of the soldered PCB was carried out and potential problems were identified and solved with the help of hand soldering.
   - The final phase of this thesis, was to test the prototype and validate it with the simulation results. The testing phase was divided into 2 parts: Gate driver testing phase and power board testing phase. OPAL-RT controller was utilized for controlling the hardware prototype. The workflow of how an OPAL-RT controller enters the real-time operation mode has been explained in detail along with a simple block diagram for the gate driver test-setup.
   - The results of gate-driver setup not only indicated that the gate-signals are correct with suitable dead-time and maximum and minimum values but, also helped in verifying that the Global Shutdown and Enable logic implemented in case of a fault, blocks the PWM signals ensuring that the semiconductor switches remain OFF. On the other hand, the testing of the power board and the open-loop efficiency test was carried out at the same time. The open-loop efficiency involved utilizing the power analyzer to compute the efficiency of the prototype by operating the same at 3 operating points with the help of a resistive load.

- Results indicated that the prototype achieved an efficiency of over 97 % as opposed to the theoretically calculated efficiency of 95 %. This can be justified by the fact that there was an overestimation in the loss calculation since, parameters given the data sheet correspond to the test conditions that were not set during this experimental test. However, the results obtained from this test were sufficient enough to consider that the converter design and efficiencies are acceptable.

9.2 Future Work

Potential research in the future can be based on the following topics:

- Measure the leakage current and propose methods to mitigate the same so as to reduce conductive EMI.
- As mentioned in Chapter 1, the focus of this thesis was to design the DC/AC stage of the double stage non-isolated microinverter. A potential extra project can be designed which requires the design of DC/DC stage for this microinverter.

Appendix A

A.1 Filter inductor design calculation

The data utilized for design calculations has been obtained from Table 6.4, 6.5a, & 6.5b. Detailed design steps has been shown for the filter design of the 5-level CHB converter. Similar steps can be followed for 19-level CHB converter filter design.

A.1.1 Design Steps

- **Step-1: Calculate the minimum number of turns**

$$N_{\text{min}} = \frac{L_{\text{f}} \cdot I_{\text{max}}}{B_{\text{sat}} \cdot A_{\text{c}}} \tag{A.1}$$

$$N_{\text{min}} = \frac{75 \times 10^{-6} \times 13.52}{380 \times 10^{-3} \times 280 \times 10^{-6}}$$

$$\boxed{N_{\text{min}} = 10 \text{ turns}}$$

where,

$$I_{\text{max}} = \hat{I}_{\text{g(nom)}} + \frac{\Delta i_{\text{ripple}}}{2} \tag{A.2}$$

- **Step-2: Determine maximum flux density, $B_{\max}$**

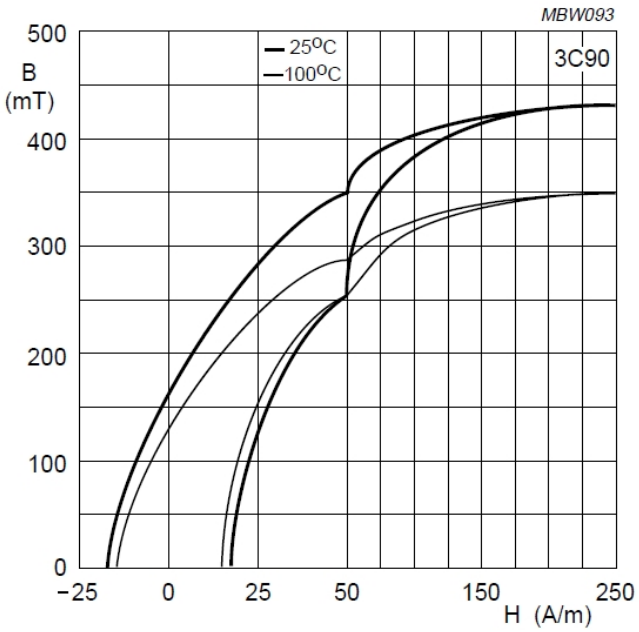


Figure A.1: B-H Characterisitics of 3C90

The selection of the maximum flux density must be made such that it is at the knee region of the B-H curve charactersitics of the chosen core material. Having a very small maximum flux desity increases the air gap required as well as increases the number of turns for the same inductance. On the other hand, selecting a very large value, would lead to core saturation.

$$\boxed{B_{\max} = 270 \text{ mT}}$$

- **Step-3: Determine air-gap length**

$$\frac{L_{\mathrm{f}} \cdot I_{\max}^2}{2} = \frac{B_{\max}^2 \cdot A_{\mathrm{c}} \cdot l_{\mathrm{g}}}{2 \cdot \mu_0}$$

$$l_{\mathrm{g}} = \frac{L_{\mathrm{f}} \cdot I_{\max}^2 \cdot \mu_0}{B_{\max}^2 \cdot A_{\mathrm{c}}} \tag{A.3}$$

$$\boxed{l_{\mathrm{g}} = 0.85 \text{ mm}}$$

- **Step-4: Determine number of turns**

$$N = \sqrt{\frac{L_{\mathrm{f}} \cdot \left(l_{\mathrm{m}} + \left(\mu_{\mathrm{r}} - 1\right) \cdot l_{\mathrm{g}}\right)}{\mu_0 \cdot \mu_{\mathrm{r}} \cdot A_{\mathrm{c}}}} \tag{A.4}$$

$$\boxed{N = 14 \text{ turns}}$$

- **Step 5A: Determining the conductor cross-sectional area**

  The RMS current flowing through the winding is given by,

$$I_{\text{rms}} = \frac{I_{\text{max}}}{\sqrt{2}} \tag{A.5}$$

$$\boxed{I_{\text{rms}} = 9.56 \text{ A}}$$

  Considering current density, J = 4 A/mm^2, the bare conductor cross-sectional area is given by,

$$A_{\text{bare}} = \frac{I_{\text{rms}}}{J} \tag{A.6}$$

$$\boxed{A_{\text{bare}} = 2.4 \text{ mm}^2}$$

  The minimum cross-sectional area of the conductor required to ensure that the current density is below 4 A/mm^2 is **2.4 mm**^{2}
  Therefore, based on the American Wire Gauge Table (AWG) shown in [60], the AWG 13 conductor was chosen.

Parameter		**Value**
Material		Copper
Bare cross-sectional area	A_{bare}	2.63 mm^2
Resistance		6.56 Ω/Km

Table A.1: Conductor selected for the inductor winding

  Therefore, recalculating the current density with Equation A.6 we have,

$$\boxed{J_{\text{new}} = 3.63 \text{ A}}$$

- **Step 5B: Estimate window utilization factor**

  Note, that the conductor cross-sectional area considered in the previous step did not take into account the insulation thickness of the conductor. Therefore, According to [61], a **heavy build AWG 13 copper wire** would have maximum diameter of **1.923 mm**. Therefore, the corresponding cross-sectional area considering the insulation was found to be,

$$\boxed{A_{\text{wind}} = 2.9 \text{ mm}^2}$$

  The window utilization factor can therefore be calculated,

$$k = \frac{A_{\text{wind}} \cdot N}{A_{\text{w}}} \tag{A.7}$$

$$\boxed{k = 0.1286}$$

  Note, that the window utilization factor, typically should lie between 25-30%. A smaller value would imply that the core is too large for the calculated number of turns. On the other hand, a larger value, would imply the core is too small for the required number of turns.
  In this design, a large core has been chosen to ensure that there is a single layer of winding to decrease the proximity losses.

- **Step 6A: Estimate the length of winding**
  The length of the winding can be calculated as follows,

$$l_{\mathrm{w}} = MLT \cdot N \tag{A.8}$$

$$\boxed{l_{\mathrm{w}} = 1.34 \text{ m}}$$

- **Step 6B: Determine resistance of the winding**

$$R_{\mathrm{dc}} = l_{\mathrm{w}} \cdot \text{Resistance} \tag{A.9}$$

$$\boxed{R_{\mathrm{dc}} = 8.7 \text{ m}\Omega}$$

- **Step 7: Determine number of turns per layer**

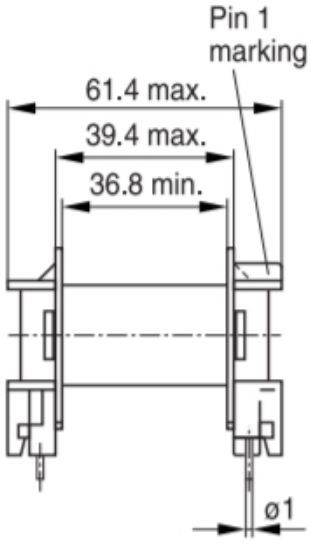


Figure A.2: Coil Former of ETD 54 [55]

Based on the coil former shown in Figure A.2, the length of former, L_{f} on which the windings can be placed is approximately **36.8 mm**. The number of turns per layer can therefore be calculated as follows,

$$\text{Number of turns per layer} = \frac{l_{\mathrm{f}}}{d_{\mathrm{wind}}} \tag{A.10}$$

$$\boxed{\textbf{Number of turns per layer} \approx 19 \text{ turns/layer}}$$

Therefore, the number of turns per layer are greater than the number of turns for the required inductance therefore, this inductor will contain a single layer of winding.

For the 19-level CHB converter filter design, Equations A.1, A.2, A.3, A.4, A.5, A.6, A.7, A.8, A.9, & A.10 can be used. The parameters for the 19-level CHB converter filter are as follows:

Parameter		**Value**
Number of Turns	N	15
Air-gap length	l_{g}	1.3 mm
Winding gauge	AWG	11
Window utilization factor	k	0.21
Length of Winding	l_{w}	1.44 m
Resistance of the winding	R_{dc}	6 mΩ
Number of layers	m	1

Table A.2: 19-level CHB Converter Parameters

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