

Wide-Input-Range Power Conversion for RF Energy Harvesting and Wireless Power Transfer

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WIDE-INPUT-RANGE POWER CONVERSION FOR RF ENERGY HARVESTING AND WIRELESS POWER TRANSFER

WIDE-INPUT-RANGE POWER CONVERSION FOR RF ENERGY HARVESTING AND WIRELESS POWER TRANSFER

Proefschrift

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aan de Technische Universiteit Delft,
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voorzitter van het College voor Promoties,
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door

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SUMMARY

This thesis presents the design and measurement of an RF energy harvesting and power management unit that operates across a wide range of available input power. The system comprises an adaptive impedance matching network, a single-stage cross-coupled differential-drive rectifier, a start-up charge pump, an adaptive buck-boost converter, a Maximum Power Point Tracking (MPPT) circuit and a control loop to regulate the load voltage. The MPPT circuit controls the switching frequency of the buck-boost converter and configures the impedance matching network, optimizing the interfaces between the rectifier and antenna and between the rectifier and the storage capacitor, guaranteeing that the power is being harvested at maximum efficiency. To boost the rectifier output, to accumulate energy in the storage capacitor and to provide energy to the load, a single-inductor buck-boost converter that has two inputs and three outputs is used. Circuit techniques that reduce the power consumption of the control circuits and that allow for adapting the interfaces between the antenna, the rectifier and the load are presented.

In order to introduce adaptability to the circuits while maintaining high power conversion efficiency and high sensitivity, new circuit techniques are introduced. The novel circuits presented in this paper are: a low-power, compact input power estimation circuit employed in the maximum power point tracking (MPPT) circuit, configurable power switches employed in the DC-DC converter, and a high-speed low-power zero current detector also employed in the DC-DC converter. In this thesis we introduce a method of designing optimal multi-stage impedance matching circuit. Furthermore, the proposed system employs an adaptive impedance matching network and a method of regulating the load voltage while performing energy harvesting using a single power inductor.

The designed system operates on input power ranging from -24 to $+15$ dBm. The employed technology is a standard $0.18\mu\text{m}$ CMOS process. It is designed to receive power at the 403.5 MHz center frequency. The peak energy harvesting efficiency is 40.2% at -9.1 dBm available input power and the sensitivity is -24 dBm while producing a 1.8 V output.

1

INTRODUCTION

The term "Internet of Things" (IoT) is used to describe the network of physical devices (or "things"), embedded with electronics, that are able to connect and exchange data through the existing internet infrastructure. It includes, but it is not limited to, vehicles, domestic appliances, smart-building appliances, wearables, and medical devices. The ability to exchange information over the internet augments the functionality of everyday objects, integrating the physical world into computer-based systems, which can improve their efficiency, accuracy, and economic benefit. It is expected that the IoT market size will grow from USD 392 billion in 2020 to about USD 525 billion by 2025 [1]. By the same year, it is estimated that there will be 41.6 billion IoT devices in use [2]. Supplying power to such large number of devices is becoming a problem, especially with the current method of powering those devices, which is using batteries.

The total energy capacity of batteries¹ sold in the world in 1990 was about 2 GWh. It increased to more than 77 GWh in 2018, and it is estimated to be between 600 to 4000 GWh by 2040 [3, 4], part of which is attributed to the IoT market. The sourcing of the necessary toxic chemicals and the production and disposal of the billions of batteries have a negative environmental impact [5], especially considering that not all batteries are properly recycled at the end of their life [6].

There is work being done in three fronts that help to overcome this issue. The first one is in battery development and disposal. There are new techniques to increase the lifetime of batteries, to reduce the pollution and materials needed to fabricate them, and to enhance the recycling process [7–9]. The second one is in power consumption reduction in the electronics, in which the focus is how to reduce the energy needed to perform a given task and, therefore, to increase the battery lifetime. Research is being done to improve power efficiency in different aspects of a device, from the perspective of systems and software to the level of circuit design and device fabrication [10]. The last one is in the development of energy harvesting techniques.

Energy harvesting is an alternative to batteries. It is also an enabling technology for powering devices that are difficult or inconvenient to access with wires, such as in

¹Only lithium-ion batteries are considered. However, they take more than 90% of the battery market [3].

several biomedical, infrastructure monitoring, and industrial applications. Energy harvesting can reduce cost, since battery replacement is expensive in the deployed wireless sensor networks or medical devices implanted in the body. Another potential benefit is the form factor reduction, since batteries tend to be larger in order to provide longer lifetimes [11]. Therefore, there is great economic interest in the development of energy harvesting units. However, energy harvesting has the big disadvantage of intermittent energy supply, and the viability of the device depends heavily on the environment and the modality of energy harvester that is employed. This creates the demand for research on new techniques and careful design of energy-harvesting powered systems.

1.1. RF ENERGY HARVESTING AND WIRELESS POWER TRANSFER

Energy harvesting is broadly defined as the electrical energy generation from low-power sources. There are several types of energy harvesters. Among them, the most popular are photovoltaic, thermoelectric, vibrational, and radio-frequency (RF) harvesters [12]. The work in this thesis focuses on RF energy harvesting. More specifically, it focuses on circuit and system design techniques applied to the RF energy harvester (RFEH), the power receiver.

The advantages of RF energy harvesting are the ubiquity of RF signals in urban environments and their ability to reach environments in which other sources of energy are not present. However, RF signals may present low power density and therefore require power conversion circuits that are efficient at very low power levels. Some applications require more power, which calls for a dedicated RF power source that is located closer to the receiver. This configuration is usually characterized as wireless power transfer (WPT). At the same time, when a dedicated RF power transmitter is used, a large available power may be presented to the RFEH and, if it is not designed to accommodate such power levels, the extra energy is wasted.

Examples of RF energy harvesting and WPT applications are in smart buildings, warehouse (inventory) management, and bio-electronic implants. In smart building and warehouses, there are little vibrations or temperature gradients and low ambient light, since the device might be installed inside a wall, in a package, or in a generally dark place that is not frequently accessed by humans [13, 14]. In bio-electronic implants there is little light or temperature gradients. There is usually enough vibration, but it is not guaranteed and wireless power transfer is still the preferred way due to its reliability [15].

Regardless of the application, there are always two basic components in such systems: the power transmitter (source) and the power receiver. In the case of energy harvesting, the source is not a dedicated power source, as its function is to transmit data. Therefore, the available power at the receiver is usually in the order of micro-watts [16], and the carrier frequency can be high, such as 2.45 GHz for signals in the WiFi band [17]. In the case of WPT, the source is a dedicated power source. The available power is higher and there is more flexibility in the selection of the transmitter frequency, as long as it respects the spectrum allocation and regulation [17]. If a lower frequency signal is used, the distance between transmitter and receiver can be larger for the same received power, but also the antenna size needs to be larger. If a higher frequency signal is used, the antenna size can be decreased, but the free space losses are larger, reducing the maximum distance between transmitter and receiver.

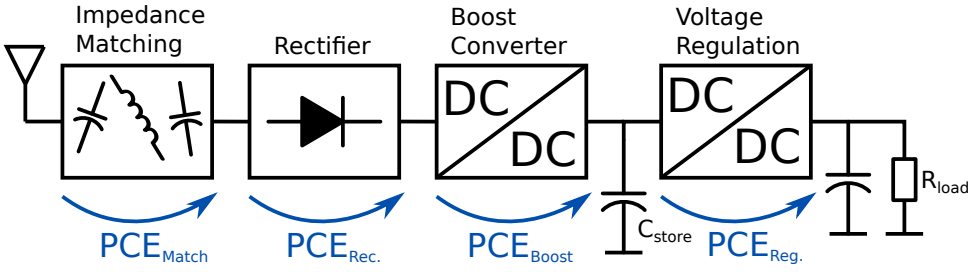


Figure 1.1: Block diagram of a typical RF energy harvesting power conversion chain.

We can categorize the transfer of wireless power in terms of the field region of the transmitting antenna in which the receiving antenna is located. The field region is defined based on the distance between transmitter and receiver, relative to the wavelength λ of the transmitted signal and to the antenna dimensions [18]:

- **Reactive near-field:** the distance between transmitter and receiver is short. The boundary is defined at a distance $0.62\sqrt{D^3/\lambda}$, in which D is the largest dimension of the antenna. For very short antennas, the boundary is considered to be $\lambda/2\pi$. The reactive fields are dominant in this region. Therefore, it is characterized by non-radiative coupling through magnetic or electric fields. Magnetic coupling using coils has been widely studied and used in consumer applications [19, 20].
- **Radiating (Fresnel) near-field:** in-between the reactive near-field and the far-field regions. It is sometimes referred to as the "mid-field". The boundary between this region and the far-field region is $2D^2/\lambda$ for long antennas. For short antennas, this region does not exist. The radiating fields are dominant in this region and the angular field distribution depends on the distance from the antenna. It has been explored in recent works as a region for high energy transfer in biomedical implants [21].
- **Far-field (Fraunhofer):** the distance between transmitter and receiver is large. There is no coupling in this region and the power transfer is carried by radiating waves. The angular field distribution is independent of the distance. This region is useful for both energy harvesting, from distant sources, and dedicated WPT. Since there is no difference for the power receiver whether the source is dedicated or not, in this thesis, we use RFEH to denominate the receiver in both cases, for simplicity.

The work in this thesis focus on the far-field region, targeting both energy harvesting and WPT. However, most of the techniques presented here can be applied to other types of WPT.

1.2. POWER CONVERSION CHAIN

The power conversion chain of a typical RFEH and power management unit is presented in Fig. 1.1. The electromagnetic signal is received by the antenna and converted into an AC electric signal. To ensure maximum power transfer from the antenna to the rectifier,

the impedance matching network performs the conjugate matching between them. The rectifier block converts the AC signal into a DC signal, which is then used by the DC-DC converter to charge the storage capacitor (or battery). In case the rectifier output is large enough due to either a large input power or an increased number of rectifying stages, this DC-DC converter is optional. However, the DC-DC converter is desirable, as will be presented in this thesis, since it matches the rectifier output impedance and increases its power conversion efficiency (PCE). Finally, a voltage regulator is used to present a stable DC voltage to the load. This last stage is also optional. In the case the load is able to deal with a large variation of supply voltage, it can be connected directly to the storage capacitor. Or if the storage capacitor is replaced by a battery, the load might be connected directly to the battery.

We can break down the total PCE of the typical power conversion chain in the following way:

$$\text{PCE}_{\text{tot}} = \frac{P_{\text{load}}}{P_{\text{av}}} = \text{PCE}_{\text{Match}} \cdot \text{PCE}_{\text{Rec.}} \cdot \text{PCE}_{\text{Boost}} \cdot \text{PCE}_{\text{Reg.}}, \quad (1.1)$$

in which P_{load} is the power delivered to the load and P_{av} is the available power from the antenna. The other PCE terms in the equation are the conversion efficiency of each block in the chain, as seen in Fig. 1.1.

The power conversion chain can be designed and optimized for a given P_{av} , antenna, and output voltage. In this case, the value of the PCE terms of (1.1) are maximized only for the given condition. If more flexibility is needed, a maximum power point tracking (MPPT) circuit can be employed to configure one or more blocks of the chain, tracking the changes and returning the PCE to a high value. To enable the use of an MPPT circuit, the blocks must be configurable. To illustrate the benefit of configurability, Fig. 1.2 presents the PCE of three different power conversion chains:

- a power conversion chain in which the impedance matching network and the DC-DC converter are fixed and cannot adapt to the input power changes;
- a power conversion chain in which only the DC-DC converter is configurable;
- a power conversion chain in which both the impedance matching network and the DC-DC converter are configurable.

In this illustration, all the blocks are ideal and configurable except the rectifier. The fixed power conversion chain presents a fast PCE drop when the available power deviates from the point for which the chain was designed. In the second chain, the configurability of the impedance matching network, and the interface between rectifier and antenna is optimized for every value of P_{av} . However, the interface between rectifier and load is still kept fixed. It can be optimized further by reconfiguring the DC-DC converter, which leads us to the third power conversion chain. The configurability of both the impedance matching network and the DC-DC converter results in a higher PCE for a broader available power. The variation in PCE that is left is only due to the rectifier conversion efficiency variation.

It is possible to distinguish two sources for PCE variation. The first one is the variation of the input and output impedances of each block, which affects the interfacing between adjacent blocks. The second one, which can be seen through (1.1), is the PCE

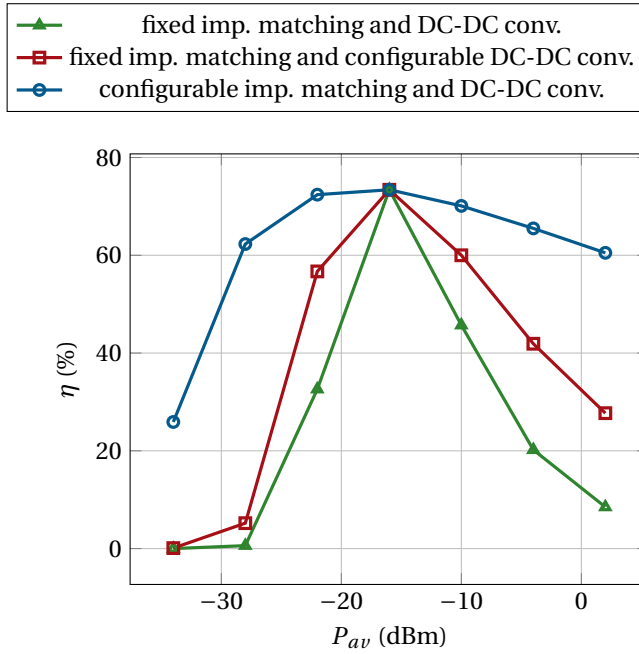


Figure 1.2: Simulation results of three power conversion chains with different levels of configurability.

variation of each block. Therefore, these two factors must be taken into consideration when designing each block.

1.3. MOTIVATION

Considering that the transmitter and the receiver have fixed antennas, the received power P_r varies with distance, alignment between the antennas, propagation medium, and matching between the antenna and the electronics at both the transmitter and the receiver sides. It is possible to extend the Friis' equation to include these factors [22]:

$$\frac{P_r}{P_t} = G_t(\theta, \phi) G_r(\theta, \phi) \left(\frac{\lambda}{4\pi d} \right)^2 (1 - |\Gamma_t|^2) (1 - |\Gamma_r|^2) e^{-\alpha d}, \quad (1.2)$$

in which P_t is the transmitted power, d is the distance between the antennas, G_t and G_r are the transmitting and receiving antenna gains, Γ_t and Γ_r are the transmitting and receiving reflection coefficients, and α is the path loss exponent, which depends on the propagation medium. In the case of RF energy harvesting from non-dedicated sources, network traffic may also affect P_r [23]. Because of variations of all these parameters, it is not easy to predict what the received power in most applications will be.

The RF energy harvester might be designed for the worst-case scenario (lowest available power) of a target application, guaranteeing that the application is going to have enough energy to operate. However, whenever there is a large amount of available power, there will be losses due to the efficiency reduction. There are three main advantages of

having a harvester that presents high efficiency over a wide range of available power. The first one is that the same design can be used in different applications, since they will have different power specifications. The second one is to enable a better performance for power-aware devices. Such devices are aware of the available power and change their operating performance depending on it [24, 25]. For example, if there is a high available power, a power-aware sensor would increase its acquisition rate and accuracy or a power-aware micro-controller would increase its clock frequency to process more data. When the available power decreases, the device would reduce its performance in order to consume less power. The third advantage is to enable applications that can combine RF energy harvesting and WPT, harvesting ambient RF when far from a dedicated source, but efficiently converting power when near the source. Therefore, being able to increase the input power range for which an RFEH device can operate efficiently will enable us to use energy that otherwise is being wasted.

1.4. CHALLENGES AND OBJECTIVES

The objective of this thesis is to research, design, and measure an RFEH and power management unit that presents high efficiency for a broad input power range, a high peak PCE, and a high sensitivity. This enables new applications of RF energy harvesting technology and reduces energy loss. As discussed previously, variations in the rectifier interfaces and in the PCE of each block lead to the reduction of the total PCE as the available power deviates from the optimal point. The implementation of configurability in the power conversion chain blocks can solve this problem. However, the additional circuits tend to create new trade-offs. More power is necessary to control such circuits, which will lead to a PCE reduction by itself. Moreover, additional area is needed, which increases the overall footprint of the device. Both tend to increase with the level of configurability. Therefore, innovations at both the circuit and system levels are needed to reduce power consumption and area.

1.5. SYSTEM DESCRIPTION AND THESIS ORGANIZATION

This thesis presents the system described by the block diagram in Fig. 1.3. The system is designed in a standard $0.18\ \mu\text{m}$ CMOS technology due to its low cost and availability. The target frequency for the RF input is 403.5 MHz, the center frequency of the MICS band, suitable for biomedical devices. Nevertheless, the techniques presented in this thesis are not strongly dependent on the signal frequency and can be tailored to different input and output specifications. The system converts the RF energy received by the antenna (modelled as a voltage source V_{ant} in series with an impedance Z_{ant}) into DC energy and stores it on capacitor C_{store} . Besides that, it supplies the load, modelled as resistor R_{load} (capacitor C_{load} is used to filter the voltage across R_{load}).

The first step is to convert the RF signal into DC, charging C_{rec} . This is performed by an RF-DC converter that comprises the impedance matching network and the rectifier. These blocks are presented in Chapter 2, where we also present a method of designing an efficient multi-stage impedance matching network and use it to aid in the design of a configurable network.

Initially, the supply capacitor (C_{supply}), which provides the supply voltage to the sys-

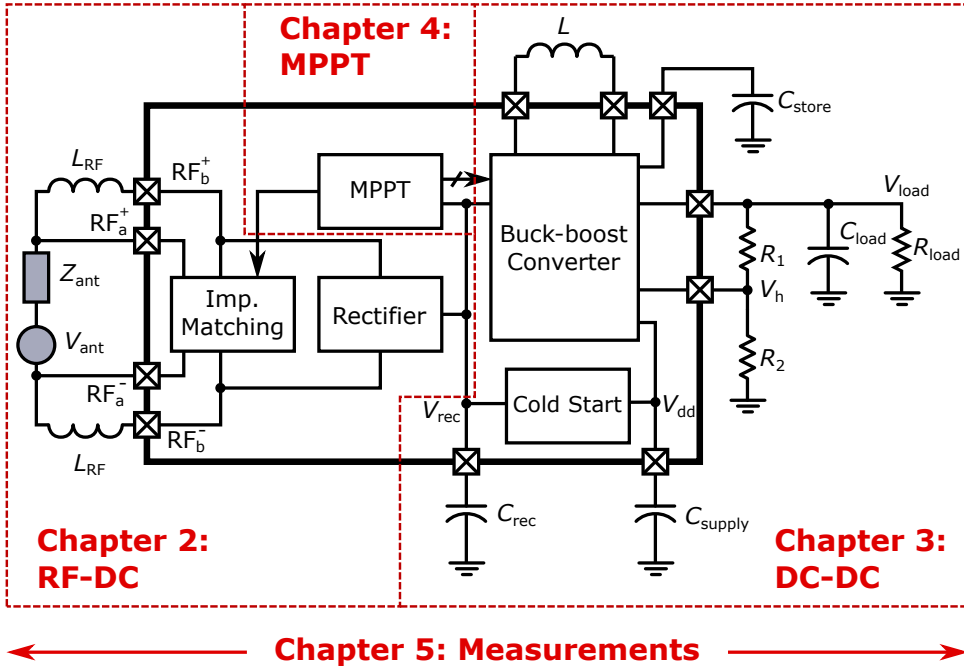


Figure 1.3: Block diagram of the implemented system. The thesis chapters discuss the blocks as shown in the figure.

tem (V_{dd}), is depleted and needs to be charged. A cold-start circuit, a Dickson charge pump [26] driven by a conventional ring oscillator [27] that can operate from input voltages down to 300 mV, is employed to charge C_{supply} . A single-inductor dual-input triple-output (SIDITO) buck-boost DC-DC converter [28] is used to charge C_{store} , to regulate V_{load} , and to charge V_{supply} when needed. It draws energy from the rectifier to charge C_{store} and C_{supply} . When supplying the load, one of two possible scenarios takes place. One of the scenarios is when there is enough power available power to continuously supply the load. In this case, the load is charged with energy directly from the rectifier output and the energy previously stored in C_{store} is saved. The other scenario is when there is not enough power available. In this case, the load charging is duty cycled. First, the load is not charged until there is enough energy in C_{store} . Then, the load is charged with energy coming from C_{store} . Once the storage capacitor is depleted, the charging of the load stops and the charging of C_{store} starts again. The converter regulates V_{load} by comparing a fraction of it (V_h) to a reference V_{ref} (not shown in Fig. 1.3, but generated on chip [29]) and charging capacitor C_{load} when $V_h \leq V_{ref}$. The cold-start and DC-DC converter circuits are presented in Chapter 3. Circuit techniques are presented that allow for the reduction of power consumption and the increase of the PCE across a wide range of DC input power and voltage.

The MPPT circuit, which sends control signals to the buck-boost converter and the impedance matching network, is presented in Chapter 4. The main innovation in the

MPPT circuit is a method of power estimation that does not interfere with the power path and is low power and compact.

In Chapter 5, the full chip is measured and the results are compared to the state of the art.

The concluding remarks and suggestions for future work are presented in Chapter 6.

2

RF-DC CONVERTER

To supply power to a load, the RF energy harvester (RFEH) must convert the AC signal provided by the antenna into a DC output, assuming a DC load. The rectifier in combination with a low pass filter (a capacitor placed at its output) performs this task. The input impedance of the rectifier must be conjugate matched to the antenna impedance to ensure maximum power transfer from the antenna to the rectifier [30]. This task is performed by the impedance matching network, which is a two-port circuit placed between the antenna and its load and that makes both of them “see” their respective conjugate impedances. The rectifier and the matching network are highlighted in Fig. 2.1, which depicts the system block diagram.

In this chapter, we explain the variation of the rectifier parameters with respect to the available input power P_{av} . This illustrates the importance of adapting the RFEH for P_{av} variations. We then present a method to design and optimize the impedance matching network. The technique presented can be applied to any antenna and load impedances to find the most efficient network. A tunable matching network is presented for the system that is being considered.

2.1. RECTIFIER

Several rectifier topologies have been employed in RFEH systems. Some of the topologies are presented in Fig. 2.2. Among them are the half-wave rectifier, the full-wave bridge rectifier, the Cockcroft-Walton/Greinacher/Villard charge pump [31] and the Dickson charge pump [26]. The latter type of rectifiers has become popular in RFEH due to its high efficiency and capability of generating higher voltages by simply increasing the number of stages. These rectifiers can be improved with techniques such as replacing the diodes with diode connected MOSFETs or MOSFET switches, orthogonal switching [32] and threshold compensation [33].

Building upon the threshold compensation technique, the self- V_t -cancellation technique has been proposed [34, 35]. Since it does not require extra circuitry to generate biasing of the switches, avoiding extra power dissipation, this technique has been proved

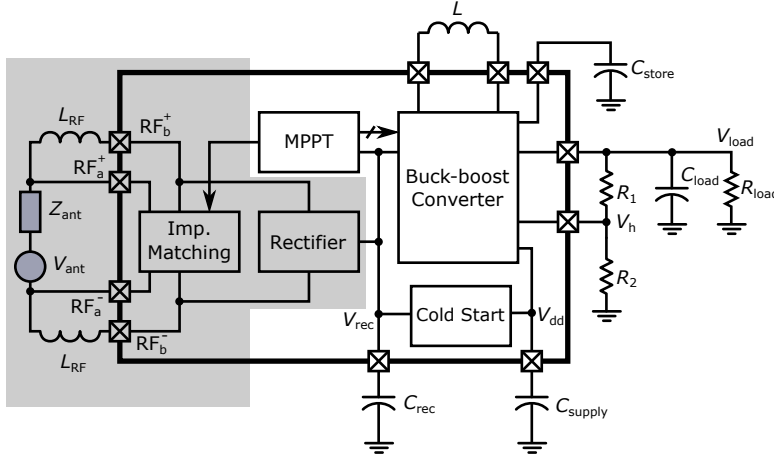


Figure 2.1: System block diagram: the RF-DC converter blocks are highlighted

useful to achieve high PCE at low input power levels. Its further development led to the cross-coupled differential-drive rectifier topology [36], presented in Fig. 2.3. This rectifier and the ones derived from this topology have shown high PCE and high sensitivity results, specially for high-frequency RFEH [37–39]. For this reason, we have chosen to employ the differential-drive rectifier in this work.

The current flow in the differential-drive rectifier is similar to the one in the full-bridge rectifier (Fig. 2.2(b)). During the negative half-cycle, C_1 is charged through M_1 , since voltage V_1 increases and V_{in}^+ decreases. During the positive half-cycle, C_1 is discharged to V_{out} through M_2 , since voltage V_1 decreases and V_{in}^+ increases. The opposite happens to C_2 : it is discharged during the negative half-cycle and charged during the positive half-cycle. The gates of the transistors are biased with a voltage that depends on the value of V_{out} and the dimensions of the transistors. This bias voltage cancels the V_t of the transistors, increasing its efficiency [36]. Similar to the Dickson topology (Fig. 2.2(d)), this rectifier can be cascaded to generate a higher output voltage. However, as discussed later in this section, it results in a lower power conversion efficiency.

There is an output load value that maximizes the rectifier PCE. Both this optimum output load and the rectifier input impedance depend on P_{av} . Therefore, the variation of these parameters must be known in order to design an RFEH that is efficient over a large P_{av} range.

2.1.1. INPUT IMPEDANCE AND OPTIMUM LOAD VARIATION

Even though the rectifier is a non-linear circuit, its input impedance can be approximated by a linear one. By doing so, we can design an impedance matching network and minimize the losses due to reflection. The input impedance of a rectifier can be represented as $Z_{in} = R_{in} + jX_{in}$. The real part R_{in} is mainly determined by the resistive losses and the load current. The imaginary part X_{in} is mainly determined by the parasitic capacitances of the devices. Other elements that influence Z_{in} are the parasitics of the interconnections, bond pads and bond wires.

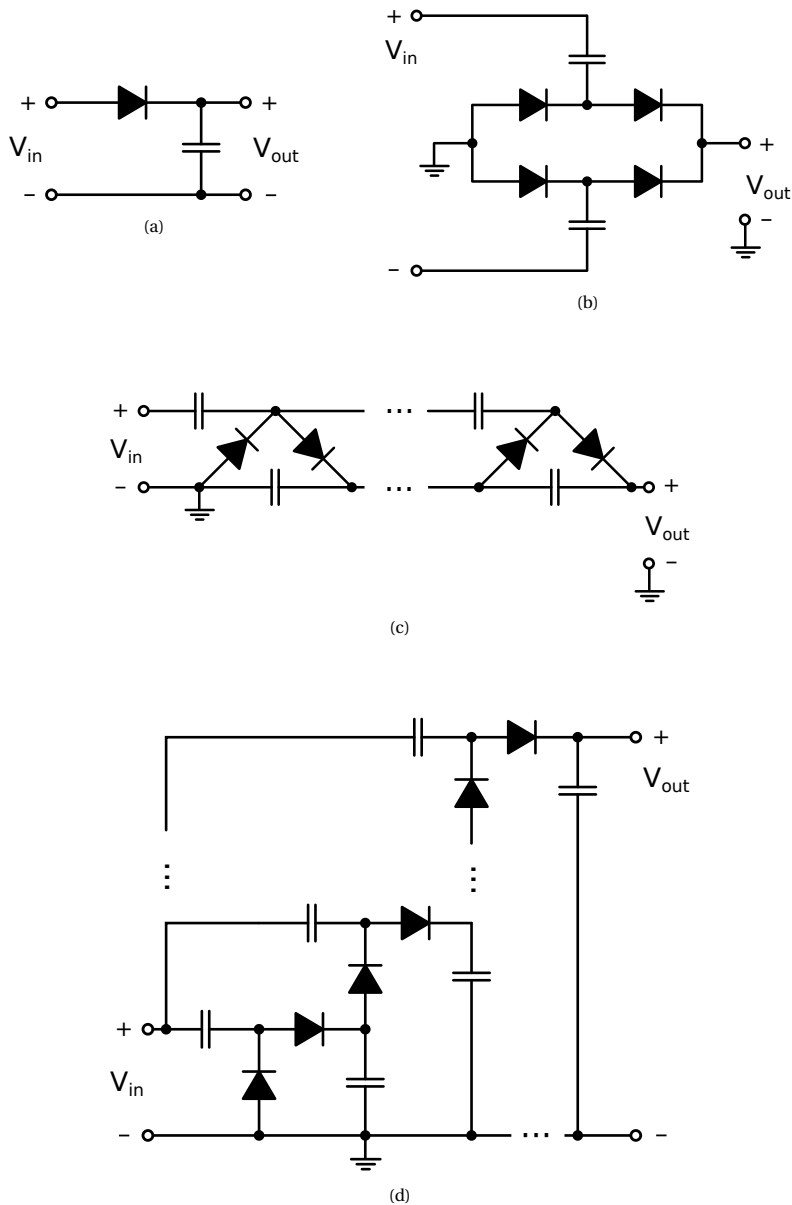


Figure 2.2: Rectifier topologies: (a) half-wave rectifier, (b) full-wave bridge rectifier, (c) Cockcroft-Walton/Greinacher/Villard charge pump, and (d) Dickson charge pump.

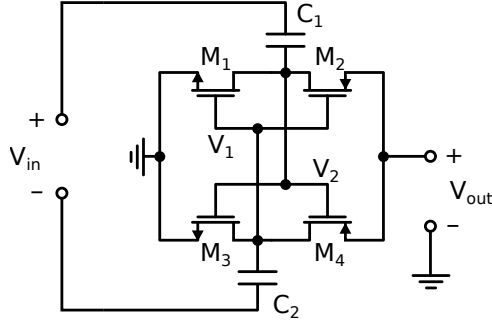


Figure 2.3: Cross-coupled differential-drive rectifier.

Table 2.1: Values of components used in the rectifier.

| Component | Value |
|------------|---------------------------------|
| C_1, C_2 | 1.83 pF |
| M_1, M_3 | 3 $\mu\text{m}/180\text{ nm}$ |
| M_2, M_4 | 8.1 $\mu\text{m}/180\text{ nm}$ |

In the rectifier of Fig. 2.3, for an increasing available power, the input voltage amplitude increases as well as the DC voltages at nodes V_{out} , V_1 and V_2 . This reduces the R_{ON} of the devices and change their parasitic capacitance, which has a direct effect on the input impedance. Fig. 2.4(a) shows R_{in} and X_{in} obtained through simulation of the rectifier with the component parameters presented in Table 2.1. In this simulation, for each P_{av} value, R_{load} is swept and, for each of its values, the source impedance Z_s is matched to the rectifier impedance ($Z_s = R_{\text{in}} - jX_{\text{in}}$). The optimum load and input impedance for a given P_{av} are the ones for which the PCE is the highest. The PCE and optimum load versus P_{av} are presented in Fig. 2.4(b).

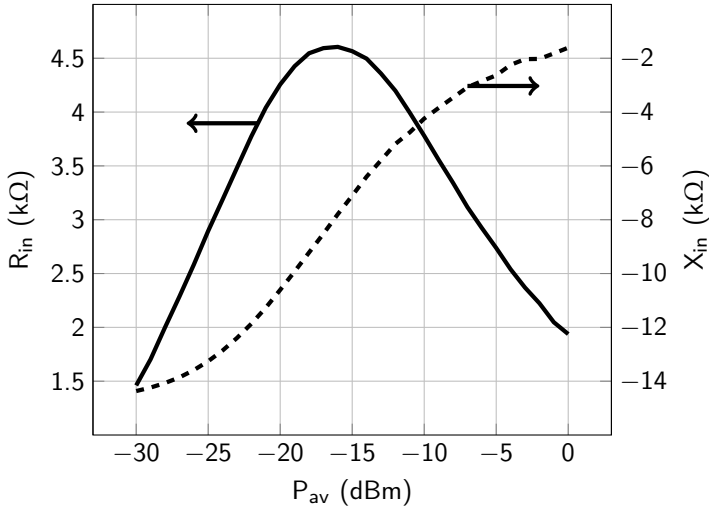
2.1.2. POWER CONVERSION EFFICIENCY

The rectifier PCE is given by:

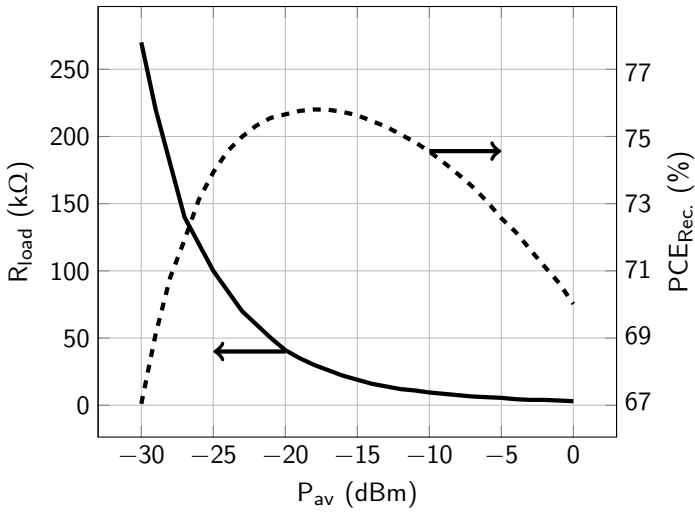
$$\text{PCE} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}}, \quad (2.1)$$

in which P_{out} is the output power and P_{loss} is the power loss, which is determined by the conduction losses and leakage [40]. The leakage increases with the output voltage and the W/L of the switches. On the other hand, conduction losses decrease with W/L and the gate voltage, since the R_{on} of the switches decreases.

For an increase in the number of rectifier stages, the output voltage increases, which can enable higher sensitivity in systems that do not employ a DC-DC converter to boost the rectifier output [32, 33, 37]. However, this leads to a PCE reduction due to an increase of the conduction losses, since more stages are placed in series. Furthermore, the



(a)



(b)

Figure 2.4: The real and imaginary parts of the rectifier input impedance (a), as well as its optimum load and PCE (b), vary with its input power.

amplitude of the rectifier input voltage decreases, as it can be written as:

$$|V_{in}| = |I_{in}| |Z_{in}| = \sqrt{\frac{2P_{av}}{R}} \sqrt{R_{in}^2 + X_{in}^2}. \quad (2.2)$$

2

The reduction of the equivalent input impedance, that occurs when several rectifying stages are employed, results in a reduction of $|V_{in}|$. Alternatively, this effect can be seen as a reduction of the passive voltage boost from the antenna to the rectifier [41]:

$$G_{V,boost} \approx \frac{X_{in}}{R_{ant} + R_{in}}, \quad (2.3)$$

in which R_{ant} is the antenna resistance.

The rectifier is usually the most inefficient block in the power conversion chain [12]. If a high-efficiency DC-DC converter can be designed to boost the rectifier output voltage, a single-stage rectifier is the best option for obtaining high PCE. In this work, we use the rectifier presented in Fig. 2.3 with component values presented in Table 2.1. It is designed to have high efficiency over the targeted P_{av} range. As can be seen in Fig. 2.4(b), it presents an efficiency higher than 67% from -30 to 0 dBm.

2.2. IMPEDANCE MATCHING

Impedance matching networks are applied, for example, in communication circuits [30, 42, 43], DC-DC converters [44] and rectifiers [45]. They are employed to assure maximum power transfer when the impedance of the power source is not equal to the conjugate of the load impedance. Such networks are two-port circuits placed between source and load and make them “see” their respective conjugate impedances.

Most analyses of matching networks assume no losses and power efficiency is not the goal [30, 42, 43]. But in some applications, like wireless energy harvesting and transfer, the power conversion efficiency is the most important goal and the energy losses in the matching network cannot be neglected. To realize a more efficient matching network, in some cases, a combination of several L-matches may be used [43, 46]. In [46], a method for obtaining high-efficiency matching networks is presented, but only purely real impedances are considered. Not including complex impedances may discard the most efficient network from the solution space.

The goal here is to develop a method of optimization of multistage matching networks and design a tunable matching network to match the rectifier to the antenna over a large P_{av} range. To this end, we first analyze, in Section 2.2.1, the efficiency of the basic matching network, the L-match [42], for the general case of complex source and load impedances. In Section 2.2.2, we define the efficiency of the multistage matching network and optimize it for maximum efficiency. In Section 2.2.3, we apply this optimization technique to some design examples and to the rectifier presented previously. A tunable impedance matching is presented in Section 2.2.4.

2.2.1. EFFICIENCY ANALYSIS

In order to analyze the efficiency of a multistage matching network, we first analyze its basic building block, the L-match, which is shown in Fig. 2.5. In this circuit, reactances

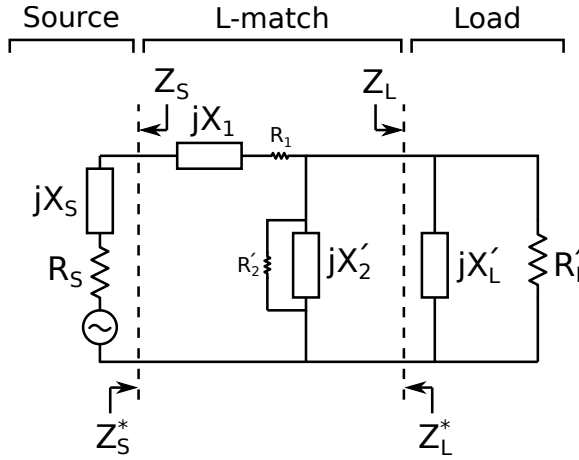


Figure 2.5: Lossy L-match network matching complex impedances

X_1 and X_2 represent the inductors or capacitors used to transform the impedance, and resistances R_1 and R_2 represent their losses. Note that, throughout this chapter, the prime symbol denotes the equivalent parallel values of the components at the frequency of interest, as $jX'_L \parallel R'_L$ in Fig. 2.5 is the equivalent of $Z_L = R_L + jX_L$.

For high-efficiency matching networks we may state, initially, that resistors R_1 and R_2 are small enough so that they have negligible influence on the matching. We know that the transformation quality factor of the network must be equal to the series and shunt legs' quality factor when the impedances are matched [30]. For complex load and source impedances, as in Fig. 2.5, the quality factor is

$$Q = \sqrt{\frac{R'_L}{R_S} - 1} = \frac{|X_1 + X_S|}{R_S} = \frac{R'_L}{|X_2 \parallel X'_L|}. \quad (2.4)$$

The input and output power are given by

$$P_{\text{in}} = I_S^2 R_S, \quad (2.5)$$

$$P_{\text{out}} = \frac{V_L^2}{R'_L}, \quad (2.6)$$

in which I_S is the RMS current in the series leg and V_L is the RMS voltage across the shunt leg. We can calculate the losses in the parasitic resistors:

$$P_{\text{loss},1} = I_S^2 R_1 = \frac{Q}{Q_1} \left| \frac{X_1}{X_1 + X_S} \right| P_{\text{in}}, \quad (2.7)$$

$$P_{\text{loss},2} = \frac{V_L^2}{R'_2} = \frac{Q}{Q_2} \left| \frac{X_2 + X_L}{X_L} \right| P_{\text{out}}, \quad (2.8)$$

in which Q_1 and Q_2 are the quality factor of the components used in the L-match. The

output power is equal to the input power minus the losses in the parasitic resistances:

$$P_{\text{in}} = P_{\text{out}} + P_{\text{loss},1} + P_{\text{loss},2}. \quad (2.9)$$

Knowing that PCE is the ratio between output and input power and substituting (2.7) and (2.8) in (2.9), we get

$$\text{PCE} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{1 - \frac{Q}{Q_1} \left| \frac{X_1}{X_1 + X_S} \right|}{1 + \frac{Q}{Q_2} \left| \frac{X_2 + X_L}{X_L} \right|}. \quad (2.10)$$

Because the equations were defined for the up-converting L-match (Fig. 2.5), the impedances can be matched and (2.10) is valid when $R'_L > R_S$. When this is not the case, we may swap Z_L and Z_S . This is the equivalent of using a down-converting L-match. With that in mind, (2.10) can be applied for any impedance transformation.

Equation (2.10) is similar to the one presented in [46], but we include the reactances of source and load to it. This addition is important to obtain better PCE in multistage networks as will be explained in the next section.

2.2.2. MAXIMIZING EFFICIENCY FOR MULTISTAGE MATCHING

Using two or more L-matches, as shown in Fig. 2.6, may increase the efficiency. The multistage matching network gradually transforms the impedance while reducing the Q of each stage and balancing their losses. To do that, we must select the correct intermediary impedances $Z_{S,n}$ of the network. Doing this, the bandwidth of the matching network tends to increase because the Q is decreasing as the impedance changes from load to source in smaller steps [30].

The efficiency of a multistage matching network with N stages is defined by

$$\text{PCE} = \prod_{n=1}^N \text{PCE}_n(Z_{S,n}, Z_{L,n}), \quad (2.11)$$

in which the efficiency of the n -th stage PCE_n is calculated through (2.10) and its parameters are obtained with the stage's selected source and load impedances, $Z_{S,n}$ and $Z_{L,n}$, respectively.

When the impedances are matched, the network presents $Z_{L,n} = Z_{S,n+1}^*$ at each section [43]. Therefore, we must only find the vector $Z_{S,n}$ with size $N-1$ that optimizes PCE, in which N is the desired number of L-match stages. Notice that $Z_{S,0} = Z_S$ is the source impedance and $Z_{S,N} = Z_L^*$ is the conjugate of the load impedance. We may find the best vector $Z_{S,n}$ by means of numerical optimization using (2.4)-(2.11) with specified Z_S , Z_L and quality factor of the components used in the matching network.

To optimize the network we use MATLAB's *Globalsearch* class [47, 48] with the *fmincon* local solver [49]. We need to apply a global optimization algorithm because this problem presents several local maxima. While using the *fmincon* solver it is important to set the solution constraints correctly. These are set as nonlinear constraints, checking if the vector of section impedances can be realized by the desired (up-converting or down-converting) L-match.

Running the optimization for several values of N , we find that there is a minimum number of stages N_{min} that produces the maximum achievable efficiency. Increasing

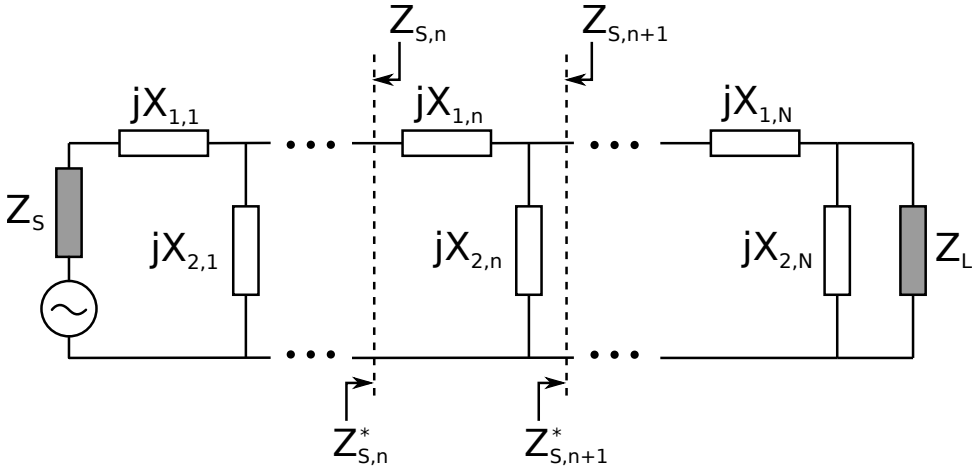


Figure 2.6: Multistage impedance matching network

N beyond $N > N_{\min}$ does not decrease the efficiency because we consider intermediate complex impedances and the values of $X_{1,n}$ ($X_{2,n}$) can be equal to zero (infinity), which produces effectively the same network for greater values of N . The value of N_{\min} increases with the impedance transformation, but it also depends on the imaginary part of the impedances, which may limit the number of stages.

APPROXIMATIONS

In order to reduce the computation time, we may apply some approximations to simplify (2.11). For example, suppose that we want to match a capacitive load ($X_L < 0$) to an inductive or resistive antenna ($X_S \geq 0$), which is a common scenario. The best way to match is by using L-matches with series inductors and parallel capacitors (which can be seen from (2.4) and (2.10)). As a first, yet realistic, approximation, we may consider all quality factors constant for any value of inductance and capacitance, i.e., Q_1 is always equal to Q_{ind} and Q_2 to Q_{cap} . When using capacitors with Q_{cap} much greater than the inductors' Q_{ind} , we can approximate the PCE equation to

$$\begin{aligned} \text{PCE} &= \prod_{n=1}^N \left(1 - \frac{Q_n}{Q_{\text{ind}}} \left| \frac{X_{1,n}}{X_{1,n} + X_{S,n}} \right| \right) \\ &= \prod_{n=1}^N \left(1 - \frac{|Q_n - Q_{S,n}|}{Q_{\text{ind}}} \right), \end{aligned} \quad (2.12)$$

in which $Q_{S,n} = |X_{S,n}|/R_{S,n}$ is the quality factor of the source impedance of each stage.

As a second approximation, we may consider only high-efficiency networks, i.e., when the negative term in (2.12) is much smaller than 1. In this case, we may further approximate the equation to:

$$\text{PCE} \simeq 1 - \frac{1}{Q_{\text{ind}}} \sum_{n=1}^N |Q_n - Q_{S,n}|. \quad (2.13)$$

When using the *fmincon* solver to optimize (2.13), it is necessary to update the solution constraints to check whether the vector of section impedances can be matched by L-matches composed of a series inductor and a parallel capacitor.

2

LOW-EFFICIENCY MATCHING NETWORKS

When the efficiency of the matching network is low, the approximations above will not apply. Furthermore, (2.10) is not valid anymore because the parasitic resistances are now influencing the matching and consequently changing the current through the components and their losses. The efficiency equation for the L-match that uses series inductors is

$$\text{PCE}_n = 1 - \frac{|Q_n - Q_{S,n}|}{Q_{\text{ind}}} \frac{4R_{S,n}^2}{(2R_{S,n} + R_{1,n})^2} - |\Gamma_n|^2, \quad (2.14)$$

in which $R_{1,n} = X_{1,n}/Q_{\text{ind}}$ is the inductor series resistance and Γ_n is the updated reflection coefficient, given by

$$\Gamma_n = \frac{R_{1,n}}{2R_{S,n} + R_{1,n}}. \quad (2.15)$$

Note that in (2.14) we consider that the extra losses take the matching network away from the matched condition ($\Gamma_n \neq 0$). Another approach would be to match source and load considering the extra losses, which would make $\Gamma_n = 0$. However, optimizing (2.14) is a better approach when dealing with lossy components or high impedance transformations, because the matched state may not present the best efficiency [19].

SIMULATIONS

Setting the source impedance to 50Ω , we apply the optimization for a large range of purely real load impedances, from 200Ω to $50\text{k}\Omega$. For this test, we consider the inductors to have a quality factor equal to 80 and the quality factor of the capacitors to be infinite. We simulate the matching network obtained through optimization and compare its efficiency to the one calculated through the high-efficiency approximation. The results are presented in Fig. 2.7 along with the minimum number of stages that produces the maximum efficiency (N_{min}). As expected, the value of N_{min} and the difference between calculated and simulated efficiency increases with R_L (as the impedance transformation increases).

The variation of efficiency with number of stages for the case of $Z_S = 50\Omega$ and $Z_L = 25\text{k}\Omega$ is presented in Fig. 2.8. The efficiency increases with N , but for larger values of N its increase may not justify the use of more components. For example, from $N = 6$ ($\eta = 91.85\%$) to $N = 7$ ($\eta = 91.98\%$), the increment in efficiency is only 0.13%. At $N = 1$, for which the efficiency is lower, we can observe that the approximation result presents a larger error, but for bigger N the error is reduced (down to 0.34% for $N = 7$). Fig. 2.8 shows that it is possible to obtain much higher efficiencies by using a multistage network while optimizing its intermediate impedances, when compared to a single stage network.

In Fig. 2.8 we also show how the 3 dB bandwidth varies with the number of stages. In this analysis we consider the frequency of interest equal to 1 GHz. Due to the reduction of impedance transformation between each stage, the bandwidth increases from 45 MHz, for $N = 1$, to 379 MHz, for $N = 7$.

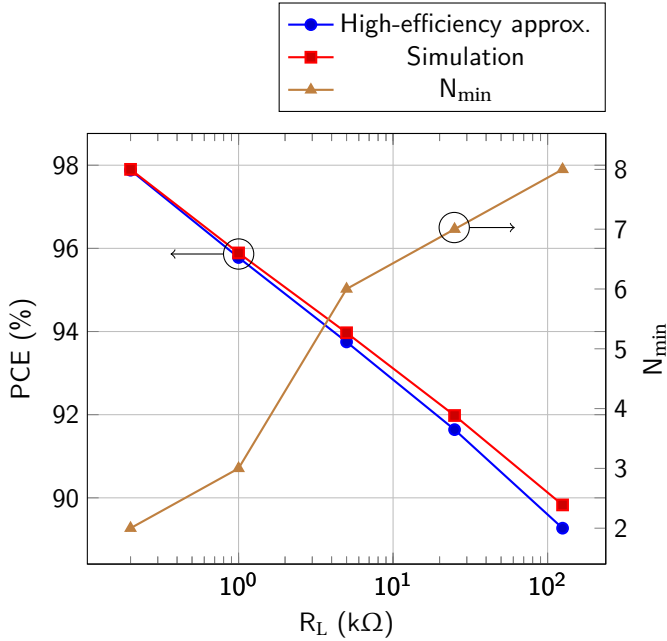


Figure 2.7: Comparison of simulation and approximation results along with number of stages (N_{min}) to obtain maximum efficiency. For each value of R_L , both efficiency values were obtained with the corresponding N_{min} shown in the plot

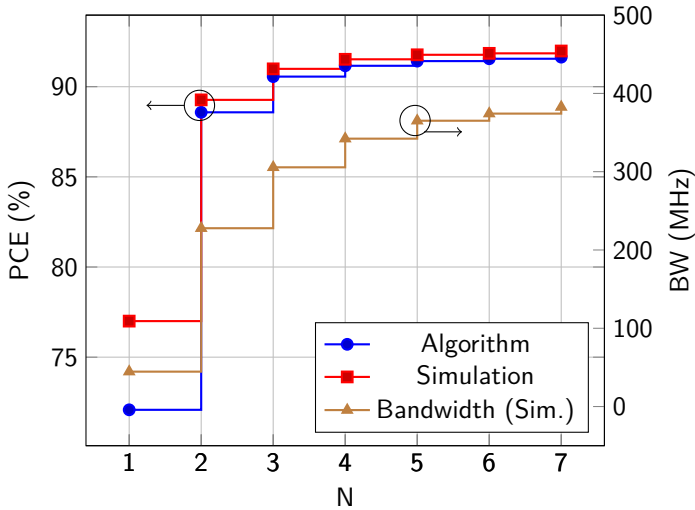


Figure 2.8: Efficiency and bandwidth of matching networks varying the number of stages for $Z_s = 50\Omega$ and $Z_l = 25k\Omega$

COMPARISON WITH PREVIOUS ART

In Fig. 2.9 we show the intermediate impedances of the matching network designed using the method presented in [46], which uses only real intermediate impedances, and using the method proposed in this work. We compare the methods in one case in which we have only real source and load impedances ($Z_S = 10\Omega$ and $Z_L = 3\Omega$) and in another case in which we have complex source and load impedances ($Z_S = 10 + j50\Omega$ and $Z_L = 2770 - j3772\Omega$). The impedance levels of the second case can be found in the problem of matching a rectifier to an inductive antenna.

In the first case, for which the impedance transformations are shown in Fig. 2.9(a)-2.9(b), our method presents a reduction of 5% in losses (as the efficiency increases from 91.45% to 91.88%) for $N = 3$. The work in [46] does not introduce a guideline to match complex impedances. Thus, for the second case, we make the matching network absorb the imaginary part of the load and source impedances while applying the method that considers real impedances, which is possible for $N = 2$ and $N = 1$. In this case we obtain a reduction of 1.8% of the losses (as the efficiency increases from 93.97% to 94.08%) by using intermediate complex impedances with the same number of stages. Increasing the number of stages to $N = 6$, we obtain a 95.93% efficiency with the proposed method. When increasing the number of stages with the previous method [46], a drop in efficiency occurs. In Figs. 2.9(c)-2.9(d), the Smith charts are normalized to 500Ω to facilitate the visualization. All the results above are computed from simulations.

2.2.3. OPTIMIZATION

We will now apply the proposed multistage matching method to two cases. In the first one, we use the method to assist us in selecting the best rectifier-matching combination considering a 50Ω antenna impedance. In the second case, we match the rectifier operating at different P_{av} to an inductive antenna. In both examples, we consider the operating frequency to be 403.5 MHz and the rectifiers are designed in the AMS $0.18\mu\text{m}$ technology. We optimize the networks using (2.14), the low-efficiency equation, because the large impedance transformations in these cases produce low-efficiency matching networks that are not well described by (2.13).

CHOOSING THE BEST RECTIFIER-MATCHING COMBINATION

While selecting the transistors' width in a differential-drive rectifier, using small values may increase the efficiency, as shown in Table 2.2. The reason for this is that the input voltage amplitude increases when the equivalent series capacitance decreases, as seen in (2.2), which makes the series resistance of the switches smaller (counteracting the width reduction effect on it). However, the matching network efficiency will be reduced because the impedance transformation increases as the transistor width becomes smaller. Therefore, there is a transistor width that will present the most power efficient rectifier-matching combination. For our case, this happens when the width of NMOS transistors W_n equals $3\mu\text{m}$ as can be seen in Table 2.2.

The data in the table was obtained using an antenna impedance $Z_s = 50\Omega$ and input power $P_{in} = -28\text{dBm}$. The width of the PMOS transistors are set as $W_p = 2.7W_n$. We consider the matching network to be off-chip using inductors with $Q = 80$. We also consider the parasitic capacitance of the pads in simulations to find the rectifier input impedance

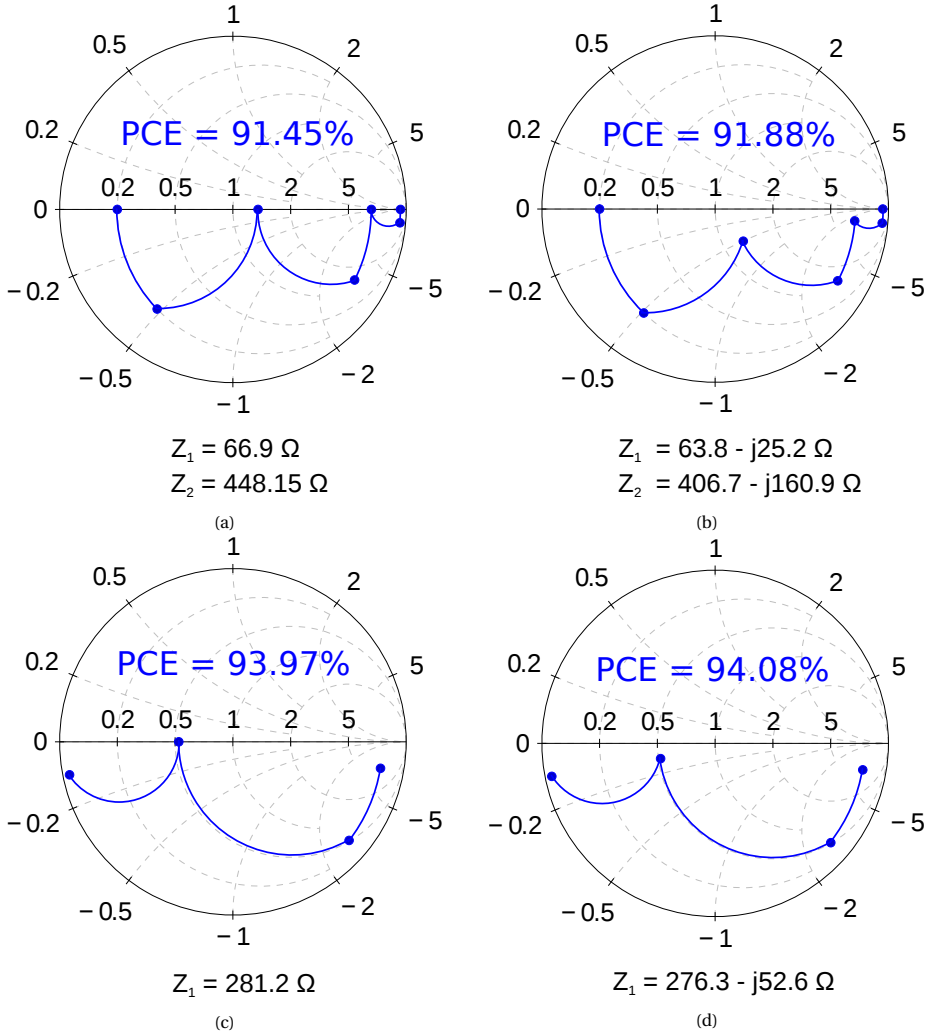


Figure 2.9: Comparison of the method presented in [46] (a, c) with the proposed method (b, d) for two cases: matching real impedances (a, b) and matching complex impedances (c, d). Impedance values of intermediary nodes (between L-matches) are shown below the Smith charts

Table 2.2: Comparison of power conversion chains for various rectifier transistor widths

| W_n (μm) | PCE_{rect} (%) | Z_L (Ω) | PCE_{match} (%) | PCE_{total} (%) |
|-------------------------|-------------------------|--------------------|--------------------------|--------------------------|
| 1.5 | 71.1 | $68 - j2860$ | 62.4 | 44.3 |
| 3 | 68.6 | $74.4 - j2731$ | 65.7 | 45.1 |
| 6 | 62.7 | $74.3 - j2506$ | 67.8 | 42.5 |
| 12 | 50.5 | $64.5 - j2167$ | 68.0 | 34.3 |

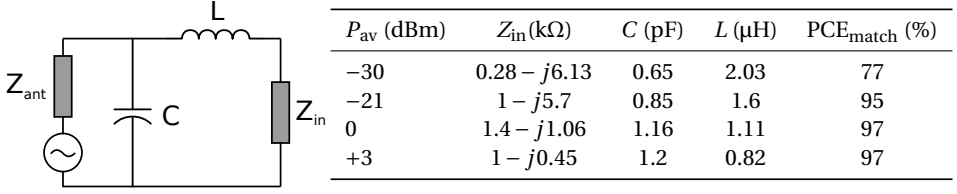


Figure 2.10: Impedance matching of a loop antenna ($Z_{ant} = 40 + j380\Omega$) to the rectifier for different values of P_{av} .

Z_L and efficiency PCE_{rect} . For those impedance values, all matching networks have the best efficiency when the number of stages $N = 2$.

MATCHING THE RECTIFIER FOR DIFFERENT P_{av} VALUES

Using a purely real antenna will not result in the best PCE for the RFEH. A capacitive load is matched more efficiently to an inductive antenna [37, 50]. Therefore, we select an inductive antenna with impedance $Z_{ant} = 40 + j380\Omega$. For this value of Z_{ant} , we calculate the best impedance matching circuits considering different values of P_{av} . Using the rectifier with components presented in Table 2.1 and running the optimization algorithm, the impedance matching circuit in Fig. 2.10 was obtained. The best matching network has a number of stages $N = 2$ for all considered values of P_{av} . However, the component in series with the antenna has close to zero reactance ($X_{1,1} \approx 0$) and the component in parallel with the load has a very large reactance ($X_{2,2} \approx \infty$). Resulting in the circuit in Fig. 2.10. For simplification, the circuit is presented in its single-ended form. For this rectifier, we employ pads with few metal layers and reduced ESD diodes, to reduce the parasitics. The impedance of the rectifier for a few values of P_{av} and the resulting matching efficiency (for inductors with $Q = 80$ and lossless capacitors) are also shown in Fig. 2.10.

2.2.4. TUNABLE IMPEDANCE MATCHING NETWORK

To design the tunable impedance matching network, we consider the same antenna ($Z_{ant} = 40 + j380\Omega$) and the same frequency ($f = 403.5\text{MHz}$) as in the previous subsection. Considering the results presented above, one could switch between two (or more) of the matching networks presented in Fig. 2.10 by means of series switches. But the resistance of the series switches are high, due to the large amplitude of the signal at high P_{av} . By using switches that are connected to the ground node, the voltage amplitude on its drain is reduced when the switch is conducting, resulting in a lower “on” resistance and higher PCE. Moreover, additional off-chip inductors are needed and more pads and external connections are necessary, increasing the parasitics. To avoid these problems, a π -network topology is employed in combination with capacitor banks. The tunable impedance matching network is presented in Fig. 2.11.

The matching is implemented for two cases: high and low P_{av} , which are selected at values -21 dBm and $+3\text{ dBm}$. Those two values are selected because they result in reasonable matching over the entire P_{av} range. The matching network configuration is set by the control bit V_{hp} . When V_{hp} is low, switches M_1 are off and the network is

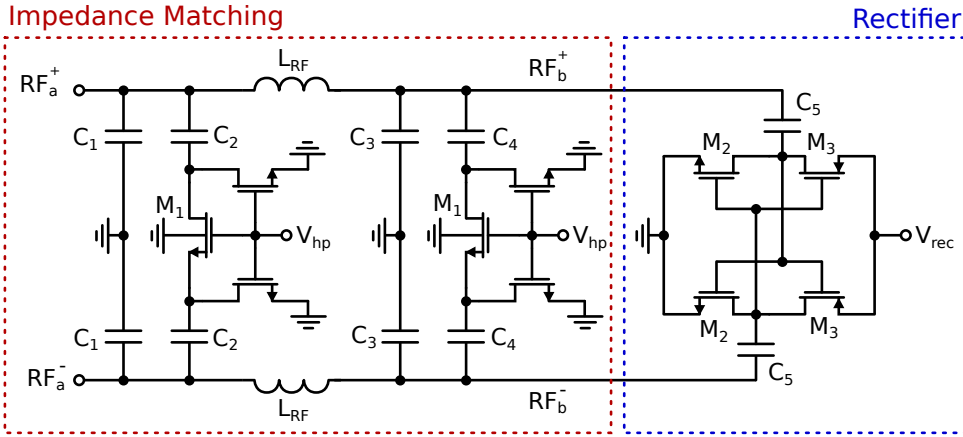


Figure 2.11: Adaptive impedance matching and rectifier circuit schematics.

Table 2.3: Value of components used in the RF-DC conversion.

| Component | Value |
|-----------------|---------------------------|
| C_1 | 393 fF |
| C_2 | 2.79 pF |
| C_3 | 110 fF |
| C_4 | 1.71 pF |
| C_5 | 1.83 pF |
| M_1 | 200 μm /180 nm |
| M_2 | 3 μm /180 nm |
| M_3 | 8.1 μm /180 nm |
| L_{RF} | 100 nH |

configured for harvesting at low power levels. When V_{hp} is high, the network is in high-power mode. The signal V_{hp} is provided by the MPPT block, discussed in Chapter 4, which estimates the available power.

The component values of the circuit in Fig. 2.11 are presented in Table 2.3. Switches M_1 are designed with a large width in order to keep the quality factor of the capacitors high ($Q > 150$). Post-layout simulation are necessary to tune the values of C_1 - C_4 .

The simulation results are presented in Fig. 2.12. In Fig. 2.12(a), we present the S11 variations as a function of the RF input frequency. Since the rectifier input impedance changes with P_{av} , the bandwidth and reflection coefficient change as well. The variation of the S11 with P_{av} , as well as the RF-DC conversion efficiency, are presented in Fig. 2.12(b). As can be seen, the S11 decreases with P_{av} , when P_{av} is between -18 and -3 dBm. However, when higher available power is detected (around $P_{\text{av}} = -3$ dBm), the MPPT activates the high-power mode of the adaptive impedance matching block, decreasing the S11. This results in an RF-DC conversion efficiency ($\text{PCE}_{\text{RF-DC}}$) increase for $P_{\text{av}} > -3$ dBm, extending the operating power range of the RFEH. The $\text{PCE}_{\text{RF-DC}}$ in

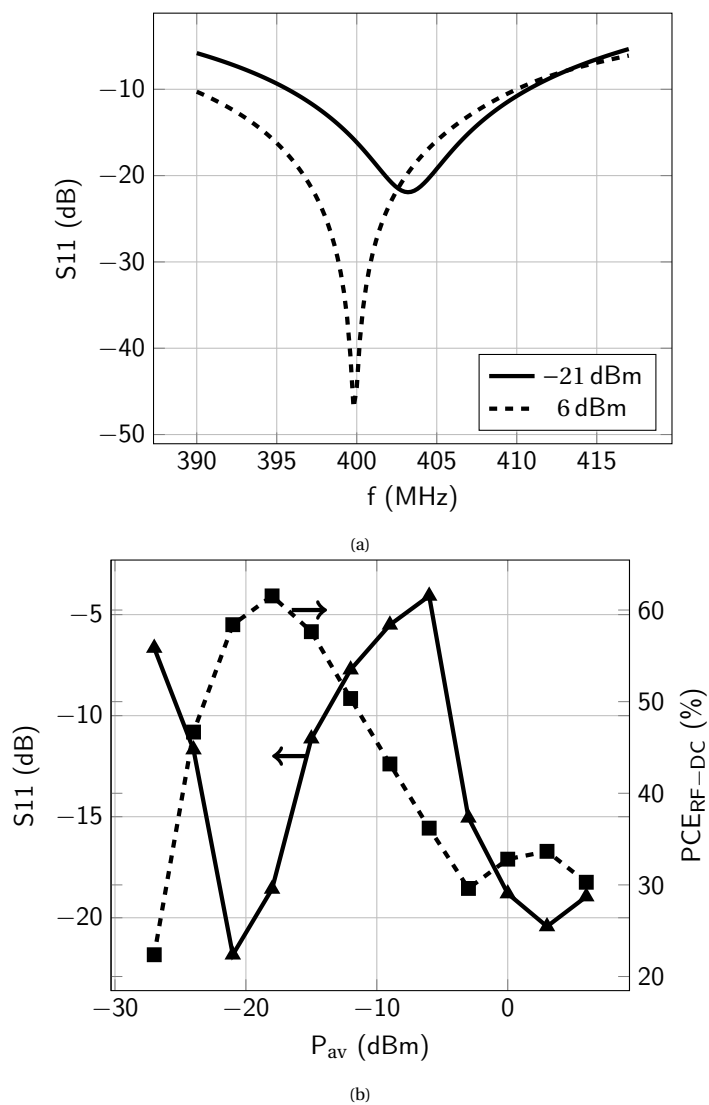


Figure 2.12: Harvester S_{11} variation with (a) frequency and (b) available power.

the high-power configuration is not as high as in the low-power configuration because there are more losses in the impedance matching network in the first case. The peak PCE_{RF-DC} is 61.5% at -18 dBm, for the low-power configuration, and 33.6% at 3 dBm, for the high-power configuration. In between -18 dBm and 3 dBm, the S_{11} increases and the efficiency drops. This efficiency drop could be reduced by increasing the complexity of the matching network by adding more configurations, which would also increase the control complexity.

2.3. CONCLUSIONS

In this chapter, we have shown how P_{av} variation influences the rectifier efficiency, input impedance and optimum load. Simulation results of the cross-coupled differential-drive rectifier topology have been presented to illustrate this. From the various rectifier topologies available, this topology is selected due to its high efficiency and sensitivity at high-frequency operation. We show that, in order to enable high efficiency over a broad range of available power, the impedance matching network and output load must be tuned accordingly (the method of controlling the load is presented in Chapter 3).

We have presented a method to design a multistage impedance matching network that has the highest possible efficiency. To this end, the efficiency analysis of an L-match and of a generic matching network formed by several L-match stages were presented, both considering complex load and source impedances. Based on these analyses, we developed a design method based on numerical optimization, which takes as input the source and load impedances and the quality factor of the components. The method considers complex impedances between stages and the optimization step finds the impedances that present the highest possible efficiency, which has not yet been shown in the literature. Comparisons of the estimation and simulation results validated the method and show that it is possible to obtain better results than the previous state-of-the-art method. In cases where there is little flexibility in selecting the source impedance or where the impedance transformation is high, our matching method is especially useful, allowing one to find the most efficient multistage matching network. The method is limited by the global optimizer algorithm employed, since there are many local maxima for the efficiency. It is also important to notice that even if we have better efficiency when increasing the number of stages of the matching network, it may not be the best solution for some cases due to the increase in the number of components and thereby the cost and area. Besides that, the extra losses due to the physical implementation of these additional stages may even reduce the total efficiency.

In this chapter, we have also presented a tunable impedance matching network that matches the selected rectifier and inductive antenna. It has two operating modes and it is set by a control bit provided by the MPPT (presented in Chapter 4). Simulation results shows that the matching network enables higher efficiency of the RF-DC conversion over a large range of available power.

3

DC-DC CONVERTER

A DC-DC converter is used to up-convert the rectifier output and charge the storage capacitor. Conventionally, an additional converter is used in cascade to supply and regulate the voltage across the load. This regulating converter can be a linear regulator or a switched converter (or a combination of both). In this work, we combine the up-conversion and load regulation converters in a single dual-input triple-output buck-boost (SIDITO) converter. This enables a reduction of the total size of the system, by employing only one inductor to perform both tasks [28]. And the use of a buck-boost converter as a regulator allows the voltage over the storage capacitor to swing from a high value to a low one, increasing the duty cycle of the load, because more energy can be drawn from the storage capacitor.

The blocks and external components that comprise the DC-DC converter, which are discussed in depth in this chapter, are highlighted in Fig. 3.1. Besides the buck-boost converter itself, a cold-start charge pump converter is employed to initially charge the supply capacitor C_{supply} with energy from the rectifier output capacitor C_{rec} . This is done in order to supply the main DC-DC converter with enough energy so it can be controlled and self sustain its operation. Resistor R_{load} represents the load to be powered by the system and capacitor C_{load} is its filter capacitor, which smooths out V_{load} . Resistors R_1 and R_2 are used in the load regulation feedback loop. Inductor L is the buck-boost converter's power inductor, and C_{store} is the storage capacitor.

The block diagram of the implemented buck-boost converter is presented in Fig. 3.2. Its two inputs are the rectifier output node V_{rec} and the storage capacitor node V_{store} , which are connected to the power inductor L through switches S_1 and S_7 , respectively. Its three outputs are V_{store} , V_{dd} and V_{load} , connected to L through switches S_3 , S_5 and S_6 , respectively. Inductor L is charged from one of the inputs, when V_g is low, for a fixed period T_{ON} , the ON time. The current flow during this period is presented in Fig. 3.3(a). Subsequently, L is discharged to one of the outputs, which takes a time T_{OFF} , the OFF time. The current flow during this period is illustrated in Fig. 3.3(b). Which input is active during the ON time and which output is active during the OFF time depend on the voltage levels of V_{dd} , V_{store} , and V_{load} . When the inductor current falls to zero and no

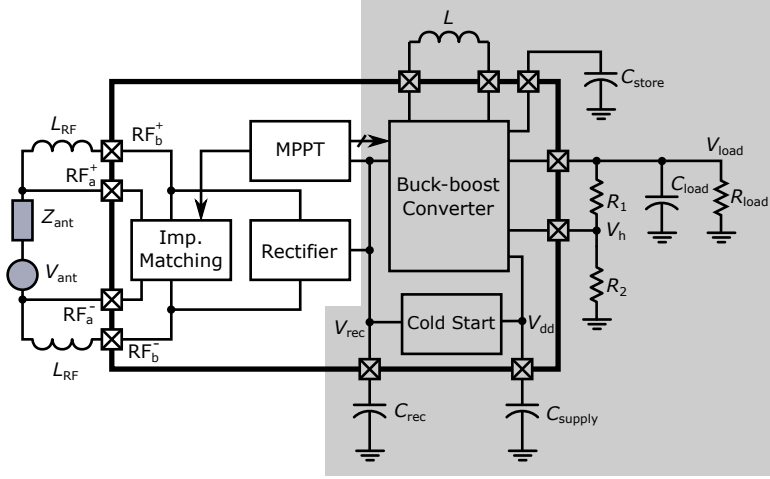


Figure 3.1: System block diagram: the DC-DC converter blocks are highlighted.

more activity is needed during the current clock cycle, all switches are turned off and the converter enters the dead time. Fig. 3.3(c) illustrates the inductor current waveform.

The converter presents a load to the rectifier, the value of which can be optimized to obtain the highest harvesting efficiency for a varying P_{av} [51]. The switched-mode converter input resistance R_{in} depends on parameters such as input and output voltage, switching frequency and duty cycle. Since the energy harvester operation consists in charging a storage capacitor that will be discharged when supplying the load, the converter output voltage is constantly changing. If R_{in} depends on the output voltage, the other parameters must be controlled to keep R_{in} constant during the harvesting, which leads to additional power consumption. To avoid this problem, we use a converter topology in which R_{in} is independent of the output voltage. This behaviour is obtained with the buck-boost converter operating in Discontinuous Conduction Mode (DCM) and open loop [52]. As can be observed in Fig. 3.3(c), the input current depends on the values of V_{in} , inductance L , duty cycle D , and switching period T . The peak current is given by:

$$I_{pk} = \frac{V_{in}DT}{L}. \quad (3.1)$$

V_{in} may assume the value of V_{rec} or V_{store} , but since we are interested only in presenting a fixed resistance to the rectifier, D and T must be constant only when V_{in} is connected to V_{rec} . Considering that S_1 and S_4 are turned on for a time DT once during the clock period, we can calculate the average input resistance as seen from V_{rec} as [52–54]:

$$R_{in,avg} = \frac{V_{rec}}{I_{rec,avg}} = \frac{2L}{D^2T}, \quad (3.2)$$

in which $I_{rec,avg}$ is the average input current coming from the rectifier.

Therefore, once every clock cycle, a pulse of current is drawn from V_{rec} . After the first pulse, when the inductor current falls to zero, more pulses are drawn from C_{store} when it

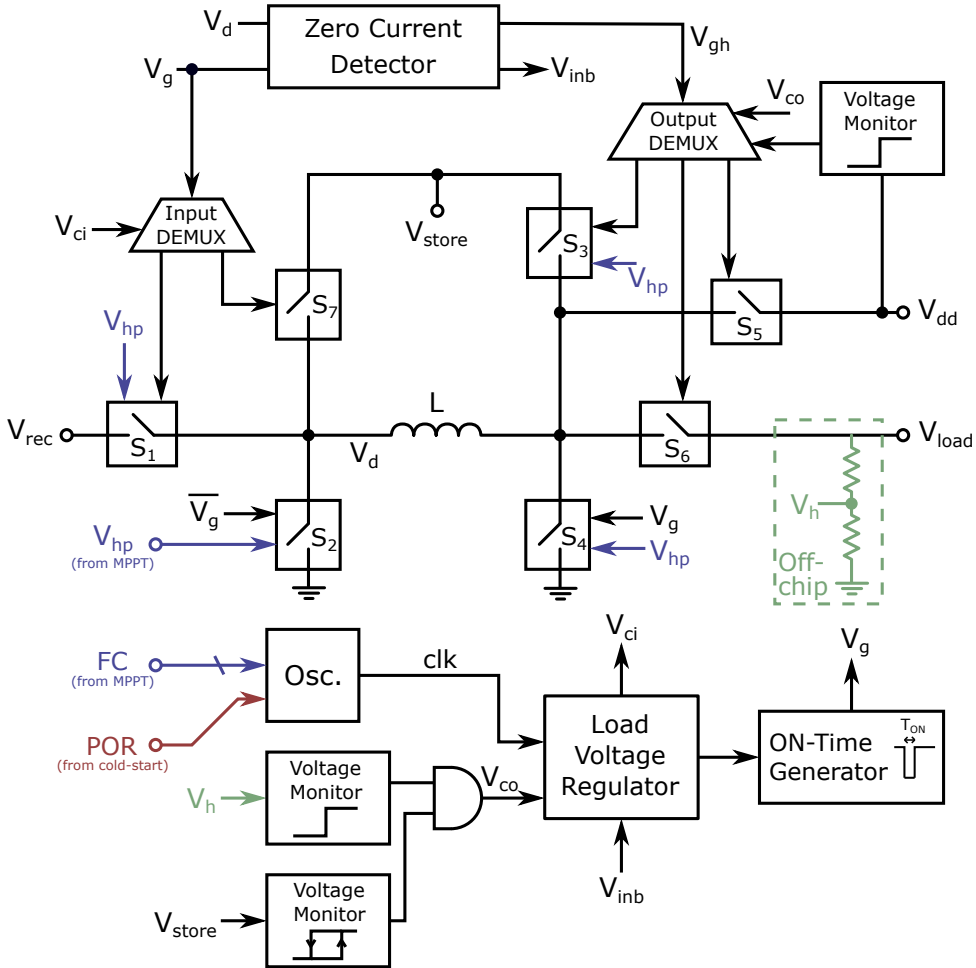


Figure 3.2: Block diagram of the buck-boost converter.

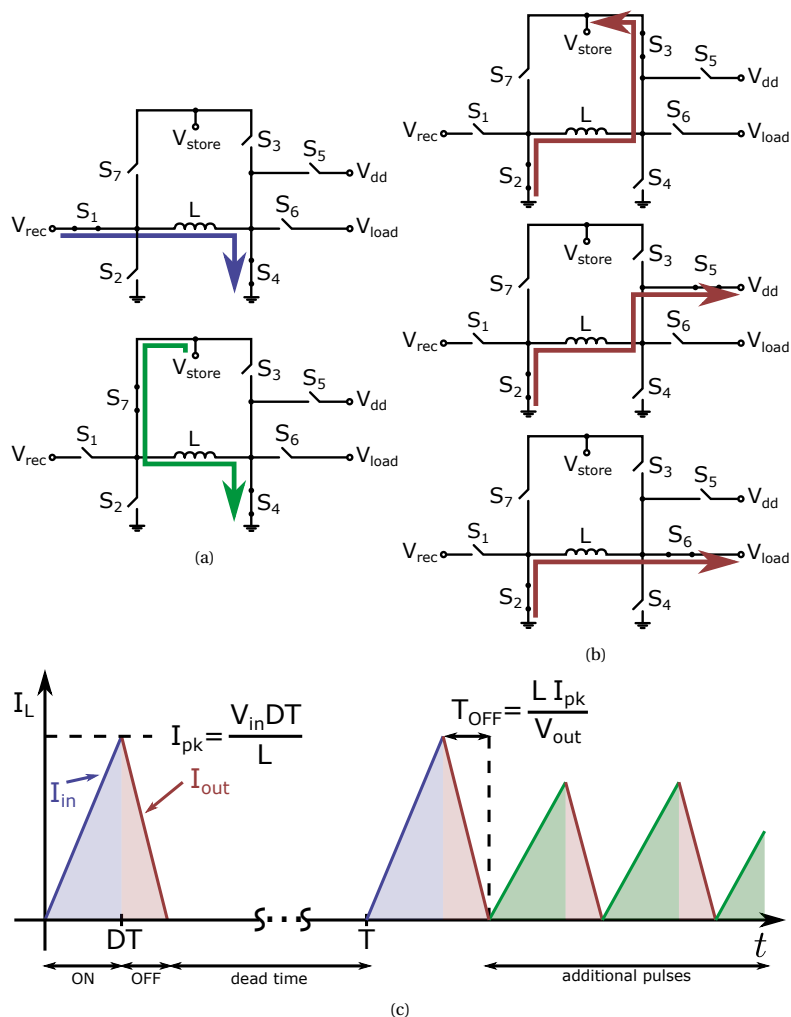


Figure 3.3: Buck-boost converter current flow: (a) ON time diagram, (b) OFF time diagram, (c) example of inductor current (in which V_{in} is either V_{rec} or V_{store} and V_{out} is V_{store} , V_{dd} or V_{load} , depending on the converter configuration).

is necessary to charge the load. In the example of Fig. 3.3(c), two different scenarios are portrayed. In the first scenario, the first current pulse is drawn from V_{rec} and the dead time starts immediately after it. This will happen when there is not enough energy in the system (either in C_{supply} or C_{store}) or when V_{load} is above the target voltage. In the second cycle, because V_{load} is below the target, additional pulses are drawn from V_{store} and directed to V_{load} . In this second scenario, the dead time will start only when V_{load} is above the target or V_{store} is below a critical level.

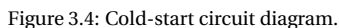
During the first pulse of current of every clock cycle, once the switches S_1 and S_4 are turned off, S_2 and one of the switches S_3 , S_5 or S_6 are turned on. If V_{dd} is below 1.8 V, S_5 is turned on. The charging of V_{dd} has the highest priority. If $V_{\text{dd}} > 1.8$ V and $V_{\text{store}} < 1.8$ V, switch S_3 is turned on to charge C_{store} . If V_{store} has reached 1.8 V and V_{load} is below the target level, which can be configured by the selection of R_1 and R_2 shown in Fig. 3.1, S_6 is turned on. The charging of V_{load} will continue until V_{store} drops below 0.4 V. This is done to guarantee that there is enough energy to supply the load for a minimum time. The monitoring of V_{store} is performed by a comparator with hysteresis. When the current pulse is finished, there will be a rising edge of V_{inb} , triggering the load voltage regulator. The regulator checks if the V_{store} monitor output is high (signaling there is still enough energy in C_{store}) and if the V_{load} monitor output is low (signaling that V_{load} is below the target level), through the signal V_{co} . If both conditions are met, S_7 and S_4 are turned on for a period equal to T_{ON} and, after they are turned off, the procedure explained above is repeated. Otherwise, the converter enters the dead time and all switches are kept off until the next clock cycle.

In this chapter we present the circuits and techniques that comprise the buck-boost converter. The blocks are the zero-current detector, supply-voltage controller, load-voltage controller, configurable power switches, oscillator and ON-time generator. We also present the cold-start circuit that is responsible for initially charging C_{supply} from a low V_{rec} voltage, so that V_{dd} reaches a voltage from which the buck-boost converter can operate correctly.

3.1. COLD-START CIRCUIT AND SUPPLY-VOLTAGE CONTROLLER

Before the buck-boost converter starts its operation, the system must start itself from a low input voltage and 0 V supply. This process is called cold start. A Dickson charge pump [26] is employed to boost V_{rec} and initially charge C_{supply} . This type of charge pump is preferred because it does not require a sharp clock signal and the clock phases do not need to be non-overlapping for its correct operation, which simplifies the oscillator design for low supply voltages.

The buck-boost converter can operate from $V_{\text{dd}} > 0.7$ V. This limit is set by its voltage and current reference generator. If this condition is satisfied, the converter can autonomously charge C_{supply} up to 1.8 V, the supply voltage limit of the technology, and maintain this supply voltage level, as long as there is sufficient energy available. To have some margin so that the buck-boost converter can initiate its operation and start charging C_{supply} before V_{dd} falls below 0.8 V, we initially charge C_{supply} from 0 V up to 1.1 V. To this end, the cold-start circuit presented in Fig. 3.4 is used. It comprises a Dickson charge pump with 10 stages, a ring oscillator, a non-overlapping clock generator, and a voltage monitor. Each stage of the charge pump consists of a diode connected PMOS



The voltage-monitor circuit turns off the cold-start circuit by switching off its connection to V_{rec} . This monitor must have a low power consumption, because it is supplied by a charge pump that has low output power in the worst-case scenario. This is because the cold-start charge pump and its oscillator operate with low input voltage, resulting in a low frequency and low voltage amplitude, therefore its input power and its efficiency are low. Furthermore, the voltage monitor is always on, even after the charge pump has been turned off, in order to detect whether V_{dd} has fallen below the critical level and, if this happens, turn on the cold-start process again.

The voltage-monitor core circuit is presented in Fig. 3.5. It consists of a comparator operating in weak inversion, a crude voltage-reference generator and a voltage divider that provides $V_{dd}/2$. When the voltage divider output is larger than the voltage reference, which happens for $V_{dd} > 1.1$ V, the cold-start circuit is disabled and the buck-boost converter is enabled. The cold-start circuit is enabled again if V_{dd} falls below 0.8 V. This hysteresis is built into the voltage monitor through switches M_1 and M_2 , which change the voltage reference to which $V_{dd}/2$ is compared to. When the voltage monitor output (POR) is low, M_1 is on and M_2 is off. When V_{dd} exceeds 1.1 V, POR rises, turning M_1 off and turning M_2 on. This feedback also increases the speed at which the output switches

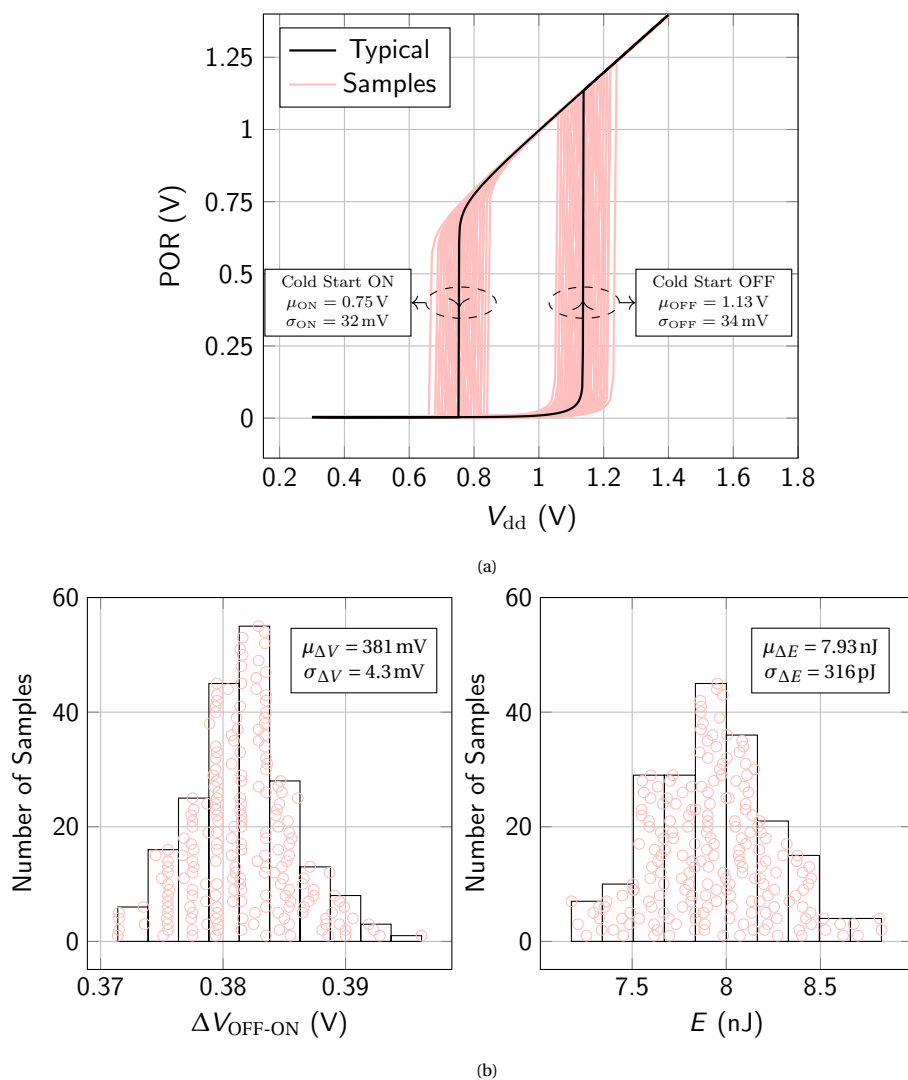


Figure 3.6: Monte-Carlo simulation results of the cold-start voltage monitor (200 samples): (a) Output variation as a function of the supply voltage, and (b) window size variation and its effect on the available energy in the capacitor.

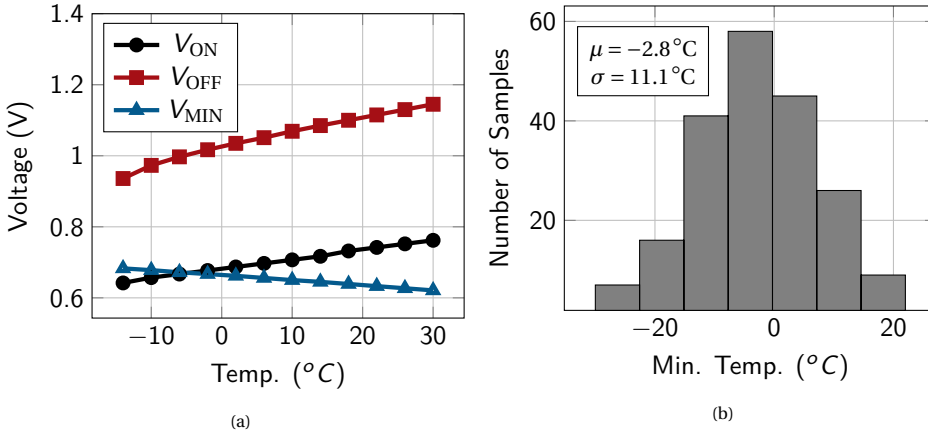


Figure 3.7: Variation of voltage levels V_{ON} , V_{OFF} , and V_{MIN} of the cold-start circuit across temperature. The cold start has full range of operation when $V_{ON} > V_{MIN}$: (a) typical case, and (b) Monte-Carlo simulation showing the minimum temperature (crossing point of V_{ON} and V_{MIN}).

$V_{OFF} - V_{ON}$ distribution is also presented. In the worst-case scenario (3σ), ΔE is about $0.318C_{supply} = 7\text{ nJ}$.

The typical value of V_{MIN} for which the buck-boost converter is able to recharge C_{supply} is about 0.63 V, at room temperature. This is due to the voltage-reference generator. If the voltage reference V_{ref} is too low, the voltage monitors will not function correctly, resulting in the wrong operation of the system and discharging of C_{supply} . V_{ref} is derived from the reference generator mentioned previously, which is an all-MOS reference generator [29]. The voltage and current references generated by this circuit are employed throughout the system. The variation of V_{MIN} , V_{ON} , and V_{OFF} with temperature is presented in Fig. 3.7(a), which shows that the system can safely start up for $T > -3^{\circ}\text{C}$. Fig. 3.7(b) presents the Monte Carlo simulation results for the minimum temperature from which the system can start up, which is the crossing point V_{ON} and V_{MIN} . As can be seen, the large variation with process is a big disadvantage of this circuit. This problem can be solved either by circuit trimming or by increasing the values of V_{OFF} and V_{ON} . The problem with the latter approach is that the cold-start circuit needs a larger area, because it needs more states to reach a higher voltage. Also the operating range of the system is reduced, because the minimum voltage has increased. Alternatively, the variation of the voltage monitor can be reduced by increasing its power consumption, with the penalty of reduced efficiency, specially at low input power levels.

Once the start-up process is complete, to keep the supply voltage above 1.8 V, current pulses must be directed to C_{supply} through switch S_5 , shown in Fig. 3.2. The V_{dd} voltage monitor, shown in the same figure, is used to detect if $V_{dd} < 1.8\text{ V}$. It consists of a latched comparator, and it compares a fraction of V_{dd} to the reference voltage V_{ref} every clock cycle. The V_{dd} monitor output is directed to the output demultiplexer in order to switch on and off S_5 when necessary. If $V_{dd} > 1.8\text{ V}$, S_3 or S_6 are operated (depending on the signal V_{co} , to be discussed later). In this way, charging C_{supply} has priority over charging the storage capacitor or the load. Fig. 3.8 shows the result of a cold-start transient sim-

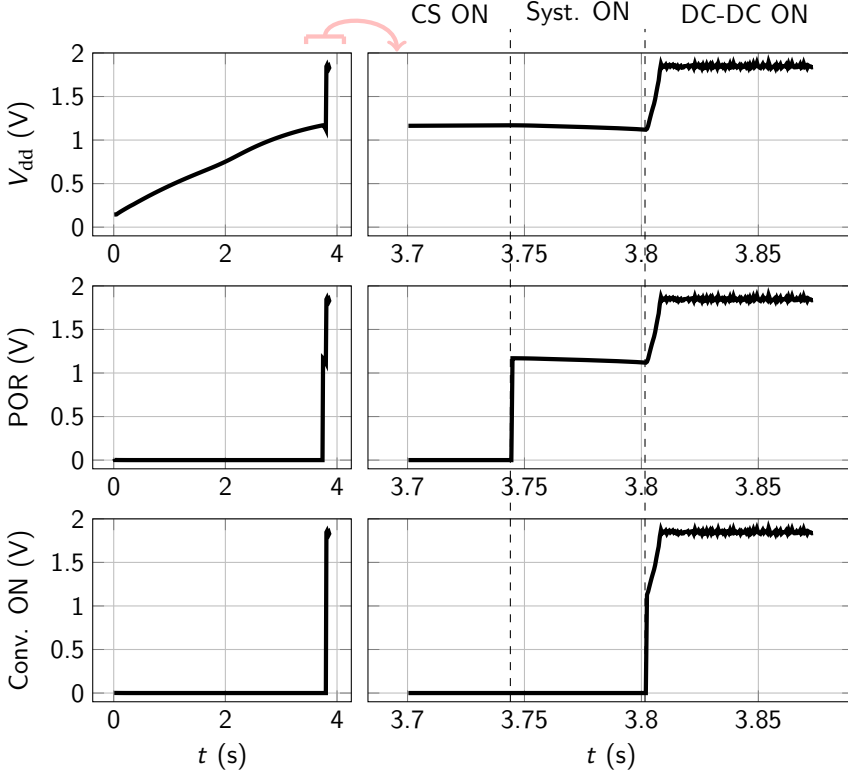


Figure 3.8: Transient simulation results of the cold-start process, and a zoom-in of the start-up sequence.

ulation. In this simulation, input voltage V_{rec} is set to 350 mV. The value of C_{supply} is set to 22 nF. At $t = 3.73$ s, the cold-start circuit is switched off (POR rises) and the system is still starting up. After a few clock cycles, at $t = 3.8$ s, the buck-boost converter is turned on, C_{supply} is charged further, and V_{dd} is kept above 1.8V.

3.2. ZERO-CURRENT DETECTOR

Since the buck-boost converter operates in DCM, there must be a mechanism in place to detect when the inductor current I_L falls to zero and to disconnect the inductor when this happens. This is necessary because, if I_L becomes negative, the output is discharged, introducing considerable losses. The zero-current detector (ZCD) performs this task. When the OFF time of the converter begins, the ZCD is activated. It detects when I_L drops to zero by comparing the voltage V_d , the voltage across the switch S_2 , to zero. Switch S_2 is always on during the ON time, independent of which output is being charged, which makes it convenient to monitor the voltage across it for zero-current detection. After the ZCD performed the detection, it deactivates itself, preventing unnecessary power consumption. At the same time, it starts the converter dead time by turning off S_3 , S_5 or

S_6 , depending on which one of them is activated at the time.

The ZCD is composed of a level shifter, a comparator and a controller, as shown in Fig. 3.9. The level shifter is employed to shift V_d and ground, creating the signals $V_{d,shift}$ and $V_{gnd,shift}$, which are at a level that is convenient to the comparator. The comparator will switch its output from low to high when $V_{d,shift}$ crosses $V_{gnd,shift}$, i.e., V_d crosses 0 V. It is a continuous-time comparator and it must have a small delay time to not degrade the system efficiency. The controller turns on the level shifter and comparator when the converter enters the OFF time and turns them off at the rising edge of the comparator output.

3.2.1. LEVEL SHIFTER

Two source followers, M_1 - M_2 , are used to shift the ground and V_d voltages by 0.9 V (half the value of V_{dd}) in order to present input signals to the comparator that are at an adequate level. Transistors M_3 - M_4 are used as current sources and transistors M_{s1} - M_{s4} are used to switch off the level shifter and to hold output voltages $V_{d,shift}$ and $V_{gnd,shift}$ when this block is not in use. The output is held to speed up the comparison, since $V_{d,shift}$ and $V_{gnd,shift}$ do not have to start from a too low or too high voltage during the level shifter start-up.

OPTIONAL OFFSET CONTROL

To increase the converter efficiency, an offset might be added to the detector in order to compensate for any delay in detecting the moment that I_L falls to zero. The presented ZCD employs an adaptive bias comparator that exhibits low delay, making the desired offset negligible. However, some systems might benefit from an offset to adjust the ZCD accuracy. Here we present a method for dynamic controlling the detector's offset in ZCDs in which the voltage offset is low but the propagation delay is considerable.

Considering that the change of the buck-boost converter output voltage V_{out} is negligible during a single OFF time, the slope of I_L during the OFF time is:

$$\frac{dI_L}{dt} = -\frac{V_{out}}{L}. \quad (3.4)$$

If we also consider that the ZCD has a fixed delay T_d , the value of I_L after the zero current detection has taken place (I_{L0}) can be calculated as:

$$I_{L0} = \frac{dI_L}{dt} T_d = -\frac{V_{out} T_d}{L}. \quad (3.5)$$

We can use the value of I_{L0} to define the offset voltage V_{offset} to be applied to the level shifter, remembering that V_d is equal to I_L times the R_{ON} of switch S_2 . The dependence of I_{L0} on V_{out} is illustrated in Fig. 3.10, in which the inductor current waveform is presented for two different values of V_{out} . In the case of a low V_{out} , when the offset is zero, $I_{L0} = I_{L0,1}$. Therefore, the offset should be set to $V_{offset,1}$. In the case of a higher V_{out} , $I_{L0} = I_{L0,2}$ and the offset should be set $V_{offset,2}$, which is a higher value.

Since V_d is proportional to I_L , an offset that is proportional to I_{L0} must be applied. Through (3.5), we can conclude that V_{offset} must be proportional to V_{out} , because L and T_d are constant. One way of creating this offset is by subtracting a current from the

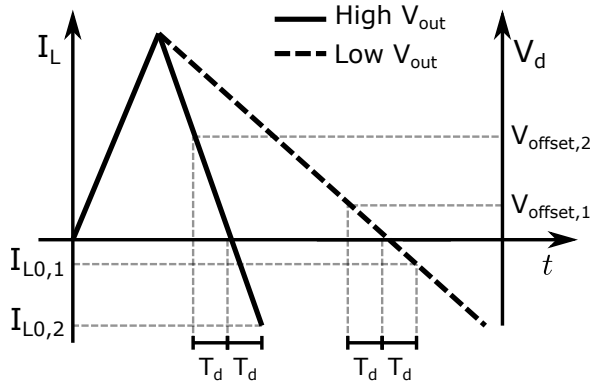


Figure 3.10: Slope of the inductor current and necessary offset with lower V_{out} and higher V_{out} .

branch that shifts the ground voltage. This is done through the resistor R_{offset} and the current mirror $M_{o1}-M_{o2}$, in Fig. 3.9. Even though the offset dependence of V_{out} is not linear when using this technique, V_{offset} increases with V_{out} and the circuit can be designed to produce the desired offset across a limited V_{out} range. It is a simple way to increase the power conversion efficiency of the system.

3.2.2. ADAPTIVE-BIAS COMPARATOR

Even though an offset can be created to mitigate delay effects, a better approach would be to make the ZCD comparator fast enough, so that its delay is negligible. Among the defining parameters of the comparator speed is its bias current [55]. One can increase the comparator's bias current in order to increase its speed. However, the bias current cannot be increased indefinitely because it impacts the power consumption. To overcome this problem, we introduce an adaptive-bias comparator whose bias current changes with its differential input voltage V_{in} . The main idea is the following: when the inductor current I_L is far above zero, V_{in} is large and the comparator bias current is low. When I_L is coming closer to zero, V_{in} is coming close to zero as well and the bias current increases, making the comparator faster when it is necessary. This technique allows for a fast detection while reducing the average power consumption [52].

The comparator circuit schematic is presented in Fig. 3.9. It is a three-stage amplifier based on the adaptive-bias amplifier presented in [56]. We introduce a differential pair and a degeneration resistor to the amplifier's feedback loop. As we will show in this section, these modifications allow for the increase of the current feedback factor A , reducing the average power consumption while keeping the same delay.

The comparator's first stage is biased by a fixed current set by M_5 and an adaptive current set by M_{15} . The feedback loop that adjusts the adaptive current is formed by $M_{10}-M_{15}$ and R_S . When I_L is positive, $V_{d,shift}$ is below $V_{gnd,shift}$ and the drain current I of M_7 is low. At this moment, the source voltage of M_{10} is low, so I is effectively mirrored and flows through the differential pair $M_{11}-M_{12}$. This differential pair will make the feedback current increase more sharply when V_{in} gets closer to zero. The drain current of M_{11} is multiplied by a factor A and added to the tail current through the current mirror formed



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equation becomes:

$$\sqrt{\frac{2I}{\mu_n C_{ox}(W/L)_9}} = \sqrt{\frac{8I}{\mu_n C_{ox}(W/L)_9 A}} + R_S \frac{4I}{A}. \quad (3.8)$$

Isolating I , we obtain:

$$I = \frac{A^2}{8\mu_n C_{ox}(W/L)_9} \frac{1}{R_S^2} \left(1 - \frac{2}{\sqrt{A}}\right)^2, \quad (3.9)$$

which shows that the circuit is stable for any value of A . However, in practice, increasing A indefinitely will not lead to less power consumption for the same delay of the converter. This is due to the increase of the parasitic capacitances of the current mirror formed by M_{15} and M_{13} , which will become dominant for a large value of A .

POWER CONSUMPTION COMPARISON

To illustrate the advantage of the proposed circuit, Fig. 3.12 presents the current consumption of three different comparators, labeled C1 to C3. All the comparators are designed to have the same delay. Comparator C1 is designed with $A = 2$, without the differential pair in the feedback loop, and without R_S . Comparator C2 has $A = 4$, the differential pair in the feedback loop, but R_S is not included (i.e., equals 0). Comparator C3, the proposed one, uses $A = 8$, $R_S = 40\text{ k}\Omega$, and the differential pair in the feedback loop. As shown in Fig. 3.12, the addition of the extra differential pair in C2 and the increase of A makes the curve of the current consumption I_{cons} versus the differential input voltage steeper when close to $V_{\text{in}} = 0\text{ V}$. This leads to power saving, compared to the case of C1, because more time is spent in a situation of low I_{cons} , while the peak tail current (and therefore I_{cons}) is similar. Furthermore, the addition of R_S and further increase of A , in C3, leads to the reduction of the tail current when $V_{\text{in}} \ll 0\text{ V}$, while obtaining a similar I_{cons} when $V_{\text{in}} = 0\text{ V}$.

The energy consumption will finally depend on the waveform of V_{in} . For the case of the ZCD, the peak V_{in} depends on the peak inductor current. The value of V_{in} increases linearly with time as the inductor current falls to zero. To compare the three topologies, we apply a V_{in} signal that takes 100 ns to rise from -50 mV to 0 mV , which is a common scenario during conversion. Each comparator is presented with a capacitive load of 50 fF . With a 1.8 V supply, the energy consumed by C1, C2 and C3 are 4.8 pJ , 3.1 pJ and 1.7 pJ , respectively. Which means that the comparator C3 presents 45% less power consumption than C2 and 65% less than C1. When considering the present system, in which the switching frequency varies from 10 kHz to 2 MHz and the DC-DC converter input power varies from $1\text{ }\mu\text{W}$ to 2 mW , the peak DC-DC PCE is increased by roughly 3% when using C3 (in comparison to using C1).

NOISE COMPARISON

To evaluate the effects of the presented technique on noise, it is interesting to calculate the input referred noise voltage, since we can relate it to the inductor current and, therefore, the power loss. The input referred noise voltage spectral density is given by:

$$\frac{v_{\text{ni}}^2}{\Delta f} = \frac{2}{g_{m7}^2} \left[i_{n7}^2 + i_{n9}^2 + \frac{i_{n5}^2 + i_{n15}^2}{4} + \frac{i_{n11}^2 + i_{n13}^2 + i_{nRs}^2}{4A^2} \right] \frac{1}{\Delta f}, \quad (3.10)$$

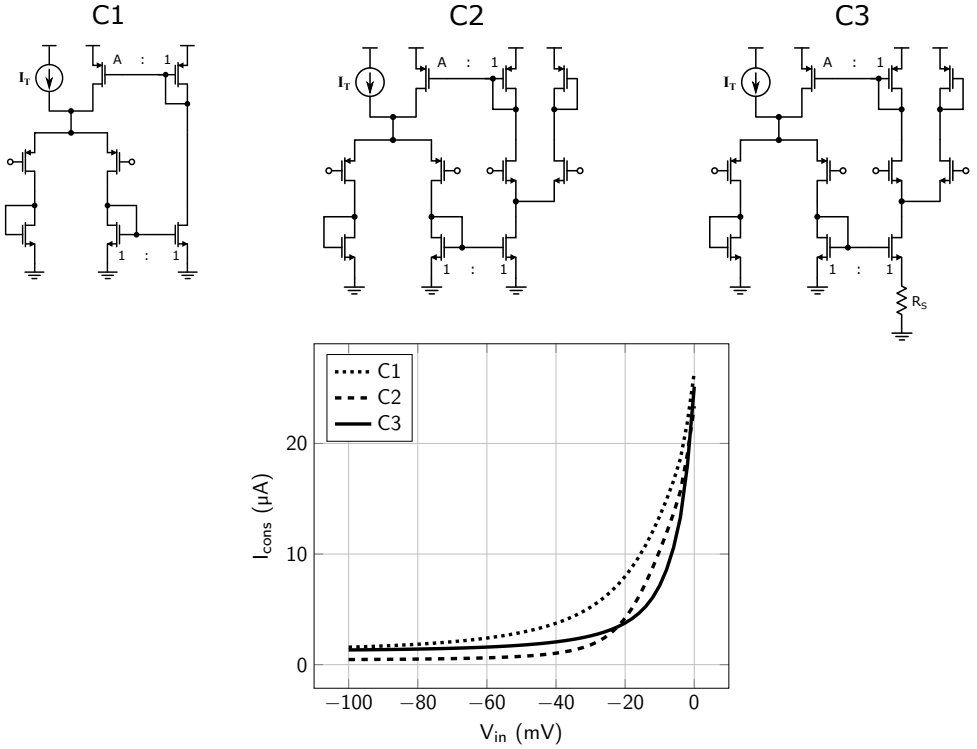


Figure 3.12: Comparison of three different comparators using different versions of the adaptive-bias technique.

in which i_{ni} is the channel noise current of transistor M_i .

There is additional noise coming from the feedback loop. However, usually the differential input pair noise is dominant, and i_{n7}^2 and i_{n9}^2 are dominant in (3.10). If this is the case, the additional noise can be neglected.

OFFSET COMPARISON

The comparator voltage offset directly affects the DC-DC converter PCE, in the same manner as the input referred noise. Offset due to gradients of physical parameters across the chip can be minimized by adequate layout techniques [57]. Nevertheless, random mismatch is still present due to fluctuations of those parameters. It can be shown that the standard deviation of the average values difference of such parameters is [58]:

$$\sigma(\Delta P) = \frac{A_P}{\sqrt{WL}}, \quad (3.11)$$

in which A_P is the area proportionality constant for parameter P , which is technology dependent. Therefore, increasing the area (W and/or L) of the transistors in the comparator will reduce mismatch.

Regardless of layout techniques and transistor area, current and voltage mismatches in the MOSFET also depends on its drain current. The gate-source voltage mismatch is

related to the differential input voltage of the comparator. The standard deviation of the average value difference of the gate-source voltage is given by [57, 59]:

$$\sigma(\Delta V_{gs}) = \sqrt{\sigma^2(\Delta V_t) + \left[\frac{I_D}{G_m} \frac{\sigma(\Delta\beta)}{\beta} \right]^2}, \quad (3.12)$$

in which V_t is the threshold voltage and $\beta = \mu C_{ox} W/L$. This equation assumes that ΔC_{ox} is negligible, making ΔV_t and $\Delta\beta$ uncorrelated, and that Δn is also negligible. Similarly, the drain current mismatch in the current mirrors of the comparator can be described by [57, 59]:

$$\frac{\sigma(\Delta I_D)}{I_D} = \sqrt{\left[\frac{\sigma(\Delta\beta)}{\beta} \right]^2 + \left[\frac{G_m}{I_D} \frac{\sigma(\Delta\beta)}{\beta} \right]^2}. \quad (3.13)$$

In strong inversion saturation, due to the decrease of G_m/I_D with I_D , increasing the comparator bias current (increasing I_D), decreases the current mismatch and increases the voltage mismatch.

For a large I_D , the current mismatch becomes negligible and the voltage mismatch becomes dominant. Since the bias current is proportional to the comparator speed, there is a trade-off between speed and mismatch. Therefore, a balance must be made in order to not degrade the DC-DC converter efficiency when increasing the ZCD speed. Alternatively, a calibration process can be applied after fabrication. The calibration might be done by, for example, laser trimming or an external biasing. Additional circuit techniques, such as auto-zeroing, may also be applied. Both alternatives will add to the cost and complexity of the system.

ENABLING/DISABLING THE COMPARATOR

Transistors M_{s5} - M_{s16} , in Fig. 3.9, act as switches that turn the comparator on or off when EN is high or low, respectively. They turn off the currents in all branches when the comparator is off in order to avoid any current consumption when the comparator is not needed. When the comparator is turned off, these switches also ensure that the output voltage is high and capacitor C is discharged. When the comparator is turned on, they initially bring the output of the comparator to ground by connecting C to the output node. Initially, $V_{d,shift}$ and $V_{gnd,shift}$ are close to each other as there is a small settling time until they reach their correct values. During this time, the comparator is also starting up and will not be able to bring its output voltage high. When the comparator bias current is high enough, its inputs are already brought further apart ($V_{d,shift} < V_{gnd,shift}$). This behavior ensures that the comparator output is always at a known level and that it will always present a rising edge, which is necessary for the correct operation of the switch controller, as will be explained in the next section.

3.2.3. SWITCH CONTROLLER

The switch controller block switches the level shifter and the adaptive-bias comparator on and off, and generates signal V_{gh} that controls the output switches (S_3 , S_5 , and S_6). Furthermore, this block provides signal V_{inb} , which is used in the load voltage regulator block and indicates when there is no current flowing through the inductor. This signal is used in the load voltage regulator block, introduced in Section 3.5.

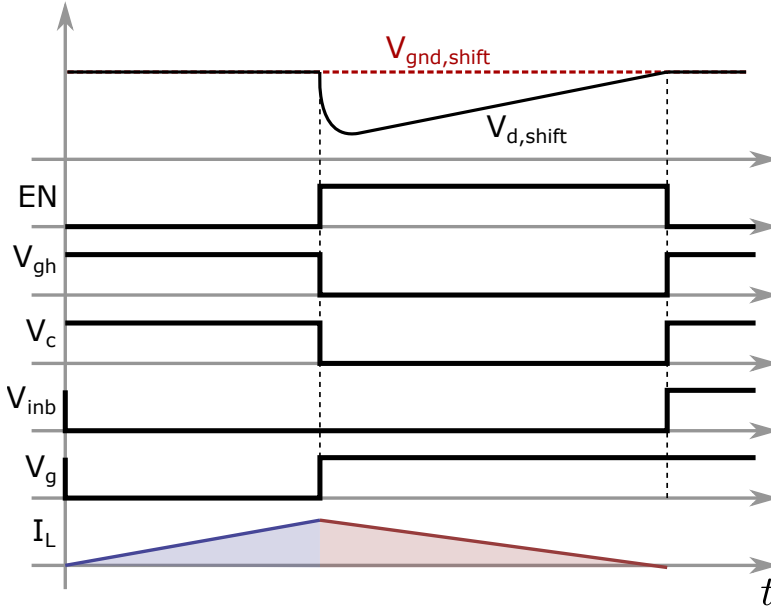


Figure 3.13: Timing diagram example of the signals related to the switch controller block.

Fig. 3.13 shows an example timing diagram of the signals related to the switch controller. The inputs of the controller block are the ZCD comparator output and signal V_g . When V_g drops to logic value '0', the ON time of the DC-DC converter begins. At this moment, the flip-flop in the switch controller (see Fig. 3.9) is cleared, setting V_{inb} to '0', which disables the level shifter and the comparator and sets V_{gh} to '0'. When V_g rises, the OFF time of the DC-DC converter begins. The level shifter and the comparator are enabled, initially setting the comparator output to '0' and V_{gh} to '0'. The level shifter and the comparator are enabled, initially setting V_c to '0' and V_{gh} to '0' (turning on the output power switches). When the inductor current crosses zero, V_c rises to '1', setting the flip-flop output to '1', which disables the level shifter and the comparator. At this moment, V_{gh} returns to '1' (turning off the output power switches and preventing negative inductor current) and the ZCD returns to its initial state.

In the case that initially there is no inductor current (or it is very low), the comparator output should be '1' (or should become '1' shortly) when the comparator is enabled. It is important that the comparator output is initially set to '0' to ensure that there will always be a rising edge. Otherwise, there would be no edge and a large reverse current would build up. This is the reason for the comparator output to be pre-discharged to ground, as discussed in the previous section.

3.3. CONFIGURABLE POWER SWITCHES

The major contributors to the power losses in a switched-mode converter are the conduction loss (P_{cond}), switching loss (P_{sw}), shoot-through loss (P_{sh}) and the power loss

due to the power consumption of the control circuits (P_q) [60]. Therefore, the total power loss can be approximated by:

$$P_{\text{loss}} \approx P_{\text{cond}} + P_{\text{sw}} + P_{\text{sh}} + P_q. \quad (3.14)$$

Considering that P_{sh} is mitigated by careful design and simulation of the power switches, their drivers and their driving signals, and that P_q can be scaled down with input power by using circuit techniques such as the ones presented in this chapter, P_{loss} is minimized by balancing P_{cond} and P_{sw} . For a given fabrication technology and available off-chip passive components, there is a minimum P_{loss} that is achieved by balancing P_{cond} and P_{sw} . To find this balance, we need to analyse both terms separately. For the sake of simplicity, we consider, in this analysis, that only switches S_1 - S_4 are present in the buck-boost converter and that the input and the output are V_{rec} and V_{store} , respectively. Therefore, in DCM, P_{cond} is given by:

$$P_{\text{cond}} = \frac{I_{\text{pk}}^2}{3T} (T_{\text{ON}} R_{\text{ON}} + T_{\text{OFF}} R_{\text{OFF}}), \quad (3.15)$$

$$R_{\text{ON}} = R_1 + R_3 + R_L + R_C, \quad (3.16)$$

$$R_{\text{OFF}} = R_2 + R_4 + R_L + R_C, \quad (3.17)$$

in which I_{pk} denotes the inductor peak current, R_{ON} is the total resistance in the current path during the ON time and, and R_{OFF} is the total resistance during the OFF time. The resistances R_{ON} and R_{OFF} can be broken down into the parasitic resistances of the components: R_1 - R_4 are the ON resistances of the switches, R_L is the inductor series resistance, and R_C is the capacitor series resistance. To make the relation between P_{cond} and the switching frequency clear, we can replace I_{pk} , which depends on T , by $\sqrt{2P_{\text{in}}T/L}$. This is an approximation, since it does not account for the losses, but allows us to calculate P_{cond} for a given input power. Furthermore, T_{ON} and T_{OFF} can be replaced by DT and $DT(V_{\text{in}}/V_{\text{out}})$, respectively. These modifications lead to:

$$P_{\text{cond}} \approx \frac{2}{3} \frac{P_{\text{in}}}{L} DT \left(R_{\text{ON}} + \frac{V_{\text{in}}}{V_{\text{out}}} R_{\text{OFF}} \right), \quad (3.18)$$

in which the duty cycle, D , is given by:

$$D = \frac{1}{V_{\text{in}}} \sqrt{\frac{2LP_{\text{in}}}{T}}. \quad (3.19)$$

This shows that P_{cond} decreases with the switching frequency ($P_{\text{cond}} \propto \sqrt{T}$) for constant input power, and constant input and output voltages. It is also shown in (3.18) that P_{cond} decreases when wider switches are employed (R_1 - R_4 decrease with transistor width).

Switching losses are mainly due to the charging and discharging of the gate and drain capacitances [61, 62]. The resulting total switching loss can be calculated as:

$$P_{\text{sw}} = \frac{1}{T} (V_{\text{dd}}^2 C_g + V_{\text{d}}^2 C_d + V_{\text{o}}^2 C_o), \quad (3.20)$$

in which C_g is the sum of all gate capacitances charged in a cycle, V_{dd} (the supply voltage) is the voltage to which they are charged, C_d is the total drain capacitance of the switches

Table 3.1: Power transistors width. The selected length is 0.18 μm , the minimum allowed by the technology.

| | M_{HP1} | M_{LP1} | M_{HP2} | M_{LP2} | M_{HP3} | M_{LP3} | $M_{LP3,N}$ | M_{HP4} | M_{LP4} |
|---------------------|-----------|-----------|-----------|-----------|-----------|-----------|-------------|-----------|-----------|
| W (μm) | 560 | 60 | 125 | 25 | 360 | 56 | 12 | 75 | 75 |

connected on the input side of the converter, and C_o is the total drain capacitance of the switches connected on the output side. The voltages V_d and V_o are the voltages to which those capacitances are charged and discharged every cycle. Hard switching losses, which are due to the non-zero voltage-current overlap that exists across a switch when it is switched off, and reverse recovery losses, which are due to energy dissipated when a body diode is switched from reverse-biased to forward-conducting mode, are also present in the converter [60], but they are less pronounced. They play a larger role in high-power converters [63, 64]. Nevertheless, the switching losses are proportional to the switching frequency and to the width of the switches, contrary to the conduction losses.

Considering the analysis of P_{cond} and P_{sw} , there are a switching frequency and transistors widths that present the lowest P_{loss} for given passive components, fixed input power, and fixed input and output voltages. When the power varies over a wide range, this balance can be obtained in multiple ways, such as the simultaneous modulation of pulse width and frequency [65], the adaptation of the supply voltage of the gate drivers [66], or the dynamic control of the number of transistors in parallel that compose the switches [67–69].

The pulse width modulation approach is not convenient in this case, since it adds an extra varying quantity (D) to the equivalent input resistance of the buck-boost converter, as seen from (3.2). This would complicate the design of the input power estimation circuit on the MPPT circuit (see Chapter 4) and eventually increase the power consumption necessary to perform this task. Varying the supply voltage of the buffers that drive the power switches requires additional DC-DC regulators to generate the different voltage levels. A simpler and more power-efficient approach is to control the number of transistors in parallel that form the power switches. Fig. 3.14 presents the schematics of the implemented switches, S_1 - S_4 . Table 3.1 presents the dimensions of the power transistors. Differently from previous works, the transistor type used in the input switch must be changed as well. This is due to the variation of input voltage with respect to the input power. For higher input power, a PMOS transistor is used in S_1 . When the control bit V_{hp} is set to '1', the high-power mode is activated and all transistors are used in the switches. Otherwise, only M_{LP} is switched while M_{HP} is kept off. The control bit V_{hp} is derived from the MPPT output, since it is associated with the input power level.

Fig. 3.15 shows the conversion efficiency of the buck-boost converter when using the presented method and how it compares to the same converter using conventional switches. In the figure, the low-power mode (LPM) and high-power mode (HPM) are the modes in which the configurable switches are used but V_{hp} is kept constant, either high or low. The combination of both modes (CM) is the desired operation mode, in which V_{hp} is set to obtain the configuration that presents the highest efficiency. For the sake of comparison, the results for the comparator using conventional switches that are designed for low power (LPCS) and for high power (HPCS) are also presented. In the

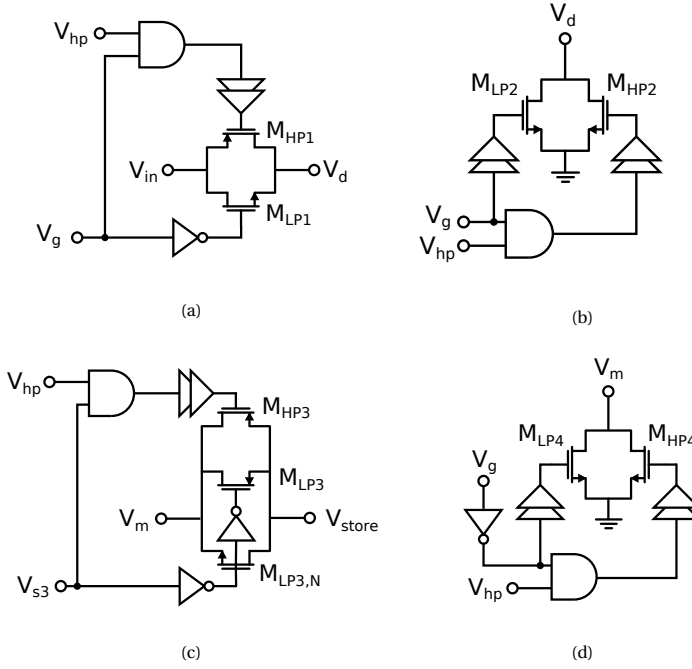


Figure 3.14: Circuit schematics of the configurable switches for balancing conduction and switching losses.

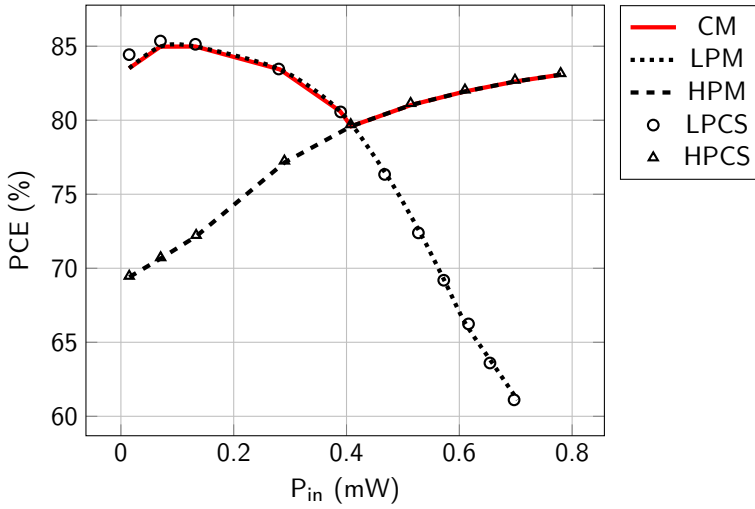


Figure 3.15: Simulation results of the low-power mode (LPM) and high-power mode (HPM) of the configurable switches, the combination of both modes (CM) and the converter employing conventional switches (LPCS and HPCS).

simulation, the output voltage is set to 1.8 V. The input voltage is varied from 0.3 to 1.3 V, according to rectifier simulation results (its optimum output voltage increases with the input power), i.e., for every value of input power there is a corresponding value of input voltage. It is observed that the low-power mode presents much lower efficiency at higher input power. This happens because the input switch is a single NMOS transistor. Therefore, the conduction losses increase considerably with the increase of input voltage. It can also be seen that the LPCS converter performs slightly better at low power. This is due to the output capacitance charging losses of M_{HP} , which are present even when the transistor is not being switched. The performances of the HPCS and the HPM converters are the same, since their parasitics are the same.

3.4. OSCILLATOR

As seen in (3.2), the average input resistance of the DC-DC converter is proportional to the switching frequency. This frequency is set by the oscillator presented in Fig. 3.16. The frequency control signal, FC, is a 9-bit word in thermometric scale and is generated by the MPPT circuit. It controls a set of switches, changing the bias current of the oscillator. The aspect ratios of transistors M_{B0} - M_{B8} are selected to present a bias current that increases by a factor of about 1.7 times for each incremental step of FC. This value is chosen considering the sensitivity of the input power estimation circuit of the MPPT (with a low factor, it is difficult to sense the difference in input power) and the power conversion efficiency (with a high factor, there are fewer possible oscillator frequencies, reducing the MPPT efficiency).

A Schmitt trigger compares the voltage across capacitor C_{osc} with $V_{dd}/2$, controlling whether the current is fed to or drained from C_{osc} . The schematic of this block is presented in Fig. 3.17. The adaptive bias technique, presented previously in this chapter, is also used in this circuit in order to speed up the comparison and reducing the oscillator power consumption. The additional differential pair M_3 - M_4 has aspect ratio $(W/L)_{3,4} = 1/5(W/L)_{1,2}$, in order to create scaled copies of the main differential pair drain currents and to create the positive feedback to the tail current. Which drain current is going to be used for the feedback, from M_3 or M_4 , is selected depending on the direction to which the input V_c is moving towards. This is determined by the output signal clk. This signal controls switches M_{S1} and M_{S2} , which turn on and off the current mirrors M_9 - M_{10} and M_{11} - M_{12} . Therefore, when clk is high, which happens during the period that C_{osc} is discharging and V_c is lowering, current mirror M_{11} - M_{12} is on (M_9 - M_{10} is off) and the comparator tail current increases as V_c decreases. This decreases the clk propagation delay from high to low, which is when the Schmitt trigger reaches its lower trip point. When clk is low, the opposite happens. Current mirror M_9 - M_{10} is on (M_{11} - M_{12} is off) and the tail current increases with V_c . This decreases the clk propagation delay from low to high, which is when the Schmitt trigger reaches its higher trip point.

3.5. LOAD-VOLTAGE REGULATOR

The clock signal generated by the oscillator is processed by the load voltage regulator, which controls which input of the DC-DC converter is active, through signal V_{ci} , and generates signal clk', which is fed to the ON-time generator. Within a clk period, signal

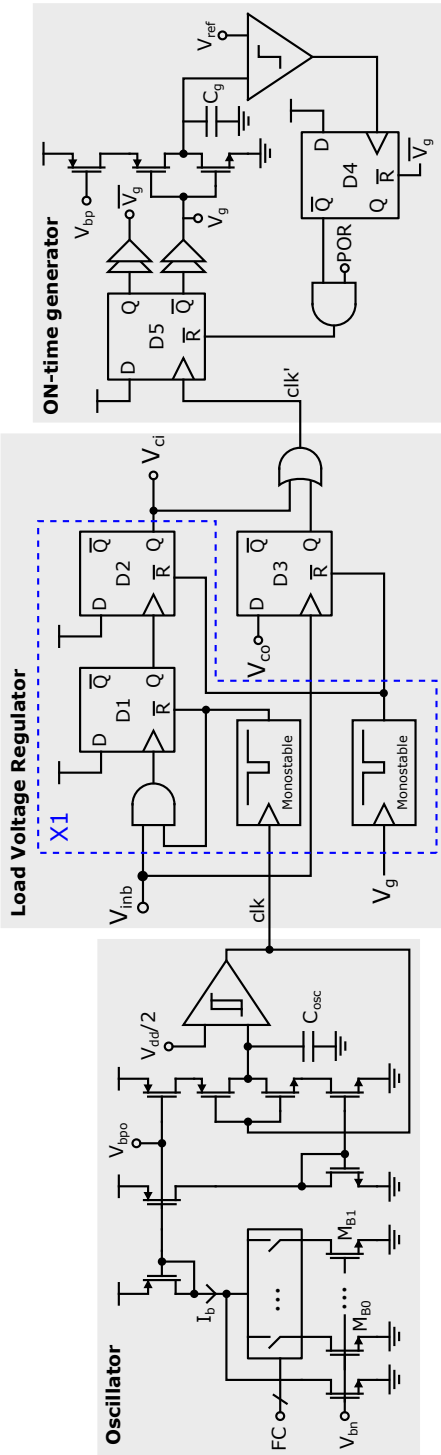


Figure 3.16: Oscillator, load regulator, and ON-time generator circuit diagram.

clk' contains a first rising edge, which starts a current pulse from input V_{rec} , and additional rising edges while $V_h < V_{\text{ref}}$, which start current pulses for load voltage regulation. To regulate V_{load} , voltage V_h is compared to a reference voltage V_{ref} by a latched comparator controlled by V_g , which means that the comparison is performed every current pulse. Voltage V_h is derived from V_{load} through the resistive divider formed by R_1 and R_2 in Fig. 3.2. If $V_h < V_{\text{ref}}$, the pulse of current is directed to V_{load} . If $V_h > V_{\text{ref}}$, the converter enters the dead time until the next rising edge of the clock. This type of regulation is possible because the buck-boost converter operating in DCM has a single pole at low frequencies, making the system intrinsically stable [44].

The first current pulse after every clock rising edge comes from V_{rec} , in order to keep the energy harvesting rate constant. This means that V_{ci} is '0' only once every clock period and it is '1' during the subsequent pulses within the clock period. However, if a clock rising edge happens and the inductor is being used, the charging cycle must be completed before a new current pulse is drawn from V_{rec} . By doing so, it is guaranteed that the inductor current is zero before connecting the inductor to V_{rec} and that the converter's R_{in} is maintained. This behaviour is ensured by sub-circuit X1 in Fig. 3.16. If there is a current pulse during the clock rising edge ($V_{\text{inb}} = '0'$), it waits for it to be finished. Once the current pulse is finished or if there is no inductor current on the clock rising edge, it sets $V_{\text{ci}} = '1'$ and generates a clk' rising edge. Once the current pulse during which $V_{\text{ci}} = '1'$ is finished, V_{ci} is set back to '0'.

At circuit level, sub-circuit X1 works in the following manner:

1. The clock rising edge resets D1.
2. If $V_{\text{inb}} = '1'$ (the inductor is not being used), D1 is immediately set to '1'. Otherwise, D1 will be set once V_{inb} rises.
3. When D1 is set, it triggers D2, setting V_{ci} to '1'

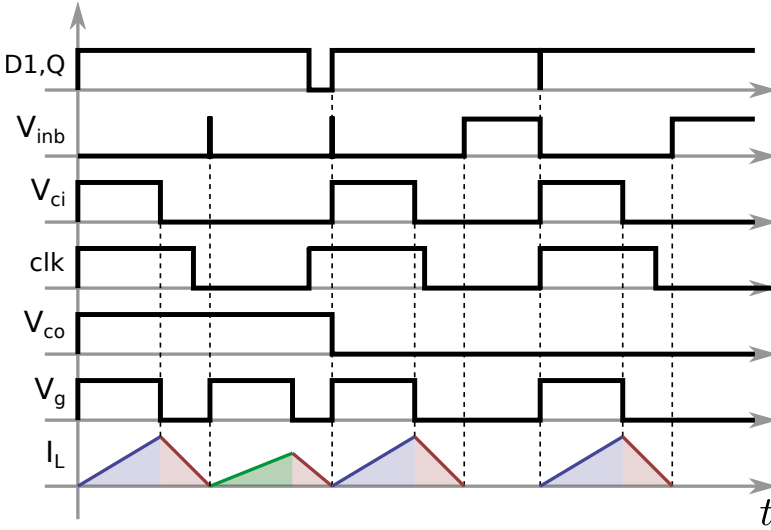


Figure 3.18: Example of the load voltage regulator signals.

4. When V_{ci} rises, it triggers the ON-time generator, which will start the current pulse by lowering V_g .
5. When V_g rises, it resets D2. This means that $V_{ci} = '1'$ during one ON time within a clock cycle and then it is set to '0'.
6. This process is repeated on the next clock rising edge.

If V_{co} is high (V_{load} is below the target), additional current pulses are triggered through flip-flop D3. Once the current through the inductor crosses zero, V_{inb} rises, setting D3 and creating a clk' rising edge. Since V_{ci} is always '0' when this happens, the current pulse is drawn from V_{store} . This circuit creates a loop that stops once V_{load} is above the target voltage (V_{co} is low).

Some of the digital signals discussed here, along with the inductor current, are presented in Fig. 3.18 for clarification. In this example, V_{load} reaches the target voltage after the second current pulse (V_{co} falls to '0'). During the second current pulse, a clk rising edge happens and a current pulse drawn from V_{rec} starts when V_{inb} rises. The third clk rising edge arrives when there is no inductor current, therefore a current pulse drawn from V_{rec} starts immediately.

One important aspect of load regulation is the load voltage ripple. Some systems require low supply voltage ripple for correct operation. The ripple can be minimized by increasing capacitance C_{load} . However, it must be much smaller than C_{store} . Otherwise, duty cycled operation is not possible, since there will not be enough energy in C_{store} to charge C_{load} . Therefore, if C_{load} has to be increased, C_{store} must be increased with it. While doing so, it is important to take in consideration the additional leakage of the capacitors, which will compromise the system PCE at low input power levels.

3.6. ON-TIME GENERATOR

The ON-time generator produces a pulse with a 440 ns width by charging capacitor C_g and comparing its voltage to reference V_{ref} . Its circuit schematic is presented in Fig. 3.16. The current that charges C_g and voltage V_{ref} are derived from the reference generator.

Before the system starts up, the power-on reset signal, POR, is '0', ensuring V_g is set to '1'. Signal POR becomes '1' when V_{dd} is high enough, enabling the ON-time generator is enabled. At every rising edge of clk' , V_g is set to '0', allowing the charging of C_g with a constant current. When the voltage across C_g surpasses V_{ref} , the comparator output rises, triggering flip-flop D4, which resets flip-flop D5. This causes V_g to return to '1', finishing the ON time. Therefore, the T_{ON} pulse width is the time it takes for the voltage across C_g to reach V_{ref} starting from 0 V.

The comparator used in this block has the same topology as the one used in the ZCD (Fig. 3.9). It is turned on at the beginning of the ON-time, when V_g drops to '0', and turned off at the end of the ON-time, when V_g rises to '1'.

3.7. SIMULATION RESULTS

The simulation results of the DC-DC converter are presented in this section. Since the converter is continuously charging and discharging the storage capacitor (in the case of the duty cycled load), it must present good power conversion efficiency results for a varying output voltage V_{store} . Fig. 3.19 presents the simulated PCE of the DC-DC converter for V_{store} ranging from 0.2 to 1.8 V and a input power ranging from 1 μ W to 1 mW. Its peak efficiency is 76.3% at $P_{in} = 1 \mu$ W and 86.3% at $P_{in} = 1$ mW. A lower efficiency at low V_{store} is observed because the output power switches are not optimized for low output voltages. An additional NMOS transistor in parallel to the output switch would be necessary to increase this efficiency. However, V_{store} is above 0.4 V in normal operation and most of the time it is at a high voltage level.

Fig. 3.20 presents transient simulation results of the inductor current in two different scenarios. In the first scenario, presented in Fig. 3.20(a), C_{load} is not being charged, resulting in a single current pulse for each clock cycle. The inductor is charged from V_{rec} and its current is used to charge C_{store} in this scenario. In the second scenario, presented in Fig. 3.20(b), C_{load} is being charged. The inductor is still charged from V_{rec} once per clock cycle (the shorter current pulses), but additional charges are drawn from V_{store} (the larger current pulses) until C_{load} is fully charged. As explained previously in this chapter, this behaviour keeps the input impedance as seen from V_{rec} constant while the load is being charged with energy that comes from both V_{rec} and V_{store} .

Fig. 3.21 presents the converter PCE when charging the load. The input power (delivered at V_{rec}) ranges from 1 μ W to 1 mW and the load current ranges from 2 μ A to 20 mA. The target voltage for V_{load} is set to 1.2 V. The value of C_{store} is set as 10 times C_{load} . The PCE is defined as:

$$PCE = \frac{\overline{P_{load}}}{\overline{P_{in}}} = \frac{\overline{V_{load} I_{load}}}{\overline{P_{in}}}. \quad (3.21)$$

The system keeps P_{in} constant. The load current is modeled as duty cycled load that is turned on whenever $V_{load} > 1.1$ V. Therefore, P_{load} is averaged over a full cycle. The cycle starts when C_{store} starts being charged, which happens when V_{store} drops below 0.4 V.

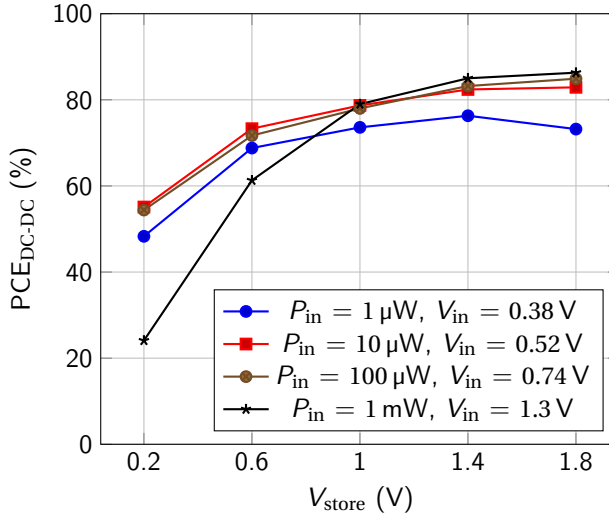


Figure 3.19: Efficiency results of the buck-boost converter for various output voltages and input power levels.

This process is shown in Fig. 3.22, for $P_{\text{in}} = 10 \mu\text{W}$ and $I_{\text{load}} = 200 \mu\text{A}$. When V_{store} reaches 1.8 V, the load charging starts, the load current is activated, and C_{store} is discharged. The cycle ends as soon as V_{store} crosses 0.4 V again. Therefore, the two conversion steps are considered in the PCE calculation: from V_{rec} to V_{store} , and from V_{store} to V_{load} . Only the scenarios when $\overline{P_{\text{load}}} > P_{\text{in}}$ are considered. When P_{load} is too small, C_{store} is not discharged and V_{store} increases indefinitely, since there is no over-voltage protection in the implemented system. If an additional over-voltage protection is used, V_{store} stops increasing and C_{load} is charged directly from V_{rec} .

3.8. CONCLUSIONS

In this chapter, we presented circuit techniques to be used in a DC-DC converter employed in RF energy harvesting. The presented DC-DC converter is a buck-boost converter operating in DCM, which has an input resistance that is not dependent on its output voltage. This characteristic makes it easier for the MPPT circuit (presented in Chap. 4) to control the converter in the presence of a varying output voltage, which is the case for a duty-cycled load supplied by a storage capacitor. Furthermore, the DCM operation facilitates the design of the presented SIDITO buck-boost converter, since the inductor current always falls to zero after each cycle, it is simple to switch inputs and outputs. The presented topology uses a single inductor to charge the storage capacitor, to provide the supply voltage for the DC-DC converter circuits, and to supply the load, while presenting little area overhead.

The circuits presented in this chapter aim to reduce the power consumption and increase the PCE of the DC-DC converter across a wide input power range. The following circuits were discussed: (a) a low-power voltage monitor for cold-start operation, (b) an adaptive-bias converter for zero-current detection, (c) configurable power switches for

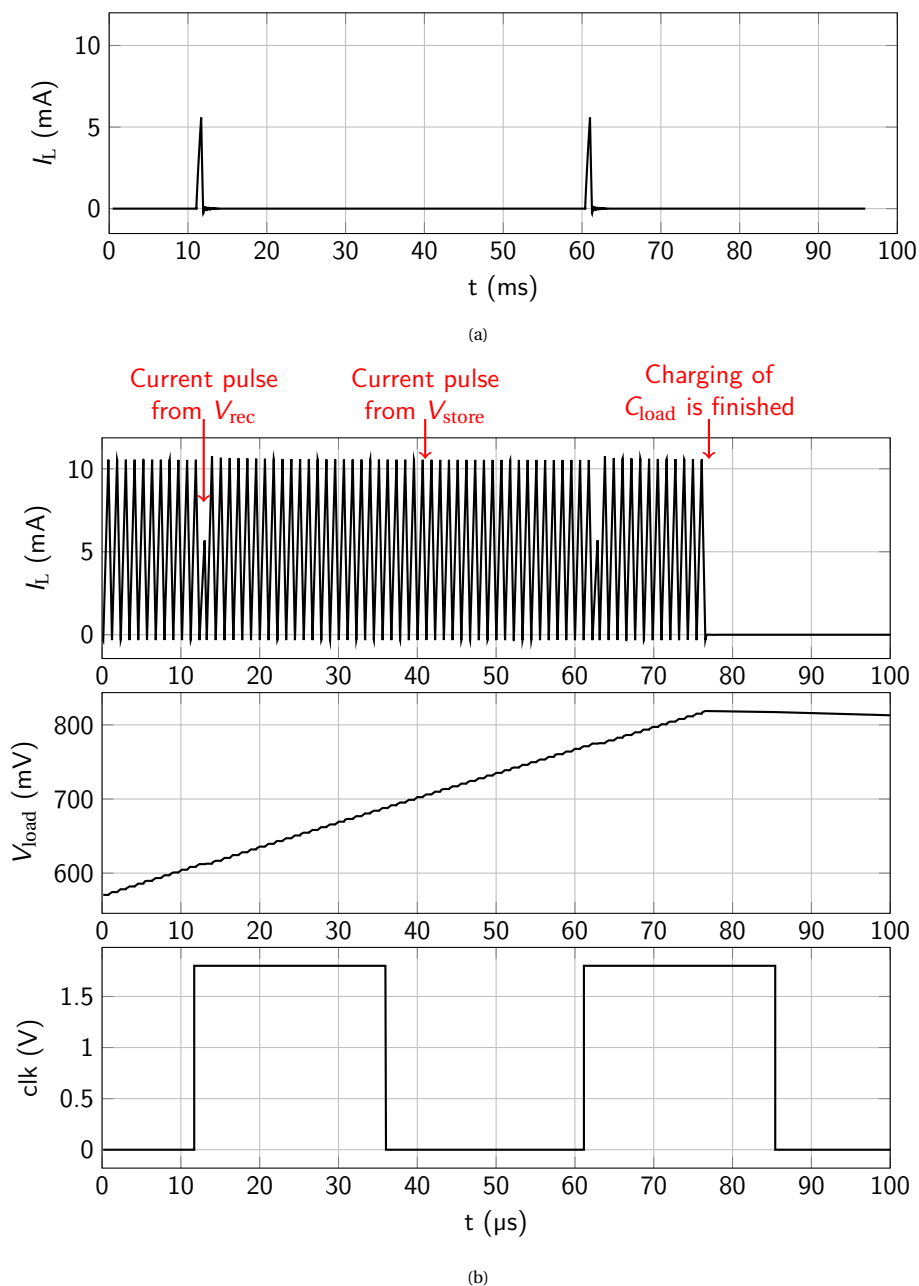


Figure 3.20: Inductor current transient simulation results: (a) V_{load} is not charged; (b) V_{load} is charged until it reaches the target value.

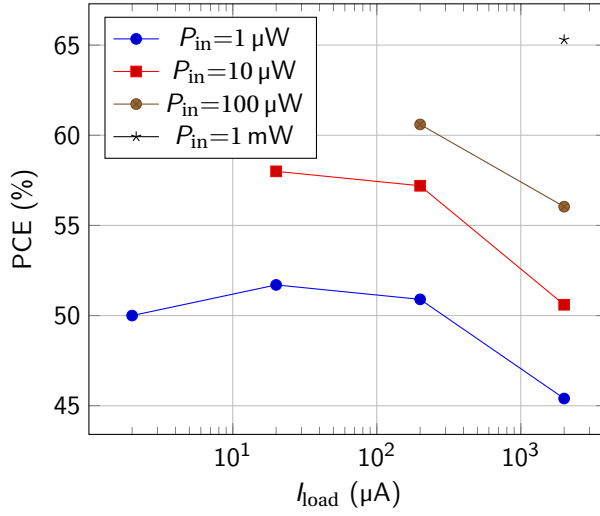


Figure 3.21: Total PCE of the SIDITO buck-boost converter. The PCE is calculated as the average load power divided by the average input power.

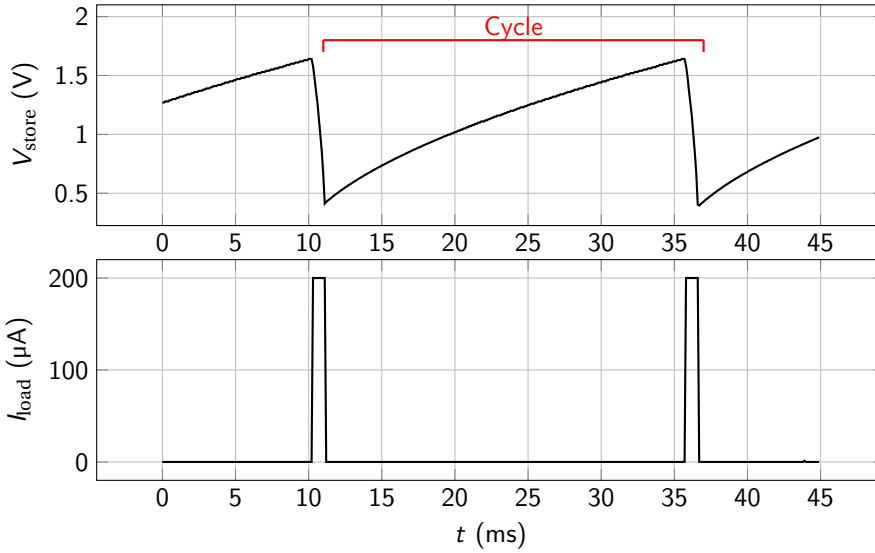


Figure 3.22: Transient simulation results showing the cycle period used for the PCE calculation. In this simulation, the case of $P_{in} = 10 \mu W$ and $I_{load} = 200 \mu A$ was considered.

extending the input power range, (d) a digitally-controlled low-power oscillator, and (e) an asynchronous load voltage regulator that uses the dead time to supply the load. Considering the complete RFEH system, the combination of those circuits helps to increase the available power range, the sensitivity, and the peak PCE.

4

MAXIMUM POWER POINT TRACKING

An energy harvesting system may be designed for a single available power level. Usually, this is a very low power level in order to present the highest possible sensitivity. However, when the available power changes, the entire power conversion chain is taken away from its optimum operating point and the power conversion efficiency decreases. To mitigate this problem, a maximum power point tracking (MPPT) circuit can be employed. The goal of the MPPT circuit is to adjust the power conversion chain parameters as the available power changes. This ensures the proper power matching between all the blocks in the chain, bringing the system to the highest power conversion efficiency point. In this work, the MPPT circuit controls the DC-DC converter and impedance matching network.

In the case of the DC-DC converter block, its parameters are changed to match the converter input resistance to the source output resistance, resulting in maximum power transfer. The converter parameters depend on its topology. In a switched-inductor converter, the parameters can be: switching frequency, switch size, duty-cycle, and inductor value. Furthermore, the converter can switch between continuous conduction mode (CCM) and discontinuous conduction mode (DCM); it may employ burst mode, in which an additional parameter would be the number of current pulses within a clock period; or it may employ critical conduction mode (KCM), in which the main control parameter is the input switch ON time. In a switched-capacitor converter, the parameters can be: switching frequency, boost factor (circuit topology), and flying capacitor values. By changing one or more of the aforementioned parameters, the input resistance and therefore the rate of harvesting is changed. Traditionally, only one parameter is controlled, because it reduces the MPPT circuit complexity and it is usually enough to cover the desired available power range. MPPT algorithms that control more parameters are often called multi-variable, 2-D, or 3-D MPPT [70–73]. The MPPT circuit implemented in this work simultaneously controls the buck-boost converter switching frequency and the impedance matching configuration. However, it is a single-dimension MPPT because

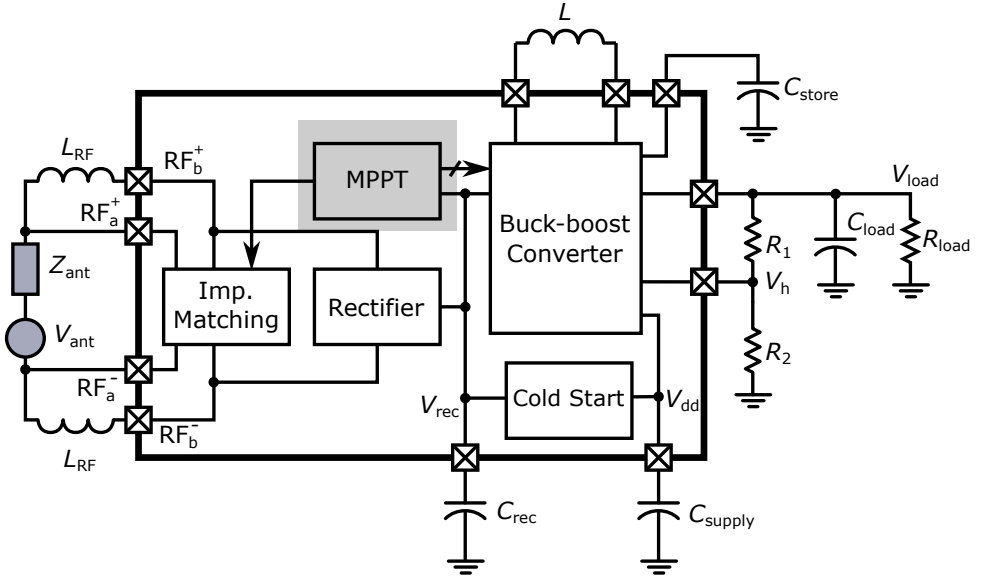


Figure 4.1: System block diagram: in the proposed system, the MPPT block controls both the DC-DC converter and the impedance matching network.

both parameters are controlled simultaneously by a single MPPT output, as presented later in this chapter. The MPPT circuit is the highlighted block in the system block diagram in Fig. 4.1.

There are several MPPT algorithms in the literature [74]. The algorithms that are commonly used in energy harvesting are: the fractional open-circuit voltage (FOCV) method [75, 76], the perturb and observe (P&O) method [77, 78], and the incremental conductance method [79–81].

The FOCV method consists in first turning the DC-DC converter off, to present a high impedance to the energy harvester, and sampling the harvester output voltage, which is called the open-circuit voltage (V_{OC}) in this condition. Then, a reference voltage that is equal to a fraction of V_{OC} is created: $V_{ref} = kV_{OC}$, in which k is the multiplication factor. In a next moment, the DC-DC converter is turned on and its parameters are tuned to make the harvester output voltage equal to V_{ref} . The FOCV method is a simple and low-power method of achieving maximum power point tracking. However, the predetermined value of k is fixed, reducing the available power range across which the MPPT works efficiently. Furthermore, not all energy harvesters present a maximum power point that is equal to a fixed fraction of V_{OC} over a range that is meaningful. There is a fractional short-circuit current method, which is similar to the FOCV method, but uses a fraction of the harvester current when connecting its output to ground [82]. However, it is seldomly applied in energy harvesting systems because it is more complex and power consuming to measure and sample current.

The P&O method is a hill climbing method that consists in first incrementing or decrementing a control parameter (perturbation) and then checking whether the har-

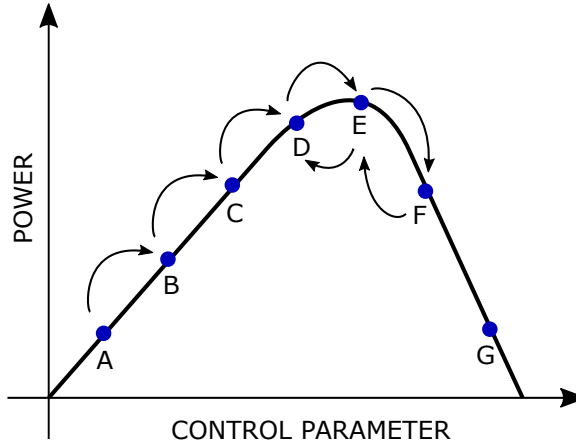


Figure 4.2: Illustration of the Perturb and Observe algorithm.

vested power increases or decreases (observation). If the measured power is larger than the previous measurement, the next perturbation is applied in the same direction. Otherwise, the perturbation direction is inverted. The P&O algorithm is illustrated in Fig. 4.2. The MPPT procedure starts with the converter at point A. A perturbation is applied, increasing the control parameter value and leading the converter to point B, which presents higher power. Therefore, the perturbation direction is kept. The process is repeated until point E is reached, which is the maximum power point. After the next perturbation, the converter is at point F and the power is lower, so the perturbation direction is inverted, returning the converter to point E. Again, the next perturbation leads to a point of lower power, point D, and the perturbation direction is inverted again. The procedure continues, while the system operates around the maximum power point. This method presents better accuracy and flexibility than the FOCV method, but it is more complex and requires more power. Another drawback is that it presents an oscillation around the maximum power point.

The incremental conductance method was created to solve the oscillation problem of the P&O method. It is a hill climbing algorithm that relies on the observation that the derivative of the harvester output power with respect to its voltage (dP/dV) at the maximum power point equals zero. This means that:

$$\frac{d(VI)}{dV} = 0 \Rightarrow \frac{dI}{dV} + \frac{I}{V} = 0. \quad (4.1)$$

At every step, the algorithm compares the instantaneous conductance (I/V) with the incremental conductance (dI/dV) and decides whether to increase or decrease the control parameter. Once the maximum power point is reached, the condition of (4.1) is met and no more perturbations are applied. If the available power changes, I and V changes and the algorithm will apply a perturbation again, the direction of which will depend on the instantaneous and incremental conductance values. This method presents a better performance for rapidly changing input power in comparison with the P&O method. It also presents better accuracy and flexibility than the FOCV method. On the other hand,

it presents a higher complexity and power consumption due to the additional computations in comparison to the P&O method. Furthermore, accurate measurement of both the input voltage and the input current are necessary to implement this algorithm.

In this work, the MPPT circuit was designed based on the P&O algorithm, due to its inherent low-power consumption [83]. Together with a low-power input power estimation circuit and a scheme to shutdown all analog blocks when not in use, the MPPT circuit exhibits low power consumption and allows for tracking over a large input power range. In this chapter, we first present the MPPT block diagram and details about its algorithm in Section 4.1. In Section 4.2, we discuss in detail all the blocks that comprise the MPPT circuit. In Section 4.3, we present simulation results of the MPPT circuit to validate its correct operation for different scenarios. The conclusion of this chapter is presented in Section 4.4.

4

4.1. MPPT BLOCK DIAGRAM AND ALGORITHM

The MPPT circuit block diagram is presented in Fig. 4.3. The DC-DC converter input power is estimated by the power estimation block. Its output signal is a current that is fed into a current-to-voltage converter. The output of the current-to-voltage converter is then sampled in the sample and hold (S&H) block. The comparator that follows the S&H block is used to compare voltages sampled at two different points in time for two different control parameter values. The up/down bit generator takes the comparator output and generates the control signal for the up/down counter. The counter output is the system's control parameter and it is mapped into the DC-DC converter switching frequency, FC , and the impedance matching network configuration control signal, V_{hp} . To control all the aforementioned blocks, a 12-bit counter and sequencer are used. The 12-bit counter is controlled by the system clock and sets the MPPT cycle, which starts when the counter value overflows and returns to zero.

In conventional MPPT algorithms, the power is measured at the beginning of each MPPT cycle, the control parameter is changed, and the measured value is held until the beginning of the next cycle for comparison with the next measurement. To lower the power consumption, the analog circuits are turned off as soon as the measurement is performed. To lower it even further, the cycle duration is made as long as necessary. However, it requires a sample and hold circuit that can hold for a very long time, which dissipates power. In this work, to avoid the long hold time, the rectifier output power is sampled one extra time, within a shorter period [84]. Then the comparison is performed and a decision is made by the up/down bit generator. Only the decision is held in the flip-flop over the rest of the MPPT cycle, which requires less power. Together with a low-power and simple power estimation circuit, we are able to design a wide-range and low-power MPPT circuit. Therefore, the implemented MPPT algorithm executes the following sequence of events:

1. Enable the power estimation circuit for first power measurement.
2. Wait for the power estimation circuit to settle. Hold its output value.
3. Change the control variable (Perturbation) and disable the power estimation circuit.

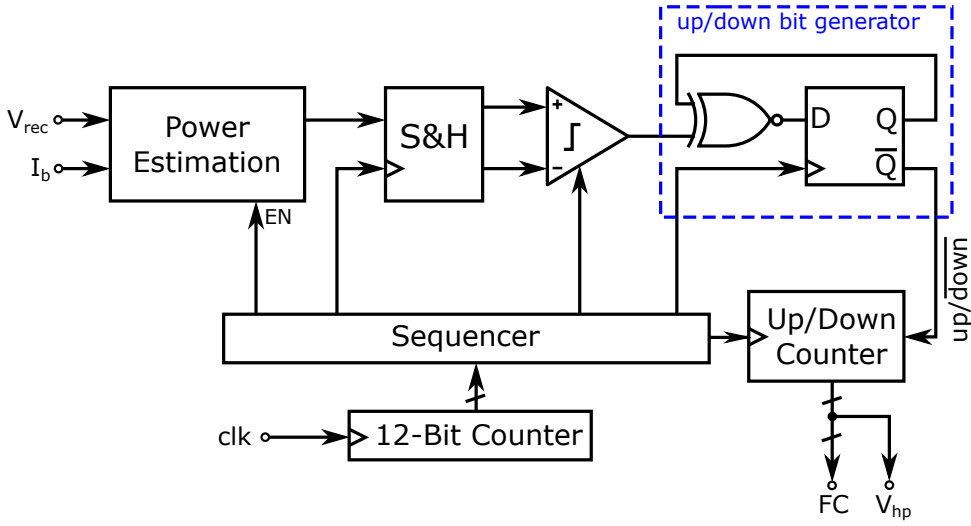


Figure 4.3: MPPT block diagram.

4. Wait for the system to settle.
5. Enable the power estimation circuit for a second power measurement.
6. Wait for the power estimation circuit to settle. Compare its output with the held value (Observation). Disable the power estimation circuit.
7. Make the decision whether to continue perturbation in the same direction or to invert the perturbation direction. Store the decision and wait for the beginning of the next cycle.

The timing diagram of this sequence of events is presented in Fig. 4.4.

The MPPT circuit speed is set by the clock frequency, which in turn is controlled by the MPPT circuit itself. The higher the available power, the higher will be the clock frequency. Therefore, the speed of the MPPT increases with the available power, but so does its power consumption. The harvested power increases linearly with the switching frequency, in the matched condition, so the increase in the MPPT circuit power consumption does not affect the power conversion efficiency.

There are two waiting periods that must be considered. The first one is the waiting period for the settling of the power estimation circuit. It can be verified through circuit simulation and enough clock periods are allotted for this waiting time. The second waiting period is the system settling time, which is set to 32 clock periods. This settling time depends on the settling time of the oscillator that generates the clock signal and on the settling time of voltage V_{rec} , which changes every time that the control parameter is changed. As shown in the power estimation circuit description, presented in the next section, those two variables alone are enough to estimate the converter's input power. The dominant period is the settling time of V_{rec} , which depends on three factors:

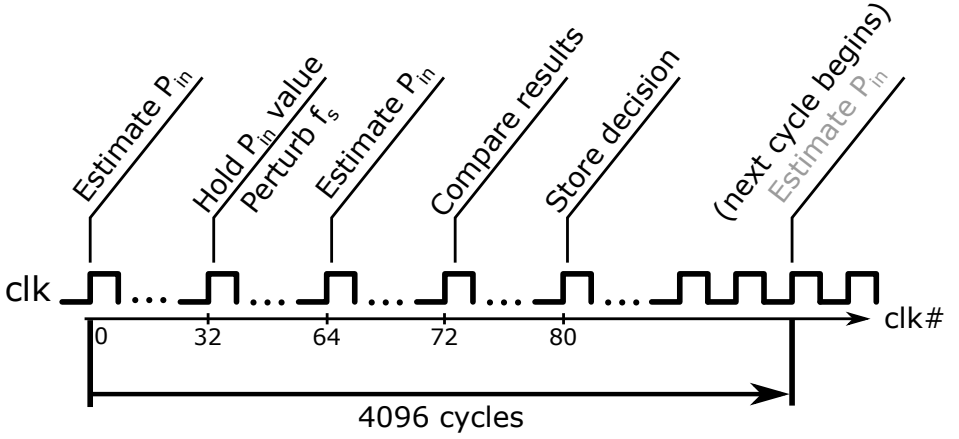


Figure 4.4: Timing diagram of the MPPT circuit.

capacitance C_{rec} (shown in Fig. 4.1), the equivalent input resistance of the buck-boost converter (R_{in}), and the equivalent output resistance of the rectifier. Capacitance C_{rec} has a constant value. For a fixed available power, the equivalent output resistance of the rectifier is fixed and it is equal to R_{in} in the matched condition. Its value is smaller for a larger available power, and the clock frequency will also increase as the MPPT algorithm is running. Therefore, with a faster the clock, there is less time for settling, but also less time is needed because the resistances are smaller. Through simulation, we guarantee that 32 clock cycles is enough (with some margin) for the designed system using a 10 nF C_{rec} . The same is true for the power estimation circuit: its waiting time reduces as the clock frequency increases, but its settling time reduces because its bias current is also increased.

4.2. MPPT SUB-CIRCUITS

In this section, we discuss in detail the blocks that comprise the MPPT. The blocks are shown in the block diagram of Fig. 4.3.

4.2.1. POWER ESTIMATOR

To track the maximum power point with the P&O method, it is necessary to measure the power that goes through the DC-DC converter. This power can be measured either at the input or at the output of the DC-DC converter. Measuring the power at the output is more accurate because it also considers the converter PCE in the tracking and the maximum output power will be achieved. However, if the DC-DC converter PCE is approximately constant over different operating conditions, we get the same results when measuring the input power.

There are several ways to measure or estimate the power flowing through a DC-DC converter. One of the methods is to add a resistor in series with the power switches

to convert its current to a voltage, and use the voltage value in the calculations [85, 86]. Alternatively, a coil can be coupled to the power inductor to copy and measure its current [87, 88]. The disadvantage of both methods is that they introduce conduction losses to the converter, reducing its PCE. To avoid this problem, the parasitic resistance of the power switches can be exploited and the current through the power switch can be copied [77]. However, if the parasitic resistance is too small, the accuracy of the measurement is compromised. Indirect methods of estimating the DC-DC converter power have been created to avoid having to measure its current. One of such methods is to charge an output capacitor for fixed time and compare the final voltages [71], or to measure the time it takes to charge an output capacitor to a fixed voltage. The disadvantage of this method is that it takes a long time to estimate the output power, if a large storage capacitor is used for this task. A solution would be to use a smaller output capacitor just for this task, disconnecting the converter from the storage capacitor. But in that case the converter output power would be wasted while the power estimation measurement is performed. In this work, we propose an indirect way of estimating the DC-DC converter input power by measuring only its input voltage and switching frequency. No additional lossy element is added to the power path and the converter can operate normally while the power estimation is performed. The proposed power estimator is applicable to the buck-boost converter operating in discontinuous conduction mode (DCM).

The power estimation is based on the equation of the input power of a buck-boost converter in DCM. If we consider that C_{rec} , its input capacitance, is large enough, we can approximate the converter input voltage V_{rec} as a DC voltage. Therefore, the converter input power can be written as:

$$P_{\text{in}} = \frac{V_{\text{rec}}^2}{R_{\text{in,avg}}}, \quad (4.2)$$

in which $R_{\text{in,avg}}$ is the average input resistance of the converter as seen from V_{rec} . Substituting (3.2) in (4.2), we can rewrite it as:

$$P_{\text{in}} = V_{\text{rec}}^2 \frac{D^2 T}{2L} = V_{\text{rec}}^2 f_s \frac{T_{\text{ON}}^2}{2L}. \quad (4.3)$$

The switching frequency f_s is proportional to the oscillator bias current I_b , which leads to:

$$P_{\text{in}} \propto V_{\text{rec}}^2 I_b. \quad (4.4)$$

Because the other factors in (4.3) are constant, maximizing $V_{\text{in}}^2 I_b$ leads to the maximization of the input power. The same result is obtained if we maximize the square root of this value, which can be readily obtained using a differential pair in strong inversion. Therefore, an operational transconductance amplifier can be used as a power estimator circuit in this scenario.

The power estimator circuit is presented in Fig. 4.5. The output current I_{out} is the difference between the drain currents of the differential pair. We can derive it by means of a small signal analysis of the differential pair. Considering that its transistors are in strong inversion, their g_m is given by:

$$g_m = \sqrt{2\beta I_D}, \quad (4.5)$$

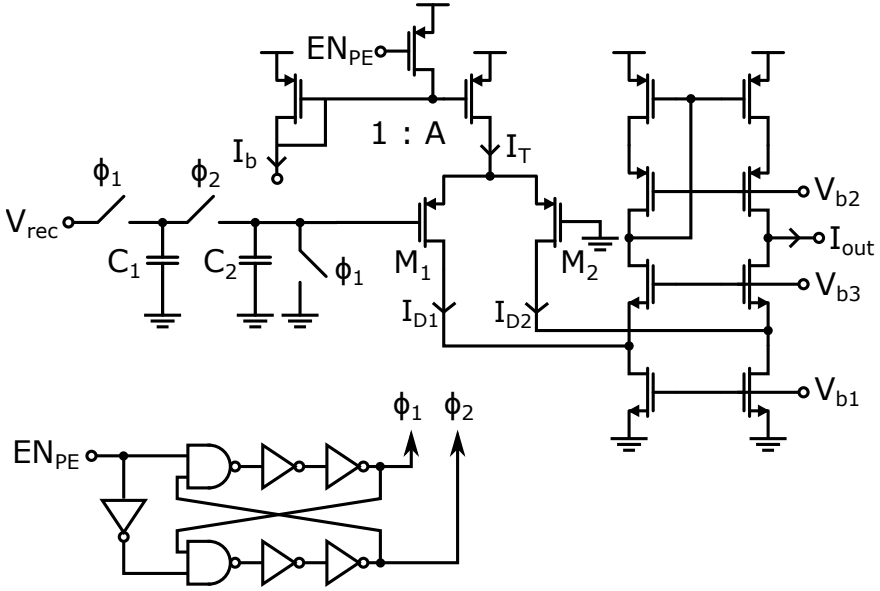


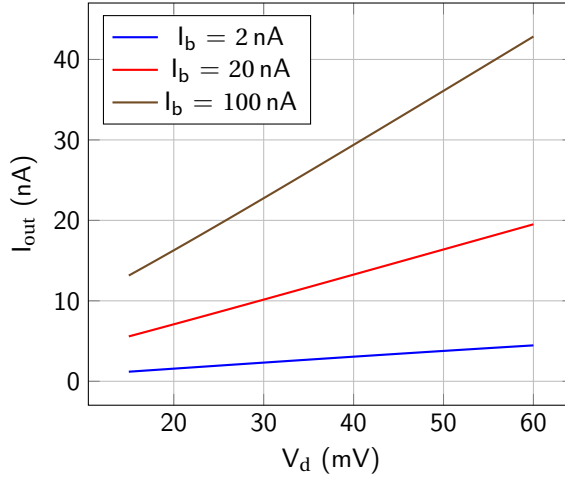
Figure 4.5: Rectifier output power estimator schematic.

in which $\beta = \mu_n C_{ox} \frac{W}{L}$. Therefore, I_{out} is given by:

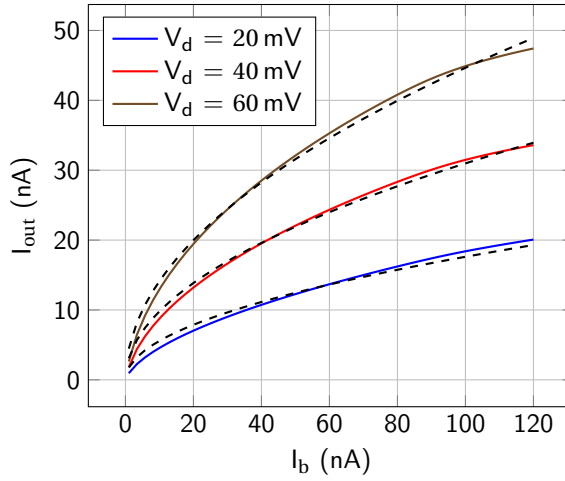
$$i_{out} = i_{D2} - i_{D1} = g_m \frac{V_d}{2} - g_m \frac{-V_d}{2} = \sqrt{\beta I_T} V_d = \sqrt{\beta A} \frac{C_1}{C_1 + C_2} \sqrt{I_b} V_{rec}, \quad (4.6)$$

in which V_d is the differential input, which is a fraction of the input voltage, and I_T is the tail current, which is made proportional to I_b . Therefore, the output current of this circuit is proportional to the square root of (4.4) and maximizing it will maximize the rectifier output power.

The folded-cascode topology shown in Fig. 4.5 was selected because it allows for a high voltage drop across the differential pair, allowing it to operate in saturation over a large bias current range. The switched capacitor circuit, placed between V_{rec} and the gate of M_1 , divides the input voltage, making the (absolute value of) V_{GS} of M_1 larger and helping that transistor to stay in strong inversion even at high input power levels (high input voltage). At the same time, it makes the differential input voltage small enough so (4.6) still holds. Multiplying the input voltage by a constant factor, which is the function of switched capacitor circuit, does not affect the MPPT result, since all power measurements are multiplied by the same factor. The power estimator DC simulation results are presented in Fig. 4.6. We can observe the linear variation of I_{out} with V_d , in Fig. 4.6(a), and its square root variation with I_b , in Fig. 4.6(b), in which the dashed lines are the best fitting square root curves. With those figures, we can observe that the power estimator circuit is performing the function defined by (4.4).



(a)



(b)

Figure 4.6: Simulation results of the power estimator circuit output current for (a) a sweep of the differential input voltage V_d and (b) the bias current I_b .

EFFECT OF MISMATCH

Device mismatch of both transistors and capacitors affect the power estimator circuit output. The accuracy of the output current I_{out} is affected by mismatch in the following parts: the switched-capacitor voltage divider, the current mirror that generates I_T , the differential pair, the current mirror formed by M_3 - M_4 , and the current sources formed by M_5 - M_6 . Each of these mismatch sources are analyzed below and their influence on the MPPT accuracy are considered.

If the matching of the voltage divider is affected by a ΔC , the differential input voltage becomes:

$$V_d = \frac{C_1}{C_1 + C_2} (1 + \Delta C) V_{\text{rec}}. \quad (4.7)$$

This variation in V_d multiplies I_{out} by a constant. Therefore, I_{out} is still proportional to $\sqrt{I_b} V_{\text{rec}}$ and the MPPT accuracy is not affected.

Something similar happens to the current mirror that provides I_T . Considering that it has a variation ΔA due to mismatch, we can rewrite I_T as:

$$I_T = (A + \Delta A) I_b. \quad (4.8)$$

Again, this multiplies I_{out} by a constant, which does not affect the MPPT accuracy.

The differential pair transistors are affected by a $\Delta\beta$ and a ΔV_t , which impacts the difference between the drain currents. Considering both variations, we can write the drain currents as:

$$I_{D1,2} = \frac{\beta \pm \Delta\beta}{2} (V_{\text{GS}} - V_t \pm \Delta V_t)^2 = \frac{\beta \pm \Delta\beta}{2} (V_{\text{GS}} - V_t)^2 \left(1 \pm \frac{\Delta V_t}{V_{\text{GS}} - V_t} \right)^2. \quad (4.9)$$

For $\Delta V_t \ll V_{\text{GS}} - V_t$:

$$I_{D1,2} = \frac{\beta \pm \Delta\beta}{2} (V_{\text{GS}} - V_t)^2 \left(1 \pm \frac{2\Delta V_t}{V_{\text{GS}} - V_t} \right). \quad (4.10)$$

For $V_d = 0$, the difference between drain currents is:

$$I_{D2} - I_{D1} = -2\Delta V_t \beta (V_{\text{GS}} - V_t) - \Delta\beta (V_{\text{GS}} - V_t)^2. \quad (4.11)$$

Because the tail current is the summation of both drain currents, we have:

$$I_T = \left(\beta + \frac{2\Delta\beta\Delta V_t}{V_{\text{GS}} - V_t} \right) (V_{\text{GS}} - V_t)^2. \quad (4.12)$$

If we consider $2\Delta\beta\Delta V_t / (V_{\text{GS}} - V_t) \ll \beta$, we can approximate $I_T \approx \beta (V_{\text{GS}} - V_t)^2$ and rewrite the difference between drain currents as:

$$I_{D2} - I_{D1} = -2\Delta V_t \sqrt{\beta I_T} - \frac{\Delta\beta}{\beta} I_T. \quad (4.13)$$

For a small V_d , the difference between the drain currents can be approximated through a small signal analysis. The g_m of both transistors are:

$$g_{m1,2} = (\beta \pm \Delta\beta) (V_{\text{GS}} - V_t \pm \Delta V_t). \quad (4.14)$$

Therefore, the small signal drain current difference can be written as:

$$i_{D2} - i_{D1} = (\sqrt{\beta I_T} + \Delta\beta\Delta V_t) V_d. \quad (4.15)$$

Finally, the total difference can be written as:

$$I_{D2} - I_{D1} = (\sqrt{\beta I_T} + \Delta\beta\Delta V_t) V_d - 2\Delta V_t \sqrt{\beta I_T} - \frac{\Delta\beta}{\beta} I_T, \quad (4.16)$$

which shows that the MPPT will be affected, since the drain current difference does not increase with $\sqrt{I_T} V_d$ as intended and will not reflect the input power value.

The mismatch of the current sources in the cascode stage, modeled as ΔI_0 , affects the output current in the following manner:

$$I_{out} = I_{D2} - I_{D1} + \Delta I_0. \quad (4.17)$$

Even though ΔI_0 is added to the drain current difference, it is constant with V_d and I_b . This does not affect the MPPT accuracy because the MPPT circuit calculates the difference between I_{out} at two different instants, which cancels out ΔI_0 :

$$\begin{aligned} I_{out}(t_1) - I_{out}(t_0) &= (I_{D2} - I_{D1})_{t_1} + \Delta I_0 - [(I_{D2} - I_{D1})_{t_0} + \Delta I_0] \\ &= (I_{D2} - I_{D1})_{t_1} - (I_{D2} - I_{D1})_{t_0}. \end{aligned} \quad (4.18)$$

Finally, considering the current mirror mismatch in the cascode stage as a variation ΔB , the output current becomes:

$$I_{out} = (I_0 - I_{D1})(1 + \Delta B) - (I_0 - I_{D2}) = I_{D2} - I_{D1} + \Delta B(I_0 - I_{D1}). \quad (4.19)$$

The additional term is not constant. It depends on both V_{rec} and I_b , which will affect the MPPT accuracy.

To ensure that I_{out} is proportional to $\sqrt{I_b} V_{rec}$ (plus a constant), the differential pair mismatch ($\Delta\beta$ and ΔV_t) and the current mirror mismatch (ΔB) must be minimized. This can be done, for example, by increasing the transistors area, using layout techniques for improving matching, and trimming. The same is not true for the voltage divider mismatch (ΔC), the tail-current current mirror mismatch (ΔA), and the current source mismatch (ΔI_0). However, these mismatches will influence the input voltage range for which the MPPT will perform correctly.

EFFECT OF PROCESS AND TEMPERATURE VARIATION

Process and temperature variations alone will not directly affect the MPPT accuracy. Referring to (4.6), the differential pair's β and bias current I_b will suffer from variation, but I_{out} will still be proportional to $\sqrt{f_s} V_{rec}$ (as long as the oscillator frequency remains linear with respect to I_b):

$$I_{out} = \sqrt{\beta' k' A} \frac{C_1}{C_1 + C_2} \sqrt{f_s} V_{rec}, \quad (4.20)$$

in which β' is the affected version of β , and k' is the affected proportionality factor of f_s with respect to bias current I_b .

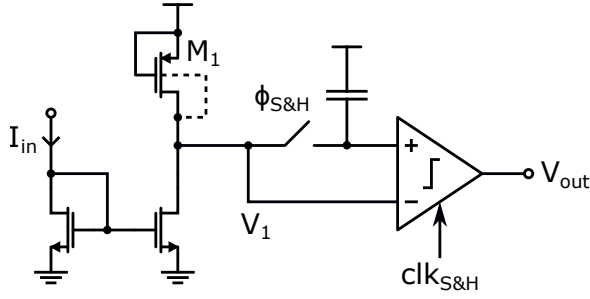


Figure 4.7: Circuit schematic of the S&H block.

4

Even though the MPPT accuracy is not directly affected by process and temperature variations, the input power for which the MPPT is functional might be affected. For example, if the bias current is too small, the differential pair might enter weak inversion. If the bias current is too large, the voltage drop across the differential pair is too high, damaging the functionality of the current mirrors. This can be avoided by designing a current reference generator that is not too affected by process and temperature variations. Similarly, if the V_t of the differential pair becomes too large, the transistors might come out of strong inversion at low bias current levels, which means that the MPPT would not be working correctly at low input power levels.

EFFECT OF RANDOM NOISE

Random noise in the power estimator is translated to noise in its output current, which is then converted to a voltage and sampled by the S/H block to be further compared to another power estimation at a different moment. If the voltages to be compared are close to each other, the noise might induce a wrong MPPT decision. The effect of noise in the MPPT accuracy can be mitigated by selecting a multiplication factor between frequency steps that is large enough, in such a way that the power estimator outputs at each step are far apart. As presented in Chapter 3, the frequency is multiplied (or divided) by 1.7 on every step. If this multiplication factor is too large, the MPPT accuracy will be reduced, since the possible values of input impedance of the DC/DC converter are reduced. If this multiplication factor is too small, the MPPT accuracy will be reduced due to the effects of noise and the offset of the sample-and-hold (S&H) comparator.

4.2.2. SAMPLE-AND-HOLD AND COMPARATOR

This block comprises a current-to-voltage converter, a sampling capacitor, and a latched comparator. Its circuit schematic is presented in Fig. 4.7. The output current of the power estimator block is the input of the S&H (I_{in}). This current is mirrored and then converted into a voltage (V_1) by transistor M_1 . Voltage V_1 is then sampled into a capacitor. After the MPPT circuit introduces a perturbation, the S&H circuit is presented with a new I_{in} and a new V_1 is generated. The new V_1 value is compared to the sampled value by a latched comparator [89], which is activated by $clk_{S\&H}$.

Voltage V_1 versus bias current I_b is plotted in Fig. 4.8 for different values of the differential input voltage of the power estimator circuit. As can be seen, the current-to-voltage

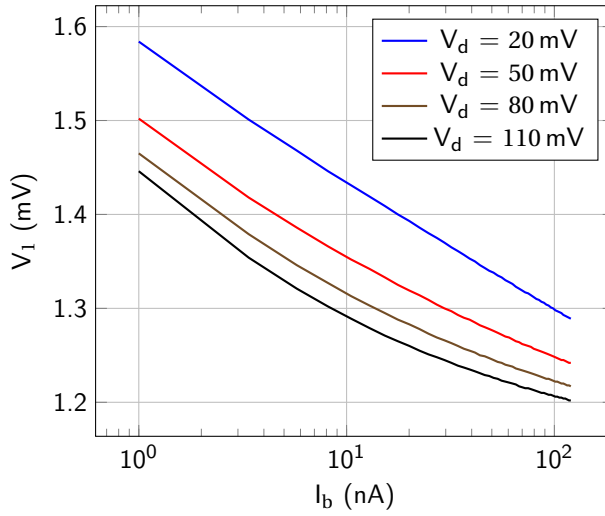


Figure 4.8: Output of the current-to-voltage converter versus bias current I_b for different values of differential input voltage of the power estimator circuit (V_d). Bias current I_b is used in the oscillator and in the power estimator circuit.

conversion is not linear. Since we just want to compare whether different values I_{in} are larger or smaller than each other, the conversion does not have to be linear, but just needs to be monotonic. The non-linearity makes it easier to compare smaller values of I_{in} , relaxing the design of the latched comparator. Also notice that the value is inverted, so a higher I_{in} generates a lower V_1 .

4.2.3. UP-DOWN BIT GENERATOR

The up-down bit generator provides the input for the up-down counter based on the S&H comparator output and its own previous output. The function of this circuit is to implement the hill climbing functionality. It keeps the up-down counter counting in the same direction in case the DC-DC converter input power is increasing with every perturbation or it reverts the up-down counter direction in case the input power is decreasing.

The S&H comparator output is '1' when the DC-DC converter previous input power (before the perturbation) is less than the current input power (after the perturbation). In this case, the output of this block (up/down) is kept. Otherwise, the S&H comparator output is '0' and up/down is inverted. This leads to the truth table and circuit presented in Fig. 4.9. The output is taken at the flip-flop's inverted output (\bar{Q}) because during system start-up all flip-flops are reset ($Q = 0$) and the up-down counter must start counting up. Therefore, up/down must be '1' after start-up.

4.2.4. UP-DOWN COUNTER

The up-down counter is a thermometer code counter that counts upwards or downwards, depending on its input bit up/down. The thermometer code is necessary to ensure the monotonicity of the oscillator frequency with the counter output (FC). Addi-

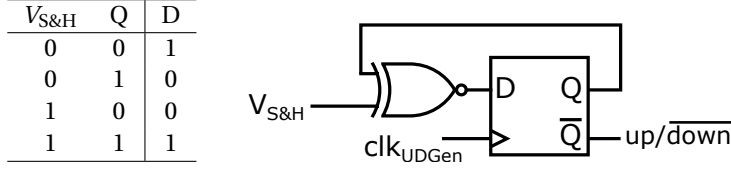


Figure 4.9: Truth table and circuit implementation of the up-down bit generator.

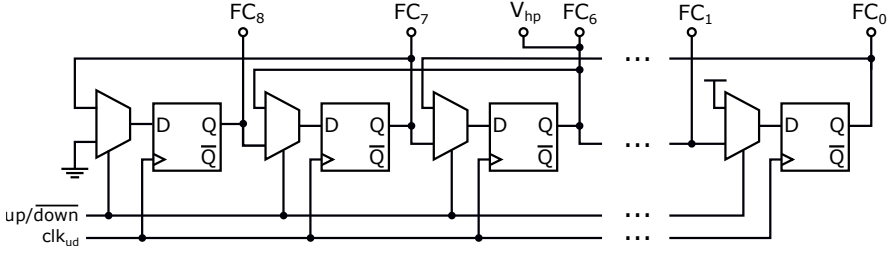


Figure 4.10: Up-down counter circuit schematic.

tionally, control signal V_{hp} , used to set the DC-DC converter's power switches and the impedance matching network into high-power or low-power mode, is derived from this block. Fig. 4.10 shows the up-down counter circuit schematic. The counter's clock signal (clk_{ud}) presents a rising edge once per MPPT cycle, when the perturbation is applied.

4.2.5. 12-BIT COUNTER AND SEQUENCER

A 12-bit counter sets the MPPT cycle duration and generates the input for the sequencer. The counter clock signal (clk) comes from the system's oscillator (presented in Chapter 3). Therefore, the higher the DC-DC converter input power, the faster is the MPPT cycle. The sequencer enables/disables all the other blocks in the MPPT circuit and generates the clock signal for them.

The 12-bit counter and sequencer circuit schematic is presented in Fig. 4.11(a). The sequencer outputs are: the power estimator enable bit, EN_{PE} ; the control bit for the S&H switch, $\phi_{S\&H}$, which turns the switch on when its value is high; the up-down counter clock signal, clk_{UD} ; the S&H comparator clock signal, $clk_{S\&H}$; and the up-down bit generator clock signal, clk_{UDGen} . The rising edge of all the clock signals generated by the sequencer trigger the blocks they are connected to. Fig. 4.11(b) presents the sequencer output bits versus the system clock cycle number, considering that when the cycle number is 0, outputs Q of all flip-flops in the 12-bit counter are low. When 4096 clock periods have passed, the MPPT cycle is finished and the procedure begins from the start. The sequencer output bits control all blocks in the MPPT circuit in order to execute the sequence presented in Section 4.1. We repeat the sequence below, relating the events to the transitions in the sequencer output bits:

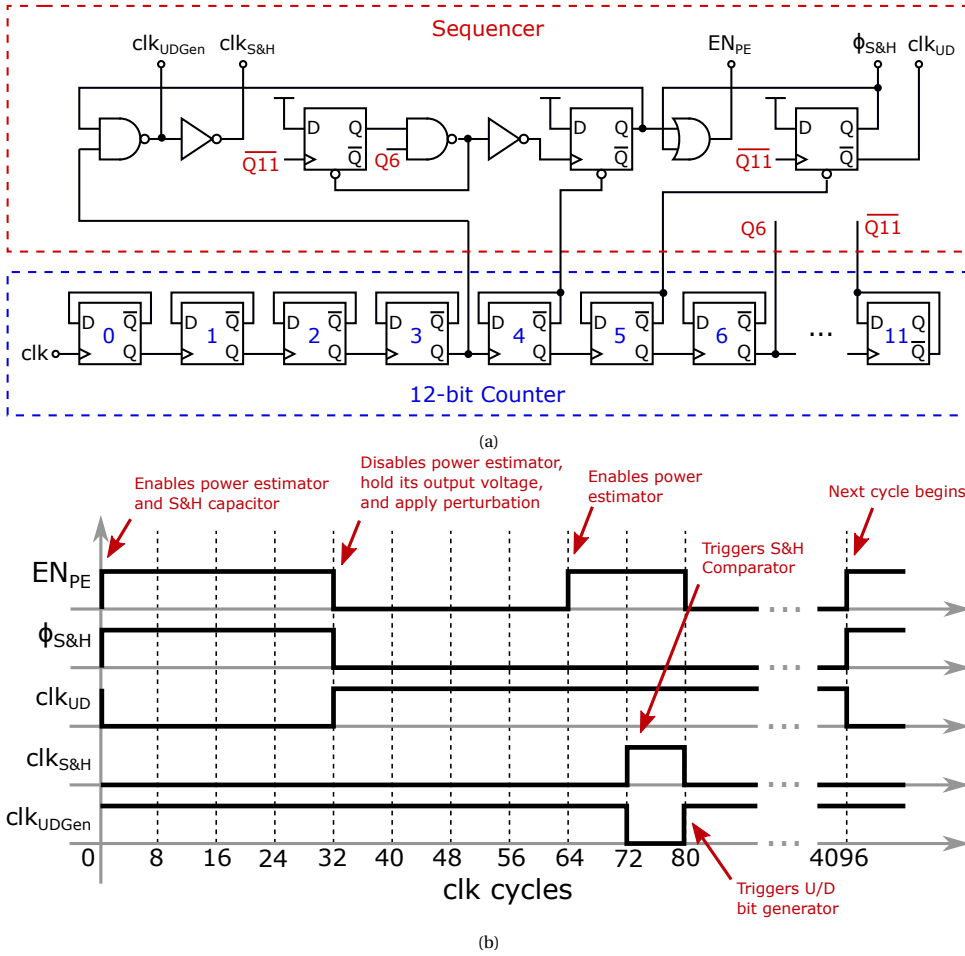


Figure 4.11: Sequencer and 12-bit counter (a) circuit schematic and (b) outputs versus clk cycle number. When the clk cycle is 0, output Q of all flip-flops in the 12-bit counter is 0.

1. When the clk cycle is 0, the power estimator is enabled and the S&H switch is turned on, and EN_{PE} and $\phi_{S\&H}$ are set to '1'. The power estimator needs some time to produce its output and charge the capacitor in the S&H. At the same time, clk_{UD} is set to '0' to prepare to present a rising edge at the end of this waiting time.
2. When the clk cycle reaches 32, the power estimator is disabled and the S&H switch is turned off to hold the power estimator output, and EN_{PE} and $\phi_{S\&H}$ are set to '0'. Signal clk_{UD} is set to '1' to trigger the up-down counter and perform the perturbation. The system needs some time to settle after the perturbation.
3. At the clk cycle 64, the power estimator is enabled again for the second measurement, EN_{PE} is set back to '1'. The power estimator needs some time to generate its output, but less time is needed in this second estimation since no S&H capacitor needs to be charged.
4. At the clk cycle 72, the S&H comparator is triggered by setting $clk_{S\&H}$ to '1'. At this moment the comparison between the two input power measurements is performed. Simultaneously, clk_{UDGen} is set to '0' to later present a rising edge.
5. At the clk cycle 80, the up-down bit generator is triggered to process the comparator output, clk_{UDGen} is set to '1'. Signal $clk_{S\&H}$ returns to '0' at the same time. At this moment, the MPPT process is turned off and the MPPT circuit is waiting for the next cycle to begin.
6. At clk cycle 4096, all bits in the 12-bit counter return to '0' and the MPPT cycle starts again.

The settling times of steps 1, 2, and 3 were obtained through circuit simulations. These settling times also scale with the system's clock frequency, because the power estimator is biased with a current that is proportional to the current that biases the oscillator, and the system settling time of step 2 is dominated by the DC-DC converter, which speeds up as its clock frequency increases.

4.3. SIMULATION RESULTS

To verify the correct operation of the MPPT circuit, we use a voltage source in series with a resistor as the input to the DC-DC converter [41]. It does not accurately model the rectifier across the entire power range, but it is good enough to allow us to speed-up the simulation and characterize the MPPT. The DC-DC converter input resistance is modelled as a variable resistance according to (3.2), in which switching period T is controlled by FC, the MPPT circuit output, according to:

$$T = \frac{1}{10\text{kHz} \cdot 1.7^{FC}}, \quad (4.21)$$

in which 10 kHz is the minimum frequency of the oscillator and 1.7 is the multiplication factor between each step of frequency. Fig. 4.12 presents the DC-DC converter input voltage (V_{rec}) and input power (P_{in}) while the MPPT circuit controls FC to find the

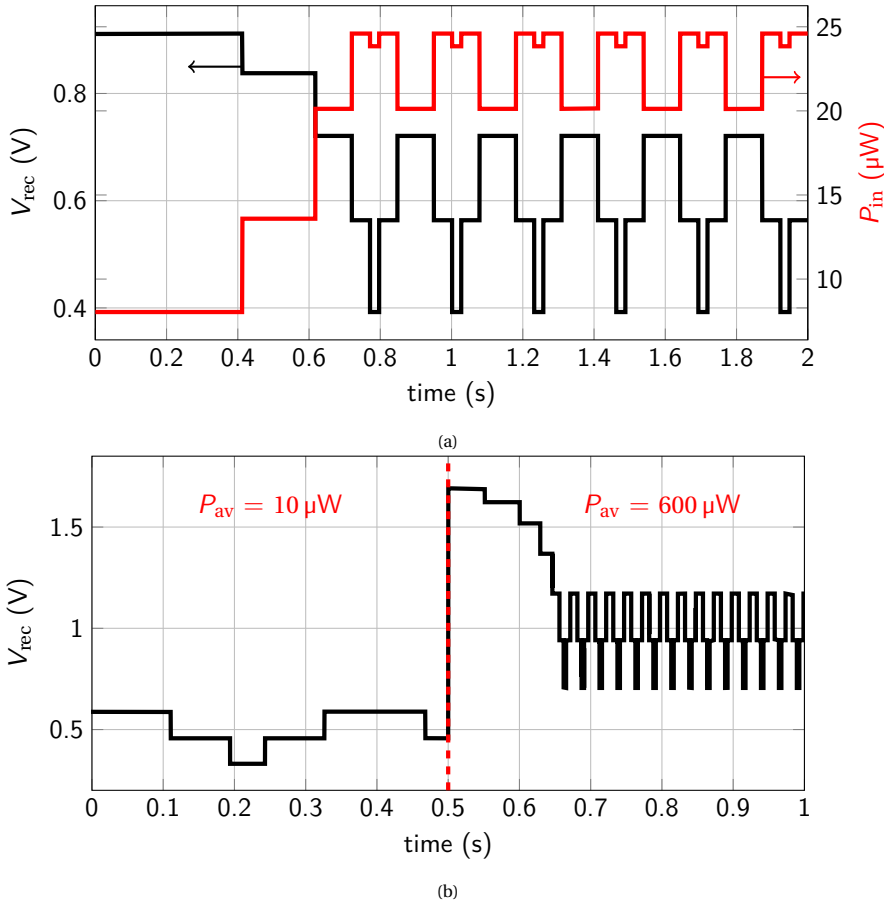


Figure 4.12: MPPT circuit simulation results: (a) $P_{av} = 25 \mu W$ and starting from $FC=0$; (b) P_{av} is switched from $10 \mu W$ to $600 \mu W$ at $t = 0.5s$.

maximum power point. In Fig. 4.12(a), the system is starting from $FC = 0$, the lowest frequency, and the available power is set to $25 \mu W$. The input power increases as the system gets closer to the maximum power point frequency and subsequently oscillates around it. In Fig. 4.12(b), the available power is initially set to $10 \mu W$ and later, at $t = 0.5s$, it is switched to $600 \mu W$. When the available power is switched, V_{rec} increases immediately because the DC-DC converter input resistance is too high. As soon as the MPPT circuit increases the switching frequency, V_{rec} drops closer to the maximum power point level.

The MPPT efficiency measures how well the MPPT circuit matches the DC-DC converter to its source. It is defined as:

$$\eta_{MPPT} = \frac{P_{in,DC}}{P_{av,DC}}, \quad (4.22)$$

in which $P_{av,DC}$ is the power available for the DC-DC converter, i.e., it is the maximum

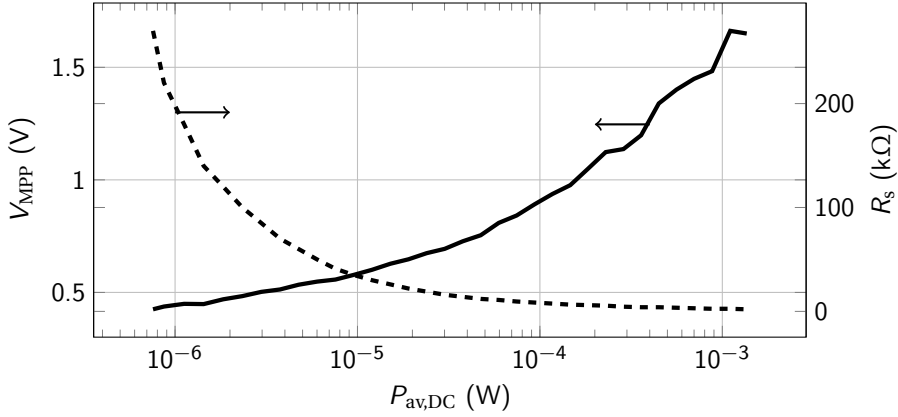
power it can harvest, and $P_{in,DC}$ is the DC-DC converter input power. To test the efficiency of the designed MPPT, we gather data from rectifier simulations and model the rectifier as a DC voltage source in series with a resistor. At the maximum power point, this combination provides an output voltage equal to V_{MPP} and an output power equal to $P_{av,DC}$. The V_{MPP} and resistor values as a function of $P_{av,DC}$ are plotted in Fig. 4.13(a). A transient simulation is used to determine η_{MPPT} for each $P_{av,DC}$. The value of $P_{in,DC}$ is then calculated as the average of the DC-DC converter input power over a long period, since the MPPT circuit makes the DC-DC converter to oscillate around the maximum power point. The duration of this period must be a multiple of 4 times the MPPT cycle, since this is the duration of the period in which the MPPT oscillates around the maximum power point. The efficiency results are plotted in Fig. 4.13(b). For P_{av} above $1.4 \mu W$, the MPPT efficiency is above 94%.

4

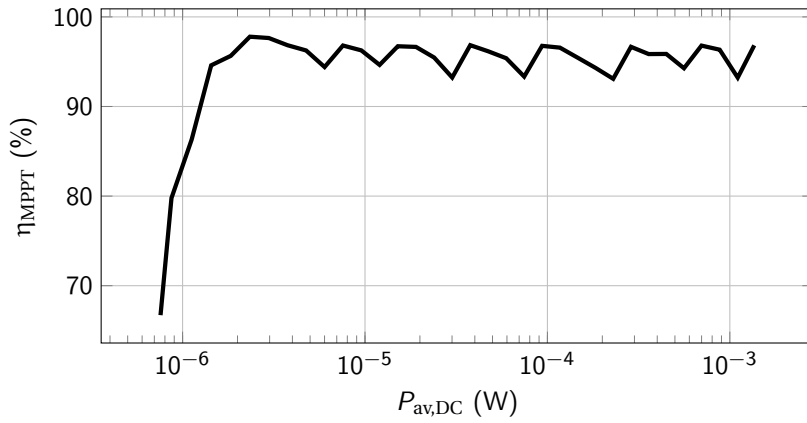
4.4. CONCLUSIONS

In this chapter, we presented the design and simulation of an MPPT circuit that estimates the input power of a buck-boost converter in DCM and tunes the switching frequency of the converter to maximize the estimated input power. The MPPT circuit building blocks and algorithm have been presented. Finally, simulation results illustrate the MPPT operation and its efficiency.

The proposed power estimation method proves to be an effective way to track the maximum power point without affecting the DC-DC converter operation or the need for adding sensing elements to the power path, which might degrade the PCE. The disadvantage of this method is that the DC-DC converter input power is maximized, and not its output power. However, if the DC-DC converter presents an approximately constant efficiency over the desired power range, maximizing the input power leads to the maximization of the output power.



(a)



(b)

Figure 4.13: Simulation results to verify the MPPT efficiency: (a) V_{MPP} and resistance of the source a function of $P_{av,DC}$. These values are extracted from the rectifier simulation results and used in the MPPT simulations. (b) MPPT efficiency as a function of $P_{av,DC}$.

5

MEASUREMENT RESULTS

In the previous chapters, we have presented circuit topologies and techniques for RF-DC converters, DC-DC converters, and maximum power point tracking (MPPT) circuits. We have also presented their implementation in the context of RF energy harvesting. With these techniques, we are able to design an RF energy harvester and power management IC that operates across a wide range of available input power (P_{av}). As we present in this chapter, the designed system comprises all the techniques presented in the previous chapters and is able to operate with P_{av} ranging from -24 to $+15$ dBm. Its power conversion efficiency (PCE) is above 5% across a 34 dB range. In this chapter, we present separately the measurement results of the RF-DC converter, of the DC-DC converter, and later of the complete system.

The micrograph of the designed chip is presented in Fig. 5.1. The chip was fabricated in a standard $0.18\text{ }\mu\text{m}$ CMOS IC process. The full chip area is 1.05 mm^2 (0.95 by 1.1 mm), but it is mostly dominated by the pad ring that contains several pads used for testing purposes. The chip area can be reduced in a future design, since its active area is just 0.2 mm^2 .

The measurement setup is presented in Fig. 5.2. This setup is used throughout the measurements and the connections represented by switches 1 to 4 are connected or disconnected depending on the measurement to be performed. In the RF-DC converter measurements, switches 1 and 2 are turned on while switches 3 and 4 are turned off. In the DC-DC converter measurements, only switch 3 is turned on while the rest of the switches are turned off. The RF power source is disabled in the DC-DC converter measurements, since the rectifier output is not needed. And in the full system measurements, only switch 4 is turned on. In this chapter, the RF-DC power conversion efficiency is called $\text{PCE}_{\text{RF-DC}}$, the DC-DC power conversion efficiency is called $\text{PCE}_{\text{DC-DC}}$, and the harvester conversion efficiency is called PCE. The latter is defined as the power delivered to C_{store} divided by P_{av} .

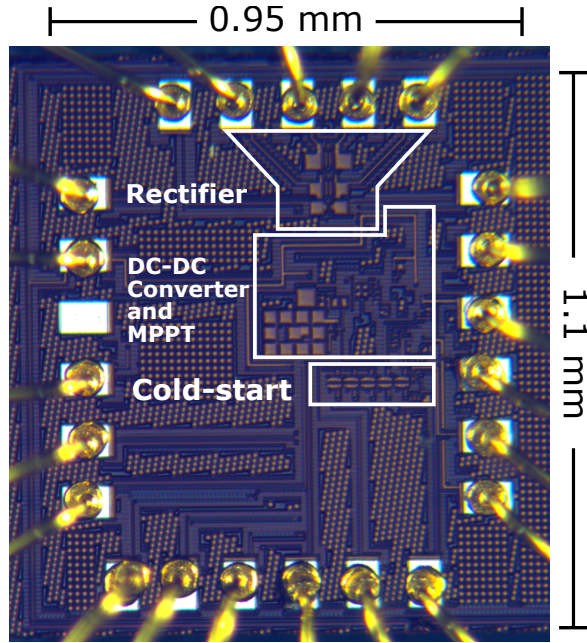


Figure 5.1: Micrograph of the RF energy harvesting and power management chip.

5.1. RF-DC CONVERTER MEASUREMENT RESULTS

For the RF-DC converter measurements, an RF source (the leftmost block of Fig. 5.2) is connected to a balun to generate a differential RF signal. An impedance matching PCB is then used to emulate the antenna impedance, which is set to $40 + j100 \Omega$. This antenna impedance is selected based on the simulation results of the RF-DC converter considering the parasitics of the PCB and off-chip components. The PCB that emulates the antenna impedance has two traces for each phase of the input signal, each one containing one 20 nH inductor (Johanson L-15W20) and two tunable capacitors, 1.5–3 pF (Murata TZY2Z030AC01) and 5.5–30 pF (Knowles Voltronics JZ300), in a T-match configuration. Each of the traces are tuned separately, using a Vector Network Analyzer (VNA) to verify the output impedance. We used the Agilent 8510B VNA. After tuning the impedance matching PCB, its outputs are connected to an oscilloscope to verify if the phase delay between the two outputs and their amplitude is as expected. The rectifier PCE is compromised if the phase delay is much different from 180° or if the difference between the signal amplitudes is too high. The measured signals are presented in Fig. 5.3, which shows that the phase delay close to 180° and that there is little difference between the signal amplitudes.

In order to calculate the $P_{\text{CE}_{\text{RF-DC}}}$, we must de-embed the impedance matching PCB and the balun losses. We are able to measure the S-parameters results for the impedance matching PCB and the balun with a VNA and calculate their insertion losses. The impedance matching PCB presents a 2.66 dB insertion loss and the balun presents a 1.31 dB insertion loss. The available power, P_{av} , is then calculated by subtracting both losses from the

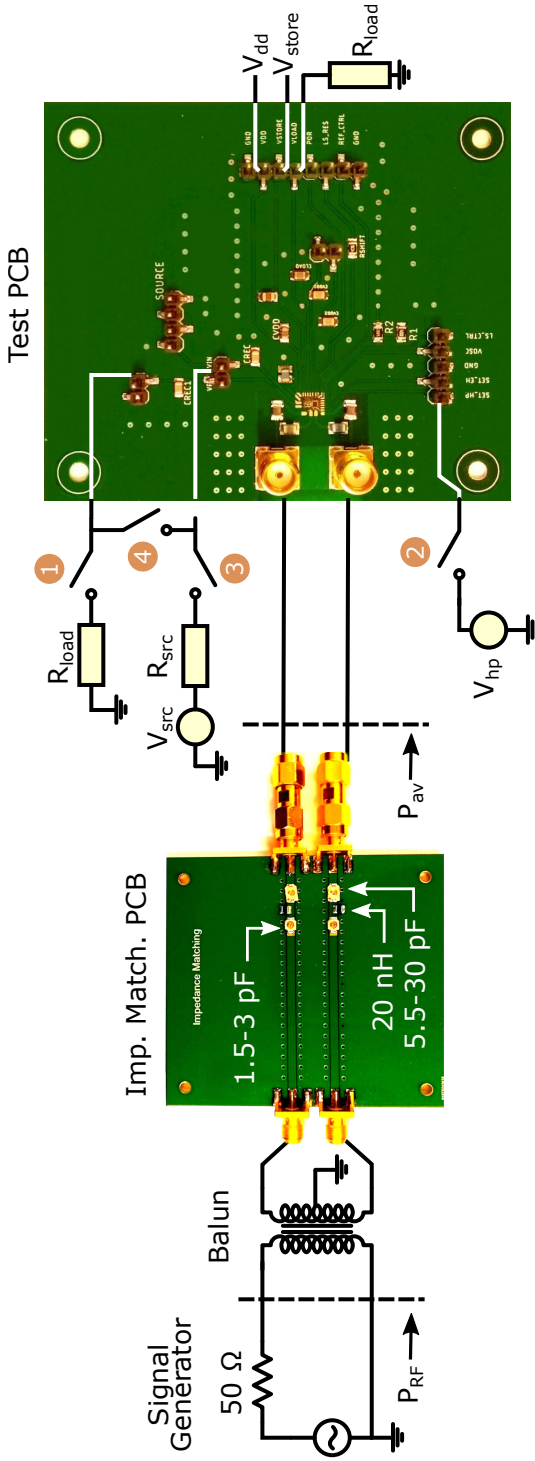


Figure 5.2: Diagram of the measurement setup. The RF-DC measurement is done by placing the load at the rectifier output (switch 1) and externally controlling signal V_{hp} (switch 2). The DC-DC converter measurement is done by connecting a power source to the DC-DC converter input (switch 3). The full system measurement is done by connecting the rectifier output to the DC-DC converter input (switch 4).

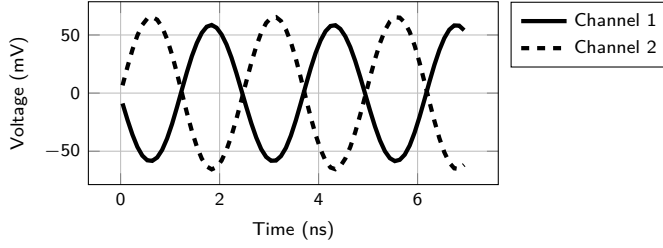


Figure 5.3: Impedance matching PCB output signals measured with an oscilloscope.

signal generator power, P_{RF} (see Fig. 5.2). In this way, we do not consider the losses of the balun and impedance matching PCB in the measurement results, but we consider the impedance mismatch between the test PCB and the emulated antenna.

After tuning the impedance matching PCB, its outputs are connected to the test PCB. A resistive load, R_{load} , is connected to the rectifier output and a voltage source, V_{hp} , is used to set the chip's impedance matching network to either high-power or low-power mode. A voltage source is connected to the chip supply voltage V_{dd} to bias the pad ring. This source does not provide any power to the rectifier, but it avoids the ESD protection circuit to turn on as soon as there is enough voltage at the rectifier output or input pins. The leakage from V_{dd} to the rectifier output through the ESD protection when V_{dd} is applied is less than 10 pW according to measurements with a semiconductor parameter analyzer. Therefore, the effect of the leakage on the measured PCE_{RF-DC} is negligible. The low leakage is due to the reduced size of the diodes employed in the ESD protection circuit. The reduced ESD diodes were used in all pads of the chip. Besides the low leakage current, they present low parasitic capacitance, which is beneficial for the RF input pads. However, the penalty is a reduced ESD protection for the chip.

Fig. 5.4(a) shows a magnified view of the impedance matching network on the test PCB and Fig. 5.4(b) shows the circuit schematic of this section. Two inductors, L_S , were added, when compared to the original matching network presented in Chapter 2, to compensate for variation of the on-chip capacitors due to process variation and to compensate for parasitics of the PCB and discrete components. The values of L_S and L_{RF} are selected based on simulation results considering the PCB parasitics and on measurement results. The value of inductor L_S is 6 nH (Coilcraft 0805HQ-6N2) and the value of inductor L_1 is 100 nH (Coilcraft 0805HP-101). The selected inductors have a 0805 footprint and a quality factor of approximately 80 at 403.5 MHz.

To measure the PCE_{RF-DC} , the signal generator frequency is set to 403.5 MHz and P_{RF} is swept from -21 to +19 dBm. By switching V_{hp} from 0 to 1.8 V, the impedance matching network is switched from the low-power (LP) to the high-power (HP) mode. Using a resistive load (R_{load}) at the rectifier output, the available power is swept and the output power is measured to plot the RF-DC PCE. Therefore, two curves are generated for a single R_{load} , one for each power mode. Fig. 5.5 presents such curves for two values of R_{load} : 25 k Ω and 800 Ω . The PCE for the low value of $R_{load} = 800 \Omega$ is higher at high power levels, making the HP mode more efficient. The opposite happens for the higher value of R_{load} . By sweeping R_{load} and repeating this process for each of its values, the

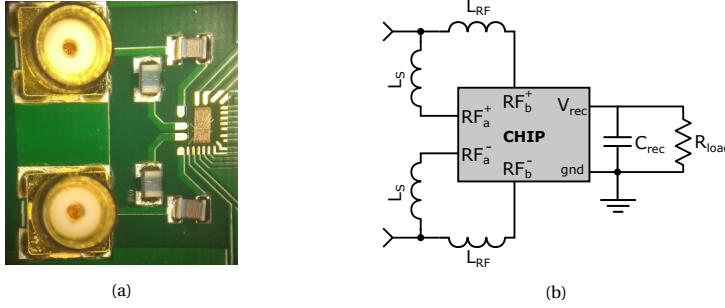


Figure 5.4: Zoom at the inductors used in the impedance matching network on the test PCB (a) and its circuit schematic (b).

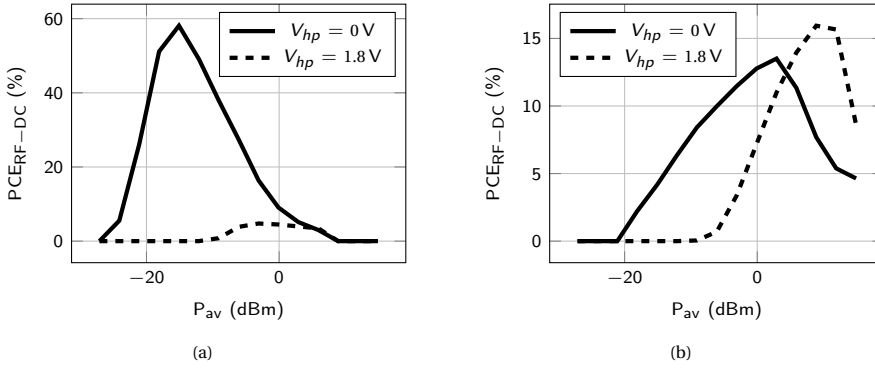


Figure 5.5: RF-DC power conversion efficiency with (a) $R_{load} = 25 \text{ k}\Omega$, (b) $R_{load} = 800 \Omega$.

highest PCE_{RF-DC} versus P_{av} curve is obtained, which is presented in Fig. 5.6. This curve represents the maximum PCE_{RF-DC} and can be seen as the highest total PCE curve that would be obtained with an ideal DC-DC converter and ideal MPPT. The MPPT circuit must switch V_{hp} around the point where the maximum PCE for the HP mode is equal to the maximum PCE for the LP mode. This point is around +5 dBm, as can be seen in Fig. 5.6. But it changes with process variations and the system can be calibrated by selecting which bit of the FC signal V_{hp} is connected to.

In Fig. 5.7 we analyse the bandwidth of the RF-DC converter. The figure presents the PCE_{RF-DC} variation as a function of the input signal frequency for two cases of P_{av} : -21 dBm (low-power mode) and +10 dBm (high-power mode). The converter was designed to receive power in a narrow band around 403.5 MHz. Its PCE is above half its peak PCE in a 16 MHz band around the center frequency. Keep in mind that the variation of the input signal frequency also changes the emulated antenna impedance.

5.2. DC-DC CONVERTER AND MPPT MEASUREMENT RESULTS

To measure the DC-DC converter we enable the connection represented by switch 3 in Fig. 5.2 and disable the remaining connections. The power inductor employed in the DC-

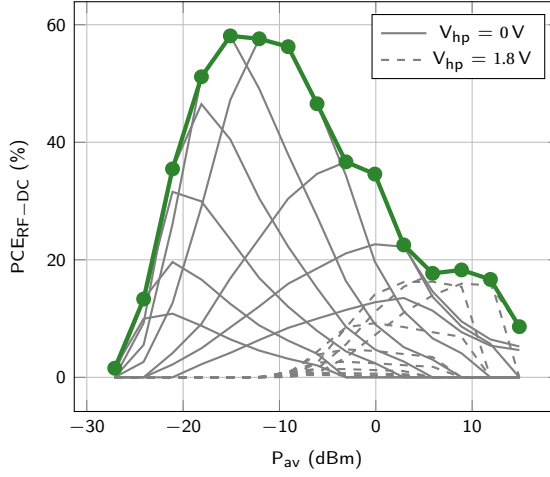


Figure 5.6: The highest RF-DC PCE is shown by sweeping R_{load} from 400 k Ω down to 800 Ω and switching V_{hp} between 0 (LP mode) and 1.8 V (HP mode).

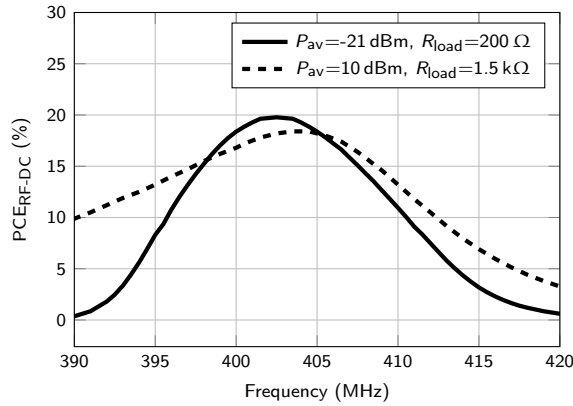


Figure 5.7: Variation of the RF-DC PCE with frequency for $P_{av} = -21$ dBm and $P_{av} = 10$ dBm.

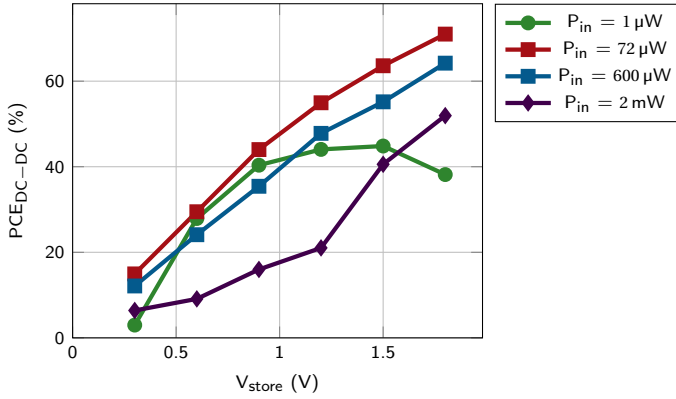


Figure 5.8: DC-DC converter efficiency for multiple values of input power.

DC converter has an inductance of $100 \mu H$ and an equivalent series DC resistance (DCR) of 3.1Ω (TDK MLF2012C101KT). The capacitors used in the test PCB are C_{rec} (10 nF), C_{supply} (22 nF), C_{store} (22 μF), and C_{load} (4.7 μF). Since this inductance is large, an inductor that presents a small DCR will have a large footprint and will not be suitable for most applications. We selected an inductor that has a larger-than-average DCR (3.1Ω), but has a smaller volume than most commercially available inductors (about 3.6 mm^3). Other supply capacitors (10 nF), connected to the MPPT and buck-boost converter supply pins, are placed on the PCB for allowing the powering of the MPPT and buck-boost converter separately, used only for debugging purposes. Resistors R_1 and R_2 (in the order of $M\Omega$) are also present on the PCB and are used for setting the target V_{load} .

Fig. 5.8 presents the PCE measurement results of the DC-DC converter, in conjunction with the MPPT, for a varying output voltage and input power. The measured peak efficiency is about 71% at $72 \mu W$ input power.

The load voltage regulation capability is presented in Fig. 5.9, which shows the transients of the storage capacitor voltage, V_{store} , and the load voltage, V_{load} , for different values of R_{load} . The target V_{load} is set to 0.6 V by selecting R_1 and R_2 equal to 1 $M\Omega$. Once V_{store} reaches 1.8 V, the system stops charging C_{store} and starts charging C_{load} . The system starts recharging C_{store} when V_{store} reaches 0.4 V. In practice, these voltage values change slightly due to offsets in the voltage reference and voltage monitors. The results of Fig. 5.9(a) are obtained by using a high value (200 $k\Omega$) of R_{load} . Once V_{store} reaches the predefined 1.8 V value, the system starts charging the load and the voltage V_{store} drops due to leakage. In this scenario, the system is on the edge of having enough power to operate. It cannot charge C_{store} at the same time as it charges the load, but it charges the load with energy coming from V_{rec} and does not require additional energy from C_{store} . This changes in the scenario of Fig. 5.9(b), in which we employ a medium R_{load} value (20 $k\Omega$). As soon as V_{store} reaches 1.8 V, the system uses the energy from both V_{rec} and C_{store} to charge the load. In this condition, we can see a faster drop in V_{store} as soon as the system starts to supply V_{load} . Reducing R_{load} even further (down to 3 $k\Omega$) leads to the scenario presented in Fig. 5.9(c). Most of the energy delivered to the load comes from

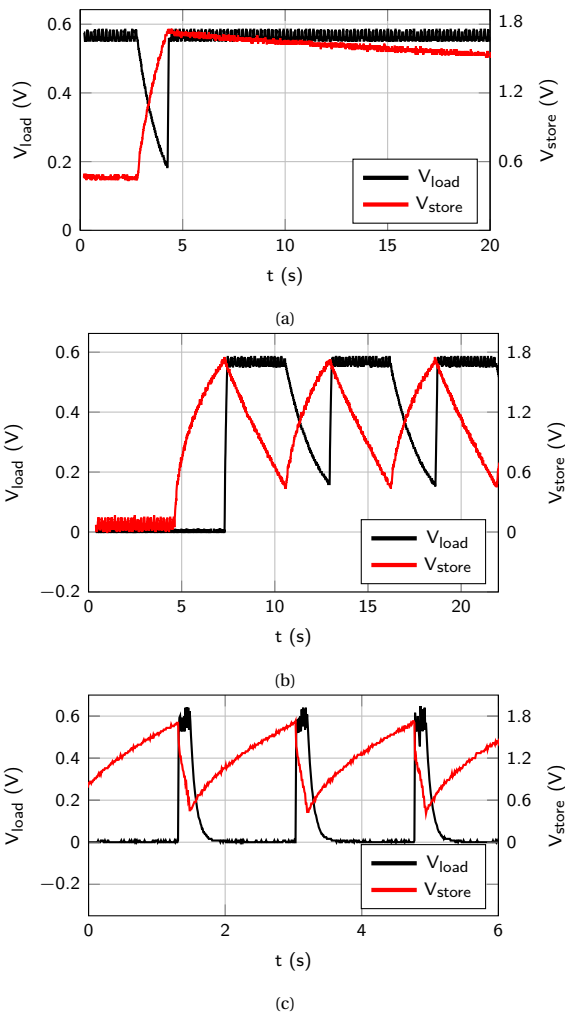


Figure 5.9: Load voltage regulation for (a) high R_{load} (200 k Ω), (b) medium R_{load} (20 k Ω), and (c) low R_{load} (3 k Ω).

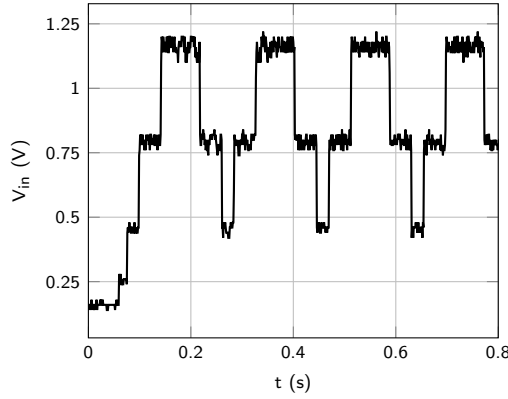


Figure 5.10: DC-DC converter input voltage during MPPT operation.

C_{store} and the voltage across it drops rapidly in order to sustain the load voltage.

Fig. 5.10 shows the DC-DC converter input voltage and illustrates the MPPT functionality. In this scenario, the input power is maximized when the input voltage is approximately 0.8 V. It can be observed that the input voltage moves back and forth around this value. As discussed in Chapter 4, this behaviour shows that the MPPT is checking the power at the switching frequencies that are adjacent to the maximum power point one, which is characteristic of the Perturb and Observe algorithm. The MPPT efficiency, defined as $P_{\text{in,DC}}/P_{\text{av,DC}}$ (see Chapter 4), is 85% in this scenario. The MPPT efficiency is lower than simulated because the changes in the oscillator frequency between some steps in the MPPT process are not as expected, most likely due to mismatch in the current mirrors that multiply the current and bias the oscillator.

5.3. FULL SYSTEM MEASUREMENT RESULTS

As shown in Section 5.1, the maximum RF-DC PCE is 58% at -15 dBm. However, both the DC-DC converter and the MPPT circuit introduce power losses. Combining the RF-DC converter with the DC-DC converter and MPPT circuit produces the PCE results presented in Fig. 5.11. The output power provided to charge the storage capacitor, $P_{\text{out,store}}$, is considered for the PCE calculation:

$$\text{PCE} = \frac{P_{\text{out,store}}}{P_{\text{av}}}. \quad (5.1)$$

The power losses for supplying the load are not taken into consideration in this figure, since they vary with the load current and the target load voltage. The peak PCE is 40.2% at $P_{\text{av}} = -9.1$ dBm.

The output power range extension provided by the adaptive circuits in the impedance matching and in the DC-DC converter is presented in Fig. 5.12. For P_{av} above $+6$ dBm, the system is switched from the LP to the HP mode and the output power reaches 1.33 mW at $+14.9$ dBm (30.9 mW) input. This represents an extension in the available power range of approximately 9 dB.

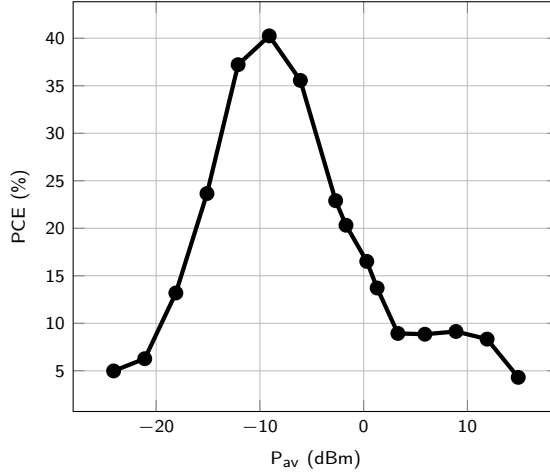


Figure 5.11: RFEH power conversion efficiency at 1.8 V output voltage.

5.4. COMPARISON WITH THE STATE OF THE ART

Table 5.1 presents the comparison of this work with the state of the art. In this section, we present the advantages and disadvantages of the papers in Table 5.1 and compare them with the system presented in this thesis.

The work in [90] presents a Cross-Coupled Differential-Drive (CCDD) rectifier architecture that employs body biasing to reduce the V_{th} and the leakage in order to increase the input power range. It obtains a high peak PCE, but not employing a DC-DC converter or additional rectifier stages leads to a reduction in sensitivity. Furthermore, an impedance matching network is not considered and its losses and the mismatch between the rectifier impedance and its source, which appears across a wide input power range, are not taken into account.

An RFEH with a reconfigurable rectifier is reported in [91]. The input impedance of the rectifier is kept constant when switching the number of stages by reusing stage capacitors and by combining transistors. But the effect of P_{av} on the input impedance is not considered, which limits the effective power range. Another disadvantage is that an external supply is necessary for operating the system.

In the system presented in [45], a boost converter and a single-stage rectifier are employed. This combination allows for a high output voltage generation at low input power levels. However, the fixed rectifier and impedance matching network cannot accommodate for a large input power variation.

A reconfigurable multi-stage rectifier is presented in [92]. A controllable on-chip network is employed, but it is not automatically controlled by the MPPT. Furthermore, a $50\ \Omega$ source is used, which leads to additional losses in the matching network when compared to a source impedance that has a positive imaginary (inductive) part. The latter case is more efficient because the source impedance is closer to the complex conjugate of the rectifier input impedance. Several rectifier stages are used in the system, which might lead to additional power losses. The system can control the load voltage and store

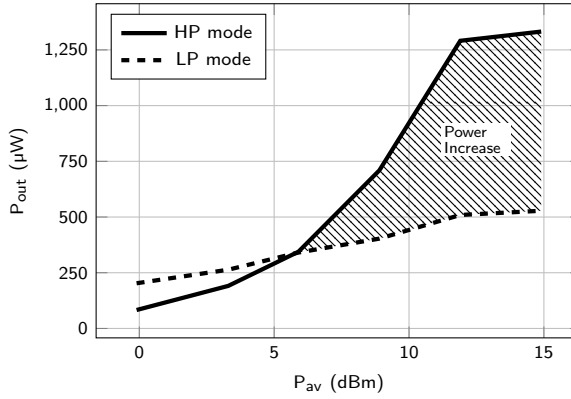


Figure 5.12: Output power range extension.

excessive energy, but it does not address how to use the energy stored to charge the load.

In [37], a 5-stage CCDD rectifier with a configurable impedance matching network is presented. The use of an inductive antenna improves the sensitivity. The impedance matching is controlled by an external micro-controller, but it was not designed to support the large variations of input impedance due to the input power variations. In addition, the multiple-stage rectifier generates a high output voltage when the input power increases, presenting a hazard to the chip and limiting the maximum input power.

By using a single stage rectifier, a non-50 Ω source, and adaptive circuits in the power conversion chain, we have shown that it is possible to obtain a high sensitivity, high input power range, and competitive peak PCE. Employing a DC-DC converter, we can obtain high output voltages even at low available power levels. Moreover, the SIDITO topology allows for the independent control of the load voltage and of the input impedance, isolating the load from the energy harvester.

5.5. CONCLUSIONS

In this chapter, we have presented the measurement of an RFEH and power management unit that operates from -24 to $+15$ dBm of available input power. The system is designed with the techniques presented in the previous chapters of this thesis. The system employs adaptive techniques in the impedance matching network and DC-DC converter in order to increase the operating P_{av} range. An MPPT circuit is responsible for controlling the DC-DC converter switching frequency and impedance matching configuration to obtain maximum power transfer. Furthermore, the system employs a single inductor for energy harvesting (charging C_{store}) and load voltage regulation (charging C_{load}), while keeping its own internal supply (charging C_{supply}). This allows for a reduction of the overall system size. The system is designed to receive RF power at the center frequency of 403.5 MHz. The measured peak energy harvesting efficiency is 40.2% at $P_{av} = -9.1$ dBm and the sensitivity is -24 dBm while producing a 1.8 V output. The input power range is 34 dB wide while maintaining a PCE above 5%, and 15 dB wide while maintaining a PCE above 20%.

Table 5.1: Comparison Table

| Reference | This Work | TCAS'19 [90] | JSSC'19 [91] | TCAS'15 [45] | JSSC'17 [92] | JSSC'14 [37] |
|---------------------------------|---|------------------------------------|----------------------------------|--------------------------------------|--------------------------------------|-----------------------------------|
| Technology (nm) | 180 | 130 | 180 | 180 | 180 | 90 |
| Frequency (MHz) | 403.5 | 900 | 915 | 900 | 900 | 868 |
| Active Area (mm ²) | 0.2 | 0.06 | 0.4 | 0.27 | 1.08 | 0.029 |
| Additional System Requirements | External Inductors (100 μ H Power Ind.) | Deep N-Well | Ext. Vdd + Loading Control | External Inductors (1 mH Power Ind.) | - | Ext. Micro-Controller |
| Sensitivity (dBm) | -24 (@ 1.8V) | -18.7 (@ 1V) | -17.8** (@ 1V) | -17 (@ 2V) | -14.8 (@ 1V) | -27 (@ 1V) |
| Reported Input Power Range (dB) | 34 (PCE > 5%) 15 (PCE > 20%) | 18* (PCE > 5%) 14.5 (PCE > 40%) | 25* (PCE > 5%) 13 (PCE > 20%) | 10* (PCE > 30%) | 19.5* (PCE > 5%) 10* (PCE > 20%) | 15* (PCE > 5%) 11* (PCE > 20%) |
| Peak PCE | 40.2% (@ 1.8V, -9.1 dBm) | 80.3% (@ 1.1 V, -17 dBm) | 34.4%** (@ +1.3 dBm) | 44.1% (@ 2V, -12 dBm) | 25% (@ -5 dBm) | 40% (@ -17 dBm) |
| System Architecture | CCDD Rectifier + DC-DC Conv. | Modified CCDD Rectifier | Reconfigurable Rectifier | CCDD Rectifier + DC-DC Conv. | Reconfig. Rect. + Voltage Regulation | CCDD Rectifier |
| Number of Rectifier Stages | 1 | 3 | 2-12 | 1 | 1-8 | 5 |
| DC-DC Converter Architecture | SIDITO Buck-Boost Conv. | - | - | Boost Converter | - | - |
| Load Regulation Capability | Yes | No | No | No | Yes | No |

* Extracted from figures.
** Includes the antenna efficiency (93%).

6

CONCLUSION

This thesis focuses on increasing the available input power range for which an RFEH device operates efficiently while maintaining high sensitivity. Broadening the available power range is an interesting topic of energy harvesting research because it increases the number of possible applications of a single RFEH design and enables new applications of energy harvesting technology. In Chapter 1, the motivation and objectives of this thesis, with respect to the above statement, are laid down by studying state-of-the-art RF energy harvesters and wireless power receivers. An RFEH and power management system is proposed and its building blocks are discussed, detailing how their efficiency changes with respect to available power changes.

As we showed in this thesis, the ability of power range broadening is due to two factors. The first one is the possibility of designing adaptive circuits that change their characteristics with respect to a varying input power. We present an adaptive matching network, in Chapter 2, that enables the matching of the antenna-rectifier interface for different power levels. Without this circuit, the losses due to reflection would increase for large input power changes. In Chapter 3, we present the application of configurable power switches in a DC-DC converter. This method broadens the input power range because it balances the conduction and switching losses as the input power and voltage change. However, this level of circuit adaptability comes at a price. By using additional circuits in the chip we are also increasing its current leakage and introducing parasitic capacitances to critical nodes in the power path. Therefore, the same techniques that increase the input power range might lead to a decrease in sensitivity and power conversion efficiency.

The second enabling factor in power range broadening is the ability to reduce the system power consumption. The sensitivity, which is related to the lower point in the available power range, is increased as the power consumption is reduced, because it allows for harvesting at lower power levels. And the power conversion efficiency is increased as well, because of the reduced power losses. In Chapter 3, we present a low-power zero current detection circuit that has low propagation delay. In Chapter 4, we show a input power estimator that exhibits very low current consumption and does not affect the

harvested power. In the same chapters we have shown how we can scale the power consumption of the system with the available power. We use the information from the MPPT circuit to update the settings of the adaptive circuits.

With those two enabling factors, we are able to design an RF energy harvester that presents wide input power range, high sensitivity, and high peak power conversion efficiency. The experimental results of this design and the comparison with the state of the art are presented in Chapter 5. In this concluding chapter we present the original contributions, presented throughout the thesis, that led to these results. We also make recommendations for future work based on the findings of this thesis.

6.1. ORIGINAL CONTRIBUTIONS

The original contributions of this thesis are the following:

- In Chapter 2, a method for finding the most power-efficient, multi-stage matching network composed of lumped capacitors and inductors is presented [50]. The method consists in first deriving the equation of power loss for a simple L-match network, given its input and output impedances. Then, using this simple equation, we derive the equation for a matching network that consists of N L-match stages. A numerical optimization method is then used to find the values of the intermediate impedances in such a way that the power efficiency is maximized, given the quality factor of inductors and capacitors used in the matching network. Finally, the inductor and capacitor values are calculated based on the intermediate impedances values.
- In Chapter 3, we introduce a variation of the W-switching technique [67] that is applied to the common energy harvesting scenario in which the DC-DC converter input voltage changes with the available power. The widths of the main power switches are modulated with the input power and the type of MOSFET used in the power switch connected to the input is also modified. When the input power increases, so does the input voltage, and an NMOS is used in parallel to the PMOS in that input switch. With this technique, we are able to increase the available power range across which the DC-DC converter presents high efficiency [84, 93].
- The zero-current detection capability is fundamental for converters working in DCM to avoid reverse current and discharging of the output capacitor (or battery). However, a fast detector usually presents high power consumption. In Chapter 3, a novel zero-current detector that presents low power consumption and low propagation delay is presented. It consists of an adaptive-bias continuous-time comparator that changes its own biasing current based on its differential input voltage. Therefore, when the inductor current is high, the differential input voltage is high and the comparator current consumption is low. When the inductor current decreases, and the time instant to detect the zero current gets closer, the comparator current consumption increases [84, 93]. In this way, the average power consumption of the detector is reduced. The same technique is applied to the oscillator that generates the system clock signal.

- In Chapter 4, we present an input power estimator circuit used for maximum power point tracking. The presented method does not add sensing elements to the power path, avoiding additional conduction losses. It takes advantage of the buck-boost converter input current characteristic when it is operating in DCM, and it uses only the converter input voltage and switching frequency information to estimate the input power. The circuit consists of a single operational transconductance amplifier that has small area and presents low power consumption [93]. Furthermore, the entire system power consumption is scaled with the MPPT circuit output, leading to low power consumption in low-power conditions and high speed at high-power conditions [84].

6.2. RECOMMENDATIONS FOR FUTURE WORK

The recommendations on topics and directions for future work are the following:

- The sensitivity and peak power conversion efficiency can be further improved by lowering the supply voltage of most of the control circuitry to minimize its power consumption. Besides scaling the operating frequency, as we did in this thesis, simultaneously scaling the supply voltage of the control circuits reduces power consumption. This technique is called Dynamic Voltage Scaling (DVS) and it has been shown that its combination with frequency scaling can lead to considerable power savings in typical digital applications [94].
- In this thesis, the number of stages of the rectifier is kept fixed. In order to further increase the input power range, more research on adaptive rectifiers is necessary. A few recent works in the literature present designs of adaptive/reconfigurable rectifiers [91, 92], but the additional switches in series with the power path tend to degrade the peak power conversion efficiency. Furthermore, their efficiency tends to be low at low available power levels. This is usually due to increased input capacitance, which reduces the input voltage swing.
- The implementation of additional capacitor banks (composed of small capacitors) for enabling impedance matching network fine tuning would be a valuable addition to this system because of two reasons. The first one is the ability to calibrate the matching network against process variations. As shown in Fig. 5.4, in Chapter 5, additional inductors on the PCB were necessary to adjust the matching network. Two capacitor banks can be added in parallel to the existing capacitors, making it possible to calibrate their equivalent capacitance and avoiding the need for those additional external components. The second reason is the ability to calibrate the matching network against input frequency variation. As shown in Fig. 5.7, also in Chapter 5, if the source frequency deviates too much from the center frequency, the power conversion efficiency drops dramatically. By employing a secondary MPPT circuit, the capacitor banks can be adjusted to produce the highest rectifier output voltage, which means that the matching is optimized. However, this secondary MPPT operation must be timed correctly so it does not interfere with the primary MPPT algorithm.

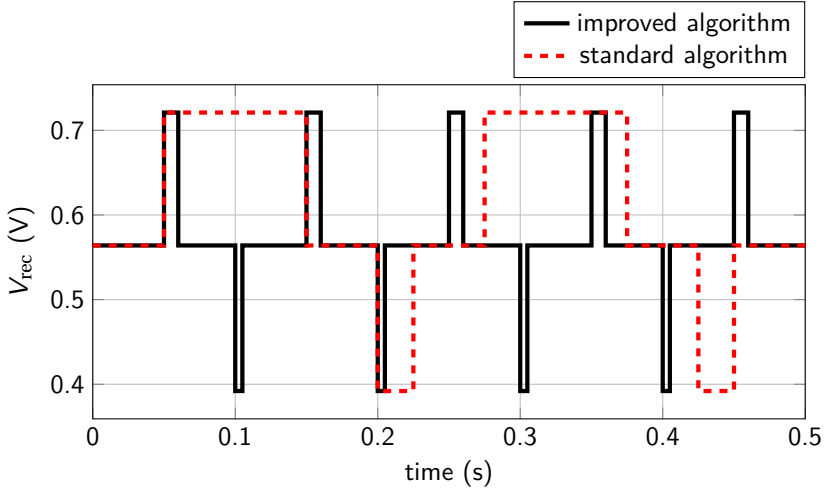


Figure 6.1: An improved MPPT algorithm operation. In this illustration, the V_{Mpp} is about 0.5 V

- Switches S_6 and S_7 of the buck-boost converter (shown in Fig. 3.2, in Chapter 3) are employed to charge the load and are not configurable. The load power range can be extended by making them configurable in the same fashion as switches S_1 - S_4 . To implement this, the average load power information can be programmed into the chip, since it is application dependent. Alternatively, the average load power can be estimated by counting how many pulses of current (N) are necessary, within a pre-determined period (T_L), to regulate the load voltage. If this information is combined with the value of V_{store} , the load power can be estimated by:

$$P_{load} \approx \frac{N}{T_L} \frac{V_{store}^2 T_{ON}^2}{2L} \propto N V_{store}^2. \quad (6.1)$$

- The implemented MPPT algorithm follows the standard P&O algorithm and updates the control parameter FC once at the beginning of the MPPT cycle. However, this behaviour leads to unnecessary reduction of the MPPT efficiency. A better approach is to update the control parameter as soon as the decision is made, i.e., twice within one MPPT cycle. Therefore, less time is spent in configurations that are not the maximum power point one. The desired waveform of the DC-DC converter input voltage would be as the one presented in Fig. 6.1.
- In Chapter 3, we have shown that by generating an offset that is proportional to the DC-DC converter output voltage, the power conversion efficiency can be increased. However, the presented circuit is not truly proportional to the output voltage. So its effect is only optimal in a narrow range of the output voltage. An offset control circuit that is truly proportional to the buck-boost converter output voltage could increase the efficiency. The necessary offset is usually in the order of mV and the offset control circuit must be sufficiently low power, so that the addi-

tional output power is not wasted in the circuit itself.

- The presented system charges its own supply voltage capacitor and it starts charging the storage capacitor when the supply is fully charged. If the available power is much larger than the load power, the storage capacitor will be charged indefinitely, which will damage the chip. In order for this system to be fully autonomous, an over-voltage protection for V_{store} must be implemented. If V_{store} is above the limit, the over-voltage protection circuit would stop the DC-DC converter from charging C_{store} , but allowing it to charge the load if needed.
- It is possible to design power estimation circuits for different topologies and operating modes, following the principles of the power estimation circuit presented in Chapter 4. However, they will be more complex since the input power in those topologies also depends on the output voltage. For example, the input power of the buck converter and the boost converter in DCM are respectively:

$$P_{\text{in,buck}} = \frac{T_{\text{ON}}^2 V_{\text{in}}^2}{2TL} \left(\frac{1}{V_{\text{in}}} + \frac{1}{V_{\text{out}} - V_{\text{in}}} \right), \quad (6.2)$$

$$P_{\text{in,boost}} = \frac{T_{\text{ON}}^2 (V_{\text{in}} - V_{\text{out}})^2}{2TL} \left(\frac{1}{V_{\text{in}} - V_{\text{out}}} + \frac{1}{V_{\text{out}}} \right). \quad (6.3)$$

Therefore, a single differential pair will not be enough to implement any of these functions.

6

In this thesis we have presented circuit techniques that aim to increase the input power range of an RFEH. More research is necessary to combine these techniques with techniques that widen the input frequency band, which would increase the range of applications that could be targeted by the system. Furthermore, different types of harvesters could be tackled, bypassing the RF-DC converter and not limiting the system to RF energy harvesting. To make energy harvesting an attractive choice for replacing batteries, key aspects that need further investigation are the reduction of size and cost. Such a device would facilitate the adoption of energy harvesting to several applications.

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- **G. C. Martins**, A. L. Mansano, M. Stoopman, and W. A. Serdijn, "Introduction to RF energy harvesting," in *Wearable Sensors*, 2nd ed., London, UK: Elsevier Inc. Academic Press, 2021, pp. 311–336.

PRESENTATIONS AND INVITED TALKS

- **G. C. Martins** and W. A. Serdijn, "Rectifier Automatic Impedance Matching for Biomedical Implants," 5th Dutch Bio-Medical Engineering Conference, Egmond aan Zee, The Netherlands, Jan. 2015.
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