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DOI

[10.1109/TBCAS.2020.2971066](https://doi.org/10.1109/TBCAS.2020.2971066)

Publication date

2020

Document Version

Final published version

Published in

IEEE Trans Biomed Circuits

Citation (APA)

Shi, C., Costa, T., Elloian, J., Zhang, Y., & Shepard, K. L. (2020). A 0.065-mm³ Monolithically-Integrated Ultrasonic Wireless Sensing Mote for Real-Time Physiological Temperature Monitoring. *IEEE Trans Biomed Circuits*, 14(3), 412-424. Article 8979270. <https://doi.org/10.1109/TBCAS.2020.2971066>

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A 0.065-mm³ Monolithically-Integrated Ultrasonic Wireless Sensing Mote for Real-Time Physiological Temperature Monitoring

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Abstract—Accurate monitoring of physiological temperature is important for many biomedical applications, including monitoring of core body temperature, detecting tissue pathologies, and evaluating surgical procedures involving thermal treatment such as hyperthermia therapy and tissue ablation. Many of these applications can benefit from replacing external temperature probes with injectable wireless devices. Here we present such a device for real-time *in vivo* temperature monitoring that relies on “chip-as-system” integration. With an on-chip piezoelectric transducer and measuring only 380 $\mu\text{m} \times 300 \mu\text{m} \times 570 \mu\text{m}$, the 0.065-mm³ monolithic device, in the form of a mote, harvests ultrasound energy for power and transmits temperature data through acoustic backscattering. Containing a low-power temperature sensor implemented with a subthreshold oscillator and consuming 0.813 nW at 37 °C, the mote achieves line sensitivity of 0.088 °C/V, temperature error of +0.22/−0.28 °C, and a resolution of 0.0078 °C rms. A long-term measurement with the mote reveals an Allan deviation floor of <138.6 ppm, indicating the feasibility of using the mote for continuous physiological temperature monitoring.

Index Terms—Backscattering, monolithic integration, temperature sensor, ultrasound, wireless sensing system.

I. INTRODUCTION

CORE BODY temperature plays a critical role in many biological processes, including the regulation of metabolism and homeostasis. It is normally controlled through thermoregulation and indicates the body’s state of health [1]. Deviation of more than 1 °C from the normal 37 °C level is usually associated with loss of thermoregulation and potential diseases [2]. Therefore, monitoring of core temperature is crucial for many medical diagnoses and finds wide applications in daily routine monitoring and clinical settings for pre-operative or post-operative patient monitoring. Conventional approaches for core

temperature monitoring include rectal or esophageal probes [1]–[5] and telemetric temperature sensors in the form of ingestible capsules [1], [4], [6]. Commercially available ingestible sensors, including CorTemp (CorTemp HQ Inc.) and VitalSense (Mini Mitter Co., Inc.), contain biohazardous batteries and present relatively large sizes and weights (sizes of >20 mm × 8 mm and weights of >1.7 g [4]), making them ill-suited for the injectable implants pursued here.

In addition to measuring core body temperature, there are various biomedical needs for more localized temperature monitoring for therapeutic purposes, such as the hyperthermia treatment to eliminate tumors [7], [8] or tissue ablation applications with high-intensity focused ultrasound [9]. For thermal-related procedures, accurate real-time temperature mapping at the treatment site is needed to control the amount of applied energy to achieve the desired therapeutic effects while avoiding tissue damage. A common approach to such temperature monitoring is the use of implanted thermal probes placed interstitially within thin plastic catheters in the treatment site [8], [10], [11].

In this work, we consider how multiple miniaturized CMOS-based injectable devices could be used as an alternative for temperature monitoring. We have developed a sub-0.1-mm³, fully-integrated, wireless sensing mote for real-time continuous monitoring of temperature for both core temperature monitoring and temperature monitoring during therapeutic procedures.

The ability to scale the size of a wireless device is limited by the wavelength of the energy used for powering and communication while the implantation depth is limited by absorption and scattering of this energy in tissue. Light offers the shortest wavelengths (sub- μm), enabling the smallest devices but providing for very limited penetration depths (typically <1 mm) [12]. Radio-frequency (RF) energy in the GHz regime allows for devices on the centimeter scale with comparable penetration depths [13], [14]. Ultrasound in the sub-10-MHz regime offers the best trade-offs [15], allowing for device sizes on the order of 200–300 μm with centimeters of penetration thanks to the low tissue attenuation of ~ 0.5 –1 dB/cm/MHz [16]. Ultrasound also offers a much higher safe exposure intensity limit in tissue, 7.2 mW/mm² [17], compared to that of RF energy, which is 10–100 $\mu\text{W/mm}^2$ [18], [19], and is widely used as a safe and noninvasive medical imaging modality. We, therefore, chose ultrasound for powering the motes developed here and for transmitting the acquired temperature data. The

Manuscript received September 17, 2019; revised November 4, 2019 and December 27, 2019; accepted December 30, 2019. Date of publication February 3, 2020; date of current version May 27, 2020. This work was supported in part by the W. M. Keck Foundation and in part by DARPA ElectRx Program HR0011-15-2-0054. (*Corresponding author: Chen Shi.*)

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Digital Object Identifier 10.1109/TBCAS.2020.2971066

use of ultrasound also allows these motes to be identified with imaging, providing biogeographical information *in vivo*.

To achieve the smallest overall volume for these motes, we employed “chip-as-system” integration [20] with “more-than-Moore” enhancement to CMOS [21], [22]; specifically, a microscale piezoelectric transducer is monolithically fabricated on a temperature sensor chip containing all the interfacing electronics [23]. This enables a fully-wireless mote measuring only $380\ \mu\text{m} \times 300\ \mu\text{m} \times 570\ \mu\text{m}$, resulting in a total displaced volume of $0.065\ \text{mm}^3$ and a mass of only 0.3 mg, orders of magnitude smaller and lighter than the commercial sensing capsule, while consuming only 0.813 nW of power at 37 °C. Such extreme miniaturization through monolithic integration allows these motes to be injected using minimally invasive procedures with improved biocompatibility and reduced foreign body response [24]. This offers new approaches for localized *in vivo* monitoring of spatially-fine-grained temperature distributions.

This paper is organized as follows. Section II presents an overview of the proposed temperature sensing mote. Section III describes the design methodology for the mote, including the circuit implementation of the CMOS IC and the fabrication procedures for integrating a piezoelectric transducer with the IC. Section IV discusses the experimental results, and Section V concludes the paper.

II. OVERVIEW OF THE SENSING MOTE

The mote contains a custom low-power temperature sensor IC implemented in a 180-nm CMOS technology and a single lead zirconate titanate (PZT) piezoelectric transducer integrated on the top surface of the IC chip without any other interfacing electronics or bonding wires (as found in larger millimeter-sized sensing systems [12], [13], [15], [25]–[28]). PZT, a piezoelectric ceramic material commonly used in ultrasound imaging [29], is chosen as the transducer for our mote because of its superior piezoelectric properties ($d_{33} \approx 650\ \text{pC/N}$ [30]) that improve energy conversion efficiencies. An external ultrasound probe transmits ultrasound energy to the mote, which is converted by the integrated transducer into electrical energy to wirelessly power the IC. The IC modulates temperature information on the reflected ultrasound echoes returning to the external ultrasound probe through acoustic backscattering [26], [27], [31], [32], thus allowing both wireless power and data transmission. There exist other methods for communication, such as the utilization of a dedicated piezoelectric transducer driven by a transmitter [33] or the employment of an RF coil [15]. These require additional circuit blocks that cost power and area, not feasible for the miniaturized sub-0.1-mm³ mote presented in this paper. We used a commercial linear-array ultrasound probe, L12-3v (Verasonics, Inc.), coupled with a programmable and configurable ultrasound transceiver array, the Vantage 256 system (Verasonics, Inc.), to perform ultrasound energy transmission and data acquisition and analysis through a MATLAB (The MathWorks, Inc.) interface. The Vantage system can be programmed to generate ultrasound at a specific frequency with the desired waveform (including pulse duration and pulse repetition period), beam profile (including focal depth and steering angle), and output power level through

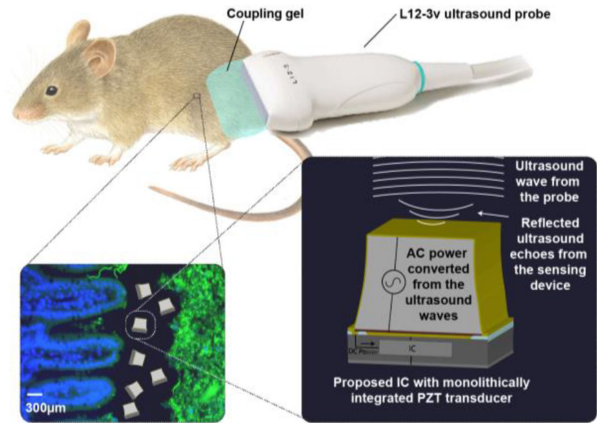


Fig. 1. Conceptual figure illustrating the proposed motes with integrated piezoelectric transducers performing *in vivo* temperature monitoring.

the L12-3v probe. Pulsed ultrasound with an ultra-low duty cycle of $<0.5\%$ is used for receiving the acoustic backscattering data. After transmitting each pulse to the mote, the ultrasound system receives the reflected echoes and extracts the temperature information modulated on the echoes during the idle time in which there is no ultrasound transmission until the next pulse is transmitted, enabling continuous real-time acquisition of temperature data with repeated pulses. This imposes strict requirements on the power harvesting and energy storage components of the mote to maintain proper circuit functionality even without input power, which will be addressed in Section III.

With an extremely compact and lightweight form factor, a number of these motes can be injected into animals to perform localized *in vivo* real-time monitoring of the core body temperature or continuous acquisition of temperature distributions during thermal-related procedures with the biogeographical location of the mote contained in the ultrasound image. Fig. 1 illustrates how multiple motes can be used for mapping physiological temperature inside animal tissues.

III. SYSTEM DESIGN

A. Characterization of the PZT Transducer

The PZT transducer (PZT-5H, Piezo Systems, Inc., [30]) employed to interface with the IC chip has an area of $250\ \mu\text{m} \times 250\ \mu\text{m}$ and a thickness of $267\ \mu\text{m}$. It can be electrically modelled as a parallel-plate capacitor along with a series resistance-inductance-capacitance (RLC) branch representing the mechanical resonance of PZT [34], as displayed in the inset of Fig. 2(a). This electrical model in series with an open-circuit output voltage source forms the Thévenin equivalent circuit of a PZT transducer with ultrasound excitation. The impedance of a $2\ \text{mm} \times 2\ \text{mm}$ PZT piece with the same thickness was measured with a network analyzer (N5230A, Keysight Technologies Inc.). In order to simulate the acoustic load to the PZT when implanted, the measurements were performed by immersing the PZT piece into deionized (DI) water as the ultrasound transmission medium with an acoustic impedance close to that of biological tissues. Since the impedance of each component in the PZT electrical

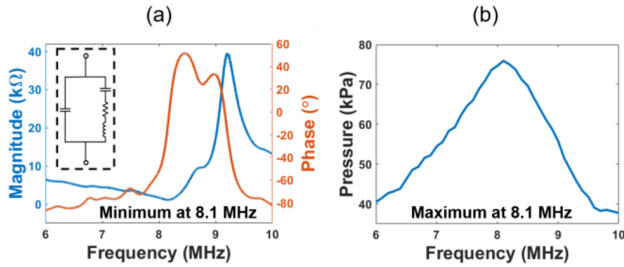


Fig. 2. (a) Derived impedance of a $250 \mu\text{m} \times 250 \mu\text{m}$ PZT piece scaled from the measured impedance of a $2 \text{ mm} \times 2 \text{ mm}$ PZT piece. Inset: the electrical model of PZT; (b) the output pressure amplitude of the $2 \text{ mm} \times 2 \text{ mm}$ PZT piece with excitation voltage across frequency.

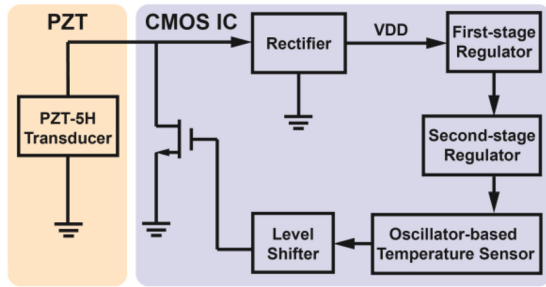


Fig. 3. Block diagram of the temperature sensing mote.

model scales approximately inversely with area, the measured impedance was used to derive the impedance of a $250 \mu\text{m} \times 250 \mu\text{m}$ transducer by scaling the magnitude of the impedance at the same measured phase. As shown in Fig. 2(a), this scaled impedance has a minimum of $1.13 \text{ k}\Omega$ at resonance (8.1 MHz). This resonance was confirmed by exciting the same PZT piece with a 5-V -peak-to-peak sinusoidal signal between 6 MHz to 10 MHz and measuring the amplitude of the acoustic pressure generated from the PZT with a hydrophone (HGL-0200, Onda Corp.), as plotted in Fig. 2(b). The PZT exhibited the strongest piezoelectric response with the highest output pressure at 8.1 MHz . As a result, we chose our operating frequency to be 8.3 MHz , the supported frequency of the Vantage 256 system closest to 8.1 MHz and also the center frequency of the L12-3v ultrasound probe. With a wavelength of $\sim 185 \mu\text{m}$, this operating frequency provides a lateral resolution of $\sim 280 \mu\text{m}$ and a focal spot size as small as $\sim 350 \mu\text{m}$, matching the dimensions of the motes and enabling these motes to be resolved and detected in imaging and to be targeted for more effective powering and communication.

B. Circuit Design

The temperature sensor IC, as illustrated in Fig. 3, consists of a front-end rectifier, two voltage regulators with built-in voltage references, a temperature sensing oscillator, a level shifter, and an n-type metal-oxide-semiconductor (NMOS) transistor acting as a backscatter modulator. The rectifier is based on a voltage-doubler topology implemented with low-leakage MOS diodes. It converts the AC ultrasound energy harvested from the PZT transducer into the DC supply voltage V_{DD} , which is fed into two stages of subthreshold voltage regulators. The

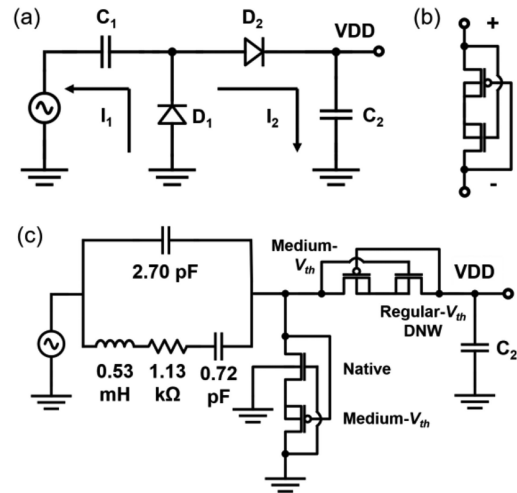


Fig. 4. Schematics of (a) a voltage doubler rectifier, (b) a ULP diode used to implement D_1 and D_2 in (a), and (c) the rectifier in (a) with C_1 replaced with the electrical model of PZT and D_1 and D_2 replaced with ULP diodes.

output of the second-stage regulator provides the supply for a temperature-sensing subthreshold relaxation oscillator, whose oscillation frequency varies with temperature. The temperature-dependent oscillator output is level-shifted to V_{DD} to drive the NMOS modulator shunted across the piezoelectric transducer to induce a two-level change in the electrical loading of the transducer. The resulting modulated ultrasound echoes transmit the temperature information back to the ultrasound probe through acoustic backscattering. Subthreshold operation of the major circuit blocks ensures sub- 1-nW power consumption for the mote. The design specifications and considerations of each circuit block are detailed below.

The voltage-doubler rectifier is shown in Fig. 4(a). The steady-state circuit operation can be described for each half-period [35]. During the negative phase, D_1 is forward-biased and the current I_1 through D_1 charges C_1 to a DC voltage ideally equal to the AC input voltage amplitude; D_2 is reverse-biased and prevents charge on C_2 from flowing back into C_1 . During the positive phase, D_2 is forward-biased and the current I_2 through D_2 discharges C_1 and charges C_2 to create an output voltage ideally equal to twice the input voltage amplitude; D_1 is reversed biased and prevents charge on C_1 from flowing back to ground.

The rectifier output is usually lower than twice the input voltage amplitude due to a finite turn-on voltage and a finite on-state resistance of the diodes. For conventional MOS-based diodes, the turn-on voltage is the threshold voltage V_{th} of the MOS transistors; this voltage drop is usually minimized through the use of low $-V_{th}$ devices. However, low $-V_{th}$ transistors, especially native transistors with a near-zero V_{th} , typically come with large leakage currents when they are reverse biased. In this design, we optimized the forward-to-reverse current ratio for the diodes that maintains proper circuit function for 0.5% -duty-cycle ultrasound pulses. To achieve this, we used the ultra-low-power (ULP) diode [36], displayed in Fig. 4(b), to implement D_1 and D_2 in the rectifier. The ULP diode consists of an NMOS transistor and a p-type MOS (PMOS) transistor. When forward biased, the ULP diode behaves like two conventional MOS diodes connected in series. When reverse biased, however,

both transistors in the ULP diode operate in the deep subthreshold region with negative gate-to-source voltages (V_{GS}) as their sources are connected together. This leads to significantly lower leakage current compared to that of a standard MOS diode, which shows a zero V_{GS} when reversed biased.

Fig. 4(c) presents the detailed schematic of the rectifier, in which the model of the PZT transducer derived from the electrical impedance shown in Fig. 2(a) replaces C_1 and different types of MOS devices are used to implement D_1 and D_2 for efficiency optimization. C_2 is a 250-pF on-chip capacitor, which stores the energy accumulated from the input source and stabilizes the rectifier output. This capacitor takes up the majority of the chip area and serves as the sole storage capacitor in the mote. D_1 employs an NMOS native transistor to maximize the forward conduction and minimize the turn-on voltage, while D_2 is implemented with an NMOS regular- V_{th} transistor with deep-N-well (DNW) to minimize the reverse leakage of charge from C_2 . The NMOS native transistor in D_1 has a slightly higher junction leakage, as native devices have no DNW for separate body connections. PMOS medium- V_{th} transistors are used in both D_1 and D_2 to optimize the forward-conduction-to-reverse-leakage ratio. The body connections of the PMOS transistor in D_1 and both the NMOS and PMOS transistors in D_2 reduce the parasitic junction leakage currents, cancel the source-body biasing in reverse bias, and also avoid latch-up during start-up [35]. To further reduce the chances of latch-up, we performed careful layout by physically separating the NMOS and PMOS transistors and placing guard rings around each of the transistors. In addition, at a sub-1-nW operating power level, transiently, input voltages are less than 2 V and input currents are less than 5 μ A, minimizing the risk of latch-up. The rectifier is designed around the operating frequency of ultrasound with a simulated power conversion efficiency of 71.3%.

Two cascaded stages of voltage regulators with the same architecture are used to regulate the rectifier output and generate a stable supply voltage (peak-to-peak ripple of <50 mV) for the temperature sensing oscillator. Employing two back-to-back regulators improves the power supply rejection ratio (PSRR) and the line sensitivity, defined as the variation of the oscillation frequency of the oscillator to the supply voltage. Each regulator contains a subthreshold voltage reference, which is regulated with a NMOS voltage follower in negative feedback. The basic structure of the voltage reference consists of two stacked NMOS transistors [25], as shown in Fig. 5(a). M_1 serves as a subthreshold current source and feeds a current into the diode-connected transistor M_2 to create an output voltage V_{ref} . The drain current I_D , flowing through a transistor operating in the subthreshold region can be expressed as

$$I_D = \mu_0 C_{OX} \left(\frac{W}{L} \right) (n-1) V_T^2 \left(e^{\frac{V_{GS}-V_{th}}{nV_T}} \right) \left(1 - e^{-\frac{V_{DS}}{V_T}} \right) \quad (1)$$

where μ_0 is the zero bias mobility, C_{OX} is the gate oxide capacitance, W is the transistor width, L is the transistor length, n is the substrate factor, $V_T = kT/q$ is the thermal voltage (~ 26 mV at 300 K), and V_{DS} is the drain-to-source voltage

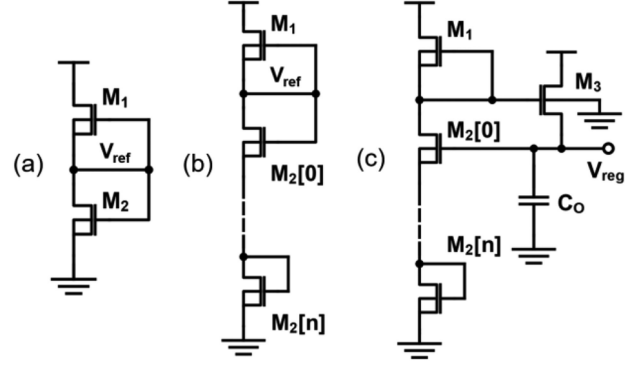


Fig. 5. Schematics of (a) a subthreshold voltage reference, (b) the reference with stacked NMOS diodes, and (c) the complete voltage regulator.

[37]. For V_{DS} greater than 5–6 V_T , I_D can be approximated as

$$I_D = \mu_0 C_{OX} \left(\frac{W}{L} \right) (n-1) V_T^2 \left(e^{\frac{V_{GS}-V_{th}}{nV_T}} \right) \quad (2)$$

By assuming the same V_{th} for M_1 and M_2 and equating the current expressions for M_1 and M_2 , we obtain

$$\left(\frac{W_1}{L_1} \right) \left(e^{\frac{-V_{th}}{nV_T}} \right) = \left(\frac{W_2}{L_2} \right) \left(e^{\frac{(V_{ref}-V_{th})}{nV_T}} \right) \quad (3)$$

and V_{ref} is found to be

$$V_{ref} = nV_T \ln \left(\frac{W_1 L_2}{W_2 L_1} \right) \quad (4)$$

which is proportional to the process-independent thermal voltage. Since V_T is proportional to absolute temperature (PTAT), V_{ref} is also PTAT. The two transistors are both DNW devices with their bulks tied to their corresponding sources to eliminate the body effect. Transistor lengths are made large ($>10 \mu\text{m}$) to reduce short channel effects.

M_2 can be replaced with stacked and identical NMOS diodes to generate a different output voltage [38] (Fig. 5(b)). Different numbers of stacked NMOS diodes are used for the first-stage and second-stage regulators, creating ~ 0.64 V and ~ 0.48 V outputs with a 1.5-V input while consuming ~ 34.4 pA and ~ 18.9 pA of currents, respectively, in simulation at 37 $^\circ\text{C}$. For each regulator, the reference voltage V_{ref} from Fig. 5(b) is then fed into an NMOS source follower M_3 with the output fed back to the NMOS diode $M_2[0]$, providing negative feedback to create a regulated voltage approximately equal to V_{ref} [39], as illustrated in Fig. 5(c). All-NMOS design for these voltage regulators reduces process variation.

A decoupling capacitor C_O (1.45 pF for the first stage and 1.58 pF for the second stage) is added at the regulator output to improve the line sensitivity and PSRR. The output from the second-stage regulator, V_{reg} , provides the local supply for a temperature-sensing RC relaxation oscillator with an oscillation frequency that tracks the temperature. Without dedicated compensation, the PTAT characteristic of V_{reg} is incorporated into the overall temperature characteristics of the sensing mote. When driving the oscillator, the first-stage and second-stage

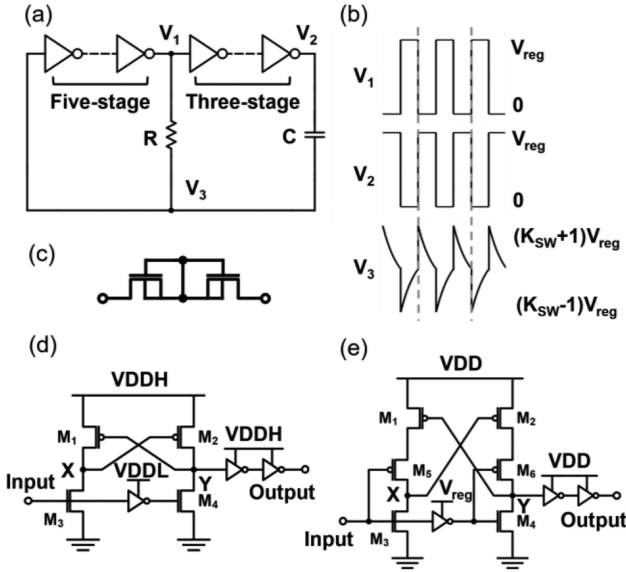


Fig. 6. (a) The schematic of a relaxation oscillator; (b) the voltage waveforms at nodes V_1 , V_2 , and V_3 in (a); (c) the pseudo-resistor used to implement the resistor R in (a); (d) a conventional level shifter; (e) a contention mitigated level shifter used in this design.

regulators show simulated efficiencies of 37.8% and 69.9%, respectively, where the lower efficiency of the first-stage regulator results from it having a larger drop-out voltage from the input of 1.5 V to the output of ~ 0.64 V.

The basic architecture of the relaxation oscillator is shown in Fig. 6(a), with the voltage waveforms at node V_1 , V_2 , and V_3 illustrated in Fig. 6(b). The oscillator contains two inverter chains, a capacitor C connected from V_2 to V_3 , and a resistor R connected from V_1 to V_3 . The use of inverter chains here (of five and three stages) provides high gain and ensures a square-wave voltage at the output [39]. If we define the inverter switching point as $K_{SW} = V_{SW}/V_{reg}$, where V_{SW} is the switching voltage when the input equals the output, the circuit operation can be described as follows. Assuming node V_1 is initially at ground, node V_2 is high at V_{reg} , and node V_3 is at a voltage higher than $V_{SW} = K_{SW}V_{reg}$. The capacitor starts to discharge with a time constant of RC until node V_3 reaches V_{SW} . The inverter chains change states such that node V_1 is high and node V_2 is low. Node V_3 is then immediately pulled down to $(K_{SW} - 1)V_{reg}$ as the voltage across the capacitor cannot change instantaneously. The capacitor C then starts to charge up until it reaches V_{SW} , switching the inverter chains again. This time, V_3 is pulled up to $(K_{SW} + 1)V_{reg}$ before discharging starts, and the operation repeats. V_2 is used as the oscillator output after a buffer stage. The oscillation period is the sum of the time it takes for the capacitor to discharge (t_1) and to charge (t_2) and the total delay through the inverters, denoted as τ_{inv} , during one cycle. t_1 and t_2 are determined by:

$$(K_{SW} + 1)V_{reg}e^{-\frac{t_1}{RC}} = K_{SW}V_{reg} \quad (5)$$

and

$$V_{reg} + ((K_{SW} - 1)V_{reg} - V_{reg})e^{-\frac{t_2}{RC}} = K_{SW}V_{reg} \quad (6)$$

Therefore, the oscillation frequency f can be expressed as

$$f = \frac{1}{(t_1 + t_2) + \tau_{inv}} \approx \frac{1}{Q_{SW}RC + \tau_{inv}}, \quad (7)$$

where $Q_{SW} = \ln\left(\frac{(K_{SW}+1)(2-K_{SW})}{K_{SW}(1-K_{SW})}\right)$. K_{SW} is designed to be 0.5, where the duty cycle of the oscillation is 50% and f achieves the highest immunity to K_{SW} variation. A 10% variation of K_{SW} from 0.5 decreases the oscillation frequency by only 0.4%. In addition, we target f in the Hz-range such that $\tau_{inv} \ll Q_{SW}RC$ and $f \approx \frac{1}{Q_{SW}RC} \approx \frac{1}{2.2RC}$. Such low frequencies save power and are sufficient for quantifying slowly-varying physiological temperature. V_{reg} allows the inverters to run in the subthreshold region with a simulated current of <300 pA at oscillator frequencies of a few Hz at 37 °C.

To achieve these oscillation frequencies, the resistor R must be in the G Ω range, with the pseudo-resistor structure (Fig. 6(c)), in which two identical, well-matched NMOS transistors are connected in series. Looking from both terminals, the pseudo-resistor can be viewed as an off-state NMOS with a zero V_{GS} in series with a forward-biased NMOS diode, and the equivalent resistance in both directions is determined by the voltage difference across the pseudo-resistor, $|V_1 - V_3|$, and the subthreshold leakage current I_D in (1) through each of the two NMOS transistors. Since $|V_1 - V_3|$ is between $0.5V_{reg}$ and $1.5V_{reg}$ (when $K_{SW} = 0.5$), which is larger than $5-6V_T$, I_D becomes largely independent of $|V_1 - V_3|$ and can be approximated as in (2). In that case, the capacitor C is charged and discharged with a constant current flowing through the pseudo-resistor, resulting in a linear voltage ramp of $K_{SW}V_{reg} - (K_{SW} - 1)V_{reg} = V_{reg}$ during the charging cycle and $(K_{SW} + 1)V_{reg} - K_{SW}V_{reg} = V_{reg}$ during the discharging cycle at node V_3 . Therefore, f can be calculated as

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{C_{eff}V_{reg}}{I_D} + \frac{C_{eff}V_{reg}}{I_D}} = \frac{I_D}{2C_{eff}V_{reg}} = \frac{\mu_0 C_{OX} \left(\frac{W}{L}\right) (n-1) V_T^2 \left(e^{-\frac{V_{th}}{nV_T}}\right)}{2C_{eff}V_{reg}}, \quad (8)$$

where C_{eff} is the effective capacitance of the capacitor C , implemented with an NMOS capacitor, and f is no longer affected by K_{SW} , resulting in a stable 50% duty cycle across process corners. By taking into account the temperature dependences of μ_0 , V_T , and V_{th} , and letting $V_{reg} = V_{cons} V_T$, where V_{cons} is a temperature independent constant, the relation between f and the temperature, T , can be expressed as [40]

$$f(T) = \frac{\mu_0(T_0) \left(\frac{T}{T_0}\right)^{-1.5} C_{OX} \left(\frac{W}{L}\right) (n-1) \left(\frac{kT}{q}\right)^2 \left(e^{-\frac{q(V_{th}(T_0) - K(T-T_0))}{nKT}}\right)}{2C_{eff}V_{cons} \frac{kT}{q}} = AT^{-0.5} \left(e^{\frac{B}{T}}\right) \quad (9)$$

where T is absolute temperature, $T_0 = 300$ K, and the temperature-dependent mobility and threshold voltage are given by $\mu_0(T) = \mu_0(T_0)(T/T_0)^{-1.5}$ and $V_{th}(T) = V_{th}(T_0) - K(T - T_0)$ [41], respectively. Here, the secondary effects, such as the variation

of V_{reg} due to supply noise, the temperature dependence of the capacitor C , and the matching errors in the pseudo-resistor R , are not included. We define the temperature-independent coefficients A and B as:

$$A = \frac{\mu_0(T_0) \left(\frac{1}{T_0}\right)^{-1.5} C_{OX} \left(\frac{W}{L}\right) (n-1) \frac{k}{q} \left(e^{\frac{qK}{nk}}\right)}{2C_{eff} V_{cons}},$$

and

$$B = \frac{-q \cdot (V_{th}(T_0) + KT_0)}{nk}, \quad (10)$$

respectively. A two-point calibration (f measured at temperatures T_1 and T_2) can be used to determine fitting values for A and B , denoted as \tilde{A} and \tilde{B} . \tilde{B} is determined from:

$$\frac{f(T_1)}{f(T_2)} = \left(\frac{T_1}{T_2}\right)^{-0.5} e^{\tilde{B} \left(\frac{1}{T_1} - \frac{1}{T_2}\right)}. \quad (11)$$

With this value of \tilde{B} , the overall scaling factor \tilde{A} is then determined from:

$$f(T_1) = \tilde{A} T_1^{-0.5} e^{\frac{\tilde{B}}{T_1}}. \quad (12)$$

Such two-point calibration, performed for each oscillator, accounts for the chip-to-chip variation in I_D , C_{eff} , and V_{reg} . We define the temperature T_{fit} as the one determined by \tilde{A} , \tilde{B} , and the measured frequency f :

$$T_{fit} = \frac{\tilde{B}}{\ln\left(\frac{f}{\tilde{A} T_{fit}^{-0.5}}\right)}, \quad (13)$$

which must be solved self-consistently for T_{fit} . The difference between T_{fit} and each measured temperature T is taken as the temperature error for this oscillator. As an alternative to this calibration, the trimming of the oscillator frequency could also be achieved using a capacitor array with on-chip programmable fuses to implement the capacitor in the oscillator [32].

The oscillator output, V_{osc} , is level-shifted from V_{reg} to the rectifier output, VDD , which is the highest available DC voltage in the circuit, using a level shifter to provide a large enough turn-on voltage for the NMOS modulator. In a conventional level shifter that converts a lower level of $VDDL$ to a higher level of $VDDH$ [42] (Fig. 6(d)), when the input is $VDDL$, M_4 is turned off and M_3 is turned on, pulling node X to ground, which turns on M_2 . This pulls up node Y and the output to $VDDH$, which ensures that M_1 is off. Similarly, when the input is low, the output is driven low. However, this architecture suffers from contention between the PMOS transistors and NMOS transistors and also crowbar currents when the PMOS and NMOS devices are simultaneously on during signal transitions, which increases dissipated power. We, therefore, implemented a contention mitigated level shifter [43] with two additional transistors, M_5 and M_6 , as illustrated in Fig. 6(e). M_5/M_6 along with M_3/M_4 acts as a quasi-inverter to speed to full-rail logic levels at node X and Y . This reduces contention and crowbar currents and saves power with a simulated current consumption of 179.2 pA at 37 °C.

The up-shifted oscillation signal from the level-shifter, periodically turns the NMOS modulator on and off (Fig. 3). This switching places a low electrical impedance (when the

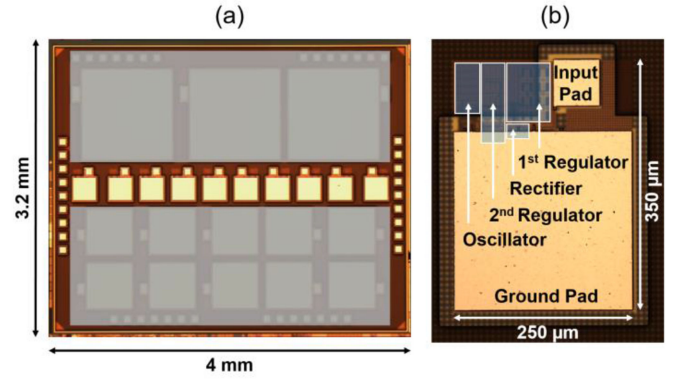


Fig. 7. (a) The die micrograph showing the ten identical temperature sensing chips; (b) the micrograph of one individual chip with the input pad ($65 \mu\text{m} \times 65 \mu\text{m}$), the ground pad ($250 \mu\text{m} \times 250 \mu\text{m}$), and the major circuit blocks labelled.

modulator is on) or a high impedance (when the modulator is off) in parallel with the PZT transducer. This varying electrical impedance at the transducer causes the amplitude of the backscattered ultrasound echoes to vary accordingly [44]. In this way, the oscillation frequency and thus the encoded temperature information can be extracted with the ultrasound system that receives and processes the reflected echoes.

The die micrograph of the chip is shown in Fig. 7(a). It measures $4 \text{ mm} \times 3.2 \text{ mm}$ and contains two standalone oscillators and ten identical temperature sensor chips, each with an area of $350 \mu\text{m} \times 250 \mu\text{m}$ (Fig. 7(b)) located at the center of the die. Of the ten sensor chips, the left-most and right-most chips have wire-bonding pads connected to certain critical nodes inside the chips for both electrical characterization and testing with ultrasound input. The remaining eight chips contain no testing pads enabling only wireless ultrasonic operation.

C. Integration of PZT Transducers With IC Chips

Conventionally, discrete piezoelectric transducers are packaged with the interfacing electronics for ultrasonic wireless systems [15], [26]–[28]. Here, we instead chose to directly build the PZT transducers on the top surfaces of the sensor chips, which significantly reduced the mote volume and the parasitic capacitances associated with the PZT-CMOS interfaces compared to packaged solutions. For achieving this monolithic integration, the rectifier input and chip ground nodes were routed to the top metal layer as accessible pads, as illustrated in Fig. 7(b). The integrated PZT transducer, directly fabricated on the chip, is $300 \mu\text{m} \times 300 \mu\text{m} \times 267 \mu\text{m}$ (with an effective area defined by the size of the ground pad, which is $250 \mu\text{m} \times 250 \mu\text{m}$) with the bottom and top terminals of this transducer electrically connected to the ground and the rectifier input, respectively. Similar piezoelectric structures that can be integrated on-chip include the capacitive micromachined ultrasonic transducer (CMUT) [45] and piezoelectric micromachined ultrasonic transducer (PMUT) [46]. However, a CMUT device requires a large DC bias near the so-called collapse voltage [45], which increases the risk of failure of the device [46] and is difficult to produce from our

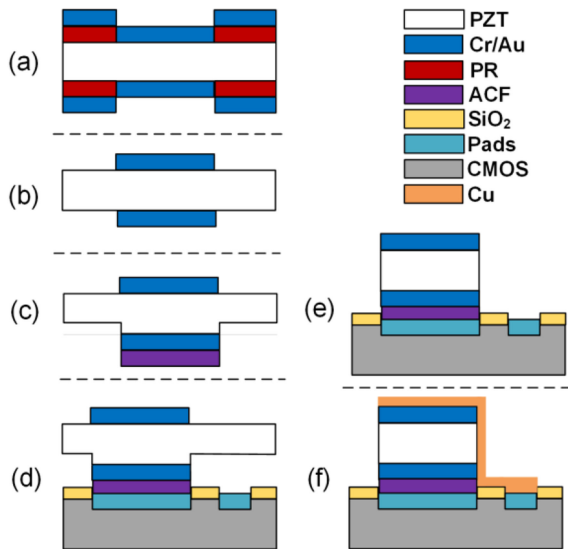


Fig. 8. The fabrication procedures for monolithically integrating the CMOS chips with PZT transducers, including (a) photolithographic patterning and Cr/Au deposition, and (b) lift-off of PR to create contacts on both sides of the PZT that match with the ground pads on CMOS chips, and (c) adhesion of the ACF with the bottom side of the PZT and dicing of the PZT from the bottom side, and (d) bonding of the PZT to the CMOS chips with precise alignment, and (e) dicing of the PZT from the top side to create free-standing PZT transducers, and (f) deposition of copper to connect the top sides of the PZT transducers with the corresponding input pads (modified from [23]).

low-voltage sensor chip. On the other hand, a PMUT device typically shows much weaker electromechanical coupling than that of bulk PZT [47], which is used here.

The fabrication procedures are similar to those previously reported [23], [48], as demonstrated in Fig. 8. The fabrication flow begins with a $7.24 \text{ cm} \times 7.24 \text{ cm} \times 267 \mu\text{m}$ sheet of poled bulk PZT material plated with 50 nm of nickel on both sides. First, the nickel plating is stripped using ferric chloride for 5 s, exposing the PZT surface. Photolithographic patterning with AZ-1512 photoresist (PR) is used to define arrays of $300 \mu\text{m} \times 300 \mu\text{m}$ openings on the top side of the PZT sheet, followed by electron-beam evaporation of a 10-nm chromium (Cr) layer and a 50-nm gold (Au) layer (Fig. 8(a)). Lift-off in acetone is subsequently performed to create contacts that match the ground pads of the CMOS chips (Fig. 8(b)). The same process is applied to the bottom side of the PZT sheet to create vertically aligned contacts on both sides. The sheet is then diced into $4 \text{ mm} \times 3.2 \text{ mm}$ pieces using a dicing saw (DAD3220, Disco). A piece of anisotropic conductive film (ACF, TFA220-8, H&S High Tech) of the same size is then placed on the bottom side of a diced PZT piece. A sub-micron-resolution die-bonder (Fineplacer Lambda, Finetech) is used to apply 0.1 N of force to the ACF at 80°C for 5 s, adhering the ACF to the PZT piece. The PZT piece is then partially diced from its bottom side to a thickness of $\sim 60 \mu\text{m}$ into the PZT (Fig. 8(c)). It is then precisely aligned and bonded to a CMOS die through the ACF by applying a 100-N force at 150°C for 5 s with the die-bonder (Fig. 8(d)), such that the metal contacts on the PZT piece are electrically connected to the corresponding pads on the CMOS die. The conductive particles in the ACF only allow conduction vertically through the metal contacts and not laterally in a manner that would short the pads

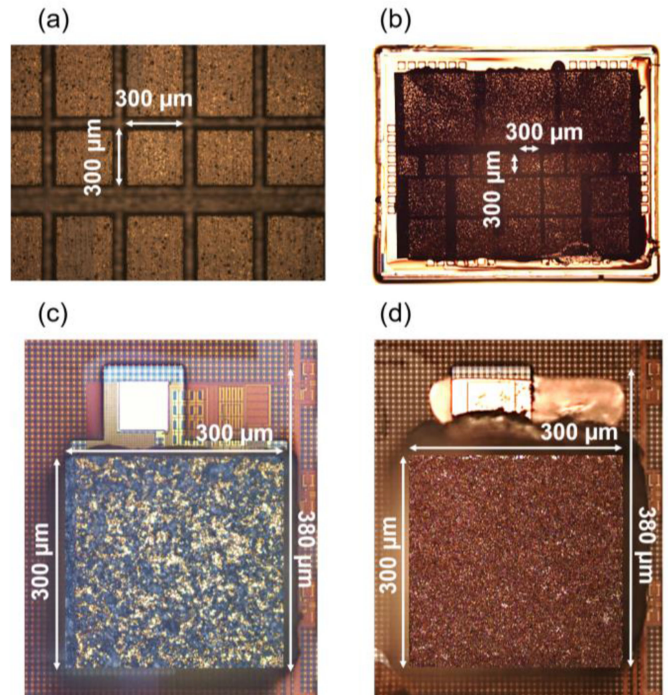


Fig. 9. The microphotograph of the major fabrication procedures for monolithically integrating the CMOS chips with PZT transducers: (a) after bottom-side dicing; (b) after bonding the PZT die with the CMOS die; (c) after the top-side dicing; (d) after metal deposition for the top-side connection.

together. The remainder of the PZT piece outside of the pad areas for each chip is then diced away, leaving free-standing PZT transducers built on top of the CMOS die (Fig. 8(e)). To form the top contact, photolithography with AZ-4620 PR is performed to mask the entire die except for the chip areas, followed by DC sputtering of a 9-nm layer of Cr and a $1.2\text{-}\mu\text{m}$ layer of copper. Sputtering is used to provide sufficient sidewall coverage. After a lift-off process that removes the metal outside of the chip areas, the top side of each PZT transducer is electrically connected to the corresponding rectifier input pad of each chip (Fig. 8(f)).

The micrographs after each of the fabrication steps illustrated in Fig. 8(c)–Fig. 8(f) are shown in Fig. 9(a)–Fig. 9(d), respectively. Finally, the fully-integrated chips are completely encapsulated with a biocompatible, $8\text{-}\mu\text{m}$ -thick parylene film [49], which provides reliable device passivation at thicknesses significantly less than wavelength of ultrasound at our operating frequency, minimizing acoustic losses [50]. Up until this step, ten PZT transducers are monolithically integrated with their corresponding chips on a single die. The fabricated chips are further diced to individual motes sized $380 \mu\text{m} \times 300 \mu\text{m} \times 570 \mu\text{m}$, as shown in Fig. 10. In addition, although this fabrication flow is currently performed at the die level, the same procedures can be applied at the wafer level by scaling up the sizes of the PZT and ACF to match wafer sizes.

IV. EXPERIMENTAL RESULTS

First, the relaxation oscillator with and without the voltage regulation was electrically characterized, including the line sensitivity and jitter performance. The PSRR of each of the

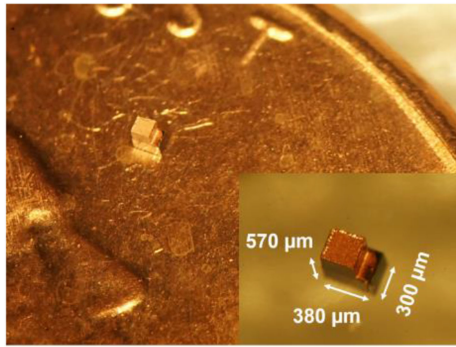


Fig. 10. A fully-integrated and released standalone mote placed on top of a US penny. Inset: a detailed photograph of the device with dimensions.

two stages of regulators was also measured. The temperature sensing performance of three fully-integrated motes prior to their separations from the dies were then tested with an ultrasound input by wire-bonding the motes to custom printed circuit boards (PCBs). Finally, two standalone motes released from the corresponding dies were characterized with an ultrasound input fully-wirelessly in an *in vitro* setting.

A. Electrical Measurements

Six standalone relaxation oscillators were tested at room temperature ($\sim 22^\circ\text{C}$) by directly probing the test pads with DC probes (DCP 100, FormFactor Inc.) to provide the power supply to the oscillator and measure the output frequency, as shown in Fig. 11(a). The oscillators have an average line sensitivity of 145.3%/V (the standard deviation σ over the mean μ is 0.0087) as the average frequency changes from ~ 4.13 Hz to ~ 1.73 Hz when the supply voltage varies from 0.25 V to 0.65 V. Also, the current consumption varies from ~ 56.5 pA to ~ 269.2 pA as the biasing condition of the inverters in the oscillator changes from weak inversion to strong inversion with increasing supply voltage. With the on-chip voltage regulation, however, the average line sensitivity reduces to 0.61%/V ($\sigma/\mu = 0.17$), as plotted in Fig. 11(b). In this measurement, a DC voltage from 0.8 V to 1.8 V was directly applied to the input of the first-stage regulator.

In addition, the period jitter for the oscillator was measured by taking 100 consecutive periods and computing the standard deviation over the mean of the measurements. The oscillator alone shows an average jitter of 287.9 parts-per-million (ppm, $\sigma/\mu = 0.082$) with a 0.4-V supply, while the regulated oscillator shows an average jitter of 401.1 ppm ($\sigma/\mu = 0.18$) with a 1.5-V supply. The PSRR was also measured separately for both regulators from 1 kHz to 20 MHz using an oscilloscope (MSOX4054A, Keysight). The two regulators yield a combined PSRR of ~ 83.9 dB at the ultrasound frequency of 8.3 MHz (Fig. 11(c)). The power consumption of the major circuit blocks, including the two regulators, the oscillator, and the level shifter, was measured to be ~ 541.9 pA at 37°C with a 1.5-V supply (~ 0.813 nW) applied at the regulator input. In simulation, the average power absorbed into the mote, was found to be ~ 26.1 nW (~ 47.2 nW when the modulator was on and ~ 2.1 nW when the modulator

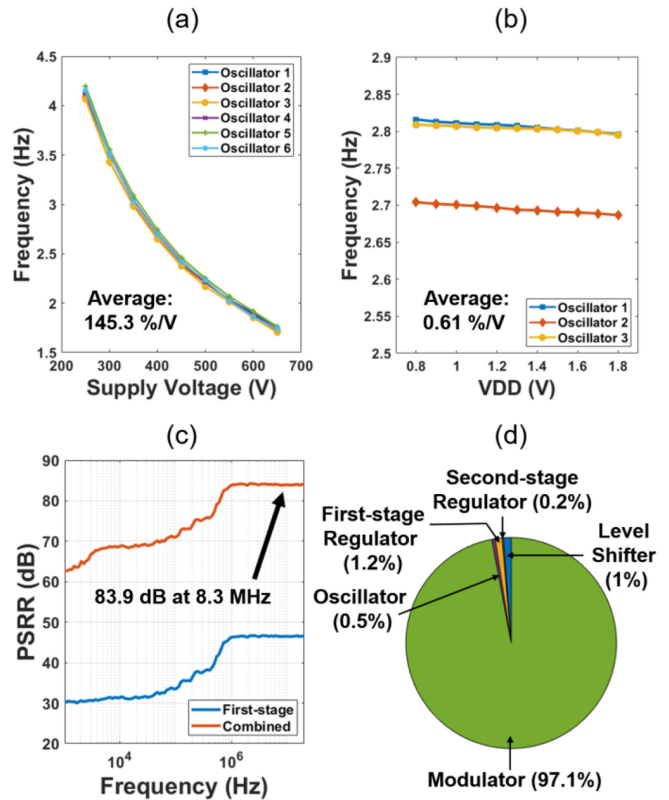


Fig. 11. (a) The line sensitivity of six oscillators; (b) the line sensitivity of three oscillators with voltage regulation; (c) PSRR measurements for both regulators; (d) the simulated power breakdown of the major circuit blocks.

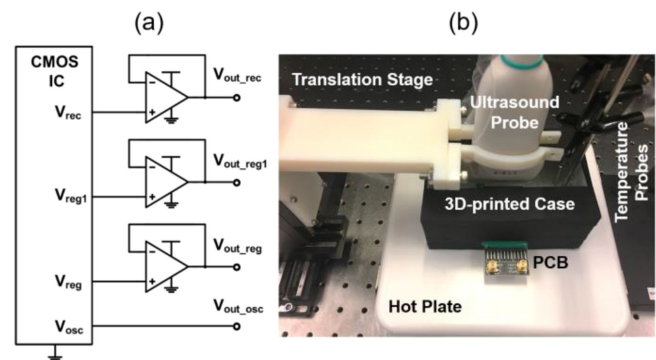


Fig. 12. (a) The schematic of the PCB testing board; (b) the experimental setup consisting of the PCB inserted into a 3D-printed case filled with DI water for testing the performance of the mote.

was off). The simulated power breakdown of each circuit block is shown in Fig. 11(d).

B. Acoustic Measurements of Wire-Bonded Motes

Three fully-integrated motes unreleased from the die were then characterized acoustically with an ultrasound input to evaluate their temperature sensing performance. These motes were wire-bonded to PCBs that contain unity-gain buffers for viewing the output voltage waveforms of the rectifier, the voltage regulators, and the oscillator during circuit operation. Fig. 12(a) shows the schematic of the PCB, and Fig. 12(b) demonstrates the

experimental setup for testing one of the unreleased motes. The PCB with the wire-bonded mote was inserted into an opaque case to eliminate the effects of light on circuit operation. The case was filled with DI water for ultrasound transmission and placed on a hot plate with controlled temperature. A PT-1000 temperature probe in the water bath was used for feedback temperature control. The water temperature was also monitored with a high-accuracy digital thermometer (HH376, Omega Engineering) as the reference temperature throughout the experiments. The L12-3v ultrasound probe, which contains 192 elements with a pitch of $200\ \mu\text{m}$ and an elevation focus of $20\ \text{mm}$ [51], was controlled by a translation stage to move in three-dimensions (3D) and positioned $22\ \text{mm}$ (limited only by the measurement setup) above the mote for power and communication.

A B-mode imaging script is first used to precisely locate the mote. A sub-section of 128 elements on the probe scan as a linear phased array. These are organized into 192 scan lines, segmented such that each line reconstructs a $133\text{-}\mu\text{m}$ -wide region. The transmitted waveform is one cycle of pulse at $8.3\ \text{MHz}$ with an on-time of $\sim 120.5\ \text{ns}$ repeated every $160\ \mu\text{s}$, which is the pulse repetition period. A reconstructed B-mode image can be produced approximately every $40\ \text{ms}$, resulting in a frame rate of approximately $25\ \text{frames/s}$.

Once the mote is located, the software switches to a different mode, in which ultrasound is focused directly onto the mote with a 0° incident angle to activate the mote and process the backscattering data. Again, 128 of the 192 transducer elements on the probe are used. In this case, the ultrasound waveform consists of pulses with a pulse repetition period of $100\ \mu\text{s}$. Each pulse is four cycles of an 8.3-MHz signal with an on-time of $\sim 481.9\ \text{ns}$, such that the duty cycle of the ultrasound signal is approximately 0.48% . As shown in Fig. 13(a), the waveform at the location of the mote was measured using the hydrophone, where the peak pressure amplitude was found to be $\sim 305\ \text{kPa}$, resulting in a spatial-peak temporal-average intensity (I_{SPTA}) of $\sim 0.149\ \text{mW/mm}^2$ calculated as the time-averaged intensity at the focal spot. Four cycles of pulses are found to be optimal with the lowest I_{SPTA} for delivering sufficient power to the mote, as demonstrated in Fig. 13(b). This ultrasound waveform successfully powered up the mote by delivering $\sim 9.3\ \mu\text{W}$ of power to the mote, resulting in an acoustic-to-electrical conversion ratio from the ultrasound source to the mote of $\sim 0.28\%$, similar to the results presented in [31] for ultrasonic devices at the $100\text{-}\mu\text{m}$ scale. The output voltage waveforms of the rectifier, the two regulators, and the oscillator measured at 37°C are shown in Fig. 13(c). The rectifier and the two regulators had voltages of $\sim 1.5\ \text{V}$, $\sim 0.65\ \text{V}$, and $\sim 0.45\ \text{V}$, respectively, and the oscillator ran at $\sim 7.6\ \text{Hz}$. The second-stage regulator shows slightly larger ripple than the first-stage because the second-stage directly drives the oscillator which introduces current transients during transitions. However, this ripple ($< 50\ \text{mV}$ in amplitude) is tolerable since it results in a less-than-120-ppm change in the period jitter of the oscillator.

To obtain the acoustic backscattering data containing the temperature information, the reflected ultrasound echoes for each transmitted pulse are received by the 128 elements of the probe at two samples per wavelength for a total of 896 samples. Each sample corresponds to $60.24\ \text{ns}$ of round-trip travel time

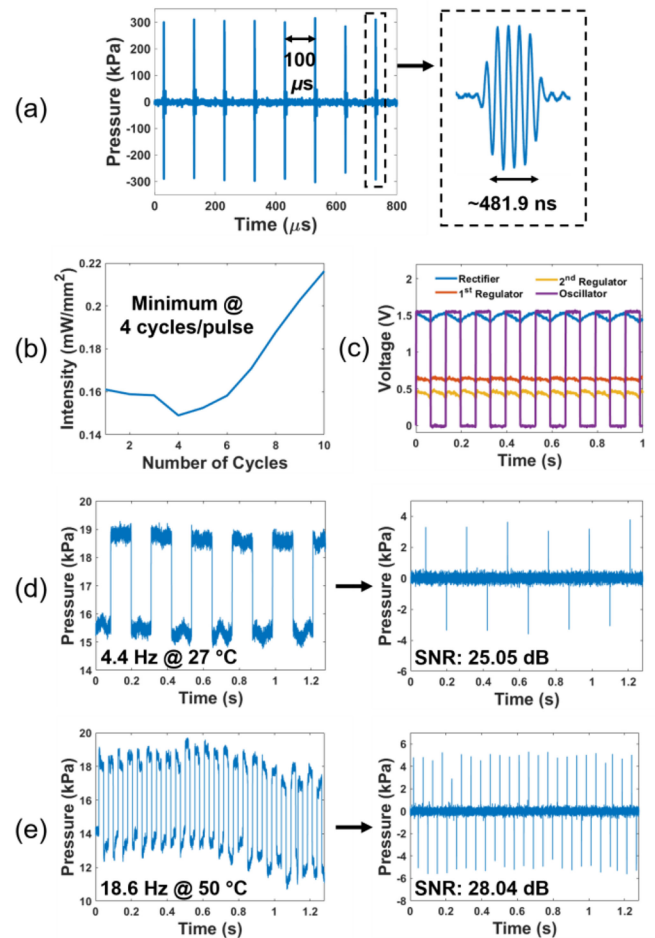


Fig. 13. (a) The waveform of the ultrasound used to power the mote, showing a pressure amplitude of $\sim 305\ \text{kPa}$ with a $100\ \mu\text{s}$ pulse repetition period; (b) the ultrasound intensity to activate the mote with respect to the number of cycles in each pulse; (c) output voltage waveforms of the rectifier, the two regulators, and the oscillator from testing of a wire-bonded mote with an ultrasound input at 37°C , showing an oscillation frequency of $\sim 7.6\ \text{Hz}$; (d) backscattering data acquired at 27°C with an SNR of $25.05\ \text{dB}$; (e) backscattering data acquired at 50°C with an SNR of $28.04\ \text{dB}$.

of ultrasound, translating to a depth resolution of $46.4\ \mu\text{m}$ at a maximum depth of $41.6\ \text{mm}$ with 896 samples. The peak amplitude of the echoes is stored as one frame of backscattering data. 12800 temporally consecutive frames, each separated by the pulse repetition period of $100\ \mu\text{s}$, are acquired to produce $1.28\ \text{s}$ of data. This leads to a minimum detectable change in the oscillation period of $100\ \mu\text{s}$ (limited by the Vantage 256 system and comparable to the jitter of the oscillator) and a sampling rate of $10\ \text{kHz}$, which, together with the jitter of the oscillator, determines the sensitivity of the temperature measurements. A Fourier transform is performed on the acquired data picked up by each element at each depth until the distinct frequency that carries the temperature information is detected. Two examples of the acoustic data obtained at 27°C and 50°C are shown in the left of Fig. 13(d) and Fig. 13(e) with an oscillation frequency of $4.4\ \text{Hz}$ and $18.6\ \text{Hz}$, respectively.

To determine the high-to-low and low-to-high transitions of the oscillator, the difference between adjacent time-points in

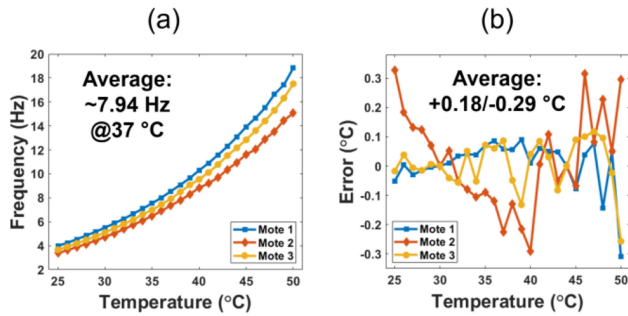


Fig. 14. (a) The temperature curves of three wire-bonded motes; (b) the temperature error for the motes with an average of $+0.18/-0.29$ °C.

the data is calculated. Events in this signal are determined by setting a threshold for magnitudes larger than 2 kPa. The mean magnitude of these events is taken as the average signal, while the standard deviation of the remaining difference values is taken as the rms noise. The SNR is calculated as this average signal divided by this rms noise. As shown in Fig. 13(d) and Fig. 13(e), the SNR values are 25.05 dB and 28.04 dB, respectively, for the two presented sets of acoustic data. In addition, the period of oscillation can be calculated as the difference between these high-to-low or low-to-high transition events, and the averaged period value within each 1.28-s acquisition time is converted to a temperature value with the fitting model in (13). The process repeats in real time to obtain continuous temperature measurements.

The temperature curves of three motes from 25 °C to 50 °C, the biologically relevant temperature range, were acquired acoustically where the frequency varies with temperature from 3.67 Hz to 16.06 Hz in average (Fig. 14(a)). With a two-point calibration at 30 °C and 44 °C, a fitting curve can be obtained using (11)–(13) for each mote. The fit provides an average temperature error of $+0.18/-0.29$ °C with the error across temperature for each mote shown in Fig. 14(b). This performance is comparable to other wireless temperature sensors with much larger form factors [12], [25].

From measurements of these three motes, we find the average oscillator period jitter to be 447.66 ppm (154.8 μ s) ($\sigma/\mu = 0.076$) by taking 100 consecutive period measurements at 22 °C, which is very close to the jitter performance quantified in the electrical testing. This shows that wireless powering with ultrasound introduces a less-than-50-ppm increase in the period jitter of the oscillator. Dividing the jitter by the measured temperature sensitivity at 22 °C (0.0198 s/°C), the temperature resolution (1σ) is found to be 0.0078 °C rms on average, sufficient for physiological temperature monitoring [52]. Also we can convert the line sensitivity of 0.61%/V to 0.088 °C/V with the temperature sensitivity expressed as a percentage (6.9%/°C), which is low enough for the proper temperature sensing functionality. Specifically, the required I_{SPTA} of the input ultrasound power to generate a rectifier output from 0.8 V to 1.8 V was measured to be from 0.07 mW/mm² to 0.25 mW/mm², a wide input range within which the temperature error due to supply variation is only 0.088 °C.

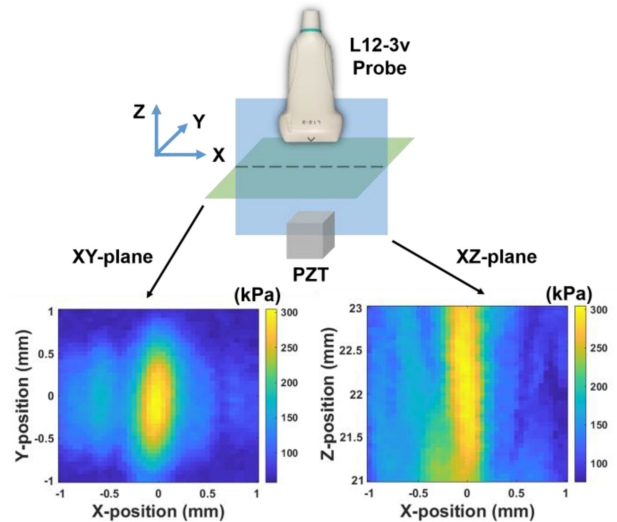


Fig. 15. Top: an illustration of measuring the ultrasound beam profile using a fabricated $250\ \mu\text{m} \times 250\ \mu\text{m}$ PZT transducer; bottom left: the pressure map in the XY-plane at a 22-mm distance in a $2\ \text{mm} \times 2\ \text{mm}$ region; bottom right: the beam pattern in the XZ-plane in a $2\ \text{mm} \times 2\ \text{mm}$ region.

C. Acoustic Measurements of Standalone Motes

The measurements of the wire-bonded motes assumed good alignments between the motes and the ultrasound source, which can be impaired when the motes are implanted. The effects of misalignment were investigated by acquiring the beam profile of the ultrasound applied to a $250\ \mu\text{m} \times 250\ \mu\text{m}$ PZT transducer, that is, one having the same size and fabricated in the same way as the on-chip transducers. As illustrated at the top of Fig. 15, the L12-3v probe was swept in 3D using the translation stage while the output voltage across the receiving PZT transducer was measured at each swept location for the ultrasound source and converted to the received pressure amplitude. The acquired pressure map in a $2\ \text{mm} \times 2\ \text{mm}$ XY-plane parallel to the receiving transducer at a 22-mm distance is shown at the bottom left of Fig. 15. Additionally, the ultrasound beam pattern in a $2\ \text{mm} \times 2\ \text{mm}$ XZ-plane at 21-mm-to-23-mm distances perpendicular to the PZT is shown at the bottom right of Fig. 15. Both plots illustrate a maximum received pressure when the PZT transducer is well-aligned with the ultrasound source with a 0° incident angle. Any misalignment requires an increased ultrasound power to compensate for the loss of the received pressure.

Knowing the beam profile of the ultrasound received by the PZT transducer, we further tested three integrated and standalone motes released from the dies fully-wirelessly with only an ultrasound energy source. In this way, no electrical outputs can be acquired and the only way to determine circuit operation is through the acquired acoustic backscattering data. The experimental setup is shown in Fig. 16. Each mote was separately mounted to the center of a 3D-printed case, similar to the setup for testing the wire-bonded motes. A piece of ~ 3 -mm-thick chicken thigh was placed on top of the mote to mimic biological tissues. To overcome the attenuation due to the chicken thigh, ultrasound was transmitted with a peak pressure amplitude of

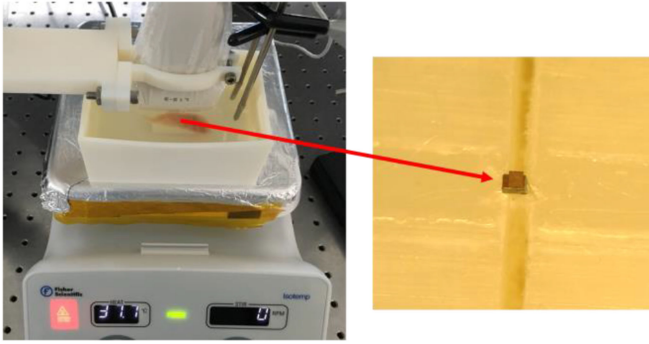


Fig. 16. The experimental setup for fully-wireless ultrasound testing with a mote released from the die. Similar to the testing setup for the wire-bonded devices, the standalone device was mounted on a case and covered with a 3-mm-thick chicken thigh as a biological tissue medium.

~ 451.1 kPa and an I_{SPTA} of ~ 0.33 mW/mm², much lower than the FDA limit of 7.2 mW/mm² [17]. On the other hand, the mechanical index (MI) that characterizes the effects of the peak pressure on animal tissues [29] is calculated to be 0.11, also much lower than the limit of 1.9 [17]. In addition, the thermal index [29] is estimated to be 0.12, indicating a minimal temperature increase of ~ 0.12 °C due to ultrasound under these conditions.

Acoustic backscattering data was acquired again from 25 °C to 50 °C for wireless operation of the three standalone motes (Fig. 17(a)). After a two-point calibration at 30 °C and 46 °C, the average temperature error is found to be $+0.26/-0.26$ °C, as shown in Fig. 17(b), similar to the wire-bonded motes. The average temperature error for the three wire-bonded motes and the three standalone motes combined is found to be $+0.22/-0.28$ °C. Due to device-to-device variation, the six tested motes show moderately different frequency readouts at the same temperature (Fig. 14(a) and Fig. 17(a)). However, after two-point calibration, the six motes produce accurate and similar temperature outputs when compared with the reference temperature, as shown in Fig. 17(c), with an average σ / μ of 0.0035 across the temperature range.

A long-term continuous measurement for one of the motes was performed at ~ 45 °C for over four hours. The acquired temperature data that tracked the temperature fluctuations due to the environment is shown in Fig. 17(d), along with the logged reference temperature simultaneously measured with the thermometer. The Allan deviation of the long-term measurement from the mote is shown in Fig. 17(e), showing a floor of <138.6 ppm, limited only by the measurement time. This demonstrates the minimal self-heating effects from ultrasound on the circuit operation and the feasibility of using the proposed mote for long-term physiological temperature monitoring. Moreover, continuous immersion of a standalone mote in water for >7 days revealed no damage to the film and negligible effects on the circuit functionality, demonstrating the effective encapsulation with parylene.

In addition, the required ultrasound intensities to activate the mote and reliably receive the backscattering data at different incident angles were measured for up to $\pm 20^\circ$ using a rotation stage, where the intensity at $+20^\circ$ or -20° is around nine times

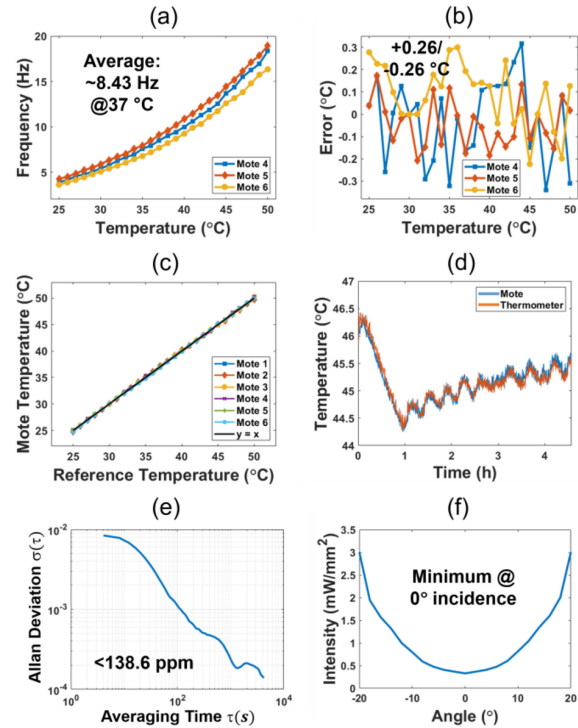


Fig. 17. (a) The temperature curves of three standalone motes; (b) the temperature error for the motes with an average of $+0.26/-0.26$ °C; (c) the calibrated temperature outputs from the six tested motes compared with the reference temperature; (d) a long-term measurement of over four hours of one wireless mote at ~ 45 °C compared with the reference thermometer; (e) Allan deviation of the long-term temperature measurement in (d) showing a floor of <138.6 ppm (limited by the measurement time); (f) the required ultrasound intensity to activate the mote with respect to the incident angle.

TABLE I
COMPARISON WITH STATE-OF-THE-ART

	This work	[12]	[14]	[25]
Technology	180 nm	55 nm	130 nm	180 nm
Dimension	$380 \times 300 \times 570$ μm^3	$360 \times 400 \times 280$ μm^3	480×480 μm^2 (chip only)	$1.1 \times 2.2 \times 0.4$ mm^3
Volume	0.065 mm^3	0.04 mm^3	-	0.97 mm^3
Monolithic Integration	Yes	No	No	No
Calibration	Two-point	Two-point	Two-point	Two-point
Resolution (rms)	0.0078 °C	0.034 °C	0.046 °C	0.3 °C
Sensing Error	$+0.22/-0.28$ °C	$+0.38/-0.33$ °C	$+1.3/-2.6$ °C	$+1.5/-1.4$ °C
Power Source	Ultrasound	Light	RF	Battery
Power Consumption	0.813 nW	16 nW	1.05 μW	71 nW

that at 0° (Fig. 17(f)). This suggests a preferable orientation with no angular mismatch between the motes and the ultrasound source and confirms an inevitable increase in the required ultrasound energy when the motes are not well-aligned with the source. Therefore, the motes should be oriented towards and aligned with the external ultrasound source as much as possible when implanted.

Table I compares the proposed temperature sensing mote with other similar wireless sensing systems, showing a better or

similar sensing performance including temperature resolution and error, but with a more compact form factor with the CMOS-PZT integration efforts pursued in this work.

V. CONCLUSION

This paper presents a miniaturized, low-power, fully-wireless mote with a monolithically-integrated ultrasound transducer for accurate and safe physiological temperature monitoring. Harvesting ultrasound for wireless power and transmitting temperature data through acoustic backscattering, the mote achieves a compact and lightweight form factor through monolithic integration of a CMOS temperature sensor chip with a microscale PZT transducer. Measurement results of fully-integrated motes show a temperature error of $+0.22/-0.28$ °C from 25 °C to 50 °C with a ~ 0.813 nW power consumption at 37 °C. Fully-wireless long-term measurements show a negligible effect from ultrasound on the proper operation of the proposed mote. Therefore, the mote enables continuous *in vivo* temperature monitoring in real time in a minimally-invasive manner.

ACKNOWLEDGMENT

Microfabrication was performed in part at the Columbia Nano Initiative (CNI) cleanroom and the City University of New York Advanced Science Research Center (ASRC) Nanofabrication Facility.

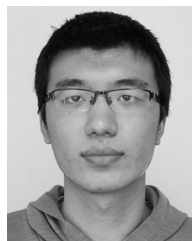
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