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A WAFER-SCALE PROCESS FOR THE MONOLITHIC INTEGRATION OF CVD GRAPHENE AND CMOS LOGIC FOR SMART MEMS/NEMS SENSORS

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ABSTRACT

In this paper we present, for the first time, the successful monolithic wafer-scale integration of CVD graphene with CMOS logic for highly miniaturized smart sensing structures with on-chip readout electronics. The use of a patterned CMOS compatible catalyst for pre-defined regions of CVD graphene growth, and the transfer-free process used, allows the direct implementation of patterned graphene structures between the front-end-of-line (FEOL) and back-end-of-line (BEOL) processes. No significant deterioration of the graphene properties and of the CMOS logic gate performance due to the high temperature graphene growth step was observed. This is a significant leap towards industrial production of graphene-based smart MEMS/NEMS sensors.

INTRODUCTION

Graphene is an extremely attractive material for a variety of sensors [1-2], such as gas, pressure [3], optical and magnetic, due to the high sensitivity originating from the large specific surface area, high mobility [4] and low electric noise [5]. Integrating the graphene sensors with a low-voltage readout technology is highly desirable to ensure signal integrity and opens the door to smart graphene sensors.

Since the first successful isolation of graphene using scotch tape [4], various synthesis methods have been investigated. From all investigated methods, including epitaxy from crystalline SiC wafers and liquid exfoliation, chemical vapour deposition (CVD) on a metal catalyst is presently regarded as the most promising large area synthesis method. However, the catalyst has to be removed to fully exploit the properties of graphene. Moreover, some of the catalysts used, such as copper, are not considered to be CMOS compatible.

For this reason, attempts on transferring graphene on single dies have been reported [6-7]. However, full wafer-scale integration has not been achieved due to the finite graphene sheet size, problems with adhesion and quality degradation due to the transfer. The transferring process is challenging to scale towards industrial production as the yield, wafer-to-wafer uniformity and production speed are intrinsically limited.

This work, integrates the transfer-free graphene fabrication [8], which was previously developed by our group, in a seven mask CMOS fabrication process [9] after the gate oxide formation and before the BEOL metallizations. This allows monolithic integration on wafer-scale (Fig. 1) by circumventing the scalability issues encountered in wafer-to-wafer transfer of graphene. To demonstrate the potential of the developed process, devices are characterized with and without the addition of graphene to investigate the impact of the graphene process on device performance. Furthermore, basic CMOS logic is designed and investigated. The graphene layer quality is monitored throughout the process to demonstrate the full compatibility.

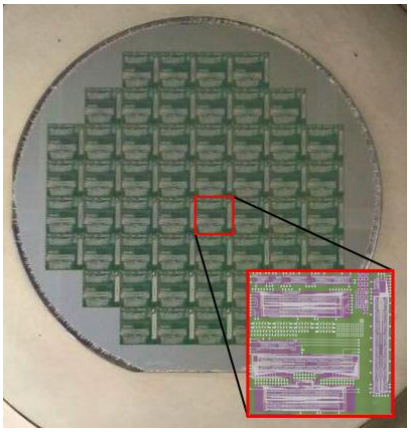

Figure 1: Device wafer. *Photograph of 4" device wafer after second metallization and before molybdenum etch. Inset shows a micro photograph of a single die, where the graphene structures and CMOS logic are located in the green and purple regions, respectively.*

EXPERIMENTAL

The fabrication process for a typical graphene structure and a PMOS transistor is illustrated in Fig. 2. The process is designed using three masks for the implantations, two for the graphene structures definition and four for the two-level interconnects. The reported process provides complete freedom in the design of the graphene structures and CMOS electronics and connects them in the second metal layer. The only restriction in the current process is that the graphene cannot be placed on top of a MOS device, but this is not an inherent limitation of the proposed integration approach.

Firstly, the doped regions, consisting of an n-well, guard ring and source/drain implants of the transistors, are implemented. Secondly, a 600 nm SiO_2 layer is deposited and patterned to form an elevated region for the graphene structures, followed by a 100 nm gate oxidation. The elevated region is an optional design choice, that has been included to ensure similar elevation in the graphene and CMOS regions which reduces step heights in the second interconnect layer. After this front-end process, a CMOS compatible molybdenum (Mo) catalyst is deposited and patterned on the elevated

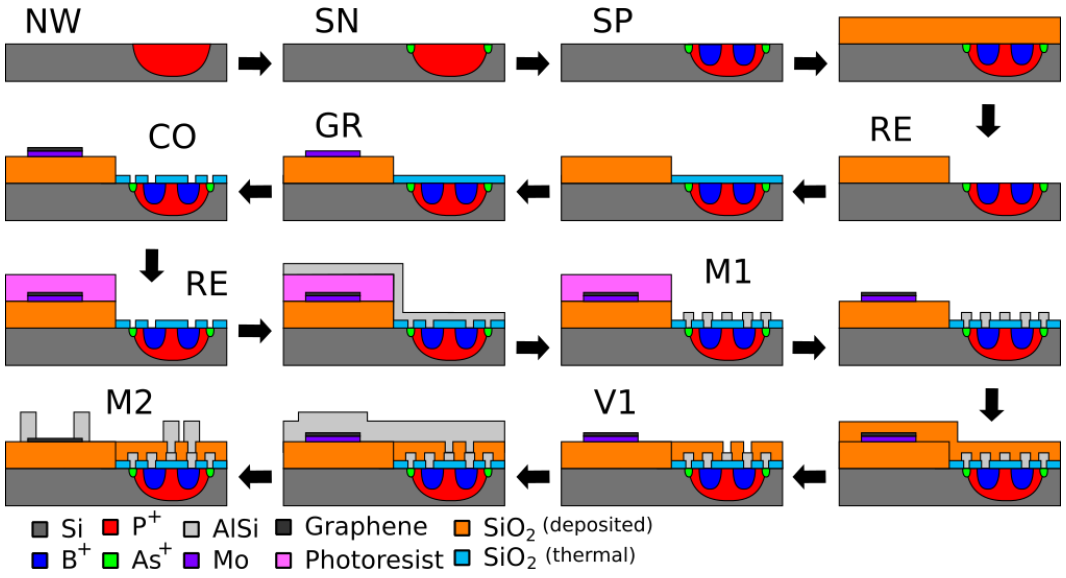

Figure 2: Process overview. *Schematic representation of the fabrication process of a monolithically integrated graphene structure with a PMOS transistor. A nine-mask design was used to implement the CMOS devices, interconnects and graphene structures; NW is n-well, SN is shallow n-type, SP is shallow p-type, CO is contact openings, M1 is first metal layer, V1 is vias, M2 is second metal layer, RE is region for graphene structures position and GR is graphene/catalyst.*

regions. Multi-layer graphene is then grown selectively on the Mo using CVD at 915 °C, for varying deposition times to investigate the graphene growing time on the MOS device performance. This is followed by the BEOL metallization. The Mo is preserved until the end of the process to ensure good adhesion of the graphene to the SiO_2 and is removed after the patterning of the second metal layer.

The Mo and graphene stack impacts the BEOL process in two ways. Firstly, the possibilities for etching the interconnect metals are limited as dry etching will also etch graphene and many chemicals used for wet etching will also etch Mo. This is solved by covering the Mo and graphene stack during the first metal layer etch and a partial dry etch followed by a wet etch in 0.5% hydrofluoric acid (HF) in the second metal layer etch. Secondly, the standard wafer cleaning steps to remove photoresist residues will also etch either the graphene or the Mo. This issue is circumvented by performing this cleaning in n-methylpyrrolidon (NMP) at 70 °C.

To investigate the graphene quality at different stages in the fabrication process, Raman spectroscopy is performed [10]. This analysis technique observes vibrational, rotational and other low-frequency modes in the sample by exposing it to a laser and monitoring its optical response. The Raman spectra are commonly used to investigate the structure of molecules or solids. Likewise, CMOS devices are electrically characterized on wafer-scale using a semi-automatic probe station.

RESULTS AND DISCUSSION

Using the reported wafer-scale fabrication process, test structures were fabricated (Fig. 1) and characterized. A selection is reported in this paper. From the Raman spectra in Fig. 3 three unique peaks, called G-, D- and 2D-peak, can be identified. The G-peak at approximately 1580 cm^{-1} corresponds to the in-plane vibrations of the sp^2 hybridized carbon atoms in the graphene lattice. The D-peak at approximately 1330 cm^{-1} is induced by all kinds of defects in the graphene film and the 2D-peak at approximately 2660 cm^{-1} is an overtone of the D-peak as well as a result of the double resonance Raman scattering process. The relatively high D peak after graphene growth originates from the CVD process and can be reduced by tuning the recipe [11]. However, a controlled number of defects can actually be advantageous for specific sensor applications, where defects act as absorption sites. The unchanged D/G ratio after the first metallization indicates no deterioration of the graphene quality and the minor change in D/G ratio indicates a minor degradation after

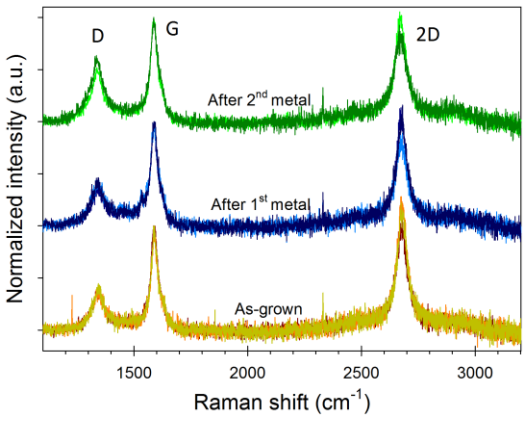

Figure 3: Raman spectra. *Raman spectra obtained at three different stages in the fabrication process, where three separate measurement results per stage are given. The D/G ratios indicate that the multi-layer graphene remains intact throughout the process with little degradation in the quality. A 633nm laser was used in the measurement setup.*

the second metallization. This degradation likely originates from the PECVD oxide deposition, during which the graphene is exposed to oxygen radicals. Adding a protective layer before the PECVD deposition could prevent this. The preserved graphene quality indicates the successful integration of graphene in the CMOS process. From the 2D/G ratio and the width of the 2D- peak it is clear that the sample consists of multi-layer graphene.

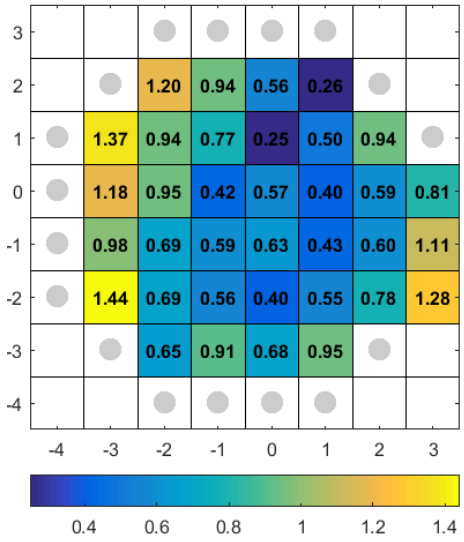

Figure 4: Graphene sheet resistance. *Wafermap of the graphene sheet resistance [kΩ], with mean value of 0.8 ± 0.3 kΩ. The grey circles mark broken devices. Part of the non-uniformity originates from the single zone heater of the CVD.*

The graphene sheet resistance is measured on wafer-scale using Van der Pauw test structures. The results are depicted in the 52 die wafer map in Fig. 4. The devices on the wafer edge are broken due to Mo residues in this region, caused by the not optimized non-uniform dry etching of the Mo to pattern it. An average graphene sheet resistance of 0.8 ± 0.3 kΩ is obtained, which is in

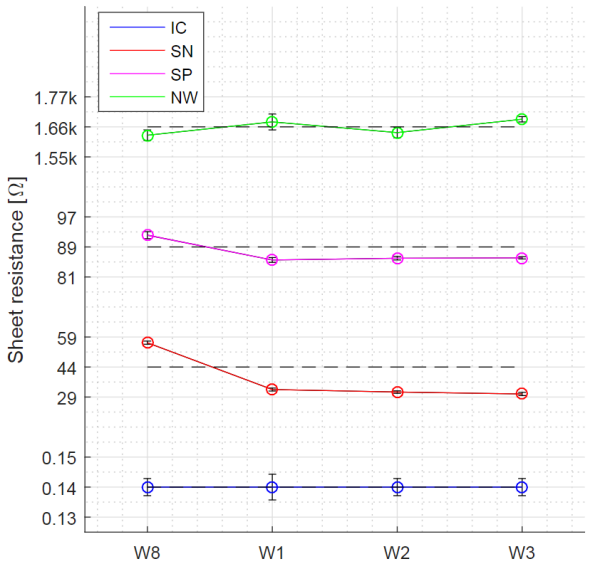

Figure 5: Doped region sheet resistance. *Results of the averaged wafer-scale measurements of the doped region sheet resistances. The n-well (NW), source/drain contacts (SN) and (SP) and the metal interconnect (IC) are included.*

agreement with previously published data on the transfer-free process [8].

Wafer-scale measurements of the doped region sheet resistance are performed on four wafers with different graphene growth times (Fig. 5) and revealed a change before and after growth for the SN and SP regions. However, the observed change is independent of the growth time, which suggests that the drop is not caused by dopant diffusion. A likely cause for the drop is that the graphene growth cycle completes the dopant activation, which may not be completed during the short thermal gate oxidation/dopant activation step in the used process.

Similarly, wafer-scale measurements of the threshold voltage were performed (Fig. 6), which revealed an acceptable shift in threshold voltage after graphene

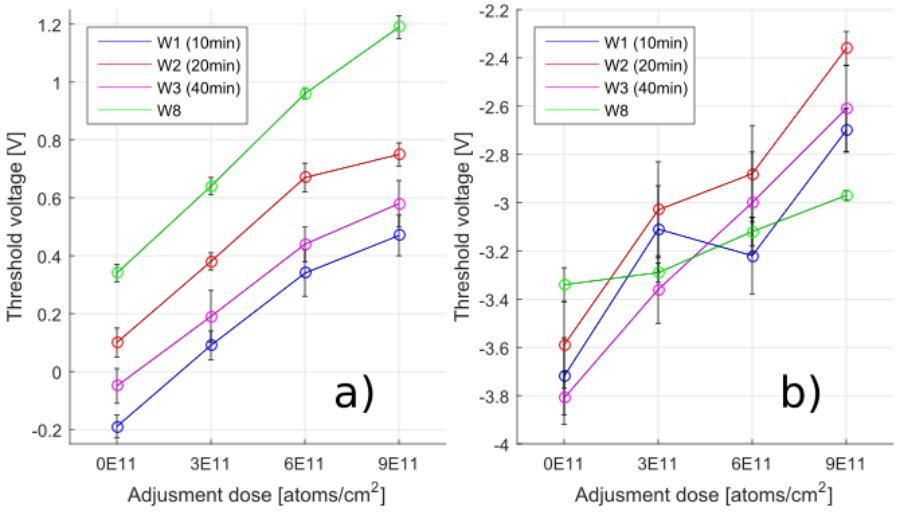

Figure 6: Threshold voltage. *Results of the threshold voltage measurements of a) NMOS and b) PMOS devices of 20 µm x 5 µm (W x L) on four wafers before (W8) and after (W1-3) graphene growth with different deposition times. Four different adjustment doses for the threshold voltage are implemented on each wafer.*

growth. The threshold voltage of an NMOS device can be determined by

$$V_{Tn} = \left(\left|Q'_{SD}(\max)\right| - Q'_{SS}\right)\frac{t_{ox}}{\varepsilon_{ox}} + \phi_{ms} + 2\phi_{fp} \quad (1)$$

where $\left|Q'_{SD}(\max)\right|$ is the magnitude of the maximum space charge density per unit area of the depletion region, Q'_{SS} the oxide charge, t_{ox} the oxide thickness, ε_{ox} the permittivity of SiO_2, ϕ_{ms} the metal-semiconductor work function difference and ϕ_{fp} the fixed work function of a p-type channel [12]. The PMOS threshold voltage is determined similarly. It was suggested by the measurement results in Fig. 5 that the graphene growth causes no significant dopant diffusion and since the sheet resistances are stable for each graphene growth time, it can be concluded that the dopant activation seems to have no effect on the threshold voltage. As a result, only Q'_{SS} is left as a variable parameter, indicating that a likely cause for the threshold voltage shift is due to a change in trapped surface charge in the gate oxide. This shift, thanks to the reproducibility of the developed process, can be taken into account during circuit design.

Similarly to the MOS device measurements, the responses of four logic gates were investigated on wafer-scale. Typical responses of each logic gate after the graphene growth are depicted in Fig. 7, which shows expected behavior.

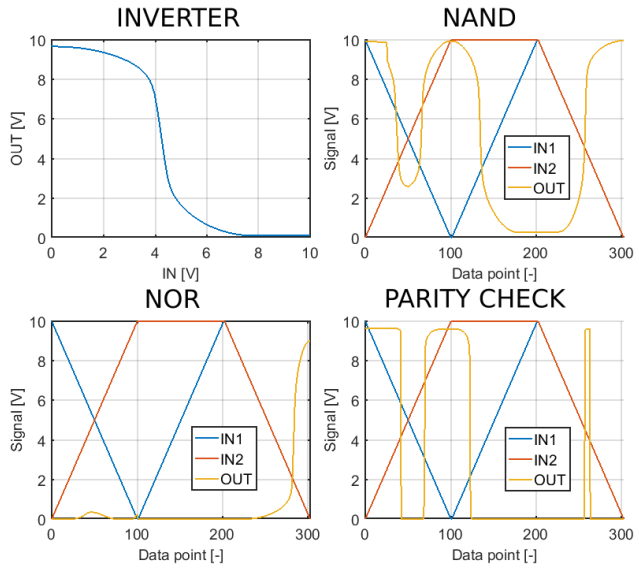

Figure 7: Logic gate responses. *Response of the inverter, NAND, NOR and parity check gates on die -2,-3 (see Figures 1 and 4 for reference). Note that the transitioning of IN1 and IN2 from high to low and vice versa cause dips or peaks in the output, which is due to the switching voltage of the logic gates not being at half of the supply voltage.*

CONCLUSIONS

The proposed process allows CVD of graphene directly on a CMOS device wafer, thus avoiding the need for transferring graphene, and without affecting correct device operation. This creates a promising platform for monolithic integration of multiple graphene-based sensors with on-chip readout, while keeping wafer-scale capability. The graphene growth caused full dopant activation and acceptable threshold voltage shift due to a change in gate oxide trapped surface charge.

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