A Self-Powered Bipolar Rectifier-Less Series-SSHI Circuit with Dual-Polarity Energy Extraction for Piezoelectric Energy Harvesting

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A Self-Powered Bipolar Rectifierless Series-SSHI Circuit With Dual-Polarity Energy Extraction for Piezoelectric Energy Harvesting

Zijun Qiu, Sreedharan Maniyil, Wenyu Peng, *Graduate Student Member, IEEE*, André C. van der Ham, and Sijun Du, *Senior Member, IEEE*

***Abstract*—This article presents a self-powered, bipolar, rectifierless series synchronized switch harvesting on inductor (BiReL-SSHI) interface circuit for piezoelectric energy harvesting. At both the positive and negative peaks of the piezoelectric transducer (PZT) voltage, a synchronous switch is automatically activated, enabling energy transfer from the PZT to a storage capacitor, while the inductor simultaneously inverts the PZT voltage for the next half cycle. Compared to conventional full-bridge rectifiers (FBRs) and series synchronized switch harvesting on inductor circuits, the BiReL-SSHI topology employs fewer components by optimizing the positive and negative synchronous switches, thereby reducing power loss and improving energy extraction efficiency. Experimental results show that the BiReL-SSHI achieves a 5.4× improvement in power extraction compared to an FBR, when the open-circuit voltage (V_{oc}) of the PZT is 8 V. Furthermore, in scenarios where a high V_{oc} is converted to a low output voltage, the BiReL-SSHI achieves superior energy transfer efficiency compared to other interface circuits. Experimental results further demonstrate that at a 3.3 V output under identical vibration conditions, the BiReL-SSHI delivers 5.86× higher output power than the FBR.**

***Index Terms*—Energy harvesting (EH), piezoelectric transducer (PZT), rectifierless, self-powered, series synchronized switch harvesting on inductor (S-SSHI).**

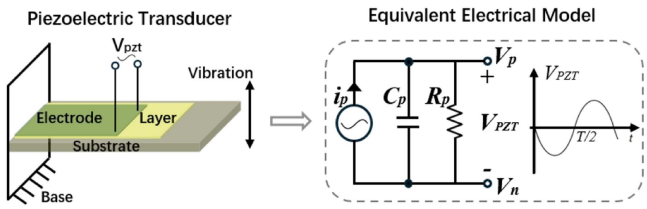

Fig. 1. PZT and its equivalent circuit.

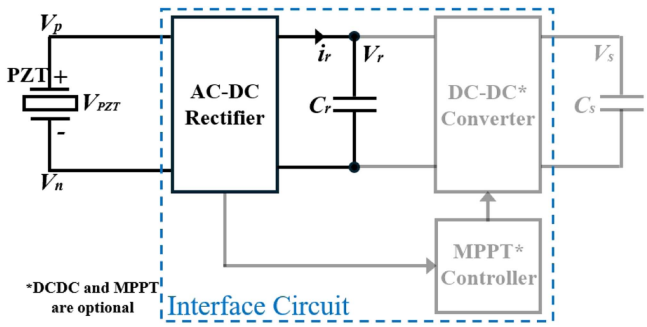

Fig. 2. Block diagram of a typical PEH system.

I. Introduction

With the rapid proliferation of Internet of Things devices and wireless sensor networks, the frequent replacement of depleted batteries has become increasingly costly and impractical, creating a strong demand for alternative power sources. Energy harvesting (EH) has emerged as a promising solution, enabling the conversion of ambient energy from diverse sources—such as solar, thermal, and kinetic—into electrical energy to power low-power electronics [1], [2], [3], [4]. Among these, kinetic energy offers distinct advantages, including low cost, low operating frequency, and relatively high power density, typically in the range of 10–500 μW/cm^2 [5]. Piezoelectric energy harvesting (PEH) is particularly effective for converting ambient mechanical vibrations into electrical energy, utilizing a piezoelectric transducer (PZT) together with an interface circuit. A weakly coupled PZT operating at its resonance frequency can be modeled by an equivalent circuit, as shown in Fig. 1, consisting of a sinusoidal current source i_p, an internal capacitance C_p, and a parallel resistance R_p. The resulting output voltage $V_{\rm PZT}$ is an ac signal [6], [7], [8], [9]. Beyond the transducer, an efficient interface circuit is critical for maximizing the effectiveness of a practical PEH system. As illustrated in Fig. 2, a typical architecture comprises an ac–dc rectifier, a dc–dc converter, a maximum power point tracking (MPPT) controller, and an energy storage capacitor [10]. Since the PZT generates an ac output, the rectifier is essential to convert this into dc power suitable for the load. In contrast, the dc–dc converter and MPPT controller are optional, providing voltage regulation and power optimization. Over the past decade, various ac–dc rectifier schemes for PZTs have been proposed, primarily based on full-bridge rectifiers (FBRs) [11], synchronized switch harvesting (SSH) [12], [13], [14], [15], [16], [17], or synchronous electric charge extraction

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Zijun Qiu, Sreedharan Maniyil, Wenyu Peng, and Sijun Du are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: sijun.du@tudelft.nl).

André C. van der Ham is with SKF B.V., 3992 AE Houten, The Netherlands.

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(SECE) [18], [19], [20]. The FBR is the simplest and most commonly used interface circuit, utilizing four passive diodes and requiring no active components. However, its energy extraction efficiency is limited. The presence of the parasitic capacitance C_p leads to additional energy loss during voltage flipping, caused by the phase difference between the voltage V_{PZT} and the current i_p [21]. Moreover, conduction through two diodes in the power path results in further energy losses due to the voltage drops across the diodes.

In contrast, the SSH method offers improved EH efficiency. Specifically, the synchronized switch harvesting on inductor (SSHI) technique enhances energy extraction by employing an inductor to flip the voltage across the PZT, thereby minimizing charge wastage associated with the parasitic capacitor C_p. Badel et al. [22] introduced the parallel SSHI (P-SSHI) rectifier, where the inductor is placed in parallel with the PZT, while Lefeuvre et al. [23] developed the series SSHI (S-SSHI) topology, connecting the inductor in series with the transducer. The SECE approach is another widely adopted technique, notable for its output power being largely independent of the connected load. A transformer-based SECE circuit demonstrated a 400% power improvement over the FBR [24]. Building upon these topologies, the authors in [25], [26], [27], and [28] proposed a synchronized switch harvesting on capacitors (SSHCs) circuit, which replaces bulky inductors with on-chip capacitors for charge flipping, enabling full integration.

However, powering and controlling the switches in these circuits typically requires an external timing circuit, which consumes additional power. This dependence limits their suitability for applications lacking an existing or precharged power supply. To address this, initial work on self-powered SSHI [29] was enhanced by Liang and Liao [30], who incorporated two electronic breakers comprising envelope detectors, comparators, and bipolar junction transistors to autonomously control switching events. Subsequent advances in self-powered series and parallel SSHI circuits have reported up to 3.6× improvements in output power over FBRs by optimizing switching delays [31], [32], [33].

However, all these designs employ FBRs, which will result in energy loss and system complexity. Also, the presence of the rectifier means that the interface circuit must overcome the threshold voltage of the rectifier to make the harvesting energy flow possible, otherwise, it cannot function [34]. To mitigate this, rectifierless architectures have been introduced recently. Shi et al. [35] introduced a rectifierless interface circuit to perform SECE with promising power performance. A rectifierless S-SSHI interface circuit was proposed in [36], which achieved an improvement of 5.9× compared to a FBR. Chen et al. [37] presented a novel rectifierless electric charge extraction and inversion interface circuit as an improvement to the SECE method while eliminating the rectifier and reported a 4.2× improvement in energy harvested as compared to an FBR. The work presented in [38] suggests that if the internal capacitance of the PZT is small, then there exists a greater chance of a second inversion occurring at the end of each inversion while performing SSHI. It goes on to suggest an interface circuit to reduce the effects of the second inversion on energy extraction performance. As an improvement to the interface circuit proposed in [38], an interface circuit was proposed in [39] that also reduces the effects of the second inversion while eliminating the FBR from the circuit.

For interface circuits that perform flipping of the piezoelectric (PE) voltage, such as the SSHI and SSHC topologies, the flipping efficiency has a pronounced effect on the power extraction efficiency. In the case of ideal flipping, the voltage at the end of the flipping is equal in magnitude to the voltage before the flipping. In this case, no charge from the transducer is used to charge up the parasitic capacitor of the transducer, thus reducing energy loss. New interface circuits were proposed in [40] and [41], which combine SSHI and SSHC techniques while flipping in multiple stages, to achieve a maximum flipping efficiency of 90.3% and 96.3%, and power enhancement of 642% and 648%, respectively.

Most of the discussed interface circuits perform best under optimal electrical tuning conditions [42]. This optimal point, which is often called the maximum power point (MPP), will be affected by many factors. Therefore, if there is a requirement to maximize power extraction efficiency, an MPPT technique is necessary. A quasi-MPPT circuit proposed in [43] utilizes open-circuit-voltage sampling and bidirectional dc–dc converters to improve the extraction efficiency of an FBR interface circuit. Yue et al. [44] proposed a duty-cycle-based MPPT system for an SSHI interface circuit and reported 98% peak MPPT efficiency and 738% improvement in output power. Despite the performance enhancement due to the MPPT circuits, they increase the system complexity and quiescent power consumption.

In this work, a novel bipolar, self-powered, rectifierless series SSHI interface circuit (BiReL-SSHI) is proposed. By eliminating the rectifier bridge and utilizing a self-starting synchronous switch, the BiReL-SSHI achieves reduced power loss and enhanced energy extraction efficiency. Compared to the FBR, the proposed circuit achieves a 5.4× improvement in power extraction. Moreover, in contrast with the rectifierless SSHI (ReL-SSHI) circuit [36], the BiReL-SSHI captures more energy in each cycle, delivering higher extraction efficiency at low output voltages. Under identical vibration conditions, the BiReL-SSHI achieves a 62.5% increase in output power at a 3.3 V output voltage. The rest of this article is organized as follows. Section II details the operating principles of the BiReL-SSHI circuit and compares it with ReL-SSHI and S-SSHI topologies. Implementation details are presented in Section III. Section IV presents simulation analysis. Section V presents experimental validation. Finally, Section VI, concludes this article.

II. Prior Arts and the Proposed BiReL-SSHI

A. Conventional S-SSHI and ReL-SSHI

Fig. 3(a) illustrates the topology of a conventional S-SSHI interface circuit. The interface circuit comprises a switch, an inductor in series with the PZT for voltage inversion, and an FBR. When the voltage across the PZT (V_{PZT}) reaches its positive or negative peak, the switch turns ON, enabling charge transfer from the PZT to the storage capacitor C_r. During this

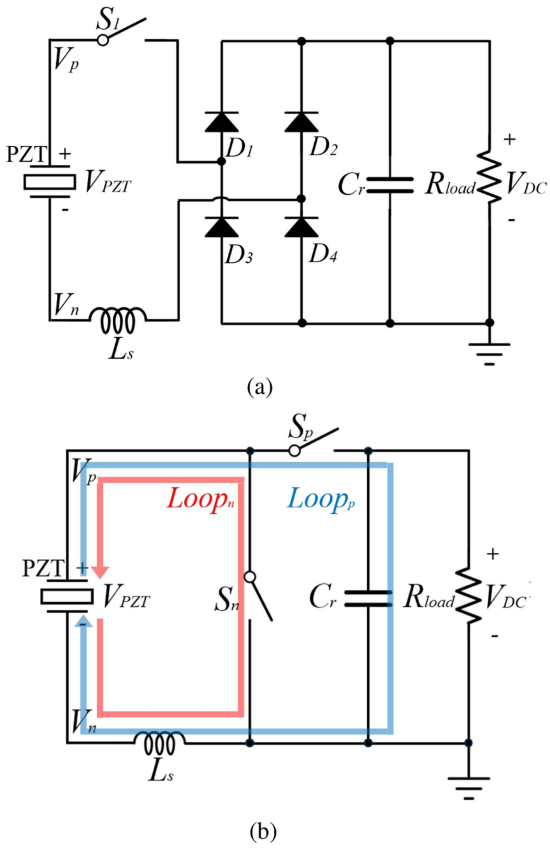

Fig. 3. Topology of the prior-art circuits. (a) S-SSHI. (b) ReL-SSHI. [36].

process, the capacitors C_r and C_p form an *LC* resonant loop with the inductor L_s. After half of the *LC* resonance period, the voltage across the PZT is inverted, and the switch S_1 is turned OFF. The voltage drop across the switch and the equivalent series resistance (ESR) of the inductor will both cause energy losses. In addition, while transferring energy to the storage capacitor, the charges must pass through two diodes in the FBR, resulting in additional energy losses.

To mitigate the diode-induced losses, Wang et al. [36] introduced a ReL-SSHI circuit. As depicted in Fig. 3(b), the ReL-SSHI employs two switches (S_p and S_n) and a single inductor L_s, along with the storage capacitor C_r and a load resistor R_{load}. When V_{PZT} reaches a positive peak, S_p is activated, creating an *LC* loop with C_r, C_p, and L_s to transfer energy onto C_r. After half of the *LC* resonance period, V_{PZT} is inverted and S_p is turned OFF. During the negative half-cycle, when V_{PZT} reaches its negative peak, S_n is switched ON, forming a loop with C_p and L_s only. As a result, during the negative half-cycle, energy is stored in C_p rather than being transferred to the storage capacitor C_r. Although the ReL-SSHI successfully eliminates diode-induced conduction losses, it harvests energy to C_r only during the positive half-cycles. This limitation effectively reduces the overall energy extraction capability of the circuit compared to designs that enable EH during both positive and negative half-cycles.

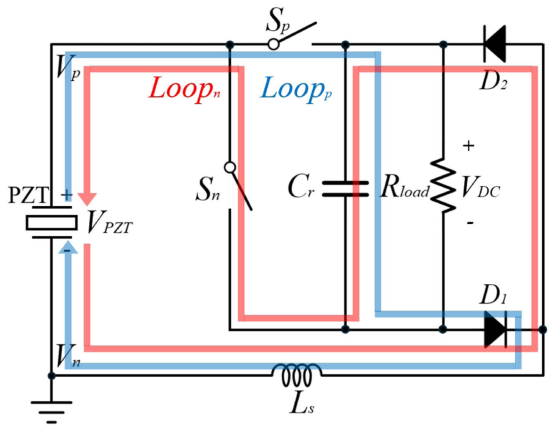

Fig. 4. Topological structure of the proposed circuit: BiReL-SSHI.

B. Proposed BiReL-SSHI

The topology of the proposed BiReL-SSHI circuit is shown in Fig. 4. It consists of switches S_p and S_n, an inductor L_s, and two diodes D_1 and D_2. Switches S_p and S_n turn ON at the positive and negative peaks of V_{PZT}, respectively, allowing charge to transfer onto the storage capacitor C_r. The diodes D_1 and D_2 ensure that the current flows through C_r in only one direction. After each half-cycle of charge transfer, the inductor L_s inverts V_{PZT}, and the switch is then turned OFF until the next peak. In contrast to the conventional series SSHI circuit, the BiReL-SSHI eliminates the FBR, thereby reducing the number of diodes in the conduction path and enhancing overall energy extraction efficiency. Furthermore, compared to the ReL-SSHI topology, which only harvests energy during the positive half-cycles, the BiReL-SSHI extracts energy in both the positive and negative half-cycles. This dual-polarity energy harvesting enables greater energy collection per cycle, particularly when operating at low output voltages, and shifts the MPP to a lower output voltage level. Consequently, the BiReL-SSHI circuit is better suited than the ReL-SSHI for high-power applications where lower output voltages are desired.

The harvesting efficiency depends strongly on the chosen inductor since it affects both the inversion factor and the energy loss to the inductor's ESR. The inversion factor of the *LC* loop can be expressed as

$$\gamma = e^{\frac{-\pi}{2Q}} \tag{1}$$

where Q is the quality factor of the *LC* loop.

Following the description in [23], the voltages $V''_{n,\text{org}}$, $V''_{p,\text{org}}$, $V''_{n,\text{max}}$, and $V''_{p,\text{max}}$ in the BiReL-SSHI (see Fig. 5) are related as

$$-V''_{n,\text{org}} + V_{\text{DC}} = \gamma(V''_{p,\text{max}} - V_{\text{DC}}) \tag{2}$$

$$V''_{p,\text{org}} + V_{\text{DC}} = \gamma(-V''_{n,\text{max}} - V_{\text{DC}}). \tag{3}$$

Here, V_{DC} is the voltage across the output capacitor C_r. Between two voltage inversions, the voltages $V''_{p,\text{max}}$ and $V''_{n,\text{org}}$ satisfy

$$V''_{p,\text{max}} - V''_{p,\text{org}} = -V''_{n,\text{max}} + V''_{n,\text{org}} = \frac{2\alpha U_M}{C_p} \tag{4}$$

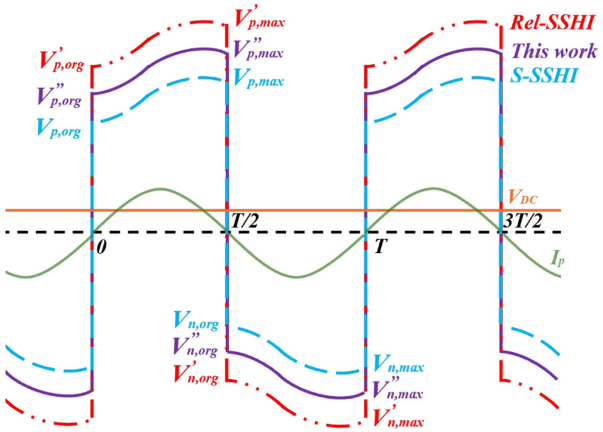

Fig. 5. Open circuit voltage of the PZT in conventional S-SSHI, ReL-SSHI, and BiReL-SSHI.

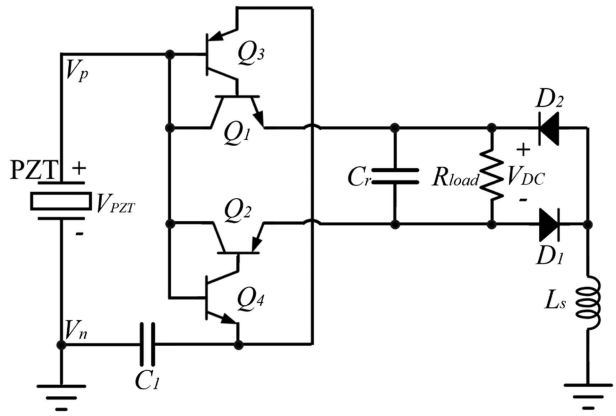

Fig. 6. Schematic of BiReL-SSHI circuit.

where α and U_M represent the PE force-to-voltage conversion factor and displacement amplitude of the PZT, respectively.

The energy delivered to the load during one half-cycle is equal to the energy dissipated by the load resistance. Thus

$$E = \int_0^{T_{LC}/2} V_{\rm DC} \cdot I_{Ls}\, dt$$

$$= V_{\rm DC} C_p (V''_{p,\max} - V''_{n,\rm org}) = \frac{V_{\rm DC}^2}{2 f R_{\rm load}} \tag{5}$$

where f is the vibration frequency of the PZT. $V_{\rm DC}$ can then be expressed as

$$V_{\rm DC} = \frac{2\alpha U_M R_{\rm load}\omega(1+\gamma)}{\pi(1-\gamma) + 2R_{\rm load} C_p \omega(1+\gamma)} \tag{6}$$

where $\omega{=}2\pi f$. It is fair to assume that the displacement amplitude U_M is a constant. In that case, the average power and maximum power can be expressed as

$$P_{\rm avg} = \frac{V_{\rm DC}^2}{R_{\rm load}} \tag{7}$$

$$P_{\max} = \frac{f\alpha^2 U_M^2}{C_p}\frac{1+\gamma}{1-\gamma}. \tag{8}$$

The power reaches $P_{\max}$ for an optimal load resistance that is

$$R_{\rm opt} = \frac{1}{4 f C_p}\frac{1-\gamma}{1+\gamma}. \tag{9}$$

The optimum $V_{\rm DC}$ is found to be

$$V_{\rm DC,opt} = \frac{V_{\rm OC,org}}{2} - V_D \tag{10}$$

where $V_{\rm OC,org}$ is the original open-circuit voltage of the PZT and V_D is the voltage drop due to the single diode in the charge transfer path. For the series SSHI topology, according to [23], all the optimum points are the same as calculated above, except for the $V_{\rm DC,opt}$, which lies at

$$V_{\rm DC,opt} = \frac{V_{\rm OC,org}}{2} - 2V_D \tag{11}$$

because of two diodes in the charge transfer path when using an FBR. From [36] it is known that for the ReL-SSHI, the optimum points are

$$P_{\max} = \frac{f\alpha^2 U_M^2}{C_p}\frac{(1+\gamma_p)(1+\gamma_s)}{(1-\gamma_p\gamma_s)} \tag{12}$$

$$R_{\rm opt} = \frac{1-\gamma_s\gamma_p}{f C_p (1+\gamma_p)(1+\gamma_s)} \tag{13}$$

$$V_{\rm DC,opt} = V_{\rm OC,org}. \tag{14}$$

Here, γ_p and γ_s are the inversion factors for the ReL-SSHI circuit in the positive and negative half-cycles, respectively.

From these equations, it becomes evident that for the series SSHI, the minimum $V_{\rm OC,org}$ to reach the MPP is $4V_D$, while for the ReL-SSHI it is 0, and for the proposed BiReL-SSHI circuit it is $2V_D$. Note that the inversion factors used here do not include the effect of diode drops inside the *LC* loop, resulting in slightly optimistic theoretical optimum points.

III. Implementation of BiReL-SSHI Circuit

This section provides a detailed discussion on the implementation of the proposed BiReL-SSHI circuit, which is shown in Fig. 6. In addition to the PZT, it includes a synchronous switch composed of two negative-positive-negative transistor (NPN) transistors Q_1 and Q_4, two positive-negative-positive transistor (PNP) transistors Q_2 and Q_3, a peak-detecting capacitor C_1, an inductor L_s, and two diodes D_1–D_2, the storage capacitor C_r, and the load resistor $R_{\rm load}$.

The operating principle of the proposed circuit is described as follows. Assume that the voltage drop across the base–emitter junction of the transistors is $V_{\rm be}$. During the positive half-cycle ($V_p > V_n$), the PE harvester charges the capacitor C_1 through the base–emitter junction of transistor Q_4 as the PE voltage V_p increases. When V_p reaches its positive maximum $V_{p,\max}$, the voltage across C_1 becomes $V_{p,\max} - V_{\rm be}$. As V_p begins to decrease, the base–emitter junction of Q_4 becomes reverse-biased. When V_p decreases to $V_{p,\max} - 2V_{\rm be}$, the emitter-base junction of Q_3 becomes forward-biased, allowing its emitter–collector path to conduct. Consequently, the voltage on C_1

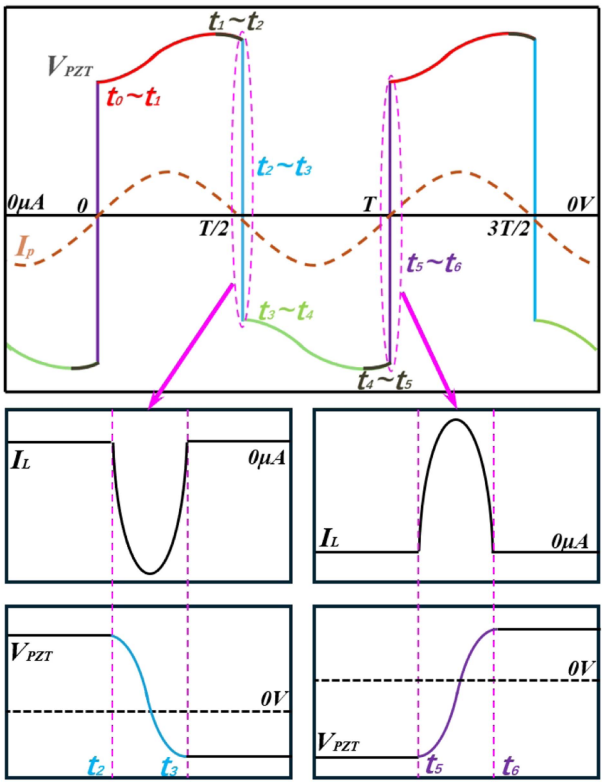

Fig. 7. Typical waveforms of the BiReL-SSHI circuit.

TABLE I
DEVICES USED IN STATE-OF-THE-ART CIRCUITS

	[45]	[46]	[32]	[13]	[39]	[17]	[47]	this work
Transistors	4	4	4	8	4	8	8	4
MOSFETs	2	0	0	0	0	1	0	0
Capacitors	2	2	2	2	1	2	2	1
Inductors	1	1	1	1	2	1	1	1
Diodes	7	4	12	0	4	1	0	2
Resistors	2	0	4	0	0	0	0	0

is applied to the base of transistor Q_1, turning it ON. As a result, an *LC* resonant loop is established, consisting of C_p, the emitter–collector path of Q_1, C_r, diode D_1, and inductor L_s. In this loop, C_p initially charges L_s and C_r, causing the inductor current I_L to rise to its peak. Subsequently, L_s discharges its stored energy back into C_r and C_p until I_L falls to zero, as illustrated in Fig. 7. The duration of a single SSHI operation is approximately half of the *LC* resonant period. The operation in the negative half-cycle ($V_p < V_n$) follows a similar sequence.

Table I compares the devices used in some state-of-the-art interface circuits with those required by this work. The proposed circuit employs the smallest number of components. To better understand the operation of the circuit, one full cycle is divided into six phases, with four key phases, as illustrated in Fig. 8.

A. First Natural Charging Phase ($t_0 < t < t_1$)

During this phase, the current source I_p charges C_p and, through the base–emitter junction of transistor Q_4, also charges C_1. The voltage on PZT can be calculated as

$$V_{\mathrm{PZT}}(t) = V_{\mathrm{PZT},t_0} + \frac{\int_{t_0}^{t} I_p dt}{C_p + C_1}. \tag{15}$$

Because the mechanical vibrations are sinusoidal, we have

$$I_p = A\sin(\omega t). \tag{16}$$

At $t = T/2$, where T is the period of the sinusoid, and just before I_P changes direction, V_{PZT} reaches its maximum

$$\begin{aligned} V_{\mathrm{PZT,max}} &= V_{\mathrm{PZT},t_0} + \frac{\int_{t_0}^{T/2} I_p\, dt}{C_p + C_1} \\ &= V_{\mathrm{PZT},t_0} + \frac{2A}{\omega(C_p + C_1)}. \end{aligned} \tag{17}$$

At the same instant, the voltage across C_1 is

$$V_{C1,\mathrm{max}} = V_{\mathrm{PZT,max}} - V_{\mathrm{be}} \tag{18}$$

where V_{be} is the base–emitter junction voltage of transistor Q_4. Evidently, the peak detecting capacitor causes some energy loss simply by being parallelly charged along with the capacitor C_p, causing C_p to reach a slightly lower peak voltage $V_{\mathrm{PZT,max}}$ and the energy lost due to this can be expressed as

$$\begin{aligned} E_{\mathrm{lost}} = &\frac{1}{2}C_p\left(V_{\mathrm{PZT},t_0} + \frac{2A}{\omega C_p}\right)^2 \\ &- \frac{1}{2}C_p\left(V_{\mathrm{PZT},t_0} + \frac{2A}{\omega(C_p + C_1)}\right)^2. \end{aligned} \tag{19}$$

To reduce this loss, C_1 should be as small as possible; however, it must satisfy

$$C_1 > \frac{1}{\beta}C_P \tag{20}$$

where β is the current gain of the transistors in the synchronous switch. Choosing C_1 too small can lead to incorrect switching behavior.

B. First Current Reversion Phase ($t_1 < t < t_2$)

After time t_1, the current reverses direction, causing C_p to begin discharging. The voltage across C_1 remains at $V_{C_1,\mathrm{max}}$ as given by (18), since it has no discharge path. As V_{PZT} falls, transistor Q_4 turns OFF when $V_{\mathrm{PZT}} = V_{C_1,\mathrm{max}}$. V_{PZT} continues to decrease, and at t_2 it equals $V_{C_1,\mathrm{max}} - V_{\mathrm{be}}$, triggering transistor Q_3 to turn ON. The phase lag between the voltage peak and the switching event is

$$\theta = \cos^{-1}\left(\frac{V_{\mathrm{PZT,max}} - 2V_{\mathrm{be}}}{V_{\mathrm{PZT,max}}}\right). \tag{21}$$

C. First Voltage Inversion Phase ($t_2 < t < t_3$)

When Q_3 turns ON, transistor Q_1 also activates, forming an *LC* resonant loop with C_p, C_r, and L_s. After half an *LC* period, charge is transferred from C_p onto C_r, while the inductor inverts V_{PZT}. The relationship between V_{PZT} at t_2 and t_3 is

$$V_{\mathrm{PZT},t_3} + (V_{\mathrm{DC}} + V_{ce} + V_D) = \gamma[V_{\mathrm{PZT},t_2} - (V_{\mathrm{DC}} + V_{ce} + V_D)] \tag{22}$$

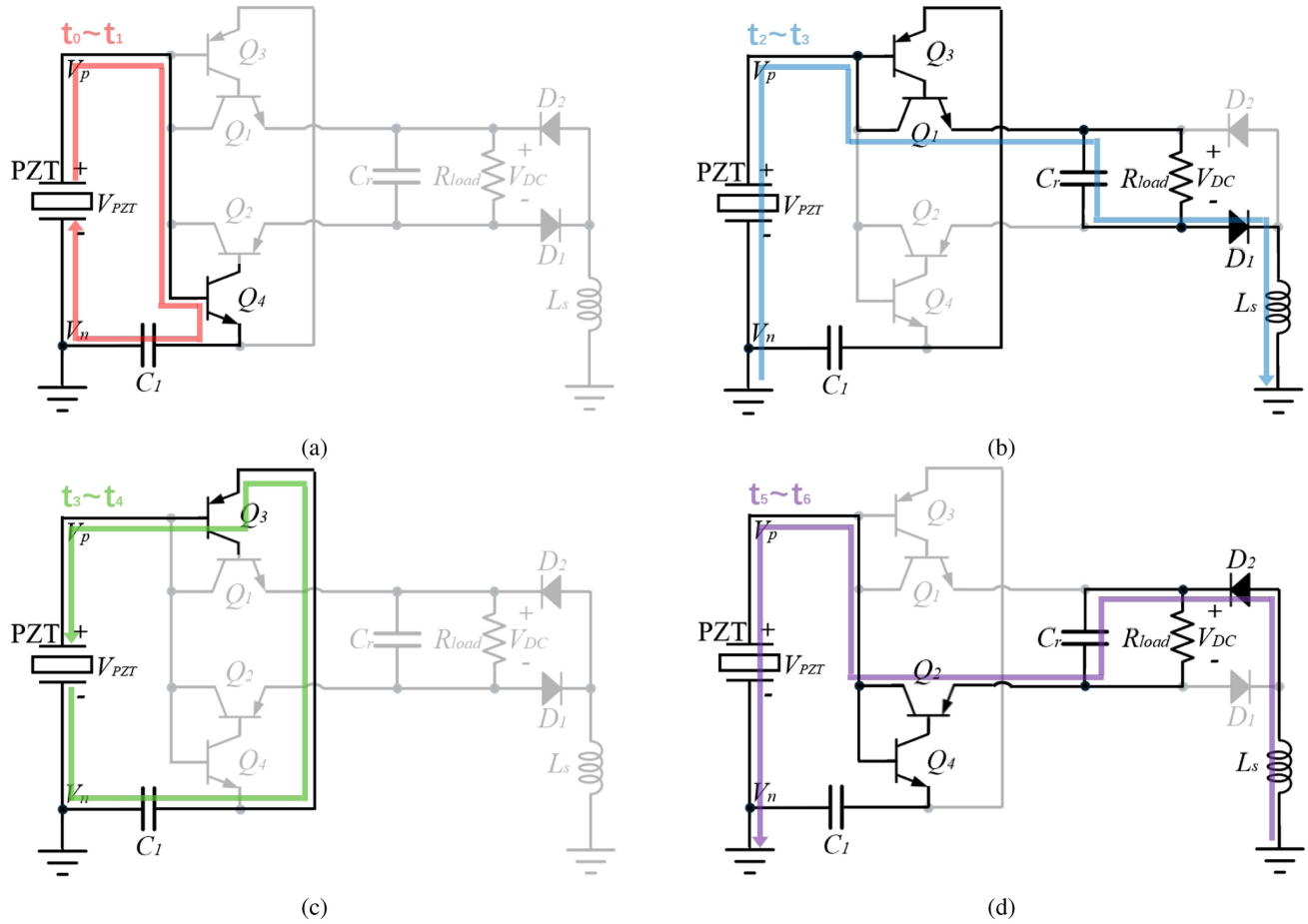

Fig. 8. Direction of current flow in the four phases. (a) First natural charging ($t_0 < t < t_1$). (b) First voltage inversion ($t_2 < t < t_3$). (c) Second natural charging ($t_3 < t < t_4$). (d) Second voltage inversion ($t_5 < t < t_6$).

where V_{ce} is the voltage drop across Q_1, V_D is the diode drop across D_1, and γ is the inversion factor as defined in (1).

During this phase, some energy is lost due to the Q_1 junction drop, the diode D_1 drop, and the ESR of L_s. This can be expressed as

$$E_{\text{lost}} = \int_0^{\pi\sqrt{LC}} [(V_{ce} + V_D)I_L + R_{\text{ESR}} I_L^2]dt \qquad (23)$$

where I_L is the current flowing through inductor L_s. Fig. 7 shows the current pulse through L_s and the resulting voltage inversion of V_{PZT}.

D. Second Natural Charging Phase ($t_3 < t < t_4$)

Similar to the first natural charging phase, C_p and C_1 charge again, but in the opposite polarity, while Q_3 remains ON. The voltage across C_1 now follows V_{PZT} at a voltage V_{eb} above it, due to the emitter–base junction of Q_3.

E. Second Current Reversion Phase ($t_4 < t < t_5$)

As the second natural charging phase ends, I_p changes direction, and V_{PZT} reaches its minimum. Since C_1 has no discharge path, its voltage remains constant while V_{PZT} begins to rise. First, Q_3 turns OFF. When V_{PZT} surpasses V_{C_1} by V_{be}, Q_2 and Q_4 turn ON, and the circuit operates similarly to the first current reversion phase.

F. Second Voltage Inversion Phase ($t_5 < t < t_6$)

When Q_2 turns ON at t_5, the *LC* resonant loop of C_p, C_r, and L_s forms again. Energy is transferred onto the load, and V_{PZT} is inverted in the same manner as during the first voltage inversion phase. According to [36], the ReL-SSHI does not transfer energy to the load in the negative half-cycle, performing only inversion. In contrast, the BiReL-SSHI can transfer energy in both halves of the cycle, thereby extracting more power over each full cycle.

IV. Simulation Analysis

The interface circuit shown in Fig. 6 was implemented in linear technology simulation program with integrated circuit emphasis (LTSpice) to validate the theoretical analysis. The simulation parameters were set as follows: $f = 31$ Hz, $I_P = 38\ \mu$A, $C_P = 22$ nF, $C_1 = 470$ pF, $C_r = 10\ \mu$F, and $L_s = 47$ mH with an ESR of $R_{\text{ESR}} = 100\ \Omega$.

A. Simulation Results

Fig. 9 presents the transient waveforms of the PZT voltage V_{PZT}, the storage capacitor voltage V_{DC} and the instantaneous

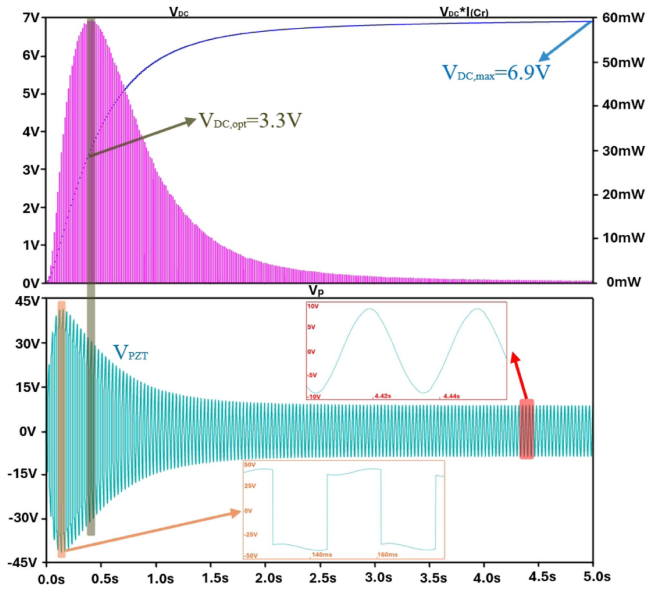

Fig. 9. Transient waveforms from the simulation analysis.

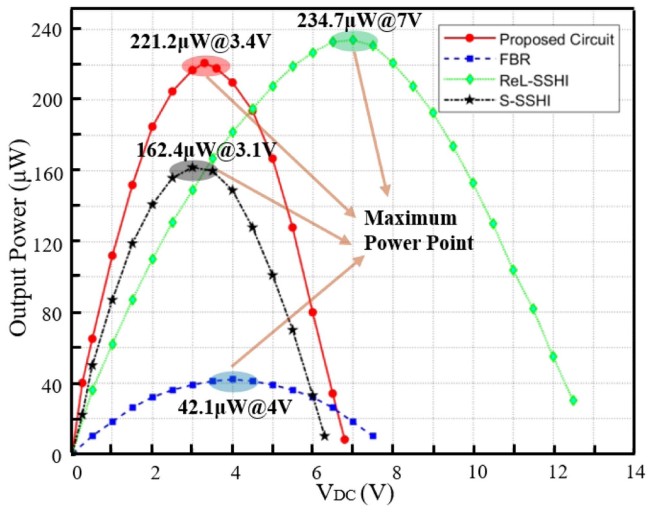

Fig. 10. Comparison of simulated Power versus V_{DC} between the proposed BiReL-SSHI circuit and prior designs, including FBR, S-SSHI, and ReL-SSHI.

power transfer pulses on storage capacitor $I_{C_r} \times V_{\mathrm{DC}}$. It should be noted that the value of power transfer pulses does not represent the actual output power of the BiReL-SSHI, but it can be used to find the MPP. The V_{PZT} waveform resembles that of a conventional S-SSHI and is symmetric about the x-axis. Furthermore, the proposed BiReL-SSHI enables power transfer to C_r twice per cycle, unlike the single transfer per cycle in the ReL-SSHI circuit. As seen in this figure, the initially increasing V_{PZT} and power transfer gradually stabilize as V_{DC} converges to a steady level. The MPP corresponds to the condition where the power transfer pulse reaches its maximum value, and the optimal V_{DC} derived from the simulation closely aligns with the theoretical prediction given by (10).

In Fig. 10, the proposed BiReL-SSHI circuit's performance was compared against other common interface circuits, with their respective output power veresus V_{DC} characteristics under the same vibration conditions ($V_{\mathrm{oc}} = 8V$). Despite using the same peak detector and inductor, the BiReL-SSHI extracts more power in each cycle. The output voltage at the MPP for the conventional SSHI and FBR circuits is comparable to that of the BiReL-SSHI, while the ReL-SSHI from [36] achieves its MPP at approximately twice the output voltage, in line with theoretical expectations derived from (11) and (14). Although the maximum power of the BiReL-SSHI is slightly lower than that of the ReL-SSHI, attributable to the additional voltage drops introduced by the two diodes, the BiReL-SSHI benefits from dual half-cycle EH and a reduced MPP output voltage, enabling it to deliver superior performance at lower output voltages. Specifically, as shown in Fig. 10, the BiReL-SSHI achieves the highest output power among the four circuits when V_{DC} is below 4.5 V. Therefore, for applications requiring maximum power extraction at lower output voltage levels, without altering the vibration conditions, the BiReL-SSHI presents the most advantageous solution.

B. Loss Analysis

As established in Section III, the power losses in the BiReL-SSHI circuit during each PZT voltage inversion cycle originate from two primary sources: 1) switching delay caused by the peak-detecting capacitor, and 2) losses in the nonideal *LC* resonant loop, including the effects of diodes, transistors, and the ESR of the inductor. Based on the simulated waveforms of V_{PZT} and V_{DC}, as shown in Fig. 9, these losses can be quantitatively estimated. Let V_p denote the peak value (positive or negative) of V_{PZT} in a given inversion cycle. Define V_1 and V_{r_1} as the values of V_{PZT} and V_{DC} before flipping, and V_2 and V_{r_2} as their values after flipping. The power loss due to switching delay in each voltage inversion cycle (with period $T/2$) can then be calculated as

$$P_{\mathrm{loss},sd} = fC_p(V_p^2 - V_1^2). \tag{24}$$

The power loss associated with the nonideal *LC* resonant loop during each voltage inversion cycle is given by

$$P_{\mathrm{loss},LC} = fC_p(V_1^2 - V_2^2) - fC_r(V_{r_2}^2 - V_{r_1}^2). \tag{25}$$

Substituting the simulation data into (24) and (25) reveals that energy loss varies across voltage inversion cycles, following the trend of V_{PZT}. Initially, as the amplitude of V_{PZT} increases, energy loss per cycle also increases. When the peak value of V_{PZT} is relatively high, the loss is dominated by $P_{\mathrm{loss,\,LC}}$. The maximum observed total power loss is approximately 220μW, of which $P_{\mathrm{loss,LC}}$ contributes about 180μW. This peak occurs during the inversion cycle when V_{PZT} reaches its maximum of approximately 38 V. As the peak of V_{PZT} decreases, the total power loss gradually declines. When V_{PZT} drops to approximately 27 V, V_{DC} reaches its optimal value $V_{\mathrm{DC,opt}}$. At this point, as shown in Fig. 10, the circuit achieves its maximum output power of 221.2 μW, with a corresponding power loss of around 125 μW. As V_{PZT} continues to decline toward 9 V,

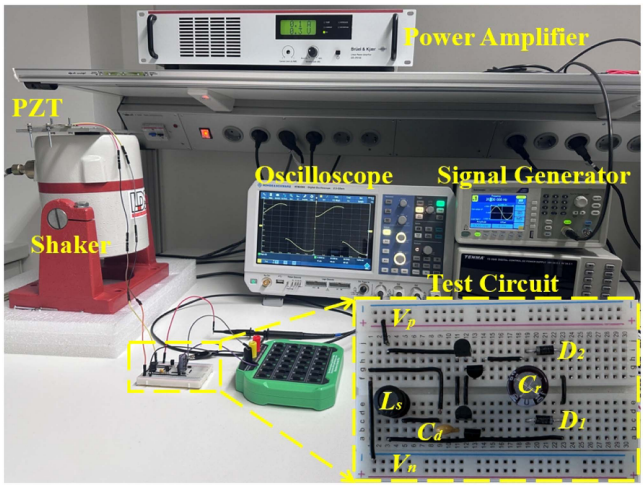

Fig. 11. Experimental Setup.

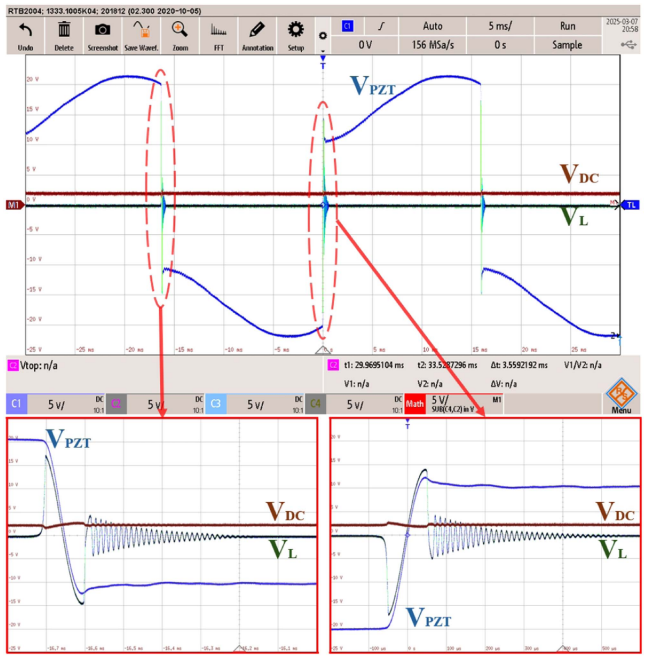

Fig. 12. Waveforms captured during the experiment.

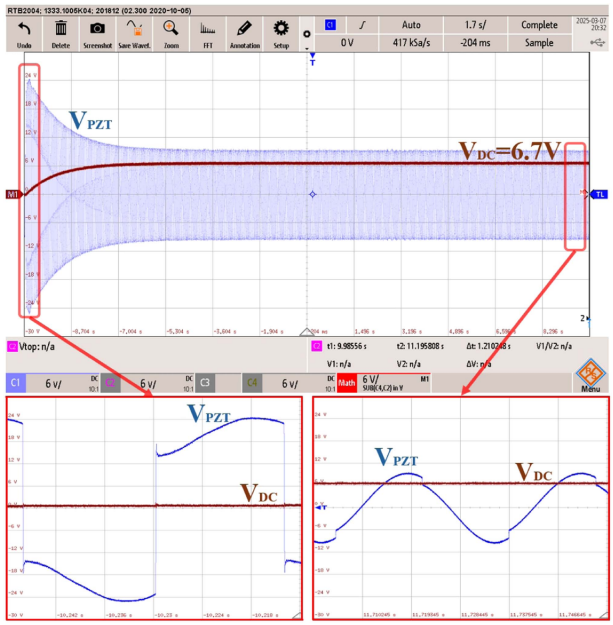

Fig. 13. V_{PZT} waveform captured during the experiment.

the total energy loss further decreases. The minimum loss is approximately 10 μW, which is primarily attributed to $P_{\mathrm{loss,sd}}$. At this stage, negligible energy is transferred to C_r and minimal current flows through inductor L_s, rendering $P_{\mathrm{loss,\,LC}}$ almost insignificant. When power loss is high, the dominant contributor is the ESR of the inductor, as it increases with the square of the inductor current I_L, in accordance with the theoretical relationship in (23). Conversely, under low-power-loss conditions, the peak-detecting capacitor becomes the primary source of energy dissipation, making $P_{\mathrm{loss,sd}}$ the most significant factor limiting efficiency.

V. Measurement Results

An experimental platform, as shown in Fig. 11, was set up to validate the simulation results. The equipments included a signal generator, a power amplifier, a shaker, the PZT, an oscilloscope, and the proposed BiReL-SSHI interface circuit. The PZT used is the MIDE PPA-1021, which has a parasitic capacitance of 22 nF, and one end of the PZT is attached to the shaker. The signal generator controls the vibration frequency of the shaker (and thus the PZT), while the power amplifier provides adjustable driving capability and vibration amplitude. The BiReL-SSHI circuit is implemented using 2N3906 and 2N3904 transistors (for PNP and NPN, respectively) that form the synchronous switch, along with 1N4148 diodes, a 10-μF electrolytic storage capacitor C_r, and a Bourns RLB0913 inductor (47 mH, internal resistance of 99 Ω ESR).

With the power amplifier settings fixed, the resonant frequency of the PZT was determined by tuning the function generator until the maximum open-circuit voltage appeared across the PZT. This frequency was approximately 31 Hz. Connecting the interface circuit to the transducer shifted the resonant frequency to about 31.1 Hz due to the loading effect.

Fig. 12 shows the experimentally transient waveforms of V_{PZT}, V_{DC} and V_L, where V_L is the voltage across the inductor L_s. As anticipated, during the positive half-cycle, V_{PZT} exhibits a voltage drop of approximately $2V_{\mathrm{be}}$ from its peak before inversion due to the base–emitter junctions of transistors Q_4 and Q_3. When V_{PZT} begins to invert, the inductor L_s is engaged, driving the voltage inversion through *LC* resonance. Similarly, during the negative half-cycle, once V_{PZT} rises by approximately $2V_{\mathrm{be}}$ from its negative peak, the inductor again forms part of the resonant loop to invert the voltage. These experimental results confirm the expected circuit operation, validating the self-powered switching and bipolar energy transfer mechanisms of the proposed BiReL-SSHI.

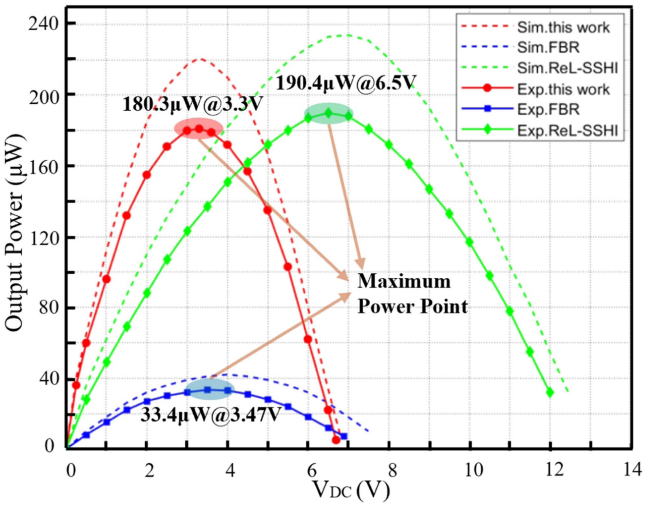

Fig. 14. Power versus V_{DC} for FBR, ReL-SSHI, and the proposed BiReL-SSHI circuit when $V_{\mathrm{oc}} = 8\ V$. (Sim: Simulation and Exp: Experimental).

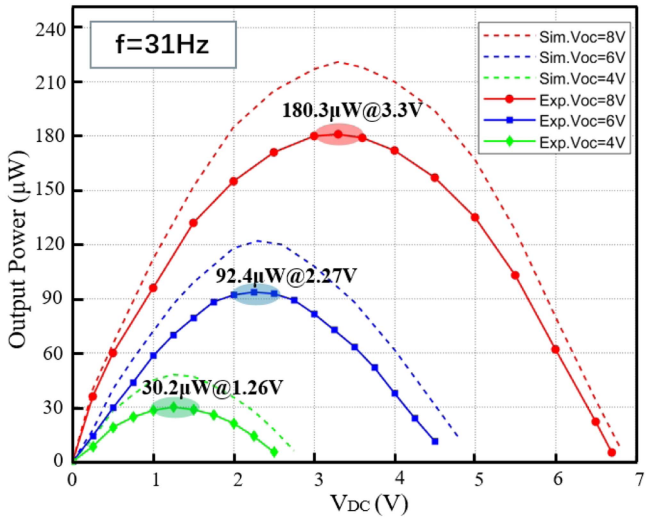

Fig. 15. Power versus V_{DC} for the BiReL-SSHI at different V_{oc}.

Fig. 13 presents the experimentally measured V_{PZT} waveform versus V_{DC}. Similar to the simulation results, the voltage initially rises sharply and then settles near the original open-circuit level as C_r charges. Because increasing V_{DC} reduces the current through the inductor, the flipping magnitude decreases, altering the waveform shape. The two zoomed-in views in Fig. 13 illustrate the V_{PZT} waveforms at the initial startup and after V_{DC} has reached its steady-state value.

Fig. 14 compares the experimental and simulated performances of the FBR, ReL-SSHI, and the proposed BiReL-SSHI circuit under an open-circuit voltage (V_{oc}) of 8 V. All three circuits utilize the same 10 μF load capacitor, and the ReL-SSHI employs the same peak detector as the proposed BiReL-SSHI for fair comparison. Consistent with the simulation results, the BiReL-SSHI achieves approximately half the output voltage at the MPP compared to the ReL-SSHI, while delivering the highest performance at lower output voltages. These results experimentally verify the BiReL-SSHI's capability to achieve high power extraction at reduced output voltage levels.

Fig. 15 presents the measured output power of the BiReL-SSHI circuit operating at its resonance frequency under varying vibration amplitudes. The experimental results closely follow the trends observed in simulation. The differences between the experimental and simulation results primarily arise from additional losses present in the physical circuit. Specifically, the simulation considers only the loss due to the inductor's ESR, whereas the experimental circuit also includes losses from transistors and capacitors, which degrade the flipping efficiency in the *LC* resonance loop. Moreover, component mismatches in the physical *LC* network, which are idealized in simulation, further impact flipping efficiency. As the vibration amplitude increases, raising the open-circuit voltage from 4 to 8 V, both the MPP and the operable voltage range expand proportionally. It can be observed that the MPP and operable range scale roughly with V_{oc}, while the maximum harvested power increases approximately with the square of V_{oc}. In addition, the power extraction efficiency of the circuit can be modestly improved by replacing the 1N4148 diodes with Schottky diodes, such as the 1N5817, which feature lower forward voltage drops and therefore reduce energy losses.

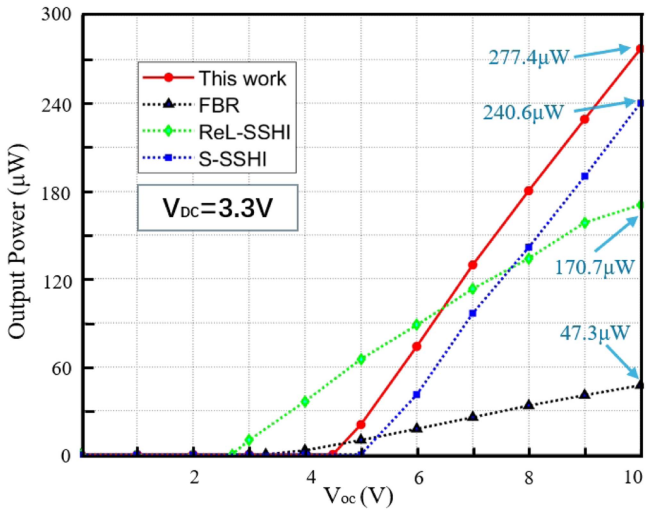

Fig. 16. Power versus V_{oc} for BiReL-SSHI, FBR, S-SSHI, and ReL-SSHI circuits when $V_{\mathrm{DC}} = 3.3$ V.

Fig. 16 illustrates the output power of four interface circuits under varying vibration amplitudes, with the output voltage V_{DC} maintained at 3.3 V. The output power curves of all four circuits scale proportionally with the open-circuit voltage V_{oc}, with the BiReL-SSHI exhibiting the steepest slope. While the BiReL-SSHI requires a slightly higher V_{oc} to achieve power delivery at $V_{\mathrm{DC}} = 3.3$ V, due to differences in control strategies and flipping mechanisms, it surpasses the output power of the FBR and ReL-SSHI circuits once V_{oc} exceeds 4.5 and 6.5 V, respectively. Beyond this point, the BiReL-SSHI consistently delivers the highest output power among the compared circuits. For example, at $V_{\mathrm{oc}} = 10$ V, the BiReL-SSHI achieves an output

TABLE II
PERFORMANCE COMPARISON

Circuit	TCAS2018 [35]	TPEL2019 [48]	JSSC2020 [49]	TPEL2021 [36]	TPEL2022 [50]	TPEL2024 [37]	TPEL2024 [51]	This work
PZT	YiBoP8-1	PZT-5A	PPA-1021	PPA-1014	PPA-2011	PPA-2011	PZT-5H	PPA-1021
C_P (nF)	220	28.42	22	41	190	190	80	22
Technology	0.18 μm CMOS	Discrete	0.18 μmCMOS	Discrete	Discrete	Discrete	Discrete	Discrete
Scheme Type	SECE	P-S3BF	SPFCR	ReL-SSHI	P-SSHI	ReL-SECE	S-SSHI	BiReL-SSHI
Self Powered	YES	NO	NO	YES	YES	YES	YES	YES
Require Rectifier	NO	YES	YES	NO	NO	NO	NO	NO
Inductor (mH)	1	47	N/A	50	1.56	4.7	10	47
Bipolar	YES	YES	YES	NO	YES	YES	NO	YES
$P_{out,max}/P_{FBR,max}$	3.56	3.88	9.3	5.9	3.22	4.2	4.8	5.4
V_{MPPT}/V_{oc}	N/A	0.2	>2	0.81	>2	>2	≈ 1	0.41
Frequency (Hz)	42	24.9	200	18.6	77.5	19	30.5	31
$V_{oc,org}(V)$	1.5-5V	15	1.4	4-8	3.9-5.8	2-6	4-7	4-8
Circuit complexity	Complicated	Moderate	Complicated	Simple	Moderate	Simple	Moderate	Simple

SPFCR: split-phase flipping-capacitor rectifier

power 5.86× higher than that of the FBR and 62.5% higher than that of the ReL-SSHI. As $V_{\rm oc}$ increases further, this performance advantage becomes even more pronounced. Consequently, for applications requiring high output power at low supply voltages, such as common chip supply levels of 3.3 or 1.5 V, the BiReL-SSHI emerges as the most suitable interface circuit.

Table II summarizes a performance comparison between the proposed BiReL-SSHI and several state-of-the-art interface circuits. The designs reported in [35], [36], [37], [50], and [51] are based on established SECE, S-SSHI, and P-SSHI topologies, and all are self-powered. In contrast, the P-S3BF circuit in [48] requires an external power supply due to its complex control scheme. In addition, the circuit in [49] relies on precharged energy for startup, and its passive self-starting circuit imposes performance penalties. The BiReL-SSHI achieves a higher $P_{\rm out,max}/P_{\rm FBR,max}$ ratio than most circuits in the comparison, with the exceptions of [36] and [49]. While Chen et al. [49] achieved high EH efficiency using capacitors instead of inductors, its circuit complexity is significantly higher. The ReL-SSHI in [36] exhibits slightly better harvesting efficiency than the BiReL-SSHI but operates at nearly double the $V_{\rm MPPT}/V_{\rm oc}$ ratio, indicating that under identical vibration conditions, the BiReL-SSHI reaches its MPP at a much lower output voltage. Although the circuit in [48] demonstrates an even lower $V_{\rm MPPT}/V_{\rm oc}$, it cannot self-start and requires a rectifier, which severely compromises its power efficiency. The SECE circuit reported in [35] mitigates phase lag using additional envelope detection modules and maintains relatively high efficiency across a wide load range. Meanwhile, the design in [37] offers good load adaptability but suffers from lower harvesting efficiency and an excessively high operating open-circuit voltage $V_{\rm oc,org}$. Overall, the BiReL-SSHI offers an advantageous balance of high efficiency, low operating voltage, and self-powered operation, making it a highly competitive choice among current state-of-the-art interface circuits.

VI. CONCLUSION

In this article, a novel BiReL-SSHI interface circuit for PEH has been proposed and demonstrated. Compared to the conventional S-SSHI topology, the BiReL-SSHI employs a minimal number of components while achieving higher output power. Furthermore, in contrast with the ReL-SSHI circuit, the BiReL-SSHI achieves a comparable MPP under the same vibration conditions but at approximately half the output voltage, making it particularly suitable for low-voltage applications. In comparison with state-of-the-art interface circuits, the BiReL-SSHI delivers the highest output power at an output voltage of 3.3 V, with this advantage becoming increasingly prominent as the open-circuit voltage of the PZT rises. Both simulation and experimental results confirm that the BiReL-SSHI provides superior EH efficiency, establishing it as a highly effective solution for low-voltage, high-efficiency EH applications.

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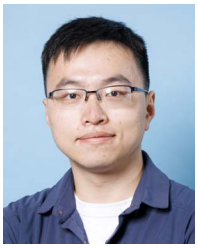
Zijun Qiu received the B.Sc. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2020. He is currently working toward the M.Sc. degree in electrical engineering with the Electronic Instrumentation Laboratory, the Department of Microelectronics, Delft University of Technology, Delft, The Netherlands.

From 2020 to 2023, he was an Electrical Engineer in Shanghai, China. His current research interests include energy harvesting and power management circuits.

Sreedharan Maniyil received the B.Tech. degree in electronics and communications engineering from Amrita Vishwavidyapeetham, Coimbatore, India, in 2020, and the M.Sc. degree in electrical engineering with the Electronic Instrumentation Laboratory, the Department of Microelectronics, Delft University of Technology, Delft, The Netherlands, 2024.

From 2020 to 2022, he worked in Chennai, India. His research interests include power management circuits and analog/mixed signal circuit design.



Wenyu Peng (Graduate Student Member, IEEE) received the B.Sc. degree from Glasgow College, the University of Electronic Science and Technology of China, Chengdu, China, in 2020, and the M.Sc. degree in electronic instrumentation section from the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, in 2023. He is currently working toward the Ph.D. degree in the Department of Microelectronics with the Delft University of Technology (TU Delft), Delft, The Netherlands.

His current research is on triboelectric and multisource energy harvesting for wearable, biomedical, and Internet-of-Things (IoT) autonomous sensors, including energy-efficient power management circuit designs, and front-end harvester fabrications.

André C. van der Ham was born in the Netherlands. He received the Ph.D. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1997.

In 2000, he joined SKF, where he has contributed to various developments in electronics for condition monitoring of bearings. Since 2010, energy harvesting has been an important aspect of his work, as part of the broader effort to enable continuous monitoring using integrated electronics. His research focuses on system optimization, with a particular focus on power management to maximize overall performance.

Sijun Du (Senior Member, IEEE) received the B.Eng. degree (with Hons.) in electrical engineering from the University Pierre and Marie Curie (UPMC), Paris, France, in 2011, the M.Sc. degree (with distinction) in electrical and electronic engineering from Imperial College, London, U.K., in 2012, and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in 2018.

He was with the Laboratoire d'Informatique de Paris 6 (LIP6), UPMC, and then was an IC Engineer in Shanghai, China, between 2012 and 2014. He was a summer Engineer Intern with Qualcomm Technology Inc., San Diego, CA, USA, in 2016. From 2018 to 2020, he was a Postdoctoral Researcher with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA. In 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, as an Assistant Professor. His current research focuses on energy-efficient integrated circuits and systems, including power management integrated circuits, energy harvesting, wireless power transfer, and dc/dc converters.

Dr. Du was the recipient of the Dutch Research Council (NWO) Talent Program VENI grant in the 2021 round. He was the corecipient of the Best Student Paper Award in IEEE ICECS 2022. He has been an IEEE ISSCC Technical Program Committee Member since 2025, IEEE ISSCC Student Research Preview Committee Member since 2023, IEEE ICECS Subcommittee Chair in 2022 and 2024, and IEEE ISCAS Subcommittee Chair in 2025.