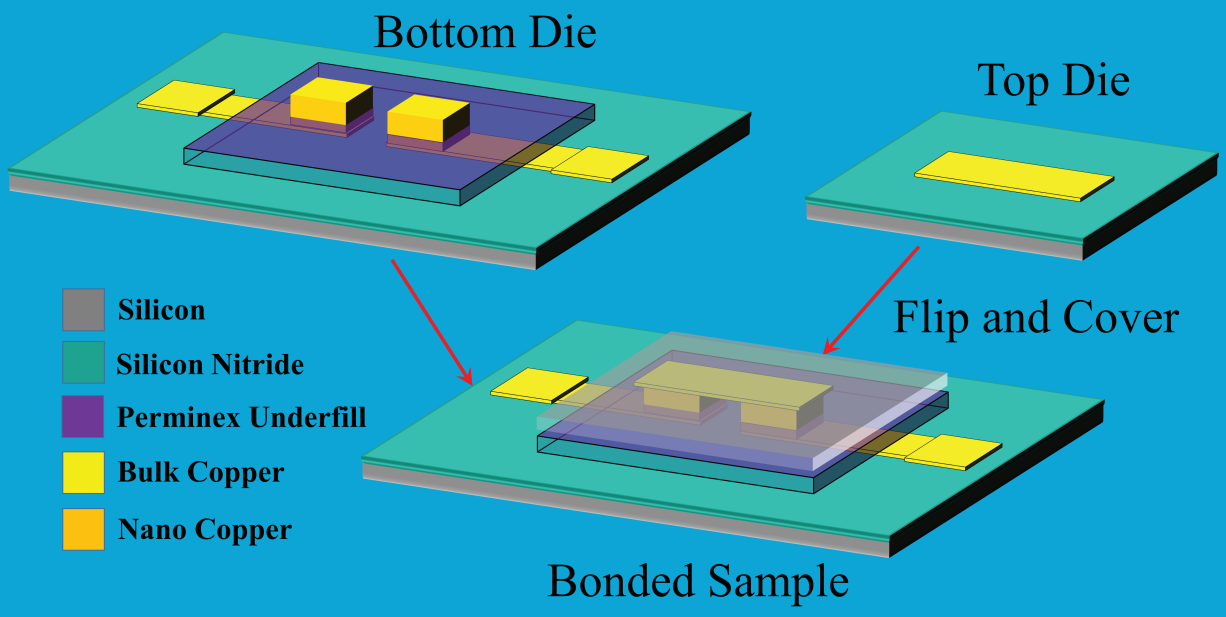
Msc thesis in Electrical Engineering

A combined vertical interconnect/underfill process for high density I/O flip chip bonding

Weiping Jiao

2022



TU Delft

A combined vertical interconnect/underfill process for high density I/O flip chip bonding

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1 ABSTRACT

This thesis investigates the all-copper fine pitch bonding process with photoimageable underfill. NanoCu paste is used as interconnect material. A bi-layer photo resist structure is manufactured and lithographic stencil printing is used to apply nanoCu paste. A new underfill injection method is realized by using epoxy resin based photo resist as underfill layer. Adhesion of sample is extensively enhanced. Various bonding methods are developed including using AML bonder and Tresky pick-and-place bonder. Electrical measurements for sintered nanoCu interconnect are conducted, sheet resistance and contact resistance are studied.

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As daily supervisor, Dr.ing. H.W. van Zeijl provides instant and key technological support, including job programming for wafer stepper, tricks for coating, methods to find proper exposure conditions and so on. Weekly meeting with him is very helpful for concluding and recording. He is willing to share his precious knowledge and experience as long as confusion pops up.

This work is mainly finished in EKL lab, engineers in EKL are experienced and helpful, they are willing to help at any time. Training for equipment is really valuable.

It is my pleasure to know that Prof.Dr.ir.Marcel Tichem is glad to be my thesis committee member.

List of Abbreviations

C2	Cu-Pillar With Solder Cap
C4	Controlled collapse chip connection
CBKR	Cross-bridge kelvin resistor
CMP	Chemical-mechanical polishing/planarization
CTE	Coefficient of thermal expansion
IC	Integrated circuit
IPA	Isopropyl alcohol
NanoCu	Nano copper
NMP	N-methylpyrrolidone
PGMEA	Propylene glycol methyl ether acetate
SAC	Tin(Sn)-Silver(Ag)-Copper(Cu)
SEM	Scanning electron microscope
TEM	Transmission electron microscopy
TLM	Transmission Line Method
TMAH	Tetramethylammonium hydroxide
UBM	Under bump metallurgy

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2 INTRODUCTION

2.1 PROJECT MOTIVATION

To satisfy requirement of low power consumption and high processing speed for future semiconductor devices, more and more attention is attracted by three-dimensional (3D) integration. To realized 3D integration, new interconnect material and process need to be developed. At first, traditional lead solder has been already forbidden by the Restriction of Hazardous Substances Directive (ROHS)[1], among various material, copper is considered as a promising candidate. Its low price and good electrical property are very suitable for interconnect material. At the same time, Metallic nano particles is proved that it can bond under relatively low temperature and attain high melting temperature, fine mechanical and electrical property as bulk metal material[2][3][4]. Therefore nanoCu is a great choice for cheap but high performance interconnect. It is worthwhile to realize all-copper interconnect by nanoCu and research nanoCu's property under real interconnect environment.

Secondly, underfill is massively used in packaging industry, but it usually takes a long time to fill in gap by underfill. Other methods to apply underfill are usually sophisticated and need special equipment. At the same time, there are always bubbles in underfill layer, which could harm reliability of whole package structure. Nowadays epoxy resin based photo resist has been developed, it is photoimageable and also can provide high adhesion after cure. Using epoxy resin based photo resist as underfill can at one hand provide splendid adhesion and at the other hand provide high accuracy because it is applied by lithographic process.

2.2 OBJECTIVE

The objective is to develop an all-copper combined vertical interconnect/underfill process for high density I/O flip chip bonding, it includes:

- Manufacture all-copper interconnect test sample.
- Find proper process to apply epoxy resin based photo resist and integrate it into test sample.
- Develop proper bonding method, adjust sample size and bonding plan
- Conduct electrical measurement to test sheet resistance and contact resistance of sintered nanoCu.

2.3 ORGANISATION OF THE THESIS

This thesis is organized to 7 chapters. Chapter 1 is the overview of motivation, objectives and thesis organisation.

Chapter 2 provides the literature review of flip chip interconnect background. solder and copper bonding technology, adhesive underfill technology and electrical measurement methods including cross Greek structure for sheet resistance, cross-bridge kelvin resistor for contact resistance, daisy chain and transmission line.

Chapter 3 describes the experiment methods used in this project. In the first section, the technique for bonding machine AML bonder and pick-and-place machine are introduced.

Chapter 4 introduces the masks used for exposure, job definition, the order for using, images' function and programming method.

Chapter 5 explains the a series of experiment conducted for photoiamgeable photo resist test. Experimental parameters for coating, exposure, developing of first underfill layer are determined by several test. In section 2, processing combined with the second photo resist layer is explored. In section 3, several bonding test are conducted to indicate the ability of adhesion for new photoimagable underfill.

Chapter 6 is for the all-copper interconnect experiment, In this chapter, It is firstly introduced that the fabrication of experimental copper wafer with photoimagable underfill layer integrated into the process by lithographic stencil printing. Secondly, nanoCu printing process is explained, a series of improvement are made for explicit pattern. Lift-off process is then presented and analyzed, Final workable result is also shown. At last, electrical characterization is conducted for all-copper interconnect samples.

Chapter 7 includes conclusion and outlook for future.

3 LITERATURE REVIEW

3.1 FLIP CHIP

As the increasing requiremnet of multifunctionality, high performance, data bandwidth, lower power, lower cost and so on, Three-dimensional (3-D) hyperintegration is considered to be a promising technology which could result to an industry paradigm shift [5].In the future, different components like processor, sensor, bio device,memory and power supply would be integrated to be a heterogeneous system as shown in Fig.3.1. To realize the data and energy transfer between different parts, the heterogeneous integration requires more advanced interconnecting methods.

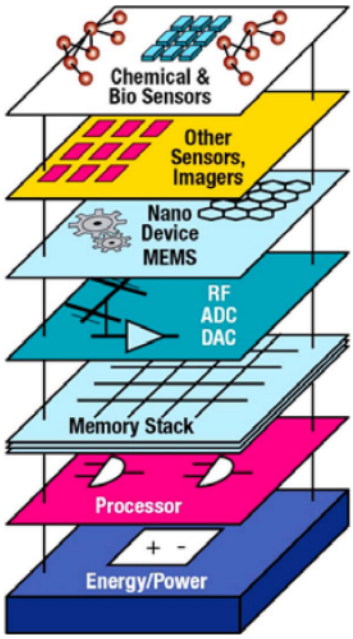


Figure 3.1: A vision of future 3-D hyperintegration of InfoTech, NanoTech, and BioTech systems[5].

Wire bonding and flip chip are two main methods IC interconnects, they both can be used to connect chip to substrate or another chip. As shown in Fig.3.23.3, the main difference is the I/O pad area. Flip chip's I/O area is facing the substrate and acting as mechanical connection at the same time. For wire bonding, chip would be firstly connected to substrate by pure mechanical connections. I/O area is at the other side of chip and connected to substrate by metal wire.

Compared to wire bonding, flip chip is more stable and robust. it is always used in high performance products like military electronics which usually requires devices can work in exterme temperture range from -55 $^{\circ}C$ to +125 $^{\circ}C$ and survive under vibration, moisture, high g, high shock, and radiation environment[6]. By directly generate electrical connection between chip and substrate, flip chip device has shorter signal path and smaller latency. Also flip chip can realize high density I/O array bonding by utilizing the area between chip and substrate[7].

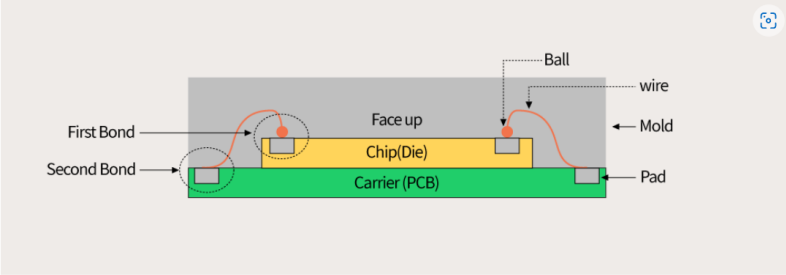


Figure 3.2: Definition of wire bonding assembly[5].

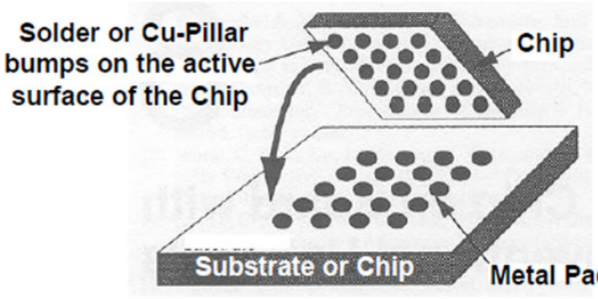


Figure 3.3: Definition of flip chip assembly[5].

In 1964, IBM invented the first flip-chip interconnect structure and applied it in their System/360 computer line[8]. An ND/OR invert logic block containing three transistors was connected to the substrate by Sn-Pb solder bump. Fig.3.4 shows the structure and flip chip assembly of this pioneer technology.A conventional flip chip the controlled collapse chip connection (C4) bump process is showed in Fig.3.5[9].

Before apply solder, an under bump metallurgy(UBM) structure would be made to enhance the adhesion between pad and solder. Usually a 0.3 - 0.8 μm copper layer is used to be adhesion layer with a 0.1 0.3 μm Ti or TiW barrier layer underneath to avoid the contamination from copper. Then 40 μm photo resist is coated and patterned by lithography and development. Next, electroplating 5 μm Cu layer. applying current through the plating bath , the wafer is the cathode. Then electroplate the solder. it is always plated more until the solder is higher than photo resist layer in order to achieve high solder bump . The photo resist, remaining Ti/TiW and Cu would be removed by heydrogen peroxide or plasma etching. At the end, the solder is heated up. the solder will melt and reflow to a ball because of the surface tension. The reflow results to that the solder joint can self-align to the UBM position and the heightness of joint only depends on the amount of solder. Usually The extra amount of solder can ensure the stand-off height during the reflow and collapse. Therefore, this process is called "controlled collapse". The Fig.3.6(a) is a SEM picture for 100 μm C4 bump.

In order to increase the count of pads in a smaller area, decreasing pitch(distance between pads) becomes to a key point to improve the flip chip technology. Derived from C4 bump, tall copper pillar with solder cap(C2) technology is invented and massively used in modern flip chip industry. A typical process of C2 is similar to C4, A tall copper pillar(up to 30m[7]) instead of solder is electroplated on the UBM after the patterning of photo resist. Then, photo resist is striped off and remaining Cu/Ti is etched. Next, after applying flux on the copper pillar, solder is electroplated on top of it and reflows under high temperature. The Fig.3.6(b) is a SEM picture for 100 μm C2 bump.Due to insufficient solder volume, it can not self align to the right position therefore it is not controllable collapse and called chip connection(C2).

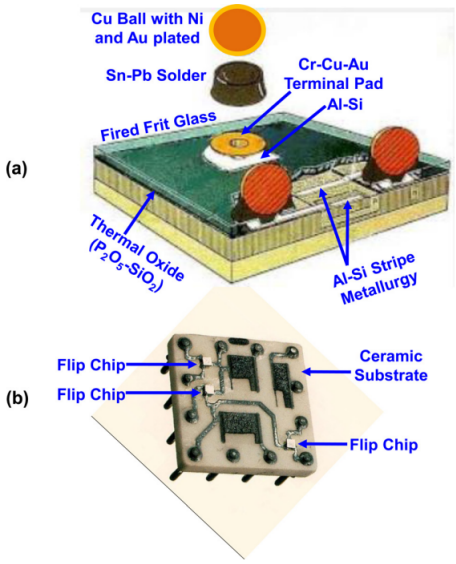


Figure 3.4: (a) IBM's first flip chip component with three terminal transistors. (b) IBM's first flip chip assembly (three chips) on a ceramic substrate[9].

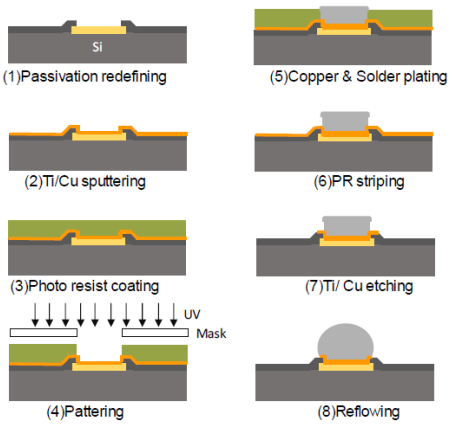
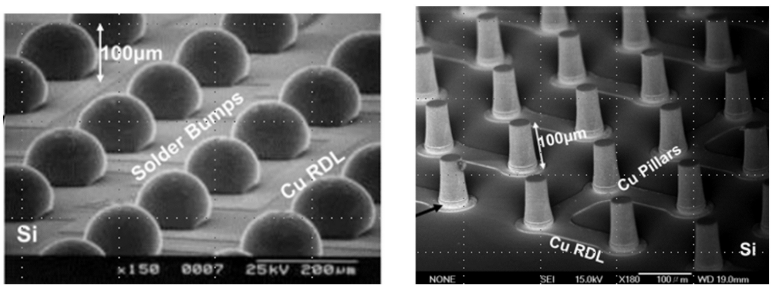


Figure 3.5: Typical process steps of solder bumping[7].

3.2 UNDERFILL

In 1992, IBM proposed the low-cost organic substrate as a substitution of relatively expensive ceramic substrate for flip-chip assemblies. To relieve the coefficient of thermal expansion (CTE) mismatch between silicon chip($2.5 \times 10^{-6}/°C$) and organic substrate($15 - 18 \times 10^{-6}/°C$) , underfill was used in their new proposal[10]. It is proved that underfill can extensively reduce the CTE mismatch and improve the reliability of solder joint.

Underfill is a encapsulate in liquid form under normal temperature. It is filled between chip and substrate and then cures under higher temperature. The main purposes of applying underfill are enhancing the adhesion between chip and substrate, decreasing the CTE mismatch, and redistributing the thermal stress to avoid it concentrates on the peripheral joints. It is demonstrated that underfill can reduce the solder strain and extend the solder joint life time from 10 to 100 times[11]. The commercial underfill material consists of liquid prepolymer which can be cured to enhance the adhesion, and silica (SiO_2) filler which can increase the composite strength and decrease the CTE[12]. Fig.3.7 demonstrates Generic configuration of C_4 with underfill.



(a) (b)

Figure 3.6: Scanning electron microscopy images of (a) C4 solder bumps and (b) C2 Cu-pillar without solder cap[9].

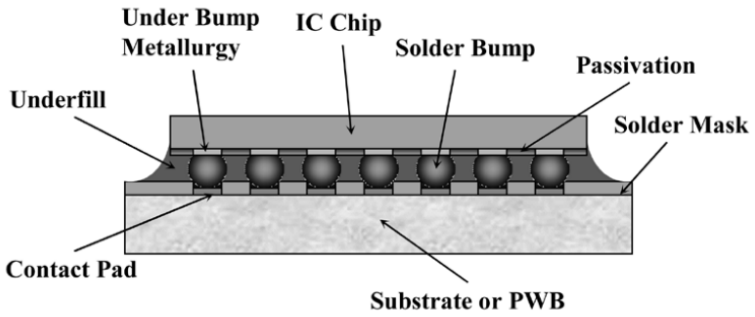


Figure 3.7: Generic configuration of C4 with underfill [11].

3.2.1 Conventional capillary underfill

Conventionally the underfill is applied after the solder bonding, As shown in Fig.3.8, it is injected from one side of interval between chip and substrate.

It spreads and fills the gap by capillary force, which is very slow. The spreading process also can result to many voids in the final solid composite. As shown in Fig.3.9, the fill time for encapsulating the gap of length L can be calculated by[13]:

$$t_{fill} = \frac{12\mu L^2}{\Delta p h^2} = \frac{6\mu L^2}{\sigma h \cos\theta} \tag{3.1}$$

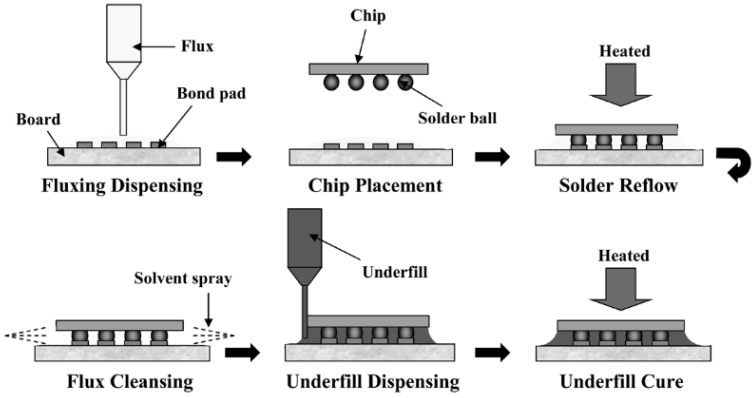


Figure 3.8: Flip-chip process using conventional underfill [11].

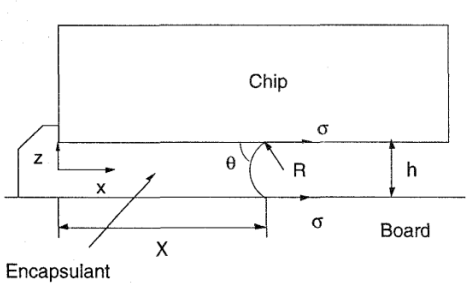


Figure 3.9: Flow of encapsulant in the cavity between chip and board. [13].

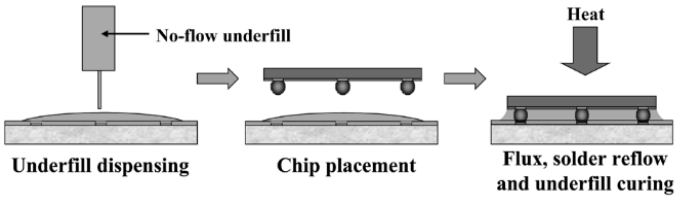


Figure 3.10: Flip-chip process using no-flow underfill [11].

where Δp is the pressure drop at location X, η is the fluid viscosity, Δ is the surface tension coefficient, h is the distance between the chip and substrate and θ is the contact angle.

Although conventional underfill process enhances the bonding strength and relieves the CTE mismatch problem, its long process time, incomplete capillary flow and flux residual still leads to many interfacial problems. To avoid them, new methods to apply underfill are developed.

3.2.2 No-flow underfill

Wong *etal*. invented the first no-flow underfill in 1996[14]. As shown in Fig.3.10, the no-flow underfill process is significantly simplified compared to conventional method. The no-flow underfill material is specially designed which have two main properties[11]: reaction latency and fluxing ability. reaction latency means the underfill needs to avoid complete reaction during the formation of solder joint, in another word, it needs to keep low viscosity under the high temperature and pressure. The reason for the requirement of reaction latency is that solder can not contact the pad well if underfill cures too soon and occupies the surface of pad.

The flux can remove and avoid the oxidation, therefore ensure the wetting of solder on the contact pad. the no flow underfill process does not have flux applying step but the underfill itself is able to behave as flux. Actually the original idea of no-flow underfill is just to integrate the flux and underfill proposed by Penisi *etal*. in 1992[15].

3.2.3 Molded underfill

In 2020, Gilleo*etal*. firstly propose the molded underfill (MUF) process. As shown in Fig.3.11, a special mold setup is placed along with chip and substrate, then underfill is injected not only the gap between chip and substrate, but also the other part of cavity in the mold. The assembly is then cured. The mold setup is removed at the end. By using molded underfill, the over-molding and dispensing underfill step are combined and total process time is saved. At the same time, more silica filler can be contained in molded underfill, the bonding's mechanical stability is improved[16].

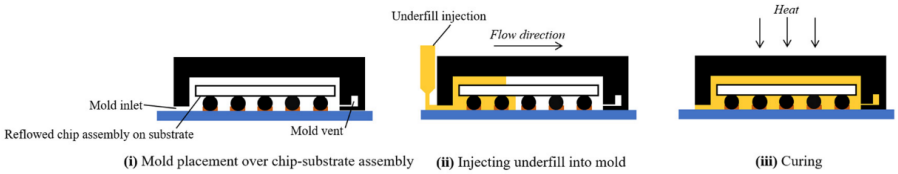


Figure 3.11: Process flow schematics of molded underfill encapsulations on chip device[16].

However, the molded underfill process can not rework if there are flaws, incomplete filling also can occur and results to void in the bonding. Lastly, it costs more because more underfill fluid is needed to over-mold the setup.

3.3 NANOMETALIC SINTERING

European directive Restriction of Hazardous Substances Directive (ROHS)[17] has been used legislation to abolish lead from microelectronic industry as solder filler. Many research are conducting to explore lead-free solder. Heterogeneous integration is facing the requirement of smaller feature size, high reliability and better electrical property[18][19][20][21][22] In order to address the rising interconnects challenge for integration, metallic nano particles material is drawing more and more attention recently. A series of research about nano silver has shown it is a promising candidate for future interconnects[23][24][25][26].

Compared to high-price silver, copper is cheaper but has almost the same electrical property. Obviously, copper can better satisfy the high volume need for interconnects material from industry. At the same time, once nano Cu is formed to bulk copper by sintering, it has the same reflow temperature as bulk copper($1085^{\circ}C$). In contrast to normal lead-free solder Sn-Ag-Cu(SAC) alloy, which would reflow at 220-250$^{\circ}C$, nanoCu bonding can be significantly stable under high temperature[27] Also, cracks and delamination problem easily happens when the solder contains multiple kinds of mental due to intermetallic compounds' growth.[28], therefore, single-component nano particle material can be a potential solution to avoid the generation of alloys in the bonding structure.

The nano metallic paste consists of nano-size metallic particles and a bunch of organic solvents. Since the nano particle is extremely easy to be oxidized in the air, organic material is added into paste to prevent the nano particle contacting air. Also, the organic additives can bind the nano particle together into the paste and adjust its viscosity. Therefore, by the form of paste, nano particle can be dispensed as the solder used in IC industry.

In Fig.3.12, transmission electron microscopy(TEM) pictures clearly show the nanoCu cores covered by organic shell. The size of nano particle is too small and they are separated by organic shell, therefore the surface is large, which result to thermodynamically instability. Under high temperature and pressure, the organic material would evaporate, then nanoCu particles would expose and interact to each other. the electrons surrounding the nanoCu surface tend to form metallic key with other copper particle because the energy of free electronics is higher than electronics in metallic key.

In 2018, Jie and Xin et al. report a novel nano silver paste die bonding experiment[30], As shown in Fig.3.13, with increasing temperature, the sintered structure morphology tends to merge into a whole porous structure from separate nano particles. At first 200$^{\circ}C$ condition, the organic shells already decompose and particles form neck connection between their boundaries. but many particles still stay in their initial morphologies. As the temperature increases, the particles start to grow into bigger part and finally are merged together. It is clearly showed that the sinter-

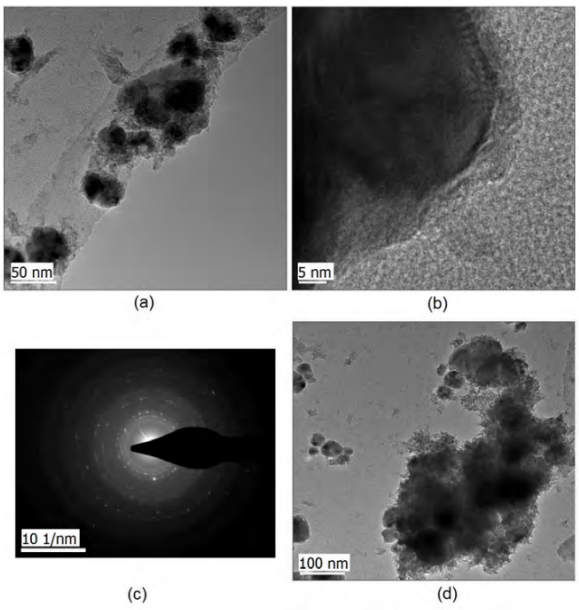


Figure 3.12: TEM images of unfused nanocopper: (a) nanocopper particles (dark areas); (b) nanocopper crystal lattice lines; (c) SAED pattern of nanocopper paste; (d) Copper nano particles surrounded by solvents and surfactants.[29]

ing process can form nano particles into high-density bulk structure though with porosities.

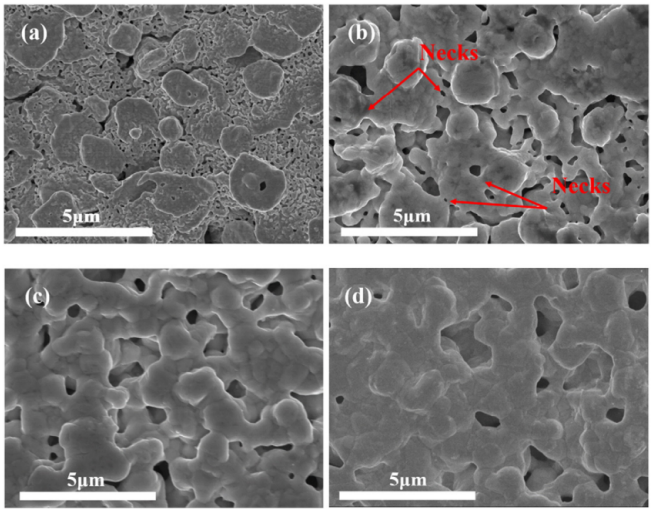


Figure 3.13: SEM images of the microstructures of the paste layers sintered in air at (a) 200°C, (b) 230°C, (c) 265°C, (d) 300°C.[30]

As a cheaper substitute to silver, Copper has a price which is only 14% of silver's and similar electrical and mechanical properties. It has been massively used not only in packaging but also inside the device. Therefore it is more meaningful to research on the bonding properties between nanoCu paste and copper pad.

3.4 ELECTRICAL MEASUREMENT STRUCTURE

Since nanoCu is used for interconnect in flip chip, its electrical property is important for future application. Resistivity (ρ) is used to compare various materials' electrical property i.e. the ability to conduct current. It is defined as the resistance of a material specimen of unit cross section and length:

$$\rho = R\frac{A}{\ell} \tag{3.2}$$

where A is the cross-sectional area, R is the resistance measured of specimen and l is the length.

3.4.1 Sheet resistance

Sheet resistance is the most basic and important property for material in semiconductor industry. It is used to quantify the capacity of material to conduct current in thin films, which is the usual case in semiconductor devices.

It is measured by four-probe method instead of two-probe method, in four-probe method, As shown in Fig.3.14, there are four probes placed on the sample with same distance. DC current is forced to flow through outside two probe and sample, inner two probes measures the voltage drop of sample. Since there is no current flowing through the inner two probes, wire resistance of voltmeter probe R_W2 and R_W3 and contact resistance between probe and sample R_C2 and R_C3 will not cause to any voltage drop, So measured voltage difference between two inner probes is only result from R_S2. Therefore, four-probe measurement can be accurate to measure small resistance.

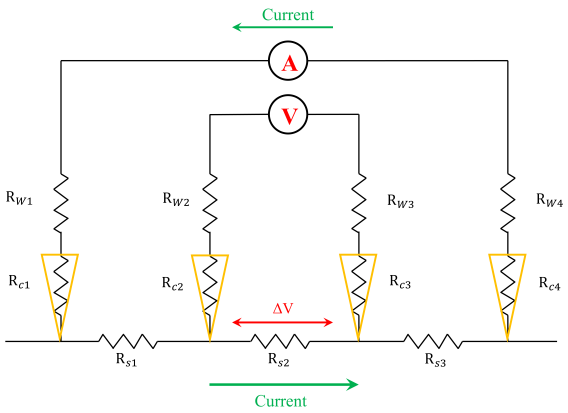


Figure 3.14: Equivalent circuit diagram of a four-point probe circuit schematic, R_W is wire resistance, RC is contact resistance, RS is sample resistance.

The greek cross is a typical four-probe test structure. it is widely used in semiconductor industry to measure ultra-small-size sheet resistance. As shown in Fig.3.15, sheet resistance can be measured by forcing current flow through one side and measure voltage drop on the other side. For example, the current flows through pad A and B, and voltage difference is measured between D and C. so sheet resistance can be calculated by:

$$R = \frac{V_{DC}}{I_{AB}} \tag{3.3}$$

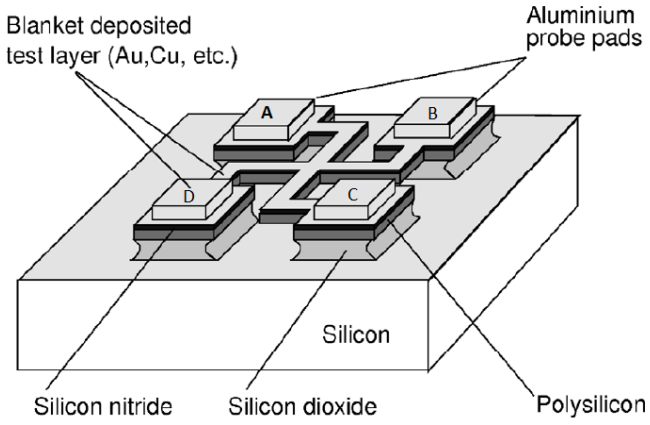


Figure 3.15: Suspended Greek cross test structure[31].

If current flows through pad BC and voltage is measured on the other side, it can also be calculated by:

$$R = \frac{V_{AD}}{I_{BC}} \tag{3.4}$$

Then Sheet resistance can be calculated by[31]:

$$R_s = f\left(\frac{\pi R}{\ln(2)}\right)[\Omega/\square] \tag{3.5}$$

Where f is the correction factor for the geometrical asymmetry of test structure. If the structure layer is uniform and homogeneous in composition, f is 1. The $\Omega/\square$ is a special unit for sheet resistance, which means the resistance is always the same if width and length of sample are same. This consistency of sheet resistance enable it can be used to compare the ability to conduct current in thin layer with same thickness of different materials.

With homogeneous film and known thickness, the resistivity can be derived as:

$$\rho = R_s t[\Omega \cdot m] \tag{3.6}$$

3.4.2 Cross bridge kelvin resistor

In semiconductor devices, there are always contacts between metal to metal, metal to semiconductor, which is called "ohmic contact". It is critical for any device's performance and reliability to have ohmic contact with low contact resistance and linear electrical I-V behavior. High contact resistance causes to high RC time constant and more delay. Power dissipation via joule heating in low frequency. in a ward, contact resistance (R_c) is important and need to be measured accurately. Specific contact resistivity can be calculated by As the ohmic contact area becomes smaller, cross bridge kelvin resistor is used frequently because it is more suitable for low-value measurement[32]. As shown in Fig.3.16, current is forced to conduct from pad C to D, voltage drop is tested between pad A and B. contact resistance can be easily derived as:

$$R_c = \frac{V_{BA}}{I_{CD}} \tag{3.7}$$

In one-dimensional analytical model, the measured resistance is the contact resistance and the specific contact resistivity(ohms times square centimeter) can be calculated by resistance R_C and contact area A:

$$\rho_c = R_c A \tag{3.8}$$

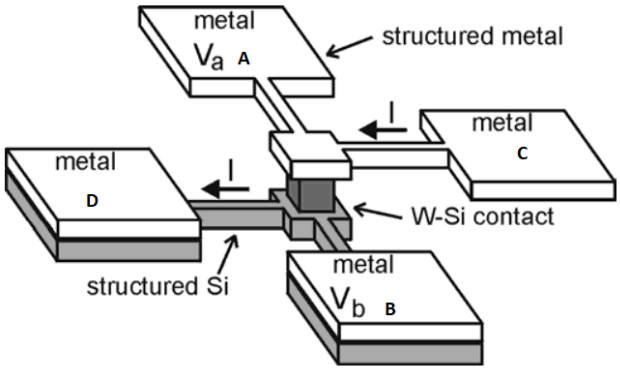


Figure 3.16: Cross-bridge Kelvin resistor[33].

3.4.3 Transmission line

As Schottky developed the accepted Schottky model for metal-semiconductor junctions[34], He also proposed a method to measure specific contact resistivity (ρ_c), As shown in Fig.3.17, the dark contacts are placed on the silicon, current is forced to flow through the whole ladder structure. the potential differences are measured between the first pad and following pads. with increasing distance, resistance measured increases also, as shown in Fig.3.18, the result can be plot as a function curve between distance and measured voltage drop. when the linear relation line is extended, horizontal intercept can be calculated. It is called transfer length (L_t), which indicates the distance where the voltage decreases to $1/e$ of the voltage at the contact[35], i.e. most of the current has already transferred to a different material. Then ρ_c can be derived as[36][37]:

$$L_t = \sqrt{\rho_c / R_{sh}} \tag{3.9}$$

Where R_{sh} is the sheet resistance of silicon under the metal contact.

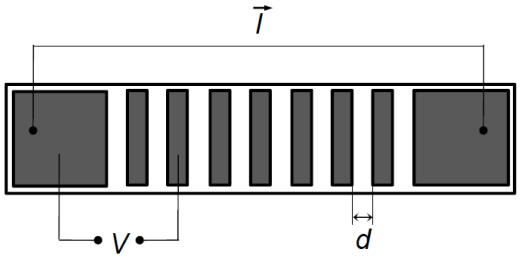


Figure 3.17: Top view of the Shockley's ladder structure, showing the contacts on silicon[38].

Then, the ladder structure with same distance was adjusted[39][37]. The contact pads are placed with different distance as shown in Fig.3.19 (a). For modified structure, voltage difference is measured between adjacent pads in order to avoid the disturbance from others contact pads in between. Now the figure is plotted by measured total resistance and distance as shown in Fig.3.19 (b), the slope of line is the sheet resistance of underneath material divided by width of contact pad, the vertical intercept is double value of contact resistance and the transfer length is the same.

In transmission line model, the contact resistivity can be expressed as[35]:

$$\rho_c = \frac{L_T}{R_{SH}} \left(\frac{R_C W}{\coth a / L_T} \right)^2 \tag{3.10}$$

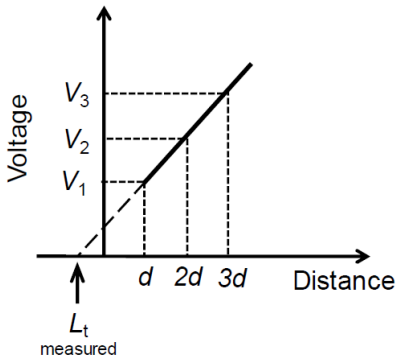


Figure 3.18: Lt extraction from the Shockley method [38].

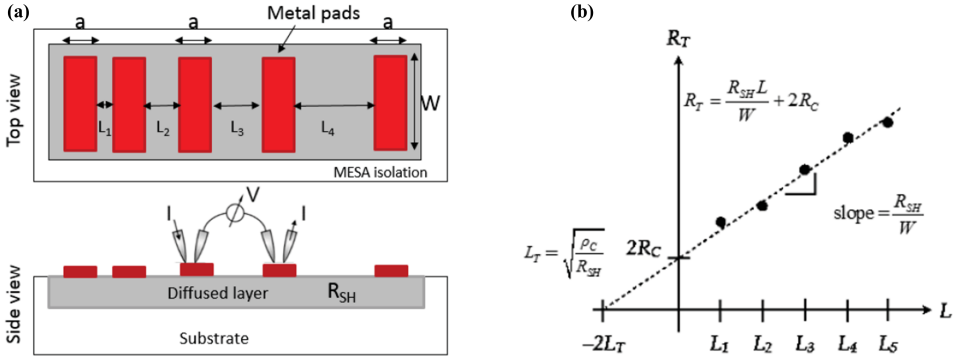


Figure 3.19: (a) Top and cross sectional views of a typical TLM structure; (b) extraction of sheet resistance and transfer length[35].

where a is the length of contact pad. Eq.3.10 can be simplified when length a is smaller than 0.5 L_T and bigger than 1.5 L_T[35]:

$$\rho_c = \begin{cases} R_C W a & a < 0.5 L_T \\ R_C W L_T & a > 1.5 L_T \end{cases} \tag{3.11}$$

3.4.4 Daisy chain

Daisy chain is massively used in IC packaging industry, process failures can be easily and cost-effectively detected by daisy chain. It is a major challenge for solder joint reliability study that recording the occurrence of cracks and monitoring the propagation of cracks. X-Ray test has a limited resolution. It is destructive that using scanning electron microscopy (SEM) to observe cross section, SEM also can not be used for in-situ monitoring of cracks propagation. At the same time, it is difficult to do cross-section cut unless knowing the exact crack position[40]. Therefore, daisy chain is necessary for engineers to know where the crack is. For example, in Fig.3.20, By applying voltage on the daisy pad, engineer can easily detect the cracks by measure the resistance of pads. Once crack happens, the measured resistance would be infinite immediately. By measuring the pads in different position simultaneously, it can also realize in-situ monitoring of soldering point.

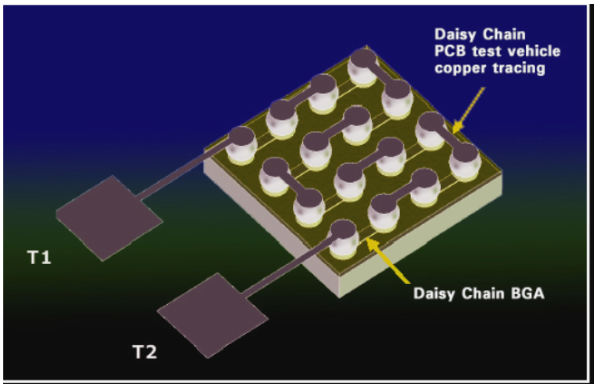


Figure 3.20: Schematic of daisy chain BGA mounted onto a PC board with complementary daisy chain circuitry[41].

4 EXPERIMENT METHODS

4.1 BONDING BY AML BONDER

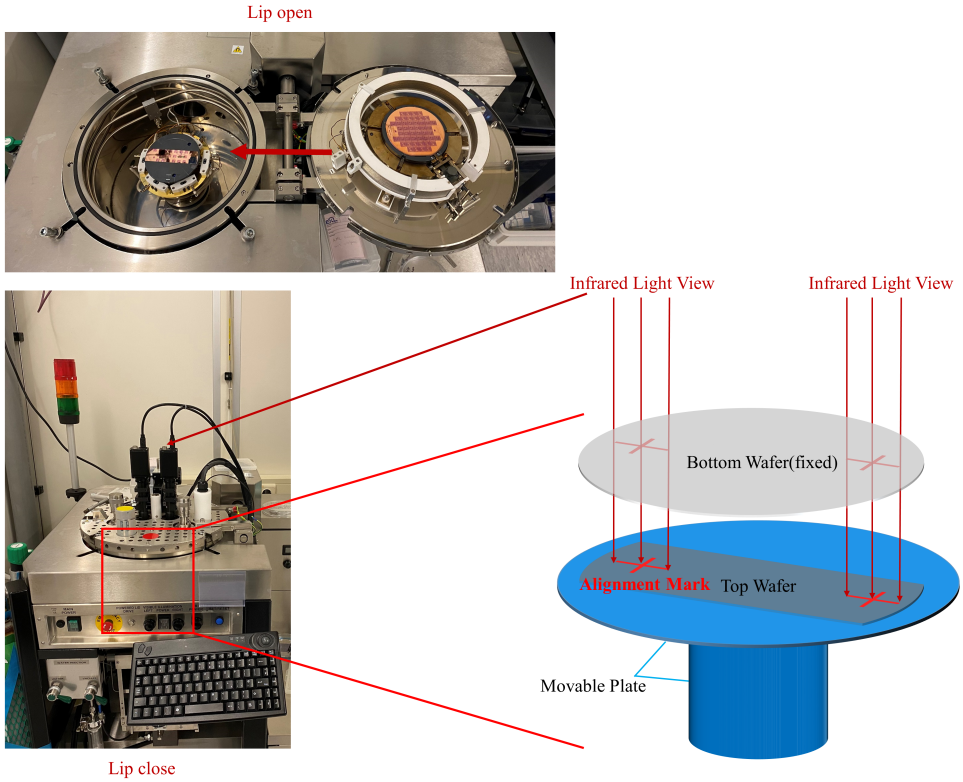


Figure 4.1: Schemetic of bonding by AML bonder.

Aligner Wafer Bonder AML is firstly used for sample bonding. A schematic of AML bonder is shown in Fig.4.1, it mainly consists of a chamber with a movable plate inside and a lip with infrared camera. One of the wafer can be clipped and attached to the lip(the wafer has to be a whole one) and another wafer(can be a die or any other form) is placed on the plate inside chamber. When lip is closed, the wafer attached to lip is fixed, the movable plate beneath can rotate and parallelly move on X, Y, Z axis. A infrared light source is placed under plate, two infrared camera on the lip can catch image of overlapping sample.

It is necessary to know some set up for samples before bonding them. As introduced before, bottom die and top die are different and made by two masks, they could have multiple combinations of various test structures. Fig.4.3 is a good case to illustrate. At first, a bottom die of 10 mm $\times$ 10 mm and top die of 6 mm $\times$ 6 mm with metal pad are made. Then a photo resist layer exposed by NM1.1 is applied on bottom die and nanoCu is also printed by photo resist stencil. As shown in Fig.4.2 (with perminex layer), top wafer is flipped and covered on top of bottom wafer, a test structure like sandwich consisting of metal pad, nanoCu and metal pad is formed. Since top die is smaller than bottom die, the remaining area will not be covered, redistribution pads are exposed to outside and connected to test structure by metal wire, therefore measurement can be done by applying and detecting voltage or current on these pad. Since the aim is to do electrical measurement,

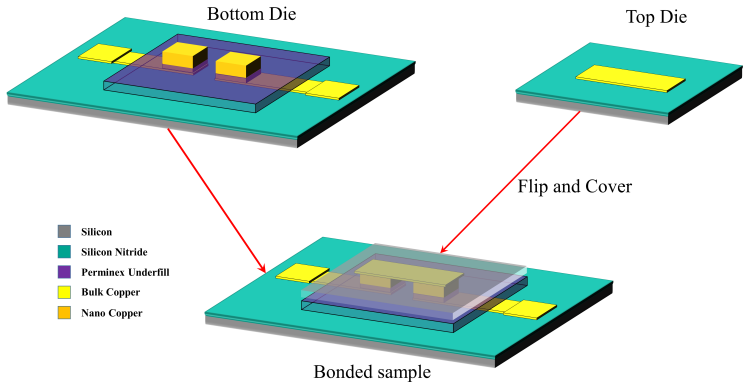


Figure 4.2: A model of bonding by perminex sample.

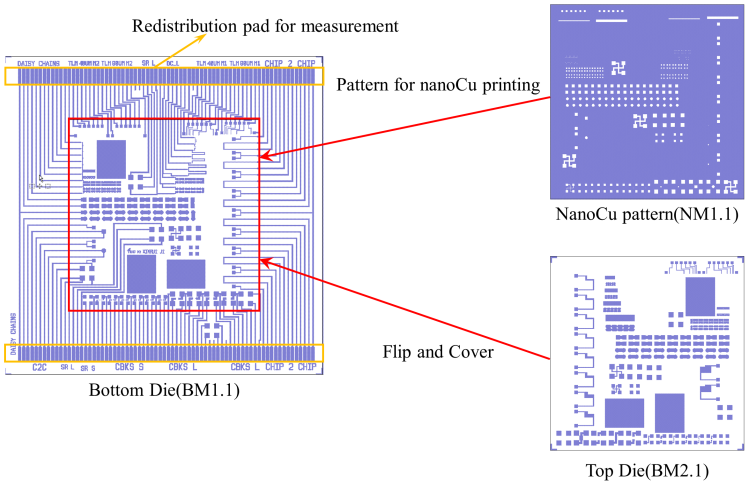


Figure 4.3: A case of mask combination.

accuracy is important for test structure such as daisy chain or cross bridge kelvin resistor. The alignment between two samples has to be precise enough to form measurement structure. To realize it, alignment marks for AML bonder is added to both bottom and top samples as shown in Fig.4.1. The infrared light can transmit through silicon but will block by metal, so silicon is transparent and metal is black under view of infrared camera. By patterning and etching, metal alignment mark surrounding silicon can be made and used for infrared light alignment.

At first, single-side-polished wafers are used for bonding, it is found out that nothing can be viewed by infrared light camera while two wafer is stacked. It is because the unpolished side of wafer is very rough in micro scale, infrared light is all scattered by two rough surface in this case. Therefore, double-side-polished wafers are used for both bottom and top wafer.

Since the position of infrared light camera is almost fixed on lip. alignment mark can only be placed on right and left side of wafers. To spare space for measurement pad, top wafer is cut off on top and bottom side. A disadvantage of this bonding method is that only top measurement pads of top line dies and bottom measurement pad of bottom line dies are exposed to out side, any other area is covered by another sample.

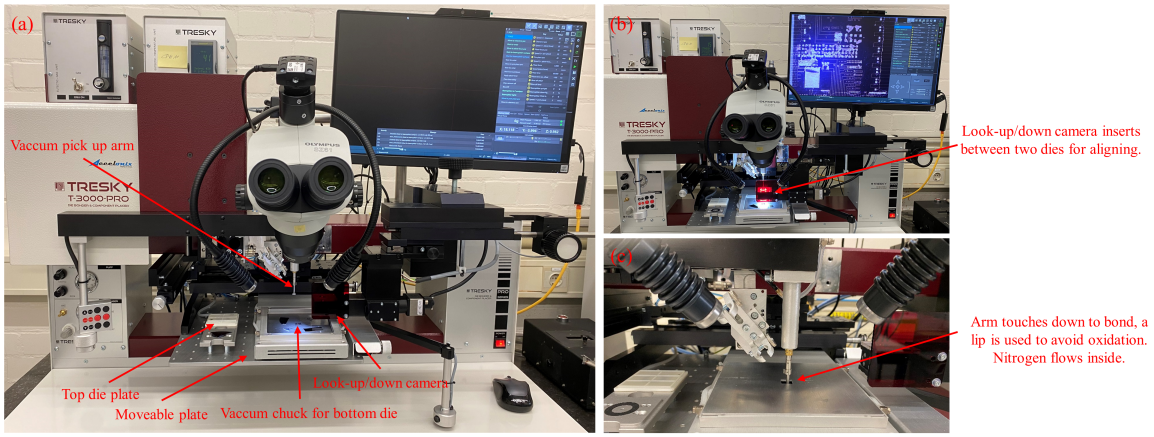


Figure 4.4: Pick and place machine.(a) Arm picks up top die; (b) Align dies by look-up/down camera; (c) Bonding dies.

4.2 BONDING BY PICK-AND-PLACE MACHINE

A better option for bonding is to pick-and-place machine. As shown in Fig.4.4, it mainly consists of a vacuum pick-up arm, a look-up/look-down camera and a vacuum chuck. The robotic arm is able to pick up a die and move it to right position, then camera can be inserted between bottom die and top die, By looking up and down at the same time, operator can align two dies precisely. After optical alignment, camera can be pull back and arm can bring top die onto bottom die and impose high force upto 6000g(1 gram-force [gf] = 0.0098 newton [N], 6000g is about 58.8N). A hot plate is also placed under vaccum chuck, which could rapidly increase temperature. by applying heating and pressure at the same time, nanoCu paste can be sintered.

Pick-and-place method is based on the application of perminex undefill layer. Main reason is adhesion and support to nanoCu provided by underfill. Since dicing is needed for gain dies from wafer, in this process, wafer needs to be fixed in certain position by sticking to fossil. Some force needs to be applied on fossil and wafer when wafer is facing down to plate. without underfill layer, nanoCu pillar may collapse under pressure and structure is ruined.

By using pick-and-place machine, the yield of measurable sample is increased significantly. At first, all good die on bottom wafer can be diced instead only two lines of die can be used. Secondly, both top and bottom measurement pad can be used instead of only one side is available. At last, top die's size is 6 mm $\times$ 6 mm, in order to match bottom die, it has to be placed in 10 mm $\times$ 10 mm square. For pick-and-place process, top wafer is also diced, it does not need to be patterned by 10 mm $\times$ 10 mm square, new design places 6 mm $\times$ 6 mm die next to each other. For a single 100 mm wafer, yield of top die can be more than 100.

5 MASK AND EXPOSURE JOB MODIFICATION

The masks used for this project are mostly designed by Xinrui Ji. It is designed and manufactured for ASML PAS 5500/80 waferstepper. It integrates multi-functional images and have to be used with programmed job.

5.0.1 Mask description

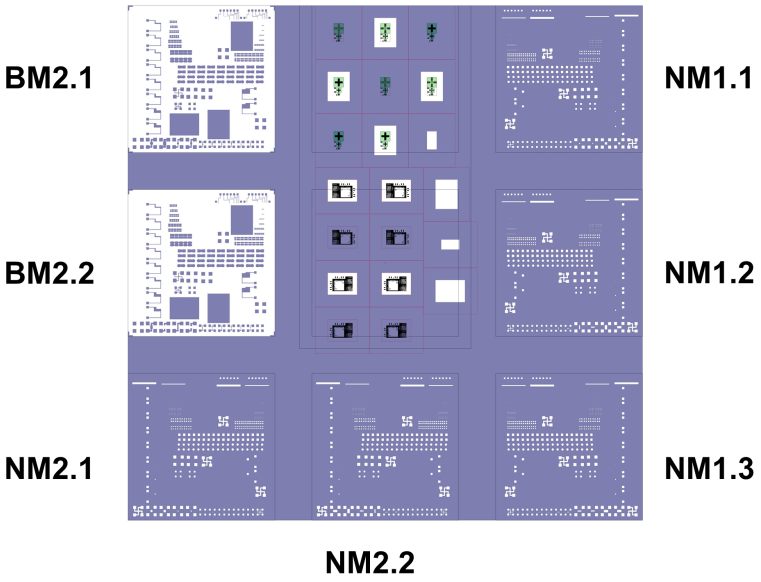


Figure 5.1: Mask1 layout.

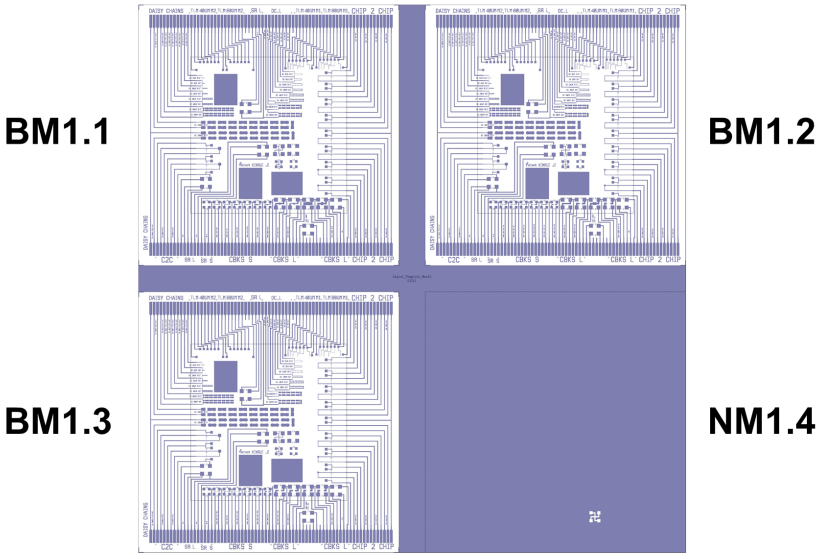


Figure 5.2: Mask2 layout.

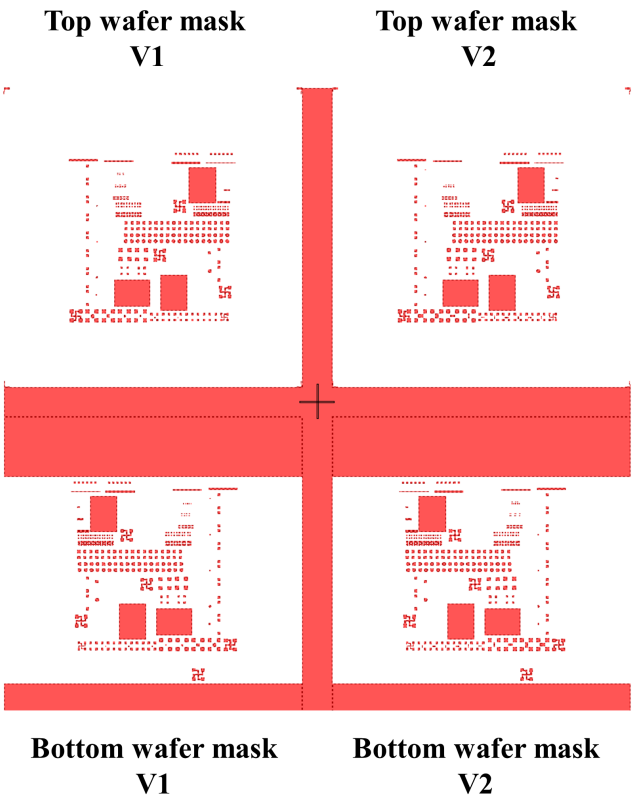


Figure 5.3: Layout of reverse mask for copper.

There are three masks used in this project. Mask1 and Mask2 is designed by xinrui, which are shown in Fig.5.4 and 5.2. They can be used for positive photo resist, several samples without perminex are made by these two masks.

Mask 1 consists of 9 $6mm \times 6mm$ images. It is mainly designed for top wafer. 7 of them can directly used for exposure. Other two blocks consist of a series of alignment marks and they needs to be specially extracted. Name for each die is shown in Fig.5.4, for the letter in name, BM means the image is for bulk copper pattern exposure, NM means the image is for nanoCu pattern exposure. For the first number, 1 is for bottom wafer and 2 is for top wafer. For the second number, 1, 2 and 3 means three different version, during manufacturing, bottom and top wafer should be exposed by same version pattern.

Mask 2 consists of 4 $10mm \times 10mm$ images, it is mainly designed for bottom wafer, the meaning of name is the same as mask 1, a special case is NM1.4, It will be used for nanoCu patterning and it should be used before any other nanoCu patterning, because its structure part is always in exposed part of other mask pattern.

For example, bottom wafer's metal pad is made by BM1.1 on mask 2, then after it is coated by 12XT, NM1.4 on mask 2 is firstly used to make a sheet resistance structure. Then NM1.1 on mask 1 is used to pattern more structure for bottom wafer. If NM1.1 is used at first, the area outside $6mm \times 6mm$ image will be exposed totally and NM1.4 can not be used any more. For top wafer, BM2.1 is used for make metal pad. Now bottom wafer and top wafer are ready to be bonded. If nanoCu is wanted on top wafer, NM2.1 can be used to make relative pattern.

To apply negative tone photo resist as underfill, a reverse mask is designed and it is shown in Fig.5.3, it contains 4 $10mm \times 10mm$ images, it is clear that all patterns for nanoCu on mask 1 and 2 like NM1.1 is converted from light to dark. Two lines are added for bottom wafer image to provide more space for measurement pad. bottom two images are for bottom wafer and top two images are for top wafer. Different version has varying contact pattern for cross bridge kelvin resistor.

For example, after metal pad manufacturing as usual, perminex is coated and it is firstly exposed by bottom wafer mask V1 on reverse mask. Then 12XT is coated and then patterned by NM1.4 and further patterned by NM1.1. Then, it is ready to be bonded with top wafer.

5.0.2 Wafer stepper job programming

There are two main steps for wafer stepper's job programming: mask defining and wafer defining. At first, programmer should define the die distribution on the wafer. For example, as shown in Fig.5.4. $10mm \times 10mm$ dies are placed on 100mm wafer.

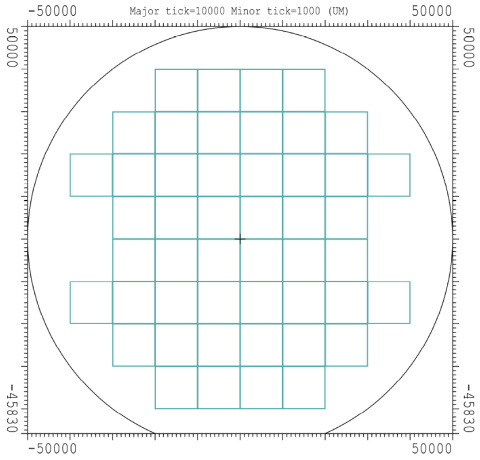


Figure 5.4: wafer defining schematic.

Secondly, user is supposed to define the mask ID. Multiple masks can be used in a single job. The ID need to be specified after loading the real mask. For example, In our project, NANOCU1 points to mask2 and NANOCU2 points to mask1. It should be noticed that the ID does not need to linked to real mask, user could also specify a different mask and wafer stepper would use this different mask to expose according to the program of specified ID. For example, our reverse mask for copper has the same image layout size(4 $10mm \times 10mm$ images) as mask 2, so while loading the reverse mask, it is also specified by NANOCU1. In a word, mask ID is a virtual object for wafer stepper's program, it can map to any mask.

The next step is to describe the image needed to use on the mask. A exposure job consists of multiple layers, each layer includes multiple images coming from mask. To build layer, image coordinates need to be specified at first, which is related to mask layout. For example, in mask 2, the left top image is for bottom wafer and its coordinate on mask is (-5500,5500), its length and width are 10mm and 10mm. By using these data, the left top image could be extracted. Now the question is where the image should place. So the reference coordinates should shift to layer layout's, as shown in Fig.5.5, layer defines the die image, its center is the die's center and size is $10mm \times 10mm$. Therefore, to fill the die with left top image, it should be placed on layer position of coordinate (0,0) and we name it "image 3".

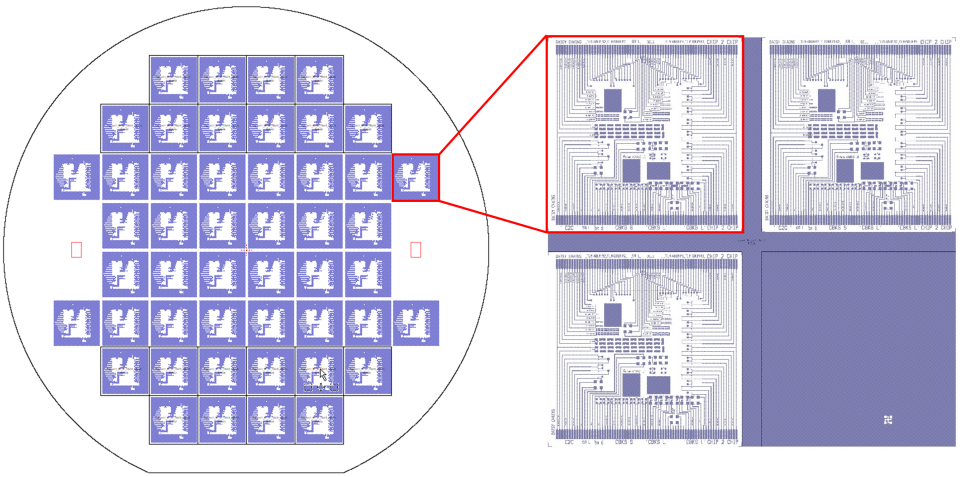


Figure 5.5: Insert image to wafer layout.

6 PHOTOIMAGEABLE UNDERFILL EXPERIMENT

A photoimageable photo resist is added as underfill, proper material and processing method need to be explored. we choose PermiNex 2015 from MicroChem Corp as our underfill material. It is epoxy resin based. low temperature and photoimageable bonding adhesive[42]. It is a negative tone photo resist, a special mask is designed for it as mentioned in last chapter. To apply a new photo resist, its data sheet is a good reference. But the real processing parameters still need to be decided by experiment since the manufacturing environment is different and material's performance is also varying with time.

The underfill layer will be added right after metal pad manufacturing step, expected thickness is 10 μ m, then it will be patterned almost same as the second photo resist layer. After development, the second photo resist layer will be added and patterned, via for nanoCu stencil printing is reserved on this bi-layer structure. After printing, the second photo resist layer will be removed along with residues on it, during this step, underfill layer should be able to survive and provide adhesion for printed nanoCu paste. Then sample will be bonded by thermocompression with another sample, underfill layer is expected to provide significant adhesion for bonded sample.

Therefore, several technical problems need to be solved: which material should be chosen? How to coat it? Can it survive lift-off step? How to expose it? how to develop it? is It still adhesive after lift-off step? A series of experiment is conducted to solve them.

6.1 COATING TEST

In our design, the perminex layer thickness is 10 μ m. As shown in Fig.6.1 from data sheet, the spin speed should be about 4000rpm

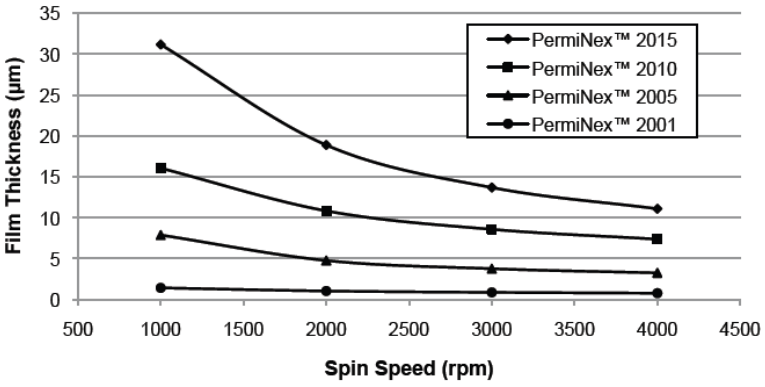


Figure 6.1: PermiNex 2000 Thickness vs. Spin Speed[42].

A wafer is coated by 4000 rpm. To ensure the right thickness, Dektak stylus profiling machine from Bruker is used to measure the thickness, the average thickness is measured as 17 μm. To decrease thickness to expected 10 μm, spin speed needs to

be increased. It is known that the photo resist thickness is proportional to a constant times the inverse of the square root of spin speed as shown in Eq.6.1:

$$\text{thickness} = \frac{\text{const}}{\sqrt{\text{spin speed}}} \tag{6.1}$$

So we can calculate the constant is about 1075.17. Then calculate the required spin speed for 10 μm, which is about 11559.9rpm. Our spin coating machine can not bear such a high speed. 8000 rpm is tried for new spin coating test. the result is 11.33 μm, standard deviation of several measurement points is 0.117. Therefore, the spin coating speed is set to 8000 rpm in following experiments.

6.2 SURVIVAL TEST

As another photo resist layer need to be removed after nanoCu printing, the patterned perminex layer is required to survive lift-off process. Before the test, we expose perminex test wafer by contact aligner and a no-pattern mask, as a negative photo resist, it can be cross-linked and strengthened by light during exposure. No development is needed since there is no pattern on wafer.

70 $^{\circ}C$ NMP (N-Methyl-2-pyrrolidone) and 35 $^{\circ}C$ acetone are used for survival test. The sample is placed in NMP and acetone with ultrasonic bath. As shown in Fig.6.3, a glass box suitable for single wafer is poured with NMP or acetone, then it is placed in ultrasonic bath equipment.

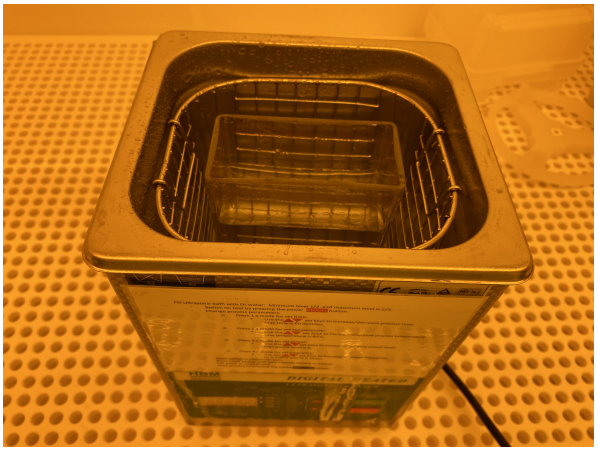


Figure 6.2: Setup for chemical treating with ultrasonic bath.

Dektak is used to measure the thickness of original and remaining photo resist layer thickness. The results of thickness changing are shown in Fig.6.3 and 6.5, which indicates that once exposed, perminex can survive in normal lift-off process and it may swell after treatment. This conclusion ensures that the perminex layer could be kept after lift-off process for normal photo resist. It means as long as we choose normal positive photo resist as the second layer to remove nanoCu residue, the perminex layer can survive.

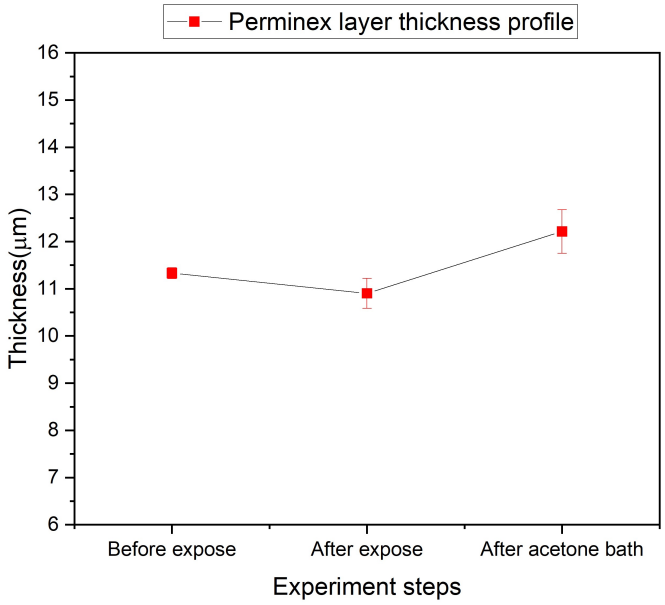


Figure 6.3: Perminex layer profile after acetone bath.

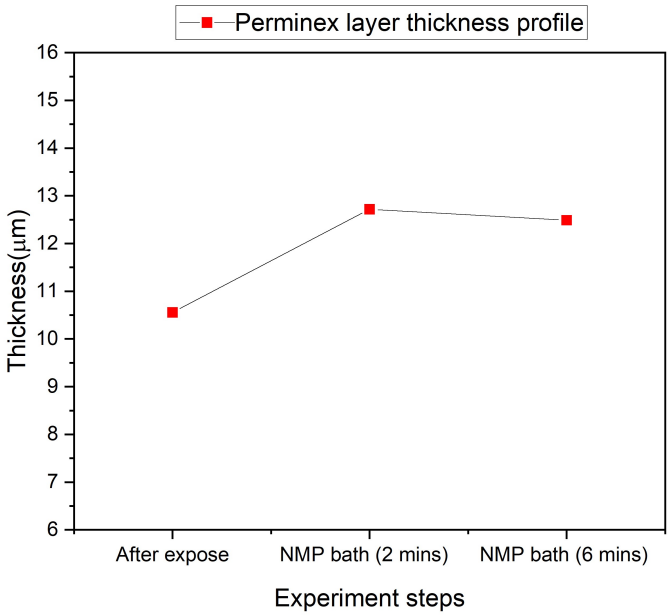


Figure 6.4: Perminex layer profile after NMP bath.

6.3 EXPOSURE TEST

To determine the proper exposure energy, a series of experiments are conducted. The exposure energy suggested in data sheet is 1000-1200 mJ/cm^2 for 10 μm layer.

6.3.1 Minimum energy exposure test

At first, contact aligner and a special mask (designed by Henk van zeijl) are used for minimum energy exposure test. As shown in Fig.6.5 and 6.6, a graduated neutral-density filter is placed on a bare glass mask, this filter has ruler scale from 0 to 100 with the optical density is graduated from 0 to 2. The neutral-density filter can decrease the intensity of light regardless of wavelength and color. Optical density is used to describe the capability of blocking light energy for the filter, high optical density indicates lower transmission rate, it can be quantified as:

$$\frac{I}{I_0} = 10^{-d} \tag{6.2}$$

Where I is light intensity after passing through the filter, I_0 is original light density, d is optical density.

As perminex is a negative tone photo resist, exposure can strengthen the photo resist by cross-link reaction. With graduated light intensity filter, as light density decreasing, photo resist becomes gradually not stable enough and will be removed later by developer at a certain point. Once the cut-off point is found, the minimum exposure energy can be calculated.

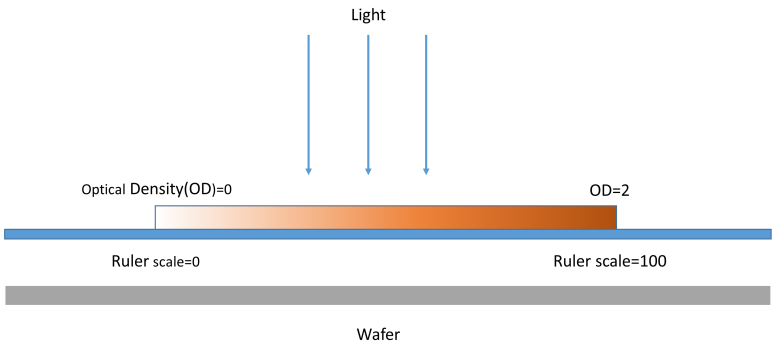


Figure 6.5: schematic of neutral density mask exposure.

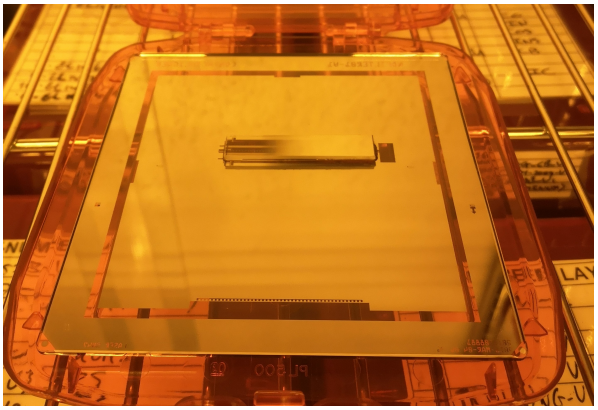


Figure 6.6: Neutral density mask.

SUSS MicroTec MA/BA8 mask aligner is used to expose perminex wafer. the exposure energy I_0 for testing is set to 4000 mJ, which is four times of recommended

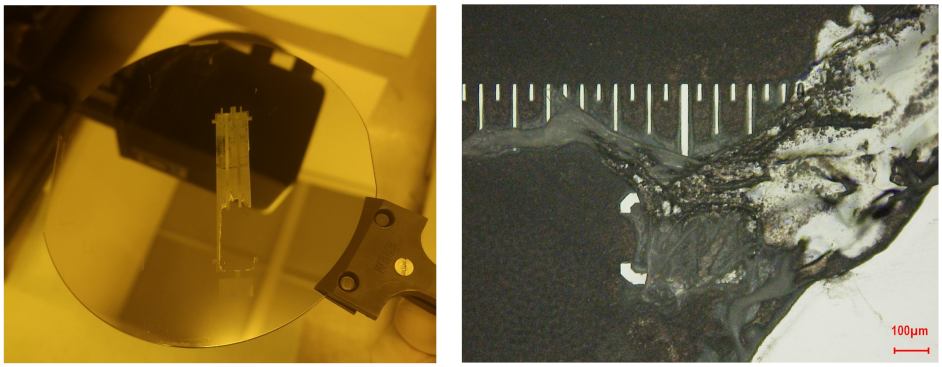


Figure 6.7: (a) Perminex sample wafer exposed by neutral density mask; (b) Cut-off point of perminex sample wafer exposed by neutral density mask.

energy. The development result is shown in Fig.6.7 (a) (b), the ruler ends at 30, where the optical density is $\frac{30}{100} \times 2 = 0.6$. According to Eq.6.2, minimum exposure energy needed for perminex is 1004.8 mJ.

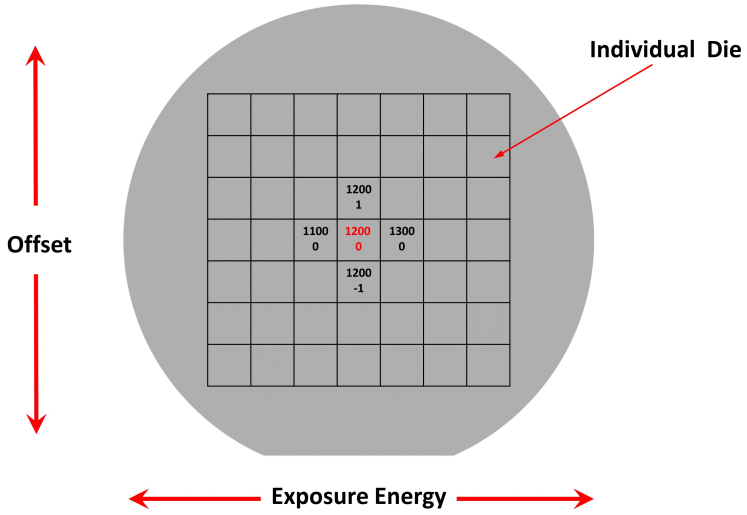


Figure 6.8: Matrix exposure test for perminex sample wafer.

6.3.2 Matrix exposure test

To determine the optimal exposure energy for perminex wafer, a matrix exposure test is conducted. The exposure job is shown in Fig.6.8, the middle die is exposed by 1200 mJ, 0 $/mum$ offset, energy increases by 100 mJ from left the right, offset increase by 1 μm from downside to upside. By this matrix test, a series of energy and offset can be tested on a single wafer. Firstly, Fig6.9 shows the pattern for dies on the middle line from left to right, the exposure energy for them are 700 mJ - 1800 mJ, the offset is all 0 μm. From (f), the structure becomes to stable and clear, which is exposed by 1200 mJ. (h) is supposed to be a special case considering the improving trend of higher energy. From Fig.6.9, it can be concluded that the minimum energy for clear pattern is above 1200 mJ.

Then, Fig6.10 shows dies on the rightmost line, which have fixed energy of 1800 mJ and different offset from -5 μm to 5 μm. It can not be specified too many differences between each other except extreme low offset. Since offset does not have

a large effect on exposure result. 0 μm in the middle position is chosen to be the offset for our process.

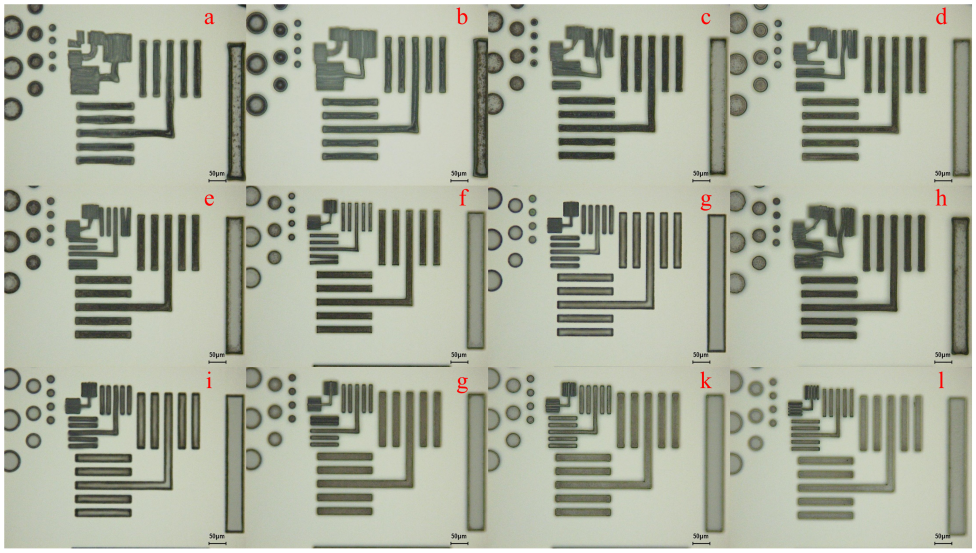


Figure 6.9: Matrix exposure test result. Offset is 0 μm (a) to (l): exposed at 700 mJ - 1800 mJ, increment is 100 mJ per figure.

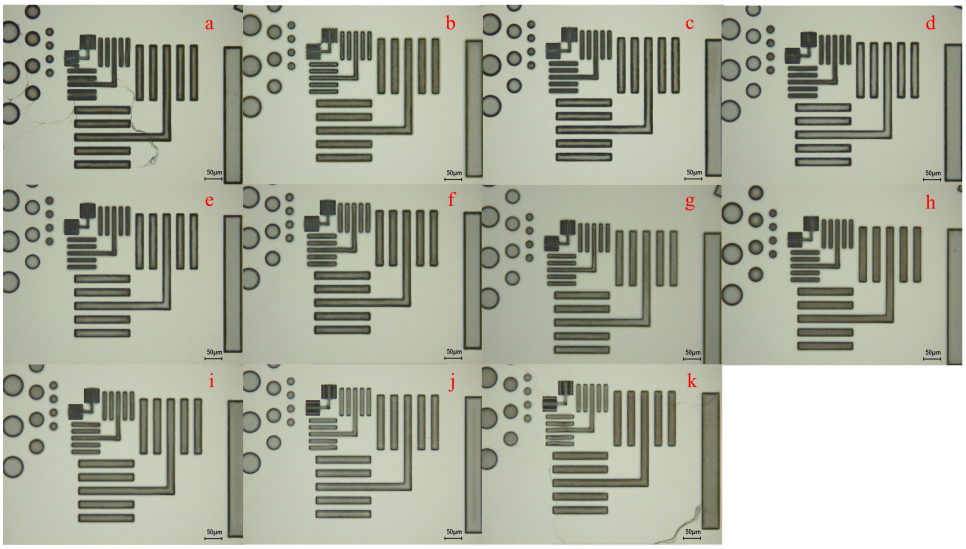


Figure 6.10: Matrix exposure test result. Energy is 1800 mJ, (a) to (k): exposed at -5 μm to 5 μm, increment is 1 μm per figure.

6.4 DEVELOPMENT TEST

To determine the develop method, we firstly tried recommended 2.38 % TMAH in data sheet, for 10 microns film, 1.5 mins development time is needed. But after immersing in MIF322 (2.38 % TMAH) for 5 mins, the unexposed area on wafer still does not solve in developer. this may result from that the photo resist has already been out of shelf time.

Since it is not possible to continue with TMAH and perminex is based on epoxy resin, we turn to using PGMEA (Propylene glycol methyl ether acetate), a usual developer designed for epoxy resin based photo resist.

6.4.1 Marangoni drying

At first, after PGMEA development, acetone is used to remove residue of PGMEA, then IPA is used to remove acetone, DI water is used to remove IPA, finally spin dry the wafer. The sample is the same one used for contact aligner exposure energy, The result is shown in Fig.6.7 and **??**, It is clearly full of white residue, under microscope, the surface is dark and dim. In following experiments, It is found that after devel-

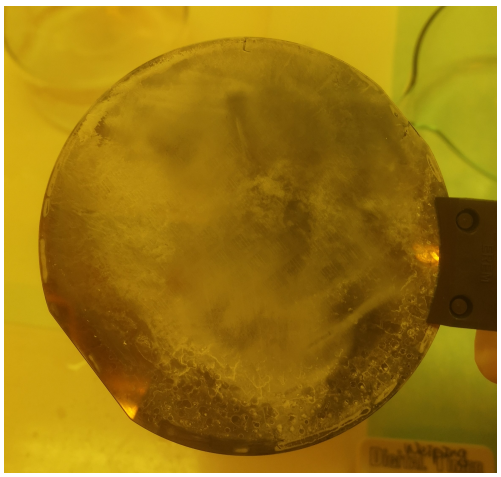


Figure 6.11: After PGMEA development, perminex wafer washed by water.

opment by PGMEA, once washed by water, There would be white residue on the wafer as shown in 6.11. It is observed that unexposed perminex photo resist would generate white residue once touched water. And also, since wafer is immersed in different liquid, the residue can be transferred for one to another, the final spin drying would leave undesired residue on the wafer because during the spin drying, though most of the wafer is removed by centrifugal force, part of water could evaporate and residue in these water would deposited on the wafer surface[43].

Since the acetone can evaporate soon in the air, it is possible to only use acetone to clean perminex wafer after development, and then remove acetone and dissolved photo resist by Marangoni drying. A schematic is shown in Fig.6.12, When wafer is lifted up from acetone, as residue is inclined to stay in acetone, by slowly lifting up, acetone will form a thin film area and a bulk liquid area. Intuitively along with the movement, residue from dry wafer part continuously enter thin film area, the upper thin film area contains more dissolved photo resist than lower bulk liquid area. Therefore the concentration of thin film area is larger than bulk liquid area. As surface tension decreases with increasing concentration of the dissolved residue[43],the surface tension at upper area will be lower than bulk liquid area. This surface tension difference result to a marangoni flow, a drainage is formed, this continuous drainage leads to a dry and clean wafer surface. Remarkable im-

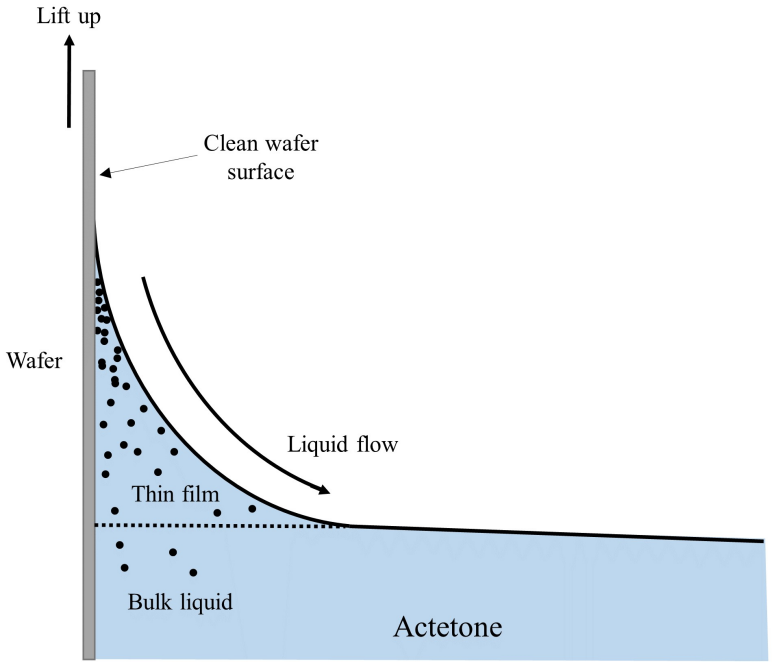


Figure 6.12: Marangoni drying for perminex wafer after development.

provement of development by using acetone and marangoni drying can be observed From Fig.6.14.

6.4.2 Development after exposure

Exposure and development are related to each other, insufficient exposure can only be observed after development. To determine optimal process, a series of experiments are conducted.

A wafer coated with perminex is exposed quarterly as shown in Fig.6.13, left side is exposed by 1000 mJ and right side is exposed by 1200 mJ. Because this wafer has no alignment marker for wafer stepper, four quarters have overlapping with each other at the edge part, which provide a good chance to observe exposure result of high energy (upto 2000 mJ and 2400 mJ).

After using acetone and marangoni drying, dim and thick white residue is removed. The result is shown in Fig.6.14 (a). However, light white residue is observed on the left side. Under the microscope, it can be seen that white residue is actually little bubbles in the photo resist as shown in Fig.6.15 (a).

The data sheet suggests a post-develop baking at $180°C$ for 5 mins. After baking, the bubbles are removed and perminex layer becomes smooth and transparent as shown in Fig.6.14 (b) and 6.15 (b).

Since 1200 mJ does not cause any undesired phenomenon, so it is a better choice to expose perminex wafer. However, It is observed that the overlapping area of 1000 mJ and 1200 mJ is smooth as well, so higher energy is might be a better solution.

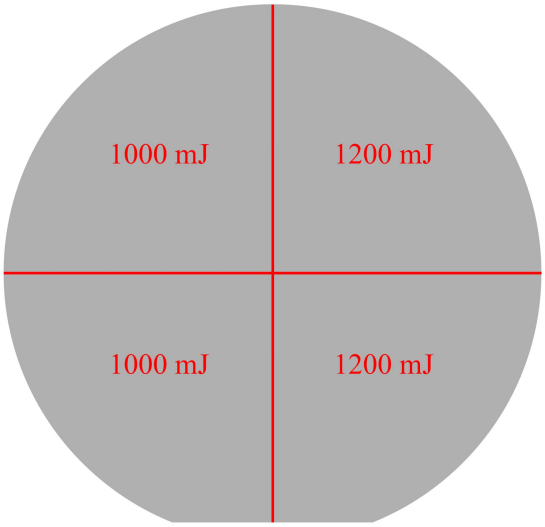


Figure 6.13: Schematic of quarterly exposure, left two quarters are 1000 mJ and right two quarters are 1200 mJ.

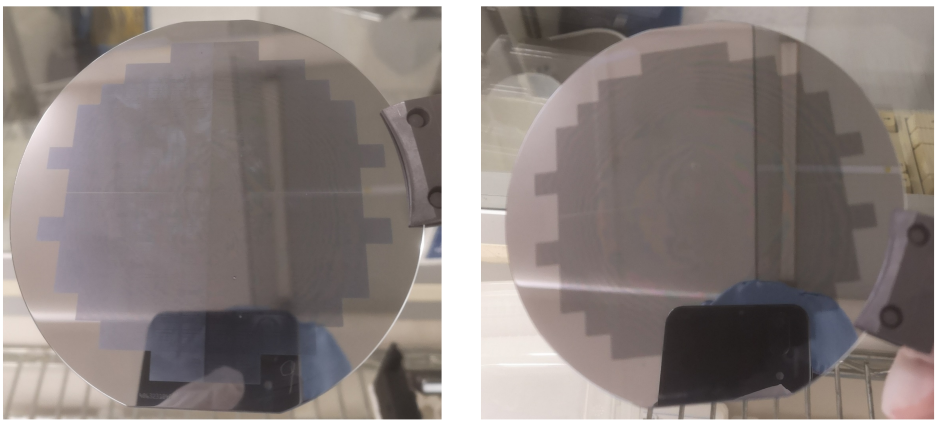


Figure 6.14: Perminex wafer's left side is exposed by 1000 mJ, right side is 1200 mJ.(a) after development; (b) after development and 180 $^{\circ}C$ post-develop baking for 5 mins.

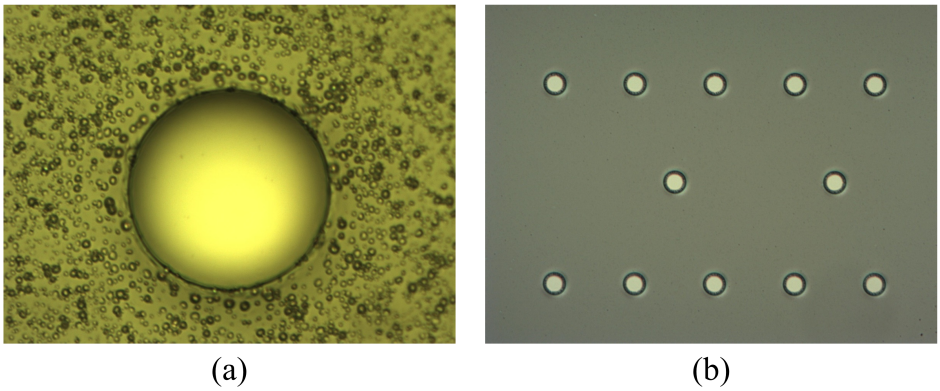


Figure 6.15: (a) 50 times enlarged picture of left side pattern, without post-develop baking; (b) left side pattern after post-develop baking at 180$^{\circ}C$ for 5 mins.

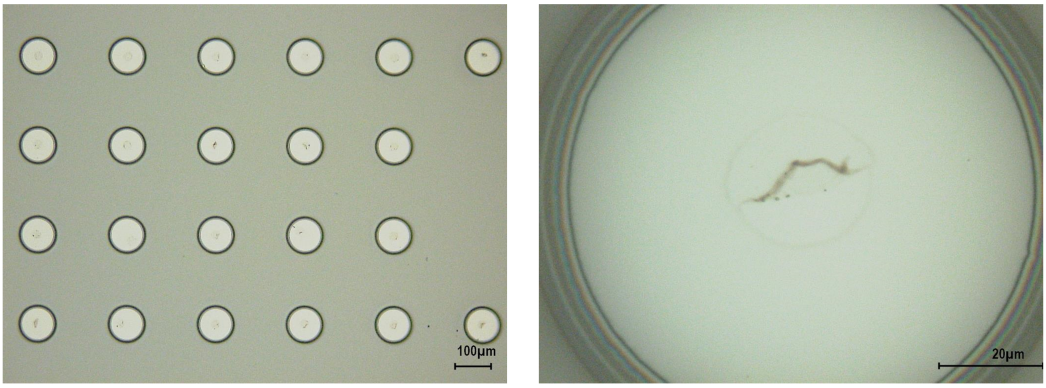


Figure 6.16: High exposure energy test result after development and baking. Left up side pattern exposed by 1500 mJ. (a) 20 times enlarged; (b) 50 times enlarged.

6.4.3 High exposure energy test

To verify if high exposure is better, another four-quarter exposure test is conducted with higher energy, which is 1500 mJ for left-top quarter, 2000 mJ for right-top quarter, 2500 mJ for left-bottom quarter and 3000 mJ for right-bottom quarter. For high energy test, It is firstly noticed that residue remains in the middle of round structure for left up quarter(exposed by 1500 mJ) as shown in Fig.6.16 (a) and 6.16 (b).

Although fewer residues are observed in other three quarters, all four quarters have residue in the round structure. It can be explained that too high energy result to the overexpose of photo resist, part of dark area is exposed and cross-linked, So residue remains on the unexposed area. This phenomena can be further illuminated by narrow line pattern. Fig.6.17 shows the narrow line pattern of left up quarter (exposed by 1500 mJ) and Fig.6.18 shows the line of right down quarter (exposed by 3000 mJ). They shows the top line of line structure, it is obvious that the left up quarter's line is developed well and its width is 25 μm, but right down quarter's line's photo resist is partly exposed and only has a width of 10 μm. Therefore higher energy than 1500 mJ can not be used for exposure of perminex because it causes overexpose for small structure and leaves remaining residue.

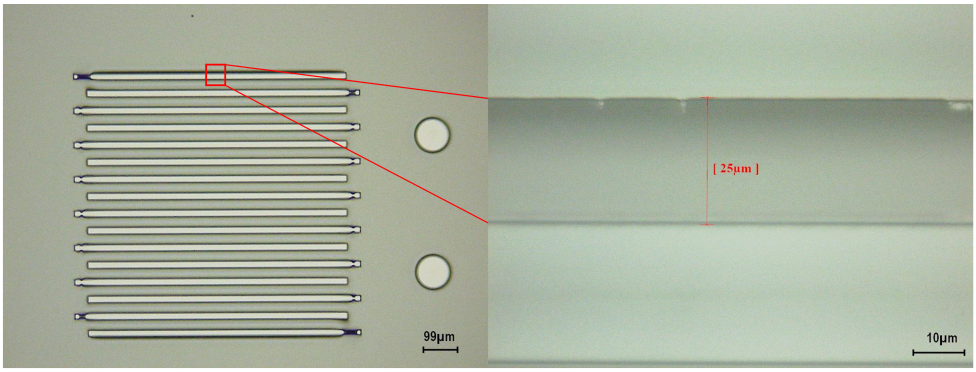


Figure 6.17: Narrow line structure of left up quarter, exposed by 1500 mJ.

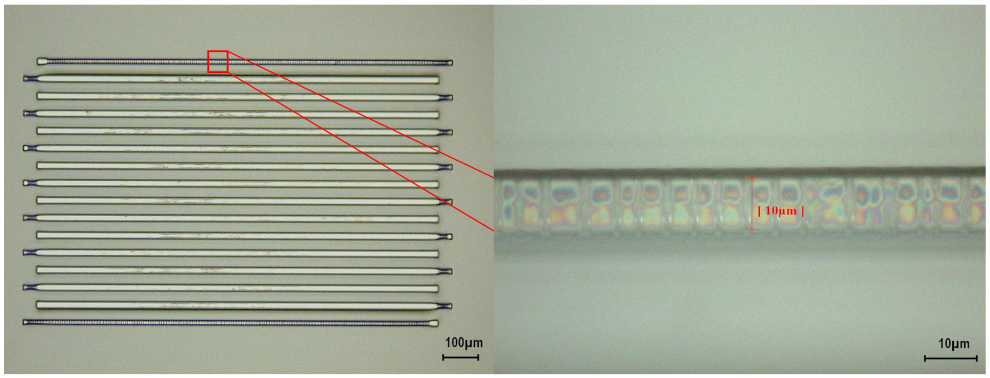


Figure 6.18: Narrow line structure of right down quarter, exposed by 3000 mJ.

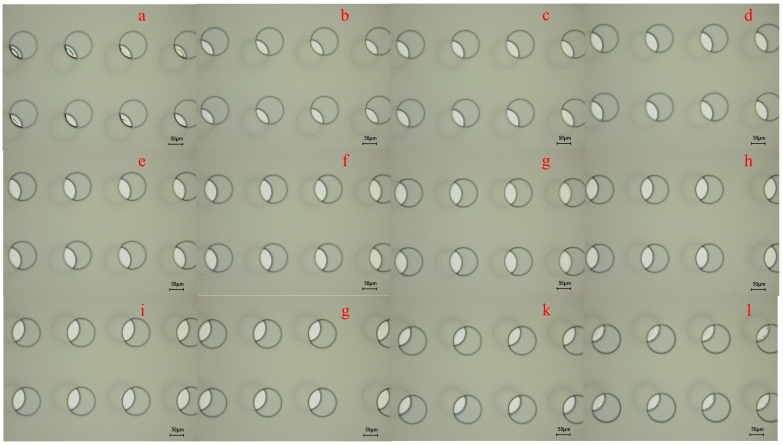


Figure 6.19: Matrix exposure test result for 12XT. Offset is 4 μm, (a) to (l): exposed by 700 mJ - 1800 mJ. Increment is 50 mJ.

6.5 THE SECOND PHOTO RESIST LAYER TEST

The second photo resist layer is needed to be applied on top of perminex undefill layer. For the second photo resist layer, it needs to be removable by normal lift-off process such as heated NMP or acetone bath. A potential candidate is AZ 12XT, which has a measure process to utilize it. For 10 um thick layer, the spin speed is 4000rpm and exposure energy is 170 mJ, offset is 4 μm. Although all the parameters are known for 12XT, it still needs to be tested because it is coated on the perminex pattern. It means 12XT's thickness on the patterned position is thicker than merely one photo resist layer. For example, perminex layer is 10 μm thick, 12XT is applied by 4000 rpm, at the perminex patterned area, the total heightness for coated 12XT is supposed to be 20 μm, therefore, the original exposure parameters are not suitable for current 12XT layer. A similar matrix test is conducted for 12XT, the middle die is set to be exposed at 400 mJ and 4 μm offset. Energy increases by 50 mJ from left the right, offset increase by 1 μm from downside to upside. The result of dies on the middle line (4 μm offset, from 150 mJ to 700 mJ) is shown in Fig.6.19, there is almost now difference for most of the dies. so it can be exposed from 200 mJ to 700 mJ. A middle value 400 mJ is chosen. At the same time, offset test also shows that 12XT is not sensitive to different offset, so 4 μm is chosen for next process.

6.6 CONCLUSION

A series of experiment has shown proper process method for applying perminex and the second photo resist on it. They can be concluded as:

- In Coating test, speed of 4000 rpm result to 17 μm thickness, and 8000 rpm results to 11.33 μm. **8000 rpm is chosen as spin coating speed.**
- In survival test, perminex wafer is processed by ultrasonic bath with 70 $^{\circ}C$ NMP and 35 $^{\circ}C$ acetone. **Perminex layer survive the lift-off process, it can be used as underfill.**
- For minimum energy exposure test, perminex wafer is exposed by a graduated neutral-density filter and 4000 mJ energy, the structure ends at 30, where energy is 1004.8 mJ. Therefore **minimum energy for perminex to be cross-linked is 1000 mJ.**
- In matrix exposure test, perminex wafer is exposed by a matrix exposure job. It is found that **perminex wafer should be exposed by more than 1200 mJ energy, and 0 m offset.**
- In development test and marangoni drying, TMAH and PGMEA are used to develop perminex. Different kinds of material are used to clean developed wafer. The conclusion is that **exposed perminex should be developed by PGMEA, then it should be washed by acetone and pulled out of acetone slowly.**
- In development test after exposure, perminex wafer is exposed quarterly, then it is developed and hard baked. **Wafer should be baked at 180 $^{\circ}C$ for 5 mins after development.**
- High exposure energy test, A quarterly exposure is tested from 1500 mJ to 3000 mJ and **Exposure energy should not be more than 1500 mJ energy.**
- second photo resist layer test, 12XT Exposed by a matrix job with varying exposure energy and offset. Conclusion is **12Xt should be exposed by 400mJ and 4 m offset.**

7 ALL-COPPER INTERCONNECT EXPERIMENT

This chapter describes the fabrication of all-copper combined vertical interconnect/underfill samples for high density I/O flip chip bonding. At first, aluminium wafer is used because it is green metal and its process saves time. several samples are bonded by AML bonder. After verification of bonding process, perminex photo resist is tested and proper process parameters are found. Then copper wafer is used to make samples. AML bonder and pick-and-place machine are both used to bond copper sample.

7.1 FABRICATION OF EXPERIMENTAL WAFER

Aluminium is firstly used for pad metal because it is considered as green metal i.e. it will not affect CMOS device's performance, therefore Al wafer can be processed by automatic machine like EVG 120 Coater-Developer and dry etching machine. Several Al wafer is made as preparation for further process. The flowchart of making bonding test sample is shown in Fig.7.1, although it only includes copper, aluminium's process is the same as long as using Al as metal pad layer. The nanoCu paste is printed by so-called lithographic stencil printing technique.

Because AML bonder's infrared light can not transmit through rough surface. both bottom and top wafer need to be double-polished. So all wafer used in this process is 500mm thick, double polished, p type silicon wafer.

7.1.1 Fabrication of Aluminium sample

Wafers are firstly cleaned HNO_3 (99%) to remove organic particle and then by HNO3 69,5% 110C (Si) to dissolve metal particles. The clean wafer is coated by Shipley 3012 photo resist and patterned with alignment mark for wafer stepper as shown in Fig.7.1 (a).Dry etching is used to etch silicon. To avoid copper diffusion into silicon in the future, silicon nitride is deposited on the wafer by LPCVD using SiH_2Cl_4/NH_3 gas flow. silicon nitride layer's thickness is 300 nm. Then, 300 nm Aluminium layer is deposited on the barrier layer by sputtering. Shipley 3012 is used again to make Al pad pattern, Al can either be dry etched and wet etched. After Al etching, photo resist residue will be removed firstly by plasma etching and then cleaned by cleaning line. With Al pad, bottom wafer can be further processed by coating with 12XT photo resist. 4000 rpm spin speed is used for about 10 μm thick 12XT layer. It is then exposed by 170 mJ, 4 μm offset.

7.1.2 Fabrication of copper sample

Wafers are firstly cleaned and patterned with alignment marker by same process as mentioned above. Then, 300 nm copper layer is deposited on the barrier layer by sputtering. To make copper structure, a Shipley 3012 photo resist layer is coated on the wafer at first. It should be noticed that once the wafer is deposited with copper, it can not be processed in the clean machine any more, which means the follow steps are all run manually. Because copper can build effective recombination centers in silicon, it shortens the minority carrier lifetime and brings significant damage to CMOS device. Therefore, it is forbidden to use normal equipment to process copper wafer in cleanroom, which means almost all automatic equipment

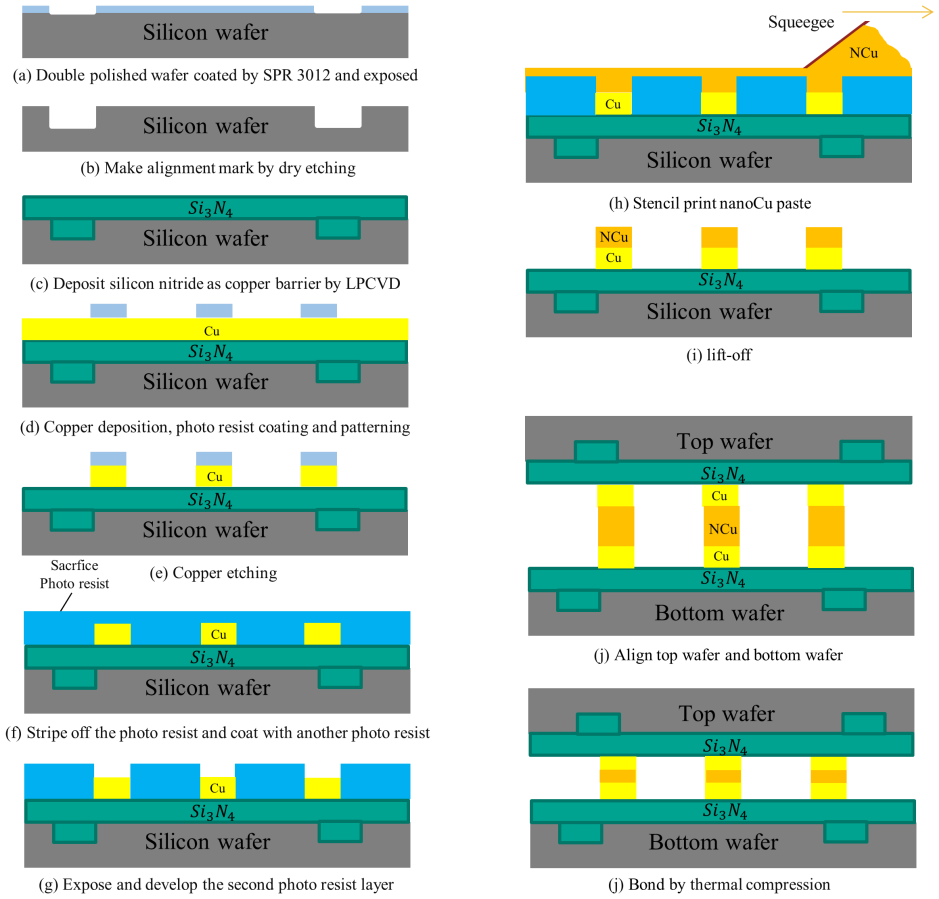


Figure 7.1: Flowchart of sample manufacturing without perminex.

for IC process can not be used for copper wafer test such as coater, developer, cleaning line and so on.

So we use manually coating, developing, cleaning. For exposure, ASML wafer stepper PAS 5500/80 is used because contact aligner can not provide enough accuracy. To avoid contamination, a carrier wafer with holes is used for exposing copper wafer. the carrier wafer has clean backside and dirty front side. After putting it into cassette by clean vaccum tweezer, copper wafer is placed against carrier wafer's front side. Then, manually align their flat side until two wafers completely coincide to each other. After perfectly alignment, two wafers are placed into wafer stepper together. Because Wafer stepper's robotic arm also uses vaccum tweezer to pick up wafer and carrier wafer has several through-holes, the air pressure caused by vaccum can be conducted to contaminated wafer through carrier wafer, two wafers can be holded tight by stepper's arm. Then the top copper wafer with photo resist is exposed without contamination to stepper.

As shown in 7.1 (d), photo resist is developed. With a patterned photo resist layer, copper wafer can be etched now. Since dry etching is not available because copper particle may contaminated the cavity of etching machine, wet etching is used for copper wafer. The etchant solution for copper is: 2000ml $H_2O + 20g$ $Na_2S_2O_8 +$ 5ml H_2SO_4. Etching equipment set is shown in Fig.7.2,

The liquid is placed in glass beaker on a magnetic stirrer. copper wafer is in solution bath with a single wafer tray. During etching, a magnetic bar is constantly spinning in the liquid to ensure good contact between copper and etchant. After about 6 mins etching, it can be observed that copper gradually disappears. But actually there is still remaining copper on wafer in form of small dot, it needs one

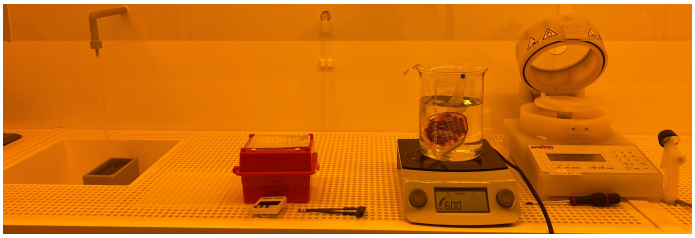


Figure 7.2: Copper etching equipment set.

more minute to totally remove all the copper. So experience etching time for 300 nm copper layer is 7 mins and etching rate is 42.85 nm/min.

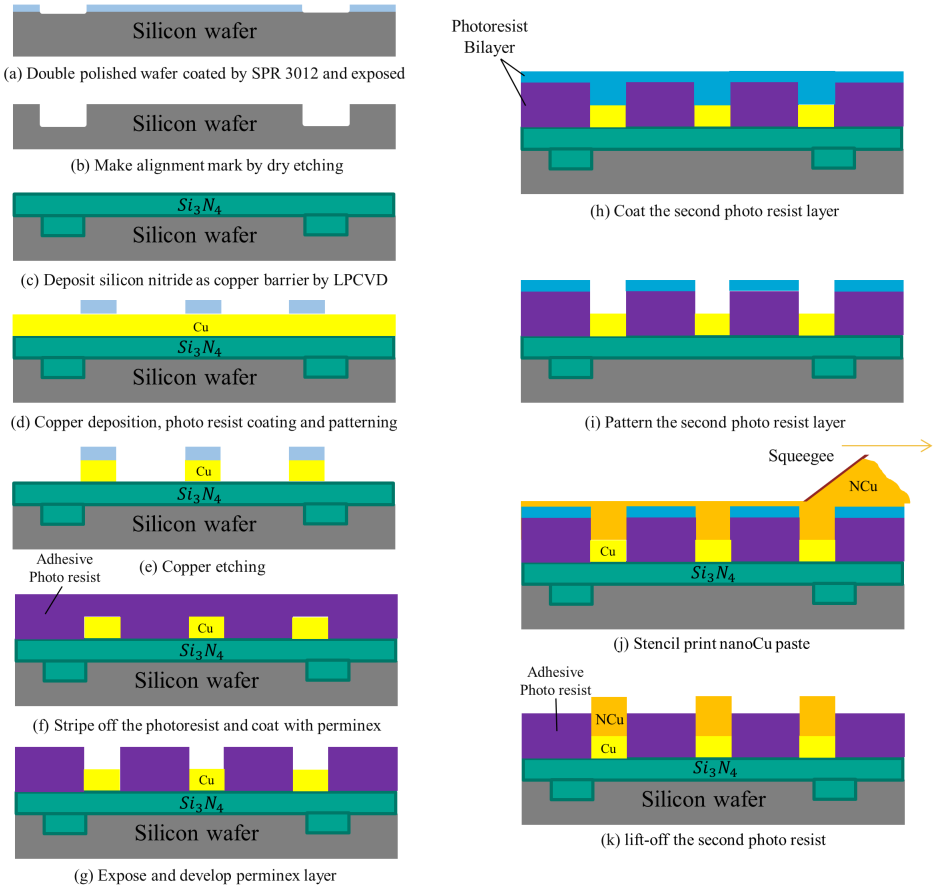


Figure 7.3: Flowchart of sample manufacturing with perminex.

As explained above, top wafer and bottom wafer can have different combination of nanoCu layer. Current experimental setting is that bottom wafer is further processed and printed with nanoCu and the top wafer only has copper pad. So after copper etching, the top wafer only needs to strip off the remaining photo resist and diced for bonding. For stripping, plasma etching is not available because the high temperature and contact to air will cause copper oxidation. Another opinion acid solution treat will also damage copper structure. so it is only practical to use organic compound like acetone and NMP to dissolve the remaining photo resist. Since NMP is more toxic and needs to be heated up to more than 60°C for good performance, but acetone's boiling point is at 56.05°C and it works well at 35°C. It is proved in practice that 35°C acetone with ultrasonic bath has a good performance to remove photo resist residue within 5 mins. After acetone bathing, IPA and DI water is used to further remove residue. In general, heated acetone with ultrasonic bath is very suitable to strip off normal photo resist and clean copper wafer. Cop-

per wafer remained for a long time also can be cleaned by this method. For copper wafer without perminex, the following process is the same as Al sample.

For copper wafer with perminex, the renewed flowchart is shown in Fig.7.3. After cleaning, as shown in 7.3 (f), bottom wafer with copper pad is coated with perminex. As explained in previous chapter, it is firstly spin coated under 8000 rpm speed to form a 11 μm layer. Then a soft bake at 95°C for 10 mins is applied. Next, the wafer is exposed by 1300 mJ with 0 μm offset in wafer stepper. Then wafer is post exposure baked at 70°C for 2 mins. The development is finished with PGMEA for 5 mins - 10 mins, then remove PGMEA by marangoni drying with acetone. At last, a post-develop bake at 180°C for 5 mins is applied. The result is described in 7.3 (g). Next step is apply the second photo resist layer as sacrifice layer to remove nanoCu residue. AZ 12XT is chosen and it is exposed by 400 mJ with 4 μm offset. The other process is the same as wafer without perminex. With two photo resist layers, bottom wafer in current case is ready to be printed with nanoCu paste.

7.1.3 NanoCu paste printing

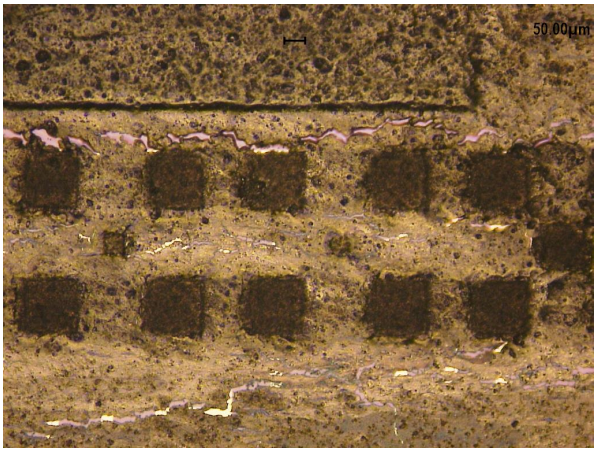


Figure 7.4: Result of nanoCu paste printeing.

As shown in 7.3(j), stencil printing is used to apply nanoCu paste on the wafer. The Bi-layer photo resist on the wafer acts as stencil. NanoCu paste is sticky and easy to be spread, a squeeze with flat edge can push and extrude paste into stencil. Since nano particle is extremely small, an extremely flat edge is required for squeeze. Normally edge fabricated by mechanical dicing is too rough to be used for spreading nano-scale material. At the same time, the normal used silicon wafer is a good choice, because it can be broke along certain crystal orientation. The wafer we usually use is (100) wafer, which means the (100) plane of silicon crystal is parallel to the wafer's smooth surface, the biggest flat edge is called primary flat, which is ¡110¿ plane for 100 wafer. Because (110) plane's density of surface bonds is smaller than (100) plane's, once imposed force on a crack, the wafer will cleave at 90 degree angles i.e. the cleaved pieces will form a sharp and straight edge. because cleave forms along the crystal orientation, the edge is smooth in atomic level.

In practice, diamond pen is used to make a small crack on the primary flat, then slightly apply force on one side of wafer, it will cleave easily along with smooth edge. 60 degree is a good choice for the angle between wafer and squeeze. hold the squeeze steadily and slowly print nanoCu paste from left to right, To avoid bulge on one side, another print from right to left is necessary. Since wet paste is easy to fall off from copper pad, a drying at 80 °C for 10 mins is applied after printing. To further improve flatness of nano paste in contact opening, a second round of print and drying at 120 °C for 15 mins is applied. The result is shown in Fig.7.4.

According to several printing test, it is considered that copper pad has been oxidized during applying two photo resist layer because photo resist process includes high-temperature baking in the air. At the same time, copper is very easy to be oxidized by air under high temperature. Therefore, to remove copper oxidation and increase the adhesion between copper pad and nanoCu, a 1-min copper etching is applied before nanoCu printing.

7.2 LIFT-OFF PROCESS AND ITS IMPROVEMENT

The next step is to remove the second photo resist layer and unwanted nanoCu residue as shown in Fig.7.3 (k). Since drying is applied, nanoCu paste has been solidated and stick to other inside parts. Lift-off can also strip off nanoCu in the contact opening if they stick to residue. At the same time, nanoCu itself does not have any adhesion to copper pad before sintering, and it is the organic compound in paste help them stick to substrate. If solvent of lift-off process is too intense, nanoCu paste will also fall off from copper pad. By using 70 $^{\circ}C$ NMP for 1 minute, nano paste is already unable to stay on the pad.

It is found that NMP at 70 $^{\circ}C$ is too intense to keep nanoCu on the pad. Acetone is chosen as a substitute. with ultrasonic bath, nanoCu pattern can be more explicit because ultrasonic wave can affect all photo resist at the same time. because the first perminex layer has 11 μm thickness and has bulge effect around small contact opening, the second photo resist layer is also not flat in the area around the opening. Therefore liquid solvent can not lift-off the photo resist in a same rate. bulge effect is stronger around small opening than bigger opening. Therefore, it is decided that conducting lift-off process with ultrasonic bath.

By same time, photo resist around bigger opening is just lifted off but nanoCu in small opening has already been removed by solvent. With intense solvent, it is hard to find a proper time window which can keep both small and big structures. So a mild and uniform lift-off solvent is needed. acetone at room temperature is too weak to rapidly solve photo resist, So it is heated upto 35 $^{\circ}C$ to enhance the capacity to solve. Experimental result shows that 35 $^{\circ}C$ acetone with lowest power ultrasonic bath works well for lift-off.

The profile of several structure after nano Cu printing is shown in Fig.7.5-7.7, the dektak's stylus moves from up side to down side of transmission line. The profile is irregular and shows that the up side and down side are high and the middle is low. The rough surface may cause to incomplete contact between nanoCu and bulk Cu pad. Therefore, the contact resistance of pads and sheet resistance between pads transmission may varies mainly due to printing result.

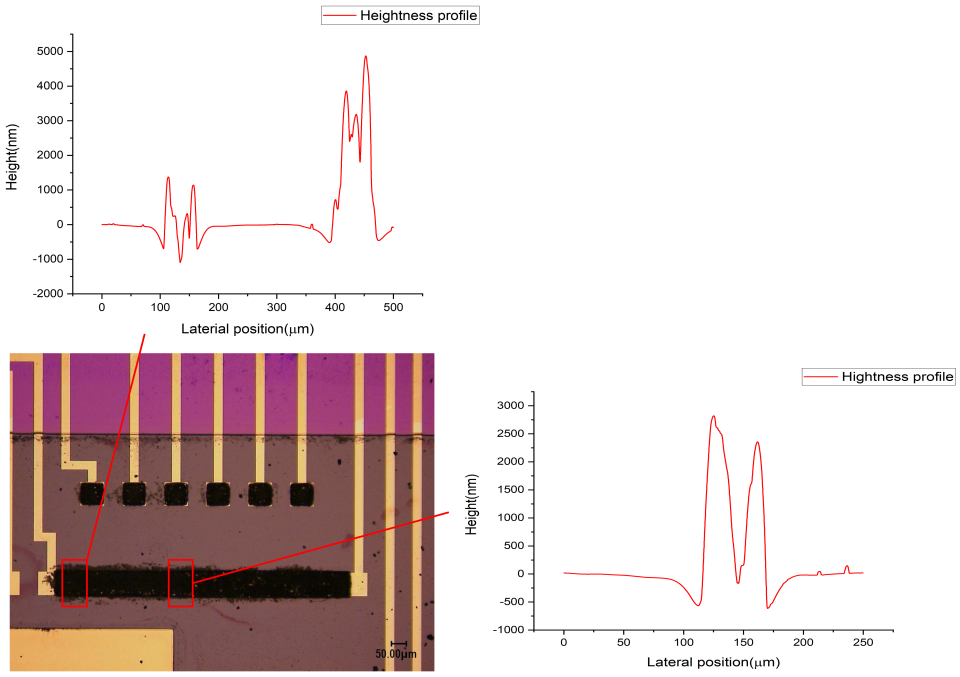


Figure 7.5: Heightness profile of transmission line after nanoCu printing.

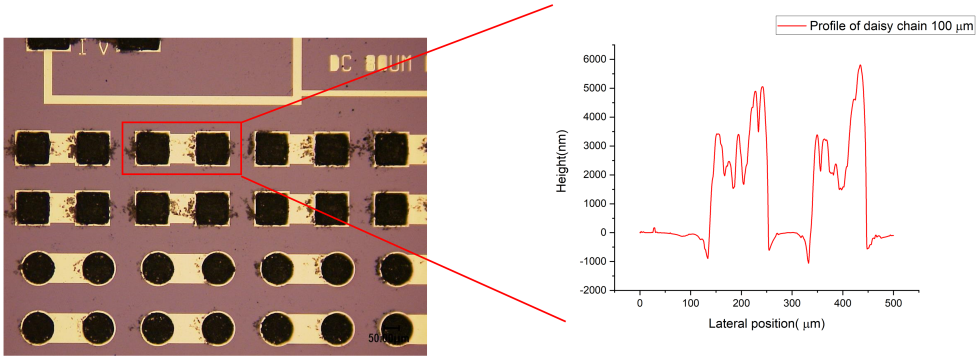


Figure 7.6: Heightness profile of 100 μm daisy chain pads after nanoCu printing.

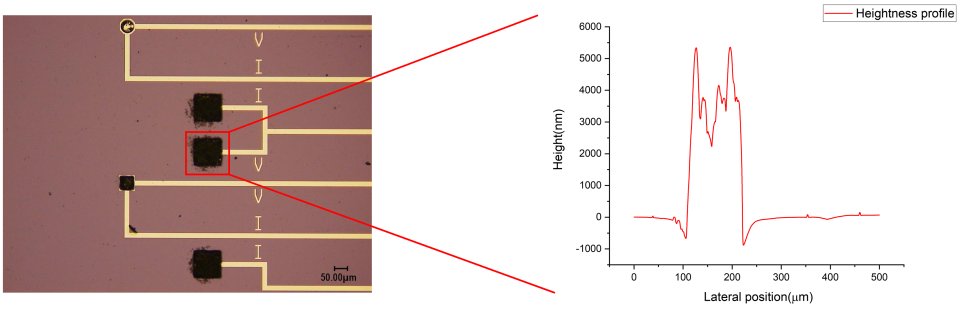


Figure 7.7: Heightness profile of chip to chip structure pad after nanoCu printing.

7.3 BONDING PROCESS

Once bottom wafer with nanoCu pattern and top wafer with copper pad are prepared, bonding process can be started. A Schematic of bonding is shown in Fig.7.8, as applying high temperature and pressure, nanoCu would be compressed and sintered. The sintering result is significantly related to pressure and temperature.

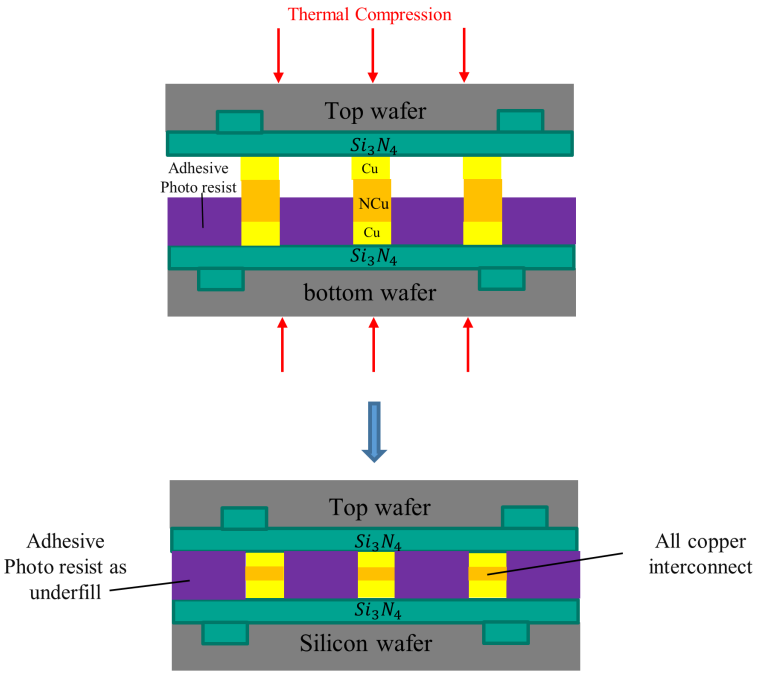


Figure 7.8: Schematic of bonding process.

7.3.1 Bonding by AML bonder

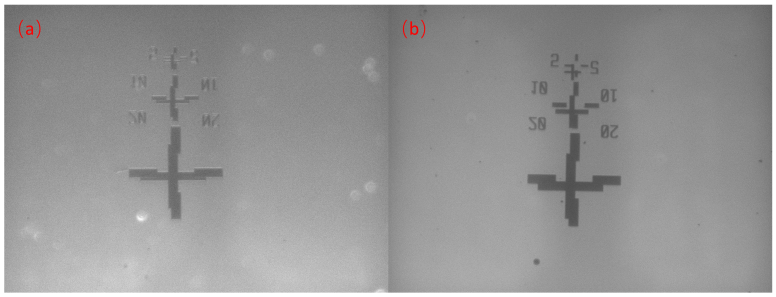


Figure 7.9: Infrared image of alignment mark while bonding. (a)left camera; (b)right camera.

After placing a whole wafer sample on the lip and dicing sample on movable plate, AML bonder's lip will be closed. four screws on lip are tightened and vacuum pump is started. As illustrated before, there is alignment marks on both bottom and top wafer for infrared alignment. By controlling moving plate to overlap two alignment marks, two wafers' position can be calibrated. An example is shown in Fig.7.9, since there is always displacement in X and Y axis while lifting up plate, for the best circumstance, misalignment is less than 20 μm. Once top and bottom samples are aligned and contact each other, force can be applied on the sample,

Now there is a small question need to be figured out, for nanoCu sintering research, pressure is a key experiment parameter, AML bonder can only provide

force, according to our classical *Pascal'slaw*, pressure is the force divided by area. The ideal situation is the force is all applied on nanoCu area, which is about 1.08×10^{-6} m^2, if pressure is set as usual 10 Mpa, the force is only about 900 N.

So at first 900 N is applied for one of the aluminium experiment, $280°C$ is set for temperature because it is enough for nanoCu sintering. When lip is open, it is found that the adhesion is too poor to bond two wafers together, they splited up while the sample was taking off from plate as shown in Fig.7.10.

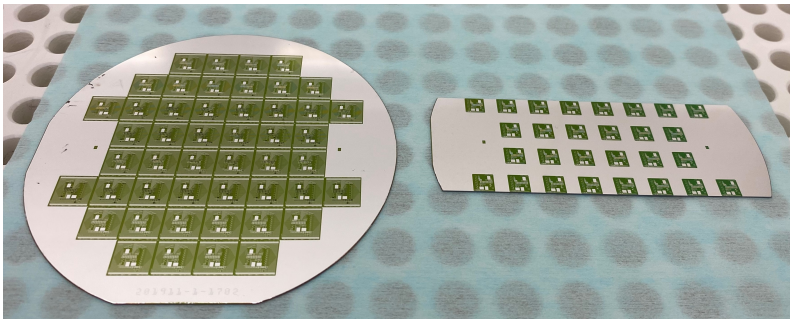


Figure 7.10: Samples bonded by 900N force at $280°C$, sample splits up.

To solve poor adhesion problem, higher force is applied for new samples, 4000 N is a usual working force for AML bonder, So two copper sample are bonded by 4000N force at $280°C$, this time sample bonded to each other but it is still easy to split up. A successful sample is shown in Fig.7.11

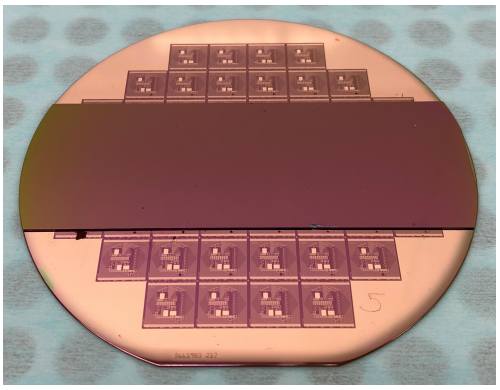
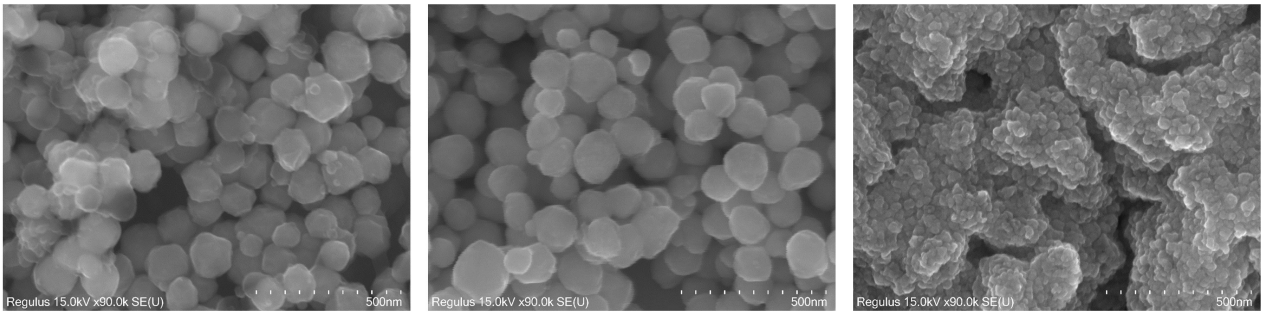


Figure 7.11: Samples bonded by 4000 N force at 280 $°C$, sample is bonded.

Above result shows that the assumption is wrong, therefore contact area is not only nanoCu contact area. it is also reasonable because manual printing can not ensure the flatness of nanoCu paste, bulge effect is serious for manually-made sample. At the same time, nanoCu paste is full of organic filling, at high temperature, it could evaporate and paste volume will decrease, profile measurement of lift-off result in Fig.7.5-7.7 can show extremely uneven surface. So under high pressure and temperature while bonding, the paste can be compressed and nanoCu pillar will collapse, then all top wafer will contact bottom wafer, so now contact area becomes to whole top wafer, which is about 0.0026 m^2. Under this consumption, 900N force can only provide 0.35 Mpa pressure and 4000N can provide 1.5 Mpa pressure.

SEM image can illustrate the reason why the adhesion is so poor. A comparison of original nanoCu paste, paste sintered by 900N force and paste sintered by 4000N force is shown in Fig.7.12, it is clear that nanoCu particle under 900N force has not significant melt and fusion phenomenon compared to original particle, while particle under 4000N force shows notable sintering result. particles gather together and become to smaller particles. Explicit fusion is observed in Fig.7.12(c), although sintered structure is full of pores, it still can provide enough adhesion.



(a) (b) (c)

Figure 7.12: Comparison of nanoCu sintering result, (a) Original nanoCu paste; (b) NanoCu sintered by 900 N force, 280°C;(c) NanoCu sintered by 4000 N force, 280°C.

7.3.2 Bonding by pick-and-place machine

Pick-and-place machine can provide high temperature and force upto 6000g(58.8N). Different from AML bonder's sample, this machine can align two dies by optical camera. So for sample preparation, bottom wafer is made with perminex. it is then diced into 10 mm $\times$ 10 mm dies. Top wafer still only contains copper pad and it is diced into 6 mm $\times$ 6 mm dies. Therefore contact area is supposed to be 6 mm $\times$ 6 mm = 3.6×10^{-5} m^2. Under 60 N force, the maximum pressure this machine could provide is 1.67 Mpa.

Since it can only provide 1.67 Mpa pressure by merely using pick-and-place machine, which is slightly larger than 1.5 Mpa provided by AML bonder, experiment's result is not expected to be different from previous data. But as epoxy resin, perminex layer becomes to be adhesive at 100°C, while 100°C is low enough to avoid sintering of nanoCu. So pick-and-place machine can be used to align and preliminary bond samples without real sintering, then, bonded sample can be further thermomechanically bonded by AML bonder. At the same time, although there is nitrogen nozzles, pick-and-place machine does not have a sealed chamber for bonding to prevent air, which may cause serious oxidation of sample. Therefore, a proper process is firstly bonding sample by pick-and-place machine at 100 °C by proper force, then further bonding sample in AML bonder by higher force. For normally used 10Mpa pressure, about 360N force is needed for current sample. A bonded sample is shown in Fig.7.13

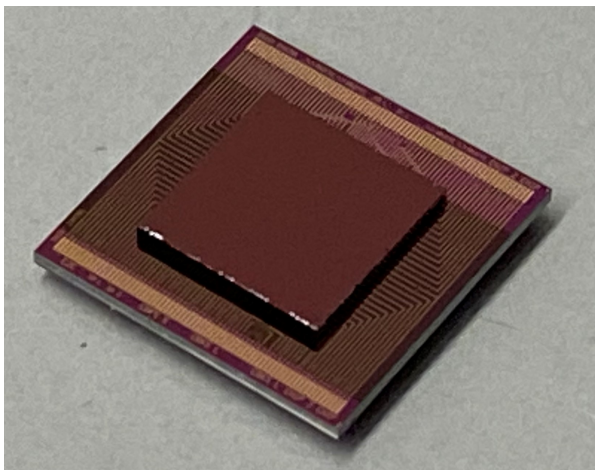


Figure 7.13: Sample bonded by pick-and-place machine.

7.4 ELECTRICAL CHARACTERIZATION

Electrical characterization is conducted for a series of bonding samples. Sheet resistance and contact resistance are tested for different bonding temperature and pressure.

7.4.1 Sheet resistance

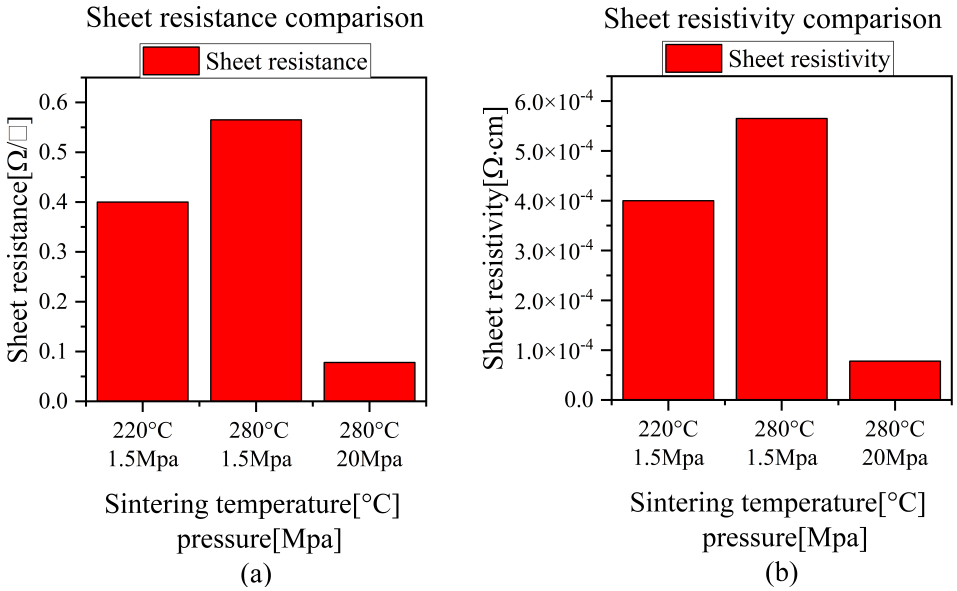


Figure 7.14: (a) Sheet resistance comparison; (b) Sheet resistivity comparison.

Several greek crosses are placed on test die. The raw measurement result is shown in Fig.7.14 (a), different temperature and pressure are tried for nanoCu sintering.

According to profile measurement, the average thickness is calculated as 10 μm, therefore sheet resistivity can be calculated, and it is shown in Fig.7.14 (b). The bulk copper's sheet resistivity is about $1.7 \times 10^{-6} \Omega \cdot$ cm, while for sample bonded by 1.5 Mpa, sheet resistivity is more than $4 \times 10^{-4} \Omega \cdot$ cm, which is more than 200 times larger than bulk copper. It can only be explained that 1.5 Mpa is not enough for nanoCu sintering. High resistance results from uneven printing result and cavities in sintering result. It can be clearly observed in Fig.7.15 that sintering result for $280°C$, 1.5 Mpa sample is full of ravines and pores. Only few thin copper interconnects are able to conduct current.

While sample bonded by much higher pressure shows massively decrease for resistance. For sample bonded by 20 MPa, sheet resistivity decreases to $7.8 \times 10^{-5} \Omega \cdot$ cm, which is about 45 times larger than bulk copper. Lower resistance indicates that high pressure results to better nanoCu sintering result and it can be concluded high pressure is necessary for nanoCu's fully sintering.

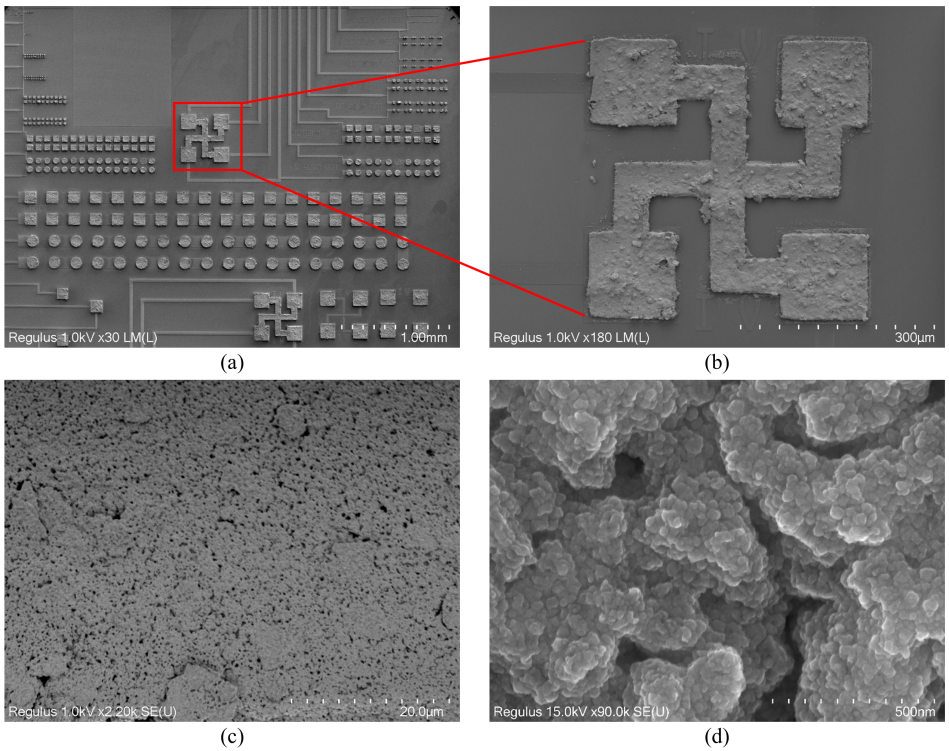


Figure 7.15: SEM picture of greek cross for sheet resistance on sample bonded by 1.5 Mpa, at 280°C. (a) enlarged 30 times; (b) enlarged 180 times; (c) enlarged 2200 times; (d) enlarged 90000 times.

7.4.2 Contact resistance

Contact resistance has been measured by a sample with perminex bonded by 4000N force at 220 $^{\circ}C$ firstly, a lower temperature 220 $^{\circ}C$ is chosen because it is uncertain that perminex can stand higher temperature. After measurement, sample is bonded again at 300 $^{\circ}C$ by 4000N. Multiple structures are measured including 50 μm and 100 μm size cross bridge kelvin resistor, daisy chain and TLM. The measurement result are shown in Fig.7.16. It should be noticed that this sample is bonded by AML bonder, which has 20 μm misalignment for all the sample. The Common

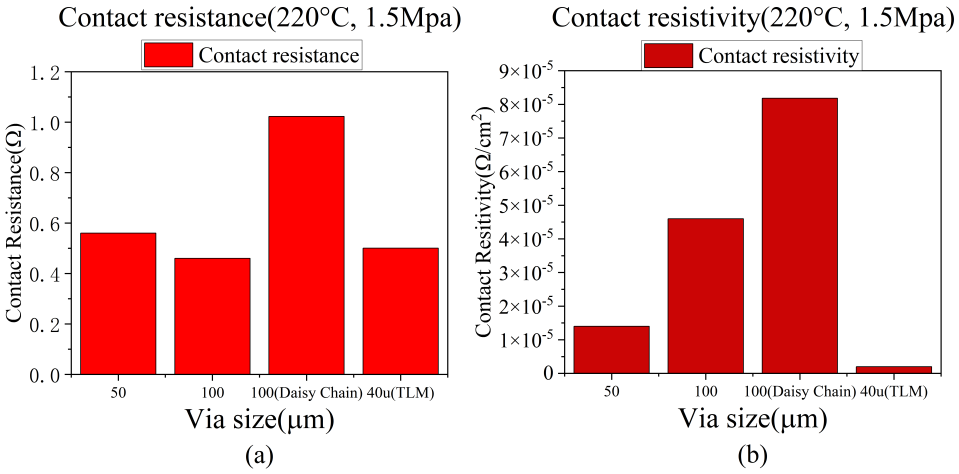


Figure 7.16: Contact resistance measurement result of different structures, sample bonded by 1.5 Mpa at 220°C. (a) Contact resistance; (b) Contact resistivity.

sense is that kelvin resistor with larger via size has smaller contact resistivity i.e. smaller average resistance because larger contact area is easier for current to flow through. But in Fig.7.16, it is observed that 50 μm via's resistivity is even smaller that 100 μm's. This abnormal phenomenon can be explained by profile measurement shown in Fig.7.5-7.7, It is clear that nanoCu paste does not have a flat profile before bonding, larger via like 100 μm has steep bulges around via edges. During thermocompression bonding, these bulges will collapse and caused to a bunch of cavities and real contact area of via is may smaller than 50μm via's.

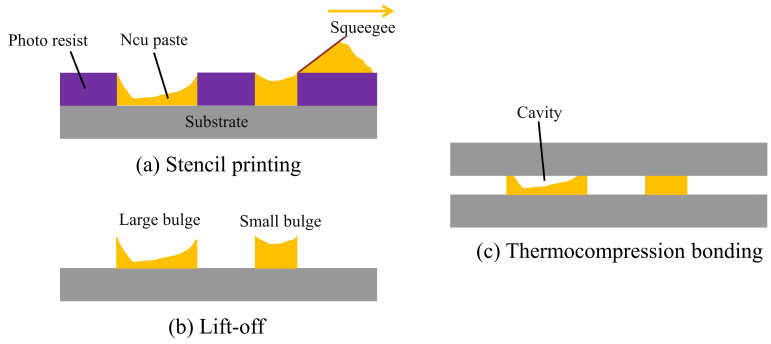


Figure 7.17: Illumination of via size and bulge effect.

Fig.7.17 illustrates the bulge effect, Fig.7.17 (a) is stencil printing step. because larger via has a larger width, squeeze movement can more easily leave higher paste bulge in the via, then in Fig.7.17 (b), photo resist stencil is removed by lift-off, nano paste bulk with bulge is kept on substrate. In Fig.7.17 (c), another sample is bonded to previous one by thermocompression. large bulge will cause to lager cavity inside

the interconnect, therefore result to smaller contact area for current flowing. As a result, larger 100 μm via has a bigger resistivity than 50 μm via.

Daisy chain on the sample has 18 dog bone structure and 36 viasit is considered that cumulative misalignment caused to higher measurement result compared to other structure. For TLM structure, although it has smaller contact area, a continuous nanoCu line ensures effective contact area, therefore, measured contact resistivity for TLM is smaller instead.

Fig.7.18 shows the comparison of contact resistance measurement result for different pressure and temperature. it should be noticed that 10 Mpa sample is made by pick-and-place machine and further bonded by AML bonder as illustrated previous. It is clearly seen that as temperature and pressure increasing, contact resistance decreases significantly. It can be concluded that both temperature and pressure have an effect on nanoCu sintering result. Higher temperature and pressure can force nanoCu melting and sintering better, as a result, good contact is formed and smaller contact resistance is measured.

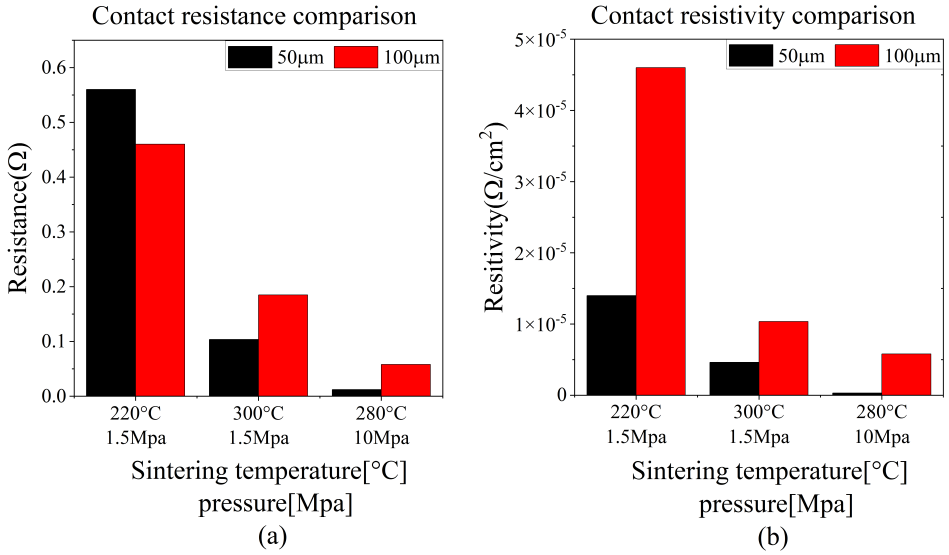


Figure 7.18: Comparison of contact resistance measurement result for different pressure and temperature. (a) Contact resistance. (b) Contact resistivity.

8 CONCLUSION AND OUTLOOK

8.1 CONCLUSION

An all-copper fine pitch bonding process with photoimageable underfill is successfully developed. It takes a lot of efforts to explore how to correctly processing copper wafer, Main steps includes exposure with carrier wafer, which need great patience to align two wafers properly, sometimes misalignment can result to time-consuming error of wafer stepper. Copper etching is another key step. when wafer is in the etchant solution, observation by eyes can not distinguish micro-size residue of copper, wafer should be dried and observed by microscope.

Application of photoimageable underfill perminex is a main challenge of this project, as a new photo resist, all process parameters need to be decide by experiment even though there is data sheet reference. Experiment result shows that its characteristics are quite different from describtion of data sheet. By multiple different exposure and development test, it is finally applied to all-copper fine pitch bonding process, the application of perminex significantly increases adhesion and enable sample to be bonded by pick-and-place machine. A new mask is designed to process negative tone photo resist perminex. Half wafer to whole wafer bonding is firstly realized by sample without perminex, special alignment mark for AML bonder is added into exposure job. Infrared light camera of AML bonder is used to adjust position of sample until alignment marks overlap each other. However, due to uncontrollable vibration and shift of AMl bonder's movable plate, 20 μm displacement is unavoidable between top wafer and bottom wafer. Electrical measurement is also affected by misalignment.

Later bonding by pick-and-place machine is successfully realized. This method is more practical than AML bonder method. At first, only two dies are needed to compose a measurable sample, which significantly increases the yield. Every die on bottom wafer now can be taken advantage and top wafer can be exposed more compact and yield more dies at once. At the same time, because now bottom die is only covered by a top die, both top and bottom measurement pad can be utilized, all structures can be measured now. Compared to AML bonder method, it saves a large amount of effort and wafer. For old method, two wafers are consumed for only once bonding, only top pad line of top die line and bottom pad line of bottom die line can be measured. In a word, most parts of treasure wafer are wasted. Pick-and-place method perfectly solves this problem. At the end, with perminex underfill layer, pick-and-place method can be extended, samples can be firstly aligned and bonded at a relatively low temperature, then further bonded by much higher force via AML bonder. By the extended method, number of experiment parameter choice is extensively enlarged, more combination of pressure and temperature can be tested now.

In conclusion:

- A photoimageable photo resist with high resolution is successfully applied as adhesive underfill, adhesion is significantly improved.
- NanoCu paste sintering enabling all-copper interconnect is realized.
- A novel photo-patternable self-aligned underfill is combined with photolithographic stencil printing.

8.2 OUTLOOKS

It is worthwhile to make this all-copper fine pitch bonding process more mature by several valuable ideas in the future.

- Exposure job can be further modified, addition alignment mark can be added into reserved area. misalignment around 5 μm is expected by using specific alignment mark to align instead of test structure.
- More nanoCu sintering experiment can be conducted, a promising direction is to find optical sintering pressure and temperature while nnaoCu interconnects show relatively low resistance.
- Mechanical property of brand new photoimageable underfill sample can be learnt by shear test. Firstly, it is meaningful to compare mechanical strength between sample with perminex and sample without perminex. Also, it is worthwhile to test bonding strength after thermal cycles in order to learn its reliability after long time and under extreme environment.
- Different photo resists can be tested as substitution of current material used in process. For example, SU-8 can replace perminex since they are both based on epoxy resin. Also, SPR3012 can replace 12xt because it can be coated thinner than 12XT, therefore it is easier to be removed and may leave less residue.
- Polisher can be used to remove the second photo resist layer and residue on it.

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