A 10-mV-Startup-Voltage Thermoelectric Energy Harvesting System Based on a Piezoelectric Cold Starter

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by

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Abstract

Traditional power batteries have been unable to meet the requirements of wireless sensor network (WSN) applications which require battery lifetime and no battery replacement. So, harvesting ambient energy and converting it into electrical energy to power wireless sensors has become an alternative to the traditional power sources. Harvesting energy from heat using thermoelectric generators (TEG) has become a prevalent topic in recent years. Since the system is required to startup with zero energy stored, the cold startup technique is necessary to activate the operation of the system in the very beginning stage without any assistance from the energy storage block, for instance, battery and capacitor. It is noted that any machines that moves, shakes, or rotates not only dissipate heat while working but also vibrate, thus the mechanical vibration can be used to startup the system. In this thesis project, a novel piezoelectric generator (PEG) startup technique is proposed to activate the system. This project focuses on pushing the minimum startup TEG voltage to an ultra-low level with the help of the PEG startup circuit.

The design of the system follows the top-down approach. Firstly, the inductive DC/DC boost converter was chosen to be the basic topology. Then, the Maximum Power Point Tracking (MPPT) technique is exploited to make sure the TEG always works at its optimal state. In addition, a Zero-current Switching (ZCS) block is proposed to regulate the synchronization of the switches and control the gate switching. Next, the state detector block monitors the state of the harvester system and instructs other control circuits to respond to the changes in the operation state. To avoid the impact of the fluctuation of supply on powering internal control circuits, a low-dropout regulator (LDO) is adopted to generate a stable supply instead. Finally, the power losses, conversion efficiency and startup principle are analysed and calculated for performance improvement.

In the last section of this project, the harvesting system was implemented in an 180-nm CMOS process, occupying an area of 0.4 mm^2. The measurement results show that a minimum startup voltage of 10 mV is achieved thanks to the PEG starter. Compared with the state-of-the-art designs, this work also achieves an relatively high energy harvesting efficiency of 63.9% at the minimum TEG voltage. The peak efficiency of the system is 82.7%, achieved with 55 mV TEG voltage.

Keywords: Thermoelectric energy harvesting, piezoelectric generator (PEG), thermoelectric energy generator (TEG), DC/DC converter, cold-startup, maximum power point tracking (MPPT).

Acknowledgments

Time flies, and it is approaching the end of my master's studying in TU Delft. Now, it is a great time to look back at what a wonderful time and unforgettable experience I had. In these two years, I have met so many kind and incredible persons, some of them are teachers, and some are colleagues and friends. I am very grateful for the opportunities that have been presented to me, which will be something I treasure for the rest of my life.

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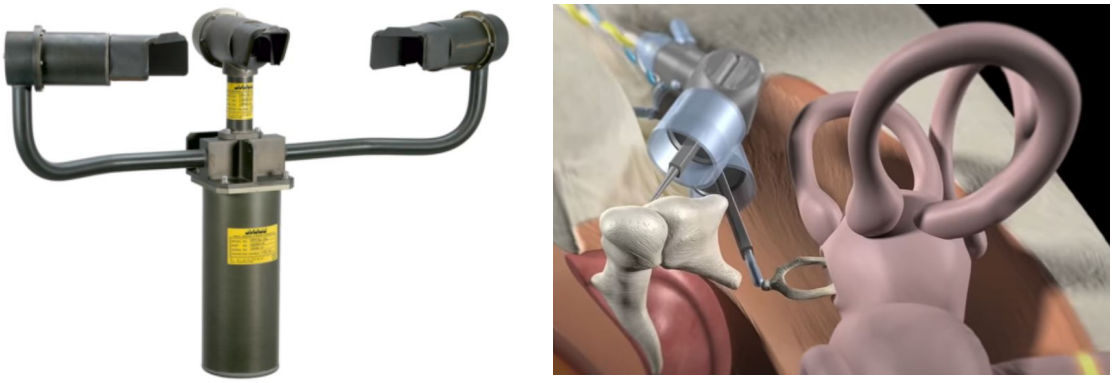
Contents

1 Introduction

1.1 Background

With the research and development of the Internet of Things, wireless sensor network related applications and products have begun to enter commercial market and daily life, especially in medical, military, environmental and other fields [1]. For example, nature monitoring technology uses a variety of sensors to collect weather conditions and real-time information about natural disasters, as shown in Fig. 1.1a, including flood disasters or forest fires. It is often used in harsh environments that cannot be monitored by humans, and it is not easy to manually replace equipment batteries. There are also implantable medical devices that can monitor the health conditions inside the human body, as shown in Fig. 1.1b. But the replacement of the battery of the implantable device is also a big difficulty. For instance, to replace the battery of pacemaker, a surgery with all corresponding risks is necessary. So, the power supply often becomes the biggest problem in the operating lifetime of these devices [2, 3]. Traditional batteries have great limitations, such as small charge storage, short working time, battery replacement, safety concern and other issues. These drawbacks affect the operating lifetime of sensors and cause high operating and maintaining costs. Therefore, how to solve the drawbacks of traditional batteries and achieve long-term stable power supply for low-power miniature wireless sensors has become a popular topic in current research.

In recent years, the researchers have turned to exploit the energy stored in the environment to avoid the issue caused by battery replacement. Consequently, the energy harvesting technique starts to draw more and more interests.



(a) (b)

Figure 1.1: (a) Weather sensor [4]. (b) The cochlear implant [5].

Energy harvesting refers to the process of extracting energy from an ambient source and converting it into electrical power. Two things are fundamentally required for this transformation: an ambient source with a relevant amount of available energy and a harvesting device capable of facilitating this transformation with a relevant efficiency. Solar energy, RF energy, thermal energy and kinetic energy are most common available resources in the surrounding environment which are easily to harvest and used to power the devices. A table of these sources with corresponding power density is given in Tbl. 1.1. Direct sunlight outdoors has by far the most harvestable energy of any of these sources. Furthermore, the photoelectric conversion technology is relatively mature, so this energy can be harvested at high efficiencies, making solar energy harvesting an excellent alternative power source. However, the main disadvantage of this energy source is that it is too weather dependent. In an environment with weak light intensity such as on rainy days or indoors, the available power rapidly drops. Technologies that harvest energy from RF electromagnetic radiation, such as radios, are capable of powering the electronics. The availability of harvestable energy, on the other hand, is highly dependent on the distance to the source and the broadcast power. Due to regulatory restrictions on RF energy broadcasting, this method of harvesting is only suitable for extreme-low-power applications. To decide the energy source for harvesting, the most efficient and direct way is evaluating its working environment. It is worth noting that vibration and heat are generated together in lots of scenarios. For example, the engines of airplanes and vehicles generate a lot of heat while working. Besides, they also vibrate. The human body is an ideal thermal source with stable available heat. Also, the movement of the human body is usually continuous. Therefore, they are ideal thermal sources to power the wireless sensors mounted on them. Meanwhile, the periodic kinetic vibration energy can be collected together.

Table 1.1: Comparison of power densities and output voltage of various energy sources [6]

Energy source	Harvesting condition	Power density	Output voltage
Solar	Outdoors (100K Lux)	10-50 mW/cm^2	0.25-5 V
	Indoors (100 Lux)	10-50 $\mu W/cm^2$	
RF	GSM (900 MHz)	0.8 $\mu W/cm^2$	0.5-5 V
	WIFI (2.4 GHz)	0.01 $\mu W/cm^2$	
Kinetic	Human body (Hz)	4 $\mu W/cm^2$	15-100 mV
	Machine (KHz)	400 $\mu W/cm^2$	1-5 V
Thermal	Human Body ($\Delta T = 5K$)	5 $\mu W/cm^2$	10-50 mV
	Machine ($\Delta T = 100K$)	500 $\mu W/cm^2$	0.1-5 V

1.2 Thermometric Energy Harvesting

1.2.1 Thermoelectric Effect

The thermoelectric effect is the direct conversion of temperature differences to electric voltage and vice versa via a thermocouple[7]. It mainly encompasses three separately identified effects: the Seebeck effect, Peltier effect, and Thomson effect. The Seebeck and Peltier effects are complementary manifestations of the same physical process which describe the conversion from temperature difference to electricity and the conversion from electricity to temperature difference, respectively. The Thomson effect represents the thermoelectric effect in a single uniform material.

In the field of energy harvesting, the Seebeck effect is widely used. It refers to the diffusion of electrons on the contact surface from high concentration to low concentration when two semiconductors (or metal conductors) with different free electron densities (or carrier densities) in a temperature difference environment are in contact with each other. And the diffusion rate of electrons is proportional to the temperature difference in the contact area. The specific phenomena is that the carriers in the semiconductor diffuse from the hot end to the cold end, so that a potential difference is generated between the cold and hot ends of the semiconductor material. Therefore, the Seebeck effect of semiconductors can be used to design thermoelectric generators (TEG).

1.2.2 Working principle of TEG

The internal carriers of the P-type semiconductor are mainly holes, so when there is a temperature difference between the two ends of the P-type semiconductor, the holes will diffuse to the cold end, so that the hot end of the P-type semiconductor is negatively charged, and the cold end is a positive charged. At this time, an electric field appears inside the P-type semiconductor, and its direction is from the cold end to the hot end, as shown in Fig. 1.2. When the drift effect and the carrier diffusion effect in the electric field cancel each other out and reach a balance, the electromotive force caused by the temperature gradient is generated at both ends of the semiconductor. The internal carriers of the N-type semiconductor are mainly free electrons, so the generated electromotive force is opposite to that of the P-type semiconductor. The hot end is positive charged, and the cold end is negative charged. If the N-type semiconductor and P-type semiconductor are connected in series, the electromotive force is also connected in series, which can increase the electromotive force.

1.2.3 Thermal Model and Equivalent Circuit of TEG

A heat transfer model based on the wearable applications on human body is constructed in [9], which can be easily extended to thermoelectric energy harvesting studies under other environments. The TEG is composed of multiple sets of thermocouples and frame

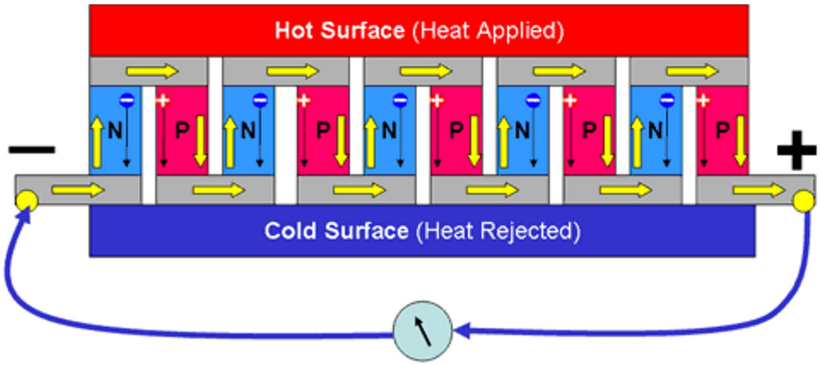


Figure 1.2: Theory diagram of the TEG [8].

structures, as illustrated in Fig. 1.3a. The hot end of the TEG is in contact with the surface skin of the human body, and the cold end is in contact with the air through the heat sink. The human body can be regarded as a continuous stable heat source of 37 degrees, and the external ambient temperature can fluctuate within a large temperature range, so it has the greatest impact on the performance of TEG. According to the diagram of the contact between the TEG, body skin and the environment, the thermal resistance model of the TEG is established, as depicted in Fig. 1.3b. R_A represents the thermal resistance at the interface of TEG and air, which is determined by the air convection [10]. Human skin is a well thermal insulator, causing the resistance between the TEG and body core. What's more, due to the surface roughness of the skin, a contact resistance exists between the interface of the skin and TEG. These two resistances caused by skin are marked as R_{skin}. R_{TE} is the resistance of the thermocouple in the TEG, usually the resistance of each pair of thermocouples is very small. R_S represents the equivalent thermal resistance of the TEG frame structure. If R_{TEG} is used to represent the thermal resistance of the TEG, its value can be expressed as

$$R_{TEG} = \frac{R_{TE}R_S}{R_{TEG}+R_S} \tag{1.1}$$

Also, the temperature difference on two sides of TEG is given by

$$\Delta T_{TEG} = \frac{R_{TE}}{R_A + R_{TEG} + R_{skin}}\Delta T \tag{1.2}$$

Assuming that the number of thermocouples contained in the TEG is N, the Seebeck coefficient of the thermoelectric material is S, the voltage generated by the TEG can be obtained by

$$V_{TEG} = N \cdot S \cdot \Delta T_{TEG} \tag{1.3}$$

As shown in the Fig. 1.3c, the TEG electrical model can be equivalent to a voltage source connected in series with a resistor R_{TEG}, externally connected to the load circuit, and R_{load} is the equivalent resistance load.

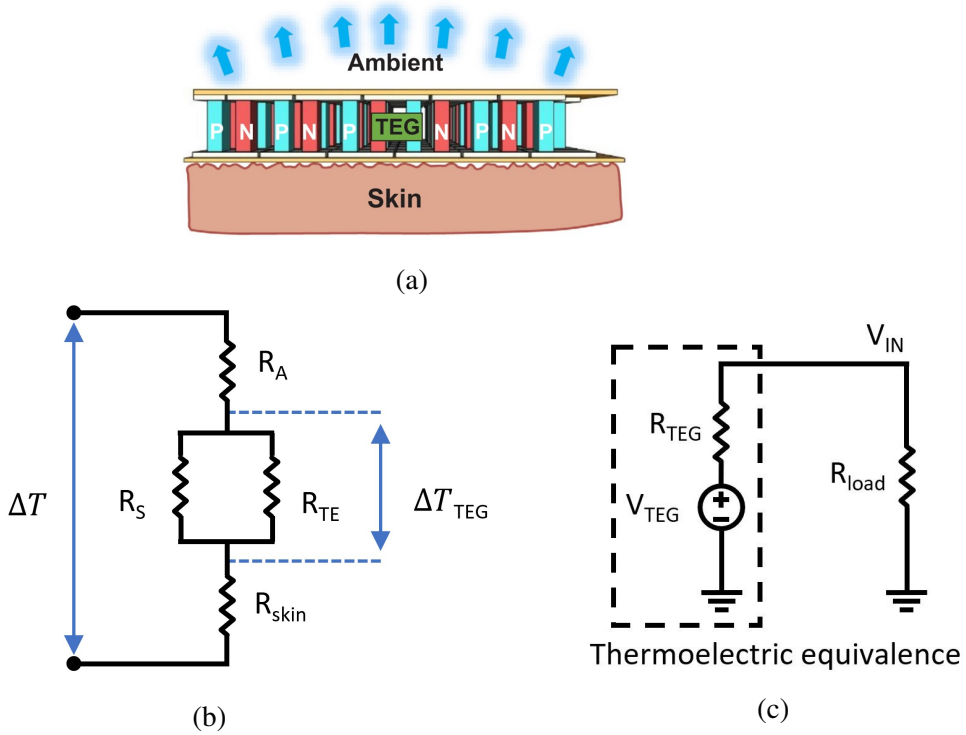


Figure 1.3: (a) TEG thermal model for body heat harvesting [9]. (b) Thermal resistance model of the TEG with various parasitic resistances.(c) TEG equivalent electrical model.

1.3 Piezoelectric Energy Harvesting

1.3.1 Piezoelectric Effect

Piezoelectric generator (PEG) can realize the conversion of vibration energy to electrical energy, mainly based on the piezoelectric effect of piezoelectric materials. In a general sense, when a piezoelectric material is deformed by an external force in a certain direction, positive and negative charges are generated on the surface due to internal polarization. The phenomenon that the charge density is proportional to the external force is called the positive piezoelectric effect. The phenomenon that an external electric field is applied to a piezoelectric material causes its deformation, which is proportional to the electric field strength, is called the negative piezoelectric effect. Fig. 1.4 shows the schematic of these two piezoelectric effects. In practical application, piezoelectric materials with positive piezoelectric effect are usually selected to make PEGs to realize the energy conversion.

1.3.2 Mechanical Model and Equivalent Circuit of PEG

From the perspective of physical mechanics, the structural model of piezoelectric materials is mainly composed of a mass block, m, a damper with an equivalent damping coefficient, C, and a spring with an equivalent stiffness, K_S, as shown in Fig. 1.5. The mass block is located above the piezoelectric material, and the bottom of the piezoelectric

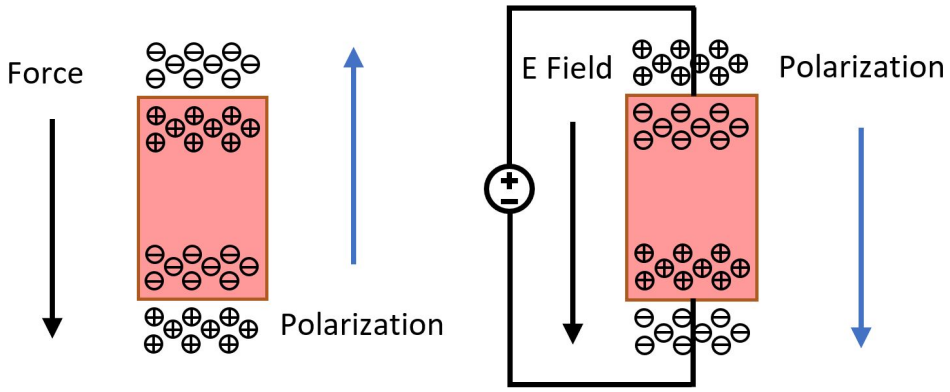


Figure 1.4: (a) Positive piezoelectric effect schematic. (b) Negative piezoelectric effect schematic.

material is fixed to the base. The external force can be described as

$$F = K_s u + C\dot{u} + m\ddot{u} \tag{1.4}$$

where u is the displacement of mass block.

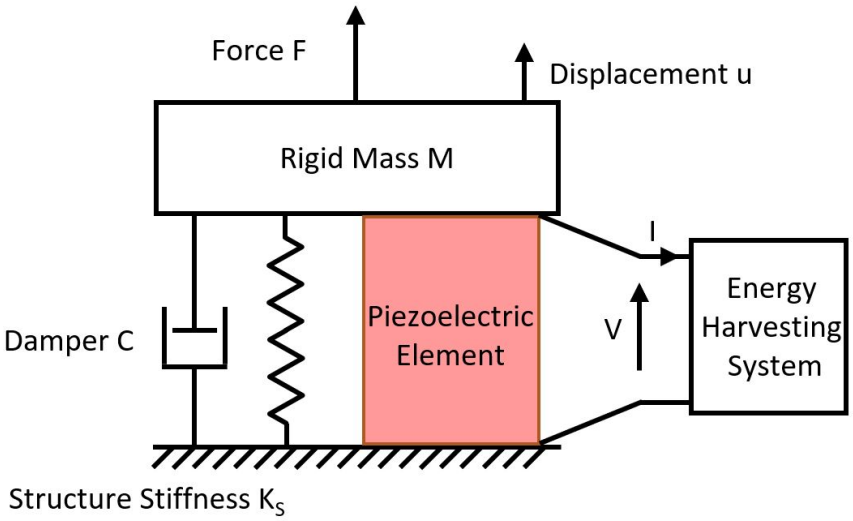


Figure 1.5: Mechanical model of a vibrating structure including a piezoelectric element[11].

The difference between PEG and ordinary power supply is that its internal impedance is capacitive rather than inductive. It is driven by mechanical vibrations that vary in amplitude and frequency. Fig. 1.6a shows its equivalent circuit model. Neglecting the mechanical loss, when the PEG performs periodic constant displacement motion, it can

be represented by the ideal current source I_{PEG} in parallel with the piezoelectric capacitor, C_{PEG}, and the leakage resistance, R_d, caused by the dielectric loss, and then in series with the resistance, R_{PEG}, caused by the piezoelectric loss. When the PEG is connected to the loop, the resistance R_{PEG} changes the output current value.

The operation frequency of PEG ranges from several hertz to several kilohertz. Compared with most switching power electronic devices, the frequency is lower, and the $\omega C_{PEG} R_{PEG}$ constant is much larger than the unit constant. Therefore, when the voltage across C_{PEG} is not large, the leakage resistance R_d can be ignored. Ignoring the loss caused by the piezoelectric effect, the PEG can be equivalent to a sinusoidal current source I_{PEG}, as shown in Fig. 1.6b, connected in parallel with a C_{PEG}. The output current is expressed as

$$i_{PEG}(t) = I_{PEG} \sin(2\pi f t) = \alpha f u \sin(2\pi f t) \tag{1.5}$$

where I_{PEG} is the amplitude of the AC current, f represents the frequency of vibration, α is the force factor. The relationship between PEG current and the open circuit voltage of the PEG is given by

$$V_{OC} = \frac{I_{PEG}}{2\pi f C_{PEG}} = \frac{\alpha u}{C_{PEG}} \tag{1.6}$$

Hence, the voltage amplitude of the PEG is related to the piezoelectric material, vibration frequency, and vibration amplitude, generally ranging from several volts to tens of volts.

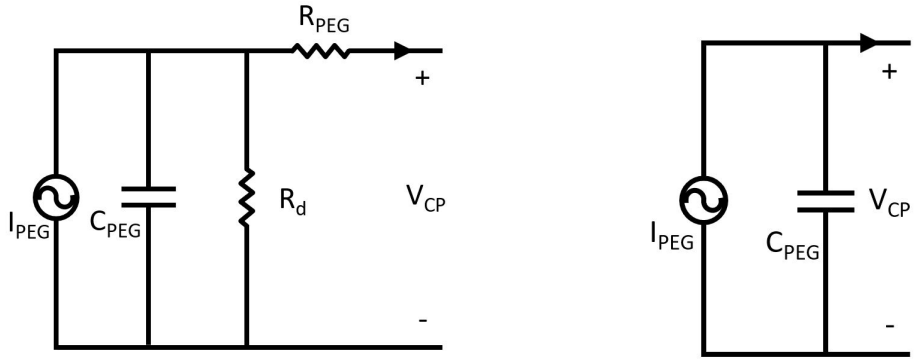


Figure 1.6: (a) PEG equivalent electrical model. (b) Simplified model.

1.4 Research Objectives and Targets

The main novelty that this work wishes to introduce is the idea of harvesting the thermal energy with the assistance of the proposed PEG starter which utilizes the kinetic energy. Since the temperature difference on the TEG can be as low as 1 or 2 K, the voltage it can generate is only tens of millivolts. With this proposed PEG starter, the system is able to achieve an ultra-low startup voltage. At this startup voltage level, the available power is extremely low. Therefore, the harvesting efficiency is supposed to achieve at least 60% to

Table 1.2: Specifications of this research

Specifications	Value
Startup voltage	10 mV
Output voltage	1.2 V
Harvesting efficiency(@ 10 mV)	60%
Maximum harvesting efficiency	80%

maintain the self-operation and power the load. As for the efficiency at high TEG voltage, it should reach state-of-the-art level. In addition, the load usually requires a 1.2 V supply voltage. According to the requirements, the design specifications can be listed in Tbl. 1.2

1.5 Thesis Outline

This thesis project entails the conceptual analysis, architecture design, circuit design, layout design, and measurement of the fabricated IC. The rest of this thesis report is organized as follows:

Chapter2 presents the three different approaches to achieving a low startup voltage. The working principle together with the merits and the drawbacks is analysed. A novel startup method is proposed and introduced, along with its working principle and schematic.

Chapter3 presents the analysis of the architectural design in a top-down approach. The fundamental structure of the harvesting system is first determined by analyzing and comparing four kinds of voltage boosting topology. The top-level architecture is presented, as well as its operation principle. The mathematical analysis of the system's overall efficiency and the startup process is also discussed.

Chapter4 gives details about the circuit implementations of each block.

Chapter5 mainly focuses on the measurement results and comparison with state-of-the-art.

Chapter6 makes a summary of this project, including conclusions and recommendations for future works.

2 Cold Startup Techniques

Based on the common application conditions of the energy harvesting system, the whole system is completely out of energy before the harvester starts to work. Therefore, the cold startup block is necessary to activate the operation of the whole system in the very beginning stage without any assistance from the energy storage block, for instance, battery and capacitor. Since the startup block only focuses on activating the system at a low input TEG voltage, the energy harvesting efficiency, conversion efficiency and charging capability are regarded inferior and can be traded for minimum TEG voltage. What's more, the startup block is usually disabled after the startup operation to improve the efficiency.

In this chapter, three different kinds of startup techniques are introduced. Based on the operation principles and merits of these designs, a novel cold startup technique is proposed.

2.1 Mechanical Switch Assisted Startup Technique

Y. K. Ramadass *et al.* [12] presents a thermoelectric energy harvesting system for wearable applications with a starter that takes advantage of the movement of human body. These mechanical vibrations are used to trigger a mechanical switch, $S0$, in the startup circuit, as shown in Fig. 2.1. This switch can turn ON or OFF with only a small amount of vibration of less than 100 mg in acceleration. For example, the vibration generated by waving arm or shaking wrist is large enough to activate the switch. The startup operation begins when the vibration closes the mechanical switch.

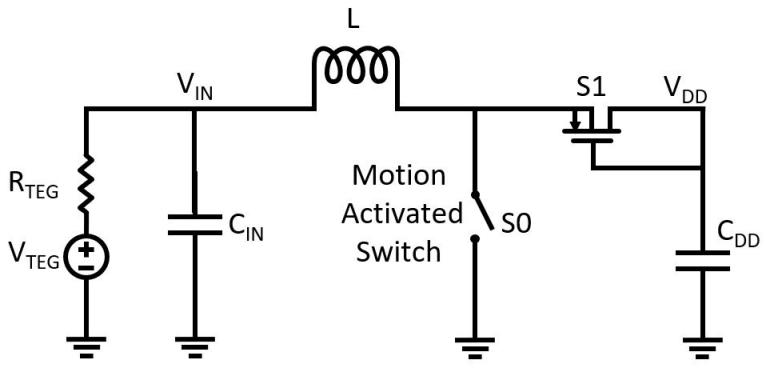


Figure 2.1: A startup circuit with the assistance of mechanical switch.

Once the switch turns ON, the voltage induced by the TEG causes a voltage difference on the two sides of the inductor. Therefore, a current is generated and flowing through the inductor. With another vibration induced by the movement of human body, the switch S0 is OFF. As the path to the ground on the right side of the inductor is closed, the current in the inductor has to find an alternate path to flow. With more and more positive charges accumulated at the source side of the diode, $S1$, the voltage at that point increases, and $S1$ turns ON eventually. By considering the $S1$ as an ideal diode, a series RLC circuit is

formed. At the end of the ON/OFF cycle, the voltage stored on capacitor, C_{DD}, can be written as

$$V_{DD,ideal} = \frac{\sqrt{L/C_{DD}}}{R_{TEG}+R_L+R_{sw}} V_{TEG} \tag{2.1}$$

where L is value of inductor, R_{TEG} is the internal resistance of the TEG, R_L and R_{SW} are parasitic resistances of the inductor and the switch. However, the diode is not ideal and the voltage drop on it therefore shall be taken into consideration. Hence, the real voltage on the capacitor formed by the harvested energy is gives as

$$V_{DD} = \sqrt{V_{diode}^2 + V_{DD,ideal}^2} - V_{diode} \tag{2.2}$$

where V_{diode} is the actual voltage drop on $S1$. To make sure the circuit work normally after the startup operation, V_{DD} is set to 1 V in this design. By subtly setting the value of RLC components in the circuit, the desired V_{DD} can be achieved.

Although this technique is easy to implement and enables the system to startup at 35 mV, a large L and small C_{DD} are required to ensure the system startup at low V_{TEG}, which leads to the increase in size and decrease in power capacity to power the load, respectively. Besides, as the body movement is continuous, the ON-OFF state of the mechanical switch can not be precisely controlled.

2.2 Charge-pump Based Startup Technique

Fig. 2.2 shows the architecture of the low-voltage starter proposed in [13]. To achieve a low input voltage, this starter adopts an LC-tank oscillator and a voltage multiplier. Firstly, the oscillator converts the input DC energy into an AC form. Then, a voltage multiplier transfers the AC energy back to DC with a boosted level. This work directly charges the output voltage during the startup stage instead of driving the boost converter to charge the intermediate storage capacitor.

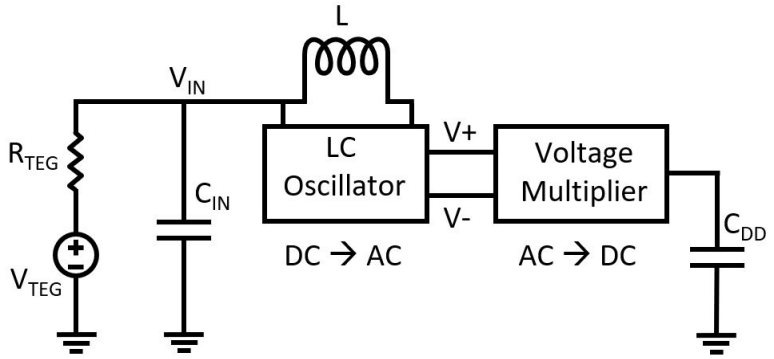


Figure 2.2: Circuit diagram of the low-voltage starter based on voltage multiplier.

The circuit diagram of the LC oscillator and its equivalent circuit is demonstrated in Fig. 2.3. Typically, the inductor has internal resistance and can be modeled by an ideal inductance, L, in series with a resistor R_L. According to the high-Q approximation in [14],

the loss of the inductor can be simplified into a equivalent resistor R_P in parallel with the inductor as

$$R_P \approx \frac{L}{R_L C_P} \tag{2.3}$$

where C_P is the parasitic capacitance of the cross-coupled transistors. To fulfill the common design constraint [15], the equivalent transconductance of the cross-coupled conductors should be at least four times of $1/R_P$. Thus, the minimum input voltage to startup the circuit can be expressed as

$$V_{IN} \geq \frac{4R_L C_P}{k_n L} + V_{TN} \tag{2.4}$$

where k_n is the transductance parameter and V_{TN} is the threshold voltage of the NMOS transistors.

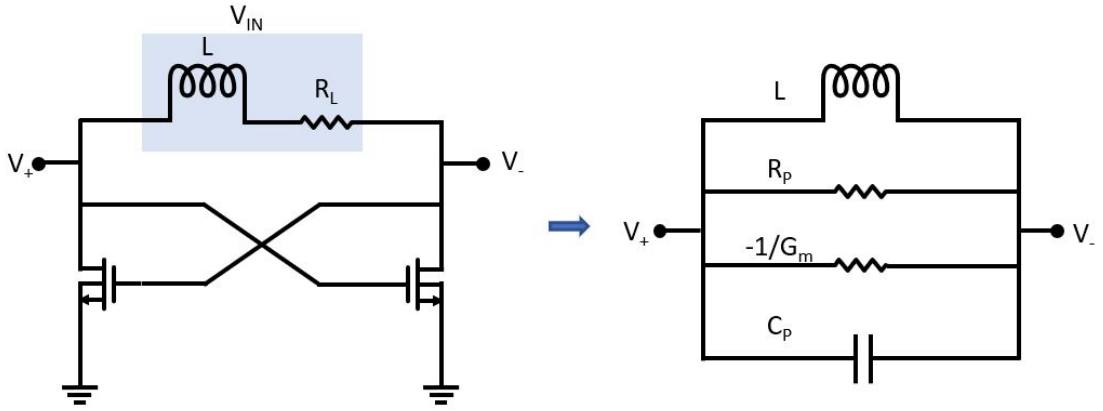


Figure 2.3: Circuit diagram the LC oscillator and its equivalent circuit.

As depicted in Fig. 2.2, the LC oscillator is followed by a voltage multiplier to boost the voltage level. Consequently, the input capacitance of the voltage multiplier, C_{VM}, works as the load of the oscillator. Compared with the parasitic capacitance of the cross-coupled transistors, the effect of C_{VM} is not negligible. As a result, the V_{IN} is rewritten as

$$V_{IN} \geq \frac{4R_L(C_P + C_{VM})}{k_n L} + V_{TN}. \tag{2.5}$$

Fig. 2.4 demonstrates the circuit schematic of a single stage of the voltage multiplier. The overall voltage multiplier is composed of N cascaded differential stages. The output voltage of each single stage is given by

$$V_{OUT_i} = V_{OUT_i-1} + 2(V_A - V_{ON}) \tag{2.6}$$

where V_A is the amplitude of the AC voltage at each stage input and V_{ON} is the voltage drop on the diode. Therefore, the final output of the voltage multiplier can be expressed as

$$V_{DD} = V_{OUT} = 4N(V_A - V_{ON}). \tag{2.7}$$

By adjusting the number of cascaded stage, this voltage multiplier is able to generate the output voltage at a desired level to startup the operation of the whole system.

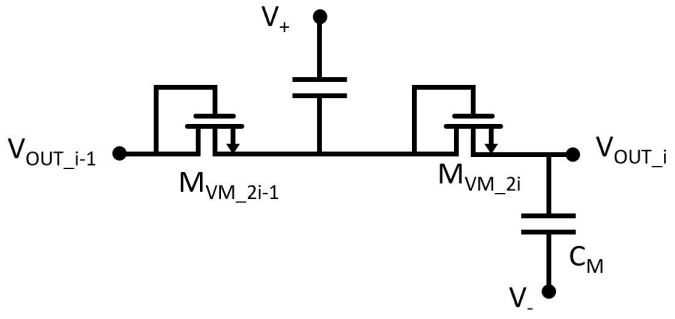


Figure 2.4: Circuit schematic of a single stage of the voltage multiplier

The limitations of this design to reach an ultra-low startup TEG voltage can be concluded into two aspects. On one hand, the internal resistance of the inductor and the parasitic capacitance make up a part of the input voltage as derived in (2.5). On the other hand, the threshold voltage of transistors in the oscillator impedes the minimum input voltage that can be achieved. So, this design has a minimum startup voltage of 50 mV which is much higher than the goal proposed in our design.

2.3 One-shot Startup Technique

In [16], a one-shot cold-start technique is adopted for self-start. Like the previous design, this low-voltage starter also consists of an oscillator and a voltage multiplier, as shown in Fig. 2.5. However, their working principles are different. During the cold-start operation stage, a charge-pump based on-chip voltage multiplier boosts the input voltage V_{IN} to an output voltage of V_{CP}. The charge pump is driven by a low-voltage ring oscillator powered by V_{IN}. Instead of directly collecting the output of charge pump as the power supply to startup the system, a single startup strobe pulse, V_{ST}, is generated by V_{CP} to drive the boost converter. In this short duration, the NMOS in the boost converter is turned ON, and the inductor is charged with the current from TEG. On the falling edge of the single startup pulse, the PMOS diode is turned on and transfers the power on the inductor to the on-chip capacitor, C_{DD}. This capacitor is small enough to generate a voltage, V_{DD}, higher than 500 mV to power a secondary oscillator to clock the entire system.

As mentioned in the charge-pump based startup technique, the threshold voltage of transistors in the low-voltage oscillator constrains the minimum self-startup voltage. This hard demand impedes its ability to startup at a lower voltage. Therefore, the minimum startup voltage of this design is also 50 mV which is rather high compared with other low startup voltage works.

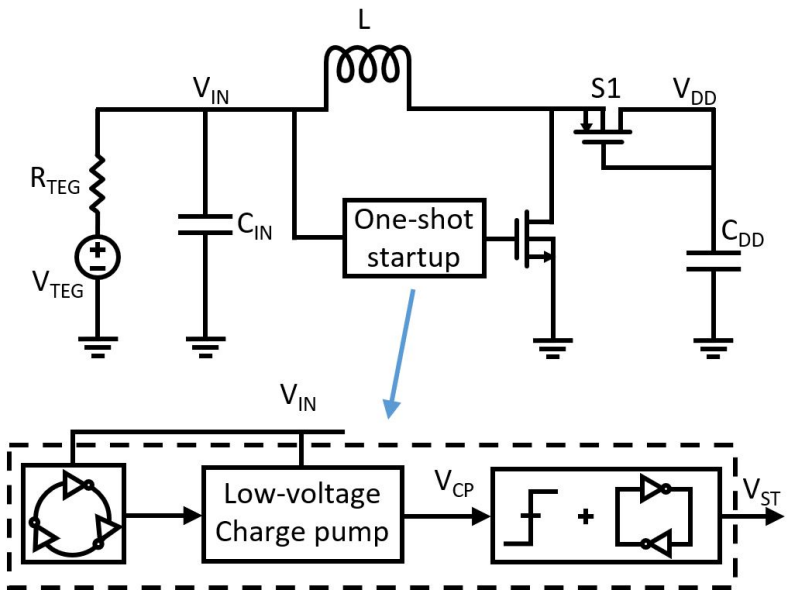


Figure 2.5: Architecture of the boost converter with one-shot startup technique.

2.4 This Work

To obtain a further low startup voltage in the thermoelectric energy harvester, an alternative approach is proposed in this subsection. By analysing and classifying the working principle of the previous designs, trade-off has been made to combine their merits and make sure the limitations of each design have as small as possible influence on the proposed startup circuit.

2.4.1 Energy Source Selection

According to the previous startup designs, there are two mainly sources from which the startup block is able to draw energy. The first one is directly using the thermal energy. By utilizing the voltage multiplier or charge pump, the low input voltage can be magnified to a high output voltage which is able to startup the system. The advantage of this method is only depending on the thermal sources, which enables the system to startup successfully as long as the TEG voltage exceeds the minimum startup voltage. However, the weakness of this approach is also noteworthy. One is that the threshold voltage of the transistors used in the startup circuit undoubtedly affect the minimum startup voltage that the system can achieve. Another concern regarding this method is that these startup designs usually take a large amount of area. Due to the small input voltage, the charge pump usually consists of tens of stages. Consequently, the area of the startup circuit may be even larger than the total area of the rest circuit in the system. Once the circuit works normally, the area occupied by the startup circuit on the chip does not function any more. This leads to a low usage efficiency of the on-chip area.

A second method is using another energy source other than thermal energy to power the startup block. As introduced in the mechanical switch assisted startup technique, the working environment of the wearable devices contains not only thermal energy but also mechanical vibrations induced by human body, which is a good source for the startup block. Hence, even though this approach relies on two different energy sources to activate the system, the working environment of different applications can provide the needed energy sources. For instance, the engines of airplanes and vehicles generate a lot of heat while working, besides, they also vibrate. Therefore, they are ideal thermal sources for the TEG to power the wireless sensors mounted on them. Meanwhile, the periodic kinetic vibration energy can be collected by a piezoelectric generator to power the startup circuit in the system.

In this paper, the startup circuit is set to draw energy from the piezoelectric generator since vibration energy is ubiquitous in the environment. The relation between the proposed startup block and the thermoelectric energy harvester is shown in Fig. 2.6.

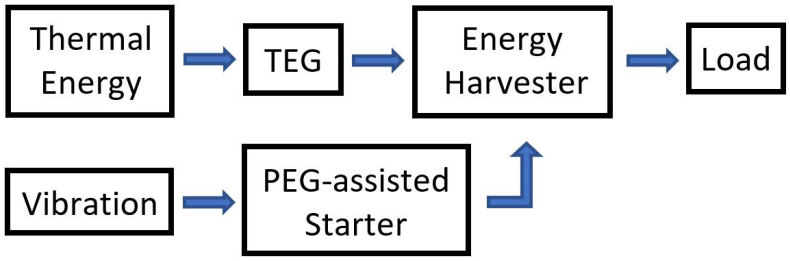


Figure 2.6: Basic composition of the energy harvesting system.

2.4.2 Working Strategy Selection

Based on the analysis of the previous startup techniques, there are two fundamental ways for the startup circuit to activate the system. The first approach is generating a high voltage and storing it on the intermediate capacitor. In this kind of startup method, the on-chip energy storage capacitor powers the internal oscillator and control circuits to generate a clock signal which drives the boost converter. A drawback of this method is the high demanding on the power that can be provided by the starter. The efficiency of the startup circuit is usually low. To make sure the starter can generate enough power for the internal oscillator, the input power of the starter should be sufficiently high. However, this is contrary to the design target that the PEG starter is only used to startup the system instead of power the whole system. Therefore, this method is not qualified in our design compared with the one which will be introduced afterwards.

The second method is to generate a clock signal by the starter to drive the NMOS transistor in the boost converter to harvest energy for the system, as shown in Fig. 2.7. This method reduces the circuit complexity of startup block and takes advantage of the property of the

signal generated by PEG. It can drive the boost converter to work at extremely low TEG voltage and store harvested thermal energy into the capacitor.

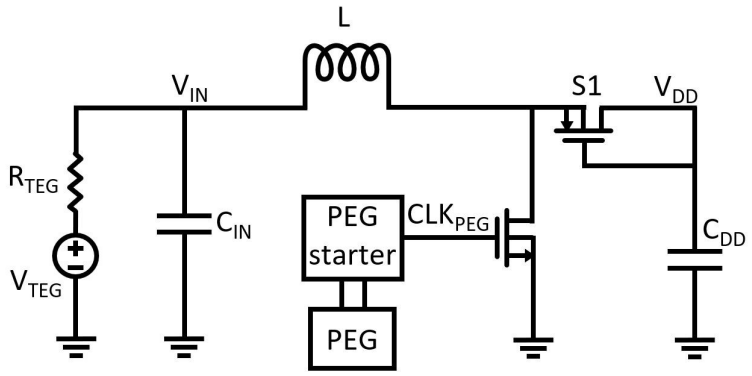


Figure 2.7: Architecture of the boost converter with PEG stater.

2.4.3 Preliminary Design of the Startup Circuit

The circuit schematic of the proposed PEG starter is shown in Fig. 2.8. To utilize the the sinusoidal current, I_{PEG}, generated by the PEG, a full-bridge rectifier (FBR) is employed to convert the AC current into a DC voltage, V_{PEG}. There are two working phases for the FBR. When the input is positive, diodes D1 and D4 are switched ON and D2, D3 are turned OFF. When the input is negative, D2 and D3 are ON state but D1, D4 are OFF state.

As the PEG has an internal capacitor, which is charged and discharged periodically by the current, the polarity of $IN+$ and $IN-$ is also reversed periodically [17]. Since the PEG itself generates an AC signal, the only thing that this starter needs to do is rectifying the sinusoidal AC signal in to a square wave to clock the boost converter in an asynchronous way. Four serially connected inverters, which are powered by V_{PEG}, regulate the voltage swing at the output of PEG to a square wave, as shown in Fig. 2.9. Although the output of the inverter is not a very good square wave due to the fluctuation in the supply, the falling edge is sharp enough to close the NMOS in the boost converter in a short time without reducing the current in the inductor too much.

Compared with the design which only uses vibration to drive the mechanical switch [12], this work is able to control the operation of startup more subtly. What's more, the proposed design allows the startup circuit to ignore the limitation of the minimum startup voltage of the transistor compared with the works that use a charge pump as startup circuit. It is noted that, during the startup stage, the startup block is totally powered by the harvested kinetic energy. So, all the harvested energy from the thermal source can be stored without sharing any portion for the startup clock generation, which dramatically decreases the required minimum TEG voltage.

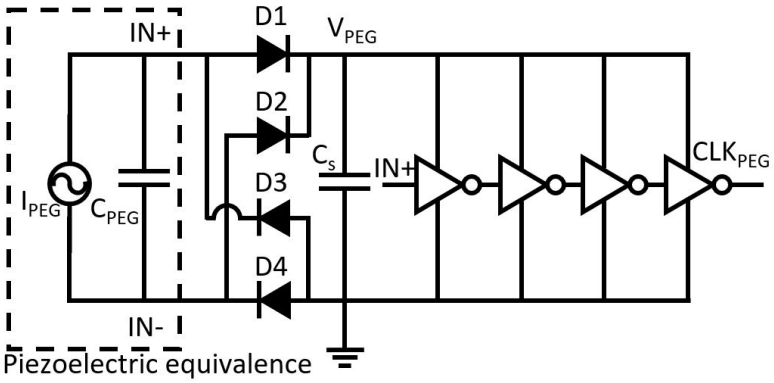


Figure 2.8: Circuit schematic of PEG startup block.

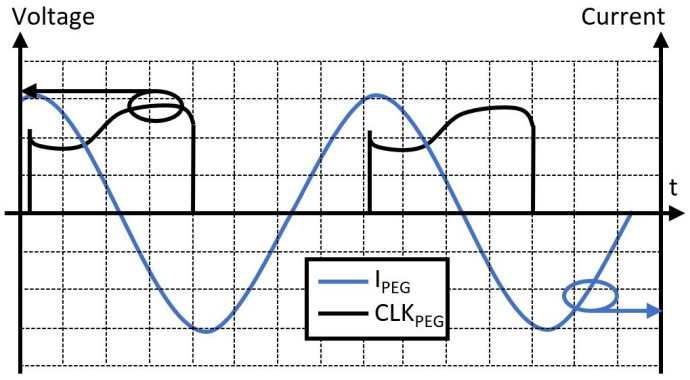


Figure 2.9: Associated waveform in the startup operation.

3 Harvester System Level Analysis and Design

In this section, the contents mainly focus on the system level design procedures of the harvester. In section 3-1, 4 kinds of voltage boosting circuits are discussed and compared, among which the boost converter that works in discontinuous conduction mode is selected as the fundamental structure of the system. Next, in section 3-2, based on the major requirements that the system is going to achieve, the key blocks are analysed and determined to realise the key functions. Then, turn to the system working principle and the state transformations in section 3-3. Mathematical analysis is done to give a comprehensive understanding of the overall efficiency in section 3-4. Finally, section 3-5 gives the analysis of the startup operation from the perspective of the relations between all related parameters in TEG and PEG.

3.1 Harvester System Structure Analysis

As introduced in previous section, the voltage at the out put of TEG is only tens of millivolts when the temperature gradient on the TEG is low. However, the power supply voltage of the CMOS circuit is generally 1.2 V to 3.6 V, so it is necessary to use the voltage boosting technique to boost the TEG output voltage to a level required by the load. The TEG output voltage and power are very low and require a very large boost multiple, so the performance requirements of the boost converter are very strict. At present, there are four main boost topologies, namely, switched capacitor DC-DC converter, DC-DC boost converter, DC-DC buck-boost converter, and DC-DC converter based on transformer.

3.1.1 Switched Capacitor DC-DC Converter

Switched-capacitor DC-DC converter, also known as charge pump as described in last section, consists only of capacitors and switches, and does not contain inductive elements. Its working principle is to realize the transfer of energy through the periodic transfer of charges on the capacitor. It can not only complete the boost, but also can achieve the function of buck or even reverse by using the transformation of the topology. There are

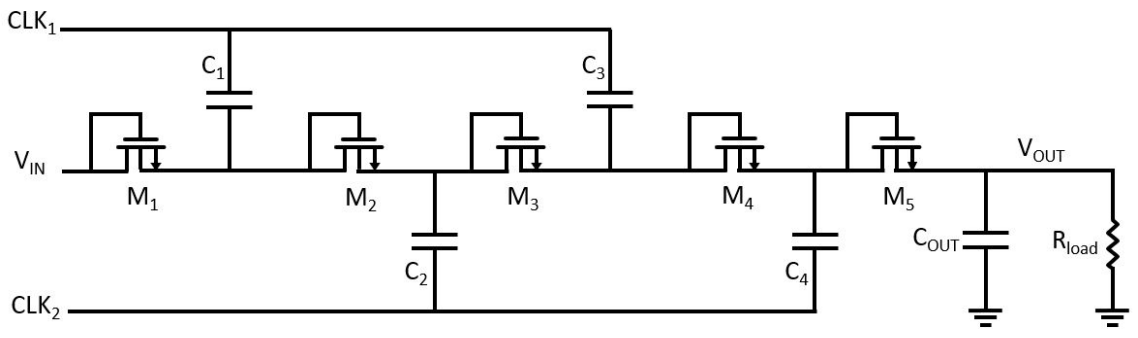


Figure 3.1: Circuit diagram of the switched-capacitor DC-DC converter.

various topological structures of the charge pump. The Dickson structure, as shown in Fig. 3.1, is used to analyze the working principle of the switched capacitor DC-DC converter.

The circuit consists of multiple pairs of capacitors and MOS transistors. The circuit is controlled by two clock signals. CLK_1 and CLK_2 have the same frequency which maintains periodic high-low alternation. By periodically lifting the potential of each capacitor, the charge transfers between the capacitors. The specific working process is as follows: First, CLK_1 is kept at a low level, CLK_2 is kept at a high level. The voltage source V_{IN} charges the capacitor C_1, and the charge in the capacitor C_2 is transferred to the capacitor C_3, and the charge in C_4 is transferred to the capacitor C_{OUT}. When the clock level is switched, the charge in the capacitor C_1 is transferred to the capacitor C_2, the charge in C_3 is transferred to the capacitor C_4, and the energy required by the load is provided by the output capacitor C_{OUT}. In an ideal state (without considering the voltage drop on the transistors), after several cycles of operation, the circuit reaches a steady state. The positive electrode potential of capacitor C_1 is maintained between V_{in} and $2V_{IN}$. Similarly, the potential of final output capacitor C_{OUT} is stable at $5V_{IN}$. If a higher output voltage is required, more sets of capacitors and transistors can be added accordingly.

Switched capacitor DC-DC converters have the advantages of low noise and low electromagnetic interference. What's more, capacitors are easier to integrate on an IC chip than inductors. However, the voltage gain of the switched capacitor DC-DC converter depends on the number of stages. For high-gain applications, the larger the stage, the more components it contains, and the increase in the loss of the components itself leads to a decrease in efficiency. Therefore it is widely used in the startup design where the efficiency is less concerned. Hence, this topology is not suitable for the thermoelectric energy harvesting design with ultra-low startup voltage.

3.1.2 DC-DC Boost Converter

The DC-DC boost converter is one of the most widely used voltage boosting structure in the low power electronics, as illustrated in Fig. 3.2. By periodically adjusting the ON/OFF state of the switches, the inductor increases or releases the energy stored in the magnetic field to resist the changes in current. Through this charging and discharging process, the energy is transferred from the input to the output. Furthermore, the low input voltage is boosted to a high level for output.

According to whether the current in the inductor is zero at the end of each switching cycle, the circuit working state can be divided into discontinuous conduction mode (DCM) and continuous conduction mode (CCM). These two working modes of the boost circuit are analyzed and derived afterward.

Fig. 3.3 - Fig. 3.5 displays the three states of the boost converter that works in DCM. In the inductor charging state, as shown in Fig. 3.3, the switch $S1$ is turned ON, and the switch $S2$ is turned OFF to prevent the reverse current from draining the energy from

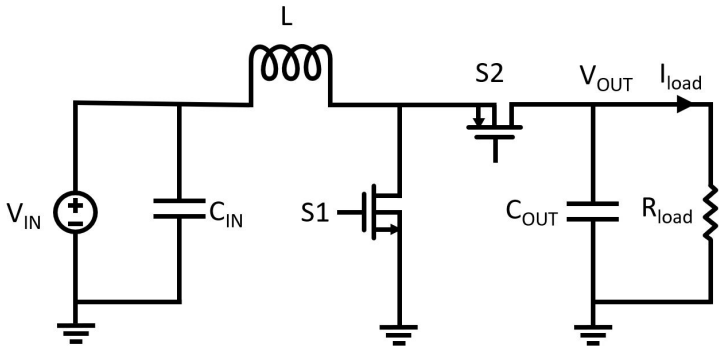


Figure 3.2: Schematic of a boost converter.

the output capacitor. Then energy stored on the C_{IN} is transferred to the inductor L in the form of an increasing current, I_L, which flows through the inductor. Therefore, a significant voltage drop can be seen on V_{IN}. The energy required by the load is provided by the output capacitor C_{OUT} during the stage. The current I_L will reach its peak value during the switch $S1$'s ON time, t_{ON}. It can be expressed as

$$I_{L,peak} = \frac{t_{ON} \cdot V_{IN}}{L} \tag{3.1}$$

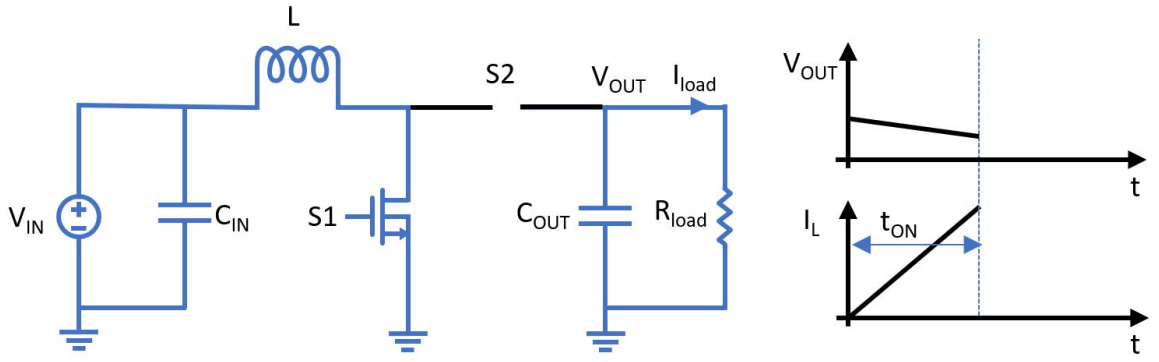


Figure 3.3: Configurations of a boost converter in inductor charging state.

As shown in Fig. 3.4, $S1$ is turned off in the conductor discharging state. Since the current in the inductor cannot change abruptly, the $S2$ is open simultaneously to conduct the current and direct it to supplement the energy to the output capacitor C_{OUT}. As the voltage drop on the inductor has an opposite direction with the inductor current, I_L decreases to zero during the closing time of $S2$, t_{OFF}. In this state, the energy stored on L is transferred to output capacitor C_{OUT}. As a result, the V_{OUT} increases. The inductor current in this stage can be derived as:

$$I_{L,peak} = \frac{t_{OFF} \cdot (V_{OUT} - V_{IN})}{L} \tag{3.2}$$

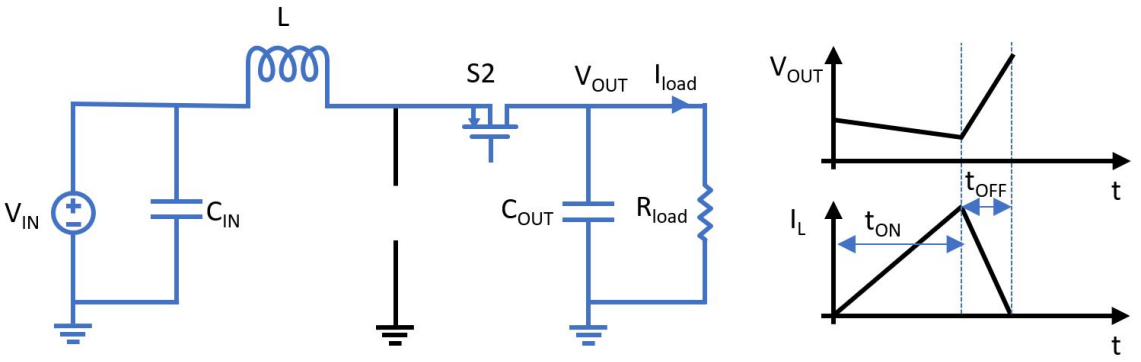


Figure 3.4: Configurations of a boost converter in inductor discharging state.

Fig. 3.5 shows the sleep state of the boost converter when both $S1$ and $S2$ are turned OFF and the inductor has no current on it. The capacitor C_{IN} restores its storage with the energy from voltage source.

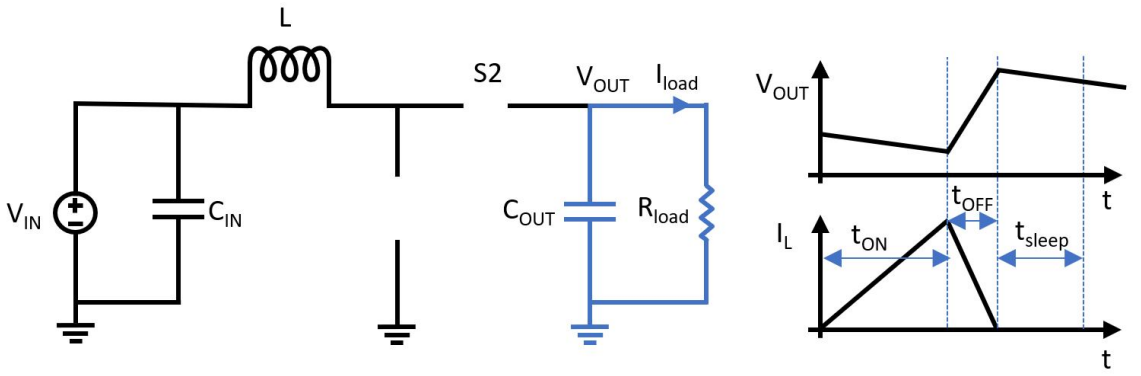


Figure 3.5: Configurations of a boost converter in the sleep state.

The working principle of the boost converter that works in CCM is quite similar to the principle of DCM. The major difference lies in the working time of the inductor. In CCM, the inductor always has current on it. Therefore, the boost converter that works in CCM has no sleep time. Fig. 3.6 shows the waveform of the boost converter in the CCM. In terms of continuous conduction mode, it is not suitable in this design which requires low harvester system losses when the input voltage is low. The reasons are given as follows. Firstly, high and continuous inductor RMS current in CCM lead to large conduction loss occur in both two power switches and inductor parasitic resistance. Secondly, by increasing frequency to reduce inductor RMS current, high frequency would lead to high power switching loss. What's more, by increasing inductance to reduce inductor RMS current,

increasing parasitic resistance of inductor would cause extra power conduction loss. And finally, loop stability needs to be analysed and circuit implementation increases system complexity. However, DCM DC-DC converter has no such issues. Therefore, the DCM boost converter is more suitable in this design. Similarly, for other DC-DC converters, only the DCM is considered and analyzed in the following subsections.

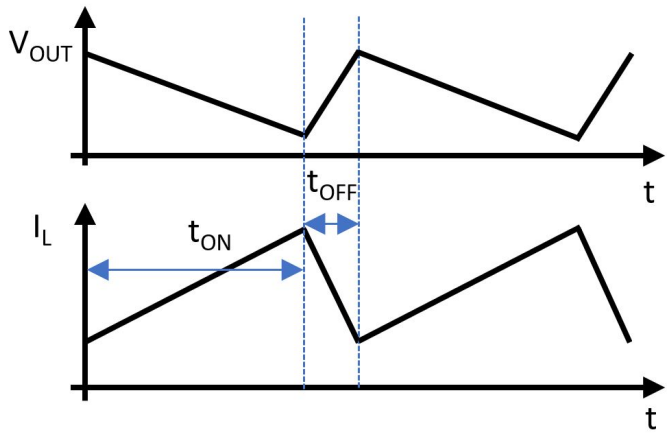


Figure 3.6: Waveforms of the boost converter in the CCM.

3.1.3 Buck-Boost Converter

DC-DC buck-boost converter topology is also a choice which can be implemented for harvest interface structure, as shown in Fig. 3.7. It not only can boost the low input voltage to a high output voltage but also can down convert a high input to a low output. Here in the energy harvesting system, only the up conversion ability is used.

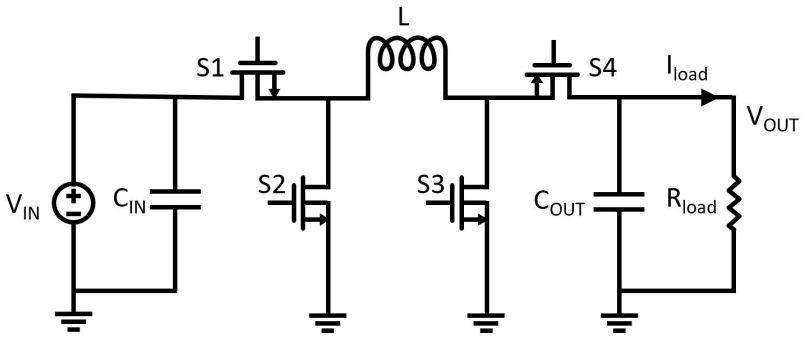


Figure 3.7: Schematic of a flyback converter.

There are three states in the DCM operation of the buck-boost converter. In the inductor charging state, as shown in Fig. 3.8, switch $S1$ and $S3$ would be turned ON and current would flow from voltage source through $S1$, L, $S3$ to ground. The inductor is energized.

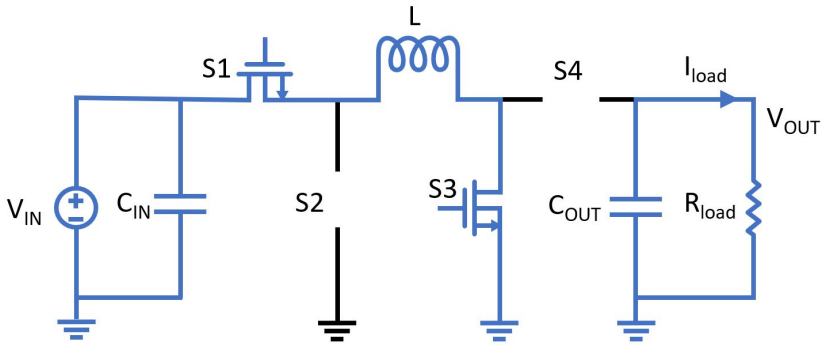


Figure 3.8: Configurations of a flyback converter in inductor charging state.

Fig. 3.9 depicts the inductor discharging state. During phase two, $S1$ and $S3$ are turned OFF but $S2$ and $S4$ are turned ON. Then, current flow though $S2$, inductor and $S4$ to C_{OUT}. The energy stored on the inductor is transferred to the output.

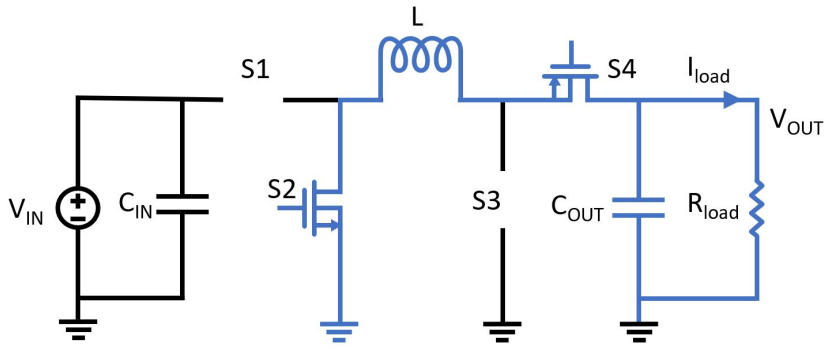


Figure 3.9: Configurations of a flyback converter in inductor discharging state.

When the current flows in the inductor drops to zero, the converter enters the sleep state where both switch $S1$, $S2$, $S3$, and $S4$ are open. The load is powered by the energy stored in the output capacitor.

In this case, switch conduction loss and driving loss would be doubled because of the two extra transistors comparing to the boost converter. Except for this, switches control circuit power losses would also be doubled. Meanwhile, in the inductor charging state, $S1$ and $S3$ should be controlled to turned ON simultaneously. And also, the turn ON for $S2$ and $S4$ just after turn OFF $S1$ and $S3$ should also be synchronous. The time laps between the switching of the switch pairs will cause more power losses. To diminish that, the proper control of four switches is required which increases the circuit design complexity.

3.1.4 Flyback Converter

The schematic of the flyback converter is shown in Fig. 3.10. The flyback converter topology applied to low power device is actually a buck-boost converter. Compared with the circuit topology based on inductor, the flyback converter uses a transformer to replace the inductor. The transformer not only plays the role of isolation, but also has the role of the inductance. The transformer turn ratio is $n = N_2/N_1$, among them, N_1 is the primary turn number, and N_2 is the secondary turn number. The secondary voltage is given by

$$V_S = NV_P \tag{3.3}$$

where V_P is the primary voltage.

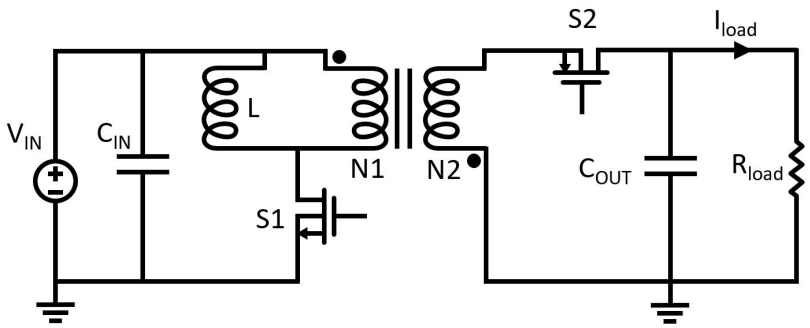


Figure 3.10: Schematic of a flyback converter.

There are three states of the DCM operation. For the inductor charging state, as shown in Fig. 3.11, the switch $S1$ is turned ON. As the input voltage source directly connects to the magnetizing inductor, the current and magnetic flux are generated and start to rise with time. In this state, the energy is transferred from the voltage source to the magnetizing inductor. Since the switch $S2$ is blocked in this stage, no current will flow through the secondary of the transformer, and also the primary current is zero. Meanwhile, the load is powered by the output capacitor.

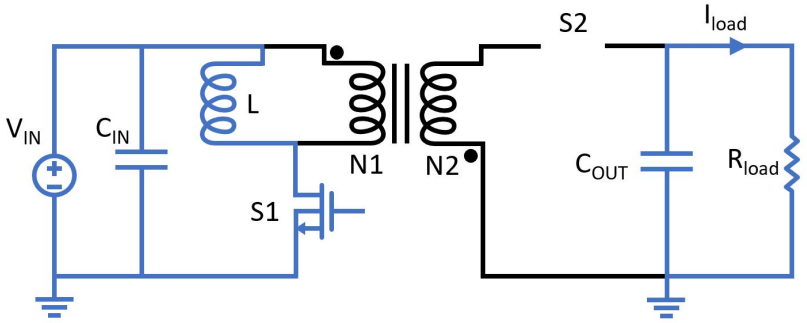


Figure 3.11: Schematic of a flyback converter in inductor charging state.

When the switch $S1$ is open, as shown in Fig. 3.12, the current flowing through the magnetizing inductor is directed to the primary side of the transformer and forms a new loop. The primary current drops rapidly as well as the magnetic flux in the primary winding. In this case, the switch $S2$ is closed, conducting the induced secondary current to the output. Hence, the energy stored in the magnetizing inductor is transported by the transformer to recharge the capacitor and supplies the load.

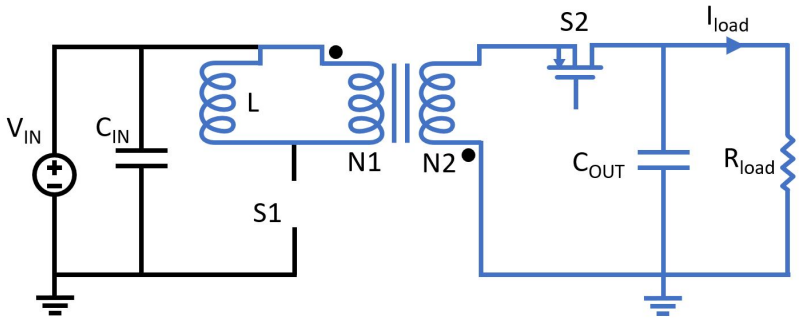


Figure 3.12: Schematic of a flyback converter in inductor discharging state.

When the current flows in the inductor drops to zero, the converter enters the sleep state where both switch $S1$ and $S2$ are open. The load is powered by the energy stored in the output capacitor.

The flyback converter can provide a large step-up ratio through the transformer, but the use of the transformer results in an excessively large area occupation and a difficulty in the MPPT design. In addition, for the flyback converter that works in discontinuous conduction mode, the presence of high RMS and peak current in the design limit the efficiency of the converter. As a result, the flyback converter is not suitable for low power thermoelectric energy harvesting applications.

3.2 Harvester System Level Design

Based on the analysis of the structure and working principle of the TEG and PEG in previous section, some fundamental characteristics of the thermoelectric energy harvesting system can be concluded as follows:

1. The input voltage and input power provided by the TEG are heavily influenced by the environment. In some extreme cases, the TEG voltage is only a few millivolts, and the available power is also no larger than several microwatts. Therefore, the available power from the ambient environment must be collected as much as possible.

2. Since the harvester system is developed based on a boost converter, the synchronization between the switches should be precisely, otherwise the synchronization loss may greatly impact the power efficiency of the converter.

3. The complete workflow of the system includes several stages. In different stages, the system usually needs different operations to the input power.

Based on these characteristics, the proposed thermoelectric energy harvesting system is integrated with different kinds of functional blocks to make sure the system work properly and enhance the performance.

1. The Maximum Power Point Tracking (MPPT) technique is exploited to make sure the TEG always work at its optimal state and provide the harvester with the highest achievable power.

2. A Zero-current Switching (ZCS) block is proposed to regulate the synchronization of the switches and control the gate switching.

3. The state detector block monitors the state of the harvester system and instructs other control circuits to respond to the changes in the operation state.

Fig. 3.13 illustrates the architecture of the proposed TEG harvesting system. It consists of three main parts: TEG-based power converter, PEG-based cold startup circuit, and control blocks.

The TEG works as the input voltage source with only a few ohms of source resistance, generating a temperature proportional voltage, V_{TEG}. During the startup period, the PEG starter provides the initial startup signal to drive the boost converter to accumulate sufficiently high V_{CTRL} from low V_{TEG} until the control blocks can operate normally. The converter stores the power in two capacitors. C_{CTRL} provides the supply voltage, V_{CTRL}, for the internal control circuit. C_{OUT} is for the external output voltage, V_{OUT}.

Control circuits are mainly composed of state detection block, MPPT block, voltage controlled oscillator (VCO), ZCS block, and low-dropout regulator (LDO). The voltage dividers in the stage detector provide a portion of V_{CTRL} and V_{OUT}, so that by comparing them with the reference voltage, V_{ref}, the stage detection block can generate signals which instruct the system to work in different operation stages. More details about the operation stages will be given in the next subsection. The MPPT and VCO blocks change the gate driving signal of switch S0 and the system operation frequency with the variation of the TEG voltage, thus ensuring the interface collect as much as possible power from the TEG. The ZCS block detects the polarity of the current in the path of switch S1 and S2. By closing the path exactly at the polarity reverse point, the circuit avoids the negative current draining energy from the capacitor and the positive current being disposed because of the early cutting off.

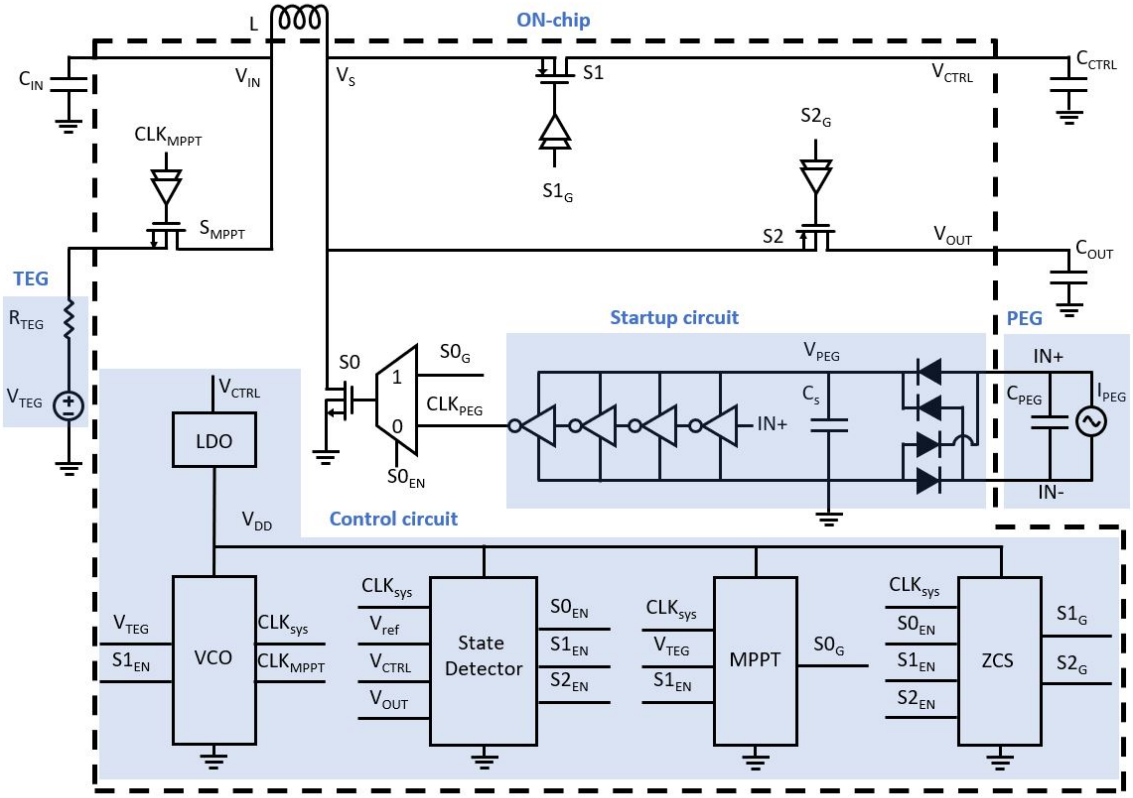


Figure 3.13: Architecture of the proposed TEG energy harvesting system.

3.3 Harvester System Working Principle

There are four operation stages for the system that are cold-start state, internal-charging state, external-charging state, and output state. The state diagram and transition requirements are shown in Fig. 3.14. The first three stages are the startup of the system. Only in output state can the system power the load steadily. The transitions between states depend on the amplitude of V_{CTRL} and V_{OUT}.

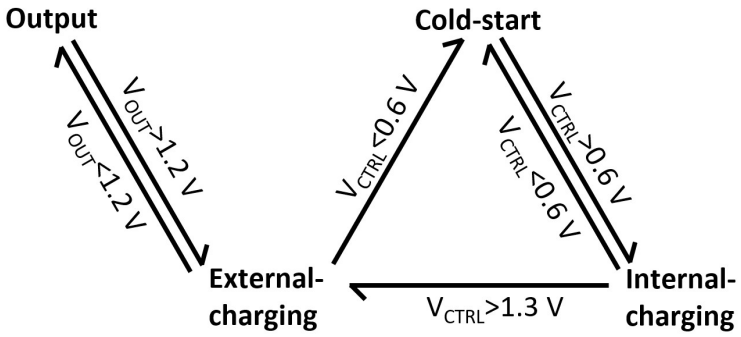


Figure 3.14: State diagram of the system.

3.3.1 Cold-start state

As shown in Fig. 3.15, the system starts from cold-start state without external battery assistance and any energy stored in the system. During this period, all the control circuits cannot work. Triggered by the movement of human body or the vibration of the vehicle engine, the PEG stater starts to generate a clock signal, CLK_{PEG}, to drive the low-side switch, $S0$. With a temperature difference across the TEG and V_{TEG} remains higher than the minimum startup voltage, a current flows through the inductor and keeps increasing. After $S0$ turns OFF, the energy stored in the inductor flows into C_{CTRL} and C_{OUT} through the high-side switch, $S1$ and $S2$. Since the ZCS block cannot control the gate switching of $S1$ and $S2$, these two transistors work as diodes to transfer the energy. In this phase, the PEG starter helps the converter to collect enough energy from TEG to establish sufficiently high voltage for the control circuits in the following stages. With a stable temperature gradient and a continuous vibration during this period, the V_{CTRL} will increase to 600 mV eventually and the system transitions from cold start to internal-charging state.

3.3.2 Internal-charging state

As the system enters the internal-charging state, the PEG starter is disabled. Some control blocks start to function, such as the ZCS block, MPPT block, and the internal system oscillator, VCO, as shown in Fig. 3.16. Both of these internal circuits are powered by V_{CTRL}. The MUX on the gate of $S0$ selects the switching clock, $S0_G$, generated by the

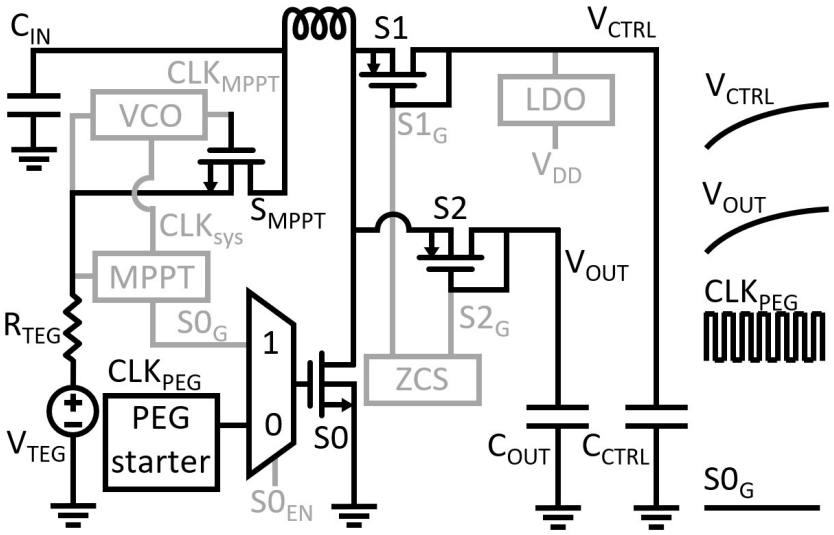


Figure 3.15: Phase diagram of the cold-start state of the system.

MPPT block to continue the operation of the boost converter. In this phase, the boost converter accelerates the charging process of C_{CTRL} as the switching frequency of $S0_G$ is much higher than that of CLK_{PEG}. Also, the switch $S1$ works in a more efficient way with the driving signal generated by the ZCS block than working as a diode. What's more, the boost converter operates in the discontinuous conduction mode as the power harvested by TEG is low [18]. The ON time of $S1$ is dynamically adjusted by the ZCS block to turn OFF the free-wheeling path so that the current in that path can neither drain energy from the capacitor in a negative direction nor flow to unwanted parts and waste energy.

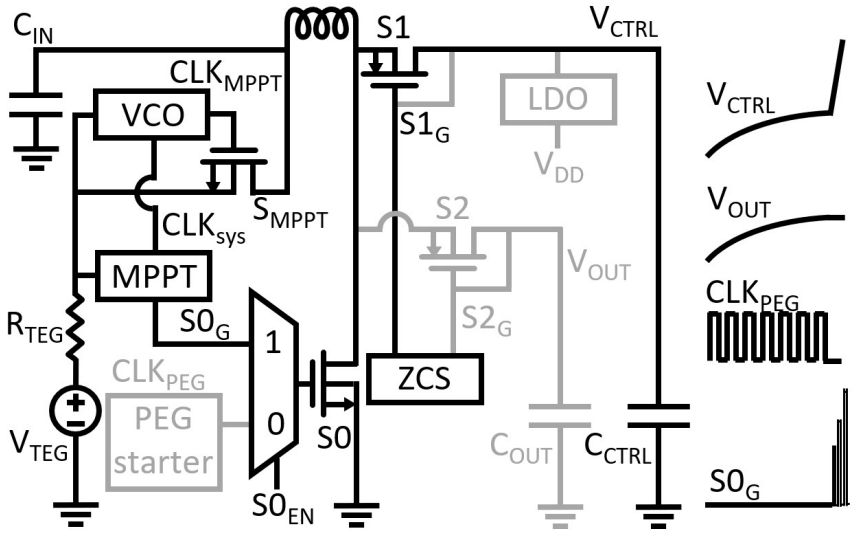


Figure 3.16: Phase diagram of the internal-charging state of the system.

3.3.3 External-charging state

The state detection block senses the rise of V_{CTRL}. As soon as V_{CTRL} reaches 1.3V, the system enters the external-charging state, as shown in Fig. 3.17. In this state, another energy harvesting path through high-side switch $S2$ is closed. The energy harvested by TEG is transferred to output capacitor C_{OUT}. It should be noticed that the amplitude of V_{CTRL} is influenced by the operation of the boost converter in two aspects. On one hand, the harvested energy is sent to charge the C_{OUT}, which means there is no energy input for C_{CTRL} in some cycles. On the other hand, the control circuits keep consuming energy stored in C_{CTRL}. As a result, the V_{CTRL} drops slowly. As C_{CTRL} provides energy for all the internal circuits, it should have the highest priority to maintain the amplitude of V_{CTRL}. Consequently, as long as V_{CTRL} drops below 1.3V, the energy harvesting path through $S2$ is closed temporarily, and $S1$ is activated to charge C_{CTRL} again until it is charged back to 1.3V. To avoid the impact of the fluctuation of V_{CTRL} on powering internal control circuits, a LDO is adopted to generate a stable supply, V_{DD}, which is 1.2V for the internal circuits. This LDO is activated as soon as the system enters external-charging state. What's more, the dynamic bulk biasing (DBB) technique is used to connect the n-well of $S1$ and $S2$ to a higher potential port between source and drain.

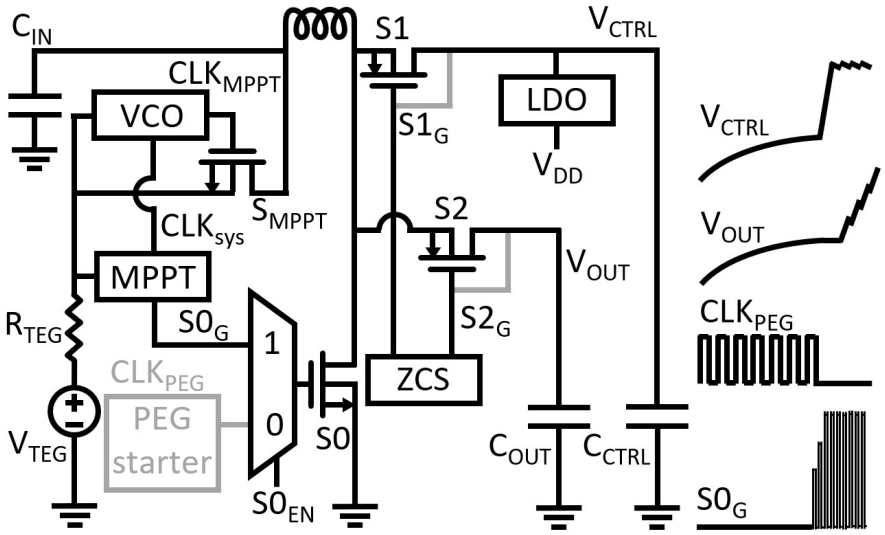


Figure 3.17: Phase diagram of the external-charging state of the system.

3.3.4 Output state

As V_{OUT} crosses 1.2V, the system enters output mode. In this stage, if V_{TEG} is stable and the input power is sufficient, the switches $S1$ and $S2$ will turn ON alternately to ensure the V_{CTRL} fluctuate around 1.3V and the output port can provide a stable 1.2-V supply. If the harvested power is insufficient for a period, the energy stored in the C_{OUT} will be consumed, and consequently, V_{OUT} starts to drop. As V_{OUT} drops below 1.2V, the system switches back to external-charging state and tries to maintain V_{CTRL}. If the input power

keeps too low, the V_{CTRL} also beings to drop. When V_{VTRL} decreases below 600 mV, the system goes to startup again. All other circuits are disabled, only the startup block keeps working to restart the system.

3.4 Efficiency Analysis

The end-to-end efficiency of the system, η_{SYS}, is defined by the multiplication of the MPPT efficiency, η_{MPPT}, and the efficiency of DC-DC converter, η_{DC-DC}, which can be expressed as

$$\eta_{SYS} = \eta_{MPPT} \times \eta_{DC-DC} \tag{3.4}$$

where η_{MPPT} determines how efficiently can the system harvest power from TEG and η_{MPPT} defines how much harvested power can be used for output. η_{DC-DC} and η_{MPPT} can be written as

$$\eta_{DC-DC} = \frac{P_{IN} - P_{LOSS}}{P_{IN}} \tag{3.5}$$

$$\eta_{MPPT} = \frac{P_{IN}}{P_{HAR}} \tag{3.6}$$

where P_{IN} is the input power of the DC-DC converter, P_{LOSS} is the power losses during the conversion and P_{HAR} is the theoretical maximum power that harvested from TEG. In order to maximize the η_{SYS}, both η_{MPPT} and η_{DC-DC} are supposed to achieve their maximum value in the operation.

3.4.1 MPPT Efficiency

According to the equivalent circuit of the TEG and the MPPT theory [19, 20], the maximum power can be extracted from the TEG when the input resistance of the DC-DC converter, R_{IN}, is equal to the internal resistance of TEG, R_{TEG}. And consequently, the theoretical maximum extractable power from TEG can be expressed as

$$P_{HAR,MAX} = \frac{V_{TEG}^2}{4R_{TEG}} \tag{3.7}$$

Since the boost converter working in the DCM, the maximum current, I_{peak}, flowing through the inductor is given by

$$I_{peak} = \frac{V_{IN}}{L} t_N \tag{3.8}$$

where V_{IN} is the input voltage of the boost converter, L is the value of inductor, t_N is the ON time of the NMOS transistor. The average current throughout the entire period, is represented as

$$I_{avg} = \frac{I_{peak}(t_N + t_P)}{2T} = \frac{V_{IN}(t_N + t_P)t_N}{2LT} \tag{3.9}$$

where T is the time period, and t_P is the ON-time of PMOS transistor. It is a common sense that the ON-time of PMOS switch is negligible compared to the ON-time of NMOS switch in the low-power energy harvester. Therefore, the input resistance is given by [21]

$$R_{IN} = \frac{V_{IN}}{I_{avg}} = \frac{2LT}{(t_N + t_P)t_N} \approx \frac{2Lf_{sys}}{D^2} \tag{3.10}$$

where f_{sys} is the switching frequency and D is duty cycle of NMOS switch. Based on the equivalent circuit of the TEG and the harvester, the actual input power provided by the TEG is derived as

$$P_{IN} = \frac{R_{IN}V_{TEG}^2}{(R_{IN} + R_{TEG})^2} \tag{3.11}$$

The η_{MPPT} can be rewritten using (3.7), (3.10) and (3.11) as

$$\eta_{MPPT} = \frac{8R_{TEG}Lf_{sys}D^4}{(2Lf_{sys} + R_{TEG}D^2)^2} \tag{3.12}$$

For a DC-DC converter with a fixed value of the inductor and R_{TEG}, by fixing either D or f_{sys} and adjusting another parameter, the input resistance matching can be easily achieved. For instance, for a fixed value of $f_{sys} = 5kHz$, the maximum MPPT efficiency, as well as input matching, is achieved by tuning D of the NMOS switch, as shown in Fig. 3.18.

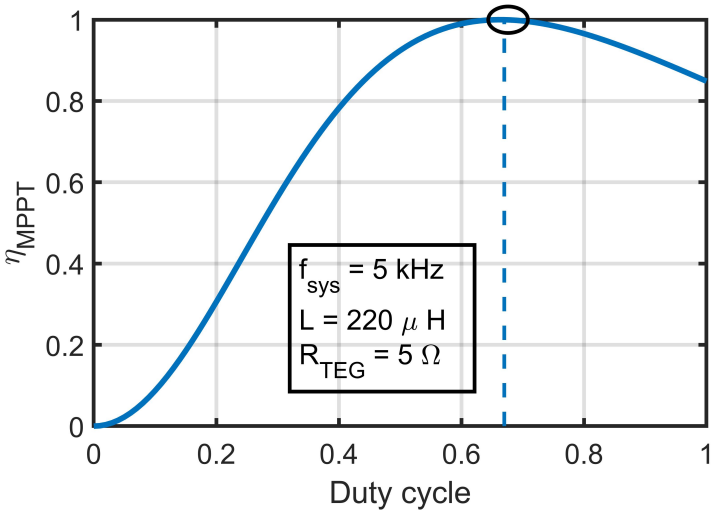


Figure 3.18: Optimum MPPT efficiency is achieved by varying duty cycle with a fixed f_{sys}.

3.4.2 DC-DC Converter Efficiency

Apart from using the equivalent circuit to calculate the input power, it can also be represented by the ratio of the transported energy over a clock period, which can be written

as

$$P_{IN} = \frac{V_{IN}(t_N + t_P)I_{peak}}{2T} \approx \frac{V_{IN}^2 t_N^2}{2LT} \tag{3.13}$$

Power losses in the operation of a boost converter are mainly composed of leakage currents, synchronization losses, conduction losses, and switching losses [22]. The power losses caused by leakage current are negligible since the energy harvesting system works at an ultra-low-power level. The synchronization losses can be neglected if the timing scheme is organized properly. Therefore, only the conduction loss, P_C, and switching loss, P_{SW} are taken into consideration to improve the converter efficiency.

The conduction losses are mainly caused by the ON-resistance of NMOS and PMOS transistors in the path. For NMOS transistors, the conduction losses, P_{CN}, is derived as

$$P_{CN} = \frac{1}{T}\int_0^{t_N} \left(\frac{V_{IN}}{L}t\right)^2 R_N dt = \frac{V_{IN}^2 t_N^3 R_N}{3L^2 T} \tag{3.14}$$

where R_N is the total ON-resistances of the NMOS transistors. The PMOS conductions losses, P_{CP}, is similarly expressed as

$$\begin{aligned} P_{CP} &= \frac{1}{T}\int_0^{t_P} \left(\frac{V_{OUT} - V_{IN}}{L}t\right)^2 R_P dt \\ &= \frac{(V_{OUT} - V_{IN})^2 t_P^3 R_P}{3L^2 T} \end{aligned} \tag{3.15}$$

where R_P is the total ON-resistances of the PMOS transistors. Assuming that $V_{OUT} \gg V_{IN}$, the P_{CP} can be rewritten as

$$P_{CP} \approx \frac{V_{OUT}^2 t_P^3 R_P}{3L^2 T} \tag{3.16}$$

The relation between t_N and t_P in a DCM boost converter is given as

$$\frac{t_N}{t_P} = \frac{V_{OUT} - V_{IN}}{V_{IN}} \tag{3.17}$$

Thus, the P_C can be written in terms of V_{IN} and t_L as

$$P_C = P_{CN} + P_{CP} = \frac{V_{IN}^2 t_N^3}{3L^2 T}(R_N + \frac{V_{IN}}{V_{OUT}}R_P) \tag{3.18}$$

Due to the large size of the power transistors used in the converter, the gate capacitors consume a large amount of power while driving the switches. By defining the total equivalent gate capacitance that is driven in each cycle as C_G, the total switching losses can be expressed as

$$P_{SW} = C_G V_{OUT}^2 f_{sys} \tag{3.19}$$

By adding up the conduction losses and switching losses, the total power losses of the boost converter is derived as

$$\begin{aligned} P_{LOSS} &= P_C + P_{SW} \\ &= \frac{V_{IN}^2 t_N^3}{3L^2 T}(R_N + \frac{V_{IN}}{V_{OUT}} R_P) + C_G V_{OUT}^2 f_{sys} \end{aligned} \tag{3.20}$$

Thus, the η_{DC-DC} can be reformulated as

$$\begin{aligned} \eta_{DC-DC} &= 1 - \frac{P_{LOSS}}{P_{IN}} \\ &= 1 - (\frac{2t_N}{3L}(R_N + \frac{V_{IN}}{V_{OUT}} R_P) + \frac{2LC_G V_{OUT}^2}{V_{IN}^2 t_N^2}) \end{aligned} \tag{3.21}$$

3.4.3 Overall Efficiency Optimization

Assuming that the MPPT block works perfectly, the input resistance matches the TEG internal resistance, $R_{IN} = R_{TEG}$, thus the harvester's overall efficiency can be rewritten using (3.10) in terms of D and f_{sys} as

$$\begin{aligned} \eta_{SYS} &\approx \eta_{DC-DC} \\ &= 1 - (\frac{4(R_N + \frac{V_{TEG}}{2V_{OUT}} R_P)}{3R_{TEG}} \frac{1}{D} + \frac{4C_G V_{OUT}^2 R_{TEG}}{V_{TEG}^2} f_{sys}) \end{aligned} \tag{3.22}$$

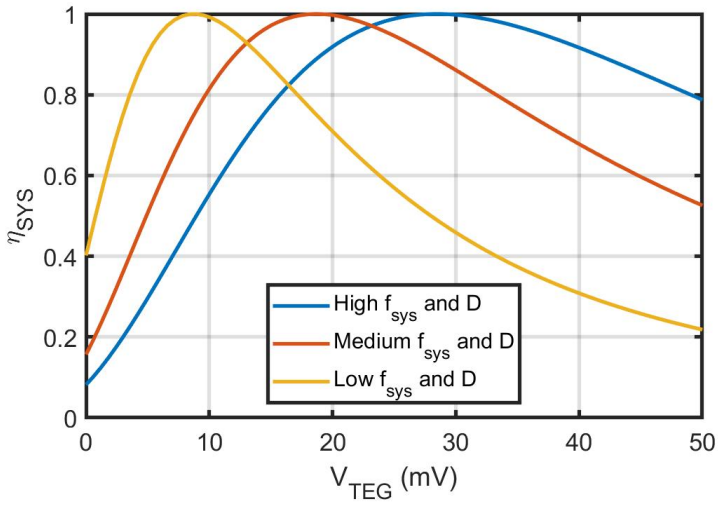


Figure 3.19: System overall efficiency versus TEG voltage. For different regions of V_{TEG}, the optimum combinations of f_{sys} and D changes.

which demonstrates that for different ranges of V_{TEG}, different kinds of losses dominate. For example, if the TEG voltage is at an extreme low level (e.g. 10-30 mV), the switching

losses become the main reason that impedes the efficiency improving. To reduce the converter losses while keeping the input matched as derived in (3.10), a smaller value of f_{sys} together with a reduced D can effectively reduce the switching loss and improve the converter efficiency, as shown in Fig. 3.19. The decrease in D does not induce too much conduction loss because of the low value of V_{TEG}. As the V_{TEG} goes higher, the previous set of D and f_{sys} becomes no longer appropriate for low power losses. As shown in Fig. 3.19, the conduction loss starts to dominate. Consequently, a larger value of D together with a proportional increased f_{sys} are beneficial to decrease the dominant conduction loss while maintaining the input resistance matched. The increase in frequency also does not affect the switching loss since the V_{TEG} is large.

Hence, a relation between V_{TEG} and f_{sys} can be found that as V_{TEG} increase, the f_{sys} also increase. Meanwhile, D and f_{sys} follows the (3.10) for MPPT. Also described in [23], the optimal switching frequency is nearly proportional to $V_{TEG}^{4/3}$. Therefore, In this design, a VCO is used to dynamically tune the operation frequency according to the TEG voltage. The MPPT block focuses on adjusting D for input matching.

3.5 Startup Analysis

The boost converter working principle is similar, no matter it works in the startup stage or output stage. The current that flows through the path mainly depends on the value of inductor, the voltage drop on it, and the conduction time of the switch. The only difference lies in the switching frequency of the converter which affects the value of peak current and the equivalent input resistance. Assuming that the harvester system is mounted on a surface with a fixed vibration frequency, the driving signal generated by the PEG stater shares the same frequency, f_{PEG}. The input resistance of the boost converter in the startup stage is given as

$$R_{IN,startup} = \frac{2Lf_{PEG}}{D^2} \tag{3.23}$$

Then, the input power can be rewritten using (3.10) as

$$P_{IN,startup} = \frac{2Lf_{PEG}V_{TEG}^2D^2}{(2Lf_{PEG} + R_{TEG}D^2)^2} \tag{3.24}$$

Based on the analysis of the working principle of the harvester, the system only starts to harvest the thermoelectric energy with the self-generated clock when the internal power supply capacitor is charged to a minimum working value, $V_{CTRL,min}$. The lowest required energy is derived as

$$W_{startup} = \frac{1}{2}C_{CTRLl}V_{CTRL,min}^2 = P_{IN,startup}t_{startup} \tag{3.25}$$

where $t_{startup}$ is the time of the startup stage. Based on (3.24) and (3.25), the minimum startup TEG voltage can be formulated as

$$V_{TEG,min} = \sqrt{\frac{C_{CTRL}V_{CTRL,min}^2}{2t_{startup}} \cdot \frac{(2Lf_{PEG} + R_{TEG}D^2)^2}{2Lf_{PEG}D^2}} \tag{3.26}$$

By setting the f_{PEG} as the only variable and setting the rest parameters fixed values, the relation between the minimum TEG voltage for startup and the frequency of the clock signal generated by the PEG starter is shown in Fig. 3.20. It can be regarded as a negative correlation between $V_{TEG,min}$ and f_{PEG}.

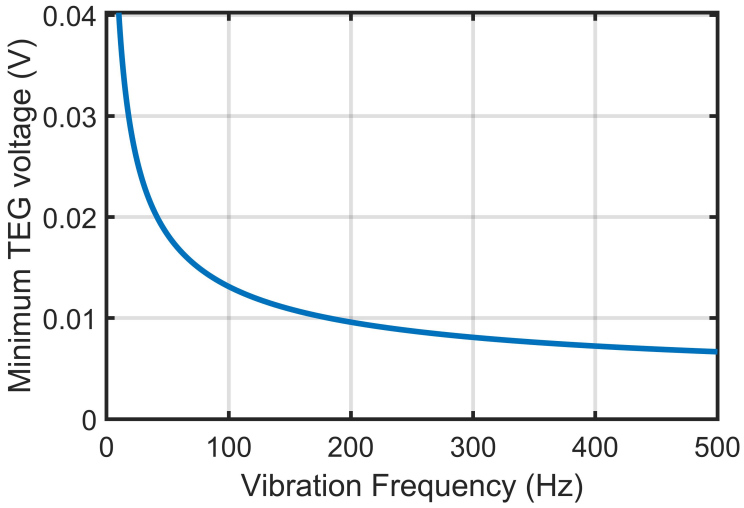


Figure 3.20: The minimum TEG voltage versus the startup frequency. As the vibration frequency rises, the required minimum TEG voltage decreases.

4 Block Level Design and Circuit Implementation

In this section, the contents mainly focus on the analysis of the specific blocks in the proposed energy harvesting system, including zero-current switching block, maximum power point tracking block, voltage-controlled oscillator and other peripheral blocks. The circuit implementations of the key components in each block are also introduced.

4.1 Zero-current Switching Block

In this design, the boost converter works in the discontinuous conduction mode, thus the energy harvesting path shall be cut off once the current that flows in the inductor reaches zero. Commonly, there are two methods to realize the zero current detection function. The first one is directly monitoring the current in the corresponding path with a current sensing circuit [24], which detects the polarity of the current and generates the switching signal. This approach has the fastest responding speed. However, the detector usually works continuously which makes it power consuming. Besides, the circuit complexity makes it difficult to design compared to the second method. Another way to achieve the zero current switching ability is measuring the polarity of the voltage difference on the PMOS transistors instead of sensing its current [25], as shown in Fig. 4.1. By comparing the voltage level on the source and drain of the PMOS switch, a signal is generated to adjust the ON time of the PMOS switch to avoid the negative current.

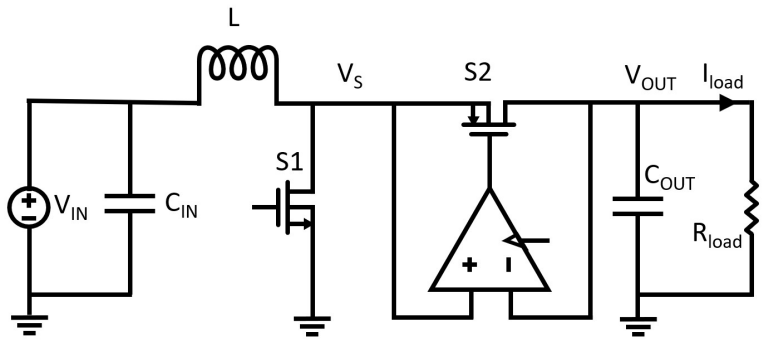


Figure 4.1: Schematic of a ZCS system.

4.1.1 Block Design

Fig. 4.2 illustrates the diagram of the ZCS block. In order to sense the polarity of the current flowing through the inductor, a compactor is used to compare the voltage on the drain and on the source of the PMOS transistor. It is important to note that there are two PMOS switches, which work for two different energy storage capacitors. Therefore, one of the inputs of the comparator is connected to the common source of $S1$ and $S2$, V_S. Another input is controlled by a MUX to choose either V_{CTRL} or V_{OUT} as the input, which is indicated by the state signal, S_{SEL}. In each cycle, the comparator generates an increasing or decreasing signal, INC/DEC, according to the polarity of the voltage

difference on the PMOS transistors. If the V_S is larger than the voltage of V_{CTRL} or V_{OUT}, the PMOS switch closes too early than desired, and its ON time will increase in next cycle. If the comparator generates a low level output, the PMOS switch closes too late, and its ON time will decrease in next cycle. The comparator is triggered by a delayed signal of the PMOS gate switching signals, either $S1_G$ or $S2_G$. This delay unit plays two roles in the operation of the comparator. On one hand, a small time slot is necessary to settle the V_S after the rising edge of the gate switching signal, since the V_S either exhibits an overshoot or an undershoot corresponding to the polarity of the current. On the other hand, the comparator needs a setup time after both inputs are settled. There are also two counters storing the delay codes for the gate switching signals in the next cycle, respectively.

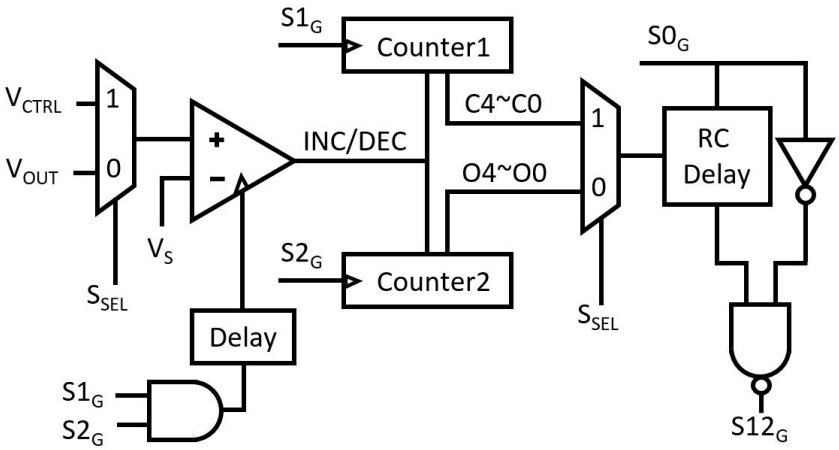


Figure 4.2: Circuit diagram of the ZCS block.

Fig. 4.3 depicts the waveforms of the ZCS block when the system works in the internal-charging state and only C_{CTRL} is being charged. As the NMOS gate driving signal, $S0_G$, goes low, the NMOS transistor is open. Meanwhile, the PMOS gate driving signal, $S1_G$, drops to conducting the inductor current. On the rising edge of $S1_G$, an overshoot appears at V_S because of the accumulation of the positive charges transferred by the residue positive current in the inductor. To solve this problem, the PMOS switch should stay closed for a longer period in the next cycle. Hence, a positive INC/DEC signal is generated. After the corresponding counter is refreshed, the programmable delay cell will enlarge the ON-time of the corresponding PMOS switching signal. In contrast, an undershoot at V_S indicates the negative current in the inductor once the PMOS switch is closed. Then the programmable delay cell will shorten the ON-time of $S1_G$ to avoid the reverse current flowing from the capacitor in the next cycle. Once V_{CTRL} and V_{OUT} are charged to steady states, the delay codes of the programmable delay cell will automatically switch between two adjacent values in consecutive clock periods.

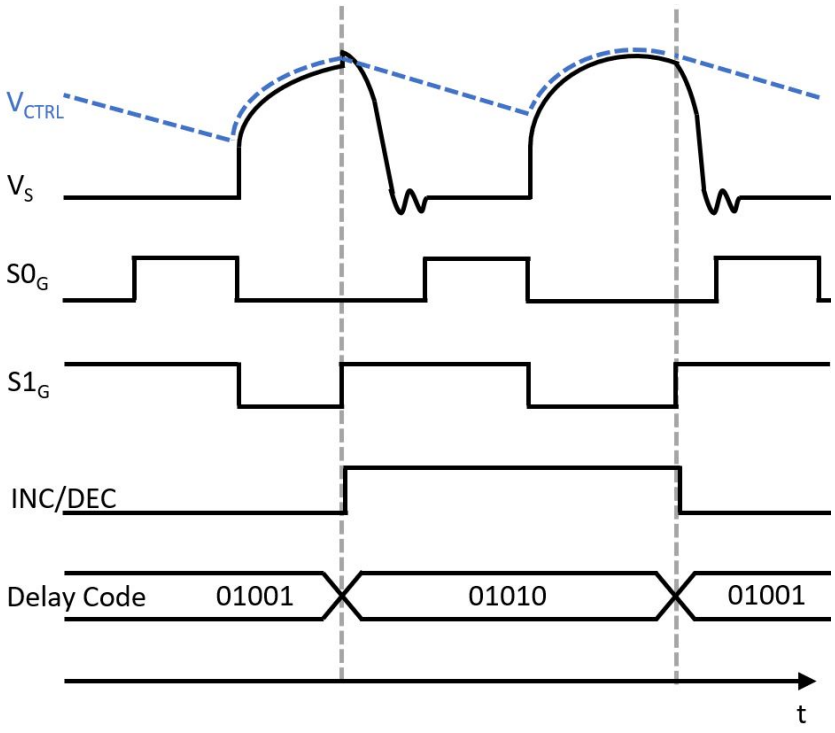


Figure 4.3: Timing diagram of the DCM operation.

4.1.2 Circuit Implementations

(1) Programmable delay cell. In order to accommodate a wide range of the clock frequency, a 5-bit counter is used to generate the required ON time with the programmable delay block, comprising 5 unit delay elements. The shortest one is capable of delaying the input pulse by 35 ns. The 5-bit up-down counter is realized with 5 D flip-flops and its logical circuits. The programmable delay block is shown in Fig. 4.4. Individual delay elements are enabled only when needed, saving power at low input voltages.

(2) Compactor. The comparator used in the ZCS block is StrongARM latch topology for the following reasons: 1) it consumes zero static power, 2) it directly produces rail-to-rail outputs, and 3) its input-referred offset arises from primarily one differential pair.

Fig. 4.5 shows the schematic of the StongARM comparator. The latch consists of a clocked differential pair, M_1 and M_2, two cross-coupled pairs, M_3 - M_4 and M_5 - M_6, and four precharge switches, S_1 - S_4. Transistors M_3, M_4 cut off the DC path between V_{DD} and ground at the end of the amplifying phase, avoiding static power drain. Transistors M_5 and M_6 restore the output high level to V_{DD}; without them, the discharge at X or Y would yield a degraded high level (lower than V_{DD}). Switches S_1 and S_2 play two roles: a) remove the previous states at nodes P and Q, suppressing dynamic offsets, and b) establish an initial voltage of V_{DD} at these nodes, allowing amplification before M_1 and M_2 enter

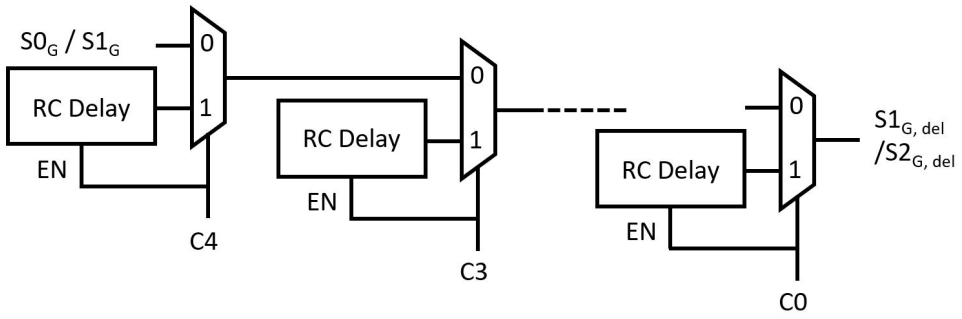


Figure 4.4: Schematic of the programmable delay cell.

the triode region. Switches S_3 and S_4 precharge X and Y to V_{DD}, ensuring that M_5 and M_6 remain off during the initial amplification and negligibly raise the offset.

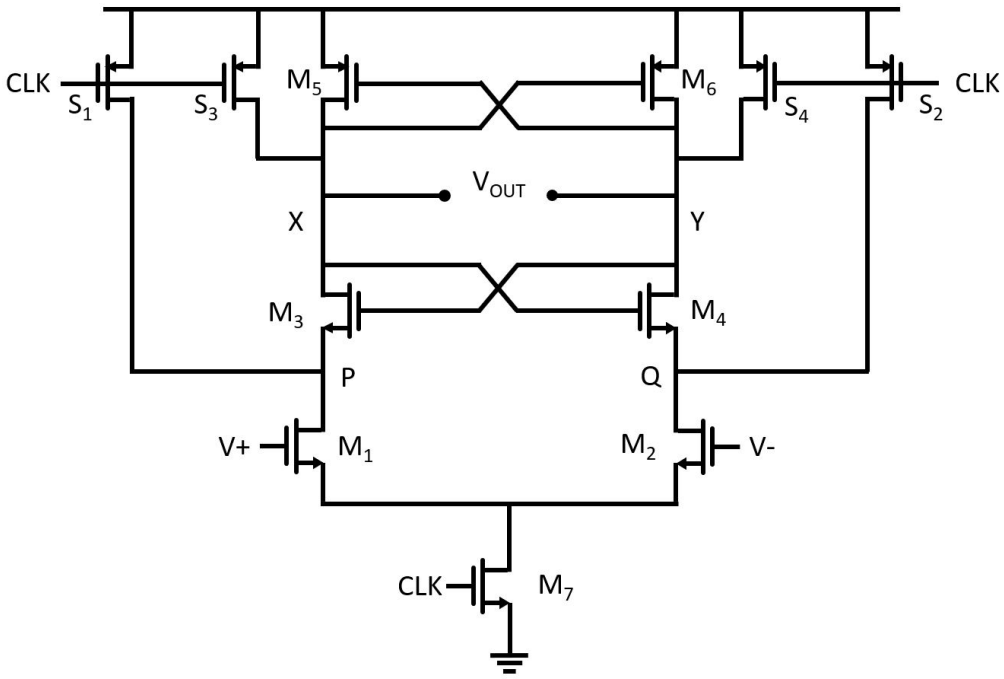


Figure 4.5: Schematic of a ZCS system.

The StrongARM latch generates invalid outputs ($V_X = V_Y = V_{DD}$)for about half of the clock cycle. For the subsequent logic to interpret the outputs correctly, an RS latch must follow the circuit. Fig. 4.6 shows a typical arrangement where inverters serve as buffers between the two latches and allow the RS latch to toggle only if V_X or V_Y falls. The power consumed by the StrongARM latch arises from primarily the charge and discharge of the capacitances. It is therefore roughly equal to

$$P_{comp} = f_{CLK}(2C_{P,Q} + C_{X,Y})V_{DD}^2 \tag{4.1}$$

where f_{CLK} is the clock frequency and the factor of 2 accounts for the discharge of both P and Q to near ground in every cycle.

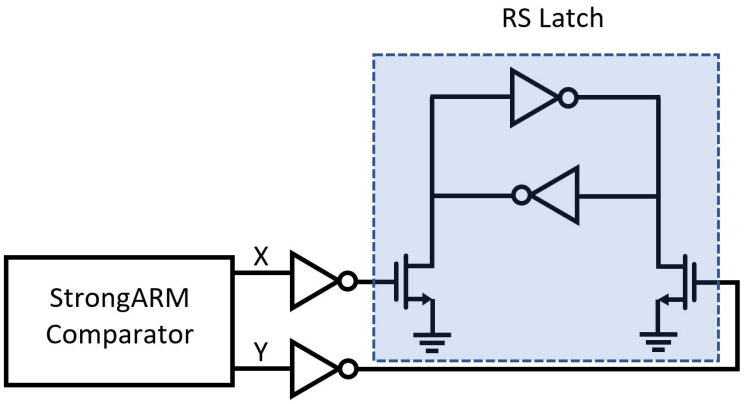


Figure 4.6: The StrongARM comparator followed by the RS latch.

4.2 Maximum Power Point Tracking Block

During the process of converting thermal energy into electrical energy by the thermoelectric generator, the temperature of the hot and cold ends of the thermocouple is constantly changing due to factors such as ambient temperature variation and heat dissipation, so the output patterns are not ideal. In order to improve the utilization of energy, the thermoelectric generator needs to work at the maximum power point as much as possible. Therefore, the MPPT technique is often implemented in the circuit to ensure that the TEG supplies power to the load with the maximum power.

4.2.1 MPPT Technique Analysis

Commonly used MPPT methods include Perturb-and-observe method, incremental conductance method and open circuit voltage method[26].

(1) The Perturb-and-observe method [27], also known as the hill climbing method, refers to adding voltage disturbance at the output of the energy harvester, monitoring the output voltage and output current of the energy harvester in real time, so as to obtain the output power $P1$ after disturbance. The previous output power $P0$ is compared with the disturbed power $P1$ to obtain the power change direction. The working state of the energy harvester is adjusted through the control circuit, so that it always works at the maximum power point. The Perturb-and-observe method has high control accuracy, but the power consumption of the circuit is relatively large, so it is not suitable for the low-power harvester system.

(2) The incremental conductance method is to track the maximum power point by calcu-

lating the instantaneous conductance and the change of the conductance of the collector [28]. When the harvester operates at the maximum power point, its Power-Voltage characteristic curve slope is zero. Since $dP = VdI + IdV$, it can be found that $\frac{dP}{dV} = V\frac{dI}{dV} + I$. When working at the maximum power point, $dP/dV = 0$. Therefore, $\frac{dI}{dV} = -\frac{I}{V}$. The incremental conductance method is to determine whether the system works at the maximum power point according to the relationship between $\frac{dI}{dV}$ and the output voltage and current, so as to adjust the output of the collector to make it work at the maximum power point. This method has precise control and fast response speed, but it requires high hardware precision and complex circuit design.

(3) The open circuit voltage method regulates the output voltage of TEG based on a constant ratio to the measured open circuit voltage[29]. Fig. 4.7a shows the equivalent circuit of a TEG harvester. V_{TEG} is the open circuit voltage of TEG, R_{TEG} is the internal resistance of TEG, and R_{load} is the equivalent resistance of the load circuit. V_{IN} is the input voltage of the harvester. The relation between V_{IN} and TEG output power P_{TEG} at $V_{TEG} = 10mV$ is shown in Fig. 4.7b. It can be seen from the figure that the output power of TEG reaches the maximum value when $V_{IN} = 1/2V_{TEG}$ and $R_{TEG} = R_{load}$. This method is simple in principle and easy to use. It is the most widely used MPPT method for TEG. Therefore, It is also used in this project.

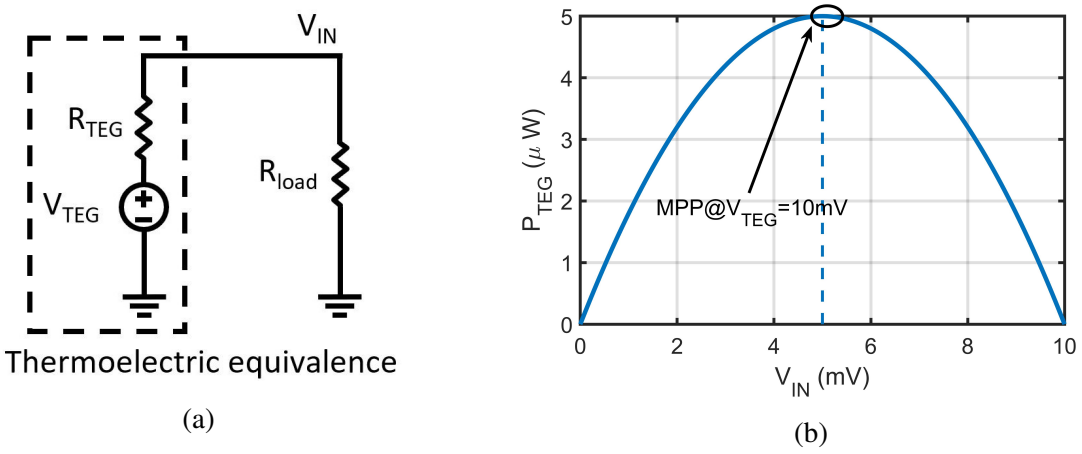


Figure 4.7: (a) PEG equivalent electrical model. (b) Simplified model.

4.2.2 Block Design

(3.10) points out that the value of R_{IN} relays on the duty cycle of the converter for a given switching frequency. In other words, the input voltage of the converter shall be maintained equal to a half of the TEG voltage by tuning duty cycle, D. Hence, a sample-and-hold circuit is utilized to periodically sample half of V_{TEG} on C_{sample}, thus $V_{sample} = 1/2V_{TEG}$, as shown in Fig. 4.8. Then it is compared with V_{IN} to decide the ON-time for Switch $S0$. If V_{IN} is large than $1/2V_{TEG}$, which means R_{IN} is larger than R_{TEG}, the comparator would generate a signal to add the counts in the 5-bit counter. Consequently, the programmable

delay cell increases the delay between CLK_{sys} and $CLK_{sys,del}$. Thus, the D increases, and R_{IN} decreases based on (3.10) and vice versa.

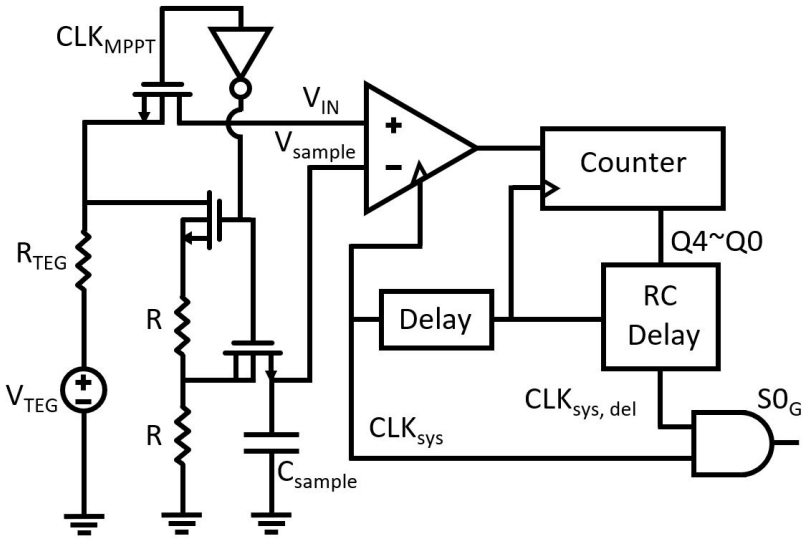


Figure 4.8: Schematic of a MPPT system.

Since the converter works in DCM, there is no energy transfer after the PMOS switches disconnect the energy harvesting path. The operation of the MPPT is triggered during the disconduction period in case of disturbing the energy harvesting process. What's more, the sample-and-hold circuit samples $1/2V_{TEG}$ every 512 system cycles as the temperature on TEG always changes gradually and thus V_{TEG} also changes with it. In contrast, the comparison between V_{IN} and V_{sample} takes place every cycle so that R_{IN} follows the change of R_{TEG} and the system tracking the maximum power point timely. Besides, the MPPT block is activated once the system enters internal-charging state, which facilitates the setup of V_{CTRL} and V_{OUT}.

4.3 Voltage-controlled Oscillator

4.3.1 Block Design

As described in the section of overall efficiency analysis, the DC-DC converter has different optimal operation frequencies for different input voltages. To minimize the power losses and improve the overall efficiency, f_{sys} is supposed to be dynamically adjusted with the varying V_{TEG}. It is noticed that instead of making a sophisticated circuit design to satisfy the precise relation, $f_{sys,optimal} \propto V_{TEG}^{4/3}$, as deducted in [23], a tradeoff is made to reduce the circuit complexity and maintain the high efficiency of the converter by simplifying it to $f_{sys} \propto V_{TEG}$.

4.3.2 Circuit Implementations

The schematic of the VCO used in this design is shown in Fig. 4.9. The VCO mainly consists of two parts, one is the biasing current generator, another is the ring oscillator. The amplifier together with its feedback loop makes up a voltage-to-current generator. The generated current is V_{TEG}/R which is replicated by a current mirror to bias the ring oscillator. Thus, the output frequency of the oscillator is proportional to the biasing current, which can be expressed in

$$f_{sys} = \frac{V_{TEG}}{RC_{OSC}V_{DD}} \tag{4.2}$$

where C_{OSC} is the capacitor in the oscillator.

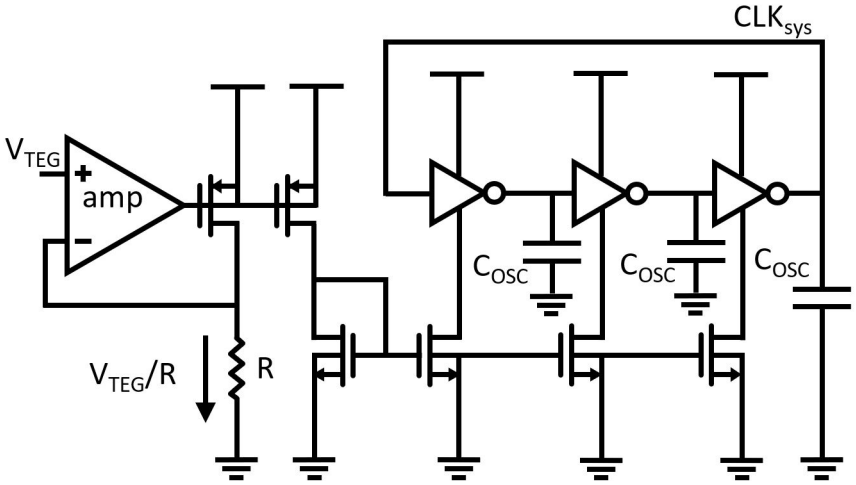


Figure 4.9: Circuit implementations of the VCO.

4.4 Voltage Reference Generator

The voltage reference generator (VRG) is a crucial building block in the harvester system, since the system states is indicated by the comparison between the reference voltage, V_{ref}, and the voltage on the storage capacitor, V_{CTRL} or V_{OUT}. Due to the fact that energy harvester startups with zero energy stored in the system, a key requirement to the VRG in this project is that it can function normally under a low power supply. In this work, the system is supposed to transfer from Startup Stage to the Internal-charging Stage at $V_{CTRL} = 600mV$, thus the VRG shall has a minimum working voltage, $V_{DD,min}$, smaller than 600 mV, and the V_{ref} is also smaller than 600 mV. It is commonly known that the minimum reference voltage obtained from a bandgap reference is around 1.25 V [30], as a result, the conventional topology is not suitable in this design. Some sub-600 mV voltage reference techniques are analysed and compared in the flowing subsection.

4.4.1 Voltage Reference Technique Analysis

(1) Bonba topology. An alternative way to circumvent the silicon bandgap limitation is by summing temperature-dependent currents instead of voltages. Fig. 4.10 shows a BGR that was proposed by Banba *et al.* [31] to realize current-mode summation using resistive subdivision. The complementary to absolute temperature (CTAT) current I_2 and the proportional to absolute temperature (PTAT) current I_1 are combined in transistor $M2$ and mirrored to transistor $M3$ where the temperature-independent current is converted to voltage through the resistor R_4. The resulting voltage reference is

$$V_{ref} = R_4(\frac{V_{BE1}}{R_2} + \frac{\Delta V_{BE}}{R_3}) \tag{4.3}$$

where V_{BE1} is the base-emitter voltage, values of resistors R_2 and R_3 can be chosen to nullify the temperature dependence around a certain temperature, and R_4 is chosen to scale the voltage to the desired level. Due to this added degree of freedom, this topology allows realizing reference voltages below the limit set by the silicon bandgap i.e. 1.25 V. However, this design suffers from several shortcomings as the voltage supply scales down. The minimum supply voltage is

$$V_{DD,min} = V_{BE1} + V_{Dsat} \tag{4.4}$$

where V_{Dsat} is the overdrive voltage above the transistor saturation level. For $V_{BE1} \approx 0.7V$ and $V_{Dsat} \approx 0.1V$, a $V_{DD,min} \approx 0.8V$ which is the minimum supply voltage limit for this topology. What's more, the power consumption of this topology is up to 60 μW [32], which is not affordable in the low-power energy harvesting system.

(2) Self-Biased NMOS Load Voltage Reference [33]. The simplified circuit schematic is shown Fig. 4.11. The selfcascode MOSFET (SCM) is composed of transistors with different threshold voltages: $M2$ is a high-VT transistor (5 V) and $M3$ is the standard one (1.8 V). V_{ref} is generated through the SCM connection of $M2$ and $M3$ which have the same gate-to-bulk voltage. The SCM, in turn, is biased by a current source that allow the control of the inversion coefficient of $M2$ and $M3$. The generation of a voltage reference through the SCM is a good choice for low power since it can operate at very low current levels. Therefore, this topology is employed in this design.

4.4.2 Circuit Implementation

Supposing that M_2 and M_3, as shown in Fig. 4.11, are saturated, both operate in weak-inversion (WI) and, with all voltages referenced to their bulk terminals, which are connected to ground, they can be written as

$$I_{D2} = 2eI_{S2}exp(\frac{V_{G2} - V_{T2}}{n_2\phi_t}) \tag{4.5}$$

$$I_{D3} = 2eI_{S3}exp(\frac{V_{G3} - V_{T3}}{n_3\phi_t} - \frac{V_{D2}}{\phi_t}) \tag{4.6}$$

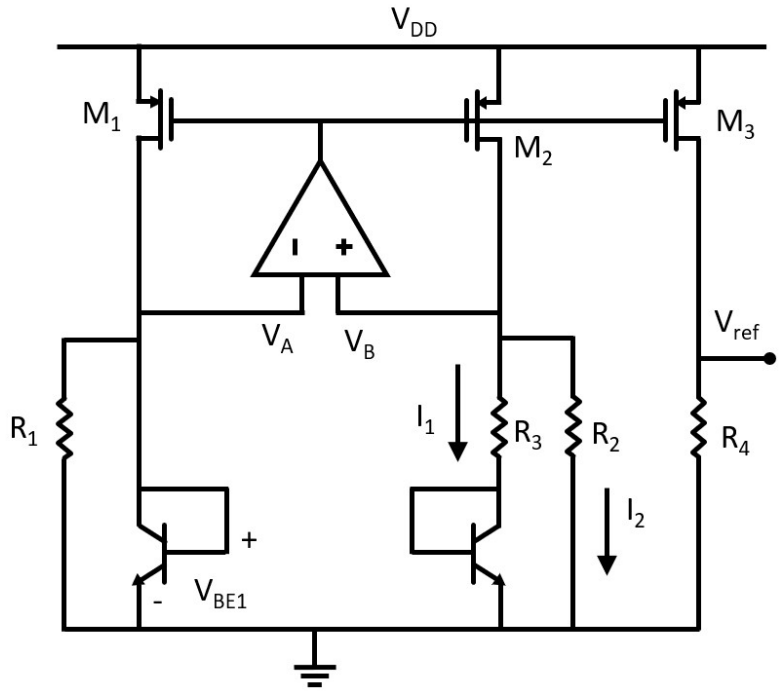


Figure 4.10: Low voltage BGR proposed by Banba *et al.* [31].

where e is the Euler's number, $I_S = I_{SQ}S$, I_{SQ} is the sheet normalization current, S is the transistor aspect ratio W/L, n is the subthreshold slope factor, V_G, V_S and V_D are the gate, source and drain voltages referenced to the bulk terminal, V_T is the threshold voltage, and $\phi_t = kT/q$ is the thermal voltage.

The NMOS load voltage V_{ref} is simply voltage V_{G2}, which is

$$V_{ref} = V_{T2} + n_2\phi_t ln(\frac{I_{D2}}{2eI_{S2}}) \tag{4.7}$$

The temperature behavior of (4.7) can be compensated since its first term is CTAT and its second, PTAT. Fig. 4.12 presents the complete circuit where all transistor operate in WI. Besides, M_1, which is a 5 V transistor, defines the bias current, M_4 acts as a cascode to shield M_1 from supply voltage variations, and transistors M_5 and M_6 act as a current mirror thus defining $K_1 = S_6/S_5$. The necessity of using the cascode transistor M4 arises from the fact that the line sensitivity of V_{ref} is directly dependent on the line sensitivity of the current source.

In the subthreshold region, the current of a MOS saturates when its drain-tosource voltage is greater than 3 to 4 times the thermal voltage, i.e. $V_{DS} \geq 3 \sim 4\phi_t$. Hence, in the self-

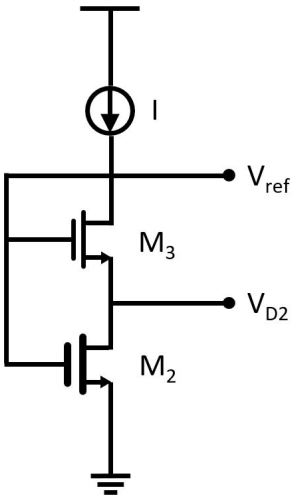


Figure 4.11: Simplified scheme of the voltage reference by Oliveira *et al.*

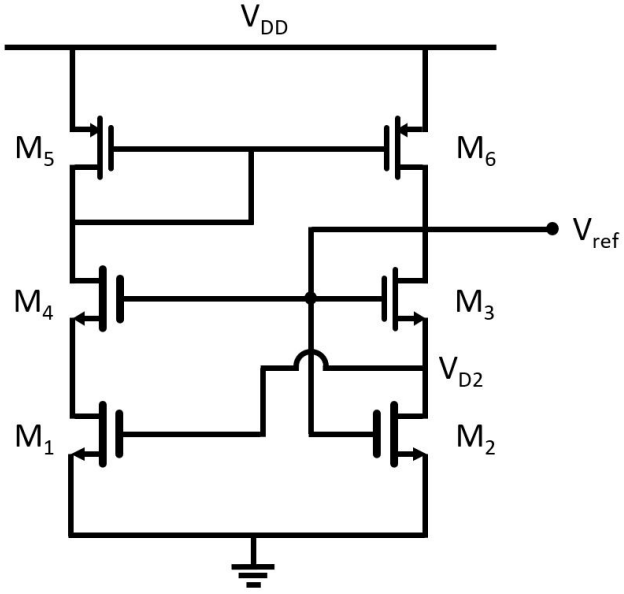


Figure 4.12: Schematic of the self-biased NMOS voltage references.

biased NMOS voltage referenc, we have

$$V_{DD,min} = V_{ref} + 4\phi_t \tag{4.8}$$

4.5 Low-dropout Regulator

To avoid the impact of the fluctuation of V_{CTRL} on powering internal control circuits, a LDO is adopted to generate a stable supply, V_{DD}, which is 1.2V for the internal circuits.

4.5.1 Block Design

The LDO structure is based on flipped voltage follower [34], as shown in Fig. 4.13. V_{IN} is the unregulated input voltage of the LDO. M_P is the power transistor, while M_{C1} and M_{C2} form a folded error amplifier in the common-gate configuration. The source of M_{C1} detects the LDO output for comparing with a control voltage defined at the gate of M_{C1}. An error signal is then generated at the gate of the power transistor to achieve closed-loop voltage regulation by the negative feedback.

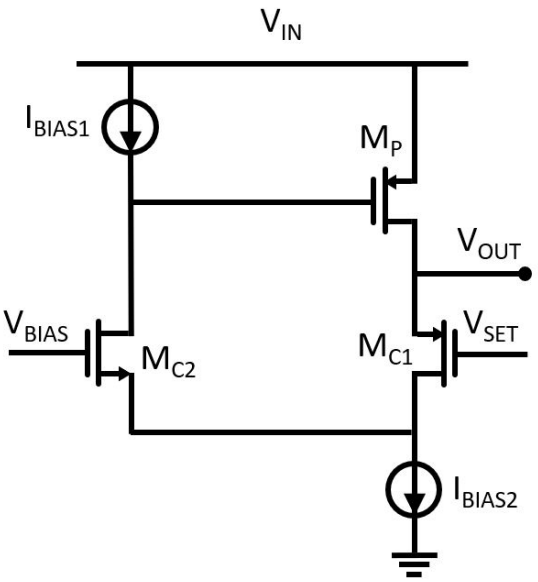


Figure 4.13: An output-capacitorless LDO reported in [34].

4.5.2 Circuit Implementation

The schematic of the LDO is shown in Fig. 4.14. M_P, M_{N1}, and M_{P3} form the core of the LDO. The bias currents in M_{N2}, M_{N3} and M_{P1} are set to be 2:1:1 so that the two identical transistors M_{P3} and M_{P4} will have the same V_{GS}. Therefore, the output voltage can be

expressed as

$$V_{DD} = V_{FB} = (1 + \frac{R_1}{R_2})V_{ref} \tag{4.9}$$

where R_1 and R_2 are two off-chip feedback resistors. The error amplifier (EA) is implemented with a single stage differential pair to lower the power dissipation.

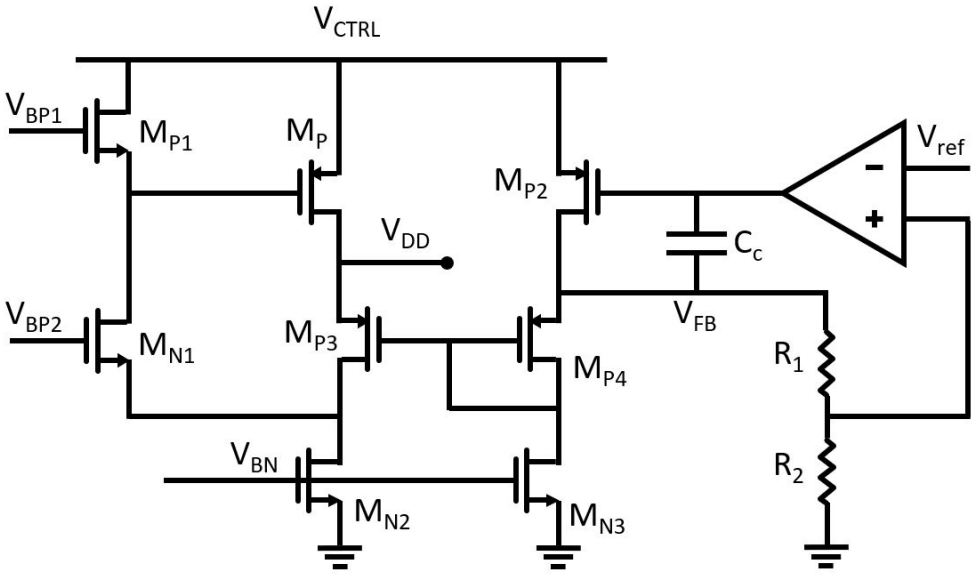


Figure 4.14: The schematic of the LDO with off-chip feedback resistors.

4.6 Peripheral Circuits

4.6.1 Dynamic Body Biasing

Usually, the body of NMOS transistors is applied to the most negative voltage in the circuit design, whereas the body of PMOS transistors should be applied to the most positive voltage. The body of the NMOS transistor in the boost converter is connected to the ground which is always the lowest voltage in the system. However, the voltage on the drain and source of the PMOS transistors in the boost converter is not fixed. For instance, the voltage at the source of the PMOS, V_S is higher than the voltage of the drain side, V_{VTRL} or V_{OUT}, when the PMOS is ON and charging the capacitor. In this case, the body of the PMOS transistors is supposed to connected with the source. Contrarily, V_S is lower when no current is flowing in the path. And thus, the body should tie to the capacitor side. The body of the PMOS transistors needs to be dynamically connected to the higher voltage level between the source and drain.

Fig. 4.15 shows the schematic the dynamic body biasing circuit. If the voltage at the left input, VL, is higher than the voltage at the right end, VR, the body of the PMOS switch is connected to the drain side and vise versa.

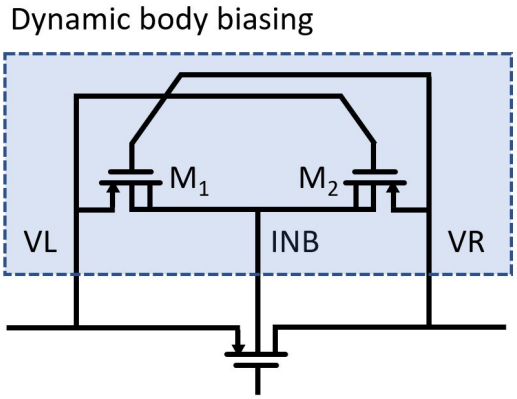


Figure 4.15: Dynamic body biasing diagram.

4.6.2 Gate Driver

In the energy harvesting system , the size of the power transistor is commonly very large. In this work, the NMOS switch in the boost converter has a size of $\frac{W}{L} = \frac{2mm}{180nm}$. To drive such large NMOS and PMOS power switches, the Fan-out of 4 strategy is used. FO4 is generally used as a delay metric because such a load is generally seen in case of tapered buffers driving large loads. As a delay metric, one FO4 is the delay of an inverter, driven by an inverter 4x smaller than itself, and driving an inverter 4x larger than itself. The circuit diagram is shown in Fig. 4.16. In order to drive a large NMOS switch with large gate capacitance, multistage buffers are applied with buffer 1 ($\frac{W}{L} = \frac{8\mu}{180nm}$), buffer 2 ($\frac{W}{L} = \frac{32\mu}{180nm}$), buffer 3 ($\frac{W}{L} = \frac{125\mu}{180nm}$), and buffer 4 ($\frac{W}{L} = \frac{500\mu}{180nm}$). Under this condition, $S0_G$ can have reasonably low delay and enough driving capability to drive the NMOS switch.

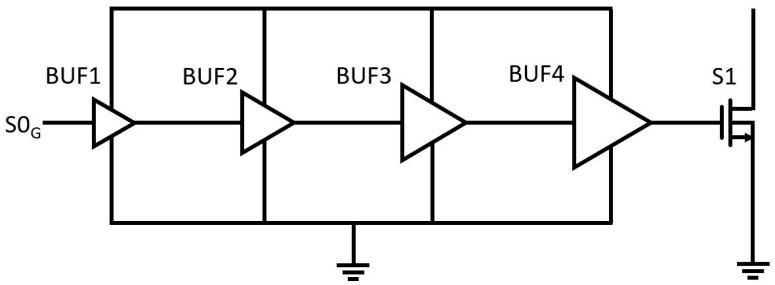


Figure 4.16: Gate driver diagram.

5 Measurement Results

In this section, the measurement setup of the proposed energy harvesting system is introduced in the first part. The test bench gives the details of how the system is measured with the components like the piezoelectric power generation platform and PCB implementation. The second part gives the measurement results and its performance analysis. The last section summarizes the performance of the system from the point of power consumption and overall efficiency. The comparison with the state-of-the-art works are given in the end.

5.1 Measurement Setup

Fig. 5.1 shows the schematic of the test bench of the thermoelectric energy harvester with a PEG starter. The input of the harvester is connected to a voltage source which simulates the voltage generated by the TEG. The internal resistance of TEG is realized by a serially connected resistor, R_{TEG}. The input of the PEG starter is connected to a piezoelectric power generation platform which consists of four parts: signal generator, power amplifier, vibration generator, and PEG which is made up of cantilever beam and piezoelectric material. The working process of the piezoelectric power generation platform is shown in Fig. 5.2: first, the signal generator generates a sinusoidal signal. Then, the sinusoidal signal is transmitted to the vibration generator after being boosted by a power amplifier, so that the cantilever beam is forced to vibrate. And finally, the piezoelectric material generates a signal which is directly connected to the input of the PEG starter. The output of the energy harvesting system is connected to a variable resistor which works as the load. Tbl. 5.1 shows the value of the components that used in the measurement. Fig. 5.3 illustrates the PCB layout based on the above described test bench.

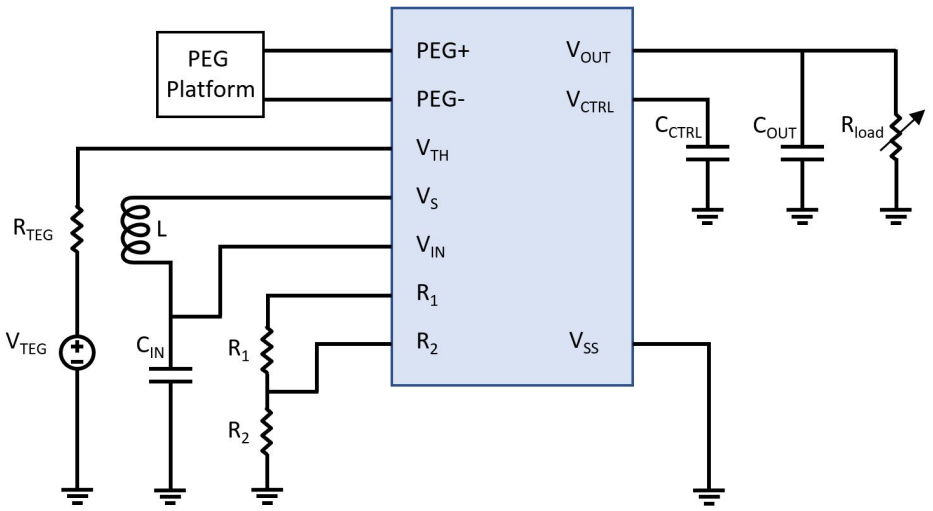


Figure 5.1: The schematic of test bench.

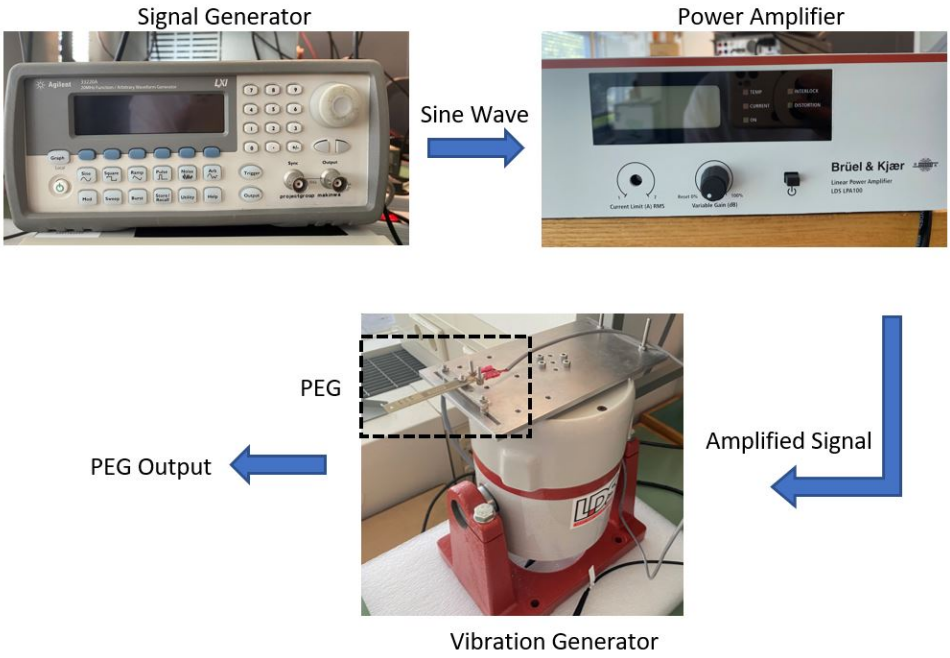


Figure 5.2: The working process of the piezoelectric power generation platform.

Table 5.1: Values of the passive components in the test bench

Components	Value
R_{TEG}	5Ω, 10Ω
L	$220\mu H$, 0.3Ω
C_{IN}	$50\mu F$
C_{CTRL}	$220nF$
C_{OUT}	$220nF$
R_1	$84M\Omega$
R_2	$40M\Omega$

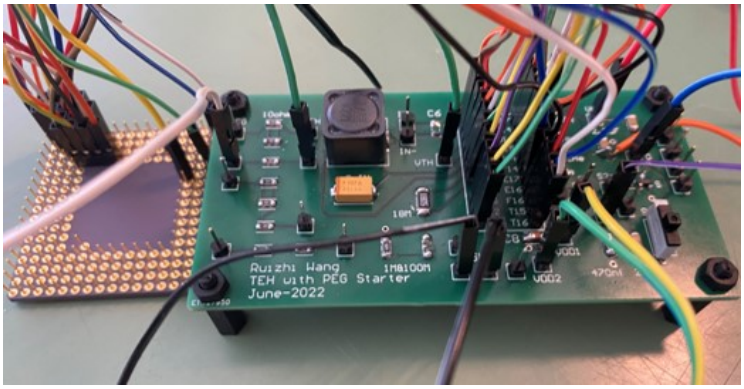


Figure 5.3: The PCB layout of the test bench.

5.2 Measurement Performance

The thermoelectric energy harvesting system is implemented in a 180-nm CMOS process. A die micrograph is shown in Fig. 5.4; the harvester system occupies an active area of 0.4 mm^2.

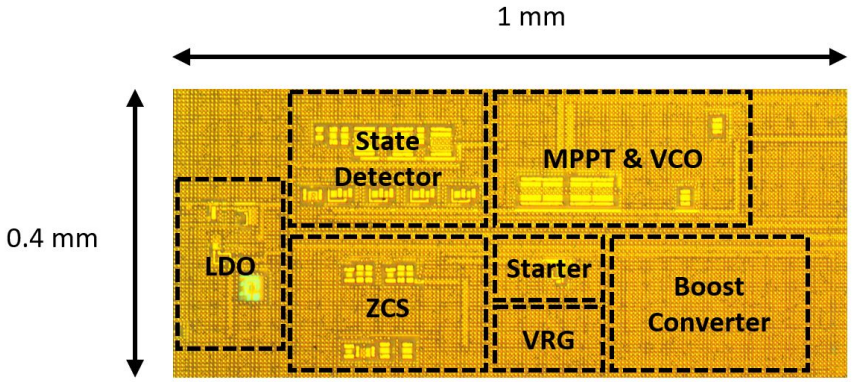
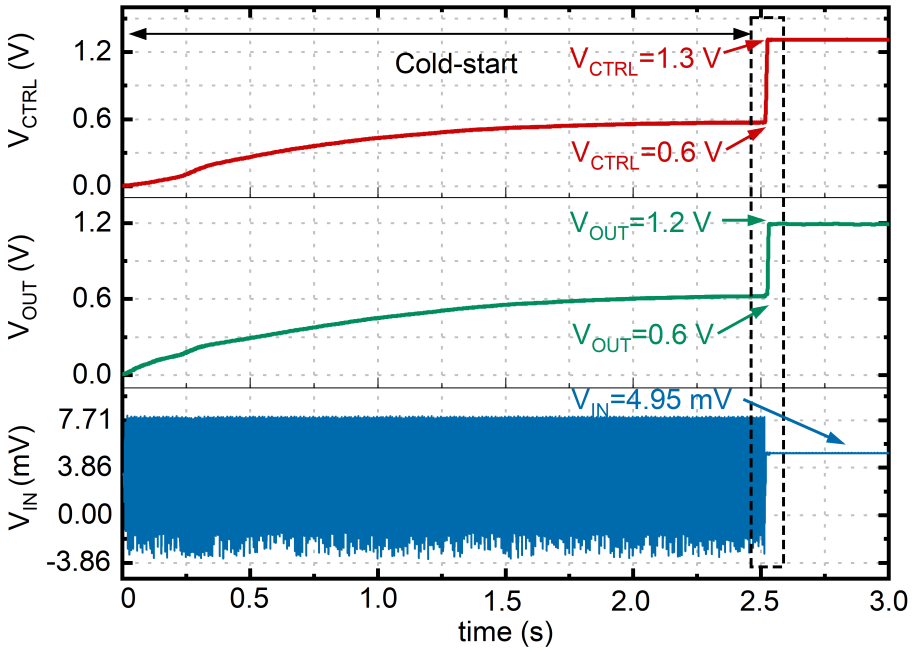


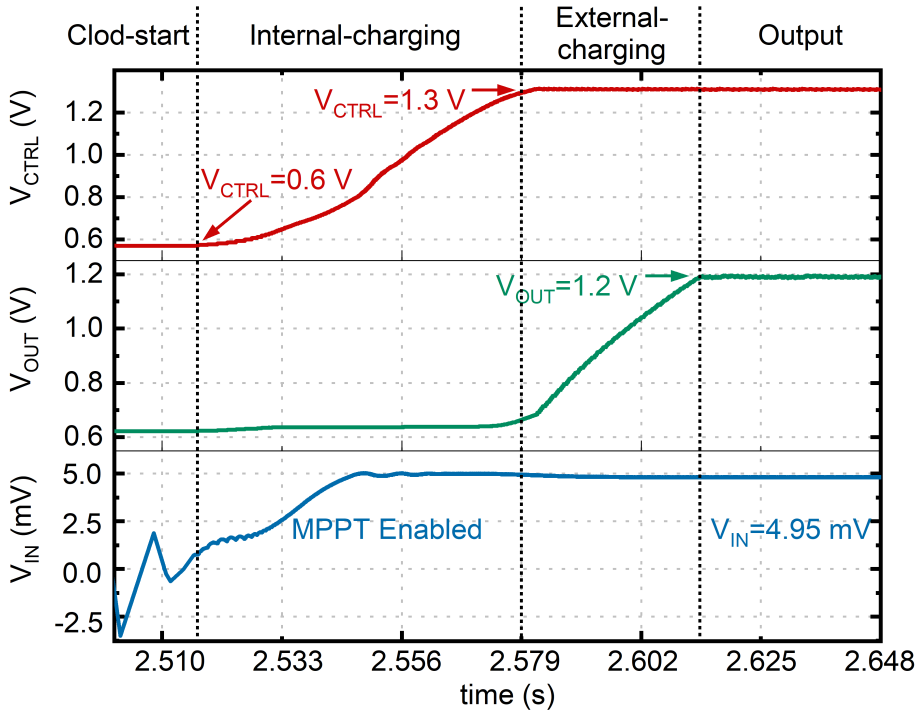
Figure 5.4: Die micrograph of the harvester system.

5.2.1 Measured Cold-startup Performance

Fig. 5.5 shows the key signals during the cold-startup of the system. The achieved minimum V_{TEG} for cold-startup is 10 mV. It takes 2.63 s in total for the whole system to startup from zero-energy-stored state to normal-output state. The startup time mainly depends on 3 parameters: One is the value of the energy storage capacitor. The larger the capacity, the longer it takes to reach the demanded voltage. Another major factor is the input power. At the minimum startup voltage, the system can acquire very limited power from the environment which increases the startup time. The final one is the frequency of vibration. As deducted in (3.26), a higher PEG startup signal frequency is able to speedup the voltage building of V_{CTRL} at the startup stage.



(a)



(b)

Figure 5.5: Startup waveform at $V_{TEG} = 10$ mV. (a) Full waveforms from the cold state to the normal operation state. (b) Zoomed-in waveforms showing the details at the internal-charging and external-charging state.

At the startup state, only the PEG startup circuit works, as shown in Fig. 5.5b. This stage takes up the longest time during the startup, even though there is no active power consumption in the circuit. The low switching frequency and high voltage drop on the PMOS diode impede the rising speed of V_{CTRL}.

As V_{CTRL} goes over 600 mV, the system enters the internal-charging state, as shown in Fig. 5.5a. The PEG starter is blocked in the following stages. All the control circuits are enabled, and the system clock is replaced by the signal generated by the internal oscillator. The MPPT is also enabled, which stabilizes the input voltage of the inductor, V_{IN} , at half of the TEG voltage. The MPPT maximizes the extractable power from the TEG source and reduces the time spent in this stage.

Once V_{CTRL} reaches 1.3 V, it stops increasing and is regulated by the ON-OFF control of ZCS block. During the external-charging state, the output voltage V_{OUT} keeps rising until it reaches 1.2 V. Eventually, in the output state, the output port is stabilized at 1.2 V.

5.2.2 Gate Switching Strategy

Fig. 5.6 shows the gate switching strategy of $S1$ and $S2$ in the external-charging state (which also applies to the output mode). When the V_{CTRL} is higher than 1.3 V, the state indicating signal, $S2_{EN}$, is high, and all the harvested energy is transferred to the output capacitor. With each switching of $S2_G$, the V_{OUT} increases step by step. Since V_{CTRL} is the power supply of the internal control circuit, it has the highest priority to maintain at a certain level. Once the V_{CTRL} drops below 1.3 V, the state detection signal $S2_{EN}$ is pulled down and disabling the $S2_G$ temporarily. Under such condition, the gate driving signal of switch S1, $S1_G$, is enabled to transfer the harvested energy to C_{CTRL} and boost V_{CTRL} to a value that is higher than 1.3 V. This may takes more than one cycle. After the V_{CTRL} increases over 1.3 V, the $S2_{EN}$ is switched back to the high state and continues the charging of V_{OUT}.

5.3 Performance Summary and Comparison

5.3.1 Power Breakdown

Fig. 5.7 shows the breakdown of the power distribution at $V_{TEG} = 10mV$. The utilization of the harvested power is shown in Fig. 5.7a, where the 63.9% of the harvested power is used for output. Among the rest 36% power consumption, 4% power loss is due to the imperfection of MPPT, and 32% power consumption is caused by the control of the system operation. Fig. 5.7b depicts the simulated breakdown of control power by block. Since the power switches have very large size, 41% of the control power consumption is used on the gate drivers of those power switches. The VCO consumes the second largest portion of control power which is 24%. The ZCS block and MPPT block take up 7% and 6%, respectively.

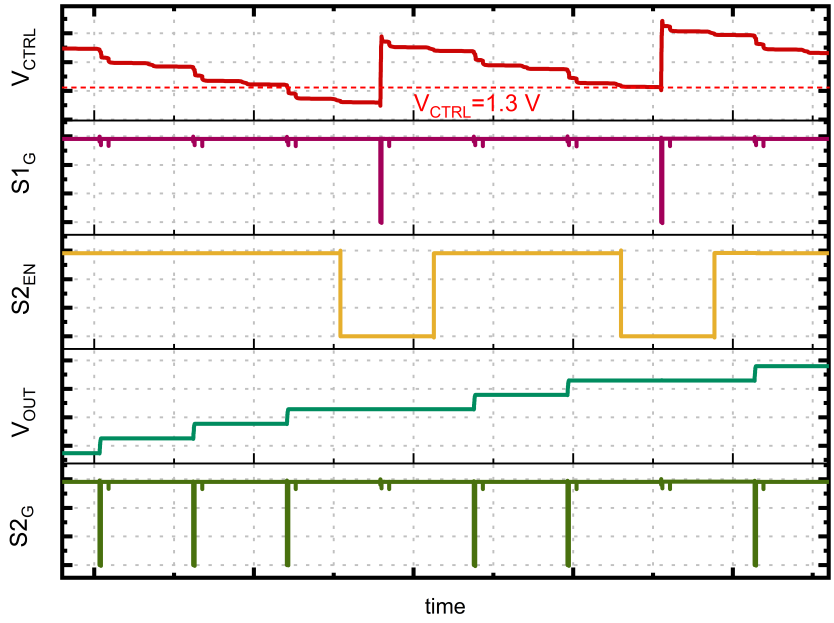
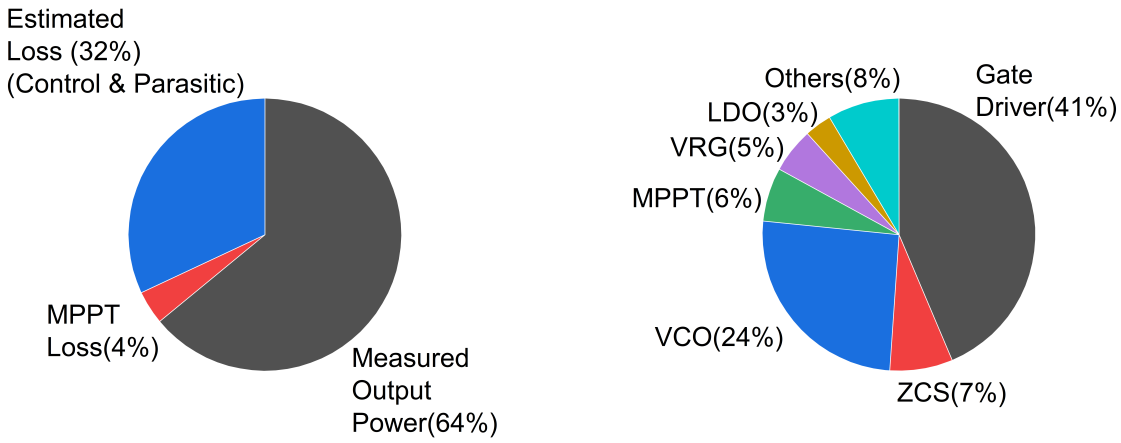


Figure 5.6: The gate switching strategy in the external-charging state.

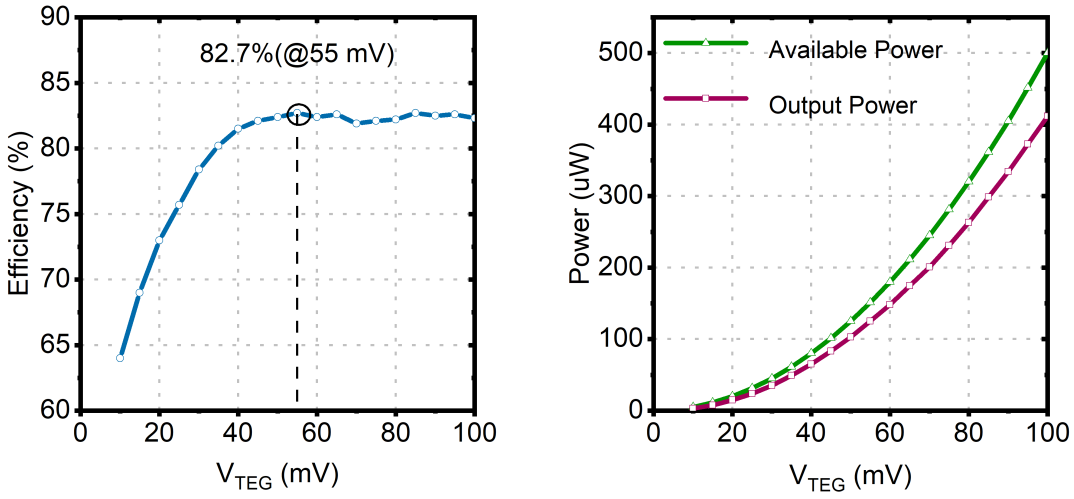


(a) (b)

Figure 5.7: The breakdown of the power distribution at $V_{TEG} = 10mV$ (a) Measured output power with estimated loss. (b) Simulated breakdown of control power by block.

5.3.2 Measured Efficiency

The efficiency of the boost converter was measured using a variable resistor as load. The maximum available output power for different values of V_{TEG} was measured by varying the load resistance at each V_{TEG}. The overall efficiency of the energy harvesting system is the ratio of the maximum available output power to the ideal maximum available input power from TEG. The variation of the overall efficiency along with the increasing V_{TEG} is plotted in Fig. 5.8a. It is noteworthy that the harvester can not only startup at an ultra-low V_{TEG} at 10 mV but also achieve an efficiency of 63.9%. The peak efficiency is reached at $V_{TEG} = 55mV$, and the value is 82.7%. For the TEG voltage that is larger than 35 mV, the overall efficiency is maintained over 80%. Fig. 5.8b shows the variation of the maximum output power versus the TEG voltage.



(a) (b)

Figure 5.8: (a) Measured efficiency of the system versus TEG voltage. (b) Measured output power of the boost converter versus TEG voltage.

5.3.3 Comparison

The comparison of the performance with the state-of-the-art works is demonstrated in Tbl. 5.2. Among all of these designs, our work achieves the lowest startup voltage which only needs a 10 mV TEG voltage to startup the system, while other designs need at least 35 mV to activate the system. This advantage is more significant if the comparison of the minimum startup voltage is limited within the on-chip integrated designs. Meanwhile, the overall efficiency at the minimum TEG voltage of proposed system also has the highest value. Compared with the efficiency at the lowest input voltage achieved in other designs which are at a level of around 40%, this work reaches an overall efficiency of 63.9%. As for the peak efficiency, a value of 82.7% is achieved, which is the third highest in all works.

Table 5.2: Comparison with the State-of-the-art works

	JSSC 2011 [12]	Analog Devices [35]	JSSC 2013 [13]	ISLPED 2014 [36]	JSSC 2018 [37]	TCAS 2018 [25]	JSSC 2019 [23]	JSSC 2021 [16]	JSSC 2021 [38]	**This Work**
Process	0.35 μm	N/A	65 nm	N/A	65 nm	65 nm	0.18 μm	0.18 μm	0.13 μm	**0.18 μm**
R_{TEG}	5 Ω	2 Ω	6.2 Ω	1 Ω $\sim$ 5 Ω	2.2 Ω	5 Ω	210 Ω	5 Ω	200 Ω	**5 Ω**
No. of Magnet Components	2	2	3	1	2	1	1	1	1	**1**
MPPT	YES	NO	YES	YES	YES	YES	YES	YES	YES	**YES**
Adaptive Switching Frequency	NO	N/A	YES	N/A	NO	YES	YES	YES	YES	**YES**
Peak Efficiency	58%	55%	73%	68%	75%	71.5%	84%	80%	90%	**82.7%**
Startup Mechanism	Mechanical Switch	Resonant Oscillator	Charge Pump	Meissner Oscillator	10-stage Voltage Multiplier	3-stage Charge Pump	Charge Pump	One-shot	Charge Pump	**PEG Starter**
Min. Startup Voltage	35 mV	30 mV	50 mV	40 mV	40 mV	210 mV	129 mV	50 mV	140 mV	**10 mV**
Efficiency @ Min. V_{TEG}	N/A	37%	45%	43%	12%	50%	23%	58%	29%	**63.9%**

6 Conclusion

6.1 Summary

This paper presents a thermoelectric energy harvesting system assisted by a PEG startup circuit. The system is mainly composed of three parts: the boost converter, the PEG-based startup block and the control block. The design focuses on minimizing the lowest startup voltage. During the operation, the PEG starter generates a startup signal which utilises the mechanical vibration, whereas the boost converter is driven by the startup clock to harvest the thermoelectric energy provided by the TEG. Since all the thermoelectric energy can be collated without sharing any portion for startup, the system can achieve an ultra-low startup TEG voltage. After the startup stage, the system can rely on its internal control module to work. In the output stage, a stable 1.2 V output is provided by the system to power the following stages. All of these state transformations are carried out by a state detector. To improve the maximum extractable power from TEG and reduce the power losses of boost converter, the adaptive working frequency and maximum power point tracking technique are employed to keep the system working at the optimal state. The VCO and MPPT circuit dynamically control the switching frequency and duty cycle by sensing V_{TEG}. Since the boost converter works in the conditions that only have ultra-low input power, it is more suitable to work in the DCM, therefore the system requires a subtle synchronization strategy. It is realized by using the ZCS block which tracks the optimal ON time for PMOS to reduce the mismatch of the gate switching and maximize the energy conversion. Moreover, a LDO block is used to reduce the impact of the fluctuation of the power supply.

This design has been implemented in a 0.18 μm CMOS process and occupies an area of 0.4 mm^2. Thanks to the PEG startup block, a minimum startup voltage of 10 mV is achieved which is currently the lowest startup TEG voltage in this field. This work also achieves an energy harvesting efficiency of 63.9% at the minimum TEG voltage. The peak overall efficiency of the system is 82.7%, achieved with 55 mV TEG voltage.

6.2 Future Work

After reviewing this design and the newly issued literature, some drawsbacks of this design are found and can be better improved in the following study and work. Two ways for the improvement in the future has been summarized as follows.

6.2.1 Improvement for PEG starter

Although this PEG starter helps the thermoelectric energy harvesting reach a 10 mV startup voltage, the startup block is disabled after the startup stage, which is a waste. Since the mechanical vibration is continuous when the machine is working and emitting heat, the PEG startup circuit can be modified into a piezoelectric energy harvesting system. On one hand, it is able to work as a startup block for the thermoelectric harvesting

system. On the other hand, more energy can be collected by this system, and therefore the output power can be improved dramatically.

6.2.2 Improvement for ZCS

In our design, the ZCS block used a 5-bit updown counter. It can be found that the more bits the counter has, the better resolution of ON time is realized, but the longer tuning time is required to reach the optimal value, that is, there is an inherent contradiction between the resolution and the tuning time. The SAR logic can be used to reduce the tuning time and keep the same resolution. For example, when the conventional ZCS fails to find the proper ON time in a certain cycle, the SAR logic is enabled.

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List of Publications

A Journal Paper

R. Wang, Y. Zou, Y Liang, and S. Du, "A 10-mV-Startup-Voltage Thermoelectric Energy Harvesting System Based on a Piezoelectric Cold Starter," IEEE Transactions on Circuits and Systems I: Regular Papers, 2022. (Under review)

Y Liang, R. Wang, Z. Chen, and S. Du, "A PV-assisted Startup Boost Converter for Thermometric Energy Harvesting," IEEE Transactions on Circuits and Systems II: Express Briefs, 2022. (Under review)

B Conference Paper

R. Wang, Y Liang, and S. Du, "A 10-mV-Startup-Voltage Thermoelectric Energy Harvesting System With a Piezoelectric Starter," IEEE International Symposium on Circuits and Systems, 2022.

Y Liang, R. Wang, Z. Chen, and S. Du, "A PV-assisted Startup Boost Converter for Thermometric Energy Harvesting," IEEE International Symposium on Circuits and Systems, 2022.