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Interconnect Reliability for Single-Step Sintered Die stack

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Abstract—**This study evaluates the reliability of die interconnect layers in a stacked die system fabricated using two different sintering agents: a microparticle-based silver paste and preform-based copper nanowires, intended for high-power packaging applications. Single-step sintering is performed to attach both dies at the same time, offering a faster and efficient assembly for improving scalability in manufacturing. The copper nanowires are sintered using KlettSintering method at 230°C for 5 minutes under a pressure of 20 MPa, while the silver paste was sintered pressure-free at 280°C for 45 minutes in nitrogen. The assembled units were characterized using shear strength and microstructural analysis. Both sintering methods showed high porosity in the top die-attach layer compared to the bottom die-attach layer, which is reflected in lower shear values for top die (35 MPa) compared to bottom die (45 MPa) in the silver sintered unit. The long-term reliability of the die-stack systems was assessed through a 500-hour high-temperature storage test and a 500-cycle temperature cycling test, revealing significant impacts of thermo-mechanical stresses on die attach layers of both sintered units. The KlettSintered system maintained consistent performance throughout the reliability tests but exhibited coarsening and oxidation during temperature cycling. Furthermore, the study identifies areas for potential improvement, particularly in improving multi-die sintering performance in a single-step process, which is crucial for ensuring durability in high-power applications.**

Keywords— Die-stacking, silver sintering, reliability, Cu nanowires, KlettSintering

I. INTRODUCTION

The evolution of semiconductor packaging is primarily driven by the growing demand for efficient, reliable, and compact electronic products, particularly in the automotive sector, where miniaturization, enhanced performance, and cost reduction are essential. Recently, Wide Bandgap (WBG) devices such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have attracted considerable attention for their ability to operate at higher voltages, frequencies, and temperatures compared to silicon devices [1], [2]. These properties make them highly suitable for high-power applications in sectors like electric vehicles (EVs), renewable energy, and industrial power systems. However, these applications also place increased demands on thermal management and device reliability, necessitating advancements in packaging technologies.

As a result, traditional interconnect methods, such as soldering, are being replaced by more advanced technologies that offer improved performance and reliability. Among these, micro-nano particle-based silver sintering is widely utilized for power electronics packaging due to its superior electrical and thermal conductivity [3], [4]. Recent developments in copper nanowire-based KlettSintering have shown promise in enhancing device reliability, particularly by enabling sintering at lower temperatures and pressures [5], [6].

Die stacking has emerged as a transformative technology in integrated circuits (IC), enhancing existing architectures and enabling high-performance, power-dense IC chips [7]. Its potential extends beyond traditional IC applications and can help significantly boost performance and efficiency, especially in high-power semiconductor packaging, where WBG materials like GaN and SiC are used to achieve superior thermal conductivity and power handling capabilities [8]. The die-attach (DA) layer plays a pivotal role in device performance and reliability as it directly contacts the die surface, particularly under high thermal and mechanical stress. Stacked die system can introduce complex thermal and mechanical stress distributions at DA interfaces [9], which require thorough investigation.

This study evaluates and compares two interconnect technologies, silver paste-based pressure-free sintering and copper nanowire-based pressure-assisted KlettSintering for die-stacking applications. Additionally, we investigate the potential of single-step die stack sintering, which reduces process steps, lowers costs, and increases throughput. However, this approach presents challenges in achieving

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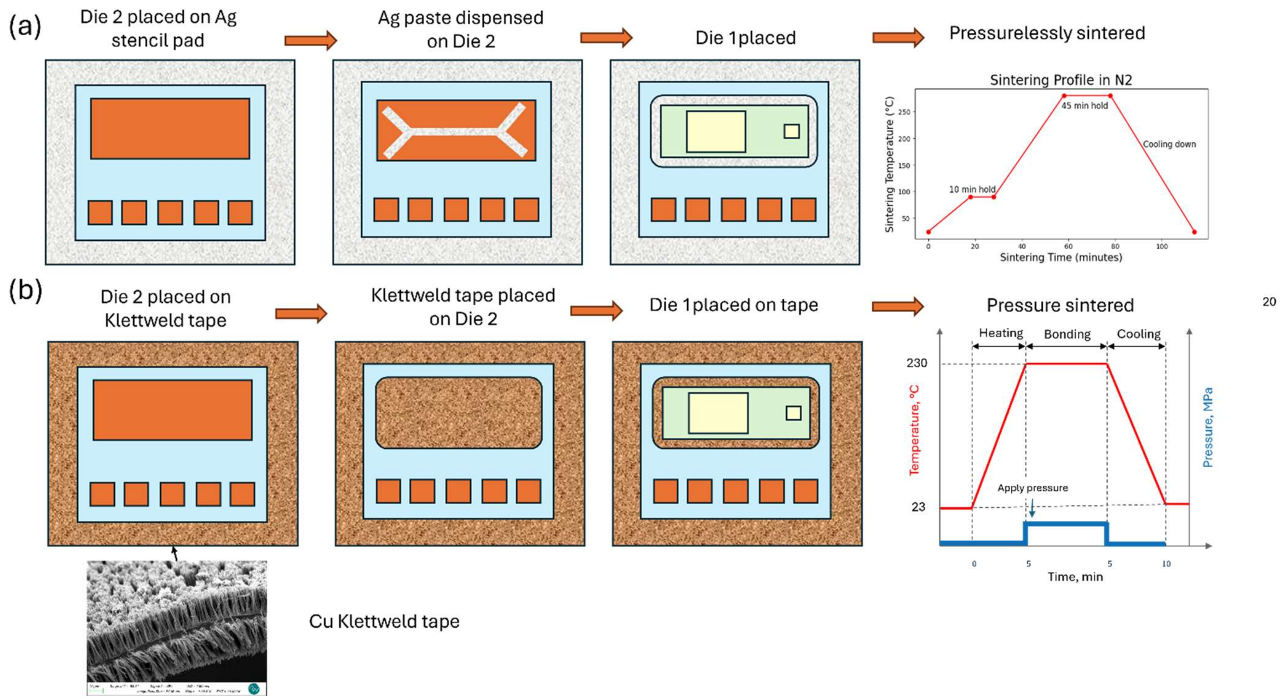

Figure 1:(a) Assembly overview for single-step Ag paste sintered die stack system; (b) Assembly overview for single-step Klettsintered die stack system.

uniform pressure and temperature distribution required for effective sintering, particularly in pressure-assisted sintering techniques. This research evaluates the advantages, challenges, and impacts of silver paste and copper nanowire sintering, contributing to the development of more efficient and cost-effective semiconductor packaging solutions.

II. SAMPLE PREPARATION METHODOLOGY

To validate the feasibility of sintering technology using Ag paste and Cu Nanowires (NW), die stack package units are fabricated and evaluated using various reliability tests, as shown in Fig.1. The packaged unit features a stacked die architecture in which Die 1 is attached to Die 2 to form the first die attach layer (DA1), while Die 2 is affixed to the copper substrate to create the second die attach layer (DA2). Heraeus's metal-ceramic substrate, based on the active metal brazing (AMB) process, is used as a Cu substrate, consisting of a 0.3 mm thick copper layer on both sides and a 0.32 mm thick Si_3N_4 ceramic core. The bottom die used for the package has dimensions of 4.5 × 4 × 0.38 mm, with Ag as the backside metallization surface and Pd as the topside metallization surface for interconnection whereas the top die exhibits a large, thin rectangular geometry of 3.8 × 1.6 × 0.15 mm and utilizes Ag for interconnection metallization.

A. Silver Paste Sintered Assembly

In this study, a commercially available microparticle-based silver paste with 92% silver content was employed for die-stack sintering. The silver attach layers for the bottom and top dies are referred to as Die Attach 2 (DA2) and Die Attach 1 (DA1), respectively. To enhance interface adhesion between the silver die attach layers and the AMB copper surface, the Cu AMB substrates were treated with formic acid to remove copper oxide. Two distinct paste application techniques were utilized for DA1 and DA2 interconnections: stencil printing for DA2 and dispensing for DA1(refer Fig. 1a). The stencil pad for DA2 was fabricated using an 80 µm Kapton tape stencil, incorporating a placement tolerance of 250 µm along each die edge. Die placement was executed using a Tresky tool with an overtravel of 300 µm. This additional overtravel ensured firm contact between the die and the AMB Cu surface. This parameter can be further optimized for improving the die edge fillet formation, bondline thickness (BLT), and overall sintering performance.

For DA1, Ag paste was applied onto the metallization pad of the bottom die using a dispensing needle. A dogbone-shaped pattern was designed to meet the geometric requirements of the top die. The dispensing parameters were optimized to achieve uniform paste distribution along the die edges and corners, maintaining a spread of approximately 75–80 µm. A similar placement overtravel was applied for Die 1 placement on the dispensed paste. The resulting fillet height in the stacked unit remained within acceptable limits for both DA1 and DA2.

The wet Ag paste in the stacked die configuration underwent pressure-free sintering at 280°C for 45 minutes using a hotplate in a Budatec oven under an N_2 environment. Due to the stacked package architecture, a temperature differential was observed between the DA1 and DA2 interfaces. A 30°C temperature offset was therefore applied to compensate for this variation, facilitating the simultaneous sintering of both die-attach layers in a single process step.

B. Cu Nanowire Sintered Assembly

For copper nanowire-based die attach sintering, KlettWelding-Tape sintering preforms were utilized. These preforms consist of a 20 µm copper foil with copper nanowires covering both sides. The nanowire coverage is approximately 30%, with an average length of ~20 µm and a diameter of 100 nm. Initially, a two-step sintering approach was employed, in which the bottom die was sintered in the first step, followed by the sintering of the top die in the second step. The sintering process was conducted at 230°C for 3 minutes under a pressure of 20 MPa. The assembly was initially placed into a cold sintering press, where pressure was applied before heating. The press was then heated to the target temperature and maintained for 3 minutes. The sintering atmosphere for all processes was air.

Preliminary evaluation of the samples was conducted through shear testing, followed by microstructural analysis. The results indicated that the DA layers were sufficiently compressed, leading to effective sintering (Fig. 4). To streamline the process, a single-step sintering approach was investigated to enable simultaneous sintering of both stacked dies. This was performed using a Pink SIN20 sintering machine equipped with a silicone soft tool. In this method, the two chips were placed with KlettWelding tape between the top and bottom dies, as well as between the bottom die and the substrate (Fig. 1b). To prevent movement during transport, a reduction agent combined with a tacking agent was employed. Unlike the two-step process, the single-step assembly was inserted into a preheated sintering machine due to the machine's limited heating capabilities. The sintering parameters remained unchanged.

III. RELIABILITY TESTING AND DISCUSSION

The reliability of the sintered die stack was assessed using various testing methodologies, as shown in Fig. 2. Scanning Electron Microscopy (SEM) analysis of the cross-section of the silver-sintered unit revealed denser porosity and a greater bondline thickness (BLT) for DA2 (~28 µm) compared to DA1 (~14 µm). This difference is reflected in the shear test results, where DA2 exhibited a higher die shear strength of 45 MPa, compared to 35 MPa for DA1 (Fig. 3). The fractured surface analysis indicated a mixed-mode failure in the shear test for both die attach layers. For the KlettSintered unit, comparable die strength was observed for both sintered dies. The shear test of DA2 resulted in chip break leading to lower nominal shear strength values. In case of DA1, presence of high organic residues in the interface can be attributed to lower shear values.

A. Cu NW sintered unit reliability testing

Figure 4 presents the SEM cross-section comparing the sintering quality of the two-step and single-step sintered die systems in their initial configurations, both employing KlettSintering technology to establish stable connections between die interfaces. The SEM cross-section of the two-step sintered device reveals excellent sintering behavior of the nanowires, forming a bulk-like material system with only minimal porosity. In contrast, the sintering quality of the single-step sintered unit was inferior, with several regions showing poor compression. Additionally, certain areas remained unsintered in the single-step unit, likely due to insufficient outgassing of residual organics. However, other regions displayed proper compression. Notably, the DA2 layer between the bottom chip and substrate exhibited better compression than the DA1 layer between the top and bottom dies. This variation may contribute to increased electrical and thermal resistance in the DA layers.

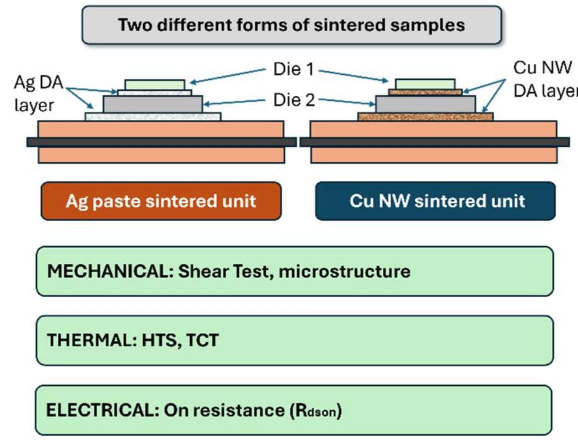

Fig. 2: Die stacking using different sintering methods and their testing methods.

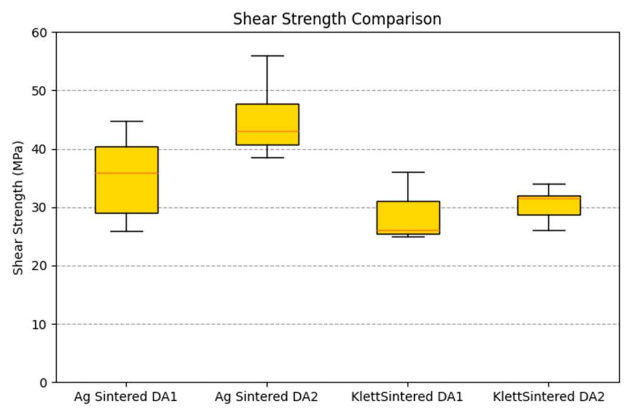

Fig. 3: Shear strength comparison for the Ag and KlettSintered die attach layers.

Further analysis involved subjecting selected samples to 500 thermal cycling tests (TCT) between -40°C and 150°C. After 500 TCT cycles, no cracking was observed at the bonding zones between the top and bottom dies, nor between the bottom die and the substrate (see Fig. 5). The mechanical condition of the dies remained stable throughout the testing, indicating the structural integrity of the sintered joints was preserved under stress. However, coarsening of the sintered layers, particularly between the bottom die and the substrate, was observed. In regions with insufficient sintering, oxidation and corrosion of the copper nanowires became apparent (see Figs. 6 and 7). Notably, this oxidation was localized to the edge regions of the nanowires, with areas exhibiting good sintering showing no oxidation. These findings underscore the critical role of sintering quality in mitigating oxidation risks.

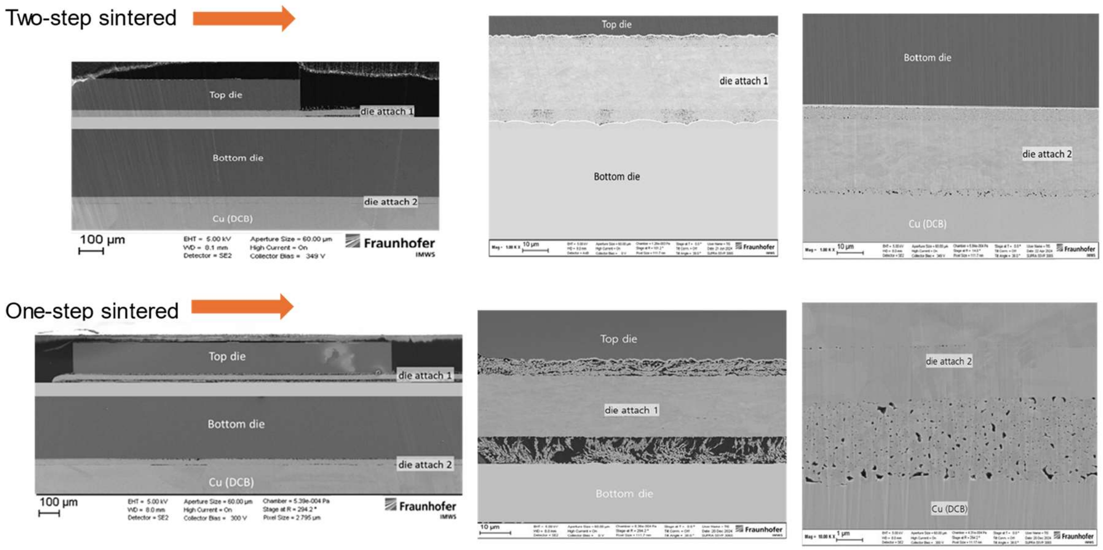

Fig. 4: Shows overview and details of the interface of two-step and single-step fabricated die systems with KlettWelding Technology.

Optimizing sintering conditions could enhance the overall integrity and performance of the die system

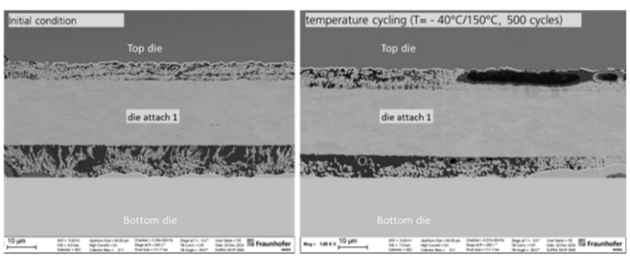

Fig. 5: Comparison of welded areas between top and bottom die in initial condition and after 500 cycles TCT.

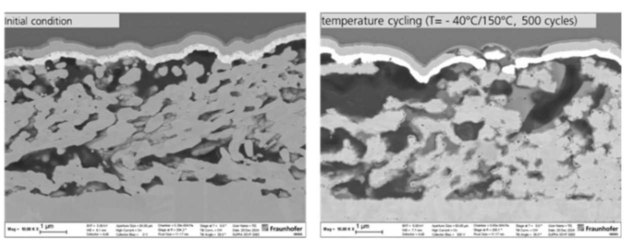

Fig. 6: Comparison of welded areas between bottom die in the initial condition and after 500 cycles TCT.

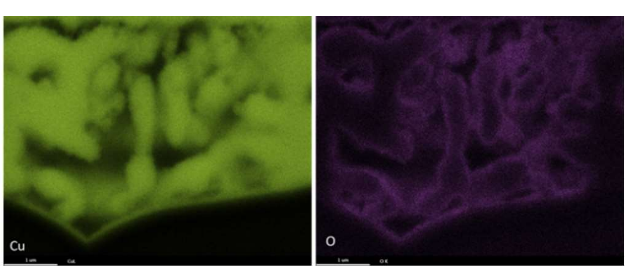

Fig. 7: EDS map of Nanowires after temperature cycling shows slight oxidation.

B. Silver paste sintered unit Reliability testing

Figure 8 demonstrates that the single-step sintered Ag die-attach system exhibits good integrity, particularly at the interface between the bottom die and the substrate, which is well-defined, homogeneous, and has minimal porosity. This strong interface enhances the overall stability and performance of the die system, ensuring effective mechanical and electrical connectivity. The low porosity suggests a successful sintering process that promotes optimal adhesion and reduces potential failure areas. In contrast, the interface between the top and bottom dies shows larger pores, likely due to the metallization structure of the second die. These larger pores raise concerns about the robustness of the inter-die connection, as they may act as stress concentrators, potentially compromising reliability under operational conditions.

After 500 thermal cycling tests (TCT), significant changes were observed at the interface between the top and bottom dies. Notably, the sintering structure increased, and the pores grew. This pore growth is concerning, as it may lead to micro-crack formation, compromising the structural integrity of the die system. These cracks reflect the mechanical stresses experienced during thermal cycling, indicating the need for further investigation into the factors contributing to this degradation. In contrast, the interface between the bottom die and the substrate displayed stress resilience in some areas but showed significant crack formation in the die-attach layer, particularly below the stacked die. No cracks were observed at the bottom die interface away from the stacked top die (Fig. 9). This phenomenon is likely due to thermal expansion mismatch between the materials used in the dies and the substrate, resulting in additional stress concentrations that accelerate crack formation. The interactions between stacked layers during TCT create complex thermo-mechanical stress distributions, which must be understood to mitigate potential failure modes. These findings highlight the critical role of the sintering process and material selection in determining the durability and reliability of die interfaces, particularly in stacked architectures.

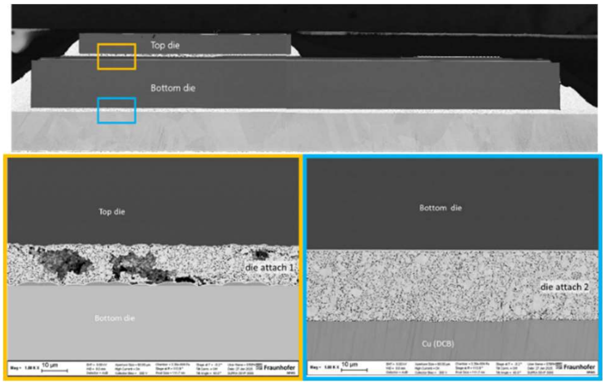

Fig. 8: Overview of one-step sintered silver attach system; Close-up images indicate details of interface for die-attach 1(yellow) and die-attach 2 (blue) in one-step-sintered die system.

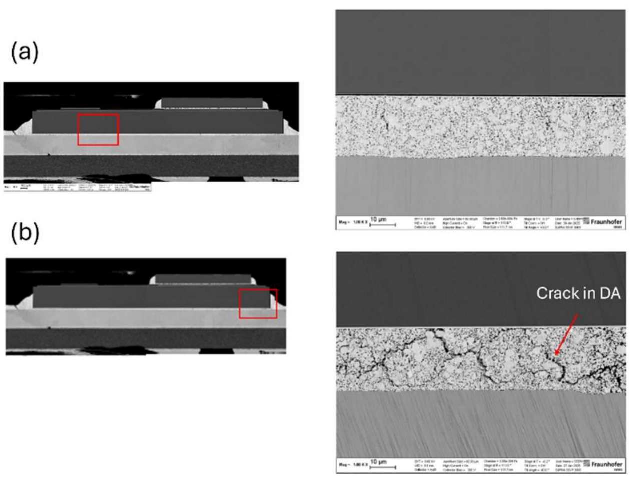

Fig. 9: Detail of thermos-mechanical impact of Die 1 on die attach 2 in single-step sintered system after temperature cycling.

Exposure to high temperatures for 500 hours at 150°C showed no significant effects on the microstructure of the sintered joints. Post-exposure microstructural analysis revealed that the sintered connection remained comparable to its initial state, indicating that the sintering process successfully established a robust interface capable of withstanding prolonged thermal stress without degradation.

In contrast, exposure to 250°C for 500 hours led to significant changes in the Ag microstructure at both die attach interfaces. The grain size of the silver joints increased and became closer to bulk material, as opposed to the random Ag particle distribution observed in the initial condition [10] (Fig. 10a). These variations in grain growth due to high-temperature exposure may compromise both the electrical and thermal properties of the die attach material, as well as affect its mechanical properties, such as stiffness, fatigue resistance, and strength [11], [12]. A similar evolution was observed in the pore distribution, where smaller pores migrated to form larger pores within the attach layer.

No die attach failure was observed at the interface between the top and bottom dies; however, delamination occurred between the bottom die and the substrate interface, suggesting differing degradation profiles for the two interfaces. One potential cause of failure could be the evolution of pores, which likely increased local stress concentrations [13], further exacerbated by the mechanical loading from the stacked die architecture. Additionally, a significant material reaction occurred between the Cu of the AMB substrate and the silver sintering material, forming a new phase or oxidation within the sintered layer. EDS mapping showed a layer of CuO delaminated from the original Cu interface and a diffusion zone consisting of Cu, Ag and O (Fig. 10 e,f). This interaction critically affects the integrity of the interface. This new phase introduces weak points that facilitate delamination from the substrate, further compromising both the mechanical and electrical connections. The formation of delamination under elevated temperatures underscores the limitations of the current material system under prolonged thermal stress, highlighting the need for a deeper understanding of the thermal behavior of materials used in chip packaging, particularly beyond operational temperature limits.

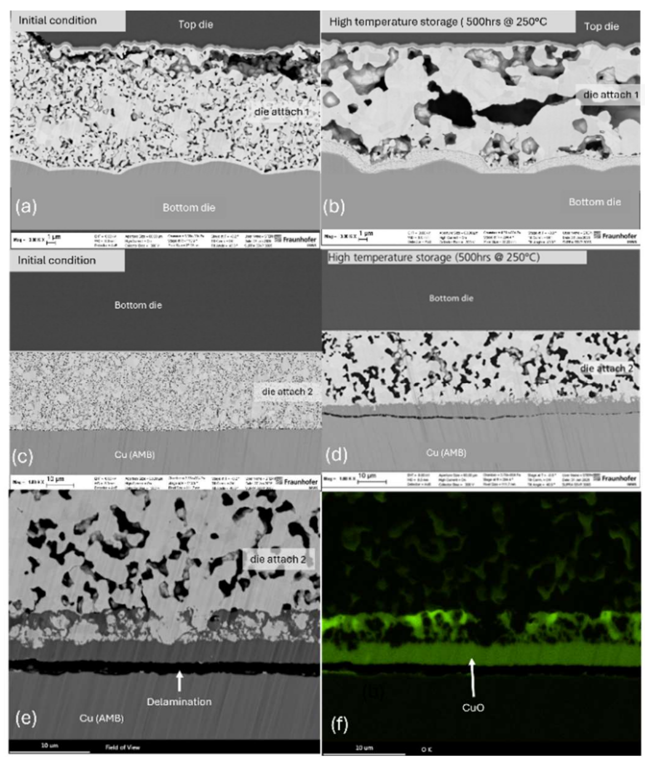

Fig. 10: (a, b) Die attach 1 interface before and after HTS @250°C; (c, d) Die attach 2 interface before and after HTS @250°C; (e) delamination in Cu AMB substrate ; (f) EDS mapping showing presence of CuO in the delaminated interface.

C. Electrical characterization

Fig. 11a shows the wire bonding diagram for evaluating the static electrical performance of the sintered die-stack assembly. Three nanowire die-attached samples were evaluated using the Semiconductor Device Analyzer B1505A (refer Fig. 11b). Only the two-step sintered assembly was assessed. Two of the samples met all required parameters except for an increased On resistance (Rdson). In contrast, the third sample exhibited failure due to excessive gate leakage current (Igss) and Rdson compared to the reference sample (refer Table 1), likely caused by damages from manual handling process.

Optical microscopy (OM) was utilized to analyze the surface conditions of the dies and sintered layers. A porous structure, approximately 50 µm in diameter, was observed on the Cu layer, which may be attributed to the reduced compression of the die-attach layer during bonding in the sintering press, potentially contributing to the elevated Rdson. Another contributing factor could be incompatible or insufficient wire bonds, leading to poor electrical interconnections.

TABLE I. MEASUREMENTS OF STATIC ELECTRICAL TESTS FROM NANOWIRE SINTERED SAMPLES

Parameters	**STATIC ELECTRICAL TEST**		
	Unit	*NW sample 1*	*NW sample 2*
Igs (VGS=22V, VDS=0V)	nA	0.35	0.25
Igs (VGS=-22V, VDS=0V)	nA	-0.57	-0.51
Vgsth (ID=1mA, VGS=VDS)	V	3.89	3.99
Vsds	V	1.85	1.89
Rdson (VGS=10V, ID=20A)	mOhm	55.77	57.88
Ids (VDS=650V, VGS=0V)	uA	1.97	2.01
Ids(VDS=650V, VGS=0V, 10ms)	uA	2.12	1.34

The single-step sintered nanowire die-attach assembly is anticipated to exhibit inferior electrical characteristics compared to the two-step sintered assembly. This is likely due to the presence of excessive organic residues, oxidized Cu nanowires, and larger voids within the die-attach layers, which result from process-related challenges discussed in previous sections. The initial electrical test with Ag sintered sample also showed elevated Rdson. In the analyzed sample, minor package and wire bond defects were observed, which attributed to inferior electrical results and will be corrected in future work.

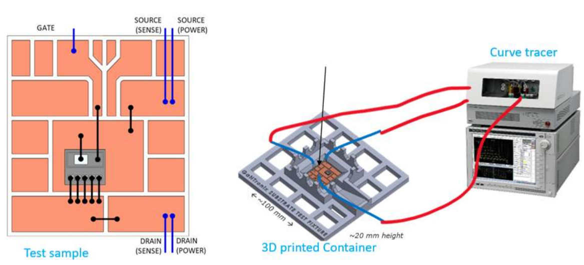

Fig. 11: a) Die assembly and wiring diagram overview; (b) Test setup for static electrical test measurements.

IV. SUMMARY AND OUTLOOK

This study investigated the reliability of silver paste and copper nanowire die-attach methods for single-step sintering in stacked die systems, assessing their performance under various stress conditions. Stress testing, including 150°C and 250°C/500-hour high-temperature storage (HTS) and -40°C to 150°C/500-cycle temperature cycling (TCT), revealed the vulnerability of the die-attach layers to thermo-mechanical stresses.

The silver-sintered package showed good sintering behaviour at initial condition but exhibited strong thermomechanical influences in the form of crack formation at the bottom die interface underneath the stacked top die, highlighting the impact of mechanical loading under thermal stress testing. Both top and bottom die attach were found to be robust against 150°C aging test but showed substantial grain growth and pore evolution at 250°C, altering the silver microstructure and resulting in delamination. These observations underscore the need for a deeper understanding of material thermal behavior under prolonged thermal stress for die-stack systems, especially beyond the operational temperature range.

While the KlettSintering method showed good performance during stress testing, it still requires improvements, particularly in the single-step bonding between the top and bottom dies wherein high pore density from leftover organic residues led to poor sintered interface. To minimize organic residues within the sintering layers, a formic acid atmosphere is tested, and sintering is performed without the use of additional organic substances. The study also highlighted the relationship between sintering performance and the oxidation of copper nanowires, indicating that optimizing sintering conditions could improve the integrity and performance of the die interconnect system.

The reliability testing of both sintering methods provides valuable insights into the effects of thermo-mechanical stresses on the die-attach interfaces in stacked die architecture. These sintering technologies demonstrate significant potential as die-attach solutions for demanding applications, such as high-power semiconductor devices. Future research will focus on optimizing the single-step sintering process for achieving uniform sintering in the overall system to enhance scalability and performance. A thorough understanding of the mechanical properties of sintering materials at elevated temperatures, coupled with stress distribution simulations across different die positions, is essential for improving the resilience of die systems in advanced semiconductor packaging.

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