Design of a Readout Scheme for a MEMS Microphone

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Abstract

This design mainly proposes a readout scheme for MEMS microphone with positive feedback to decrease the parasitic capacitance. It is designed in CMOS014 technology with a supply voltage of 3.3 V. The proposed architecture can increase the microphone's sensitivity with a comparatively low bias voltage. It enables the microphone to achieve high sensitivity even if it is loaded by an amplifier with large input capacitance. In the mean time, the SNR and THD are not affected much. The Spectre simulation shows that the system can achieve 61 dB SNR (A-weighted), 0.5% THD (1Pa sound pressure) and 1 mW power consumption. Several traditional readout schemes for MEMS microphone are also discussed and compared. The scheme which is based on amplitude modulation is tested and measured on PCB level.

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Chapter 1. Introduction

A microphone is an acoustic-to-electric transducer or sensor that converts an acoustical signal into an electrical signal. They are used in many applications such as telephones, hearing aids, mobile phones and personal audio systems. Many transduction principles have been used, leading to the development of transduction have been developed, including the piezoelectric, the piezoresistive, the capacitive and the contact microphones. The first microphone fabricated by silicon micromaching has been around for more than 20 years [1]. The introduction of silicon technology allows high precision and batch fabrication of the devices at low cost and with high reproducibility [2].

The most commonly used microphones are based on the capacitive principle for their low-power and tolerance to high temperature [3]. They also have advantages of large bandwidth and high sensitivity [4]. The capacitive microphone can be divided into two categories, namely the electret condenser microphone (ECM) and the condenser microphone. An ECM employs an electret, a component with a built-in charge-accumulating layer, which has the function of accumulating charges in the absence of an applied bias voltage. The first ECM which is based on silicon technology was presented by jHohm and Gerhard-Multhaupt in 1984 [5]. The charge on the electrets, however, was susceptible to temperature and suffered from long-term drift, which affected the sensitivity of the microphone [6]. The authors of[7] describe a promising teflon electret for use in a silicon microphone but the use of teflon in a standard industrial production process gives rise to a lot of difficulties [8].

The condenser microphone does not require an electret material. To accumulate charge, it requires an applied bias voltage. It has moderate sensing sensitivity and low sensitivity to temperature. They are usually fabricated as Micro-Electro-Mechanical System (MEMS) because of this results in small size, low cost and batch fabrication. Reading out such microphones is the main objective of this thesis and this topic will be explained in detail in the next section.

Therefore, for simplicity, the term “MEMS microphone” quoted frequently in the following text refers to a condenser microphone based on silicon.

1.1 What is a MEMS Microphone?

The MEMS condenser microphone is a design based on microminiaturized mechanical structures which can be integrated with CMOS process and other audio electronics. It can be viewed as a parallel plate capacitor that consists of a top membrane and a bottom back plate separated by a small air gap acting as a dielectric material. The back chamber acts as a reference chamber. Figure 1. 1 shows a cross-sectional view of a typical MEMS capacitive microphone. The acoustic holes on the back plate are used to alleviate air damping. An incident acoustic sound wave causes the membrane to deflect. As the membrane vibrates in accordance with the frequency and amplitude of the sound wave, the capacitance between the membrane and backplate changes accordingly due to the variable air gap. The aim of the readout circuit is thus to transform the capacitance variations into electric signals.

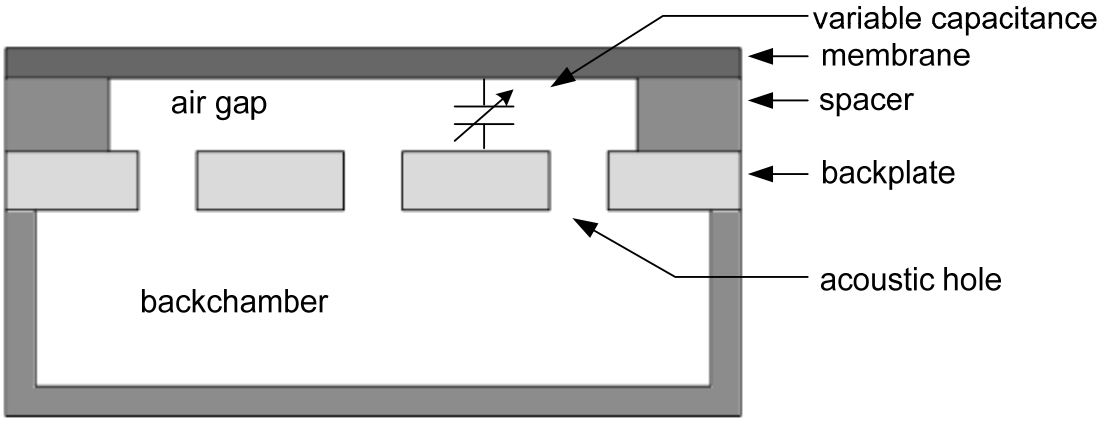

Figure 1. 1 The cross-sectional view of a typical MEMS capacitive microphone.

In the past 20 years, many researchers have investigated the fabrication of MEMS microphone with different structures or materials to improve their sensitivity and reduce their noise level. In 1992, T. Bourouina et al. proposed a condenser microphone with a p+ silicon membrane without acoustic holes that is shown schematically in Figure 1. 2 [9]. Because of the absence of acoustic holes, the air gap is increased to 7.5um to alleviate the air damping effect which results in a flat frequency response up to 10KHz.

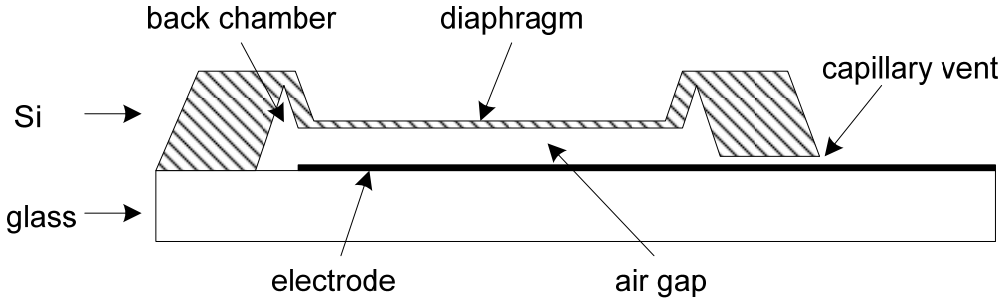

Figure 1. 2 Cross-sectional view of Bourouina et al.'s condenser microphone [9].

Since the stress of the membrane defines the microphone's sensitivity [1], the author in [10] proposes a microphone with a sandwich structure membrane which combines layers of compressive stress and tensile stress together to decrease the stress in the membrane. Another option to increase the sensitivity is to adjust the connection between back plate and membrane. The author in [11] reported that a spring type support rather than fully clamping the membrane at the whole circumference will increase the sensitivity by a factor of two. The picture of the spring-supported membrane is shown in Figure 1. 3.

Although there are still many ways to optimize the microphone's sensitivity by choosing different structures or materials, the design in this report will focus on the readout scheme which is at the circuit level. Therefore, the following sections describe a readout circuit for a MEMS microphone fabricated by NXP Semiconductors.

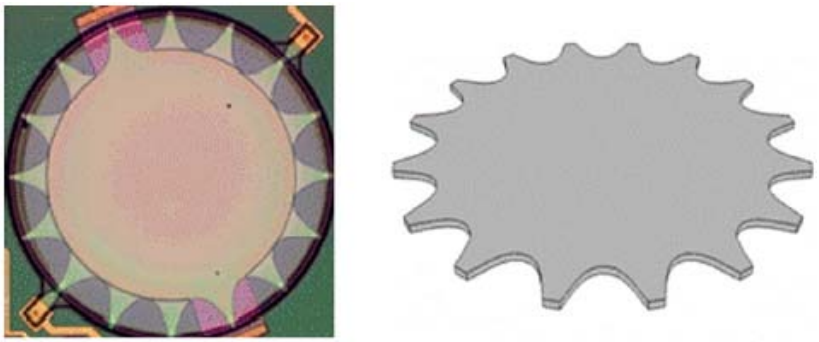

Figure 1. 3 Spring supported membrane [11].

1.2 Characteristics of the Microphone from NXP

The MEMS microphone in this design is manufactured by NXP Semiconductors. The membrane and perforated back plate are round in shape as shown in Figure 1. 4. The two electrodes are supported or connected by a silicon dioxide ring at the edge of the round plate. Figure 1. 5 illustrates the cross section of the microphone.

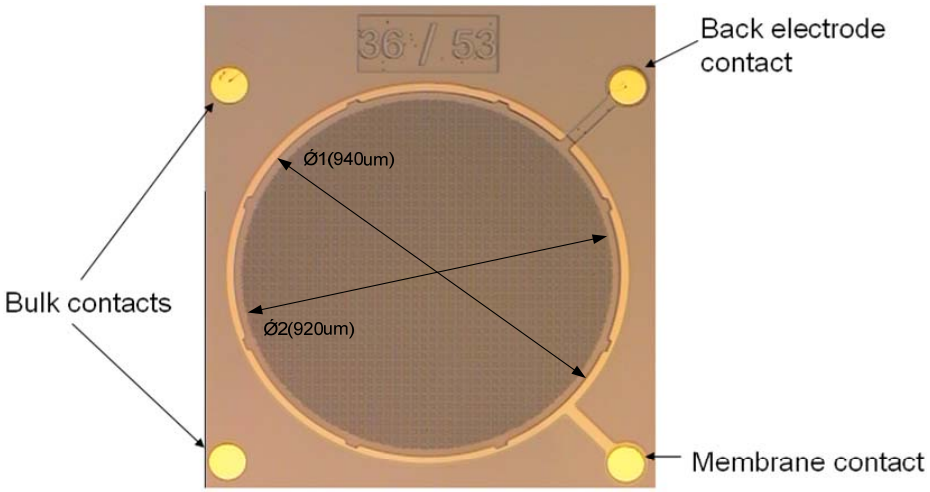

Figure 1. 4 Topview on the back electrode side.

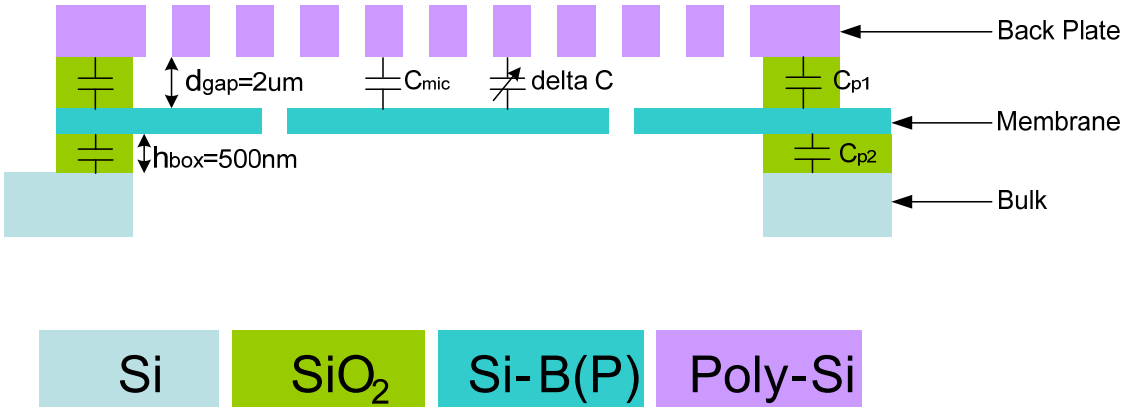

Figure 1. 5 Cross section of the microphone.

From the dimensions shown in Figure 1. 4 and Figure 1. 5, we can calculate the capacitance of the microphone when the membrane is not deflected. It is given by:

$$C_{mic} = \frac{\varepsilon_0 \varepsilon_{r1} \pi R^2}{d_{gap}} = \frac{1*8.85e^{-12}*3.14*(460e^{-6})2}{2e^{-6}} \approx 2.94\ pF \quad (1.\ 1)$$

where ε_0 is vacuum permittivity, ε_{r1} is relative static permittivity of air, R is the radius of the membrane and d_{gap} is the quiescent air gap thickness.

In normal operation, the membrane and bulk are shorted together and biased at ground to eliminate $C_{p2.}$ Thus C_{p1} shown in Figure 1. 5 is the main contribution for parasitic capacitance. The value of C_{p1} is given by:

$$C_{p1} = \frac{\varepsilon_0 \varepsilon_{r2} \pi \left((\frac{\phi 1}{2})^2 - (\frac{\phi 2}{2})^2 \right)}{d_{gap}} = 0.7\,pF \quad (1.\ 2)$$

where ε_{r2} is 4.5 which is the relative static permittivity of SiO2 , $\phi 1$ is the diameter of the membrane and $\phi 2$ is the effective diameter of the membrane.

A MEMS microphone needs a bias voltage across its two plates. During operation, there are mainly four different types of forces exerted on the capacitor structure: the mechanical input from the acoustical wave, the elastic (restoring) force generated in the vibrating membrane in response to the deflection, the electrostatic force caused by the bias voltage on the two electrodes, and the damping force generated by the air gap[12]. They are illustrated in Figure 1. 6 without the damping force since it can be neglected in equilibrium. And the electrostatic force shown in Figure 1. 6 is given by:

$$F_{es} = \frac{\varepsilon_0 A V^2}{2(d_{gap} - x)^2} \quad (1.\ 3)$$

where A is the area of the capacitor plate and x represents the displacement of the membrane. Equation (1. 3) indicates that the electrostatic force varies quadratically with the distance between the membrane and the back plate. This effect is the main reason for the microphone's nonlinearity.

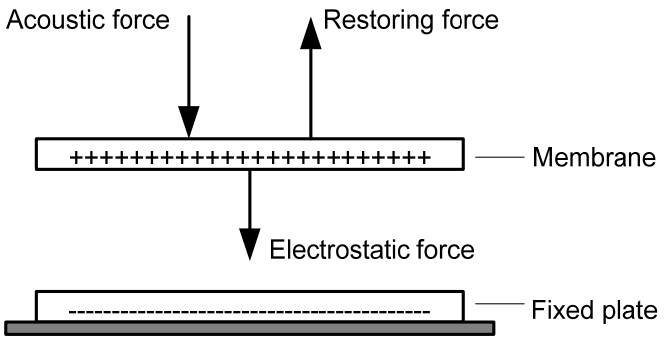

Figure 1. 6 Force diagram of a microphone in equilibrium.

Therefore the force acting on the membrane is the sum of the external mechanical pressure, the electrostatic force and the counterbalancing elastic force. When the electrostatic force exceeds the mechanical restoring force, we call the corresponding critical bias voltage the pull-in voltage. If the voltage is increased beyond this pull-in voltage, the membrane will collapse onto the fixed back plate. Figure 1. 7 illustrates the capacitance of the microphone with different voltages by finite-element simulation [13]. The pull-in voltage of the microphone is around 8V by experiment and 8.8V by simulation which can also be derived from Figure 1. 7.

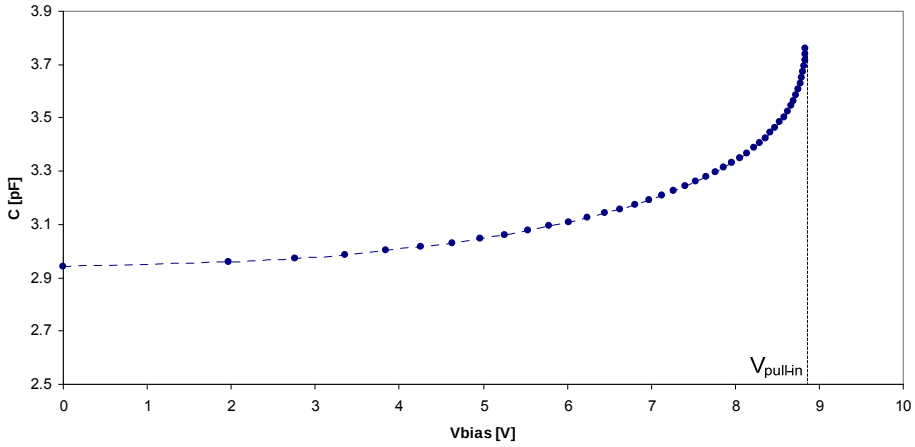

Figure 1. 7 Capacitance variance with different voltage

1.3 Sensitivity

When there is no bias voltage across the two electrodes, the deflection of the membrane with an acoustical pressure, which is shown in Figure 1. 8, can be expressed as [14]:

$$w(r,P)=\frac{P}{4\sigma h}(R^2-r^2) \qquad (1.4)$$

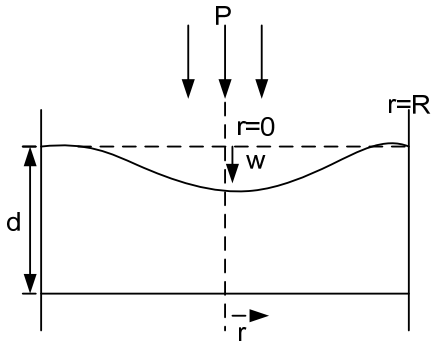

Figure 1. 8 Membrane's deflection without bias voltage.

Consequently, the capacitance between membrane and back plate is given:

$$C(P)=\int_0^R \frac{\varepsilon_0 \cdot 2\pi r}{d_{gap}-w(r,P)}dr \approx \frac{\varepsilon_0 A}{d_{gap}}\cdot(1+\frac{1}{2}\cdot\frac{R^2}{4\sigma h d_{gap}}P+\frac{1}{6}\left(\frac{R^2}{4\sigma h d_{gap}}\right)^2 P^2+...)\cdot[F] \qquad (1.\ 5)$$

With $\frac{R^2}{4\sigma h d_{gap}} = 2.38\cdot 10^{-3}\ \mathrm{m^2/N}$, the third term in the bracket on the right side of equation (1. 5) can be neglected. Thus the sensitivity to acoustical pressure is:

$$S_d = \frac{\partial C(P)}{\partial P} \approx \frac{\varepsilon_0 A}{d_{gap}}\cdot\frac{R^2}{8\sigma h d_{gap}} = \frac{\varepsilon_0 \pi R^4}{8\sigma h d_{gap}^2}\cdot[F\ /\ Pa\ ] \qquad (1.\ 6)$$

If we substitute the value of $\frac{R^2}{4\sigma h d_{gap}}$ into equation (1. 5), it gives the linear relation between the microphone's capacitance and the acoustical pressure which is given by:

$$C_{mic}(P)\approx\frac{\varepsilon_0 A}{d_{gap}}\cdot(1+0.00119\cdot P)=C_{mic}(1+kP)\cdot[F],\quad for\ \ k=0.00119\cdot[Pa^{-1}] \qquad (1.\ 7)$$

where C_{mic} is the quiescent capacitance of the microphone which is calculated in equation (1. 1). For convenience and clarity, 0.00119 is replaced with a symbol k.

From this chapter on, the frequently mentioned term C_Δ represents the capacitance variance in the time domain and it is equal to $C_{mic}kP$. If the acoustical pressure P can be represented as $\hat{P}\sin(\omega t)$, where $\hat{P}$ is the amplitude of the sound and ω is the frequency of the sound, then the amplitude of the capacitance variance in the frequency domain is $C_{mic}k\hat{P}$ and it is symbolized as C_v. Consequently, the rms value of the capacitance variance $C_{v,rms}$ is $\frac{C_v}{\sqrt{2}}$

Table 1. **1** shows the notation used in the above equations.

Symbol	Explanation
w	Deflection of the membrane [m]

R	Radius of the membrane [m]
r	Radial position [m]
σ	Initial stress of membrane [Pa], 30MPa
h	Thickness of membrane [m], 0.38e-6
P	Acoustical Pressure [Pa]
d_{const}	Quiescent air gap between membrane and back plate [m], 2e-6
ε_0	Permittivity of free space [F/m], 8.854e-12
A	Area of the membrane [m^2]

Table 1. 1 Notation used in the equation (1. 4) to (1. 7)

When there is a bias voltage, the author in [15] gives the sensitivity under this condition which is given by:

$$S_{el}^{mech} = K_{cell} \frac{V_{bias}}{d} \cdot [V/m] \ [15] \quad (1.8)$$

$$S_{el}^{ac} = K_{cell} \frac{V_{bias}}{d} S_d \cdot [V/Pa] [15] \quad (1.9)$$

Table 1. 2 shows the notations used in the above equations.

Since the movable membrane will be attracted to the fixed back plate when a bias voltage is exerted, the air gap distance becomes smaller and results in a larger sensitivity. Consequently a larger signal will be generated by the microphone with a larger bias voltage.

Symbol	Explanation
S_{el}^{mech}	Mechanical sensitivity in electrical domain
S_{el}^{ac}	Acoustical sensitivity in electrical domain
K_{cell}	Holes in the cell and the fringing fields at the edges
V_{bias}	Voltage exerted on the microphone
S_d	Acoustical sensitivity without bias voltage which is shown in equation(1. 6)
d	Air gap between membrane and back plate

Table 1. 2 Notation used in the equation (1. 8) and (1. 9)

1.4 VerilogA Model for Microphone from NXP

Given the basic characteristics of the microphone, a behavioral model of the microphone is essential for simulation. Ideally, this model should be accurate and include the non-idealities of the sensor which limit the performance. But a simple model can speed up the simulation process and reduce the design time. In this design, a proper functionality is the main objective for the model. Therefore a very simple model is coded in Verilog-A which does not consider the nonlinearity and electrostatic force limit of the microphone. The effect that sensitivity increases with increasing bias voltage is not included as well. If specification can be achieved with the lowest sensitivity, it will also be achieved with higher sensitivity.

The basic principle behind the model is regarding the microphone as a variable capacitance and its capacitance variance is controlled by a voltage source which represents the acoustical signal. The related code can be found in Appendix A.

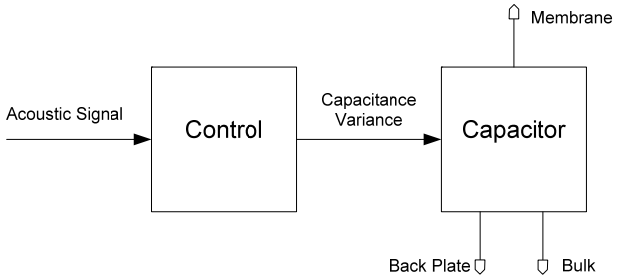

Figure 1. 9 VrilogA Model for Microphone

1.5 Specification to be Achieved

In the current MEMS microphone products market, the major manufacturers are Knowles Electronics, Analog Devices, Infineon, Akustica and Pulse MEMS. They produce both analog microphones and digital microphones. With the datasheets of these products, the main characteristics of those analog microphones are listed in Table 1. 3. There exists another design which is based on the microphone from NXP Semiconductors already. It adopts charge pump to move the bias voltage across microphone up to 5V. Its specifications are also listed in Table 1. 3.

Specification / Product	SNR@1Pa (dB)(A-weighted)	Sensitivity @1Pa (dBV/Pa)	Current (uA)	Band-width (HZ)	THD(%)
SPM0204HE5 (Knowles Acoustics)	59	-42	100 (V_{DD}=1.5~3.6V)	14K	1%@100dBSPL
ADMP401-1 (ADI)	**62**	**-37**	200 (V_{DD}=1.5~3.6V)	12K	3%@105dBSPL
AKU1126 (Akustica)	58	-42	150 (V_{DD}=1.65~3.6V)	N/A	5%@115dBSPL
SMM310 (Infineon)	59	-42	**80** (V_{DD}=2.1V)	10K	**0.1%@104dBSPL**
TC200A (Pulse MEMS)	61	-40	330 (V_{DD}=1.64~2.86V)	**20K**	10%@110dBSPL
Previous Design	60	-46	450	20K	1%@100dBSPL

Table 1. 3 The specification of the MEMS microphone products on the market.

The table shows a general idea about the behavior of the current MEMS microphone products on the market. It also indicates the most important specifications when designing the interface circuit for MEMS microphone. The data in bold type states that it exceeds the behavior of other products in this specification.

By comparing the data listed in Table 1. 3, we can have a rough idea about the specifications which are going to be satisfied. SNR at 1Pa should not be lower than 58 dB. Sensitivity at 1 Pa should not be lower than -42 dB. The current consumption is supposed to be kept as small as possible. The bandwidth which is mainly decided by the frequency response of the microphone should be the same as the previous design. And the total harmonic distortion (THD) is also expected not to exceed that of the previous design.

Since the previous design uses charge pump to increase the bias voltage across the sensor which increases the complexity of the circuit, the aim of this design is thus trying to achieve the same specification of the previous design with a lower bias voltage.

1.5.1 Sound Pressure Level

The "dBSPL" shown in the last column of Table 1. 3 is the unit of sound pressure level (SPL) which is often denoted as sound level Lp. It is a logarithm decibel scale measurement of the rms (Root Mean Square) sound pressure of a sound relative to a reference value[16]. From this section on, if not explicitly mentioned, sound pressure will be expressed in terms of its effective value (rms). The reference value is 20uPa which is the threshold of hearing (roughly the sound of a mosquito flying 3 meters away). The relation between sound pressure and sound pressure level is given by:

$$L_p = 10\log_{10}\left(\frac{p_{rms}^{\ 2}}{p_{ref}^{\ 2}}\right) = 20\log_{10}\left(\frac{p_{rms}}{p_{ref}}\right) \qquad (1.\ 10)$$

where p_{rms} is the rms value of the sound pressure being measured and p_{ref} is the reference sound pressure.
Table 1. 4 shows a comparison of sound pressure level and corresponding sound pressure which gives a general idea of the relation between the common sound source in human life and the abstract sound pressure level.

Examples	Sound Pressure Level (dBSPL)	Sound Pressure p (N/m^2=Pa)
Jet aircraft, 50 m away	140	200
Threshold of pain	130	63.2
Disco, 1 m from speaker	100	2
Diesel truck, 10 m away	90	0.63
Kerbside of busy road, 5 m	80	0.2
Vacuum cleaner, distance 1 m	70	0.063
Conversational speech, 1 m	60	0.02
Quiet library	40	0.002
Quiet bedroom at night	30	0.00063
Background in TV studio	20	0.0002

Rustling leaf	10	0.000063
Threshold of hearing	0	0.00002

Table 1. 4 Relation between sound pressure level and sound pressure [16].

1.5.2 A-weighted

When SNR specifications are stated in Table 1. 3, the term A-weighted is used. Since the human ear is most sensitive to sounds at frequencies between 1 KHz to 5 KHz, frequency-weighting curves are often incorporated with sound pressure level meters to produce a result which conforms to what we hear [17]. The weighting curves were originally different with different sound level, but A-weighting, which was originally used for low level sounds, is now often used for measuring environmental noise and the output of audio systems. The A-frequency-weighting curve is shown in Figure 1. 10. The gain curve crosses 0dB at 1 KHz. The function defining the A-weighting curve in terms of poles and zeros comes from IEC/CD 1672 (and ANSI S1.42-2001):

$$G_A(s) = \frac{k_A \cdot s^4}{(s+129.4)^2 (s+676.7)(s+4636)(s+76655)^2} \qquad (1.\ 11)$$

where $k_A \approx 7.39705 * 10^9$

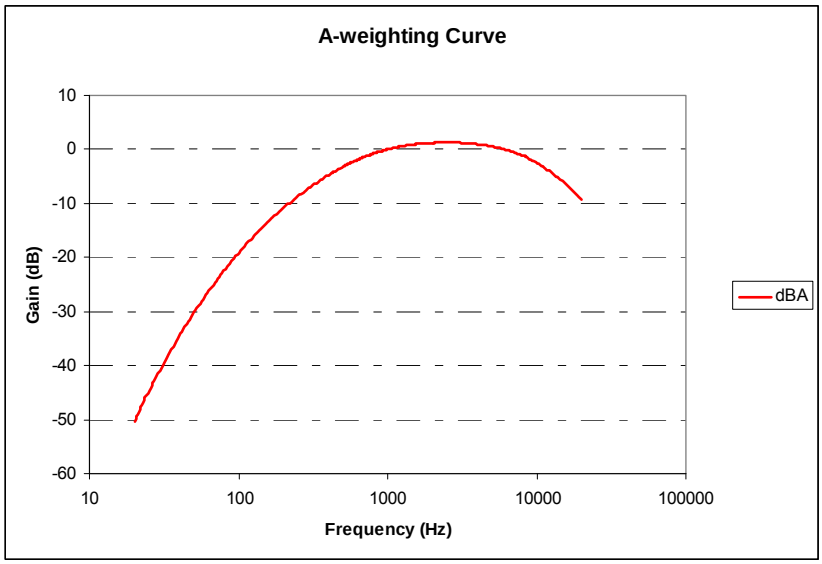

Figure 1. 10 A-weighting Curve

1.6 Motivation

As has been stated above, a large bias voltage exerted on the microphone can generate large signal until the voltage exceeds the pull-in voltage. The fact that mainstream CMOS technology cannot handle voltages greater than a few volts, however, indicates that realizing a high bias voltage will bring more difficulties. Moreover, the signal generated from the MEMS microphone needs to be readout by an interface circuit. For a specific microphone, different interface circuits will drive the microphone to have different specifications.

Therefore, the main purpose of this project is to investigate the possible interface structures and finally develop an interfacing principle which can drive a microphone biased with a low bias voltage in such a way to achieve the specification.

1.7 Outline of the Thesis

The thesis is composed of seven chapters presenting different aspects of the investigation. Following this introduction chapter, Chapter 2 describes the investigations of several possible readout schemes for a capacitive MEMS microphone sensor. These comparisons mainly focus on the signal-to-noise ratio (SNR), linearity and sensitivity. Chapter 3 proposes a new readout scheme which can increase the sensitivity of the microphone by the use of positive feedback capacitor. It mainly deals with the principle behind this scheme. The specification of the preamplifier will also be given. Chapter 4 describes the process of designing a low-noise operation amplifier (opamp) on transistor level. The design of the current source used in the biasing circuit is included as well. In Chapter 5, the opamp will be simulated with the microphone model in the whole scheme. The practical implementation issues of the system are discussed. The simulation results and the analysis of them are both presented in Chapter 6. Finally, in Chapter 7, the conclusion of the project and recommendations for future improvement are given.

Chapter 2. Readout Scheme

This section mainly analyzes the possible readout schemes for MEMS microphone. It starts with the background of some common readout schemes in literature (section 2.1). Then three different schemes will be analyzed (section 2.2~2.4). Both the advantage and disadvantage of these schemes will be explained in detail. The chapter ends with a comparison among the three schemes (section 2.5).

2.1 Read-out schemes for Capacitive Microphone

A typical MEMS microphone front-end interface has to transfer the capacitive changes in the sensor to voltage or current variations. It has relatively fixed specification driven by the characteristic of the microphone. The interface circuit also has to minimize the most critical non-idealities of the sensor (e.g. parasitic capacitance) to maximize its sensitivity [18].

In traditional design, a Junction-Field-Effect-Transistor (JFET) in the source-follower configuration is used to buffer the signal from the electret microphone which is shown in Figure 2. 1 [19]. The voltage source V_{mic} represents the input sound which is also proportional to the sound pressure. The value of R_{bias} needs to be very large to move the k_BT/C noise corner generated by the microphone and R_{bias} to low frequency where it is of no importance.

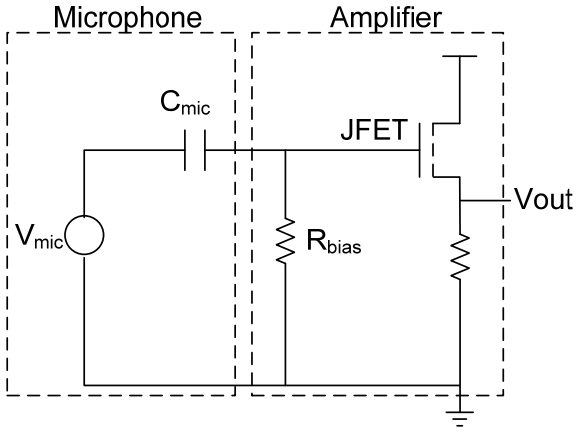

Figure 2. 1 Traditional readout scheme for ECM.

The microphone in Figure 2. 1 is an electret microphone which has long-term drift problems as mentioned in Chapter 1. For a MEMS capacitive microphone, i.e. without an electret, a typical voltage-readout scheme is shown in Figure 2. 2 [20]. The microphone is biased with a dc voltage through a large resistor. The resulting large RC time constant can guarantee that the microphone works under constant charge condition. However, the bias resistor needs to be very large (depending on the microphone's capacitance and bandwidth) which is not easy to implement in a standard CMOS technology. The sensitivity is limited by the parasitic capacitances both of the sensor itself and of the preamplifier

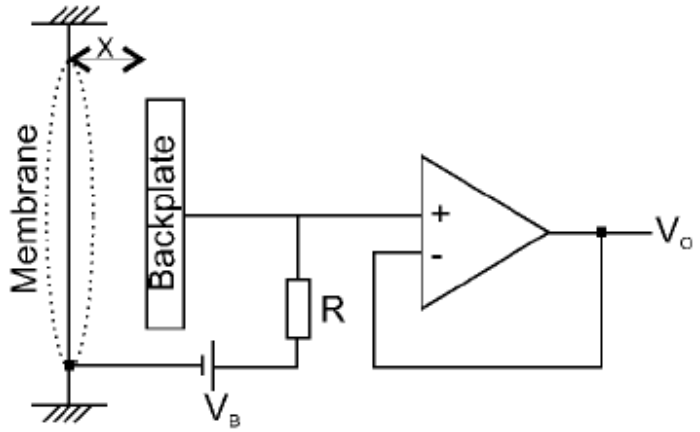

Figure 2. 2 Typical voltage-readout scheme for MEMS capacitive microphone [20].

The MEMS microphone can achieve high sensitivity with high bias voltage. Thus the author in [6] proposed a scheme which is shown in Figure 2. 3. A MEMS microphone without an electret is biased by a dc-dc converter. The Dickson type dc-dc converter behaves like a charge pump and it builds up charge at the output by the two anti-phase oscillation clocks [21].What makes this design novel is that the dc-dc converter enables the microphone to achieve high sensitivity at a low supply voltage. The main disadvantage of this design is the linearity. It has 10.1% distortion under 20 Pa sound pressures.

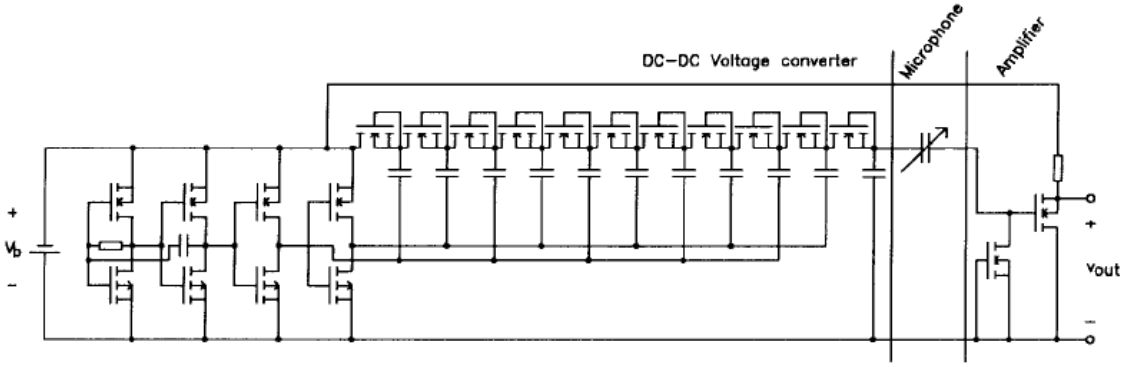

Figure 2. 3 Scheme of the integrated capacitive microphone with dc-dc voltage converter and preamplifier [6].

Recently the authors in [22] propose a solution which implements two microphones biased by voltages having opposite polarities. The SNR is thus increased by 3 dB. The bias voltage for the microphone is ± 10V which is generated from a charge pump. A 6V PMOS differential pair forms the basic gain stage. Another novel point of this design is the feedback amplifier (FA). It not only speeds up the start up transient time but also increases the insensitivity to the supply-induced noise and electro-magnetic interference (EMI). The schematic of the preamplifier used in this design is shown in Figure 2. 4. One distinct disadvantage of the design is the cost since two microphones are used.

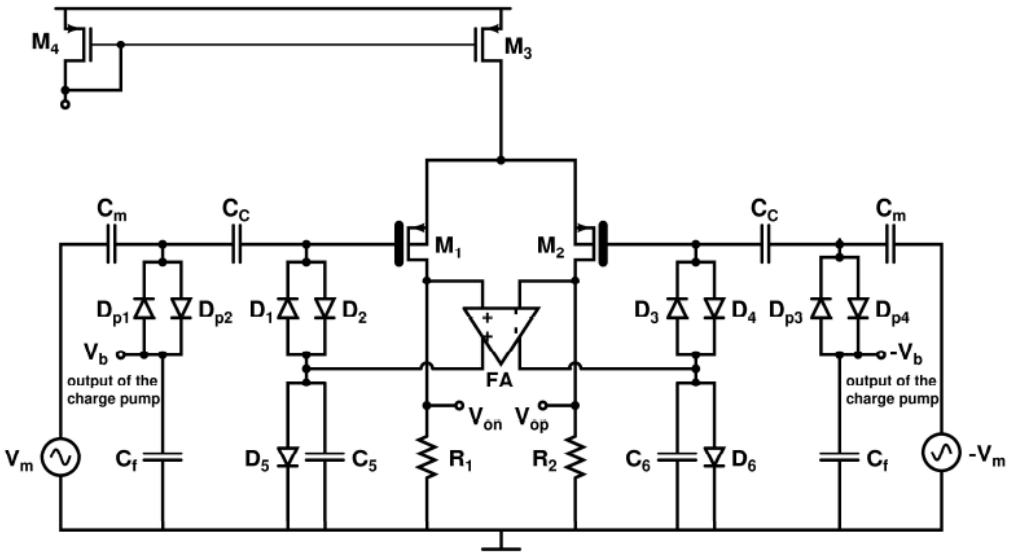

Figure 2. 4 Schematic of the preamplifier used in [22].

Another option for readout capacitive microphone adopted a different detecting principle, frequency modulation. The scheme is shown in Figure 2. 5. Cm represents the capacitive microphone and it plays the role of timing capacitance in the ring oscillator due to its variable capacitance. In this design, the microphone does not need extra dc bias. Therefore the microphone behaves more linearly to the acoustic pressure due to the small electrostatic force between the membrane and back plate. Moreover, the frequency modulated output is convenient for further digital signal processing. However, the major disadvantage of the design is its low SNR (about 60 dB SNR under 20 Pa) and high power consumption (1.96 mW) [23].

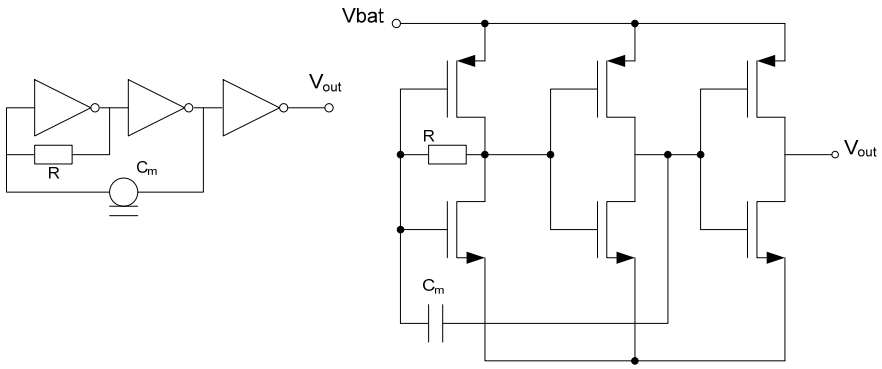

Figure 2. 5 Scheme of the integrated microphone by using frequency modulation [23].

From the above literature study, it can be seen that there are two designs use charge pump to bias the microphone. Since a charge pump is not easy to implement and the distortion increases sharply as bias voltage approaches the pull-in voltage [24], the aim of the design is thus to find out a suitable readout scheme which will get rid of the charge pump and maximize the sensitivity of the microphone under a low supply voltage. It starts with the most traditional and typical scheme and then moves on to a new scheme by reducing the drawbacks of the old design.

2.2 DC Biasing

In DC biasing, which is shown in Figure 2. 6, there is a very large resistor R_b (in the order of Giga-Ohms) connected between the microphone and a dc voltage source which is indicated as V_{ref}. The name "dc biasing" comes from the electrical characteristics of the reference source V_{ref}. The charge accumulated on the microphone does not change by much because of the large RC time constant. The charging current is given by:

$$I = \frac{V_{ref}}{R_b} e^{-\frac{t}{R_b C_{mic}}} \ [A] \tag{2. 1}$$

If R_b is infinite, $I = \frac{\partial Q}{\partial t} = \frac{V_{ref}}{R_b} \approx 0$ which means Q can be regarded as constant. The following equation is based on constant charge assumption which is given by:

$$V_o = \frac{Q_{mic}}{C_{mic}} = \frac{Q_{mic}}{A\varepsilon} d \ [V] \tag{2. 2}$$

where Q_{mic} the total charge accumulated on the sensor, C_{mic} is the static capacitance of the sensor, A is the area of the effective membrane, ε is the permittivity of the medium between the membrane and the back plate and d is the distance between the membrane and the backplate.

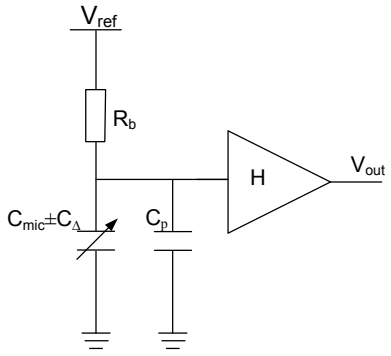

Figure 2. 6 DC biasing scheme.

2.2.1 Signal Level

Based on constant charge assumption, we can derive that:

$$Q_{const} = (C_{mic} + C_p) * V_{ref} = (C_{mic} + C_p \pm C_\Delta)(V_{ref} \mp \Delta V) \ [F \cdot V] \tag{2. 3}$$

where C_Δ is $C_{mic} kP$ which comes from equation (1. 7) and the value of C_{mic} is denoted in equation (1. 1). From this section on, C_p not only represents C_{p1} which is mentioned in section (1.3) but also includes the parasitic capacitance from the preamplifier.

(Since it is impossible to have a resistor with infinite large resistance, the calculation of the output signal without the constant charge assumption is included in Appendix B.)

As a result, the signal generated on the microphone in the time domain is:

$$\Delta V = \frac{(C_{mic} + C_p) * V_{ref}}{C_{mic} + C_p - C_\Delta} - V_{ref} = \frac{C_\Delta * V_{ref}}{C_{mic} + C_p - C_\Delta} \quad [V] \tag{2. 4}$$

2.2.2 Noise Calculation

There are mainly two noise sources in DC biasing scheme which are shown in Figure 2. 7. One is the thermal noise from the bias resistor which is represented by noise power spectrum density $\overline{v}^2_{noise,R_b}$. It is filtered by the microphone and the parasitic capacitance. The other one is the input-referred noise density of the preamplifier which is represented by $\overline{v}^2_{noise,in}$. Although the voltage source V_{ref} also contributes noise, its noise is filtered by the R_b and microphone as well. Even though, a clean bias voltage is also demanded in DC biasing scheme. For simplicity, the following calculation is based on the assumption that the bias voltage is noise free. Therefore the total input-referred noise at the input of the preamplifier is given by:

$$v^2_{noise} = \overline{v}^2_{noise,R_b} * \left| \frac{1}{1 + j * \omega R_b * (C_{mic} + C_p)} \right|^2 + \overline{v}^2_{noise,in} \quad [V^2 / Hz] \tag{2. 5}$$

Referring the noise voltage power spectrum to a capacitive noise power spectrum by using the voltage-to-capacitance transfer function (assuming C_Δ is much smaller than $C_{mic}+C_p$) yields:

$$C^2_{noise} = \left(\frac{C_{mic} + C_p}{V_{ref}} \right)^2 \overline{v}^2_{noise,R_b} \left| \frac{1}{1 + j * \omega R_b * (C_{mic} + C_p)} \right|^2 + \left(\frac{C_{mic} + C_p}{V_{ref}} \right)^2 \overline{v}^2_{noise,in} \quad [F^2 / Hz] \tag{2. 6}$$

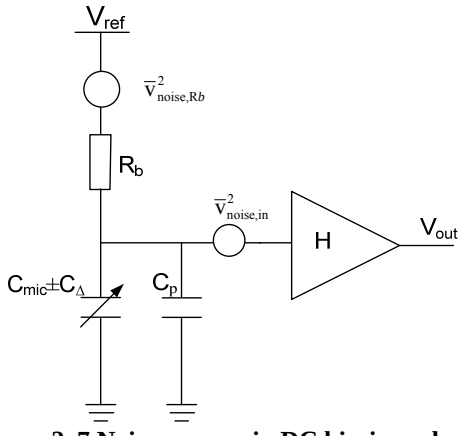

Figure 2. 7 Noise sources in DC biasing scheme.

Equation (2. 6) indicates that for a certain capacitance variance C_v, large value of V_{ref} and R_b will yield large SNR.

Although the DC biasing scheme is simple, its dominant disadvantage is that the large resistor is difficult to implement in IC technology. Moreover, in the audio bandwidth which

is from 20 Hz to 20 KHz the 1/*f* noise of the opamp dominates which is not beneficial to achieve a good SNR. Equation (2. 4) also shows that the electrical sensitivity of the microphone is inversely proportional to the quiescent capacitance (C_{mic}+C_p) of the microphone. If the preamplifier connected afterwards has large input parasitic capacitance (for low noise or coupling reason), the sensitivity of the microphone is deteriorated even more. As a result, the input-referred noise of the preamplifier has to be reduced to compensate for the sensitivity reduction. Another drawback of this scheme is the nonlinearity. Rewriting equation (2. 4) into:

$$\Delta V = \frac{C_\Delta * V_{ref}}{(C_{mic} + C_p)\left(1 - \frac{C_\Delta}{C_{mic} + C_p}\right)} \quad [V] \qquad (2.\ 7)$$

In the ideal case, the signal should be linearly proportional to the capacitance variance of the microphone. The factor $\frac{C_\Delta}{C_{mic} + C_p}$ in the denominator of equation (2. 7), however, affects the linearity. This factor is supposed to be small which implies that C_{mic}+C_p should be large. A large value of C_{mic}+C_p, however, will kill the signal level which is indicated from equation (2. 4). Therefore, there exists a trade off between the signal level and linearity when the DC biasing scheme is used.

2.3 Charge Amplifier

In order to avoid the impact of parasitic capacitance, another interfacing scheme was investigated. This is shown in Figure 2. 8. Because of feedback, the voltages on the two inputs of the amplifier will follow each other and so the bias voltage across the microphone will be stable. The voltage across the parasitic capacitor will also be stable. Consequently, C_p can be neglected in the calculation of AC transfer function which is shown below

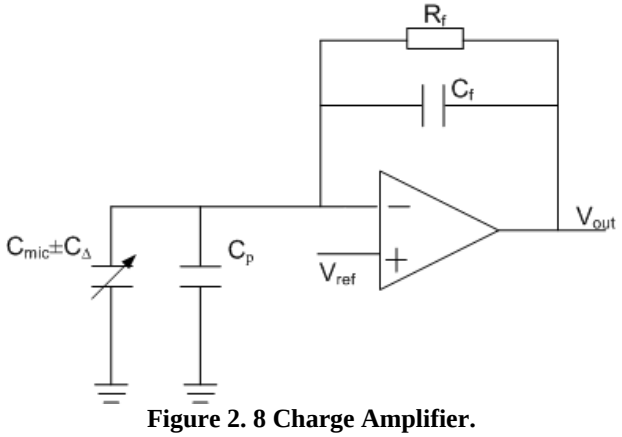

Figure 2. 8 Charge Amplifier.

2.3.1 Signal Level

When there is an acoustical signal exerted on the microphone, the time-varying capacitance will generate time-varying current which turns out to be time-varying voltage at the output because of the feedback network. The time-varying current is expressed as:

$$i_{mic}(t) = \frac{d(C_{mic} + C_{\Delta})}{dt} V_{ref} = \frac{\varepsilon_0 A}{d_{gap}} k V_{ref} \frac{dP(t)}{dt} \quad (2.\ 8)$$

The frequency-varying current is then given by:

$$i_{mic}(\omega) = \frac{\varepsilon_0 A}{d_{gap}} k \hat{P} V_{ref} \omega \quad (2.\ 9)$$

Therefore, the voltage on the output in the frequency domain is given by:

$$V_{out}(\omega) = \frac{\varepsilon_0 A}{d_{gap}} k \hat{P} V_{ref} \left(\frac{\omega R_f}{1 + j\omega R_f C_f}\right) = C_v \cdot V_{ref} \left(\frac{\omega R_f}{1 + j\omega R_f C_f}\right) \quad (2.\ 10)$$

The above calculations are all based on the assumption that the input acoustic signal is a pure sine wave and can be expressed as $\hat{P}\sin(\omega t)$, where $\hat{P}$ is amplitude of this sine wave signal. This assumption will also be used in the following parts.

Figure 2. 9 shows the amplitude of V_{out} versus frequency. Since the audio frequency that human being can hear is from 20Hz to 20KHz, the pole which is decided by $\frac{1}{2\pi R_f C_f}$ should be much lower than 20Hz to avoid attenuation on the signal. Thus the amplitude of the output signal in the audio band is $\frac{C_v \cdot V_{ref}}{C_f}$, assuming that this pole is much lower than 20Hz. Since C_f should be kept small in order not to attenuate the signal, the only way to move the pole downwards is to increase R_f. Assuming C_f is 1 pF, R_f should be about 8 GΩ to make the pole locate at 20Hz. And for noise consideration, the pole should be moved to even lower frequencies to minimize the thermal noise from R_f. Therefore DC biasing with virtual ground still can not avoid the implementation and noise issues associated with a huge resistor.

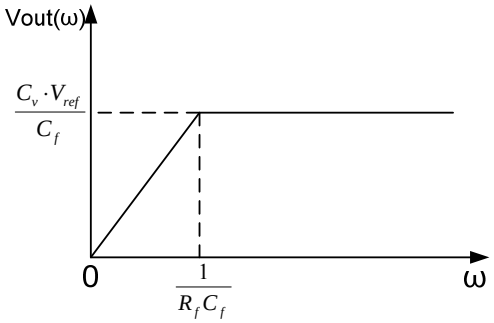

Figure 2. 9 V_{out}'s amplitude versus radio frequency.

2.3.2 Noise Calculation

Compared to DC biasing, this scheme can achieve high signal level at the output of the amplifier if C_f is smaller than C_{mic}. While for noise consideration, both of these two schemes

can not avoid the filtered huge resistance's noise, the 1/f noise from the preamplifier and the noise from the reference voltage or bias voltage. For simplicity, the following noise derivation will not take the reference voltage noise into consideration. If we denote the input referred noise of the amplifier as $\overline{v}_{noise,in}^{\ 2}$ which is shown in Figure 2. 10 , the total noise at the output can be expressed as:

$$v_{noise,out}^2 = \overline{v}_{noise,in}^2 \left(\frac{1 + j\omega R_f (C_{mic} + C_p + C_f)}{1 + j\omega R_f C_f} \right)^2 + \overline{v}_{noise,R_f}^2 \left(\frac{1}{1 + j\omega R_f C_f} \right)^2 \quad [V^2 / Hz] \tag{2. 11}$$

Referring the noise voltage power in equation (2. 11) back to a capacitive noise power at input by using the transfer function in equation (2. 10) yields:

$$C_{noise}^2 = \overline{v}_{noise,in}^2 \frac{1}{V_{ref}^2} \left(\frac{1 + j\omega R_f (C_{mic} + C_p + C_f)}{\omega R_f} \right)^2 + \overline{v}_{noise,R_f}^2 \frac{1}{V_{ref}^2} \left(\frac{1}{\omega R_f} \right)^2 \quad [F^2 / Hz] \tag{2. 12}$$

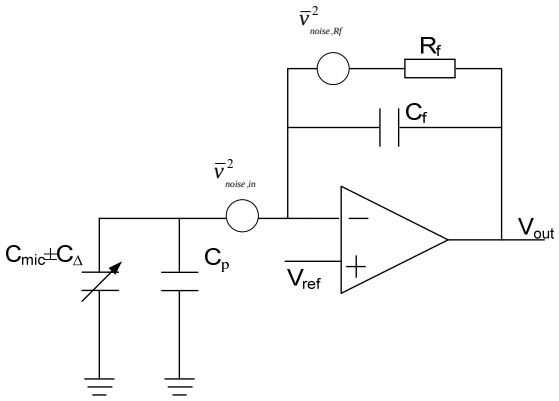

Figure 2. 10 Noise Source in Charge Amplifier

Equation (2. 11) shows that the input-referred noise of amplifier is amplified by the factor $\frac{C_{mic} + C_p + C_f}{C_f}$ in audio bandwidth (assume $\frac{1}{2\pi R_f C_f}$ is much smaller than 20Hz). To get higher signal level we need small C_f while the noise of the amplifier is amplified even more. Moreover, the 1/*f* noise of the amplifier still dominates.

2.4 AC Biasing

The problem with the charge amplifier scheme is mainly caused by input-referred noise of the amplifier. Normally, the 1/*f* noise of the amplifier will be dominant in the audio bandwidth. If we want to avoid the 1/*f* noise of the amplifier, one option is to modulate the signal to higher frequencies. That's why we introduce AC biasing to excite the microphone in order to realize amplitude modulation (AM). It is also expected that the noise level at high frequency is small and it will benefit the SNR result. The name "AC biasing" is derived from the property of the excitation source.

The AC biasing scheme is shown in Figure 2. 11. The large resistor is not necessary any more since the signal is moved to much higher frequency band and $1/f$ noise does not dominate as well. Moreover, this scheme is not sensitive to the parasitic capacitor since the voltage applied to the parasitic capacitor is constant due to the virtual ground.

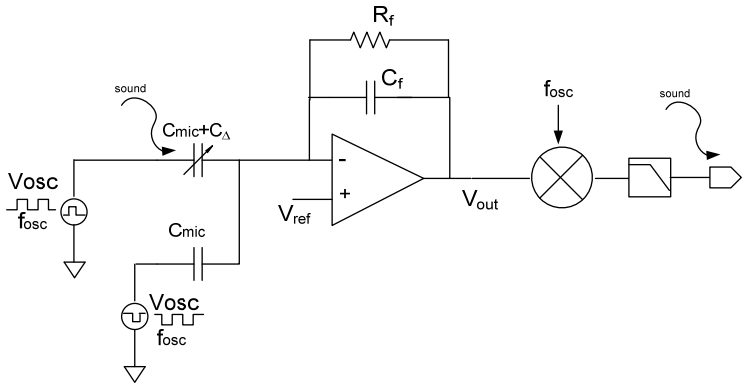

Figure 2. 11 AC biasing scheme.

The principle behind the AC biasing is mainly about amplitude modulation and demodulation. The microphone's capacitance varies with the sound signal. Meanwhile, the capacitor is excited by the AC source. Therefore, amplitude modulated current is generated. And with the feedback RC network, the modulated current generates a voltage at the output of the amplifier. The spectrum of the voltage here is composed of three components. One is carrier signal which is at the frequency of AC source. The other two are modulated signal at both sides of the carrier signal. The distance between the sidebands and carrier signal is exactly equal to the frequency of the sound. Figure 2. 12 illustrates the spectrum of the amplitude modulated signal with a square wave carrier.

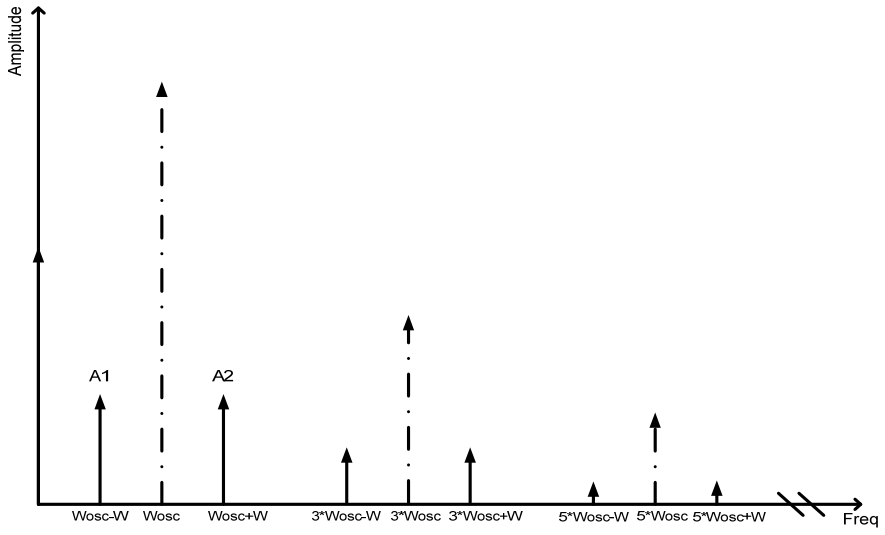

Figure 2. 12 Spectrum of the amplitude modulated signal.

Usually the carrier signal is much higher than the sidebands. The large amplitude of the carrier signal may cause saturation problem in the amplifier. Since it does not contain the sound's information, it can be reduced by a capacitor connected in parallel with the

microphone. The added capacitor has the same capacitance as C_{mic} and it is driven by the oscillation source which is 180 degrees out of phase with the source connected to the microphone. Thereby the signal at the output of the amplifier contains only the sidebands which have the information we want.

In order to demodulate sound from the signal, a synchronized mixer is added afterwards. The mixer is driven by the same frequency as the excitation source. Therefore, the two modulated sidebands are moved back and mixed together at the sound's frequency.

In ideal situation, the excitation source should generate a pure sinusoidal wave as carrier because it contains only one frequency component which is good for linearity of the sensor and filtering after demodulation. In IC design, however, it is much more difficult to implement a sinusoidal wave than generating a square wave. Therefore a square wave is chosen as excitation source. The spectrum of a square wave, however, contains odd harmonics of the base frequency. As a result, the demodulated signal is composed of several sidebands of the odd harmonics at sound's frequency and other higher frequency components which is shown in Figure 2. 12.

Therefore a low pass filter (LPF) is necessary to filter out the higher frequency components to limit the demodulated signal as pure as possible in the audio bandwidth.

2.4.1 Signal Level

To make the idea more distinct, a mathematical derivation of the principle is given below. Assume the excitation source is a square wave with amplitude V_{osc} and frequency f_{osc}, the Fourier Transform of the square wave is shown below:

$$F(t) = \frac{V_{osc}}{2} + \frac{2V_{osc}}{\pi}[\cos(\omega_{osc}t) - \frac{1}{3}\cos(3\omega_{osc}t) + \frac{1}{5}\cos(5\omega_{osc}t) - ...], \quad for\ \omega_{osc} = 2\pi f_{osc} \tag{2. 13}$$

Since the higher odd harmonics have decreasing amplitude and they will be filtered out in the end, the following derivation will only consider the base frequency component which is $\frac{2V_{osc}}{\pi}\cos(\omega_{osc}t)$.

Then the current through the microphone and the parallel capacitor is given by:

$$\begin{aligned} I(t) &= \frac{V_{osc}(t)}{Z_{mic}} + \frac{-V_{osc}(t)}{Z_{Co}} \\ &= jw_{osc}\frac{2V_{osc}}{\pi}C_v * \frac{1}{2}[\sin((w_{osc}+w)t) - \sin((w_{osc}-w)t)], \quad for\ \ C_v = C_{mic}k\hat{P} \end{aligned} \tag{2. 14}$$

Consequently, the amplitude of the sidebands at the output of the first amplifier can be expressed as: (A_1 and A_2 are shown in Figure 2. 12.)

$$A_1 = A_2 = \left| I(t) * \frac{R_f}{1 + j\omega_{osc}R_fC_f} \right| = C_v\frac{V_{osc}}{\pi}\frac{w_{osc}R_f}{\sqrt{1+(\omega_{osc}R_fC_f)^2}}\ [V] \tag{2. 15}$$

If $\frac{1}{2\pi R_f C_f}$ is much lower than the oscillation frequency f_{osc}, the amplitude of A_1 and A_2 can be expressed as $\frac{V_{osc}}{\pi}\frac{C_v}{C_f}$ which is about 10 dB ($20\log_{10}\pi$) lower than the signal level of the charge amplifier scheme.

When the mixer is added, the sidebands of all harmonics are moved back and mixed together at the base frequency. (So does the noise.) The mixer can be regarded as the input multiplied with a symmetric square wave which is indicates in Figure 2. 13[25]. The Fourier transform of the symmetric square wave is given by:

$$F(m(t)) = \frac{4}{\pi}[\cos(\omega_{osc}t) + \frac{1}{3}\cos(3\omega_{osc}t) + \frac{1}{5}\cos(5\omega_{osc}t) + ...] \quad (2.\ 16)$$

Then the demodulated signal at the output of the LPF is given by:

$$\begin{aligned} A_2' &= 2 * \left[A_2 * \frac{4}{\pi} + (\frac{1}{3})^2 * A_2 * \frac{4}{\pi} + (\frac{1}{5})^2 * A_2 * \frac{4}{\pi} + ... \right] \\ &\approx 3.1432 * C_v \frac{V_{osc}}{\pi} \frac{w_{osc} R_f}{\sqrt{1 + (\omega_{osc} R_f C_f)^2}} \cdot [V] \end{aligned} \quad (2.\ 17)$$

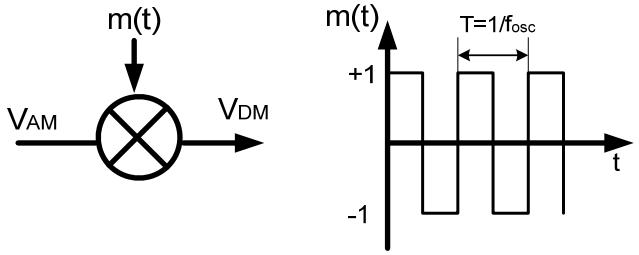

Figure 2. 13 Mixer demodulation.

2.4.2 Noise Calculation

The noise calculation of AC biasing before adding the synchronized mixer is almost the same as that of the charge amplifier scheme which is given by:

$$v_{noise,out}^{\ 2} = \bar{v}_{noise,in}^{2} \left(\frac{1 + j\omega R_f (2 * C_{mic} + C_p + C_f)}{1 + j\omega R_f C_f} \right)^2 + \bar{v}_{noise,R_f}^{2} \left(\frac{1}{1 + j\omega R_f C_f} \right)^2 \quad [V^2 / Hz] \quad (2.\ 18)$$

(Although the excitation source has phase noise, the noise calculation above is based on the assumption that the excitation source is noise free.)

Refer the output noise voltage power back to the capacitive noise power at input yields:

$$C_{noise}^2 = \bar{v}_{noise,in}^{2} (\frac{\pi}{V_{osc}})^2 \left(\frac{1 + j\omega R_f (2 * C_{mic} + C_p + C_f)}{\omega R_f} \right)^2 + \bar{v}_{noise,R_f}^{2} (\frac{\pi}{V_{osc}})^2 \left(\frac{1}{\omega R_f} \right)^2 \quad [F^2 / Hz] \quad (2.\ 19)$$

Equation (2. 19) is similar to equation (2. 12).The difference is that the input referred noise of the amplifier in AC biasing is mainly thermal noise rather than 1/*f* noise and it is amplified by $\frac{2*C_{mic}+C_p+C_f}{C_f}$ around the oscillation frequency since a compensation capacitor is added to decrease the carrier signal.

The noise calculation in equation (2. 18), however, does not consider the 1/*f* noise coming from the oscillator. Since the bias voltage across the sensor is of square wave type and swings from ground to supply voltage, the electrostatic force between the membrane and the back plate is changing from now and then which will introduce nonlinearity problem.

2.5 Practical Measurement

Since we have the MEMS microphone in hand, it is interesting to test how it behaves with electronics. Thus a PCB (Printed Circuit Board) level investigation is made mainly for the AC biasing scheme.

2.5.1 Amplitude Modulation

As has been explained in section 2.4, the principle behind the AC biasing scheme is based on amplitude modulation. It is also indicated in section 2.4 that the oscillation source used to drive the microphone should be of square wave type for considering a sine wave is more difficult to be implemented on transistor level. Since the measurement is at PCB level, a pure sine wave can be generated from an outside signal generator to drive the microphone. Consider the scheme in Figure 2. 14 (a), the signal generator which is connected to the microphone generates a pure sine wave with 0.5 voltage amplitude. The amplifier labeled as A1 is opamp NE5512 coming from the NXP Semiconductors. The sound is generated by PM5138A function generator through a speaker. It generates a sine wave with 10 V peak to peak amplitude and 1 KHz frequency. Due to the lack of a reference microphone, it is difficult to measure the actual sound pressure exerted on the membrane. The measurement is undertaken by setting V_{ref} with different voltages to prove that the sensitivity of the microphone is increased by increasing the equivalent bias voltage exerted on it. The transfer function from the input to output of A1 behaves like a band-pass filter which is shown in Figure 2. 14 (b). The lower limit of the frequency is decided by $\frac{1}{2\pi R_f C_f}$ which is about 14 KHz. And the higher limit of the frequency is decided by the bandwidth of the NE5512 which is about 3 MHz.

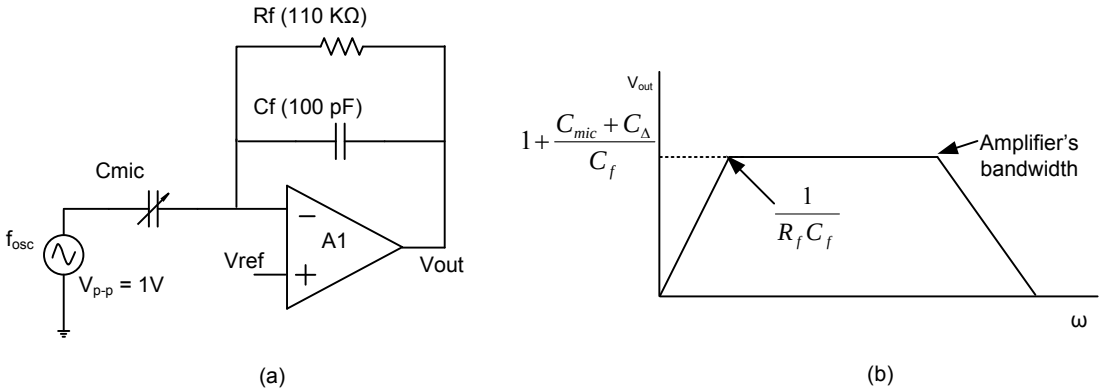

Figure 2. 14 (a) Scheme for realizing amplitude modulation. (b) Frequency response of the transfer function.

Due to the amplitude modulation, the signal at the output of A1 is composed of a main tone at the oscillation frequency with two relatively small sidebands which can be noticed on the spectrum analyzer. It is illustrated in Figure 2. 15 where f_{osc} represents the oscillation frequency; f_{sound} means the frequency of the input sound, A_m represents the magnitude of the main tone and A_s means the magnitude of the sidebands. If the pure oscillation sine wave can be represented by $V_{osc}*\sin(2\pi f_{osc}t)$ with V_{osc} as its amplitude, A_m and A_s in the flat band are given by:

$$A_m = \frac{C_{mic}V_{osc}}{C_f}\ [V] \tag{2. 20}$$

and

$$A_s = \frac{1}{2}\frac{C_{mic}V_{osc}k\hat{P}}{C_f}\ [V] \tag{2. 21}$$

where C_f is the feedback capacitor, k has been mentioned in equation (1. 7) and P is the rms sound pressure exerted on the membrane. From equation (2. 21), it can be seen that the output signal is proportional to the amplitude of the oscillation source.

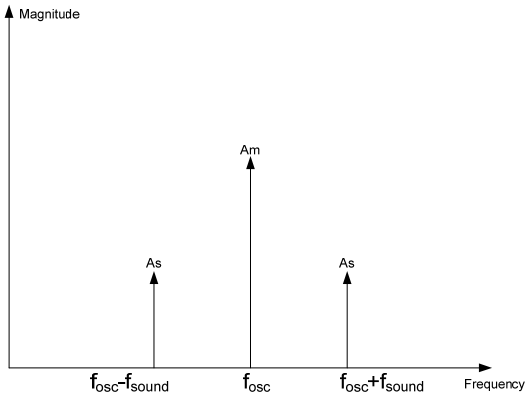

Figure 2. 15 Amplitude-modulated signal's spectrum.

Figure 2. 16 shows the magnitude of the side band versus oscillation frequency under different bias voltages. The trend of these curves roughly performs like a band-pass filter as has been mentioned before. These curves in the band (14 KHz - 3 MHz) are not uniform as it is supposed to be. The peak sensitivity appears at 1 MHz.

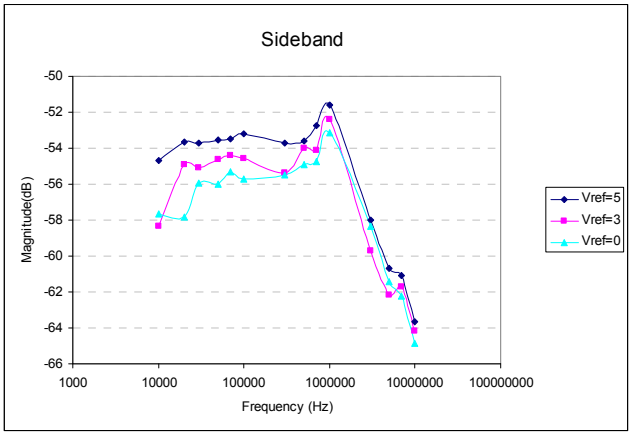

Figure 2. 16 Magnitude of the side band under different bias voltage.

This effect may caused by the sensor itself. For a normal MEMS microphone, the curve of the sensitivity versus acoustical frequency is supposed to be flat at least in the audio band which is from 20 Hz to 20 KHz. The microphone used in the measurement can guarantee a flat frequency response up to 100 KHz acoustic frequency. When an oscillation source is exerted, the membrane of the microphone also vibrates with the oscillation frequency. Since the 3 MHz oscillation frequency has exceeded the flat frequency response band, there is possibility that the microphone dose not perform normally.

Figure 2. 16 not only proves that the sensitivity increases with increasing bias voltage but also provides a rough idea about the performance of the microphone driven by a sine wave oscillation source of different oscillation frequency.

The magnitude of the main tones versus oscillation frequency with different bias voltage is shown in Figure 2. 17. The trends of these three curves are almost the same with the side band in Figure 2. 16.

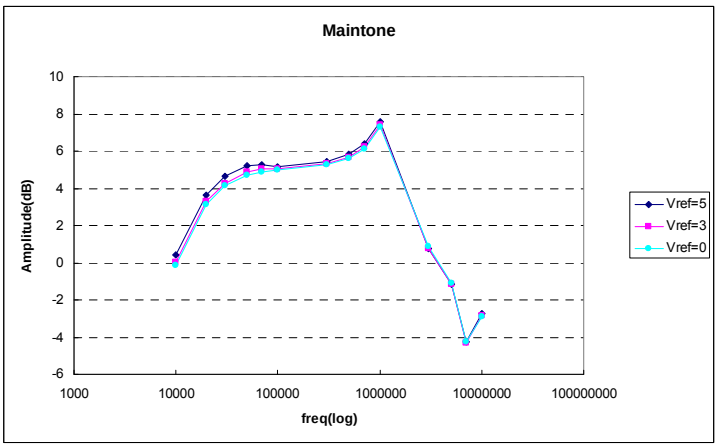

Figure 2. 17 Magnitude of the main tone under different bias voltage.

Comparing the magnitude in Figure 2. 16 and Figure 2. 17, we can see that the magnitude of the main tone is almost 60 dB higher than that of the side band. Therefore, it is necessary to reduce the main tone otherwise it may cause saturation problem of the preamplifier.

2.5.2 AC Biasing Setup

Figure 2. 18 shows the AC biasing scheme implemented at PCB level. The chain composed of NANDs and inverters is used to setup a two-phase non overlapping clock by decreasing the duty cycle of the square wave generated from an external signal generator. Since the supply voltage of all the NANDs and inverters on the board are 14V, clock signal Φ1 and Φ2 swings from 0 to 14V consequently. Therefore a resistive voltage divider is added to decrease the swing to a lower value. The potentiometer R_{p1} and R_{p2} are for the purpose of making the swing of Φ1 and Φ2 more tunable.

The opamps which are labeled as A1, A2 and A3 are opamp NE5512 coming from the NXP Semiconductors which has $30\,nV/\sqrt{Hz}$ as input referred noise and 3 MHz as small signal unity gain bandwidth. The STM-3 Microphone Preamplifier is for the purpose of amplifying the demodulated signal more easily by only tuning the mounted potentiometer.

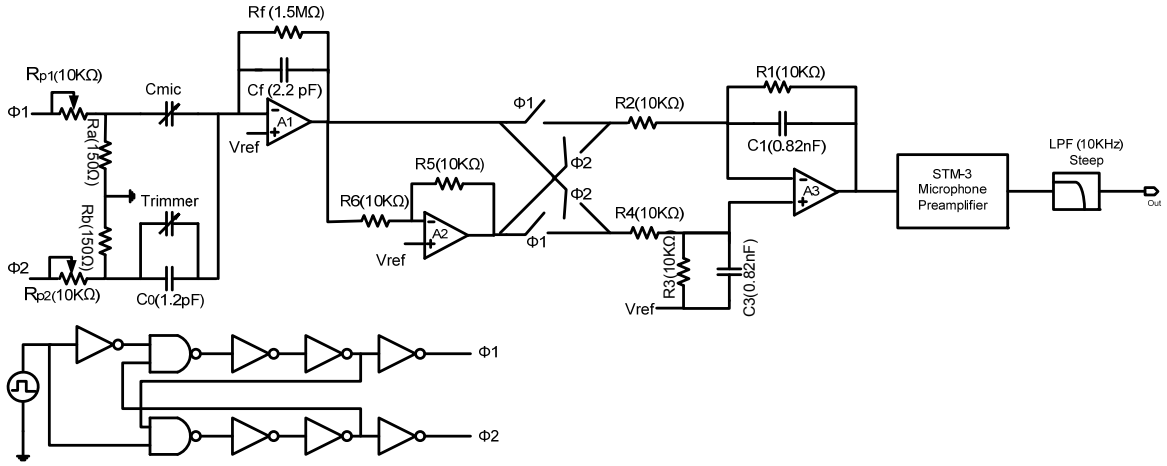

Figure 2. 18 AC biasing scheme realized on PCB.

The supply voltage is affected by the clock due to the fact that all the devices on the board share the same supply voltage. Thus, the system generates more harmonics than we expected. The RC network (R1&C1, R3&C3 in Figure 2. 18) which provides 20 KHz first-order cut-off frequency is not enough to reduce the harmonics. Therefore a 4^{th}-order LPF with 10 KHz cut-off frequency is placed after to filter out the unexpected interferences from the clock and the higher harmonics.

2.5.3 Noise Analysis

We are interested in the noise behavior on the first stage of AC biasing which is shown in Figure 2. 19. The reason is that the first stage mainly decides the sensitivity of the scheme and the noise calculation is comparatively less complicated which will reduce the difference between the theoretical calculation and measurement.

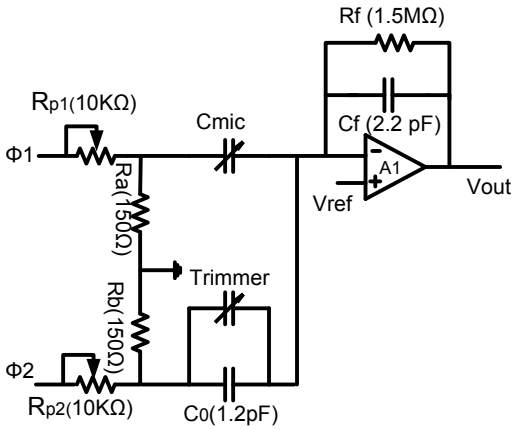

Figure 2. 19 The first stage for AC biasing.

The total noise at the output is given by:

$$V_{ntot}^2(f) = 2*\left(4k_BTR_{p1}*(\frac{R_a}{R_a+R_{p1}})^2 + 4k_BTR_a*(\frac{R_{p1}}{R_a+R_{p1}})^2\right)\cdot(\frac{j\omega R_f C_{mic}}{1+j\omega R_f C_f})^2$$
$$+V_{n,opamp,in}^2\cdot(\frac{1+j\omega R_f(C_f+C_{mic}+C_{mic})}{1+j\omega R_f C_f})^2 \qquad (2.\ 22)$$
$$+4k_BTR_f\cdot(\frac{1}{1+j\omega R_f C_f})^2 \quad [V^2/Hz]$$

where R_{p1}=R_{p2}=1950 Ω (to decrease swing of the excitation voltage exerted on the microphone to 1 V), R_a=R_b and $V_{n,opamp,in}^2$ is the input referred noise of the amplifier labeled as A1.

Equation (2. 22) was used to write a MATLAB script which yields Figure 2. 20. It shows the noise spectral density at the output of A1. It gives a general idea about the noise distribution at different frequencies. The plot shows that the noise level is low at high frequencies. Thus the amplitude modulation is expected to operate at high frequencies to get better signal-to-noise ratio.

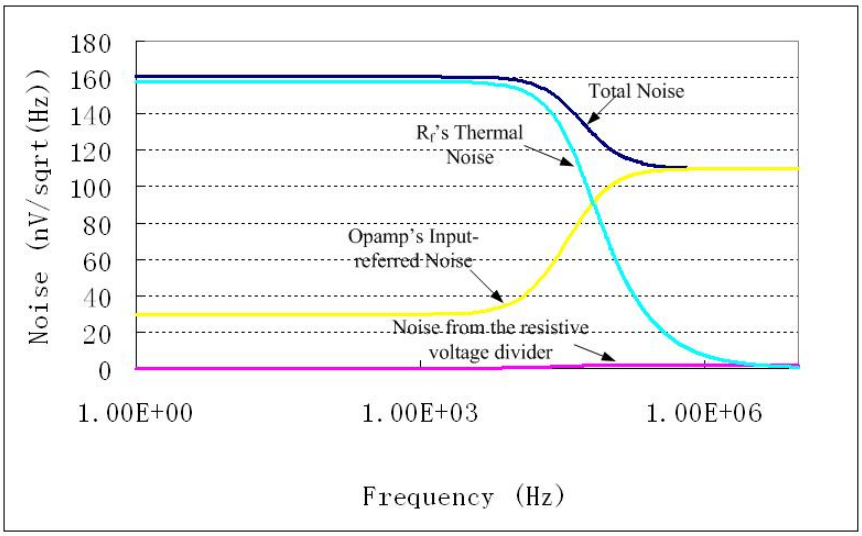

Figure 2. 20 Noise versus frequency for the first stage of AC biasing.

The noise at the output of A1 is also measured to check if the calculation in equation (2. 22) is correct. The noise measurement is undertaken by shorting the oscillation source to the ground. The result is shown in Figure 2. 21. The two curves agree to each other.

We can also predict the input-referred thermal noise level of the preamplifier by using equation (2. 15) and equation (2. 22). Assuming the amplitude of the oscillation source is 3.3 V and the feedback capacitor is 200 fF, the thermal noise level of the preamplifier is approximately $7\,nV/\sqrt{Hz}$ to achieve 60 dB SNR on the first stage without considering the thermal noise generated from the feedback resistor. It is not easy to realize such an amplifier on transistor level.

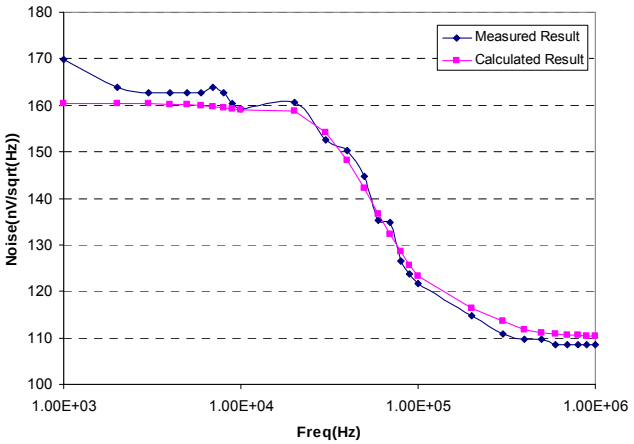

Figure 2. 21 Comparison of the noise measurement and calculation result for AC biasing.

2.5.4 Check Functionality

According to equation (1. 8) and (1. 9), the sensitivity of a microphone is proportional to the bias voltage exerted on it. And as has been mentioned in section 1.2, the pull-in voltage of the microphone is around 8V by experiment. Thus it is interesting to test the behavior of the microphone with different bias voltage and especially with pull-in voltage. Therefore, two

modes are tested. One is the normal mode which means that the equivalent bias voltage does not exceed the pull-in voltage. The other one is the collapse mode which means equivalent bias voltage exerted on the microphone is close or equal to the pull-in voltage. The collapse mode is expected to have high sensitivity because of the high bias voltage.

Normal Mode

Figure 2. 22 illustrates the signal level to oscillation frequency response with two different biasing setups. The lower curve is tested with V_{ref} =3 V and V_{osc} =1 V. The higher curve is tested with V_{ref} = 5V and V_{osc} = 5V. V_{osc} is the amplitude of the oscillation source exerted on the microphone. Since the DC value of a square wave is half of its peak to peak amplitude, the equivalent DC voltage exerted across the microphone are both 2.5 V under two cases. It is illustrated in Figure 2. 23. The aim is trying to keep the sensitivity of the microphone same under these two cases.

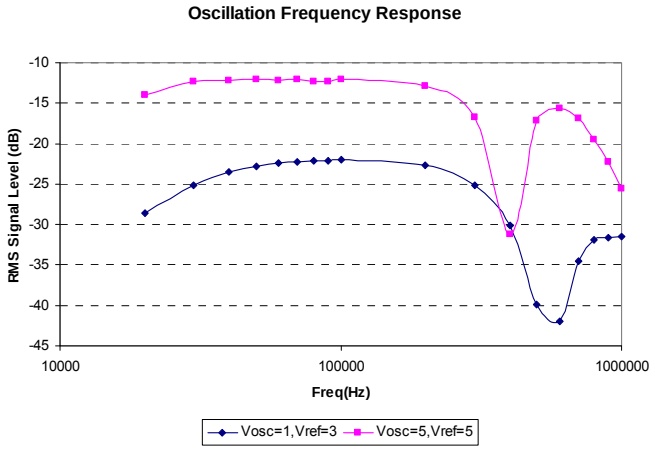

Figure 2. 22 Response to oscillation frequency with different oscillation amplitude in normal mode.

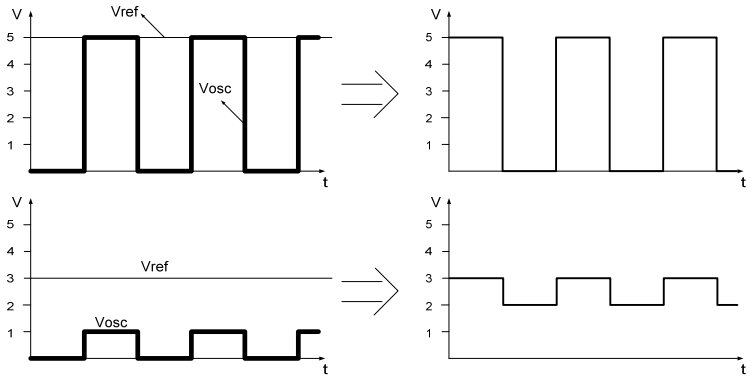

Figure 2. 23 Equivalent voltage's waveform exerted on the microphone under two cases.

The two curves are flat when the oscillation frequency is lower than 200 KHz. They drop suddenly at 400 KHz and 600 KHz respectively. It may caused by the characteristic of the microphone itself. With oscillation source connected to the fixed back plate, the membrane will vibrate at the oscillation frequency without any acoustical signal input. It will cause nonlinearity and resonant issues. The microphone might behave badly under certain oscillation frequency. The two curves also imply that the maximum oscillation frequency of a

square wave type excitation source that the microphone can handle is approximately 200 KHz.

Equation (2. 15) indicates that the amplitude of the modulated signal which contains the sound's information is linear with the oscillator's amplitude. Therefore, the signal of the case with V_{osc} = 5 V should be 14 dB ($20\log\frac{5}{1}$) larger than that of the case with V_{osc} = 1 V. Figure 2. 22, however, shows that the upper curve is only about 10dB higher than the lower curve. If we look into the equivalent voltage exerted on the microphone in two cases, it can be seen that in one case the voltage swings from 0V to 5V and in another case the voltage swings from 2V to 3V. It is illustrated in Figure 2. 23.

Figure 1. 7 indicates that the microphone has different sensitivity with different bias voltage. That is, in one cycle of the clock, the microphone has two different sensitivities. Therefore the 4 dB difference may come from the different average sensitivity under the two cases. Figure 2. 24 illustrates the effect. To test this, we can simply do the following test.

The DC biasing scheme is the most direct way to test the different sensitivity with different bias voltage. Therefore, measure the output signal level with bias voltage of 0.1V (with 0V bias voltage, there will not be a signal come from the microphone), 2V, 3V and 5V respectively in DC biasing setup. The results are listed in Table 2. 1. During this measurement, the distance between the speaker and the microphone is kept constant.

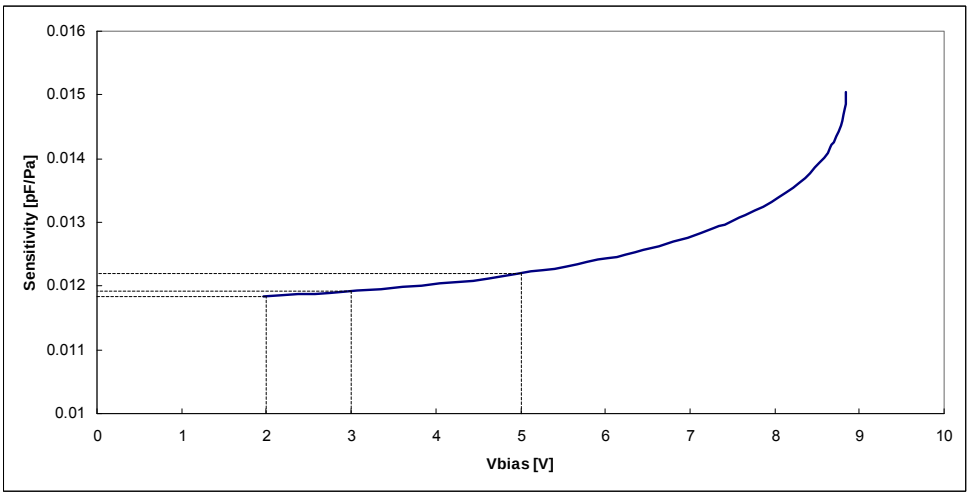

Figure 2. 24 Different average sensitivity in two cases.

DC Voltage(V)	RMS Signal Level (dB)	Average (dB)
0.1	-54	-38.5
5	-23	
2	-37	-35
3	-33	

Table 2. 1 Measurement in DC biasing with different bias voltage.

Table 2. 1 implies that with the same sound pressure level input, the microphone generates different signal with different bias voltage. The difference between the average signal levels of the two cases explains the 4 dB difference between measurement and equation (2.12) because equation (2. 15) does not take different sensitivity into consideration

Figure 2. 25 shows the waveform displayed on the oscilloscope with V_{ref}= 5 V and V_{osc} = 5 V. The demodulated signal on the oscilloscope in this case is very stable and clear.

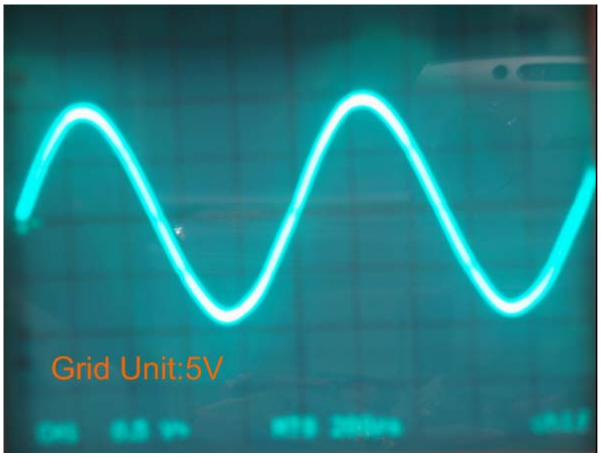

Figure 2. 25 Demodulated signal in normal mode

Collapse Mode

The response to oscillation frequency in collapse mode is shown in Figure 2. 26. The figure also includes the response in normal mode to compare with. Around 100 KHz, the collapse mode generates about 10 dB larger signal than the normal mode. However, the response has some resonant behaviors.

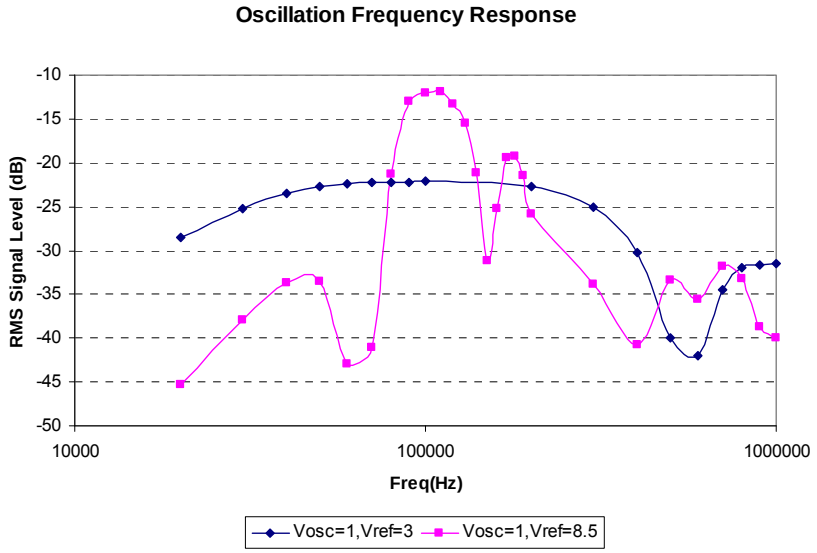

Figure 2. 26 Comparison of frequency response between normal mode and collapse mode.

The demodulated waveform at the highest peak appeared in Figure 2. 26, however, is highly distorted which is shown in Figure 2. 27.

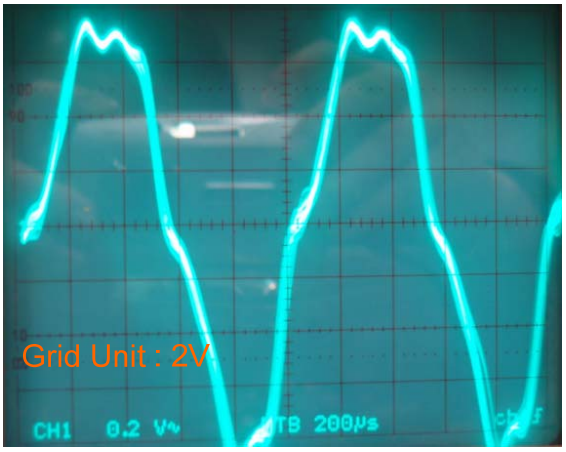

Figure 2. 27 The nonlinear demodulated signal in collapse mode at 100KHz oscillation frequency.

The collapse mode can also behave normally at certain oscillation frequency. Figure 2. 28 shows the result with 120 KHz oscillation frequency. But the amplitude is lower than that in Figure 2. 25 and Figure 2. 27 which means that the collapse mode does not have better performance than the normal mode.

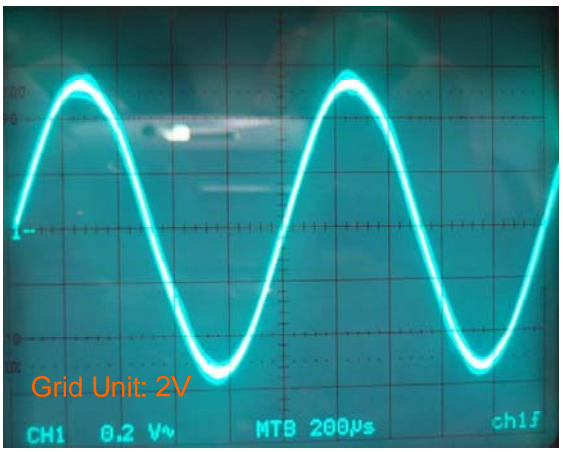

Figure 2. 28 The demodulated signal in collapse mode at 120KHz oscillation frequency.

2.5.5 Conclusion

This part investigates the AC biasing on PCB level. And the normal mode and collapse mode of AC biasing is investigated further. The aim for biasing the microphone in collapse mode is intended to make the microphone generate large signal. The results, however, show that the behavior of the collapse mode does not exceed the normal mode as much as we expected. And the non-linearity and instability of collapse mode counteracts its advantages.

2.6 Conclusion

Table 2. 2 shows a comparison between the three different readout schemes in signal and noise.

	Signal @ Input (F)	Noise @ Input (F^2 / Hz)
DC Biasing	$C_{v,rms}$	$\left(\frac{C_{mic}+C_p}{V_{ref}}\right)^2 \bar{v}^2_{noise,Rb} + \left(\frac{C_{mic}+C_p}{V_{ref}}\right)^2 \bar{v}^2_{noise,in,1/f}$
Charge Amplifier	$C_{v,rms}$	$\bar{v}^2_{noise,in} \frac{1}{V_{ref}^2}\left(\frac{1+j\omega R_f(C_{mic}+C_p+C_f)}{\omega R_f}\right)^2 + \bar{v}^2_{noise,Rf} \frac{1}{V_{ref}^2}\left(\frac{1}{\omega R_f}\right)^2$
AC Biasing	$C_{v,rms}$	$\bar{v}^2_{noise,in} (\frac{\pi}{V_{osc}})^2\left(\frac{1+j\omega R_f(2*C_{mic}+C_p+C_f)}{\omega R_f}\right)^2 + \bar{v}^2_{noise,Rf} (\frac{\pi}{V_{osc}})^2\left(\frac{1}{\omega R_f}\right)^2$

Table 2. 2 Comparison between three schemes

where

$\bar{v}^2_{noise,Rb} = 4k_BTR_b\left(\frac{1}{1+j\omega R_b(C_{mic}+C_p)}\right)^2$, $\bar{v}^2_{noise,Rf} = 4k_BTR_f\left(\frac{1}{1+j\omega R_f C_f}\right)^2$, $\bar{v}^2_{noise,in,1/f}$ stands for the $1/f$ noise dominated input referred noise of an amplifier and $\bar{v}^2_{noise,in,thermal}$ stands for the thermal noise dominated input referred noise of an amplifier. k_B is Boltzmann constant which is equal to $1.38*10^{-23}$ J/K. T is temperature (K).

From the above table and the explanation in section 2.2 to 2.4, we can not draw a conclusion that a certain scheme will definitely exceed the other two schemes in certain specification. They all have advantages and disadvantages. To summarize, the pros and cons of different schemes are listed in Table 2. 3. For instance, the charge amplifier scheme has a higher sensitivity with a small feedback capacitor while the noise of amplifier is amplified by a large factor at the same time. The AC biasing scheme seems to avoid the $1/f$ noise of the amplifier but the amplitude modulation decreases the signal level and AC excitation source exerted on the microphone generates nonlinearity problems.

	Advantages	Disadvantages
DC Biasing	Simple topology	• Large resistor is needed for low noise and small leakage current. • Moderate sensitivity because of parasitics. • $1/f$ noise.
Charge Amplifier	Insensitive to the parasitic capacitance and have high signal level.	• Large feedback resistor is needed for low noise and small leakage current. • $1/f$ noise.
AC Biasing	Get rid of 1/f Noise, insensitive to the parasitic capacitance and large feedback resistor is unnecessary.	• Oscillator has phase noise. • Changing Electrostatic force between the two plates may cause nonlinearity issues. • Low side band level.

Table 2. 3 Advantages and disadvantages for the three schemes.

The main difference between the DC biasing and the use of a charge amplifier is the effect of parasitic capacitances. The virtual ground established by a charge amplifier neutralizes the effect of parasitic capacitances. With DC biasing, however, another method can be used to

reduce the effect of parasitic capacitance. This method will be explained in detail in the following chapters.

Chapter 3. New Readout Scheme with Positive Feedback

This chapter will introduce a new readout scheme with which the parasitic capacitances of a DC biased microphone can be reduced. First, the basic principle behind the scheme will be explained (section 3.1), followed by theoretical analysis of the output signal level and the noise of the new scheme (section 3.2). The system level analysis described in section 3.3 decides the final scheme to be implemented. Specifications for amplifier in the interface circuit are proposed consequently (section 3.4).

3.1 Miller Effect

The Miller effect is a common phenomenon that occurs in many analog circuits. It is first described by John M. Miller in [26].

The Miller effect refers to the fact that the impedance seen at the input of an amplifier depends on the impedance connected between input and output of the amplifier. Consider an ideal amplifier of gain -H with impedance connected from input to output which is shown in Figure 3. 1

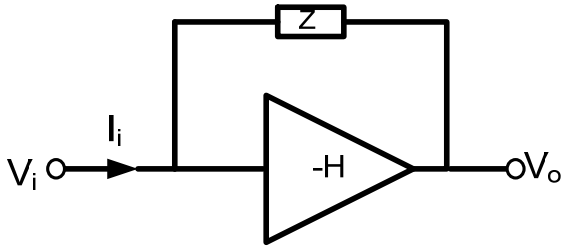

Figure 3. 1 Impedance connected from input to output of an amplifier

The input current I_i is calculated as:

$$I_i = \frac{V_i - V_o}{Z} = \frac{(1+H)V_i}{Z} \tag{3. 1}$$

Then the equivalent impedance at the input of the amplifier is:

$$Z_{in} = \frac{V_i}{I_i} = \frac{Z}{1+H} \tag{3. 2}$$

Applying the same calculation, the equivalent impedance at the output of the amplifier is:

$$Z_{out} = \frac{Z}{1+\frac{1}{H}} \tag{3. 3}$$

Since most amplifiers have negative gain, the presence of the Miller effect means that their effective input impedance is (1+H) times smaller if the impedance is resistive or inductive. And if the impedance is capacitive, the effective input capacitance is (1+H) times larger.

For non-inverting amplifiers, the Miller effect results in a negative capacitive impedance at the input. Therefore, we can use the Miller effect of a non-inverting amplifier to reduce the parasitic capacitance associated with DC biasing.

3.2 Miller Effect in DC Biasing

A capacitor C_f is connected from input to output of the preamplifier in DC biasing which is shown in Figure 3. 2 (a):

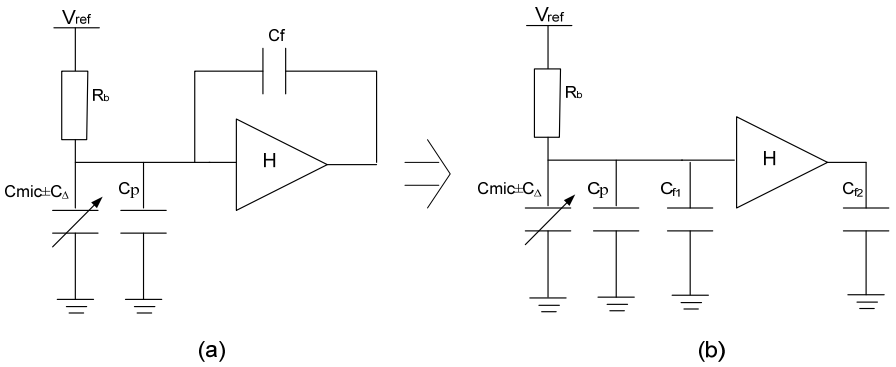

Figure 3. 2 Miller effect in DC biasing

Figure 3. 2 (b) shows the Miller effect of C_f. From Miller theory, we know that C_{f1} is equal to $(1-H)C_f$ and C_{f2} is $(1-1/H)C_f$. If H is larger than 1, C_{f1} is negative. With this negative capacitive impedance, the static capacitance of the sensor C_{mic} and the parasitic capacitance of the preamplifier and the sensor C_p can be reduced.

Based on the constant charge theory, the rms signal at the output is given by:

$$\Delta V_{rms} = H \cdot \frac{C_{v,rms} * V_{ref}}{C_{mic} + C_p + (1-H)C_f - C_{v,rms}} \quad [V] \tag{3. 4}$$

In this way, a proper combination of H and C_f can make the denominator of the fraction in equation (3. 4) extremely small which results in a large signal.

Although the signal is boosted with the positive feedback capacitor C_f, the noise is increased at the same time. The noise at the output of the preamplifier is given by:

$$\bar{v}_{noise,tot}^{\,2} = 4k_B T R_b * \left| \frac{H}{1 + j\omega R_b [C_{mic} + C_p + (1-H)C_f]} \right|^2 + \bar{v}_{noise,in}^{\,2} * \left| \frac{H[1 + j\omega R_b (C_f + C_{mic} + C_p)]}{1 + j\omega R_b [C_{mic} + C_p + (1-H)C_f]} \right|^2 \quad (3.5)$$

where $V_{noise,in}^{\,2}$ is the input referred noise of the preamplifier.

Equation (3. 4) and (3. 5) were used to write a MATLAB script with $C_{mic} + C_p = 5$ pF and H = 11. The resulting signal level, noise integrated in the audio bandwidth and the signal-to-noise ratio is shown in Figure 3. 3 by sweeping C_f from 0 to 0.5 pF with 0.01pF step size. More details of the scripts can be found in Appendix C.

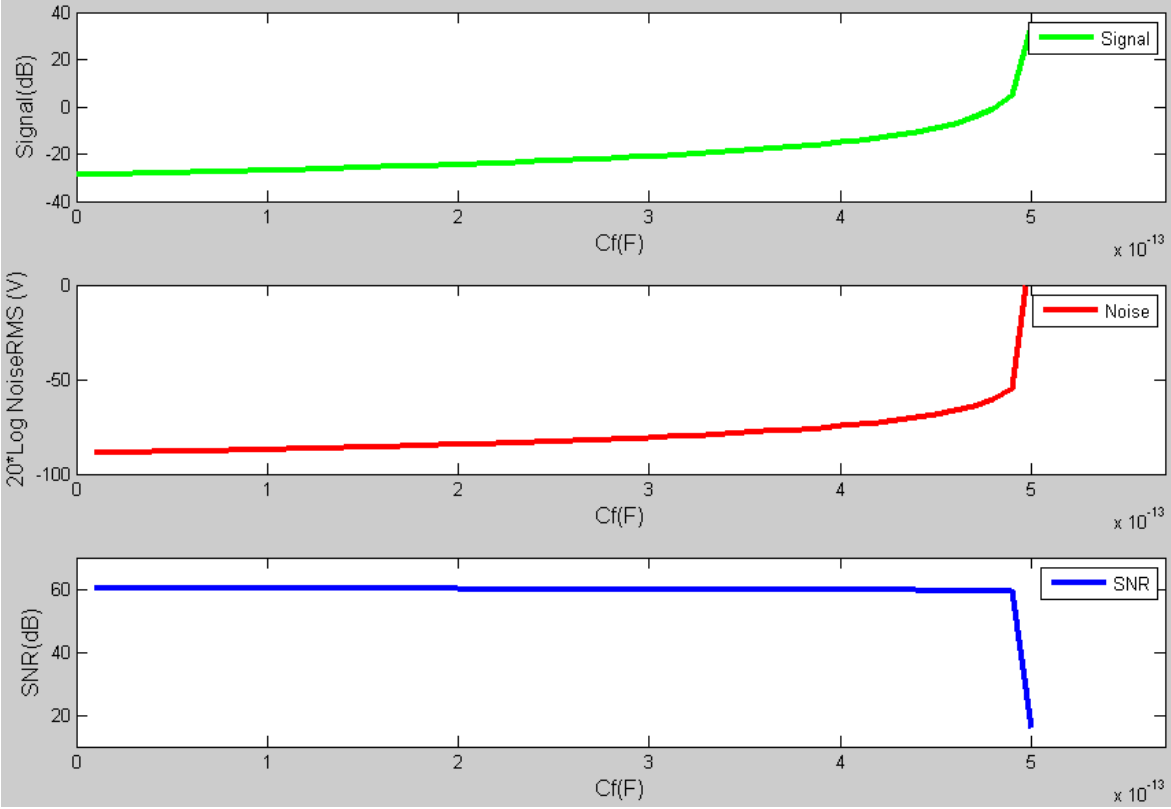

Figure 3. 3 Matlab simulation result of the DC biasing with positive feedback C_f.

Figure 3. 3 shows that the signal and rms noise increases with C_f almost at the same rate. But the SNR curve indicates that SNR drops dramatically when (1-H)C_f is equal to the value $C_{mic} + C_p$. The reason for the big drop is that the pole in the fraction of equation (3. 5) becomes infinite when (1-H)C_f = $C_{mic} + C_p$. At this point, the large thermal noise from the huge resistor R_b is not filtered any more. And the transfer function of the preamplifier will amplify the input referred noise to infinity at high frequencies. This will make the integrated noise incredibly large.

But in the range where SNR can be regarded as constant, the sensitivity of the sensor is increased about 20 dB compared to DC biasing which is a promising advantage. Although the signal at the output can be increased by increasing the gain of the preamplifier, it gives rise to some problems such as the nonlinearity, GBW and power consumption of the amplifier.

3.3 System Level Analysis

If we want to implement the DC biasing scheme with positive feedback at the transistor level, the first question that arises is how to make a non-inverting amplifier with a specific gain.

3.3.1 Define the Gain of the Preamplifier

The most common method is using a negative resistive feedback network with a high-gain amplifier to accurately define the closed-loop gain which is shown in Figure 3. 4. The gain is decided by the factor $1+\frac{R_1}{R_2}$ if the open loop gain of the preamplifier is quite large. This resistive negative feedback network, however, will amplify the DC voltage at input by the same ratio as well which will cause problems on the common-mode voltage at the output.

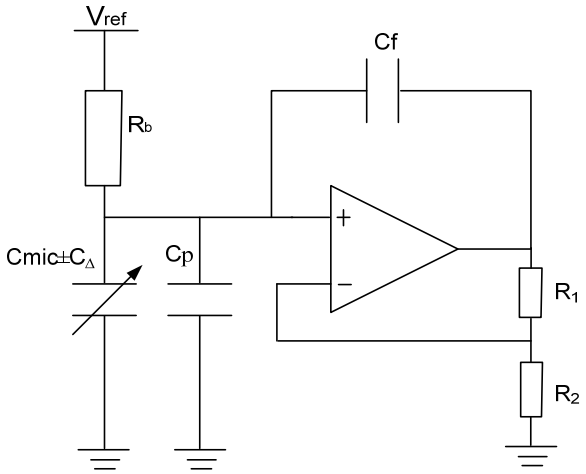

Figure 3. 4 A non-inverting amplifier with closed loop gain.

One solution is to add AC coupling capacitor C_2 in series with R_2 to block the DC signal which is shown in Figure 3. 5. The transfer function from input to output is becoming:

$$\frac{V_{out}(\omega)}{V_{in}(\omega)} = \frac{1+ j\omega(R_1 + R_2)C_2}{1+ j\omega R_2 C_2} \tag{3. 6}$$

The transfer function indicates that the pole which is decided by $\frac{1}{2\pi R_2 C_2}$ should be lower than 20 Hz to allow the signal in the audio band to go through without substantial attenuation. For noise consideration, R_2 should be kept small since its thermal noise will be amplified by the closed loop gain. For R_2=10KΩ, C_2 should be larger than 0.8 μF to move the pole below 20 Hz. 0.8 μF, however, is too large to be realized in CMOS technology.

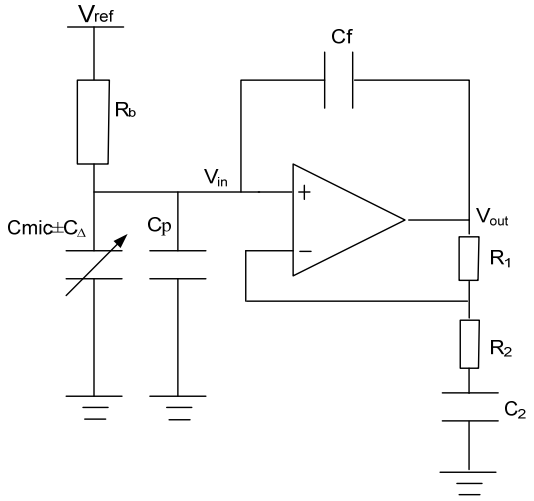

Figure 3. 5 A non-inverting amplifier with AC-coupled closed loop gain.

Another solution is to regulate the common-mode voltage at the output with the same voltage as V_{ref} by an extra voltage source connected to R_2. The scheme is shown in Figure 3. 6. In this way, the DC level on the two inputs and the output are all regulated to V_{ref}. But the $1/f$ noise from the voltage regulator will create a new problem, since its noise will also be amplified by the factor $1+\frac{R_1}{R_2}$. A low-noise voltage regulator adds extra complications to the design which is not so promising.

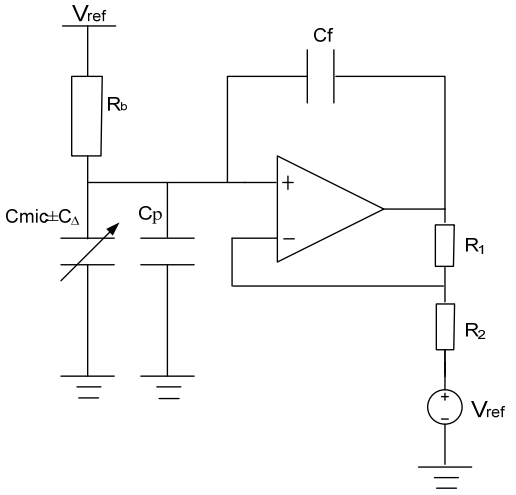

Figure 3. 6 A non-inverting amplifier with voltage regulator.

The microphone is preferably biased by the supply voltage to get the highest possible sensitivity. In most closed-loop amplifiers, however, the common-mode voltage at the output and input are usually located at mid-rail to maximize the swing at the output. Therefore, the bias voltage of the microphone in a closed loop amplifier is limited. Although a source follower is able to shift the input DC level, the additional noise and large area of it brings about another problem.

From the above analysis, it seems that an amplifier with a resistive feedback which forms a well-defined closed loop gain is not a good choice for noise consideration. Therefore an amplifier whose gain is not defined by a close loop will be used. The scheme is shown in

Figure 3. 7. The buffer connected after the preamplifier is for testability concern since the parasitic capacitance of the contact of a common measurement device is about 50 pF.

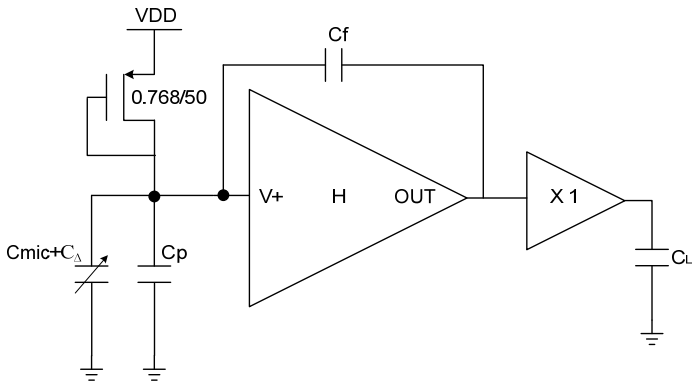

Figure 3. 7 DC biasing with positive feedback on system level.

3.3.2 Diode Connected MOSFET

In Figure 3. 7, the large resistance which is used to bias the microphone is realized by a diode connected PMOS with the aspect ratio of 0.768/50. The source and body of the PMOS are connected together which are not shown in this figure.

The I-V characteristics of a gate-drain connected MOS transistor which is illustrated in Figure 3. 8 are qualitatively similar to a pn-junction diode. When the forward bias voltage across the diode exceeds V_{on}, the diode starts conducting. When the current is small which can be regarded as leakage current, the diode can have very high impedance. In this design, the diode-connected PMOS are connected to a capacitive microphone which indicates that the DC current in the PMOS is almost zero. It implies that the diode-connected PMOS are working in the region where V is much smaller than V_{on}. In this region, since the slope of I over V is almost zero, the impedance of the diode-connected PMOS is quite high.

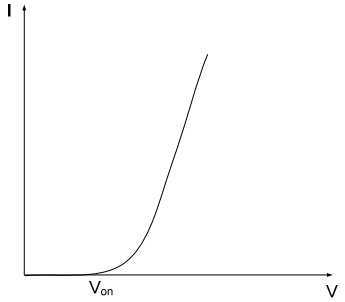

Figure 3. 8 I-V characteristic of a diode.

Consider the cross section of a diode-connected PMOS which is shown in Figure 3. 9 (a), the drain to n-well pn junction forms an anti-parallel diode D1 to the PMOS itself. The equivalent scheme can be seen in Figure 3. 9(b). Both D1 and D2 will not affect the leakage current much. (D2 is formed by n-well and p-substrate junction.) The source to n-well pn junction is not shown here since it is shorted.

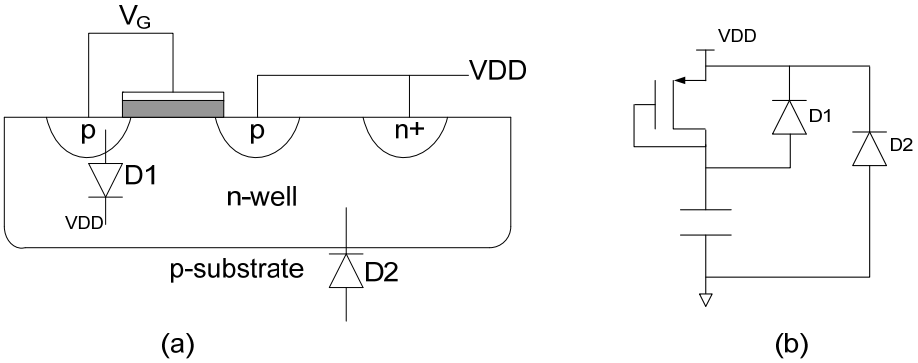

Figure 3. 9 (a) Cross section of a diode-connect PMOS. (b) Equivalent schematic.

If we replace the PMOS with a diode-connected NMOS, however, the leakage current will increase and the constant charge assumption will not be true anymore. Look into the cross section of a diode-connected NMOS shown in Figure 3. 10(a), the parasitic diode D2 formed by the source and substrate pn junction introduces a leakage path directly from the source of the NMOS to ground.

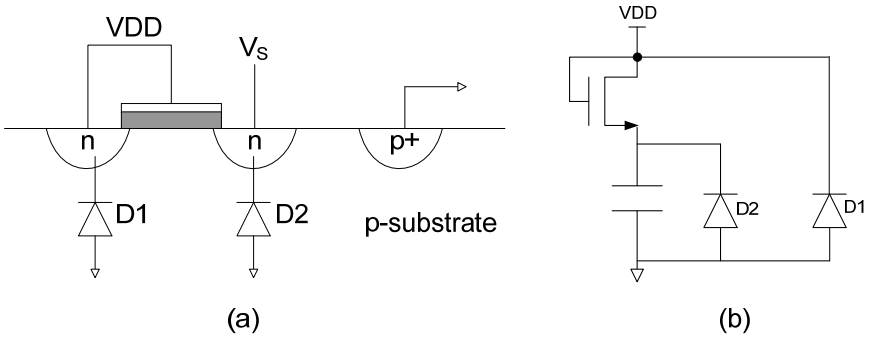

Figure 3. 10 (a) Cross section of a diode-connect NMOS. (b) Equivalent schematic.

To achieve 60dB SNR (A-weighted), and if the noise of the diode-connected PMOS can be regarded as thermal noise of its impedance, the impedance should be at least about 103 GΩ by considering the preamplifier is ideal (no noise and no parasitic capacitance). In Cadence simulation, the equivalent impedance of a diode-connect PMOS with 0.768/50 aspect ratio is about 7.65 TΩ under 27°C. With this value, the SNR on the microphone without preamplifier is about 79 dB which gives 19 dB noise margin for the preamplifier. (Not consider the parasitic capacitance of the preamplifier)

3.3.3 Stability

Consider a positive feedback system which is shown in Figure 3. 11(a), the feedback factor β(s) is defined by $X_f(s)/Y(s)$. Therefore the β(s) in Figure 3. 11(b) is given by:

$$\beta(s) = \frac{Z_{in}}{Z_{in} + Z_f} \tag{3. 7}$$

Thus the loop gain is given by:

$$\beta(s)H(s) = \frac{Z_{in}}{Z_{in} + Z_f} H(s) \tag{3. 8}$$

When the system is stable, the loop gain should be smaller than 0 dB. Assume the impedance of the diode-connected PMOS is much larger than that of the microphone, then Z_{in} is about $\frac{1}{j\omega(C_{mic} + C_p)}$ and Z_f is $\frac{1}{j\omega C_f}$. Thus the stable condition is $C_f < \frac{C_{mic} + C_p}{|H - 1|}$ by making the absolute value of equation (3. 8) smaller than 1.

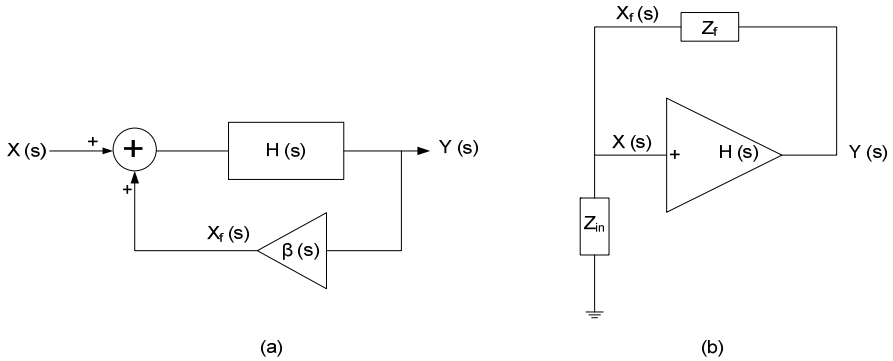

Figure 3. 11 Positive feedback system

3.4 Specification for Preamplifier

The preamplifier is the main core for an interface circuit. The specification for the preamplifier has to be decided before implementing it into transistor level. In this design, the gain, bandwidth and noise are the most important specifications. These must be chosen after considering the performance of the microphone.

The whole design is based on CMOS014 technology from NXP Semiconductors. Its supply voltage is 3.3 V. As a result, the microphone is biased with 3.3 V to achieve the highest possible sensitivity. With 1 Pa (rms) input, the rms value of the signal generated on the microphone is about 3.2 mV without considering the parasitic capacitance from the preamplifier. To achieve 60dB SNR (not A-weighted), the noise of the preamplifier integrated from 20 Hz to 20 KHz should be no larger than 3.2 μV since the noise from the huge bias resistor has not been considered yet. The value provides a basic guideline when dealing with the noise issue.

With 20 Pa (rms) input, the signal (rms) generated on the microphone is about 64 mV without considering the parasitic capacitance from the preamplifier. If the preamplifier has a rail-to-rail swing, the maximum gain of the preamplifier is about 18X. Due to the fact that the sensitivity on the input will be increased by the feedback capacitor and a rail-to-rail swing is an ideal case, the open loop gain of the preamplifier can only be decided in the design process since it is also related to the input capacitance and the output swing of the preamplifier. With

the chosen value of the gain, the size of the feedback capacitor C_f will not consume too much area as well.

Since the whole system is aiming at audio implementation, the bandwidth of the preamplifier should be larger than 20 KHz. The first pole of the transfer function should be located over 20 KHz since the open loop gain of the preamplifier is used.

3.5 Conclusion

The positive feedback capacitor in DC biasing increases the sensitivity with low bias voltage (compared to the previous design) while the SNR is slightly deteriorated. This principle has the potential to be used to increase the sensitivity of a microphone with large static capacitance or a microphone which is connected to an amplifier with high input parasitic capacitances. In the next chapter the details of this concept will be examined.

Chapter 4. Preamplifier Design

This chapter is about the preamplifier design on transistor level for the DC biasing with positive feedback readout scheme. It includes choosing the topology (section 4.1) and realizing the specifications (section 4.2) which are proposed in chapter 3. After that, the design process of the reference current source used in the biasing circuit is presented (section 4.3). The chapter ends with the detail of the amplifier including size and behavior (section 4.4).

4.1 Amplifier Topology

As has been discussed before the microphone will be biased with the supply voltage, thus we have to find a topology which can sense the positive rail.

Compared to an NMOS input differential amplifier with a current mirror load, the folded-cascode structure has better input common-mode range. Consider the two amplifiers in Figure 4. 1. It shows that the folded-cascode amplifier in Figure 4. 1(b) has a higher input common-mode range. In fact, if V_{SD4} is less than V_{TH}, the positive input common-mode voltage can exceed VDD [27]. Therefore, with an input common-mode level at supply voltage, folded-cascode structure is a good choice.

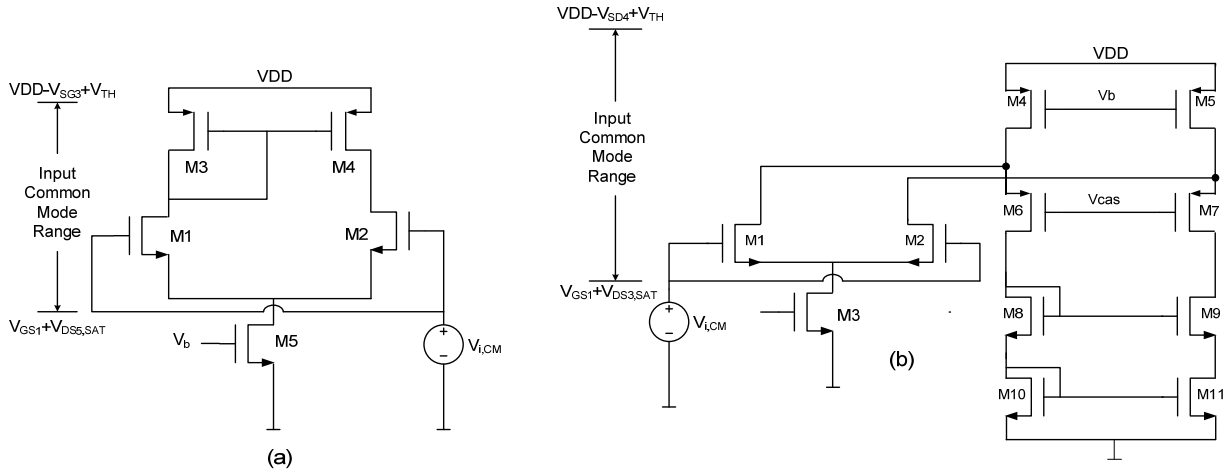

Figure 4. 1 Input common mode range for an NMOS input differential amplifier with (a) a current mirror load (b) folded-cascode with current source load.

In order to get an amplifier with a defined open loop gain, consider the amplifier shown in Figure 4. 2. The inverting input is connected directly to VDD since the common-mode voltage on the non-inverting input is at supply voltage. The input stage is a common source stage with source degeneration resistors. Therefore the equivalent transconductance G_m of the circuit is:

$$G_m \approx \frac{1}{2} \cdot \frac{g_{m1}}{1 + g_{m1} R_1} \qquad (4.\ 1)$$

where g_{m1} is the transconductance of M1.

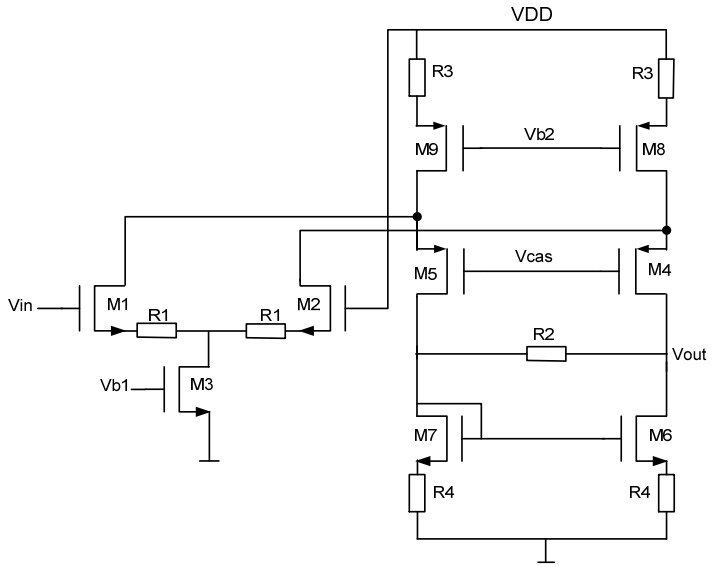

Figure 4. 2 A folded-cascode amplifier.

The equivalent output resistance R_{out} is:

$$R_{out} = R_2 \,||\, r_{o6}(1 + g_{m6}R_4) \,||\, r_{o4}\left(1 + g_{m4}[(r_{o8} + r_{08}g_{m8}R_3) \,||\, (r_{o2} + r_{o2}g_{m2}R_1)]\right) \tag{4. 2}$$

where r_{o6}, r_{o4}, r_{o8} and r_{o2} are the small signal output resistance of M6, M4, M8 and M2 respectively. g_{m4} is the transconductance of M4. If R_2 is much smaller than $r_{o6}(1 + g_{m6}R_4)$ and $r_{o4}\left(1 + g_{m4}[(r_{o8} + r_{08}g_{m8}R_3) \,||\, (r_{o2} + r_{o2}g_{m2}R_1)]\right)$, R_{out} can be simplified as R_2. Therefore, the open loop gain of the circuit is given by:

$$H = \frac{V_{out}}{V_{in}} = G_m R_{out} \approx \frac{1}{2} \cdot \frac{g_{m1}}{1 + g_{m1}R_1} \cdot R_2 = \frac{R_2}{2(\frac{1}{g_{m1}} + R_1)} \tag{4. 3}$$

Equation (4. 3) implies that as R_1 increases, H becomes a weaker function of g_{m1}. The open loop gain is therefore defined by the ratio of R_2 and R_1 and the circuit becomes more linear. The linearization obtained from source degeneration resistor R_1, however, is not good for noise performance because the source degeneration happens at the input device. There are resistors R_3 and R_4 connected to the source of M6~M9 as well. But these resistors help decreasing the 1/*f* noise since they are connected to the load devices. The reason is explained next.

The source degeneration at load rather than the input helps improving the noise performance [28]. Consider the circuit in Figure 4. 3.Sum the noise current at the output:

$$\bar{i}_{out}^{\,2} = g_{m1}^{\,2}\bar{v}_{n,g1}^{\,2} + \left(\frac{g_{m2}}{1+g_{m2}R}\right)^2 \bar{v}_{n,g2}^{\,2} + \left(\frac{R}{R+\frac{1}{g_{m2}}}\right)^2 \bar{i}_R^{\,2} \tag{4. 4}$$

Refer back to the input, yields:

$$\bar{v}_{in}^{\,2} = \frac{\bar{i}_{out}^{\,2}}{g_{m1}^{\,2}} = \bar{v}_{n,g1}^{\,2} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \left(\frac{\bar{v}_{n,g2}^{\,2}}{(1+g_{m2}R)^2} + \frac{4k_BTR}{(1+g_{m2}R)^2}\right) \tag{4. 5}$$

Equation (4. 5) indicates that the source degeneration at load decreases the input referred noise from M2 and R by the factor $(1+g_{m2}R)^2$. Although the thermal noise from R is added, it is decreased by the factor $(1+g_{m2}R)^2$ as well.

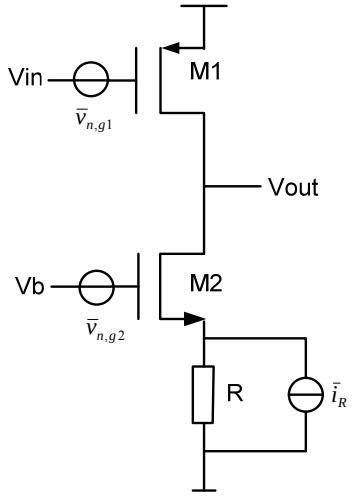

Figure 4. 3 Simple amplifier with source degeneration at load.

Since the source degeneration resistor also contributes thermal noise, the source degeneration at load technique is mainly used for decreasing the 1/f noise.

4.2 Noise Analysis in Folded-Cascode Amplifier

The basic amplifier topology is shown in Figure 4. 4 which utilize the principle about source degeneration explained in section 4.1.2. R_1 aims to improve the linearity while R_3 and R_4 are for the purpose of decreasing 1/*f* noise.

The basic rules in noise analysis in amplifiers are [28]:

- Devices in the signal path are important.
- The noise in the tail current source of the differential input pair can be neglected by symmetry and matching.
- Sum the noise current at the output.

Although the input stage is not differential which means the tail current source will contribute noise, it is not included in the following calculations for simplicity consideration. Sum the noise current at output:

$$\begin{aligned}\bar{i}_o^{\,2} &= G_{m1}^{\,2}\bar{v}_{n,g1}^{\,2} + G_{m2}^{\,2}\bar{v}_{n,g2}^{\,2} + G_{m8}^{\,2}\bar{v}_{n,g8}^{\,2} + G_{m9}^{\,2}\bar{v}_{n,g9}^{\,2} + G_{m4}^{\,2}\bar{v}_{n,g4}^{\,2} + G_{m5}^{\,2}\bar{v}_{n,g5}^{\,2} \\ &+ G_{m6}^{\,2}\bar{v}_{n,g6}^{\,2} + G_{m7}^{\,2}\bar{v}_{n,g7}^{\,2} + 2K_4^{\,2}\bar{i}_{R_4}^{\,2} + 2K_3^{\,2}\bar{i}_{R_3}^{\,2} + 2K_1^{\,2}\bar{i}_{R1}^{\,2}\end{aligned} \tag{4. 6}$$

where

$$G_{m1} = G_{m2} = \frac{g_{m1}}{1+g_{m1}R_1}; G_{m8} = G_{m9} = \frac{g_{m8}}{1+g_{m8}R_3}; G_{m6} = G_{m7} = \frac{g_{m6}}{1+g_{m6}R_4};$$

$$G_{m4} = G_{m5} = \frac{g_{m4}}{1+g_{m4}r_{o4}\left(r_{o2}(1+g_{m2}R_1) \,||\, r_{o8}(1+g_{m8}R_3)\right)};$$

$$K_4 = \frac{R_3}{R_3 + \dfrac{1}{g_{m8}}}; K_3 = \frac{R_4}{R_4 + \dfrac{1}{g_{m6}}}; K_1 = \frac{R_1}{R_1 + \dfrac{1}{g_{m1}}};$$

Considering matching and symmetry,

$$\bar{i}_o^{\,2} = 2*(G_{m1}^{\,2}\bar{v}_{n,g1}^{\,2} + G_{m8}^{\,2}\bar{v}_{n,g8}^{\,2} + G_{m4}^{\,2}\bar{v}_{n,g4}^{\,2} + G_{m6}^{\,2}\bar{v}_{n,g6}^{\,2} + K_4^{\,2}\bar{i}_{R4}^{\,2} + K_1^{\,2}\bar{i}_{R1}^{\,2} + K_3^{\,2}\bar{i}_{R3}^{\,2}) \tag{4. 7}$$

Since the denominator of G_{m4} and G_{m5} usually have 6 orders of magnitude, the noise from cascode transistor M4 and M5 can be neglected. Then refer the output noise current back to the input, we get:

$$\bar{v}_{n,in}^{\,2} = \frac{\bar{i}_o^{\,2}}{G_{m1}^{\,2}} = 2*(\bar{v}_{n,g1}^{\,2} + \frac{G_{m8}^{\,2}}{G_{m1}^{\,2}}\bar{v}_{n,g8}^{\,2} + \frac{G_{m6}^{\,2}}{G_{m1}^{\,2}}\bar{v}_{n,g6}^{\,2} + \frac{K_4^{\,2}}{G_{m1}^{\,2}}\bar{i}_{R4}^{\,2} + \frac{K_1^{\,2}}{G_{m1}^{\,2}}\bar{i}_{R1}^{\,2} + \frac{K_3^{\,2}}{G_{m1}^{\,2}}\bar{i}_{R3}^{\,2}) \tag{4. 8}$$

Since the source degeneration resistors are aiming to decrease the 1/*f* noise, the following noise analysis will only concentrate on the flicker noise.

The flicker noise voltage referred to the gate of a MOSFET is [27]:

$$\bar{v}_{n,g}^{\,2} = \frac{KF}{2\mu C_{ox}^{\,2} WLf} \tag{4. 9}$$

where KF is the flicker noise coefficient and C_{ox} is the capacitance per unit area of the gate oxide.
Substitute equation (4. 9) into (4. 8), we get:

$$\bar{v}_{n,in}^{\,2}(1/f) = \frac{KF_n}{\mu_n C_{ox}^{\,2} W_1 L_1 f}\left[1 + \left(\frac{1+g_{m1}R_1}{1+g_{m8}R_3}\right)^2 \frac{2KF_p}{KF_n}\left(\frac{L_1}{L_8}\right)^2 + \left(\frac{1+g_{m1}R_1}{1+g_{m6}R_4}\right)^2\left(\frac{L_1}{L_6}\right)^2\right] \tag{4. 10}$$

Equation (4. 10) implies the rules for good 1/*f* design in folded-cascode amplifiers:

- Make L_8 and L_6 larger than L_1.
- Increase W_1 , L_8 or L_6 will decrease $1/f$ noise.

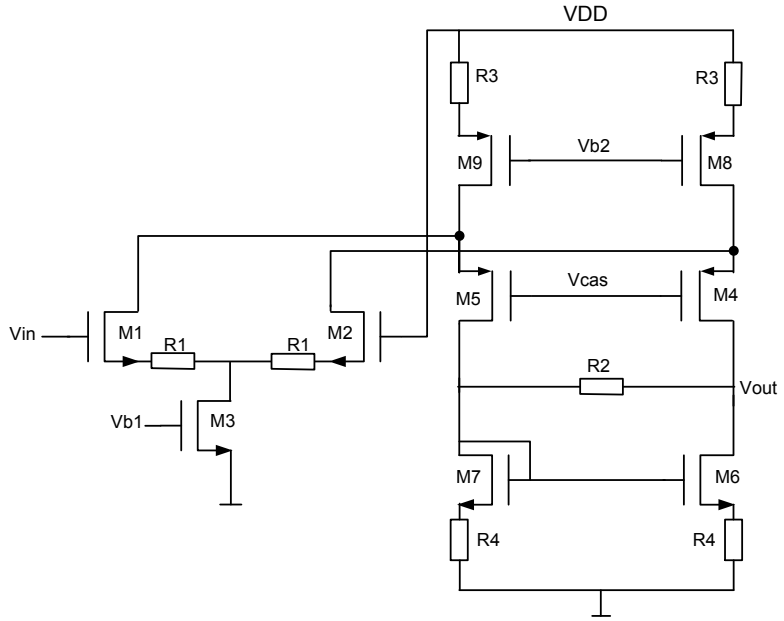

Figure 4. 4 The basic topology of the preamplifier.

$g_{m8}R_3$ and $g_{m6}R_4$ are not necessarily larger than $g_{m1}R_1$ because the existence of these factors has already decreased the $1/f$ noise. But it is beneficial to make them large for decreasing the noise more. So these two factors have to be maximized. If M8 is in saturation region, $g_{m8}R_3$ is given by:

$$g_{m8}R_3 = \mu_p C_{ox}\frac{W_8}{L_8}(VDD - I_8R_3 - V_{b2} - V_{TH})R_3 \tag{4. 11}$$

The equation shows that if W_8/L_8 and I_8 are fixed, the product of g_{m8} and R_3 is a quadratic function of R_3. Therefore, R_3 can be optimized to get better noise performance. Write equation (4. 11) into a standard form of a quadratic function yields:

$$g_{m8}R_3 = \mu_p C_{ox}\frac{W_8}{L_8}\left(R_3 - \frac{VDD - V_{b2} - V_{TH}}{2I_8}\right)^2 + \mu_p C_{ox}\frac{W_8}{L_8}\frac{(VDD - V_{b2} - V_{TH})^2}{4{I_8}^2} \tag{4. 12}$$

Thus the maximum value of $g_{m8}R_3$ is $\mu_p C_{ox}\frac{W_8}{L_8}\frac{(VDD - V_{b2} - V_{TH})^2}{4I_8}$ when R_3 is equal to $\frac{VDD - V_{b2} - V_{TH}}{2I_8}$. The same principle can be applied to the product of g_{m6} and R_4 which yields the maximum value of $g_{m6}R_4$ is $\mu_n C_{ox}\frac{W_6}{L_6}\frac{(V_{out} - V_{TH})^2}{8I_8}$ when R_4 is $\frac{V_{out} - V_{TH}}{2I_8}$. Attention has to be taken when choosing the value of R_3 since it is possible to drive M8 out of the saturation region and equation (4. 11) is not true any more.

The noise analysis in this section provides a basic guideline about choosing the size of the transistors and resistors. The next section will explain the principle of the reference current source used in the biasing circuit for the amplifier.

4.3 Reference Current Source

In a normal biasing circuit, a current source is required. Consider the circuit in Figure 4. 5(a). It is based on the technique called bootstrap reference. "If the voltage across the active device is used to create a current and this current is somehow used to provide the original current through the device, then a current or voltage will be obtained that is for all practical purposes independent of VDD. This technique is called as a bootstrap reference."[27]

M1, M3 and M6 causes the current I_1, I_2 and I_5 to be equal. I_2 flowing through M2 generates V_{GS2} which is equal to the voltage created by I_1 flowing though R_2. Since V_{GS2} is equal to I_1*R_2, an equilibrium is set up which is illustrated Figure 4. 5(b). I_2 and V_{GS2} are decided by the I-V characteristic of M2 under different temperature to find a temperature-independent V_{GS} and drain current I_D which is indicated as V_Q and I_Q in Figure 4. 5(b). Then R_2 is derived by V_Q/I_Q to make the two I-V characteristic curves cross at the temperature independent point Q. The equilibrium point is given as:

$$I_1 R_2 = V_{GS2} = V_{TH} + \sqrt{\frac{2I_1}{\beta_1}} \tag{4. 13}$$

where β_1 is $\mu C_{ox} \frac{W_1}{L_1}$. The equation can be solved for $I_1=I_2=I_Q$, giving:

$$I_Q = I_2 = \frac{V_{TH}}{R_2} + \frac{1}{\beta_1 R_2^{\,2}} + \frac{1}{R_2}\sqrt{\frac{2V_{TH}}{\beta_1 R_2} + \frac{1}{\beta_1^{\,2} R_2^{\,2}}} \tag{4. 14}$$

Equation (4. 14) indicates that I_1 and I_2 can be regarded as insensitive to VDD in first order. And since the equilibrium point is also temperature independent, I_1 and I_2 can be regarded as insensitive to temperature as well.

Figure 4. 5(b) shows that there are two equilibrium points. One is at Q and the other is at the origin. Therefore a start up circuit is necessary to avoid the circuit being biased in the wrong equilibrium point. The circuit within the dotted box in Figure 4. 5(a) functions as a start up circuit. If the circuit works at the undesired point, there will be no current flowing through R_2 and M2. The gate of the M5 and M8 are pulled down to zero. Consequently, the drain of M8 is pulled up and inverted at the gate of PMOS M7. Thus M7 is turned on and leaks current into M2 and charge the gate of M5 and M8. This causes the current to snap to the desired state. At the same time, the drain of M8 is pulled down and the gate voltage of M7 is increased to VDD by the inverter. Then M7 is turned off and the whole circuit starts to work in the desired equilibrium point.

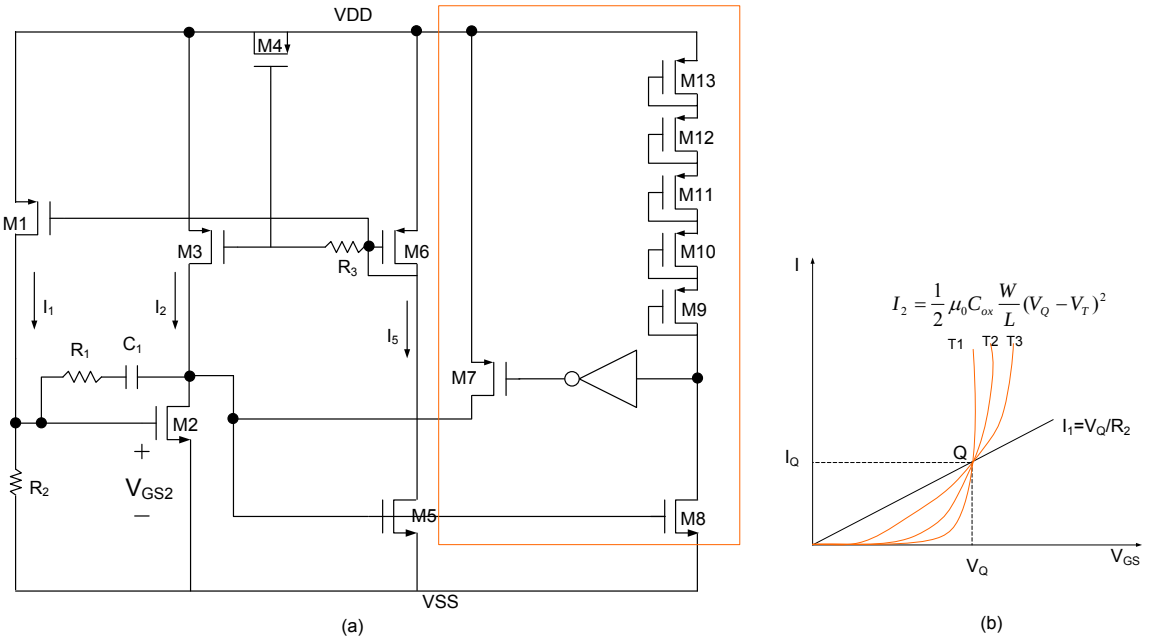

Figure 4. 5 (a) Bootstrap current source. (b) I-V characteristic curves of R_2 and M2.

Power and noise are the two basic considerations of this current source design. The following guidelines are used to save power and reduce noise. The current flowing in I_1, I_2 and I_5 branches are summed up and then provide part of the tail current of the differential input pair without wasting them. Thus the sources of M1, M3 and M6 will not be connected to VDD anymore. Current mirror is very often used in biasing circuit. The aspect ratio of the MOSFET in current mirror decides the ratio of the current amplification. If we want to supply current to M8 and M9 in Figure 4. 4 by PMOS current mirror, the ratio of the current amplification needs to be optimized because large amplification ratio will introduce more noise while small amplification ratio will waste power in the biasing circuit.

Stability is another concern in the current source. The current mirror forms a positive feedback and a negative feedback at the same time which is shown in Figure 4. 6. The inverting amplifier which is labeled as 1 is composed of M5 and M6 in common-source structure with M5 as input and M6 as load. M1 and R_2 forms amplifier 2 with M1 as input and R_2 as load. M2 and M3 makes up the third amplifier with M2 as input and M3 as load. And amplifier 4 is composed of M2 and M3 as well but with M3 as input and M2 as load. Therefore, amplifier 1 and amplifier 4 form a positive feedback and amplifier 1, 2 and 3 form a negative feedback. R_1 and C_1 therefore are for the purpose of compensation in a two-stage amplifier. R_3 and M4 forms a RC filter to attenuate the positive feedback. They are all aiming to stabilize the circuit.

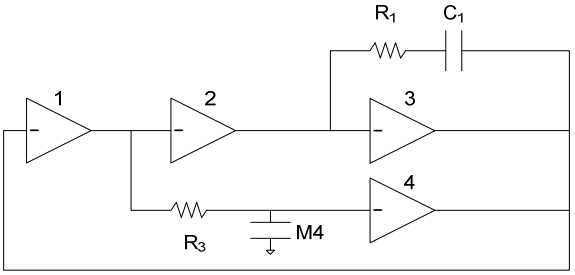

Figure 4. 6 Equivalent model for bootstrap current source.

4.4 Size of the Devices in the Preamplifier

The CMOS technology which will be used in this design is CMOS014 from NXP Semiconductors. The minimum width and length of first priority level is 0.768 and 0.16 respectively. The preamplifier and its biasing scheme are shown in Figure 4. 7. The size of the devices is listed in Table 4. 1.

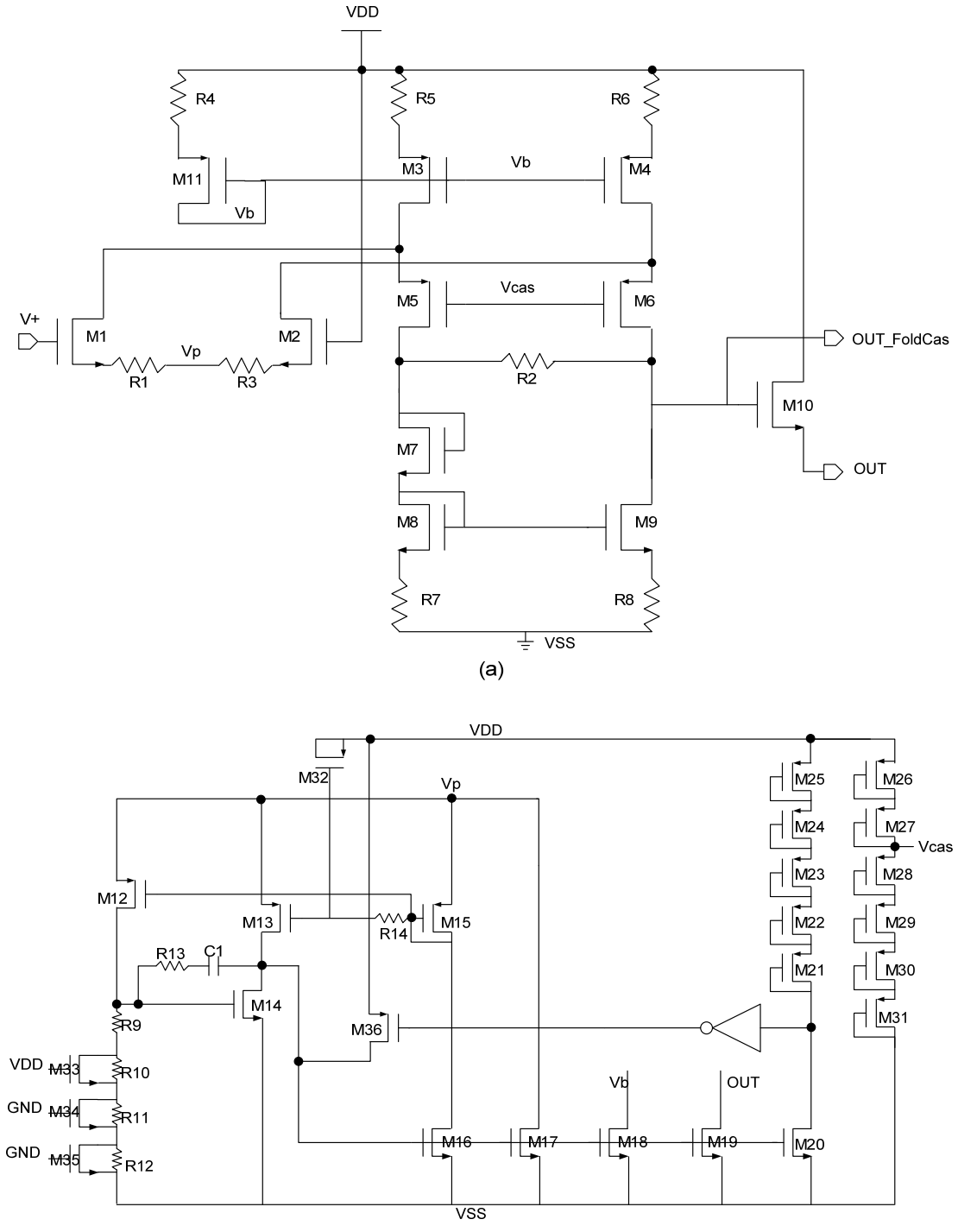

Figure 4. 7 (a) Schematic of preamplifier. (b) Biasing schematic.

Transistor	W(μm)/L(μm)	I_D(μA)	g_m(μS)	r_{out} (Ω)
M1, M2	1000/0.48	50	1569	85.9 K
M3, M4,	600/5	100	973	107K
M5, M6	500/0.32	50	1222	241 K
M7	150/12	50	499	3.242 M
M8, M9	150/12	50	492	3.3 M
M10	1000/1	10	308	1.9 M
M11	600/5	100	982	1.11 M
M12, M13, M15	60/10	10	72	26.5 M
M14, M16, M19	10/9	10	67	17 M
M17	70/9	70	472	2.54 M
M18	100/9	100	675	1.77 M
M20	10/9	6	29	20.9 K
M21 ~ M25	10/1	6	69	5.5 M
M26 ~ M31	10/1	2	30	17 M
M32	40/20	0	N/A	N/A
M33 ~ M35	20/0.16	N/A	N/A	N/A
M36	10/0.18	N/A	N/A	N/A
Resistor	Resistance (Ω)			
R1, R3	1 K			
R2	40 K			
R4 ~ R6	4 K			
R7, R8	500			
R9 ~ R12	39 K			
R13	20 K			
R14	100 K			
Capacitor	Capacitance (F)			
C1	12 p			

Table 4. 1 Size of the devices.

The values listed in the above table agree with the noise design guideline derived from section 4.2. For instance, the length of M3, M4 and M7~M9 are all larger than that of the input pair. The product of g_{m4} and R_6 is larger than $g_{m1}R_1$.

There are several notes about the circuit as follows:

- A source follower buffer is connected after the preamplifier for the ability of loading large capacitor.
- M7 is aiming to increase the common mode voltage at the output of the folded-cascode amplifier.
- M3, M4 are with the same size as M11. Otherwise, the noise from current source will be amplified if the aspect ratio of M3 and M4 are several times larger than that of M11.
- The bias voltage V_{cas} for M5 and M6 are generated from a series of PMOS diodes.
- The NMOS switch M33 ~ M35 are for the purpose of making the current source programmable.

Table 4. 2 lists some specifications of the preamplifier:

Specification	**Value**	**Unit**
Unity Gain Bandwidth	4.622	MHz
Current Consumption	320	uA
Phase Shift @ 20KHz	1.33	degree
Common-mode Voltage @ Folded-Cascode Output	1.53	V
Common-mode Voltage @ Buffer Output	0.9	V
Maximum Swing @ Output	1.7	V (peak-to-peak)
Corner Frequency	7	KHz

Table 4. 2 Specifications for the preamplifier

Next chapter will move to the discussion on applying this preamplifier to the DC biasing readout with positive feedback.

Chapter 5. System Implementation

With the preamplifier in hand, we can apply it to the readout scheme of DC biasing with positive feedback to check its performance. The parasitic capacitance of the preamplifier is found out in section 5.1. It decides the size of the feedback capacitor. After that, the stability is checked by AC simulation due to the fact that positive feedback may introduce oscillation (section 5.2). Finally, the chosen capacitor is designed to be programmable and the resulting problems are explained and solved afterwards (section 5.3).

5.1 Parasitic Capacitance

Figure 3. 3 implies that if the negative capacitance introduced from the Miller effect of C_f is quite close to the value of $C_{mic}+C_p$, the SNR will drop abruptly. Therefore the optimal value of C_f can only be decided after knowing the value of $C_{mic}+C_p$. Since C_{mic} has been defined in equation (1. 1) which yields 2.94 pF and the parasitic capacitance C_{p1} of the microphone itself is about 0.7 pF, the only value which has to be found out is the input parasitic capacitance of the preamplifier.

The input capacitance in found by putting an AC current source at the input which is shown in Figure 5. 1.

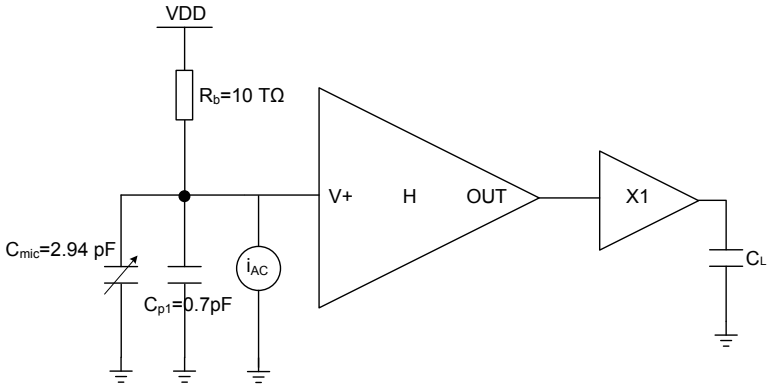

Figure 5. 1 The scheme to decide the input capacitance of the preamplifier

Therefore, the magnitude of the AC voltage V_{AC} at the input of the preamplifier is $i_{AC}*(R_b||\frac{1}{j\omega(C_{mic}+C_{p1}+C_{pin})})$. If the magnitude of i_{AC} is 1, the input capacitance C_{pin} of the preamplifier is:

$$C_{pin}=\frac{1}{j\omega R_b}\left(\frac{R_b}{V_{AC}}-1\right)-C_{mic}-C_{p1} \tag{5. 1}$$

The AC simulation shows that V_{AC} is 1.729 MV at 20 KHz. Therefore, the C_{pin} can be calculated as 0.96 pF. Thus the total parasitic capacitance at the input is $C_{mic}+C_{p1}+C_{pin}$ = 4.6 pF.

Given the total parasitic capacitance at the input, the amplitude of the signal generated on the microphone under 20 Pa (rms) can be calculated as 72.7 mV. Since the swing at the output of the preamplifier is 1.7 V, the open loop gain of the preamplifier is thus defined as 11X. In this case, the signal at the output of the preamplifier will not be clipped with 20 Pa (rms) sound pressures. When the positive feedback theory is adopted, the signal at the output will start to clip. Since a sound pressure of 20 Pa can cause hearing damage, using positive feedback theory under 20 Pa sound is not considered.

5.2 Stability Check by AC Simulation

Figure 5. 2 is the AC simulation for testing stability. The huge inductor (1 TH) here is to keep DC signal go through and block AC signal. The huge capacitor (1 F) here is to block DC and make AC signal go through easily. The capacitor which is connected to the diode-connected PMOS not only includes the static and parasitic capacitance of the sensor but also includes the input capacitance of the preamplifier for the reason that impedance at point P should be kept the same as the situation when the loop is not broken by the LC network.

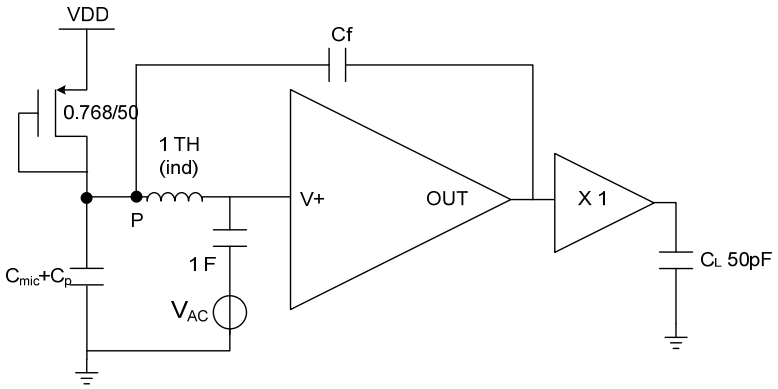

Figure 5. 2 Scheme for loop gain simulation.

Section 3.3.3 indicates that the stable condition is $C_f < \frac{C_{mic}+C_p}{|H-1|}$. Since the value of the total parasitic capacitance is given in section 5.2, an AC simulation is presented to prove the condition. Figure 5. 3 shows that when C_f is larger than 450 fF, the loop gain is larger than 0 dB. In this situation, the positive feedback will be positively added to the input signal, amplified afterwards and added to the input again. This will finally cause the system into oscillation. Therefore, for stability concern, the maximum value of C_f should be kept under 450 fF. The result agrees to the stable condition revealed in section 3.3.3. Figure 5. 3 shows the loop gain with C_f = 450fF and C_f = 600 fF.

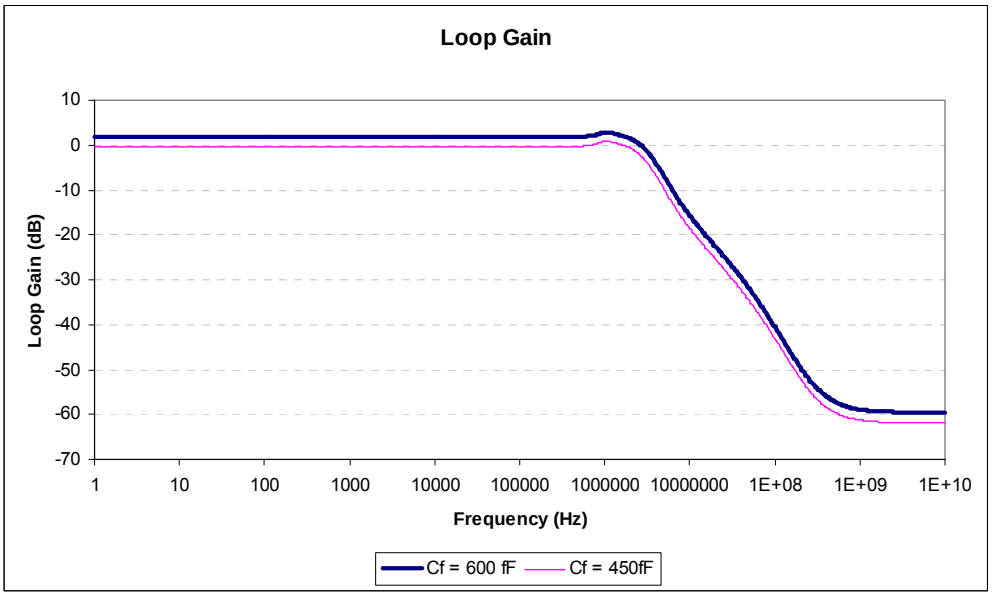

Figure 5. 3 AC simulation for Loop Gain with two different C_f.

With C_f = 450 fF, the loop gain crosses the 0 dB at high frequency. It might be caused by the inaccuracy of the calculation of the input parasitic capacitance of the preamplifier. Therefore a transient simulation has to be done to make sure the stability of the system with 450 fF C_f. It will be described later.

5.3 Programmable C_f

Since we are aiming at making a test chip, it is interesting to know how the circuit performs with different C_f. Section 5.2 indicates that C_f should be smaller than 450 fF to keep the circuit stable. Therefore the 450 fF C_f can be divided into a 4-bit DAC (Digital-to-Analog Converter) to be programmable. It results in LSB (Least Significant Bit) as 30 fF. Since the sensitivity of the microphone is increased less than 1 dB with 30 fF C_f, it is not necessary to divided C_f into more bits. The readout scheme with 4-bit DAC is shown in Figure 5. 4.

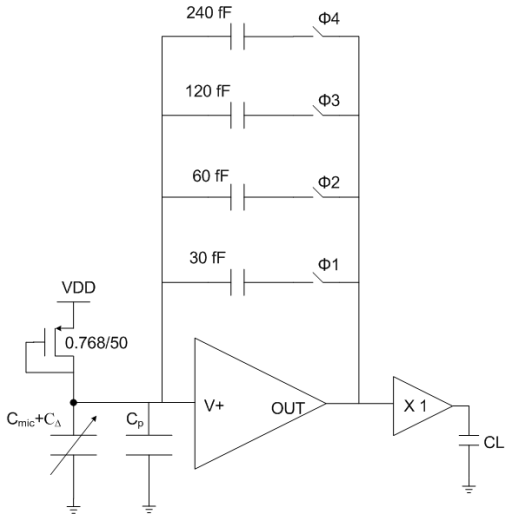

Figure 5. 4 Readout scheme with 4-bit DAC.

The type of the capacitor used in the DAC is of Nploy-Nwell type. Its cross section is shown in Figure 5. 5(a).

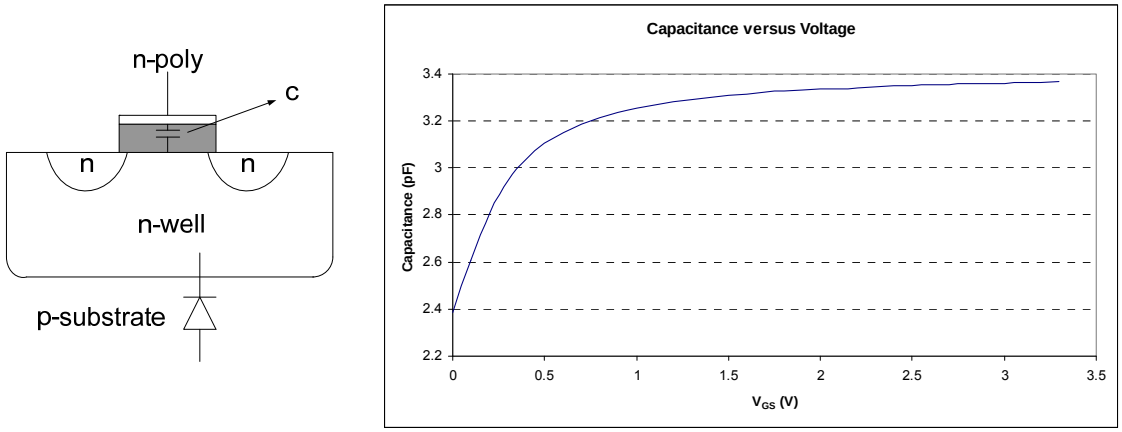

Figure 5. 5 Cross section of a Npoly-Nwell capacitor.

The capacitance of an Nwell-Npoly type capacitor is close to its nominal value when the voltage between the poly and Nwell is large. A plot of the capacitance of a 3.342 pF capacitor with different voltage exerted on its two terminals is shown in Figure 5. 5(b). In this design, the input common-mode voltage is 3.3 V and the common-mode voltage at the output is 1.53 V which yields a 1.77 voltage difference. With this voltage, the actual value of the capacitor is close to its nominal value.

The common mode voltage at the output is close to the middle of the rail, thus a transmission gate type switch is suitable. And the switches can only be put at the output side of the circuit; otherwise the diffusion diodes of these switches will cause problem on microphone biasing. The current will leak through these diodes and the charge accumulated on microphone can not be considered as constant.

The switches labeled as Φ_1, Φ_2, Φ_3 and Φ_4 are composed of the smallest size PMOS and NMOS in parallel to achieve high OFF resistance. Figure 5. 6 shows the schematic of the switch. Therefore, when the drive voltage is at supply, the switch is on and when the drive voltage is at ground, the switch is off. When the switches are off, the thermal noise of their huge OFF resistance will be filtered by the capacitor in the DAC and contribute noise at the same time. As a result, the OFF resistance should be large. Moreover, the finite OFF resistance of these switches gives rise to oscillation problems as well.

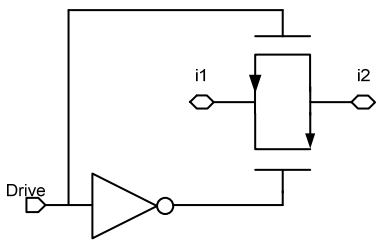

Figure 5. 6 Transmission Gate

Consider the circuit in Figure 5. 7(a). An extra C_f of value 420 fF capacitor is connected in parallel with the DAC. The switches labeled with Φ_1, Φ_2, Φ_3 and Φ_4 are off and Φ_5 is on. In

this case, the equivalent feedback capacitor is 420 fF which is supposed to be in the stable region (It has been tested with a single 420 fF C_f connected from input to output of the preamplifier). The transient simulation result, however, shows that the circuit begins to oscillate at a slow frequency (about 2.2 Hz) which is shown in Figure 5. 7(b).

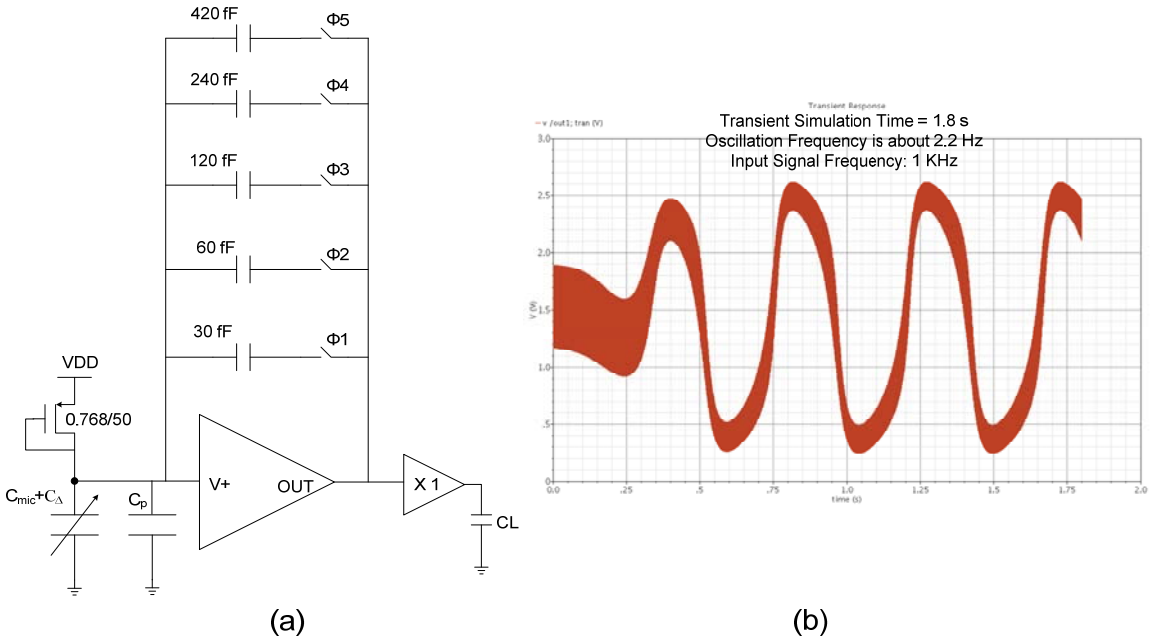

Figure 5. 7 (a) The scheme of unstable situation. (b) Oscillation waveform.

The finite OFF resistance of the switch causes the problem. The system is more stable with a smaller absolute value of the feedback transfer function β(s) which is given in equation (3. 7) .With a given Z_{in}, the system is more stable with a larger Z_f. When the switch in the DAC is off, the equivalent feedback impedance is $R_{off} + \frac{1}{j\omega C_f}$ (R_{off} is the OFF resistance of the switch). Since there are 4 paths in the DAC which have been switched off in Figure 5. 7(a), the equivalent impedance of the Z_f is approximately a quarter of $R_{off} + \frac{1}{j\omega C_f}$ in parallel with the 420fF C_f. The exact impedance of Z_f is smaller than we expected which indicates the feedback factor is larger than what it should be. Since 420 fF is close to the edge of oscillation, with the effect mentioned above, it has possibility to drive the circuit into unstable status.

For this reason, the finite OFF resistance of the switches are not supposed to affect the equivalent impedance of Z_f. The solution is adding extra switches to ground which are labeled as Φ_1', Φ_2', Φ_3' and Φ_4' in Figure 5. 8. The drive signals on the added switches are coming from the AND gate with 'ctrl' and the inversion of Φ_1, Φ_2, Φ_3 and Φ_4 as inputs. The 'ctrl' signal is for the purpose of testing the function of the final chip when the switches to ground are not there. In this way, when Φ_i (i is integers from 1 to 4) is off its off resistance is not in the feedback path which will not affect the impedance of the feedback.

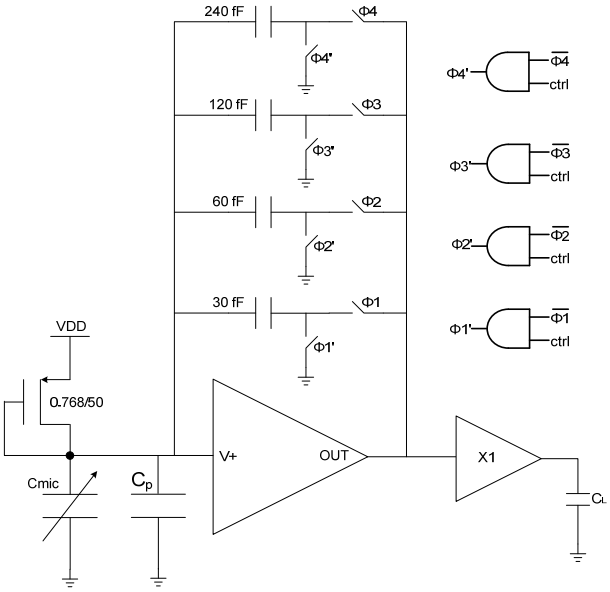

Figure 5. 8 4-bit DAC with switches to ground.

5.4 Conclusion

During the process of applying a programmable C_f into the DC biasing with positive feedback scheme, we found the hidden dangerous of oscillation. It is solved by using extra switches to ground. Next chapter is about the simulation results of the system to check if it meets the specifications.

Chapter 6. Simulation Result

In this chapter, the simulation results are given to check whether the system has met the specifications or not. It starts with a transient simulation to prove the stability with the maximum capacitor (section 6.1). After that the SNR and THD results with different value of C_f are presented in section 6.2 and 6.3 respectively. Section 6.4 proves the result of sensitivity increase. Before putting the circuit into CMOS fabrication, the performance of the system with different temperature and different process variances has to be checked (section 6.5 and 6.6). This chapter ends with the comparison between this design and the other designs.

6.1 Stability Check by Transient Simulation

The AC simulation in Figure 5. 3 shows that the loop gain curve crosses 0 dB with C_f = 450 fF at high frequencies. To make sure that this value is still in the stable region, a transient simulation can be made to check if it oscillates or not. The setup for simulating impulse response is shown in Figure 6. 1. A current pulse with 1us width and 5 uA amplitude is put at the input.

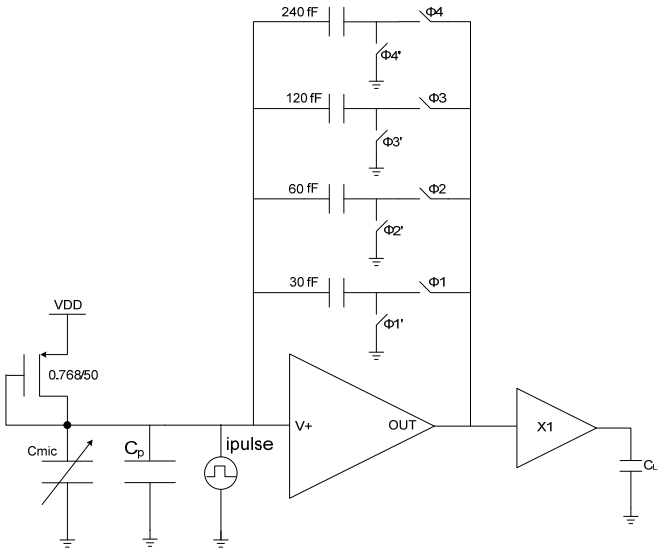

Figure 6. 1 Scheme for simulating impulse response

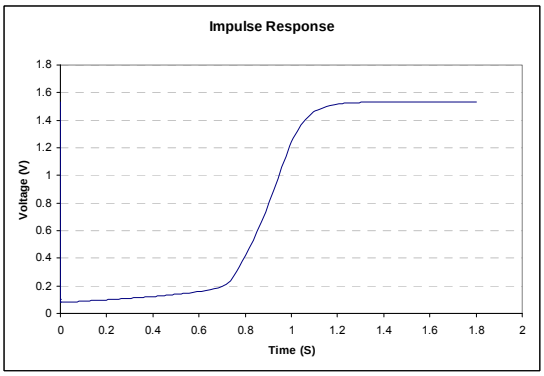

Figure 6. 2 Impulse response.

The impulse response at the output of the folded-cascode amplifier is shown in Figure 6. 2 without the input of a sound signal. The plot shows that the common-mode voltage at the output needs about 1.3 second to settle down which proves that the system with 450 fF feedback is still in the stable region.

With 390fF feedback capacitor and 1Pa, 1 KHz input, the signal at the output of the buffer is shown in Figure 6. 3. The small ramp up in the beginning is coming from circuit settling. The zoom-in figure shows that most nonlinearities of the signal come from second-order harmonics since the upper half wave's amplitude is larger than that of the lower half. The reason is that the preamplifier is not differential since normally a differential amplifier can reduce the even-order harmonics.

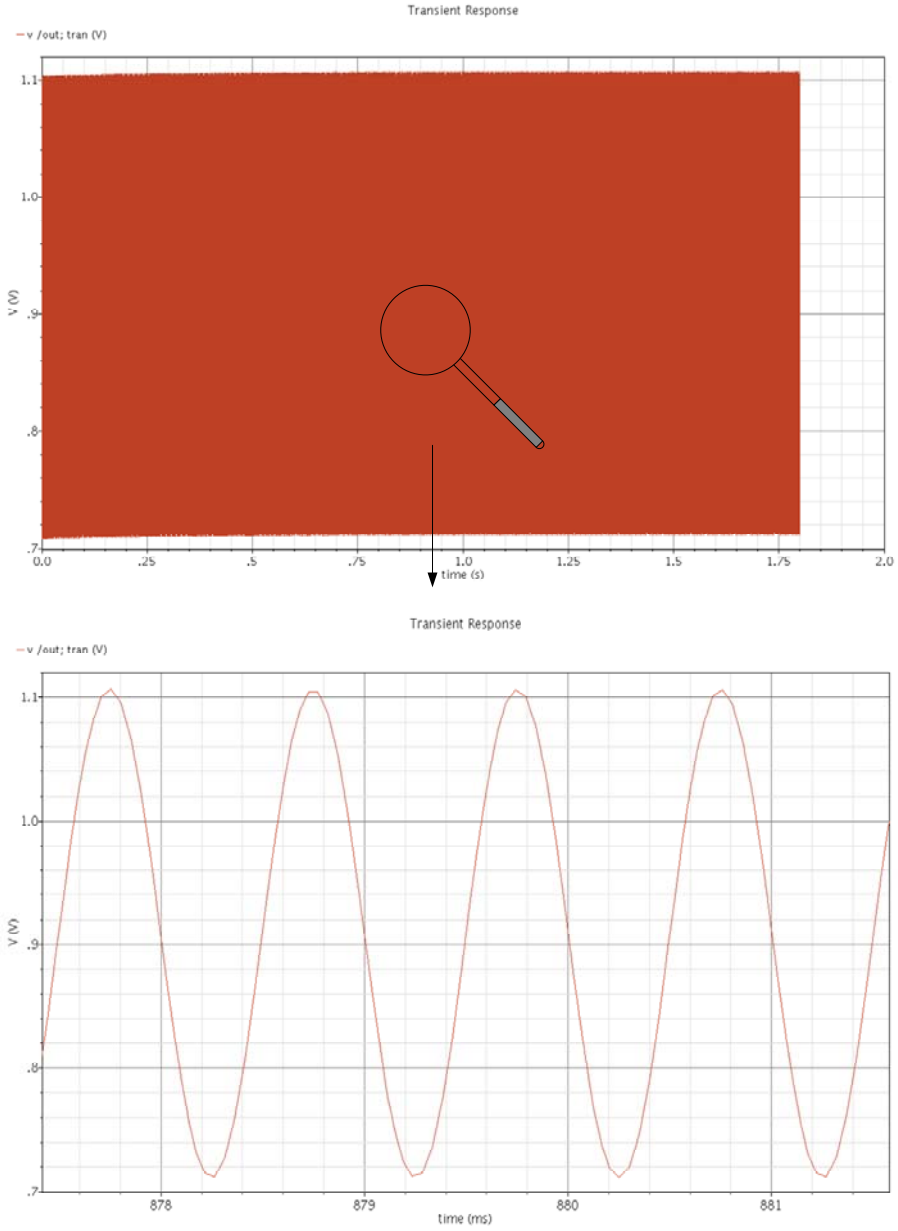

Figure 6. 3 Transient simulation result with C_f = 390 fF.

6.2 Signal-to-Noise Ratio

The SNR at the output of the buffer with different C_f is shown in Figure 6. 4. The rms value of the noise is achieved by multiplying the noise power spectrum with A-weighting transfer function (equation (1. 11)) and then integrates it from 20 Hz to 20 KHz. It is simulated under room temperature 27°C. The curve shows that SNR is decreased slightly with increasing C_f. When C_f is 420 fF, SNR is 0.6 dB less than the case without C_f. But this value (60.47 dB) still meets the specification.

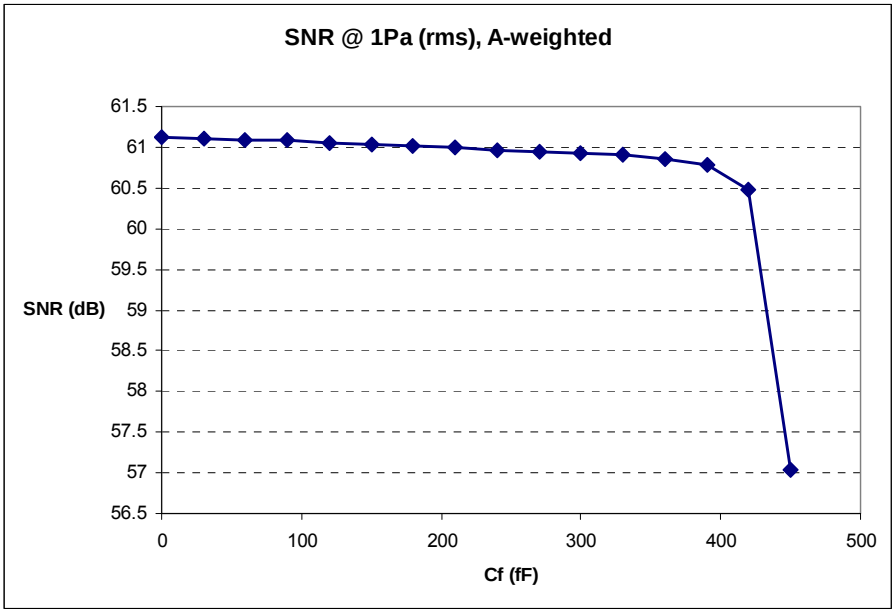

Figure 6. 4 SNR versus C_f (all available value of DAC)

6.3 Total Harmonic Distortion

"Total Harmonic Distortion (THD) is quantified by summing the power of all of the harmonics (except that of the fundamental) and normalizing the result to the power of the fundamental" [29]. With an input signal of frequency ω, the signal y(t) at the output of a nonlinear system can be approximated by Taylor expansion:

$$y(t) = A_1 \cos \omega t + A_2 \cos(2\omega t) + A_3 \cos(3\omega t) + \ldots \quad (6.\ 1)$$

For up to third-order harmonics nonlinearity, the Total Harmonic Distortion (THD) is:

$$THD = \frac{\sqrt{A_2^{\ 2} + A_3^{\ 2}}}{A_1} \cdot 100\% \quad (6.\ 2)$$

The calculation of THD in this design includes up to 12th-order harmonics. It is based on a 94dBSPL input signal with 1 KHz frequency. Figure 6. 5 shows the THD at the output of the buffer with different C_f. THD specification at 94dBSPL is 0.5%. From this curve, it can be seen that THD still meets the specification when C_f is equal to 390 fF.

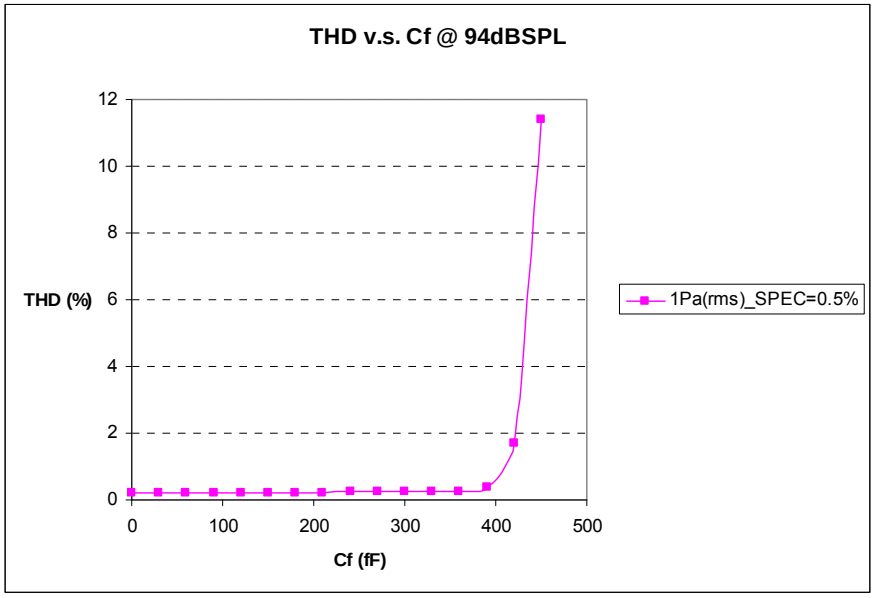

Figure 6. 5 THD versus different C_f. (all available value of DAC)

It is noteworthy to find that the linearity is quite bad when feedback capacitor C_f almost cancels all the parasitic capacitance at the input (450fF). The reason has been mentioned in section 2.2 already. Applying the same theory yields:

$$\Delta V = H \cdot \frac{C_\Delta \cdot V_{ref}}{\left(C_{mic} + C_p + (1-H)C_f\right) \cdot \left(1 - \frac{C_\Delta}{C_{mic} + C_p + (1-H)C_f}\right)} \quad [V] \qquad (6.\ 3)$$

In this case, the nonlinear factor $\frac{C_\Delta}{C_{mic} + C_p + (1-H)C_f}$ in the denominator of equation (6. 3) increases with increasing C_f. Thus the linearity is worsened. And the preamplifier connected afterwards also contributes some nonlinearity.

6.4 Sensitivity

Since the purpose of this design is to increase the sensitivity of the microphone, it is interesting to know how much sensitivity the positive feedback capacitor C_f has increased. Figure 6. 6 shows the signal level (dB) at the input of the preamplifier by sweeping C_f in DAC. It indicates that the sensitivity can be increased by 17 dB when C_f is 390 fF(The system still meets the SNR and THD specification with this value of C_f which are shown in Figure 6. 4and Figure 6. 5).

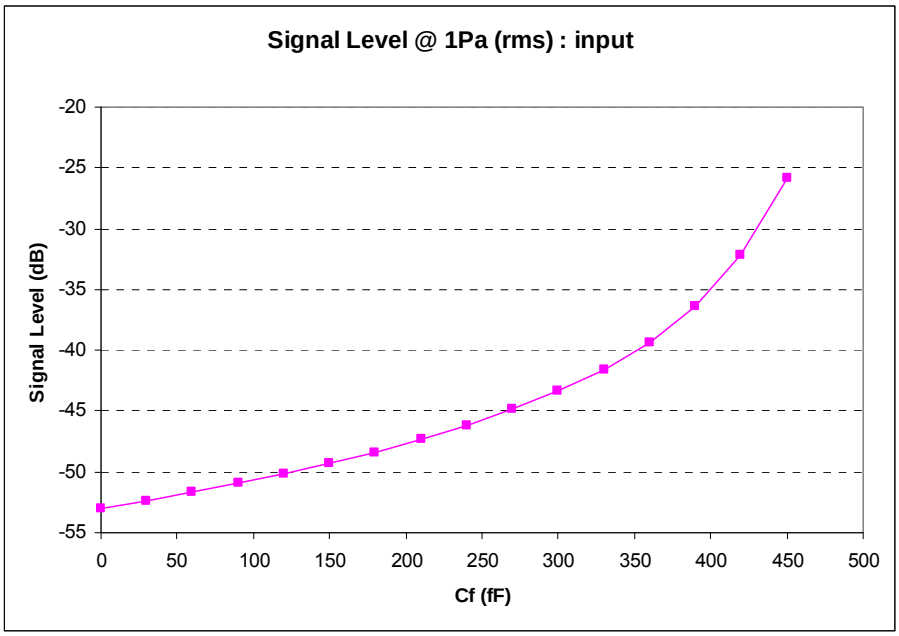

Figure 6. 6 Signal Level versus different C_f.

From the simulation results in section 6.2 to 6.4, the maximum C_f which can be used in DC biasing with positive feedback is about 390 fF because the system still meets the specification with this value of C_f. This value, however, has to be checked with process and mismatch variations to guarantee a chip with high yield.

6.5 Process Corners Simulation

Process corner simulation is the base of the yield because the characteristic of MOSFETs' variance with different chip and batches are usually big [29].The process corners include "Fast NMOS and Fast PMOS(fnfp)", "Fast NMOS and Slow PMOS (fnsp)", "Slow NMOS and Slow PMOS (snsp)" and "Slow NMOS and Fast MOS (snfp)". The following simulation will only consider the "nominal", "fnfp" and "snsp" corners.

6.5.1 Corner Simulation without C_f

Figure 6. 7 shows the corner simulation when there is no C_f. Only three temperature conditions are simulated with 3.3 V supply voltage. They are -40°C, 27°C and 120°C. It is evident that the circuit does not behave well at high temperatures. The reduction of SNR at high temperature comes from the diode-connected PMOS which is mentioned in section 5.1. The impedance of the diode drops from 7.8 TΩ at 27°C to 63 GΩ at 120°C. Another reason for the SNR reduction is that the thermal noise voltage is proportional to the square root of temperature.

Figure 6. 7 also indicates that "fnfp" corner behaves the worst compared to the other two corners. Since "fnfp" corner usually has higher transconductance than the "nominal" corner, the equivalent impedance of the diode-connected PMOS is lower. As a result, SNR is deteriorated. If we sweep the temperature from 30°C to 70°C with "fnfp" corner, the SNR meets the specification when the temperature is lower than 55°C.

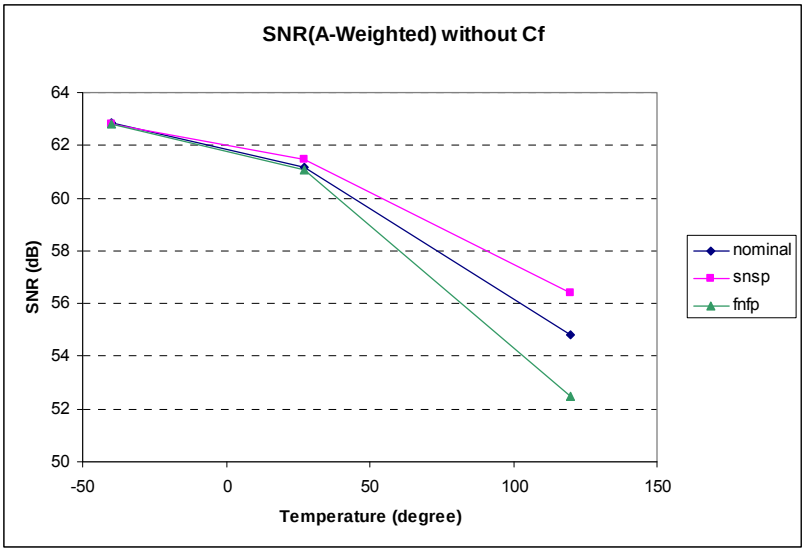

Figure 6. 7 Corner simulation for SNR when there is no C_f.

Figure 6. 8 shows the corner simulation of THD without C_f. Although the THD of "fnfp" corner at high temperature exceeds the other two corners, they all meet the THD specification which is 0.5% at 94dBSPL input.

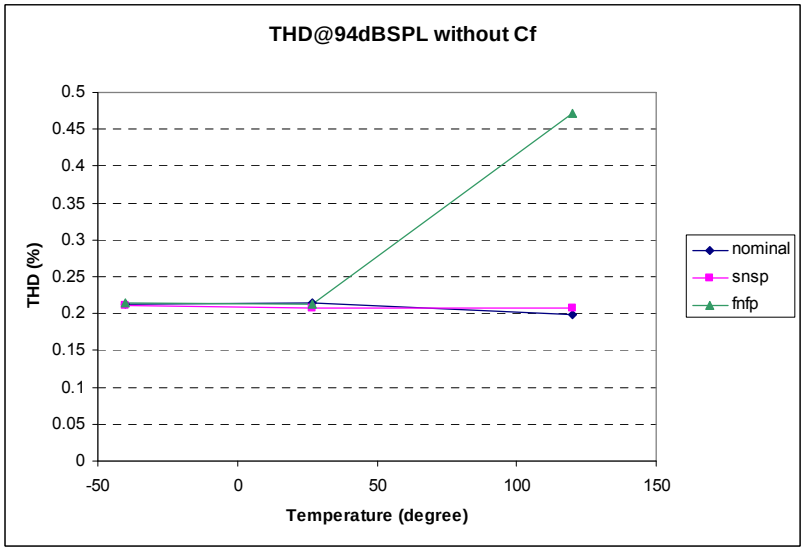

Figure 6. 8 Corner simulation for THD when there is no C_f.

6.5.2 Corner Simulation with C_f = 390 fF

The corner simulation with C_f = 390 fF is shown in Figure 6. 9. These curves have the same trend as that in Figure 6. 7. At 120°C, SNR is several dB lower than the specification. By sweeping temperature with "fnfp" corner, the highest temperature limit is 50°C.

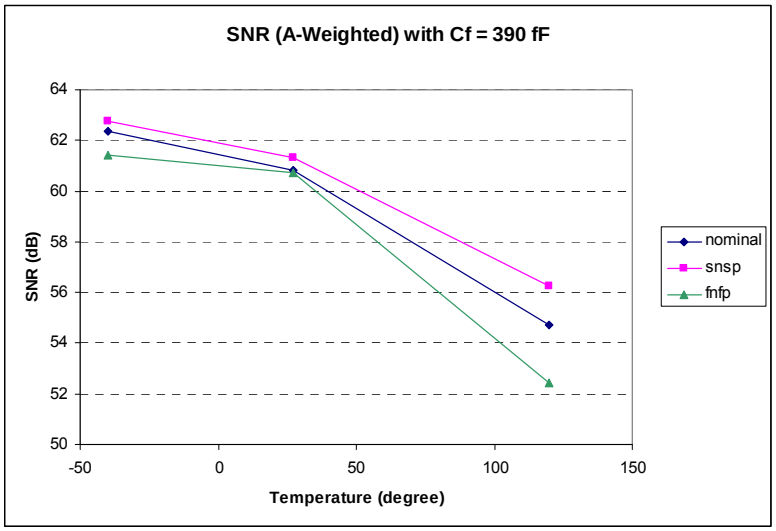

Figure 6. 9 Corner simulation for SNR when C_f = 390 fF.

Figure 6. 10 shows the THD simulation result. The "fnfp" corner still behaves the worst. And from about 60°C above, the "nominal" corner exceeds the THD specification.

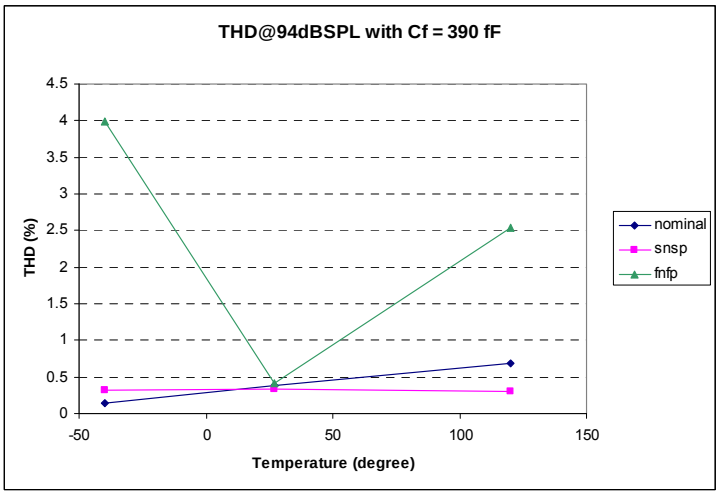

Figure 6. 10 Corner simulation for THD when C_f = 390 fF.

Figure 6. 10 indicates that for THD consideration, the 390 fF C_f is not a good value for high yield since the "fnfp" corner does not behave well. The curves of "nominal" and "snsp" corners, however, can be regarded as being confined in the THD specification.

6.6 Monte-Carlo Simulation

Monto-Carlo Simulation in Cadence is aiming at checking the effect of process and mismatch spread of CMOS technology. Figure 6. 11 is the Monte-Carlo simulation for SNR with C_f = 390 fF. The simulation runs for 400 combinations of process and mismatch spread. The mean of the SNR is 60.85 dB and the variance is 138.903 mdB which can be regarded as a good result.

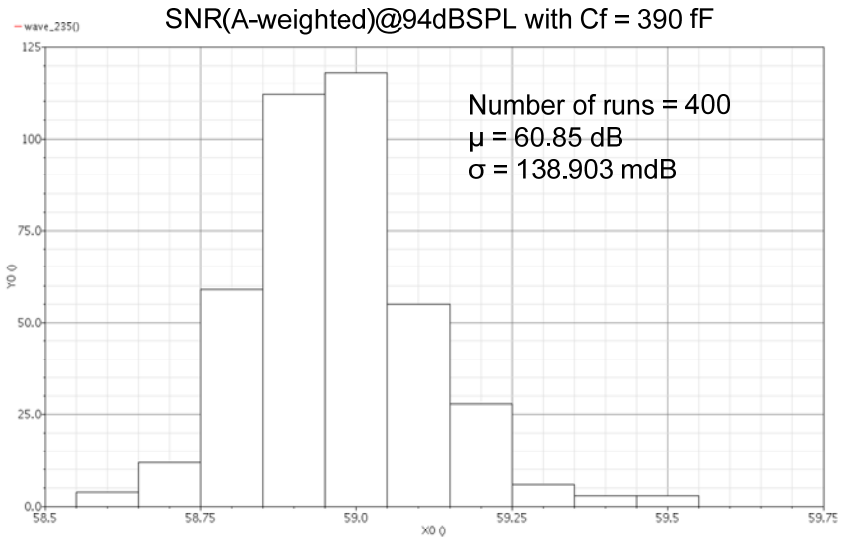

Figure 6. 11 Monte-Carlo simulation for SNR with C_f = 390 fF at 94dBSPL input.

Figure 6. 12 is the Monte-Carlo simulation for THD with C_f = 390 fF. The mean of the 400 runs is 0.42% and the variance is 0.144%.

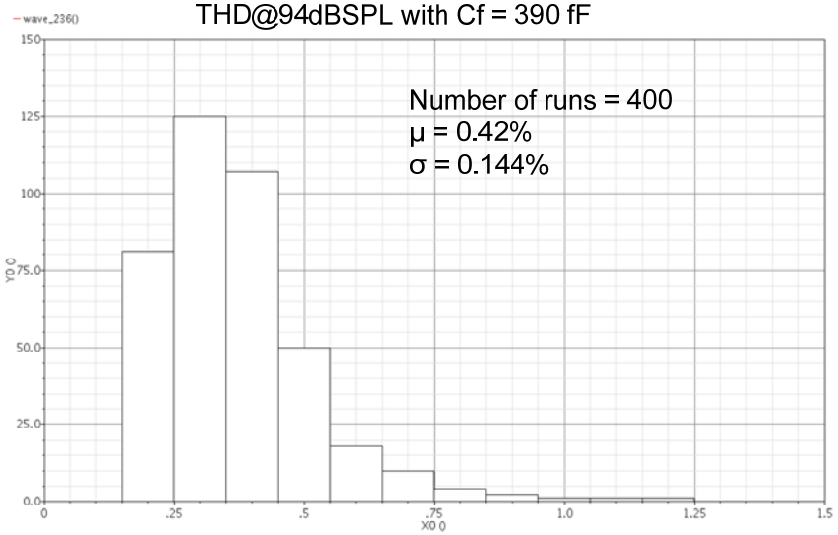

Figure 6. 12 Monte-Carlo simulation for SNR with C_f = 390 fF at 94dBSPL input.

6.7 Comparison

Table 6. 1 lists the specification of this design and the products on the market. This design exceeds in the SNR, sensitivity and bandwidth specification with comparably large power consumption.

Specification / Product	SNR@1Pa (dB)(A-weighted)	Sensitivity @1Pa (dBV/Pa)	Current (uA)	Band-width (HZ)	THD(%)
SPM0204HE5 (Knowles Acoustics)	59	-42	100 (V_{DD}=1.5~3.6V)	14K	1%@100dBSPL
ADMP401-1 (ADI)	62	-37	200 (V_{DD}=1.5~3.6V)	12K	3%@105dBSPL
AKU1126 (Akustica)	58	-42	150 (V_{DD}=1.65~3.6V)	N/A	5%@115dBSPL
SMM310 (Infineon)	59	-42	80 (V_{DD}=2.1V)	10K	0.1%@104dBSPL
TC200A (Pulse MEMS)	61	-40	330 (V_{DD}=1.64~2.86V)	20K	10%@110dBSPL
Previous Design	60	-45	450 (V_{DD}=2.5V)	20K	0.5% @ 94dBSPL
This Design	**61**	**-36**	**320 (V_{DD}=3.3V)**	**20K**	**0.37% @ 94dBSPL** **0.51% @ 100dBSPL** **1.49% @ 105dBSPL** **4.22% @ 110dBSPL** **4.28% @ 115dBSPL**

Table 6. 1 Comparison between this design and the products on market.

6.8 Conclusion

The corners simulations and Monte-Carlo simulations present a rough idea about the performance of the circuit after they are fabricated in CMOS technology. The results of these simulation implies that the circuit can achieve and even exceed the specification at low temperature and normal temperature (-40˚C ~50˚C). While at high temperature, its behavior especially the SNR drops quickly. Moreover, the effect of process variance on THD specification has to be improved.

Chapter 7 Conclusion and Future Work

7.1 Conclusion

The purpose of this work is to propose a readout scheme for a MEMS microphone with a comparatively low bias voltage due to the fact that the previous design uses a charge pump to bias the microphone which increase the circuit's complexity. The comparison between the different readout schemes indicates that every scheme has a trade-off among the specifications. For DC biasing scheme, the main disadvantage is that the existence of parasitic capacitance kills the sensitivity. This design thus takes advantage of Miller effect to decrease the parasitic capacitance. In this way the sensitivity on the microphone is increased by 9 dB compared to the previous design with only 3.3 volt bias voltage.

The Miller effect is realized by adding a positive feedback capacitor C_f from the preamplifier's output to input. In order to find an acceptable value of the positive feedback capacitor, C_f is replaced by a 4-bit DAC. For stability consideration, switches connected to ground are added.

The preamplifier employs folded-cascoded structure to be able to sense the positive rail. The aspect ratio of the transistors is chosen to minimize the noise level. The unity gain bandwidth of the amplifier is 4.6 MHz and it consumes 320 uA current.

With the maximum acceptable C_f (390 fF), the sensitivity on the microphone under 3.3 V bias voltage is increased by 9 dB compared to previous design which is with 5 V bias voltage. The specification of SNR and THD, however, is deteriorated slightly compared to the case when there is no feedback capacitor. The SNR is decreased less than 0.4 dB and the THD is increased by 0.16% with 1 Pa input sound pressure. Even though, SNR and THD still meet the specifications.

7.2 Future Work

The ultimate aim of the research is to produce outstanding products on the market. Although the current design has met the specification, it still needs further improvements.

Nowadays most of the current electronic products are based on battery supply, thus the power consumption is supposed to be kept small. Since this design has not optimized the current to achieve low noise, there exists possibility to decrease the power consumption even further while still keep the same SNR.

In this design, the preamplifier is not differential. Therefore, the noise from the current source in the bias scheme can not be neglected and the even-order harmonics can not be reduced. In order to avoid the effect, a fully differential amplifier is needed. This method, however, requires another low-noise differential-to-single-ended buffer which might compensate the noise reduced by the previous differential stage and consume more power.

The gain of the preamplifier is not accurately defined because the source degeneration resistor is not much higher than the transconductance of the input pair and thus the linearity of preamplifier is not maximized as well. Since the source degeneration resistors increase the noise in the same time, their value is limited by the SNR specification. Therefore, other linearization techniques and accurately defined gain structures are required to be investigated to make the system achieve better performance.

Another drawback of the current design is its bad performance at high temperature. The temperature dependent impedance of the diode-connected PMOS is the main reason. Thereby a bias device with high impedance and low temperature variance is highly demanded. When referring to high impedance device, switched-capacitor resistor is an option. But the transient noise of it is another concern.

Further investigations can also be directed to find another promising scheme which is based on a different readout theory. High sensitivity, low noise and good linearity are the thumbs of rules to follow when doing future research.

Appendix A

Verilog-A Model for Microphone

The Verilog-A scripts for the microphone are listed here. Figure A. 1 explains the basic principle behind the model. The model includes the parasitic capacitance between back plate and bulk as well. In this model, a simple voltage source can represent an acoustic signal. For instance, a sinusoidal voltage source with 1 V amplitude and 1 KHz frequency is equivalent to a sound wave with 1 Pa amplitude and 1 KHz frequency.

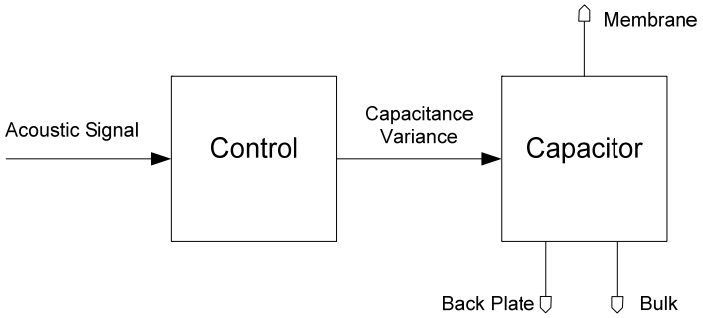

Figure A. 1 Verilog-A Model for microphone

```
// VerilogA for veriloga, Fa, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Fa(in, dc);
   input in;
   output dc; //dc stands for capacitance variance;
   electrical dc, in;

  parameter real k      = 0.00119;  //derived from
equation (1. 7);

   analog begin
    V(dc) <+ V(in)*k;
   end

endmodule
```

```
// VerilogA for veriloga, Cmic, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Cmic(mem, bp, bulk, Fa);
   input mem, bp, bulk;
   input Fa;
   electrical Fa, bp, mem, bulk;  //Fa stands for acoustical
force;

   parameter real Co = 2.94e-12;
   parameter real Cp1 = 0.7e-12;
   parameter real Cp2 = 3.2e-12;
   real v1,v2,dvar,c;

   analog begin
   v1 = V(mem,bp);
   v2 = V(bp,bulk);
   dvar = V(Fa);
   c=Co*(1+dvar)+Cp1;
   I(mem,bp) <+ ddt(v1*c);
   I(bp,bulk) <+ ddt(v2*Cp2);
   end

endmodule
```

The behavior of the model is tested in Cadence with 1 Pa (rms) input in DC biasing scheme, the signal generated from this model meets the characteristic of the microphone.

Appendix B

Mathematic Derivation without Constant Charge Assumption

Assuming the voltage on the microphone is $V_{ref} + V_\Delta$ when the capacitance variation of the microphone is C_Δ, we can derive the following equation:

$$i = -\frac{V_\Delta}{R_b} \tag{B. 1}$$

And the varying current generated from the capacitor is:

$$i = \frac{dQ}{dt} = \frac{d(C \cdot V)}{dt} = (C_{mic} + C_\Delta)\frac{d(V_\Delta)}{dt} + (V_{ref} + V_\Delta)\frac{d(C_\Delta)}{dt} \tag{B. 2}$$

Equalizing equation (B. 1) and (B. 2) and replacing C_Δ with $kC_{mic}\hat{P}\sin(\omega t)$ yields:

$$\left(C_{mic} + kC_{mic}\hat{P}\sin(\omega t)\right)\frac{d(V_\Delta)}{dt} + \left(kC_{mic}\hat{P}\omega\cos(\omega t) + \frac{1}{R_b}\right)\cdot V_\Delta + V_{ref}kC_{mic}\hat{P}\omega\cos(\omega t) = 0 \tag{B. 3}$$

Equation (B. 3) is a typical first-Order non-homogeneous linear differential equation. Given the initial condition that $V_\Delta(t = 0) = 0$, the solution is:

$$V_\Delta = -\frac{1}{1 + k\hat{P}\,\text{Sin}[w\,t]}\left(e^{-\frac{2\,\text{ArcTan}\left[\frac{k\hat{P}+\text{Tan}\left[\frac{wt}{2}\right]}{\sqrt{1-k^2\hat{P}^2}}\right]}{C_{mic}\sqrt{1-k^2\hat{P}^2}\,R_b\,w}}\left(\int_t^0 -e^{\frac{2\,\text{ArcTan}\left[\frac{k\hat{P}+\text{Tan}\left[\frac{wt}{2}\right]}{\sqrt{1-k^2\hat{P}^2}}\right]}{C_{mic}\sqrt{1-k^2\hat{P}^2}\,R_b\,w}}\,k\hat{P}\,V_{ref}\,w\,\text{Cos}[\,wt]\,dl\,t - \int_0^t -e^{\frac{2\,\text{ArcTan}\left[\frac{k\hat{P}+\text{Tan}\left[\frac{wt}{2}\right]}{\sqrt{1-k^2\hat{P}^2}}\right]}{C_{mic}\sqrt{1-k^2\hat{P}^2}\,R_b\,w}}\,k\hat{P}\,V_{ref}\,w\,\text{Cos}[wt]\,dl\,t\right)\right) \tag{B. 4}$$

Appendix C

Matlab Scripts Used in DC Biasing with Positive Feedback

```
clear all; close all;clc;
Rb=7e12;Cp=5e-12;deltac=3.528e-15/sqrt(2);
k=1.38e-23;T=300;
vref=3.3;
f=1000;
Ramp=30e3;
nop=4*k*T*Ramp;
s=j*2*pi*f;
Zb=Rb/(1+Rb*Cp*s);
Av=11;
Cf=0:10e-15:500e-15;

for n=1:length(Cf)
Zf=1/(s*Cf(n));
vzbtf=abs(Av*Zf*Zb/(Zf+(1-Av)*Zb)); % noise transfer function of from Rb to out
vnRb=4*k*T/Rb*vzbtf^2; %noise from bias resistor;

vamptf=abs(Av*(Zf+Zb)/(Zb*(Av-1)-Zf)); % noise transfer function of from in to out
vnamp=nop*vamptf^2;  %noise from opamp;
vntot(n)=vnRb+vnamp;    %total noise;

syms f
vnrms(n)= double(sqrt(int(vntot(n),f,20,20000))); %rms noise;
f=1000;
vs(n)=Av*vref*deltac/(deltac+Cp+(1-Av)*Cf(n));  %rms signal;
snr(n)= 20*log10(vs(n)/vnrms(n));

end

subplot(3,1,1),plot(Cf,20*log10(vs),'g','LineWidth',3);
legend('Signal');
xlabel('Cf(F)'); ylabel('Signal(dB)');axis([0 570e-15 -40 40]);

subplot(3,1,2),plot(Cf,20*log10(vnrms),'r','LineWidth',3);
legend('Noise');
xlabel('Cf(F)'); ylabel('20*Log NoiseRMS (V)');axis([0 570e-15 -100 0]);

subplot(3,1,3),plot(Cf,snr,'b','LineWidth',3);
legend('SNR');
xlabel('Cf(F)'); ylabel('SNR(dB)');axis([0 570e-15 10 70]);
```

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