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High Step-Up DC–DC Converter With Low Switch Voltage Stress, Continuous Input Current, and ZVS Operation

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ABSTRACT This article introduces a new fully soft switched ultra-high step-up quadratic converter. The proposed converter benefits from several advanced features including high voltage gain at low duty cycle, low switch voltage stress, low sum of diodes voltage stress, switching at ZVS condition for switches, low ripple continuous input current, and common ground between the input and load. These advantages are achieved by integrating the quadratic structure with an auxiliary circuit consisting of coupled inductors, switched capacitors, and active clamp techniques. Furthermore, the presented converter mitigates the reverse recovery problem of all diodes especially the input side diodes which is a challenge in many quadratic base converters. These properties have contributed to providing an efficient converter with wide applicability. The converter is fully analyzed, its superiority to other structures is shown, and a 200 W laboratory prototype validates the theoretical analysis.

INDEX TERMS High voltage gain converter, low switch voltage stress, ZVS operation.

I. INTRODUCTION

Today, DC-DC high step-up converters, which are integral components in many power electronic systems such as electric motors, three-phase motor drive systems, microgrid systems, and renewable energy systems, are advancing significantly and gaining increasing importance [1], [2], [3], [4]. The basic boost structure is the simplest step-up topology, but its voltage gain (VG) is limited, the output voltage is imposed on its switch, and has low efficiency at high gains. Significant research is performed to improve high step-up converters specifications including VG, efficiency, and cost. Quadratic structure is an attractive solution to enhance the VG exponentially while maintaining the boost converter advantages such as low input current ripple (ICR) and common ground (CG) between the input and output. To improve the VG and switch voltage stress, high step-up methods are merged with the basic boost and quadratic structures in numerous topologies [5], [6].

The high step-up converter in [5] is formed by the integration of two boost structures, switched capacitors (SCs) technique, and an energy storage cell, and its switch voltage stress is lower than half of the output voltage. However, employing two switches, lack of CG, and high ICR are the main drawbacks. The introduced quadratic converter in [6] uses dual coupled inductors (CIs) to improve VG and switch voltage stress. However, despite having five windings, its VG is relativity low, and coupling the input inductor leads to high ICR which limits its applicability. The high step-up converter in [7] is a combination of two boost converters and a voltage doubler cell. This converter benefits from low ICR and CG, but each boost stage has an independent switch and the switches voltage stress is still high which leads to high switching and capacitive turn-on losses. Besides, switches conduction losses are reduced by high-cost switches. Although the high step-up converter in [8] has successfully reduced the switch voltage stress using a voltage multiplier cell (VMC), it still has high ICR and employs an extra switch which increases the cost and control complexity. Integrating three windings CIs and SCs methods with the quadratic

structure provides high VG and low switch voltage stress for the converters in [9] and [10], and by coupling the quadratic converter middle inductor, low ICR merit is maintained. In these converters, an internal diode-capacitor path absorbs the leakage inductance energy which prevents any voltage spike on the switch.

Switching losses and the diodes reverse recovery problem are common drawbacks in the converters of [5], [6], [7], [8], [9], and [10] which adversely affects the efficiency, especially at high powers and frequencies. The converter in [11] achieves the exponential VG versus duty cycle by combining two boosting stages, and high step-up techniques while by switches suitable placement, zero current switching (ZCS) at turn-on is provided. By integration of boost and restructured quasi-Y-source converters, a high step-up converter is presents in [12]. The converter in [13] is formed by combining the quadratic structure, three windings CIs, and SCs methods. Despite the converters in [11], [12], [13], and [14] providing the switch ZCS turn-on and solving the reverse recovery problem, they suffer from capacitive turn-on loss and switching turn-off loss. Moreover, the converters in [11] and [14] employs two switches and their ICR is high.

In the presented converters of [15] and [16] SCs and CIs techniques improve the converter VG and switch voltage stress. In [15] and [16], a zero voltage transition (ZVT) cell realizes the zero voltage switching (ZVS) for the main switch nonetheless, their auxiliary switch is turned on at ZCS, and capacitive turn-on loss is their common problem. Extending CIs turns ratio and diode-capacitor cell numbers, improves the converter VG and switch voltage stress in [17], and an active clamp cell provides ZVS operation for both main switches. However, utilizing extreme switches in these converters leads to high cost and control complexity. The converter in [18] has a suitable component count, and using an active clamp cell achieves soft switching operation. However, the VG is relativity low and the converters in [16], [17], and [18] suffer from high ICR which is an inappropriate feature for renewable energy systems. Although the converter in [19] reduces the semiconductors voltage stress, eliminates the switching losses, and has low ICR, its VG is relativity low, and increasing the diode-capacitor stages to improve the VG, leads to high component count. The high step-up converters in [20] and [21] are a combination of quadratic structure, CIs and VMCs cells, and an active clamp circuit. These converters benefit from low switch voltage stress, low ICR, and ZVS operation. However, losing CG in [20] limits its applicability, and the three magnetic cores used in [21] leads to low power density.

In this article, a new ultra-high step-up quadratic base converter is proposed. The novel combination of CIs, SCs, and active clamp techniques with the quadratic structure provides several advantages comprising ultra-high voltage gain at low duty cycle, low switch voltage stress, and fully soft switching operation. In addition, the proper use of CIs in the quadratic converter input side provides soft recovery for the input side diodes and further improves the voltage gain and the switch voltage stress. Besides, the basic structure features including input current continuity and common ground are maintained. Moreover, the leakage inductance energy is absorbed and recycled to the load and due to the ZVZCS condition at the switches turn on, capacitive turn-on losses are eliminated. The mentioned advantages have enhanced the converter efficiency.

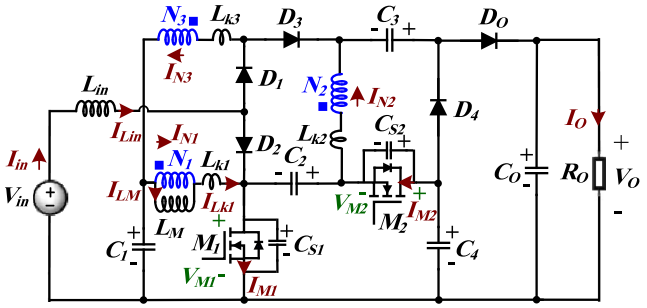

FIGURE 1. Proposed converter equivalent circuit.

II. PROPOSED CONVERTER OPERATING PRINCIPLES

The proposed converter equivalent circuit is shown in Fig. 1. In this converter, main switch M_1, input side diodes D_1 and D_2, output diode D_O, input inductor L_{in}, winding N_1, and capacitors C_1 and C_O comprise the basic quadratic converter. The auxiliary switch M_2, and capacitors C_2 and C_4 create the active clamp structure which absorbs the leakage inductance energy at the M_1 turn-off moment and provides ZVZCS at the M_1 turn-on. Notably, due to the suitable placement of C_2, it plays role in both high step-up and active clamp structures. Diodes D_3 and D_4, capacitor C_3, windings N_2 and N_3, and the active clamp components include the high step-up structure. Moreover, winding N_3 provides soft reverse recovery for input side diodes, and the snubber capacitors C_{S1} and C_{S2} eliminate the switching losses at the turn-off for M_1 and M_2, respectively. Windings N_1, N_2, and N_3 are coupled, and modeled by a magnetizing inductance L_M, an ideal transformer with $n = N_2/N_1$ and $m = N_3/N_1$ turns ratios, and the leakage inductances L_{k1}, L_{k2}, and L_{k3}. The capacitors $C_1 - C_4$ voltages and L_{in} current are assumed constant in a switching cycle due to their large values. The converter equivalent circuit in nine operating modes and its theoretical waveforms are illustrated in Figs. 2 and 3, respectively.

*Mode*1 (t_0-t_1): At t_0, switch M_1 is turned on at ZVZCS due to its body diode conduction which eliminates switching and capacitive turn-on losses. Diodes D_2 and D_4 conduct, and other semiconductor devices are off. V_{in} and V_{C1} charge L_{in} and L_M, respectively. I_{Lk1} increases from a negative value, while C_4 and N_2 are charging C_3 and C_2, and C_O supplies the load.

$$I_{Lin}(t) = I_{Lin}(t_0) + \frac{V_{in}(t - t_0)}{L_{in}} \tag{1}$$

$$I_{LM}(t) = I_{LM}(t_0) + \frac{V_{C1}(t - t_0)}{L_M} \tag{2}$$

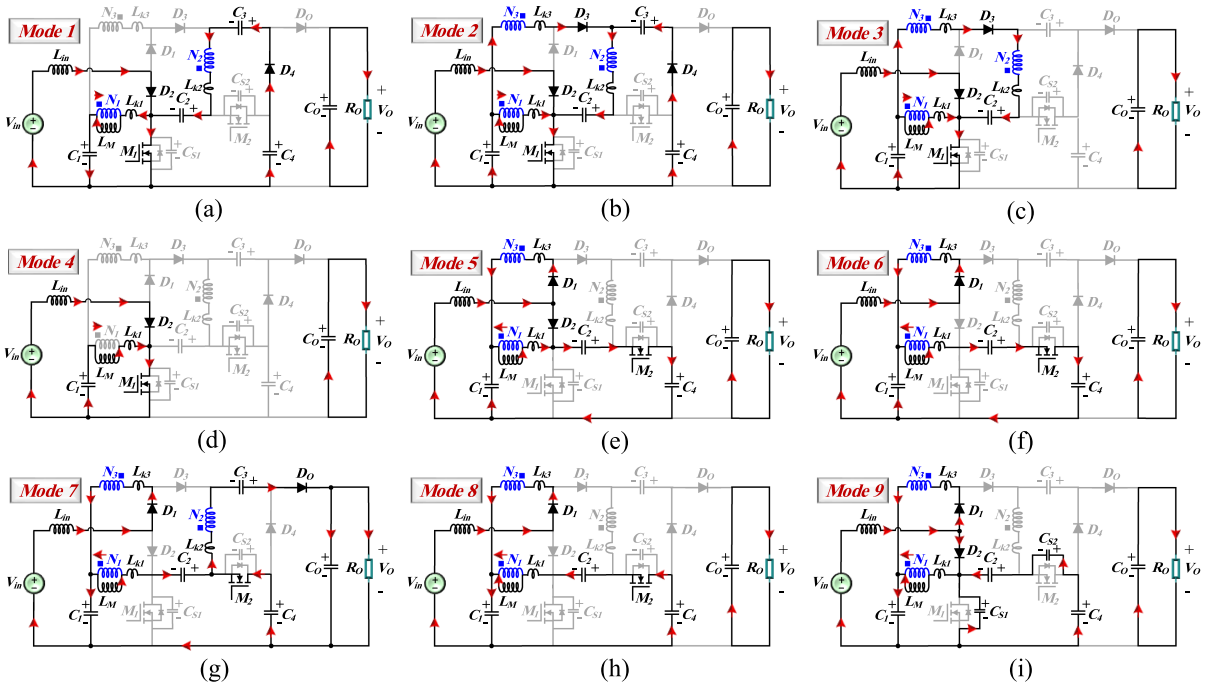

FIGURE 2. Equivalent circuit of each converter operating mode. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7, (h) Mode 8, and (i) Mode 9.

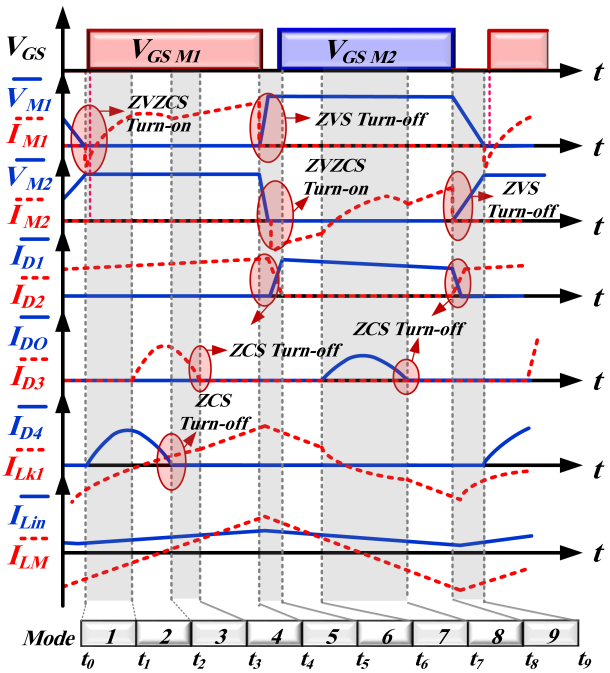

FIGURE 3. Proposed converter theoretical voltage and current waveforms.

$$nI_{N1}(t) = -I_{N2}(t) = I_{D4}(t) \simeq \frac{I_O\omega_1}{2f_{sw}}\sin(\omega_1 t) \tag{3}$$

$$\omega_1 \simeq \frac{1}{\sqrt{L_{k2}(\frac{1}{C_2}+\frac{1}{C_3}+\frac{1}{C_4})}} \tag{4}$$

*Mode*2 (t_1-t_2): At the beginning of this mode, I_{Lk1} becomes positive and thus, D_3 starts conducting while the D_4 current decreases. In this mode, L_{in} and L_m are charged like in mode 1, and the CIs windings charge C_2. At t_2, D_4 turns off at ZCS.

$$-I_{N3}(t) = I_{D3}(t) \simeq \frac{I_O\omega_2}{2f_{sw}}\sin(\omega_2(t-t_1)) \tag{5}$$

$$\omega_2 \simeq \frac{1}{\sqrt{(L_{k2}+L_{k3})(\frac{1}{C_1}+\frac{1}{C_2})}} \tag{6}$$

$$I_{C3}(t) = -I_{C4}(t) = I_{D4}(t) \simeq \frac{I_O\omega_1}{2f_{sw}}\sin(\omega_1(t-t_1)) \tag{7}$$

$$I_{C2}(t) = -I_{N2}(t) = I_{D3}(t) + I_{D4}(t) \tag{8}$$

$$I_{N1}(t) = (n+m)I_{D3}(t) + nI_{D4}(t) \tag{9}$$

*Mode*3 (t_2-t_3): In this mode, D_2 and D_3 conduct and L_{in} and L_m are charged linearly while other diodes are reverse biased. At t_3, I_{LM} reaches I_{Lk1}, the N_1 current becomes zero and D_3 turns off at ZCS.

$$-I_{N2}(t) = -I_{N2}(t) = I_{D3}(t) \simeq \frac{I_O\omega_2}{2f_{sw}}\sin(\omega_2(t-t_2)) \tag{10}$$

$$I_{N1}(t) = (n+m)I_{D3}(t) \tag{11}$$

*Mode*4 (t_3-t_4): During this mode, M_1 and D_2 are conducting and other semiconductor devices are off, the energy continues to store in L_{in} and L_M, and C_O supplies the load. At the end of this mode, M_1 is turned off at ZVS.

*Mode*5 (t_4-t_5): At t_5, M_1 is turned off at ZVS due to C_{S1}. Then, the D_1 current increases slowly due to L_{k3}, and V_{M1} +

V_{M2} is clamped to $V_{C4} - V_{C2}$ thus, by charging C_{S1}, C_{S2} is fully discharged. Then, M_2 body diode conducts, and C_2 and C_4 absorb the L_{k1} energy through M_2. At t_5, the D_1 current reaches I_{in} and D_2 turns off at ZCS.

$$I_{D1}(t) = \frac{(m+1)(V_{C4} - V_{C1} - V_{C2})(t - t_4)}{L_{k3}} \tag{12}$$

*Mode*6 (t_5-t_6): In this mode, M_2 is turned on at ZVZCS and I_{Lin}, and I_{LM} decrease linearly. At t_6, I_{Lk1} (which is equal to $I_{LM}(t) - mI_{Lin}(t)$) becomes equal to I_{in}.

$$I_{Lin}(t) = I_{Lin}(t_5) - \frac{1}{L_{in}}((m+1)V_{C1} + m(V_{C2} - V_{C4}) - V_{in})(t - t_5) \tag{13}$$

$$I_{LM}(t) = I_{LM}(t_5) - \frac{(V_{C4} - V_{C1} - V_{C2})(t - t_5)}{L_M} \tag{14}$$

$$t_6 - t_5 = \frac{L_M(I_{LM}(t_3) - (m+1)I_{in})}{V_{C4} - V_{C1} - V_{C2}} \tag{15}$$

*Mode*7 (t_6-t_7): At t_6, D_O begins conducting, and power is transferred to the load. In this mode, the current flows through M_2 in the positive direction, and $I_{L_{in}}$ charges C_1. During this mode, $II_{L_{in}}$, and I_{LM} are reduced like in the previous mode. I_{Lk1} decreases until it becomes negative while the D_O current diminishes at t_7 and D_O turns off at ZCS. This mode duration is equal to π/ω_3.

$$I_{N2}(t) = I_{DO}(t) \simeq \frac{I_O\omega_3}{2f_{sw}}\sin(\omega_3(t - t_6)) \tag{16}$$

$$\omega_3 \simeq \frac{1}{\sqrt{L_{k2}(\frac{1}{C_4} + \frac{1}{C_3} + \frac{1}{C_O})^{-1}}} \tag{17}$$

$$I_{N3}(t) = I_{Lin}(t), I_{N1}(t) = -(nI_{DO}(t) + mI_{Lin}(t)) \tag{18}$$

$$I_{C2}(t) = I_{N1}(t) - I_{LM}(t) \tag{19}$$

$$I_{C1}(t) = I_{C2}(t) + I_{N1}(t) \tag{20}$$

*Mode*8 (t_7-t_8): In this mode, only M_2 and D_1 are on and other semiconductor devices are off. Current $mI_{in} - I_{LM}$ charges C_2 and discharges C_4 respectively and $(m+1)I_{in} - I_{LM}$ charges C_1, while C_O supplies the load.

*Mode*9 (t_8-t_9): This mode starts by turning off M_2 at ZVS and C_{S2} and C_{S1} are charged and discharged respectively. At t_9, V_{M2} clamps to $V_{C4} - V_{C2}$, C_{S1} is fully discharged, and M_1 body diode conducts. Thus, M_1 can be turned on at ZVZCS. Meanwhile, the D_1 current decreases, D_2 is conducting, and L_{k3} limits the D_1 falling current slop which provides soft recovery for D_1.

III. PROPOSED CONVERTER ANALYSIS

By applying the Volt-second balance on L_{in} and L_M, the following relation is achieved:

$$V_{in}DT + (V_{in} - (1+m)V_{C1} + m(V_{C4} - V_{C2}))(1 - D)T = 0 \tag{21}$$

$$V_{C1}DT + (V_{C1} + V_{C2} - V_{C4}))(1 - D)T = 0 \tag{22}$$

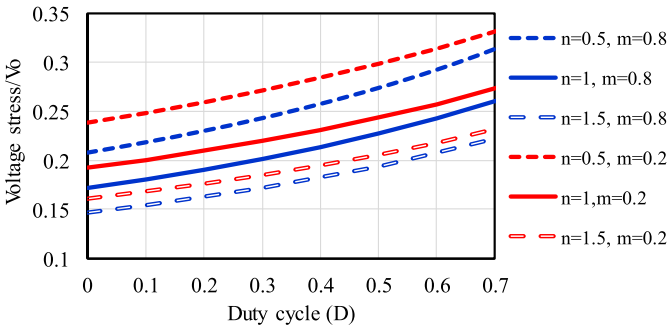

FIGURE 4. Switch voltage stress versus *D*.

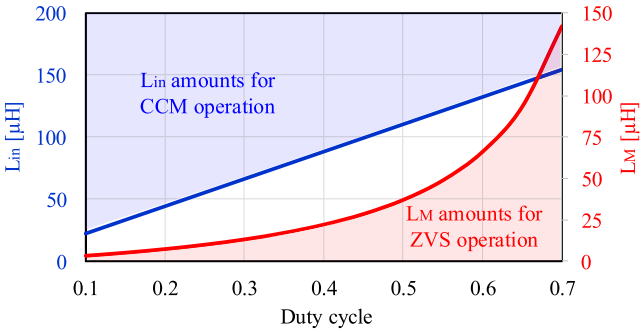

FIGURE 5. L_{in} and L_M versus D for $V_O = 700V$.

During the M_1 on-state, V_{C1} is applied on N_1, and when M_1 is off, $V_{C1} + V_{C2} - V_{C4}$ is imposed on N_1. Thus, by writing Kirchhoff Voltage Law (KVL) in mode 2 and mode 6, the following relation is obtained:

$$(1 + n + m)V_{C1} - V_{C2} = 0 \tag{23}$$

$$nV_{C1} - V_{C2} - V_{C3} + V_{C4} = 0 \tag{24}$$

Using (21)-(24), the capacitor voltages are obtained as:

$$V_{C1} = \frac{V_{in}}{1 - (1+m)D}, V_{C2} = \frac{(1+n+m)}{1 - (1+m)D}V_{in} \tag{25}$$

$$V_{C3} = \frac{1 + n(1-D)}{(1-D)(1-(1+m)D)}V_{in} \tag{26}$$

$$V_{C4} = \frac{2 + n + m - (1+n+m)D}{(1-D)(1-(1+m)D)}V_{in} \tag{27}$$

Using KVL in mode 7, the output voltage is attained as $V_{C1} + V_{C3} + n(V_{C4} - V_{C2} - V_{C1})$ thus, by substituting (25)-(27) into this relation, the converter voltage gain is achieved as:

$$VG = \frac{V_O}{V_{in}} = \frac{3 + n(2-D) + m(1-D) - D}{(1-D)(1-(1+m)D)} \tag{28}$$

Voltage $V_{C4} - V_{C2}$ is imposed on M_1 and M_2 in their off-states, and voltage $(1+m)V_{C1}$ is applied on D_1 in mode 3. The voltage stress on D_2 and D_3 is equal to $(1+m)(V_{C4} - V_{C2} - V_{C1})$ and $V_O - (1+m)V_{C1} - V_{C3} - m(V_{C2} - V_{C4})$, respectively, and when D_O and D_4 are off, $V_O - V_{C4}$ is imposed

TABLE I. Comparison Between the Proposed Converter and Other Structures

Con.	Voltage gain	Switch voltage stress	Sum of the diodes voltage stresses	Number of S[1]	D[2]	BC[3]	C/W[4]	Switching condition turn-on	turn-off	SRRP[5]	CG[5]	LICR[6]
[5]	$\frac{2+D}{(1-D)^2}$	$\frac{V_O}{2+D}$	$\frac{(8VG-1+(1+12VG)^{0.5})V_O}{(6VG+1-(1+12VG)^{0.5})}$	2	5	6	3/3	Hard	Hard	×	×	×
[7]	$\frac{1+2n+D}{(1-D)^2}$	$\frac{(1+D)V_O}{1+2n+D}$	$\frac{(4+4n-2D)V_O}{1+2n+D}$	2	5	5	2/3	Hard	Hard	×	✓	✓
[9]	$\frac{2+n+m-D(1+n)}{(1-D)^2}$	$\frac{V_O}{2+n+m-D(1+n)}$	$\frac{(3+2m+n(1-2D))V_O}{2+n+m-D(1+n)}$	1	6	5	2/4	Hard	Hard	×	✓	✓
[10]	$\frac{2+n+m+mD}{(1-D)^2}$	$\frac{V_O}{2+n+m+mD}$	$\frac{(4+3m+2n)V_O}{2+n+m+mD}$	1	6	5	2/4	Hard	Hard	×	×	✓
[12]	$\frac{2+n}{(1-(1+m)D)(1-D)}$	$\frac{V_O}{2+n}$	$2V_O$	1	5	4	2/4	ZCS	Hard	✓	✓	✓
[14]	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{V_O}{3+2n-D(3+n-D)}$	$\frac{(5+4n-2nD-3D)V_O}{3+2n-D(3+n-D)}$	2	5	5	2/3	ZCS	Hard	✓	✓	×
[17]	$\frac{(2-D)(n+m(1-D))+1-D}{(1-D)^2}$	$\frac{V_O}{(2-D)(n+m(1-D))+1-D}$	$\frac{(3n(2-D)+1-D)V_O}{(2-D)(n+m(1-D))+1-D}$	3	4	5	2/4	ZVZCS	ZVS	✓	✓	×
[18]	$\frac{m(n+1)(1+D)+2}{1-D}$	$\frac{V_O}{m(n+1)(1+D)+2}$	$\frac{(3m(n+1)+3)V_O}{m(n+1)(1+D)+2}$	2	3	5	2/4	ZVZCS	ZVS	✓	✓	×
[19]	$\frac{1+2n}{1-D}$	$\frac{V_O}{1+2n}$	$\frac{4nV_O}{1+2n}$	2	4	6	2/3	ZVZCS	ZVS	✓	✓	✓
[21]	$\frac{2+n+m}{(1-D)^2}$	$\frac{V_O}{2+n+m}$	$\frac{(3+2n+2m)V_O}{2+n+m}$	2	4	5	3/5	ZVZCS	ZVS	×	✓	✓
Pro.	$\frac{3+n(2-D)+m(1-D)-D}{(1-(1+m)D)(1-D)}$	$\frac{V_O}{3+n(2-D)+m(1-D)-D}$	$\frac{(3+2(n+m))V_O}{3+n(2-D)+m(1-D)-D}$	2	5	5	2/4	ZVZCS	ZVS	✓	✓	✓

1. Switch 2. Diode 3. Bulky capacitor 4. Magnetic core/winding 5. Solve the reverse recovery problem for all diodes 6. Common ground
7. Low input current ripple

on them. Thus, using (25)-(28), the switches and diodes voltage stresses are derived as

$$V_{M1} = V_{M2} = \frac{V_O}{3 + n(2 - D) + m(1 - D) - D} \tag{29}$$

$$V_{D1} = \frac{(1 + m)(1 - D)}{3 + n(2 - D) + m(1 - D) - D} V_O \tag{30}$$

$$V_{D2} = \frac{(1 + m)D}{3 + n(2 - D) + m(1 - D) - D} V_O \tag{31}$$

$$V_{D3} = (1 + n + m)V_{M1} \tag{32}$$

$$V_{D4} = V_{DO} = (1 + n)V_{M1} \tag{33}$$

The switch voltage stress at various n and m are illustrated in Fig. 4 indicating very low voltage stress even at low CIs turns ratios.

The main switch peak current is at the end of mode 4 (t_4) and by employing KCL at t_4, the following relation is obtained:

$$I_{M1,\max} = (VG)I_O + I_{LM} + \frac{V_{C1}D}{f_{sw}L_M} + \frac{V_{in}D}{f_{sw}L_{in}} \tag{34}$$

In mode 5, the D_1 current increases as (3) until at t_5 becomes I_{in} then, D_2 turns off. During this mode, $V_{in} + V_{C2} - V_{C4}$ is applied to L_{in}, and L_{k3} affects the VG. Thus, using Volt-second balance on L_{in} and KVL in mode 2 and mode 6, the VG by considering the L_{k3} effect is obtained as:

$$VG = \frac{V_O}{V_{in}} = \frac{3 + n(2 - D) + m(1 - D) - D}{(1 - D)(1 - (1 + m)D(1 - \frac{D_{Loss}}{1-D}))} \tag{35}$$

$$D_{Loss} = (t_5 - t_4)f_{sw} = \frac{(VG)I_O L_{k3} f_{sw}}{(m + 1)(V_{C4} - V_{C1} - V_{C2})} \tag{36}$$

IV. DESIGN CONSIDERATIONS

A. ELEMENTS DESIGN

The input inductor is designed from the general equation $L_{in} = V_{Lin}\Delta t/(\Delta I_{Lin})$. During the M_1 on-state (DT), the input voltage (V_{in}) charges L_{in}. To operate in Continuous Conduction Mode (CCM), the suitable amount of the L_{in} current ripple at the worst operating condition (CCM/DCM boundary condition at light load) is equal to $2I_{in,min}$. Assuming ideal elements, I_{in} is equal to $(VG)I_O$. Thus, L_{in} is designed as:

$$L_{in} \geq \frac{DV_{in}}{2(VG)I_{O,\min} f_{sw}} \tag{37}$$

Considering the durations of charging C_1 and C_4, and discharging C_2, C_3, and C_O, and using Kirchhoff Current Law (KCL) in the operating modes, the capacitors are designed for $x\%$ voltage ripple as

$$C_1 \geq \frac{nI_O + (1 + m)(VG)I_O((1 - D) - (t_6 - t_5)f_{sw})}{2f_{sw}x\%V_{C1}} \tag{38}$$

$$C_2 \geq \frac{\frac{I_{LM,\max}}{2}(t_7 - t_5) - \frac{nI_O}{f_{sw}} - m(VG)I_O(t_7 - t_5)}{x\%V_{C2}} \tag{39}$$

$$C_4 \geq \frac{(I_{LM,\max} + (1 - 3m)(VG)I_O)(t_6 - t_5)}{2x\%V_{C4}} \tag{40}$$

$$C_3 \geq \frac{I_O}{x\%V_{C3}f_{sw}}, C_O \geq \frac{I_O(1 - \frac{\pi}{\omega_3}f_{sw})}{x\%V_O f_{sw}} \tag{41}$$

B. SOFT SWITCHING CONDITION

In the proposed converter, C_{S1} and C_{S2} provide ZVS for M_1 and M_2 at turn-off instants and are designed like any snubber capacitor. To obtain ZVZCS condition at the M_1 turn-on, C_{S1} should be fully discharged in mode 9. In this mode, after turning off D_1, the required current to discharge C_{S1} and charge C_{S2} is approximately supplied by $-(I_{LM,min} + I_{in})$and this current must be greater than zero. $I_{LM,min}$ equals $I_{LM} - \frac{\Delta I_{LM}}{2}$, in which I_{LM} is the L_M average current, and ΔI_{LM} is the L_M current ripple. Thus, ΔI_{LM} should be greater than $2(I_{LM} + I_{in})$. In the M_1 on-state, L_M is charged by C_1 thus:

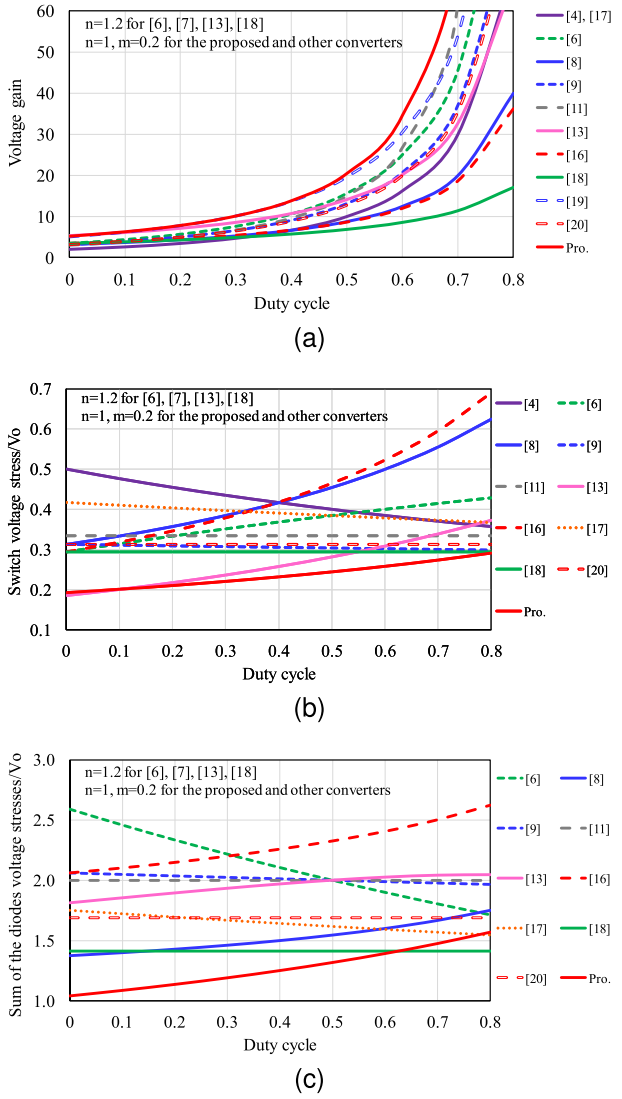

FIGURE 6. Comparison of (a) Voltage gain, (b) Switch voltage stress, (c) Sum of the diodes voltage stresses.

$$L_M \le \frac{V_{C1}D}{2(I_{LM}+I_{in})f_{sw}} \tag{42}$$

$$I_{LM} = (m+1)(1-D)I_{in} - (1+n+m)I_O \tag{43}$$

C. DESIGN PROCEDURE

The converter voltage gain and switch voltage stress are correlated to the D and CIs turns ratios. According to (12) and (13), achieving the required voltage gain by increasing the CIs turns ratios reduces the switches voltage stress thus, high quality with low-cost switches can be used. However, this leads to higher windings conduction loss, and larger magnetic core is needed. Thus, there is a trade-off between the switch cost, power density, and efficiency in selecting D and CIs turns ratio. One of the N_3 advantages is providing soft recovery for D_1 and D_2 and to reduce the winding conduction losses, m can be designed at a minimal amount. Then, to have a low switch voltage stress, D_{max} is obtained at $V_{in,min}$ from (44) and, n is determined from (45) to realize the desired VG.

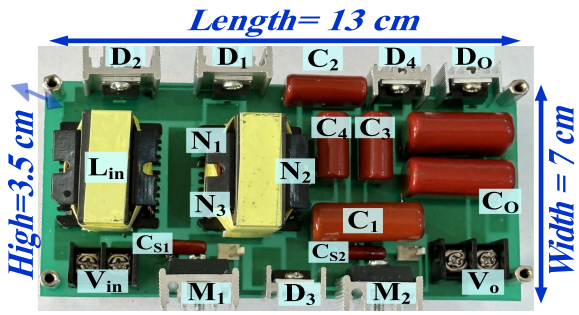

FIGURE 7. Proposed converter implemented prototype.

$$D_{\max} = \frac{(2+m) - \sqrt{m^2 + 4(1+m)\frac{V_{in,\min}}{V_{M1}}}}{2(1+m)} \tag{44}$$

$$n = \frac{\frac{V_O}{V_{M1}} - 3 + D_{\max} - m(1-D_{\max})}{2 - D_{\max}} \tag{45}$$

Regarding the above design process, the converter is designed for $V_O = 700V$ and $V_{in} = 42V - 52V$. To provide soft recovery for D_1 and D_2, and low copper loss, $m = 0.2$ is considered. In this design, to V_M lower than $200V$, an efficient operating point is $D = 0.5$ and $n = 0.5$. The suitable L_{in} to operate in CCM at 20% nominal load, and L_M to achieve soft switching for various D are indicated in Fig. 5. L_M and L_{in} are overdesigned and, capacitors are designed using (38)-(41) for less than 5% voltage ripple.

V. COMPARISON

To evaluate the proposed converter features over other high step-up structures, their main specifications are summarized in Table 1. Also, the converters voltage gain, switch voltage stress, and diodes voltage stress summation are compared in Fig. 6 which shows that the proposed converter is superior to all counterparts in these particularities. Meanwhile, only the proposed structure simultaneously has all the advantages of fully soft switching operation, solving the reverse recovery problem for all diodes, and eliminating the capacitive turn-on losses. Also, it maintains CG and low ICR, and its component count is competitive. In Fig. 6, for a fair comparison, the CIs turns ratio of the converters with one turns ratio is considered equal to the sum of all turns ratios in other converters.

Although the converters in [7], [9], and [10] have the same element number as the proposed converter, their VG is lower and higher voltage stress is imposed on their semiconductors. Moreover, the lack of CG in [5] and [10], and high ICR in [5] limit their applicability. Providing soft switching operation is an important feature to achieve high efficiency especially at high switching frequencies while the main drawback of the converters in [5], [7], [9], and [10] is hard switching operation.

TABLE II. Proposed Converter Prototype Specifications

Parameter	Specification
Input voltage: V_{in}	42-52 V (48 V nominal)
Output voltage: V_O	700 V
Output power: P_O	200 W
Switching frequency: f_{sw}	100 kHz
Switches: M_1, M_2	IRF250P225
Input diodes: D_1, D_2	VS-20CTQ150-M3
Diodes: D_3, D_4, D_O	MUR860
Capacitors: C_1, C_2, C_3	4.7, 2.2, 2.2 μF
Capacitors: C_4, C_O	2.2 μF, Two 4.7μF series
Snubber capacitors: C_{S1}, C_{S2}	4.3 nF
Input inductor: L_{in}	158 μH
Magnetizing inductance: L_M	30μH
Windings turns ratios: N_2/N_1, N_3/N_1	10/20, 4/20

Although the presented structures in [12] and [14] benefit from ZCS turn-on, capacitive turn-on and switching turn-off losses reduce efficiency. Soft switching operations contribute to high efficiency in [17], [18], [19], and [21], however high ICR limits the converter applicability in [17], and [18]. Also, the structure in [17] has the worst VG and switch voltage stress among the converters while employing a high number of switches leading to high cost and control complexity. The converters in [18], [19], and [21] improve the semiconductors voltage stresses however, their voltage gain is much lower than the proposed topology. Besides, the converter in [21] has three magnetic cores which increases the circuit volume. In the quadratic base converters, the high input current flows through the input side diodes thus, soft recovery for them is an important issue, but this is unsolved for the converters in [5], [7], and [9], [10], and [21].

VI. EXPERIMENTAL VERTIFICATION

To evaluate the converter performance, a laboratory prototype with the specifications listed in Table 2 is implemented as shown in Fig. 7. The experimental results are depicted in Fig. 8. The main and auxiliary switches waveforms in Fig. 8(a) and (b), validate the ZVS performance at full load. While Fig. 8(c) and (d) confirm ZVS at light load (40 W). Also, the experimental results switches voltage stress is consistent with the theoretical analysis. The diodes waveforms in Fig. 8(e)–(i) show that due to the leakage inductance, D_1 and D_2 turn off with low reverse recovery (LRR) problem, while all other diodes turn off at ZCS which enhances the converter performance. The input and output voltages in Fig. 8(j) acknowledge the intended voltage gain. Fig. 8(k) illustrates the converter response to load variations, transiting from full load to half load and vice versa. This confirms that the output voltage remains regulated and stable during the load changes. Fig. 9 depicts the converter efficiency at various loads and indicating almost 97% efficiency at a wide load range. Fully soft switching operation and the elimination of diodes reverse recovery losses have contributed to achieving high efficiency.

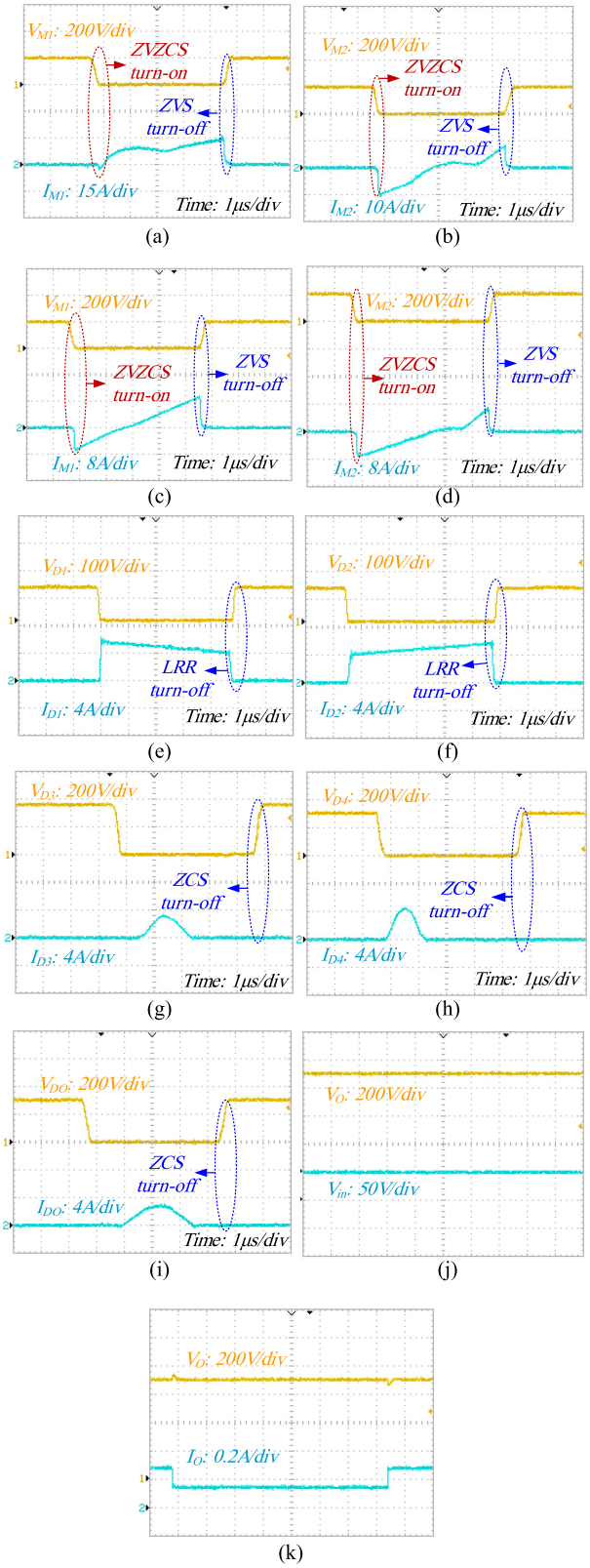

FIGURE 8. Experimental waveforms of (a) M_1 at full load, (b) M_2 at full load, (c) M_1 at light load, (d) M_2 at light load, (e) D_1, (f) D_2, (g) D_3, (h) D_4, (i) D_O, (j) V_{in} and V_O, and (k) Transient response to step load.

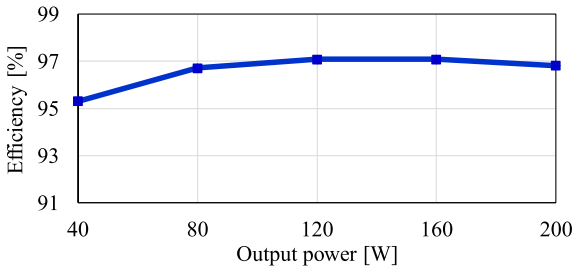

FIGURE 9. Efficiency for load variation from light load to full load.

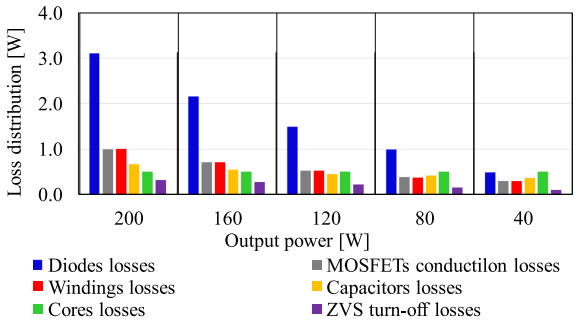

FIGURE 10. Proposed converter loss breakdown analysis for various P_O.

The elements participation in the converter losses at various powers is reported in Fig. 10.

VII. CONCLUSION

This paper presents a quadratic ultra-high step-up converter which is formed by a new combination of CIs, SCs, and active clamp methods with the basic structure. This novel configuration achieves low switch and sum of diodes voltage stresses relative to the other quadratic base converters. Also, it benefits from ZVS operation which eliminates the capacitive turn-on losses. The reverse recovery problem of the quadratic converters input diodes is a challenge that the proposed converter has overcome. Besides, the converter has sustained the basic structure advantages such as continuous input current and CG which expand its applicability. The converter is entirely analyzed, and its advantages are verified through comparison, experimental results, and efficiency evidence.

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