Delft University of Technology

Dynamic DC Voltage Enhancement for Modular Multilevel Converter Using Capacitor Voltage Ripple

Sande, Robin van der; Huwyler, Anna; Shekhar, Aditya; Bauer, Pavol

Important note
To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Dynamic DC Voltage Enhancement for Modular Multilevel Converter Using Capacitor Voltage Ripple

Robin van der Sande , *Graduate Student Member, IEEE*, Anna Huwyler, *Student Member, IEEE*, Aditya Shekhar , *Member, IEEE*, and Pavol Bauer , *Senior Member, IEEE*

Abstract—High-power flexible dc links employ modular multilevel converters (MMC) for compact active power redirection in medium and high voltage grids. During contingencies, such converters may need to provide an enhanced active power capacity to avoid overload in vulnerable grid locations. This article achieves this target by using the capacitor voltage ripple margin of the MMC submodules (SM) to enhance the dc voltage beyond the rated value. This voltage enhancement enables the enhanced active power capacity of the MMC while maintaining rated electro–thermal stresses on the components. Moreover, dynamically varying the dc side voltage reduces the MMC's circulating current, improving its operating efficiency. Because the average capacitor voltage is controlled to remain constant, the overall stresses and harmonic performance of the enhanced MMC remain the same as in the base case. In this article, the analytical expressions for the voltage and power enhancement limits are derived, revealing a dependence on the grid-injected reactive power. Furthermore, a controller is designed to achieve stable operation during transient conditions when the power enhancement is carried out. Finally, the enhancement concept is validated using simulations and experiments with a down-scaled laboratory MMC prototype.

Index Terms—AC–DC converter, active power capacity, modular multilevel converter (MMC), operational efficiency.

NOMENCLATURE

A. Abbreviations

EPS	Electric power system.
FSM	Finite state machine.
IGBT	Insulated-gate bipolar transistor.
MMC	Modular multilevel converter.
SM	Submodule.
THD	Total harmonic distortion.
VSC	Voltage source converter.

B. Symbols

C_{sm}	Submodule capacitance.
C_d	DC side capacitance.
$E_{c,u}^{\Sigma}, E_{c,l}^{\Sigma}$	Upper and lower arm energy.
$\Delta E_{c,u}^{\Sigma}, \Delta E_{c,l}^{\Sigma}$	Upper and lower arm energy ripple.
i_c	Circulating current.
i_d	DC side current.
i_u, i_l	Arm current of upper and lower arm.
$i_{s,j}$	Output current of phase $j \in \{a, b, c\}$.
i_{sw}	Submodule switch current.
k_d	Voltage enhancement factor.
$k_{d,max}$	Voltage enhancement factor boundary.
k_i	Current reduction factor.
k_p	Power enhancement factor.
L	Arm inductance.
N	Number of submodules per arm.
P	AC side active power.
P_d	DC side power.
P_{dr}	Rated dc side power.
Q	AC side reactive power.
R	Arm resistance.
$\tau_Q, \tau_{kd}, \tau_P$	Controller waiting time parameters.
ϕ	Phase angle.
v_c	Submodule capacitor voltage.
$v_{c,u}^{\Sigma}, v_{c,l}^{\Sigma}$	Upper and lower arm sum capacitor voltage.
$\Delta v_{c,u}^{\Sigma}, \Delta v_{c,l}^{\Sigma}$	Arm sum capacitor voltage ripple.
V_d	DC side voltage.
V_{dr}	Rated dc side voltage.
$v_{g,j}$	Grid voltage of phase $j \in \{a, b, c\}$.
V_{opm}	Operating margin voltage.
v_s	Output voltage.
V_{space}	Spacing voltage.
v_u, v_l	Arm voltage of upper and lower arm.
V_x	Adapted spacing voltage.
ω	Grid frequency.
X_c	Arm impedance.

I. INTRODUCTION

THE MMC is a promising technology that can serve as the interface between a medium-voltage ac grid and a dc network. The MMC offers efficient energy conversion with outstanding harmonic performance, while its modular and scalable design ensures a highly reliable and fault tolerant operation [1], [2], [3], [4]. The fundamental concept of the MMC was first proposed in [5] and later extended for wide power applications in [6]. Various applications of medium to high voltage grid-connected MMCs, including battery energy storage

systems, static synchronous compensators, and motor drives, are discussed in [7].

When the MMC serves as an interface, the power balance between the ac and dc side of the converter is maintained by the SM capacitors. The charge balance of these capacitors relies on the positive and negative half-cycles of the ac output voltage [8]. The resulting capacitor voltage ripple is then directly proportional to the operating power of the converter, with the designed maximum value occurring under rated conditions. This maximum ripple determines the energy storage requirements of the MMC, impacting both the semiconductor and capacitor costs [9], [10].

During operation, the average SM capacitor voltage is determined by the MMC's dc voltage and regulated through the arm energy controller [11]. Meanwhile, the fundamental frequency component of the arm current, which is related to the MMC's output power, is responsible for the alternating components in the SM capacitor voltage [12]. Then, as long as the inserted arm voltage of the MMC, required to maintain operation, is less than the available sum capacitor voltage, the ac and dc side operations are decoupled.

This decoupling imposes a degree of freedom in setting the converter's operating dc voltage and/or average capacitor voltage. A first concept that uses this freedom is proposed in [13] for variable-speed drives. The authors reduced the MMC's average capacitor voltage below the dc voltage to accommodate a higher voltage ripple when the motor operates below the based speed, thereby decreasing the inverter's switching losses. A further capacitor voltage reduction was achieved using harmonic injection techniques as proposed in [14] and [15].

However, for MMCs interfacing medium and high voltage grids, conduction losses are dominant as compared to switching losses [16]. Consequently, a dc voltage enhancement should be preferred over an average capacitor voltage reduction for medium-voltage high-power grid applications with given operating conditions. Accordingly, the ac/dc side decoupling can be utilized to achieve a dc voltage enhancement while keeping the average capacitor voltage and consequently the stresses/overall ratings of the converter components fixed [16]. Following [17], it can be inferred that the achievable dc voltage enhancement changes with the operation point of the MMC, making the voltage enhancement a dynamic property. An extension to this method was proposed in [18], where third harmonic injection was used to increase the MMC's dc voltage by 13.4% without altering the capacitor voltage or the number of SM. However, the authors highlighted the need for increased galvanic isolation of the converter station and dc cable, further requiring an interfacing Y/Δ transformer to eliminate the zero-sequence output current.

While the concept of using a dynamic dc voltage to benefit the system operation has been considered for MMC-based solid-state transformers in [19] and back-to-back configured hybrid MMCs in [20], both methods dynamically adjust the converter's dc voltage below the base value. In contrast, this article introduces a method for dynamically enhancing the dc voltage of an MMC beyond the rated value by utilising the power-dependent ripple in the capacitor voltage, thereby preserving the converter's
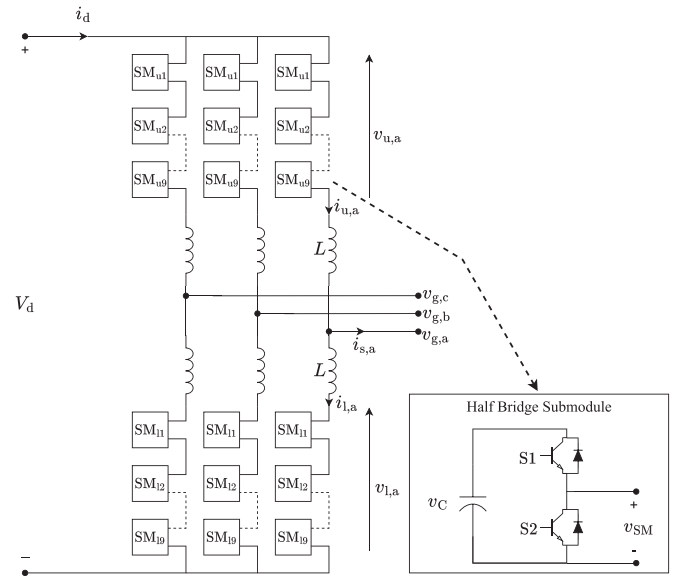

Fig. 1. Circuit diagram of the 10-level three-phase MMC.

ac side harmonic performance and maintaining rated SM voltage stresses through the control of the average capacitor voltage. While this voltage enhancement directly benefits the converter's efficiency, the active power capacity of the MMC can also be enhanced for a given electro–thermal rating of the components, which is beneficial for active power redirection during (N-1) grid contingencies. This enhancement method can be applied to point-to-point MMC-based dc links in medium/high-voltage grids such as the ones in [21], [22], [23]. These links adhere to HVDC regulations, like [24], that require the system to operate in a voltage range (e.g., 0.85–1.11 p.u. in continental Europe). However, wider voltage ranges may be permitted if economically and technically feasible. The rest of this article is organized as follows:

1) Derive the analytical expressions for the voltage enhancement and active power enhancement limits (see Section III).
2) Develop a control framework to achieve the dynamic dc voltage and active power enhancement as a function of the varying reactive power reference (see Section IV).
3) Simulate the transient behavior, SM stresses (average/ripple), and the harmonic performance of the MMC with the proposed enhancement algorithm (see Section V).
4) Validate the proposed concepts experimentally using a laboratory-scale MMC (see Section VI).

Finally, Section VII concludes this article.

II. SYSTEM DESCRIPTION

Fig. 1 presents the circuit diagram of a 10-level, three-phase MMC in a double-star configuration [1]. This 10 MW MMC serves as the interface between a 10 kV ac grid and a dc bus. The converter comprises three phase-legs, each consisting of an upper and a lower arm, which are formed with niner series-connected half-bridge SM and a $100\,\mu$H arm inductance. The SM

		Simulation	Experiments
Control frequency (kHz)	f_c	10.0	5.0
Switch frequency (kHz)	f_s	0.313	5.0
AC side:			
Grid frequency (rad/s)	ω	314.2	314.2
Grid voltage L-N (V)	v_g	5770	33.7
Grid inductance (μH)	L_g	287	-
Grid resistance (mΩ)	R_g	9.0	-
DC side:			
Rated dc side voltage (V)	V_{dr}	17100	100
Constant Power Load (W)	P_d	-	330
MMC:			
Rated apparent power (VA)	S_{max}	11e^6	607
Submodule capacitance (mF)	C_{sm}	3.3	5.0
DC side capacitance (μF)	C_d	100	-
Number of arm submodules	N	9	4
Arm inductance (mH)	L	4.0	2.4
Arm resistance (Ω)	R	0.1	0.06
Maximum output current (A)	$i_{s,max}$	641	6.0

are constructed using two 3.3 kV IGBT switches and a 3.3 mF capacitor. To ensure compliance with the maximum modulation index of 0.95, the rated dc side voltage V_{dr} is set at 17.1 kV [25]. Regulating the MMC is a cascaded controller derived from [26]. The converter and grid parameters used in simulations, as well as experiments, are provided in Table I.

III. ENHANCEMENT METHODOLOGY

During conventional operation, the dc side voltage V_d of the MMC is fixed at the rated value V_{dr}. However, in an enhanced operation, this dc voltage can be operated beyond the rated condition, as given in (1), where the voltage enhancement factor $k_d > 1$. To maintain the MMC's operating performance and reliability, both the SM stresses and converter's ac side harmonic character must be preserved. This requires the average MMC arm energy to be fixed at the rated condition and demands conservation of the sinusoidal output voltage waveform v_s throughout the enhancement process

$$V_d = k_d V_{dr}. \tag{1}$$

Operating the MMC at an enhanced dc side voltage V_d while maintaining the rated output power P_{dr} reduces the dc side current i_d. This lower dc current reduces the MMC's average circulating current, improving the operating efficiency of the converter. Alternatively, operating at an enhanced dc side voltage while maintaining rated switch current condition improves the active power capacity of the MMC. Therefore, while keeping the average arm energy constant, a capacity enhancement is achieved with the same SM switch and capacitor voltage rating.

A. DC Voltage Enhancement

The dc voltage enhancement considers two crucial MMC quantities: the arm voltage v_u, v_l and the sum capacitor voltage $v_{c,u}^\Sigma, v_{c,l}^\Sigma$. The upper arm voltage is defined as the potential across the arm submodule string and is characterized by (2). v_u retains a common-mode phase-leg voltage of $\frac{1}{2}V_d$ and a sinusoidal output

voltage of $\hat{v}_s \cos(\omega t)$

$$v_u(t) = \frac{k_d V_{dr}}{2} - \hat{v}_s \cos(\omega t). \tag{2}$$

The sum capacitor voltage is defined as the sum of the SM capacitor voltages in the respective arm. To preserve the SM voltage stresses throughout the enhancement, the average sum capacitor voltage $\bar{v}_{c,u}^\Sigma$ is kept at the rated condition. This is achieved by regulating the average SM capacitor voltage $\bar{v}_c$ to a constant value corresponding to the rated dc side voltage V_{dr}, as given follows:

$$\bar{v}_c = \frac{V_{dr}}{N}. \tag{3}$$

Since the submodule capacitor and switches are primarily dimensioned in accordance to $\bar{v}_c$, the average arm energy $\bar{E}_{c,u}^\Sigma$ is controlled to a constant magnitude given as follows:

$$\bar{E}_{c,u}^\Sigma = \frac{C_{sm} V_{dr}^2}{2N}. \tag{4}$$

The fluctuations in the SM capacitor voltage can be identified as energy exchanges between the upper and lower MMC arm at the fundamental frequency ω and between the MMC leg and the grid at 2ω [26]. This arm energy ripple is studied in [11], where the authors propose differential (5), assuming a negligible arm resistance. In this equation, i_c is the circulating current, and $\hat{i}_s \cos(\omega t - \phi)$ is the sinusoidal output current, with ϕ the phase angle between the output voltage and output current and $\hat{i}_s$ the output current amplitude

$$\frac{\delta E_{c,u}^\Sigma}{\delta t} = i_u v_u = \left(\frac{\hat{i}_s}{2} \cos(\omega t - \phi) + i_c \right) \left(\frac{V_d}{2} - \hat{v}_s \cos(\omega t) \right). \tag{5}$$

The ripple in the upper arm energy $\Delta E_{c,u}^\Sigma$ is obtained by integrating both sides of (5) while assuming a steady-state power balance. The result is expressed in (6). Following (6), it is observed that $\Delta E_{c,u}^\Sigma$ depends on the operating active power P and reactive power Q of the MMC.

$$E_{c,u}^\Sigma(t) = \bar{E}_{c,u}^\Sigma + \frac{V_d \hat{i}_s}{4\omega} \sin(\omega t - \phi) - \frac{\hat{v}_s i_c}{\omega} \sin(\omega t) \cdots$$
$$- \frac{\hat{v}_s \hat{i}_s}{8\omega} \sin(2\omega t - \phi) = \bar{E}_{c,u}^\Sigma + \Delta E_{c,u}^\Sigma(t). \tag{6}$$

The upper arm sum capacitor voltage $v_{c,u}^\Sigma$ is derived from the average arm energy and arm energy ripple, and is approximated in (7), following [26].

$$v_{c,u}^\Sigma(t) \approx V_{dr} + \frac{N}{C_{sm} V_{dr}} \Delta E_{c,u}^\Sigma(t). \tag{7}$$

Combining (1), (6), and (7) and simplifying the result gives (8), which defines the regulated upper arm sum capacitor voltage under the dc voltage enhancement. With $X_c = \frac{N}{C_{sm}\omega}$ defined as the MMC arm impedance

$$v_{c,u}^\Sigma(t) = V_{dr} + \frac{X_c}{8 V_{dr}} \Big(2 k_d V_{dr} \hat{i}_s \sin(\omega t - \phi) \cdots$$
$$- 8 \hat{v}_s i_c \sin(\omega t) - \hat{v}_s \hat{i}_s \sin(2\omega t - \phi) \Big). \tag{8}$$
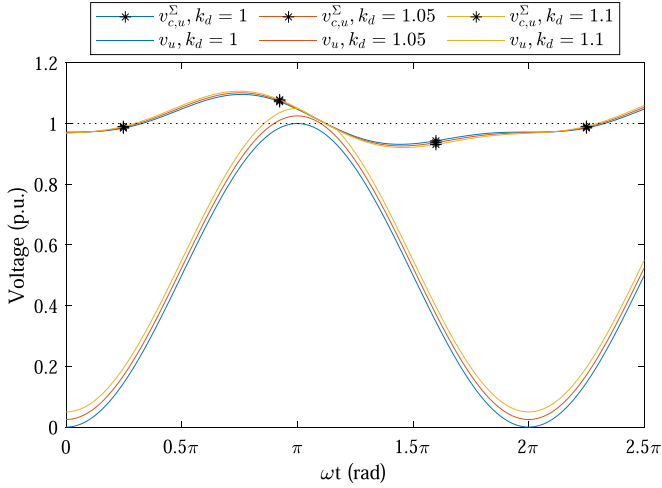
Fig. 2.   MMC arm voltages in steady state for three voltage enhancement factors operating at pf = 0.95.

Using the analytical expressions of (2) and (8), the enhancement process can be visualized as in Fig. 2. This figure contains the sum capacitor voltage and the corresponding upper arm voltage for three indicative values of the enhancement factor k_d. In Fig. 2, V_{dr} is considered as 1 p.u.

For $k_d = 1.0$, the ripple component in $v_{c,u}^{\Sigma}$, caused by the arm's energy exchange, creates a positive margin between $v_{c,u}^{\Sigma}$ and v_u near $\omega t = \pi$. This margin can be used to bias v_u while avoiding an intersection with $v_{c,u}^{\Sigma}$. The dc component of v_u is then enhanced by a factor k_d, which causes an increase in the dc side voltage to $V_d = k_d V_{dr}$. However, as observed in Fig. 2, the voltage enhancement is limited by the intersection of v_u with $v_{c,u}^{\Sigma}$. As $v_{c,u}^{\Sigma}$ represents the available arm voltage, v_u must saturate at $v_{c,u}^{\Sigma}$. Any intersection of the two introduces high-frequency arm voltage components, degrading the MMC's output harmonic performance. Moreover, this distortion can lead to a stability issue in the converter operation [27].

The dc voltage enhancement thus maximizes the use of available power-dependent ripple margin between $v_{c,u}^{\Sigma}$ and v_u by increasing the control parameter k_d. However, the preservation of the MMC's harmonic performance imposes a limitation on k_d that is expressed in the enhancement constraint of the following:

$$v_{c,u}^{\Sigma}(t) - v_u(t) = \Delta V_{\text{margin}}(t) > 0. \tag{9}$$

Substituting (2) and (8) in (9) while assuming the maximum modulation index $m = 1$, defines the value of the available ripple margin ΔV_{margin} as follows:

$$\Delta V_{\text{margin}}(t) = V_{dr}\left(1 - \frac{k_d}{2}\right) + \frac{V_{dr}}{2}\cos(\omega t) + \cdots$$

$$\frac{X_c}{8}\left(2k_d \hat{i}_s \sin(\omega t - \phi) - 4i_c \sin(\omega t) - \frac{\hat{i}_s}{2}\sin(2\omega t - \phi)\right). \tag{10}$$

Now combining constraint (9) with the ripple margin expression of (10) and rearrange for k_d leads to the inequality

expression given as follows:

$$k_d < 2 + \cos(\omega t) + \frac{X_c}{4V_{dr}}\left(2k_d \hat{i}_s \sin(\omega t - \phi) \cdots\right.$$

$$\left. - 4i_c \sin(\omega t) - \frac{\hat{i}_s}{2}\sin(2\omega t - \phi)\right). \tag{11}$$

The maximum feasible dc voltage enhancement is defined by the minimum value obtained in the RHS of (11). As implied by Fig. 2, this occurs near time-point $\omega t = \pi$ because physically, this represents the moment at which the inserted arm voltage $v_u(t)$ is at its maximum. Thus, substituting $\omega t = \pi$ into (11) provides the boundary for the voltage enhancement factor $k_{d,\text{max}}$ as described by the following:

$$1 \le k_d < \underbrace{1 + \frac{\left(\frac{\hat{i}_s}{2}\right)\sin(\phi)X_c}{V_{dr}}\left(k_d + \frac{1}{4}\right)}_{k_{d,\text{max}}}. \tag{12}$$

Physically, (12) suggests that $k_{d,\text{max}}$ is proportional to the voltage drop across the arm impedance X_c due to the reactive arm current component $(\frac{\hat{i}_s}{2})\sin(\phi)$. Therefore, it can be inferred that enhancement of the dc side voltage is positively correlated with the grid-injected reactive power Q and independent of the active power of the converter. This observation can be supported by rearranging (12) into the closed form solution (13) and recognizing that $\hat{i}_s \sin(\phi) = 4Q/3V_{dr}$ at the maximum modulation index $m = 1$. The resulting equation, given in (14), is a monotonically increasing function of Q, causing the voltage enhancement boundary to extend with a higher grid-injected reactive power. Meanwhile, for a grid absorption of reactive power $Q < 0$, the voltage enhancement factor $k_d = 1$, representing no voltage enhancement

$$1 \le k_d < \frac{8V_{dr} + \hat{i}_s \sin(\phi)X_c}{8V_{dr} - 4\hat{i}_s \sin(\phi)X_c} \tag{13}$$

$$1 \le k_d < \frac{6V_{dr}^2 + QX_c}{6V_{dr}^2 - 4QX_c} = k_{d,\text{max}}. \tag{14}$$

The impact of (14) on the proposed 10 MW MMC is provided in Fig. 3. This figure shows the voltage enhancement factor boundary $k_{d,\text{max}}$ as a function of the grid-injected active and reactive power. Note that for an absorption of reactive power $Q < 0$ (a capacitive grid), the voltage enhancement factor is constant $k_{d,\text{max}} = 1$. In addition, the waveforms of v_u and $v_{c,u}^{\Sigma}$ are provided for the MMC operating in rectification mode (−9.9 MW, 4.8 MVAr) as well as in inversion mode (9.9 MW, 4.8 MVAr). For both operation points, a dc side voltage enhancement of 13.8% is applied, as per (14). Following Fig. 3, it is concluded that $k_{d,\text{max}}$ increases with the grid-injected reactive power while remaining independent of the MMC's active power level. Although the active power influences the capacitor voltage waveform outside the constraining time-point $\omega t = \pi$, near this point, $v_{c,u}^{\Sigma}$ is defined by the reactive power level. Consequentially, the maximum voltage enhancement of an MMC is identical in the rectification and inversion mode.
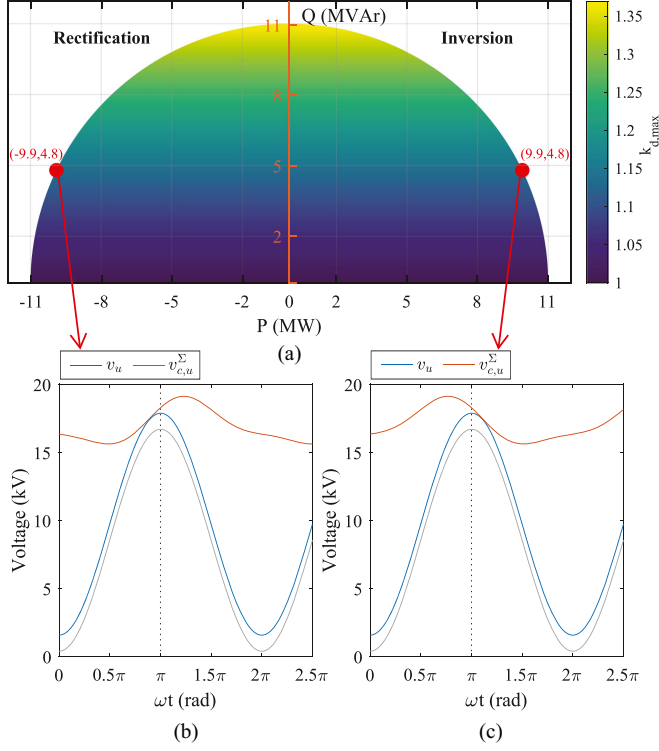
Fig. 3. Voltage enhancement factor boundary of the 10 MW MMC as a function of $\{P, Q\}$ in (a). With the MMC arm voltage and sum capacitor voltage waveforms given in (b) for the $\{-9.9\text{ MW}, 4.8\text{ MVAr}\}$ rectification and (c) for the $\{9.9\text{ MW}, 4.8\text{ MVAr}\}$ inversion. Both are operated with $k_d = 1.138$.

B. Active Power Enhancement

The dc voltage enhancement at rated power P_{dr} reduces the dc current i_d and consequently lowers the circulating current i_c in the MMC. As the SM switches are subjected to switching stresses proportional to the arm current, the reduction in i_c can be utilized to increase the operating active power P_d beyond P_{dr}. To reflect the SM switching stresses, the peak switch current $\hat{i}_{sw}$ is given as follows:

$$\hat{i}_{sw}(k_d) = \hat{i}_u = \frac{\hat{i}_s(k_d)}{2} + \frac{i_d(k_d)}{3}. \tag{15}$$

Throughout the enhancement process, the switching stresses and, thus, the peak switch current must be kept at the rated value. To sustain this requirement, $\hat{i}_{sw}$ should remain unaffected by the change in k_d. Taking the derivative of (15) and following the requirement defines expression as follows:

$$\frac{1}{2}\frac{\partial \hat{i}_s(k_d)}{\partial k_d} = -\frac{1}{3}\frac{\partial i_d(k_d)}{\partial k_d}. \tag{16}$$

In steady-state conditions, the total stored energy in the MMC is fixed. Based on the law of conservation of power, it must hold that $P_{ac} = P_d$, which prescribes as follows:

$$V_d i_d = \frac{3}{2}\hat{v}_s \hat{i}_s \cos(\phi). \tag{17}$$

Throughout the enhancement process, V_d is defined as a function of the voltage enhancement factor, given by (1). Meanwhile

the output voltage is assumed to remain constant at $\hat{v}_s = \frac{1}{2}m_a V_{dr}$. Where m_a is defined as the rated amplitude modulation index. Substituting both in (17) gives the following:

$$k_d V_{dr} i_d = \frac{3}{4}m_a V_{dr}\hat{i}_s \cos(\phi). \tag{18}$$

Rearranging (18) and expressing for $\hat{i}_s$ gives the following:

$$\hat{i}_s = \frac{k_d i_d}{\frac{3}{4}m_a \cos(\phi)}. \tag{19}$$

To achieve the MMC active power enhancement with constant switching stresses, both (16) and (19) must apply in steady-state. Therefore, substituting (19) into (16) and simplifying gives the following:

$$\frac{1}{\frac{1}{2}m_a \cos(\phi)}\left(i_d + k_d \frac{\partial i_d(k_d)}{\partial k_d}\right) = -\frac{\partial i_d(k_d)}{\partial k_d}. \tag{20}$$

Equation (20) can be restructured into (21), representing a first-order linear differential equation. This differential equation is used to find the expression for $i_d(k_d)$ as given in (22). In (22), C_1 represents the constant of integration

$$\frac{\partial i_d(k_d)}{\partial k_d} + \frac{1}{k_d + \frac{1}{2}m_a \cos(\phi)}i_d = 0 \tag{21}$$

$$i_d(k_d) = C_1 \cdot e^{-ln|k_d + \frac{1}{2}m_a \cos(\phi)|}. \tag{22}$$

At the rated condition, the dc side current is fixed at the nominal value i_{dr}. Applying this known condition to (22) provides an analytical expression for C_1. As a result, the dc side current i_d can be expressed as function of k_d, i_{dr}, m_a, and ϕ, as given in (23). This expression defines the maximum dc current under the voltage enhancement when $\hat{i}_{sw}$ is clamped at the rated condition. In (23) k_i is the dc current reduction factor

$$i_d(k_d) = i_{dr}\underbrace{\left(\frac{1 + \frac{1}{2}m_a \cos(\phi)}{k_d + \frac{1}{2}m_a \cos(\phi)}\right)}_{k_i}. \tag{23}$$

Combining (1) and (23) defines the expression for the maximum power enhancement under the operating voltage enhancement, as given in (24), where k_p represents the power enhancement factor

$$P_d(k_d) = P_{dr}\underbrace{\left(\frac{k_d(1 + \frac{1}{2}m_a \cos(\phi))}{k_d + \frac{1}{2}m_a \cos(\phi)}\right)}_{k_p}. \tag{24}$$

Following (24), it can be concluded that k_p is a monotonically increasing function of k_d. This implies that for all operation points of the MMC, the maximum feasible power capacity enhancement $k_{p,max}$ is achieved at the maximum voltage enhancement $k_{d,max}$ corresponding to the given operating Q. Note that if k_d is operated beyond $k_{d,max}$, high-frequency components are injected into v_u, degrading the MMC's output harmonic performance. Moreover, if k_p is operated beyond $k_{p,max}$, the peak SM switch current will exceed the rated value, degrading the reliability of the MMC.
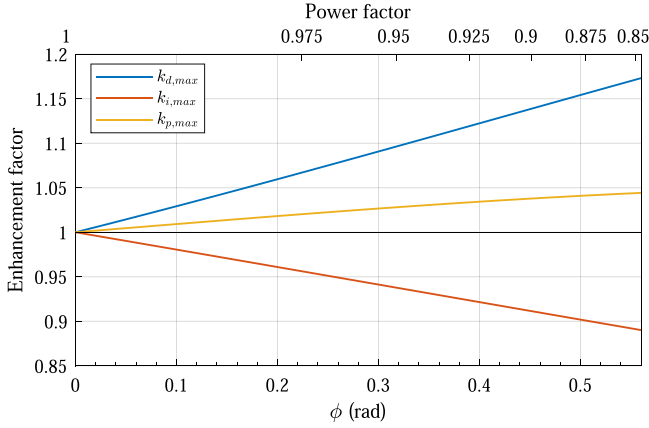
Fig. 4. Voltage enhancement, current reduction, and power enhancement factor limits of the 10 MW MMC as a function of the phase angle.
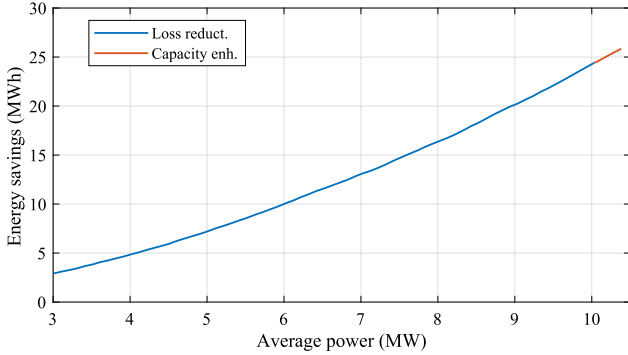

Fig. 5. Yearly energy savings of the dc voltage enhancement for the 10 MW MMC as a function of the average load profile for $Q = 4.5$ MVAr. The energy savings in capacity enhancement are with respect to a higher-rated MMC.

C. Enhanced MMC Operation

To further indicate the impact of the voltage and power enhancement on the proposed 10 MW MMC, Fig. 4 is provided. This figure shows the limit of the voltage and power enhancement factor, as well as the current reduction factor for different phase angles ϕ, as defined in (13), (24), and (23), respectively. The corresponding power factor of the MMC is provided on the top horizontal axis of Fig. 4. It is observed that, if the 10 MW MMC is operated at 0.9 power factor, the dc voltage can be enhanced by 13.9%, directly reducing the dc current by -12.2%. Alternatively, given the voltage enhancement, the active power capacity of the MMC can be extended with 3.78%, reducing i_d by -8.85%, as per Fig. 4. This all while preserving the SM stresses and maintaining the MMC's ac side harmonic performance.

Fig. 5 quantifies the impact of the voltage and power enhancement on the operating losses of the 10 MW MMC. The graph shows the yearly energy savings induced by the dc voltage enhancement when the MMC operates at a constant reactive power of 4.5 MVAr. It is observed that, for the MMC operating at 90% of the rated power, a yearly energy savings of 20.2 MWh can be achieved by employing the voltage enhancement. Using the power enhancement increases the MMC's active power

range to 10.4 MW while also achieving 25.8 MWh of yearly energy savings when compacted to a higher-rated MMC. In addition to the converter loss savings, the reduced i_d, imposed by the enhancement, can benefit the operating efficiency of the connected dc system. For a 10 MW MMC-based dc link that interfaces the grid at 0.9 pf, the dc cable conduction losses can be reduced by -22.9% and -16.9% for the voltage and power enhancement, respectively.

While the proposed enhanced MMC operation does provide a direct advantage for the efficiency and power transfer capacity of an existing MMC, it can also benefit future designs. Opting for a higher dc voltage rating (V_{dr}) during the design stage of an MMC will make the power/efficiency gain independent of the converter's operation point. However, this does require additional resources. The higher dc voltage rating would demand the MMC arms to contain additional SMs, and/or the SMs must be redesigned with a higher switch and capacitor voltage ratings. Both of these increase the cost and operating losses of the converter. In contrast, the dc voltage enhancement method benefits the MMC's efficiency/active power capacity at no added cost or increased operating losses.

D. Capacitor Voltage Ripple

Throughout the dc voltage enhancement, the average arm energy $\bar{E}_{c,u}^{\Sigma}$, $\bar{E}_{c,l}^{\Sigma}$ in the MMC is controlled to be constant in line with (4). However, the arm energy ripple $\Delta E_{c,u}^{\Sigma}$ changes with V_d, in line with (6). As a result the corresponding sum capacitor voltage ripple $\Delta v_{c,u}^{\Sigma}$ changes with k_d, as indicated in (25), that is derived from (6)

$$\Delta v_{c,u}^{\Sigma}(t) = \frac{X_c}{8V_{dr}} \big(2k_d V_{dr}\hat{i}_s \sin(\omega t - \phi) \cdots$$
$$- 8\hat{v}_s i_c \sin(\omega t) - \hat{v}_s \hat{i}_s \sin(2\omega t - \phi)\big). \quad (25)$$

The impact of (25) was observed in Fig. 2, which showed a minor increase in the peak-to-peak ripple of $v_{c,u}^{\Sigma}$ when k_d increased from 1.0 to 1.1. As $\bar{v}_{c,u}^{\Sigma}$ was controlled to V_{dr}, this added ripple caused a slight increase in the peak sum capacitor voltage $\hat{v}_{c,u}^{\Sigma}$ an therefore the peak SM capacitors voltage $\hat{v}_c$.

Fig. 6 shows the impact of the dc voltage enhancement on $\Delta v_{c,u}^{\Sigma}$ and $\hat{v}_{c,u}^{\Sigma}$ for the 10 MW MMC. It is observed that, for the MMC operating at a 0.9 power factor, the sum capacitor voltage ripple increases from 2.85 to 3.49 kV when k_d is enhanced from 1.0 to 1.14 ($k_{d,max}$). Meanwhile, the peak sum capacitor voltage is increased from 18.8 to 19.1 kV, causing a 1.6% increase of $\hat{v}_c$ compared to the rated operation. Note that, for the practical power factor range of [0.85,1], the dc voltage enhancement imposes a maximum rise in $\hat{v}_c$ of only 1.97%.

IV. CONTROL ALGORITHM

During operation, a grid-connected MMC must adhere to the active and reactive power reference $\{P_{in}, Q_{in}\}$ set by the EPS operator [28]. Following the methodology, a positive Q_{in} allows the MMC to be operated with an enhanced dc side voltage, reducing the MMC's losses, or with an enhanced dc voltage and active power, increasing the MMC's power capacity. Fig. 7
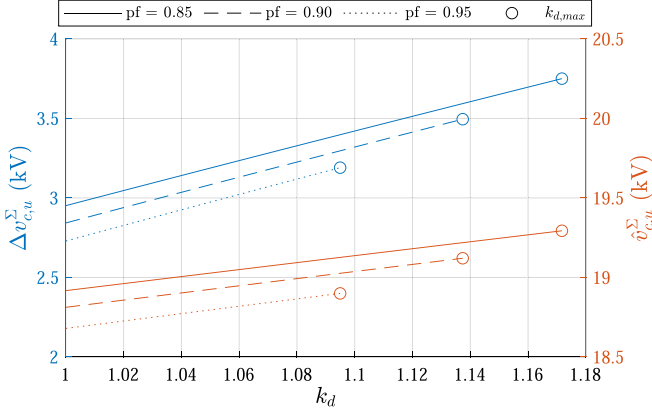
Fig. 6. Sum capacitor voltage ripple and peak sum capacitor voltage of the 10 MW MMC as a function of the enhancement factor for different pf.
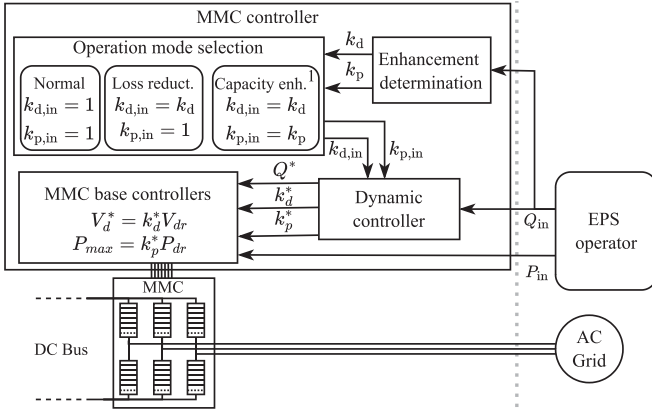

Fig. 7. Control framework for enhanced MMC operation providing a normal, loss reduction, and capacity enhancement operation mode. [1]Capacity enhancement is only performed in consultation with the EPS operator.

Fig. 8. FSM proposal for the dynamic controller.

provides a control framework for the enhanced operation of the MMC following the EPS operator's reference. This framework provides a normal, loss reduction, and capacity enhancement operation mode, by setting the voltage and power enhancement factor references $\{k_{d,in}, k_{p,in}\}$. Note that the capacity enhancement mode is only considered in consultation with the EPS operator. The control framework serves as an extension to the MMC base controller, like the ones proposed in [26] and [29].

Following (24), an enhanced active power operation $P_d > P_{dr}$ is admissible due to voltage enhancement $V_d > V_{dr}$. Meanwhile, $V_d > V_{dr}$ is admissible due to the presence of grid-injected reactive power $Q > 0$, in line with (14). This dependency imposes a strict dynamic order for changing V_d, P, and Q upon a reactive power reference change Q_{in}. For example, when the MMC operates in an enhanced state, an increase of Q can be performed directly. Though, only when Q has reached the steady-state value Q_{in}, V_d can be increased. Finally, upon the settlement of V_d, P can be enhanced. This process is reflected in (26). Any other sequence of changing the parameters can lead to an injection of output current harmonic components or an increase of the peak SM switch current. For a decrease in Q, the
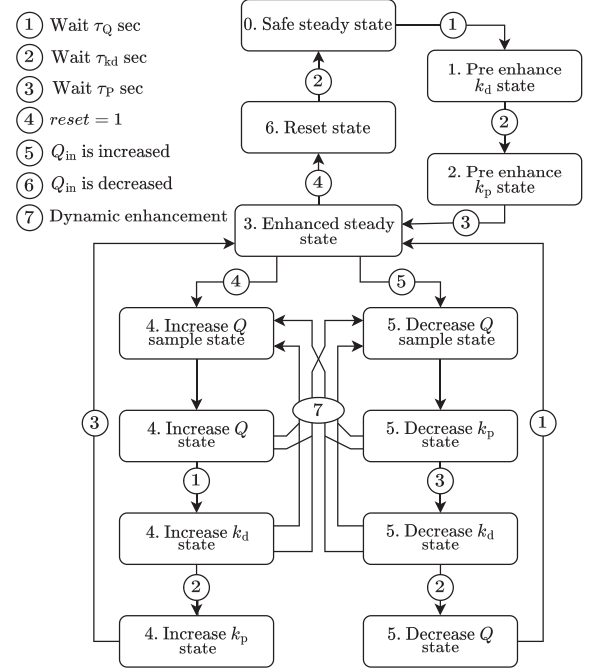
three parameters must be reduced in the reverse order of (26)

$$\text{Increase in } Q_{in} : [Q \uparrow] \Rightarrow [V_d \uparrow] \Rightarrow [P \uparrow]. \quad (26)$$

A feasible solution for managing the dynamic interdependence of V_d, P, and Q is to incorporate a dynamic control module between the operation mode selector and the MMC base controllers, as outlined in the control framework of Fig. 7. This dynamic control module, sets the reactive power reference Q^*, the voltage enhancement factor reference k_d^*, and the power enhancement factor reference k_p^* based on Q_{in}, $k_{d,in}$, and $k_{p,in}$. The sequence-based algorithm of the dynamic control module is implemented as a FSM, given in Fig. 8. This FSM poses an event-driven control method where state transitions are made conditional on the operating parameters of the MMC. The FSM is initialized in the *safe steady state*, which enforces the rated dc side voltage with $k_d^* = 1$, the rated maximum power $k_p^* = 1$, and sets $Q^* = Q_{in}$.

Once the MMC is initialized, the FSM transitions to the *enhanced steady state*. This transition involves, first, the enhancement of the dc side voltage to the reference value $k_{d,in}$ and, second, the enhancement of the power limit to the reference value $k_{p,in}$. Note that the state transitions are performed based on tuneable waiting-time parameters. In which τ_Q, τ_{kd}, and τ_P are set as the maximum step response time for a change in Q^*, V_d^*, and P^*, respectively.

In the *enhanced steady state*, three process transitions can be encountered. First, if the reset signal is triggered, the FSM transitions back to the *safe steady state* by lowering k_p^* and k_d^* to the rated value. Second, if Q_{in} is increased, the FSM transitions through the *increase Q sample state*, *increase Q state*, *increase k_d state*, and *increase k_p state*. In which it, respectively, samples Q_{in}, increases Q^* to Q_{in} while keeping k_d^* and k_p^* fixed, increases
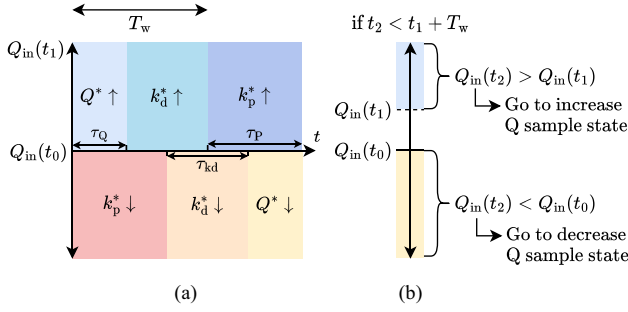
Fig. 9.   Dynamic controller algorithm with (a) the normal control concept and (b) the dynamic improvement for an increase Q transition.

k_d^* to the new reference value $k_{d,in}$ while keeping k_p^* fixed, and increases k_p^* to the new reference value $k_{p,in}$. The third process transition involves the decreased of Q_{in}, which has a structure similar to the increase transition, as shown in Fig. 8.

Observe in Fig. 8 that the dynamic constraint of (26) associated with the MMC enhancement is solved through the stepwise process of the control algorithm. This sequence-based control algorithm, that uses fixed waiting time τ_Q, τ_{kd}, and τ_P to respond to reference changes in Q_{in}, is further illustrated in Fig. 9(a). This figure indicates that the maximum response time of the proposed controller to a change in Q_{in} is $T_{res} = \tau_Q + \tau_{kd} + \tau_P$.

The design of the dynamic control module possesses a tradeoff between constraint compliance and the dynamic performance of the MMC. The proposed dynamic controller provides a stable and reliable solution, favoring output harmonic performance and SM stress preservation over a fast response time. Though, to improve the dynamic characteristic of the controller, state transitions are added to the wait states of the FSM, depicted in Fig. 8 by vector 7. If the controller encounters an input reference change, $Q_{in}(t_1) > Q_{in}(t_0)$, at time t_1, the FSM enters the increase Q transition. If a second reference change occurs while the FSM is waiting for the increase of Q or increase of k_d ($t_2 < t_1 + T_w$), a faster system response can be achieved. Following Fig. 9(b), if $Q_{in}(t_2) > Q_{in}(t_1)$ the FSM can re-enter the *increase Q sample state* directly. Alternately, if $Q_{in}(t_2) < Q_{in}(t_0)$ the FSM can transition directly into the *decrease Q sample state*. These transitions allow for faster input reference tracking and, thus, an improved dynamic performance of the controller.

V. SIMULATION VERIFICATION

A simulation model of the 10 kV-10 MW MMC is used to verify the analytical analysis of the dc voltage and active power enhancement. The MATLAB/Simulink model uses the parameters defined in Table I and is based on an arm-level averaged (ALA) model of the converter, as introduced in [26]. The simulations are used to demonstrate the dependence of the enhancement limit on the grid-injected reactive power, verify the voltage enhancement boundary expression, and analyse the steady state and dynamic performance of the MMC when applying the proposed control framework.

TABLE II
COMPARISON OF VOLTAGE ENHANCEMENT LIMITS

Q	$\hat{v}_s$	Analytical $k_{d,max}$	Simulated $k_{d,sim}$	Error
0 MVAr	8.16 kV	1.000	0.991	-0.86 %
1 MVAr	8.22 kV	1.025	1.020	-0.47 %
2 MVAr	8.28 kV	1.052	1.048	-0.17 %
3 MVAr	8.35 kV	1.079	1.081	+0.22 %

A. Enhancement Boundary

As concluded in Section III, the dc side voltage enhancement utilises the spacing between $v_{c,u}^\Sigma$ and v_u to enable the rise in V_d. This spacing was reflected in the available ripple margin expression $\Delta V_{margin}(t)$, as given in (9). The voltage enhancement was later found to be limited by the minimum value of $\Delta V_{margin}(t)$ obtained over a fundamental interval. This minimal spacing is defined as the spacing voltage V_{space} and is given in the following:

$$V_{space} = \min_{\omega t \in [0,2\pi]} (\Delta V_{margin}(t)). \tag{27}$$

For a practical rated operation of the MMC, the encountered spacing voltage is not fixed but depends on the operated P and Q. Following [30], the output voltage amplitude $\hat{v}_s$ of a VSC increases with the grid-injected reactive power. As derived in [30], $\hat{v}_s$ of an MMC can be expressed as a function of Q and the grid voltage amplitude $\hat{v}_g$, as given in (28). This derivation assumes a steady-state operation and uses the ac-side model of the MMC, where the arm inductance L is mapped to a grid filter inductance of $L/2$ as introduced in [26]. Following (28), it can be concluded that the output voltage amplitude of the MMC must exceed the grid voltage amplitude to inject the intended reactive power into the grid.

$$\hat{v}_s \approx \sqrt{\hat{v}_g^2 + \frac{2}{3}L\omega Q}. \tag{28}$$

This phenomenon is observed in the MMC simulations. Table II shows the simulated output voltage amplitude for different values of Q and a constant value of P at 10 MW. It is concluded that $\hat{v}_s = \hat{v}_g$ when the converter is operated at 0 VAr. Then for higher values of Q, the output voltage amplitude $\hat{v}_s$ increases beyond $\hat{v}_g$. Therefore, to meet required reactive power levels, the modulation index of a practical MMC is constrained to 0.95, consistent with [25].

To determine the voltage enhancement limit by simulation, the impact of the modulation index and varying output voltage amplitude must be isolated from the spacing voltage. To achieve this separation, the adapted spacing voltage V_x is proposed as an adjustment on V_{space}, which is illustrated in Fig. 10 for $k_d = 1$. This figure indicates that V_x is obtained from V_{space} by removing the initial spacing between the arm voltage and the average sum capacitor voltage. This spacing, denoted by V_{opm}, represents the operational margin of the MMC used to increase $\hat{v}_s$ beyond $\hat{v}_g$ to ensure the injection of Q. Removing this margin from V_{space}, causes the remainder to solely reflect the spacing created by the capacitor voltage ripple due to the injection of Q. To calculate V_x for $k_d > 1$, the operating margin voltage V_{opm} is represented by the spacing between the output voltage amplitude and half
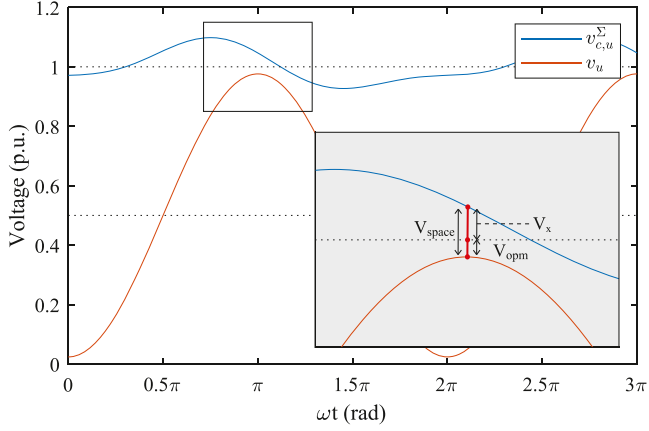
Fig. 10. Definition of the spacing voltage, adapted spacing voltage, and the operating margin voltage for $k_d = 1$.
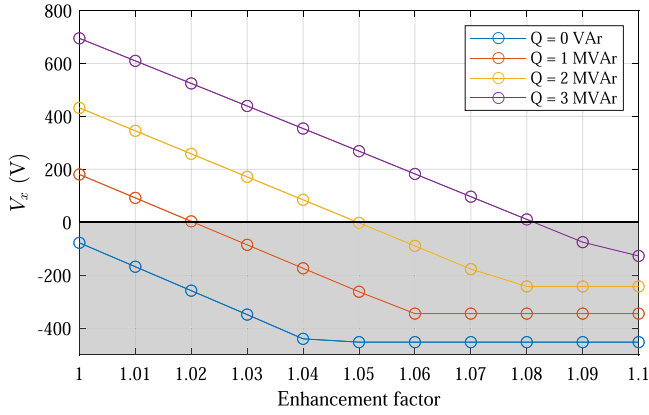

Fig. 11. Simulated V_x as a function of the operating enhancement factor for different values of injected reactive power. The gray area represent a nonfeasible operation region where the set operating margin is compromised.

the average sum capacitor voltage, as given in the following:

$$V_x = V_{space} - V_{opm} = V_{space} - \left(\frac{\overline{v}_{c,u}^{\Sigma}}{2} - \hat{v}_s \right). \qquad (29)$$

Fig. 11 shows the simulated adapted spacing voltage of the 10 MW MMC as a function of the operated enhancement factor, for different values of Q and a constant value of P at 10 MW. From Fig. 11, it can be concluded that a negative correlation is encountered between the enhancement factor k_d and the adapted spacing voltage V_x. In line with Fig. 2, this suggests that V_x is reduced in order to facilitate the rise in V_d. Furthermore, V_x is shown to be positively correlated with the operated reactive power. This implies that V_x increases with a larger injection of Q. Combining these two observations indicates that, for a fixed V_x, an increase in Q expands the operated voltage enhancement factor k_d. However, it is important to note that, the preservation of the rated MMC performance demands V_x to be non-negative. Otherwise, with $V_x < 0$, the voltage enhancement will be facilitated through a reduction of V_{opm}, which is critical during system transients and is used to ensure a steady-state injection of Q. Moreover, if $V_x = -V_{opm}$, steady-state output harmonic components are injected into the grid, further comprising the MMC

performance. Therefore, to ensure a proper voltage enhancement with conservation of the MMC performance, $V_x \geq 0$ must hold, rendering the grey area in Fig. 11 a nonfeasible operation region.

The zero crossing of the k_d-V_x curves in Fig. 11 indicates the value of k_d for which the dc side voltage enhancement begins to compromise the set operating margin in V_{space}. As any rise of k_d beyond this value increases the dc side voltage at the expense of V_{opm}, the zero crossing becomes a valid estimator of $k_{d,max}$. Table II contains both the analytical value $k_{d,max}$, from (14), and the simulated value $k_{d,sim}$. Comparing the analytical and simulated results implies that (14) accurately represents the feasible dc voltage enhancement of the 10 MW MMC. It is found that, for lower values of Q, (14) slightly overestimates the maximum voltage enhancement. However, the overall the accuracy is within $\pm 1\%$ of the actual value.

B. SM Stresses and Harmonic Performance

To examine the SM stresses and ac-side harmonic performance of the MMC throughout the voltage and power enhancement, Fig. 12 is provided. This figure shows the simulated active power P, reactive power Q, dc side voltage V_d, dc side current i_d, spacing voltage V_{space}, upper arm current i_u, peak SM switch current $\hat{i}_{sw}$, and the sum capacitor voltage $v_{c,u}^{\Sigma}$ all as a function of time. During the simulation, the MMC is enhanced using the dynamic controller of Section IV, which is initially operated with $Q_{in} = 0$ VAr in the *enhanced steady state*. Fig. 12 then indicates the response of the variables to a 4 MVAr rise in Q_{in} at $t = 0.2$ s when the waiting time parameters τ_Q, τ_{kd}, τ_P are fixed at 1.5 s. Practically, this additional injection of 4 MVAr can be demanded by the EPS operator to compensate for reactive power demand in medium voltage distribution grids [28], [31].

The first part of Fig. 12 shows the MMC's response to the 4 MVAr rise in Q_{in} at $t = 0.2$ s. It is observed that this operation point change increases V_{space} from 374 to 968 V, indicating the impact of Q on the capacitor voltage waveform, positively affecting the adjusted spacing voltage. Meanwhile, the peak SM switch current increases from 607 to 638 A, while the rms arm current rises from 350 to 368 A. Both the rise in $\hat{i}_{sw}$ and i_u are the result of the 0.8 MVA increase in apparent power (from 10 to 10.8 MVA), which is due to change in $\{P_{in}, Q_{in}\}$ as requested by the EPS operator. Therefore, 638 A and 368 A are the "pre-enhancement" values of $\hat{i}_{sw}$ and i_u, reflectively, as indicated by the dotted lines in Fig. 12.

The second part of Fig. 12 shows the response of the MMC to a 10% voltage enhancement at $t = 1.7$ s (k_d^* from 1.00 to 1.102). It is observed that for $t < 1.7$ s, both V_d and $v_{c,u}^{\Sigma}$ demonstrate quasi-steady state behavior at the rated value of 17.1 kV. Meanwhile, i_d is constant at 584 A to supply the active power of 10 MW. Note that in this rated condition, $\hat{i}_{sw}$ is 638 A while i_u is 368 A. After $t = 1.7$ s, V_d is enhanced to 18.9 kV while $v_{c,u}^{\Sigma}$ is kept at 17.1 kV. To facilitate this rise in dc voltage, it is observed that V_{space} is reduced to 112 V. Because the active power is maintained at 10 MW, the 10% voltage enhancement imposes a 10% reduction in i_d reaching 529 A. This 55 A decrease in i_d lowers the MMC's circulating current, thereby reducing the peak SM switch current to 620 A, which is 18.3 A
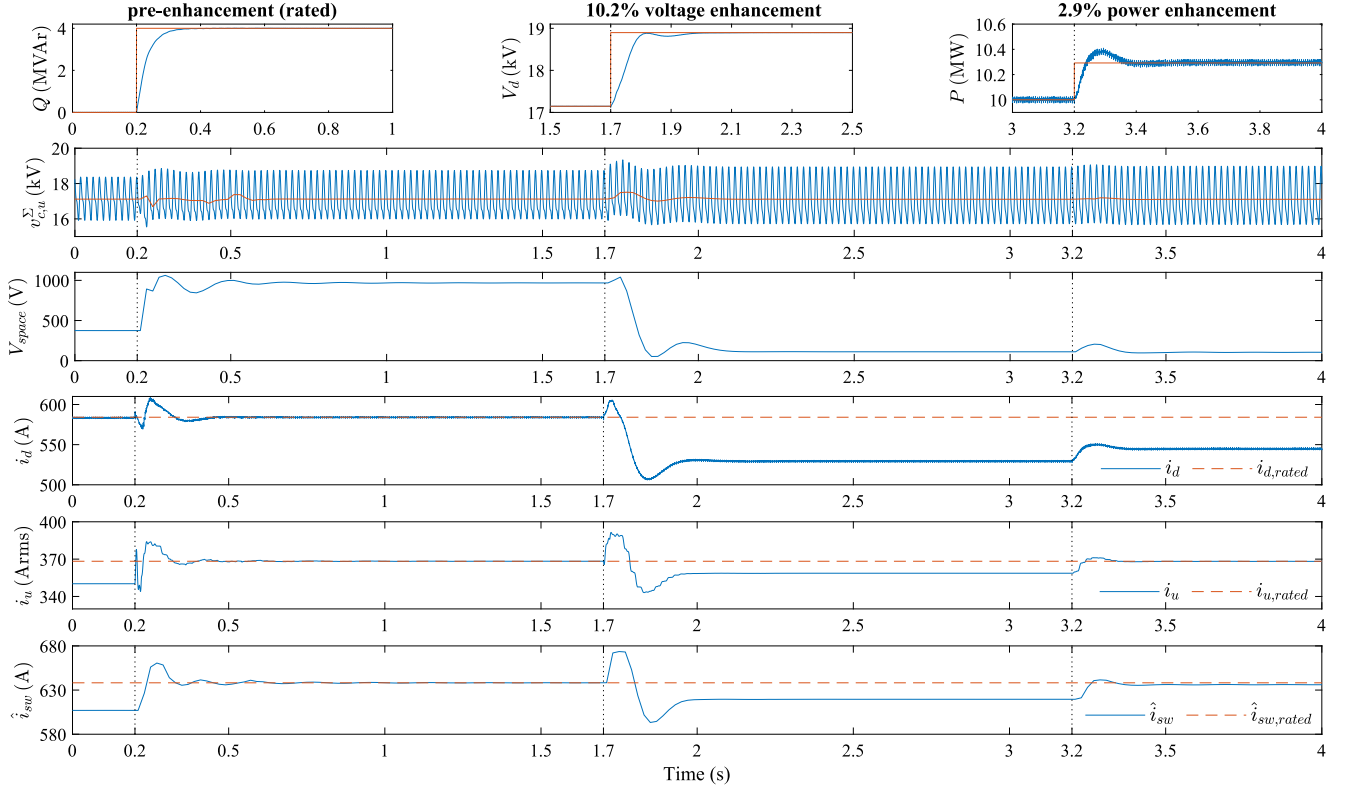
Fig. 12. Simulated response of the 10 MW MMC to an operation point shift at $t = 0.2$ s (Q_{in} from 0 to 4 MVAr) followed by a corresponding 10.2% dc side voltage enhancement at $t = 1.7$ s and 2.9% power enhancement at $t = 3.2$ s.

TABLE III
MMC STEADY-STATE PERFORMANCE: CURRENTS AND CAPACITOR VOLTAGES

Operation point:		Enhancement:			AC-side:		DC-side:	MMC currents:		MMC capacitor voltages:		
Q	S	Type	k_d	k_p	i_s (rms)	THD_i	i_d	i_u (rms)	$\hat{i}_{sw}$	Average $v_{cu,l}^\Sigma$	Ripple $v_{cu,l}^\Sigma$	$\Delta/\mu\ v_{cu,l}^\Sigma$
0 MVAr	10.0 MVA	No	1.0	1.0	582 A	0.445 %	584 A	350 A	607 A	17.12 kV	2.45 kV	14.3 %
4 MVAr	10.8 MVA	No (rated)	1.0	1.0	625 A	0.399 %	584 A	368 A	638 A	17.12 kV	2.75 kV	16.0 %
4 MVAr	10.8 MVA	Voltage	1.10	1.0	625 A	0.399 %	529 A	359 A	620 A	17.11 kV	3.22 kV	18.8 %
4 MVAr	11.1 MVA	Power	1.10	1.03	641 A	0.390 %	545 A	368 A	636 A	17.11 kV	3.30 kV	19.3 %

lower than the "pre-enhancement" value of 638 A. Moreover, the reduced i_d lowers the rms arm current to 359 A, reducing the MMC's conduction and switching losses, thereby enhancing the converter's efficiency. However, note that the dc voltage enhancement does impose a +2.8% higher capacitor voltage ripple.

The final part of Fig. 12 shows the response of the MMC to a 2.9% power enhancement at $t = 3.2$ s (k_p^* from 1.00 to 1.029). It is observed that P transitions from the rated to the enhanced value while the spacing voltage, dc side voltage, and average sum capacitor voltage remain nearly unaffected by the active power change. Consequently, to enable the rise in active power, i_d is increased to 545 A, imposing a higher dc circulating current component in the MMC. This, in turn, increases the rms arm current to 368 A and peak SM switch current to 636 A. However, note that i_u in the power enhanced mode equals the "pre-enhancement" value, indicating a preservation of conduction losses and therefore an improved converter efficiency. Moreover, observe that $\hat{i}_{sw}$ under the power enhancement remains below

the "pre-enhancement" value of 638 A, thereby preserving the MMC's SM switching stresses, in line with the requirement. This result follows the analysis of Section III, where k_p is selected to ensure preservation of $\hat{i}_{sw}$. However, note that the active power enhancement does increase the ripple in $v_{c,u}^\Sigma$ by an additional +0.5% when compared to the sole voltage enhancement.

The simulation results of Fig. 12 are summarized in Table III, which provides the MMC's steady-state performance for both the currents and capacitor voltages. Table III also provides the rms values and THD of the output current i_s. From Table III, it is noted that the THDi remains constant at 0.399% throughout the voltage enhancement and slightly reduces to 0.390% with the active power enhancement. This observation ensures the preservation of the ac side harmonic performance throughout the enhancement process. The rms value of the output current is observed to change in proportion to the apparent power of the MMC. With the active power enhancement, this increased i_s is however compensated by a lower i_d to maintain the rated arm current condition. Ultimately, this simulation verified that
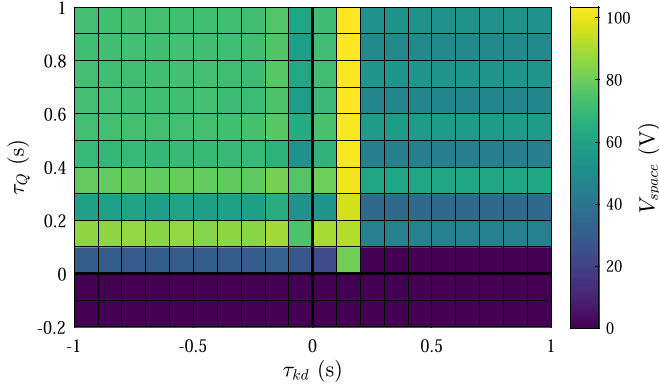
Fig. 13. Simulated minimal spacing voltage during the increase Q transition for various combinations of waiting time parameters.
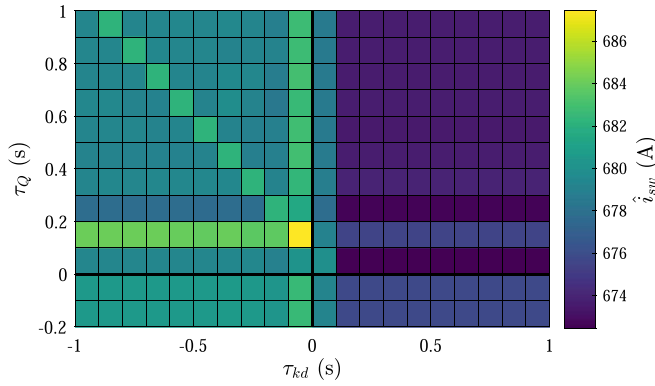

Fig. 14. Simulated peak switch current during the increase Q transition for various combinations of waiting time parameters.

Fig. 15. Experimental setup with MMC prototype.

10 MW MMC can accommodate both a 10% dc voltage enhancement and a 2.9% active power enhancement while preserving the SM switching stresses, and ac side harmonic characteristics of the MMC. The voltage enhancement then reduced the peak and rms value of the arm current, lowering the converter's conduction/switching losses and improving its efficiency. Alternatively, the power enhancement keeps the peak and rms value of the arm current at the rated condition, thereby increasing the MMC's active power capacity with rated converter losses.

C. Controller Feasibility

To analyze the feasibility and speed of the proposed control framework, the simulation of Fig. 12 is repeated for multiple values of the waiting time parameters τ_Q, τ_{kd}. The results are provided in Figs. 13 and 14, which show the minimum spacing voltage V_{space} and maximum SM switch current $\hat{i}_{sw}$ encountered during the increase Q transition, where Q_{in} increases from 0 to 4 MVAr. From Fig. 13, it can be concluded that for $\tau_Q < 0$ s, V_{space} hits a minimal value of 0 V during the increase Q process. This corresponds to an injection of high-frequency harmonics components in the output current of the MMC. From Fig. 14, it can be concluded that for $\tau_{kd} \leq 0$ s, $\hat{i}_{sw}$ is significantly higher compared to larger values τ_{kd}. Combined, these observations validate the necessity of the proposed controller, requiring

positive waiting times for the increase of k_d and k_p to preserve V_{space} and limit $\hat{i}_{sw}$, respectively. Furthermore, Figs. 13 and 14 show the speed of the proposed dynamic controller as $\tau_Q \geq 0.3$ s and $\tau_{kd} \geq 0.2$ s are required to maintain MMC performance. However, note that this speed depends highly on the characteristics of the MMC and its base controller.

VI. EXPERIMENTAL VERIFICATION

For further validation of the proposed dc voltage enhancement, an experimental setup is used with a down-scaled laboratory prototype MMC. The setup, demonstrated in Fig. 15, is composed of a three-phase 5-level MMC, a grid emulator functioning as an ac source, and a dc power load drawing a constant power of 330 W. The circuit parameters of the experimental setup are summarized in Table I. The performed experiments are used to verify the workings of the enhancement and provide reasonable proof for the feasibility of the enhancement concept on a medium voltage dc setup as proposed in Section II. In addition, an estimation of the voltage enhancement boundary is obtained to approximate (14) experimentally. Finally, the transient performance of the proposed dynamic control module is measured and compared to a direct enhancement.

A. Arm Voltages

Using the laboratory setup, the dc side voltage V_d, phase-a upper arm voltage v_u, and corresponding sum capacitor voltage $v_{c,u}^{\Sigma}$ are measured. The experimental results are provided in the scope plot of Fig. 16, which contains the measured voltages at rated condition $\{V_{d,1}, v_{u,1}, v_{c,u,1}^{\Sigma}\}$ and at a 6% dc voltage enhancement $\{V_{d,2}, v_{u,2}, v_{c,u,2}^{\Sigma}\}$. For this measurement, the MMC was operated at a constant active power of 330 W and supplied 200 VAr reactive power to the ac source.

In Fig. 16, it can be observed that the 6% rise of $V_{d,1}$ to $V_{d,2}$ results in the biasing of $v_{u,1}$ to $v_{u,2}$. $v_{u,2}$ maintains the sinusoidal
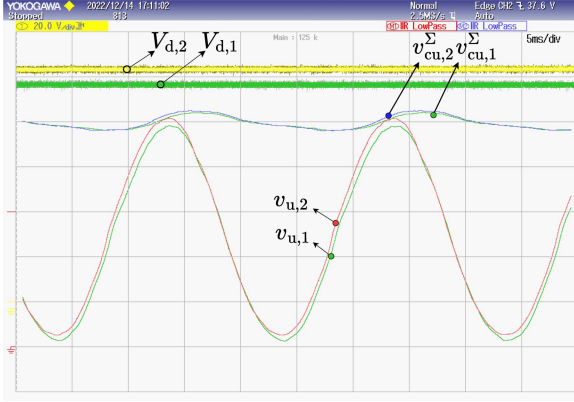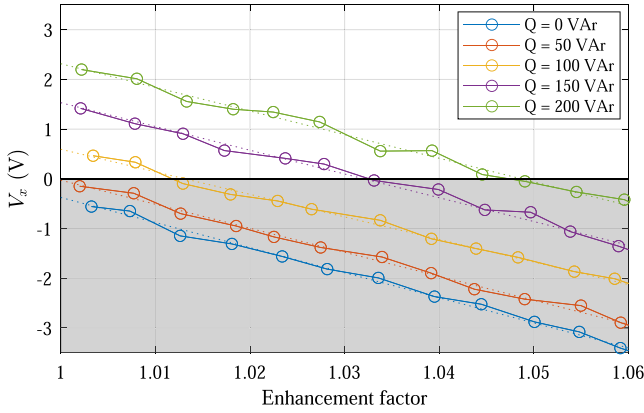
Fig. 16. Scope plot arm voltages before and after voltage enhancement.

Fig. 18. Analytical enhancement factor boundary with the empirical estimate.

Fig. 17. Measured V_x as a function of the enhancement factor for different injected reactive power references. The gray area represent a nonfeasible operation region where the set operating margin is compromised.

output waveform shape but is offset by +3 V compared to $v_{u,1}$. Furthermore, it can be observed that $v_{c,u}^{\Sigma}$ remains practically unaffected by the change in dc link voltage. The average value of the sum capacitor voltage is controlled to V_{dr}, while the ripple in $v_{c,u}^{\Sigma}$ is increased by an insignificant margin. As a result, the operated dc voltage is enhanced by 6% while keeping the ac side harmonic performance and submodule blocking voltage the same as in the rated condition.

B. Empirical Enhancement Boundary

Applying (9) and (27) to the measured waveforms of v_u and $v_{c,u}^{\Sigma}$ provides the empirical value of V_{space}. Then, in line with (29), the adjusted spacing voltage V_x is found from V_{space} by removing the operating margin between the measured $\hat{v}_s$ and $\overline{v}_{c,u}^{\Sigma}/2$. This measurement is performed for multiple values of $k_d \in [1, 1.06]$ to study the impact of the dc voltage enhancement on V_x. The results are provided in Fig. 17, which shows the k_p-V_x curves for a constant active power of 330 W and multiple values of the reactive power reference Q. As analytically, V_x is a linear function of k_d, a linear interpolation curve is fitted to the data points for the different values of Q.
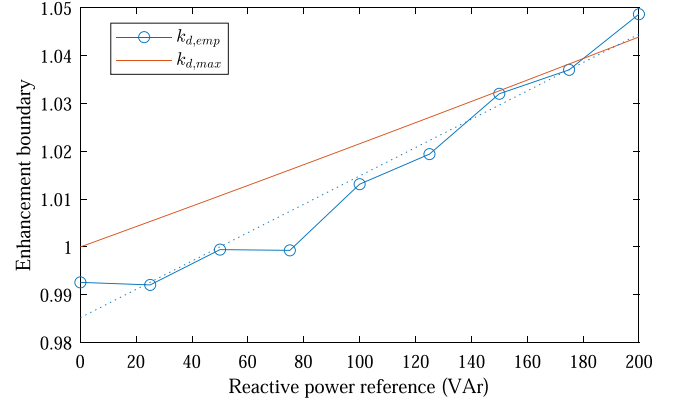
From Fig. 17 can be concluded that, for a fixed operating k_d, the adjusted spacing voltage is larger for higher values of Q. This highlight the positive impact of the grid injected reactive power on the spacing between $v_{c,u}^{\Sigma}$ and v_u, and verifies the direct correlation between of V_x and Q. Using the concept introduced in Section V, the zero crossings of the k_d-V_x curves provide an empirical estimate $k_{d,emp}$ of the boundary $k_{d,max}$. This as, for any enhancement $k_d > k_{d,emp}$, V_x is negative thereby facilitated the dc voltage rise through the reduction of V_{opm}, compromising the MMC's steady-state and transient performance. Then revisiting Fig. 17, it can be observed that an increase in Q causes a shift of the k_d-V_x curve, which in turn increase the zero crossing $k_{d,emp}$. So, Fig. 17 validates experimentally that the voltage enhancement boundary is extended as a result of the injection of Q.

Performing the measurements in Fig. 17 on a more refined scale of Q results in the enhancement boundary estimate presented in Fig. 18. This figure shows the analytical enhancement boundary $k_{d,max}$, following from (14), and the empirical boundary estimate $k_{d,emp}$ both as a function of Q. It can be concluded from Fig. 18 that there is a positive correlation between the empirical enhancement boundary $k_{d,emp}$ and the grid injected reactive power. This provides an experimental validation of the workings of the dc voltage enhancement, showing that the maximum enhancement of V_d increases with Q. Moreover, Fig. 18 shows the alignment of (14) with the empirical boundary estimate for larger values of Q. However, this accuracy is observed to be lower for smaller values of Q.

C. Empirical Controller Performance

The proposed dynamic control module is implemented on the laboratory prototype MMC. To experimentally analyze the performance, the MMC's response is measured for an increase in the reactive power reference Q_{in} from 0 to 150 VAr. In line with (14) and (24), the dc side voltage and operating active power are enhanced by 3.3% and 1.0%, respectively. The result of the experiment is provided in Fig. 19, which shows the reference of Q and P, the measured dc side voltage V_d, spacing voltage V_{space}, and peak SM switch current $\hat{i}_{sw}$, all as a function of time. Fig. 19(a) contains the dynamic response of the MMC
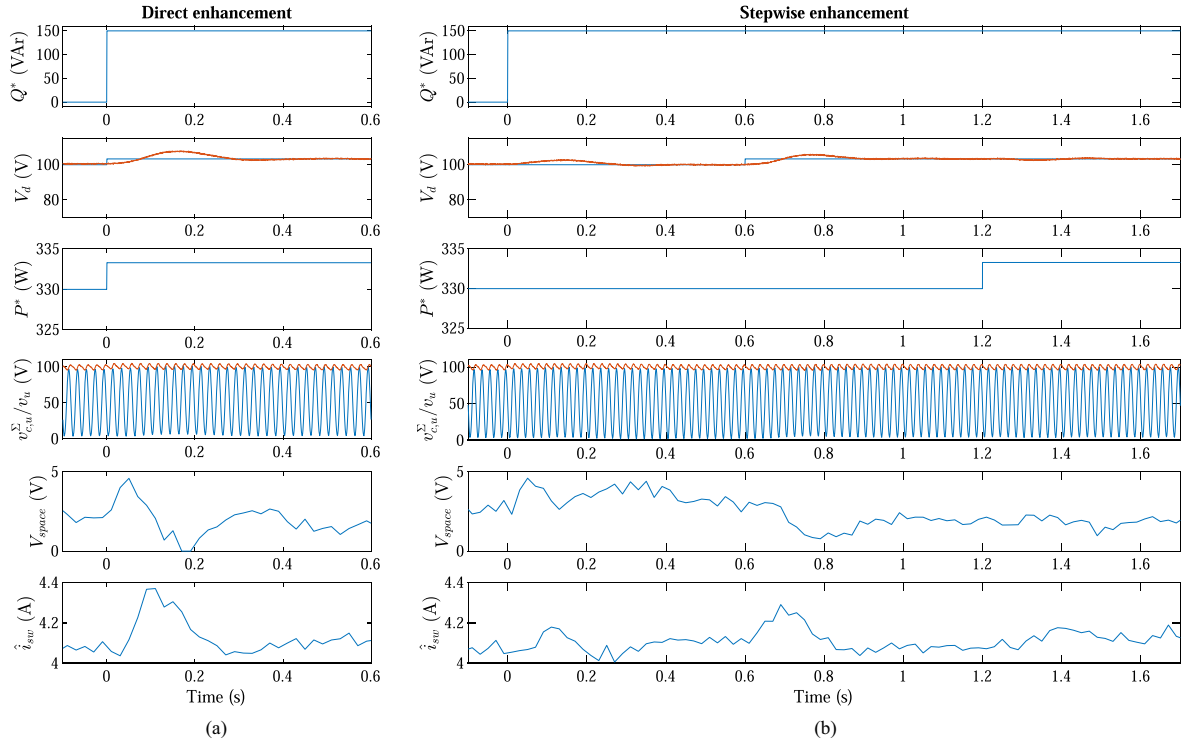
Fig. 19. Experimental dynamic results for the active power capacity enhancement with (a) a direct enhancement (b) a stepwise controlled enhancement.

with a direct enhancement, where Q, V_d, and P are simultaneously enhanced upon the change of Q_{in}. Fig. 19(b) contains the dynamic response of the MMC with a stepwise enhancement, resulting from the proposed dynamic control module, with $\tau_Q = \tau_{kd} = 0.6$ s.

From Fig. 19(a), it can be concluded that the direct enhancement causes a significant drop in V_{space} down to 0.0 V before it settles at the steady-state value of 2.1 V. This zero breaching of V_{space} corresponds to an injection of high-frequency arm voltage components during the system transient, degrading the MMC's output harmonic performance. Moreover, $\hat{i}_{sw}$ reaches a maximum value of 4.6 A during the system transient, which is higher than the steady-state value of 4.3 A. From Fig. 19(b) can be concluded that the stepwise enhancement preserves V_{space} with its minimum being at 0.8 V. This prevents the intersection of v_u and $v_{c,u}^{\Sigma}$, thus maintaining the MMC's harmonic performance. Moreover, the stepwise controlled enhancement limits the rise of $\hat{i}_{sw}$ to a maximum of 4.4 A. Comparing the response of the direct and controlled enhancement in Fig. 19 validates the dynamic interdependence of Q, V_d, and P, confirming the need for the stepwise enhancement as stated in (26). Furthermore, the comparison shows the performance advantage of the proposed controller in achieving the MMC's active power enhancement dynamically.

VII. CONCLUSION

This article presents a method for enhancing the dc voltage of a MMC beyond the rated value by utilising the converter's power-dependent ripple in the capacitor voltage. Operating the MMC at an enhanced dc voltage reduces the circulating current, thereby improving the converter's efficiency. Alternatively, this higher

dc voltage enables the MMC to operate with an enhanced active power capacity while maintaining the rated electro–thermal stresses on its components. This enhancement process leverages the spacing between the sum capacitor voltage and the arm voltage to preserve the ac side harmonic performance of the MMC. Meanwhile, controlling the average capacitor voltage to remain constant ensures that the SM stresses are kept the same as in the rated condition.

Following the arm voltage equations of the MMC, an analytical expression for the maximum dc voltage enhancement is derived. This expression ensures optimal utilisation of the capacitor voltage ripple to bias the arm voltage, increasing the dc side potential of the converter. The expression revealed a positive correlation between the voltage enhancement boundary and the grid-injected reactive power. Limiting the SM switch current of the MMC to the rated condition provided an analytical expression for the maximum active power enhancement. Combining the two expressions revealed the interdependence between the voltage enhancement, power enhancement, and grid-injected reactive power. This resulted in the need for the proposed dynamic control module, that solved the dynamic interdependence by making stepwise adjustments to V_d, P, and Q, ensuring the MMC's dynamics remain compliant in the enhanced operation.

Simulations of a 10 kV–10MW MMC verified the enhancement concept, where a 10.2% dc voltage enhancement could accommodate a 2.9% active power capacity enhancement while maintaining both the MMC's harmonic performance and SM stresses. Moreover, the voltage enhancement was found to reduce the MMC's losses, achieving a yearly energy savings of 20.2 MWh when operating at 90% of the converter's rated power. Further simulations showed the accuracy of the voltage

enhancement boundary expression for this 10 MW MMC. A similar verification of the boundary expression was obtained experimentally using the laboratory prototype MMC. Additional measurements with the proposed dynamic control module validated the transient performance and highlighted the dynamic performance advantage over a direct enhancement alternative.

REFERENCES

[1] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[2] J. Xu, P. Zhao, and C. Zhao, "Reliability analysis and redundancy configuration of MMC with hybrid submodule topologies," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2720–2729, Apr. 2016.

[3] M. Ahmadi, A. Shekhar, and P. Bauer, "Switch voltage rating selection considering cost-oriented redundancy and modularity-based trade-offs in modular multilevel converter," *IEEE Trans. Power Del.*, vol. 38, no. 4, pp. 2831–2842, Aug. 2023.

[4] Y. Xiao and L. Peng, "A novel fault ride-through strategy based on capacitor energy storage inside MMC," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7960–7971, Aug. 2020.

[5] A. Alesina and M. Venturini, "Solid-state power conversion: A fourier analysis approach to generalized transformer synthesis," *IEEE Trans. Circuits Syst.*, vol. 28, no. 4, pp. 319–330, Apr. 1981.

[6] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf. Proc.*, 2003, vol. 3, pp. 1–6, doi: 10.1109/PTC.2003.1304403.

[7] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[8] J. A. Ferreira, "The multilevel modular DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4460–4465, Oct. 2013.

[9] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014.

[10] A. Shekhar, T. B. Soeiro, Z. Qin, L. Ramírez-Elizondo, and P. Bauer, "Suitable submodule switch rating for medium voltage modular multilevel converter design," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 3980–3987.

[11] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H.-P. Nee, "Open-loop control of modular multilevel converters using estimation of stored energy," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2516–2524, Nov./Dec. 2011.

[12] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 57–68, Jan. 2012.

[13] A. Antonopoulos, L. Ängquist, L. Harnefors, and H.-P. Nee, "Optimal selection of the average capacitor voltage for variable-speed drives with modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 227–234, Jan. 2015.

[14] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, L. Ängquist, and H.-P. Nee, "Capacitor voltage ripple shaping in modular multilevel converters allowing for operating region extension," in *Proc. IECON 37th Annu. Conf. IEEE Ind. Electron. Soc.*, 2011, pp. 4403–4408.

[15] S. Fuchs and J. Biela, "Reducing losses and energy storage requirements of modular multilevel converters with optimal harmonic injection," *IEEE Access*, vol. 11, pp. 21283–21299, 2023.

[16] A. Shekhar, L. Ramírez-Elizondo, Z. Qin, and P. Bauer, "Modular multilevel converter performance with dynamic mvdc distribution link voltage rating," in *Proc. IEEE 18th Int. Power Electron. Motion Control Conf.*, IEEE, 2018, pp. 1000–1004.

[17] R. van der Sande, R. Deshmukh, A. Shekhar, and P. Bauer, "DC link capacity enhancement for MMC-based distribution link using dynamic voltage operation," in *Proc. 11th Int. Conf. Power Electron.*, 2023, pp. 636–642.

[18] R. Li and J. E. Fletcher, "A novel MMC control scheme to increase the DC voltage in HVDC transmission systems," *Electric Power Syst. Res.*, vol. 143, pp. 544–553, 2017.

[19] Z. Deng et al., "Efficiency improvement of solid-state transformers with mmc front-end AC–DC converters through adjusting DC bus voltage and active cells," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 13218–13233, Oct. 2024.

[20] M. Basić and D. Dujić, "Hybrid modular multilevel converter for variable DC link voltage operation," *CPSS Trans. Power Electron. Appl.*, vol. 6, no. 2, pp. 178–190, 2021.

[21] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel converter for a back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1538–1547, Jul. 2012.

[22] R. Li, L. Yu, L. Xu, and G. P. Adam, "Coordinated control of parallel DR-HVDC and MMC-HVDC systems for offshore wind energy transmission," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2572–2582, Sep. 2020.

[23] E. Sánchez-Sánchez, E. Prieto-Araujo, A. Junyent-Ferré, and O. Gomis-Bellmunt, "Analysis of MMC energy-based control structures for VSC-HVDC links," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1065–1076, Sep. 2018.

[24] European Commission, *Commission Regulation (EU) 2016/1447 of 26 August 2016 Establishing a Network Code on Requirements for Grid Connection of High Voltage Direct Current Systems and Direct Current-Connected Power Park Modules*, EU 2016/1447, European Commission Brussels, Belgium, 2016.

[25] Y. Li, X. Shi, B. Liu, F. Wang, and W. Lei, "Maximum modulation index for modular multilevel converter with circulating current control," in *Proc. 2014 IEEE Energy Convers. Congr. Expo.*, 2014, pp. 491–498.

[26] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2016, vol. 1, pp. 133–282.

[27] Z. Liu, K.-J. Li, Z. Guo, J. Wang, and J. Qian, "A comprehensive study on the modulation ratio for modular multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3205–3216, May/Jun. 2022.

[28] *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources With Associated Electric Power Systems Interfaces*, IEEE Std 1547-2018, pp. 1–138, 2018.

[29] A. Antonopoulos, L. Ängquist, L. Harnefors, K. Ilves, and H.-P. Nee, "Global asymptotic stability of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 603–612, Feb. 2014.

[30] A. Yazdani and R. Iravani, *Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2010.

[31] A. Shekhar, L. Ramírez-Elizondo, T. B. Soeiro, and P. Bauer, "Boundaries of operation for refurbished parallel AC–DC reconfigurable links in distribution grids," *IEEE Trans. Power Del.*, vol. 35, no. 2, pp. 549–559, Apr. 2020.

Robin van der Sande (Graduate Student Member, IEEE) received the B.Sc. degree in electrical engineering (*cum laude*) and the M.Sc. degree in electrical power engineering (*cum laude*) from Delft University of Technology, Delft, The Netherlands, in 2020 and 2022, respectively. He is currently working toward the Ph.D. degree in electrical engineering with the DC Systems, Energy Conversion and Storage Group as part of the Electrical Sustainability Energy Department, TUDelft.

He is currently working as a Guest Researcher with the Netherlands Defense Academy, Den Helder, The Netherlands. With his PhD project, he addresses the reliability and survivability aspects of dc shipboard power systems from the system design perspective to improve the availability and fault tolerance of future all-electric ships. His research interests include ship electrification, the reliability and survivability of power systems, and modular multilevel converters.

Anna Huwyler (Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering and information technology from the Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, in 2022 and 2024, respectively.

Her academic research was focused on the operation and control of power electronic systems in grid applications.

Aditya Shekhar (Member, IEEE) received the Ph.D. degree in the topic of flexible dc links in medium voltage distribution grids, improving the power transfer capacity by more than 50 percent in such networks.

He is an Assistant Professor with the field of Reliable Power Electronic Systems, Delft University of Technology and developed the Power Electronics and Reliability Lab (The PEARL), where the robustness of power electronic systems is tested. Thereafter, he worked as a PostDoc on EU projects such as Trolley 2.0, OSCD and EASY-RES. He has more than 25 Journals, 50 international conference papers and 2 book chapters and obtained research grants as part of several national and international consortiums such as PowerizeD (EU-Horizon), Sunrise (EU-Twinning), Survivable dc Power Systems for Ships (Dutch research council; NWO-KIC) and works with a team of 7 PhD students to explore research on reliable power electronic systems.

Pavol Bauer (Senior Member, IEEE) received the master's degree in electrical engineering from the Technical University of Kosice, Kosice, Slovakia, in 1985, and the Ph.D. degree in dynamic analysis of three-phase AC converters from the Delft University of Technology, Delft, The Netherlands, in 1995.

He received the title prof. from the President of Czech Republic with the Brno University of Technology, in 2008, and with the Delft University of Technology, in 2016. He is currently a Full Professor with the Department of Electrical Sustainable Energy, Delft University of Technology, where he is the Head of the DCE&S group. He is also an Honorary Professor with Politehnica University Timişoara, Romania, where he obtained an honorary doctorate too. From 2002 to 2003, he was with KEMA (DNV GL), Arnhem, on different projects related to power electronics applications in power systems. He has authored or coauthored more than 180 journal and 450 conference papers in his field.

Dr. Bauer is an author or a coauthor of eight books, holds ten international patents, and has organized several tutorials at international conferences. He has worked on many projects for the industry concerning wind and wave energy, power electronic applications for power systems such as Smarttrafo, as well as HVDC systems, and projects for smart cities such as photovoltaic (PV) charging of electric vehicles, PV and storage integration, and contactless charging. He participated in several Leonardo da Vinci, H2020, and Electric Mobility Europe EU Projects as Project Partner (ELINA, INETELE, E-Pragmatic, Micact, Trolly 2.0, OSCD, P2P, Progressus, Tulip, and Flow) and a coordinator (PEMCWebLab.com-Edipe, SustEner, Eranet, and DCMICRO). He is the former chairman of Benelux IEEE Joint Industry Applications Society, Power Electronics Society, and Power Engineering Society Chapter, the chairman of the Power Electronics and Motion Control Council, a member of the Executive Committee of the European Power Electronics Association, and a member of the international steering committee at numerous conferences.