Hierarchical EMC Design for Inverters in Motor Drive Systems

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PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof. dr. ir. J.T. Fokkema,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op maandag 7 december 2009
om 15.00 uur
door

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This research was supported financially by SenterNovem in the framework of the "Innovatiegerichte Onderzoeks Programma ElektroMagnetische Vermogens Techniek"(IOP-EMVT).

ISBN 978-90-9024883-7

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To my parents and my family

Abbreviations

AC	Alternating Current
Av	Average detector
BJT	Bipolar Junction Transistor
CM	Common Mode
CMC	Common Mode Choke
CSR	Current Source Rectifier
DC	Direct Current
DM	Differential Mode
EDM	Electrical Discharge Machining
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EUT	Equipment Under Test
FEMIT	Fast Emission Measurement In Time domain
FFT	Fast Fourier Transform
IFBW	Intermediate Frequency BandWidth
IGBT	Insulated Gate Bipolar Transistor
IT	Information Technology
LISN	Line Impedance Stabilization Network
MM	Mixed Mode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PFC	Power Factor Corrector
Pk	Peak detector
PWM	Pulse Width Modulation
QP	Quasi-Peak detector
SPWM	Sinusoidal Pulse Width Modulation
STFFT	Short Time Fast Fourier Transform
SVPWM	Space Vector Pulse Width Modulation

TDEMI	Time Domain EMI measurement
TDR	Time Domain Reflectometry
TRIAC	TRIode for Alternating Current
UPS	Uninterruptible Power Supply
VSD	Variable Speed Drive
VSI	Voltage Source Inverter
VSR	Voltage Source Rectifier
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Acknowledgements

Owning a doctoral degree is a dream of my childhood, but the road has been rather long. It has however been my good fortune to encounter many people who have given me much of their professional and personal help. When writing this acknowledgment, I realized that many individuals have lent me a hand. I cannot even recall the names of some of them but without them I could not have made all these things happen. I would like to convey my sincerest gratitude and appreciation to them.

I would first of all like to thank my promotor, Professor Braham Ferreira who gave me the opportunity to do this research at TU Delft. He supported and encouraged me all the time, not only in scientific matters, but also in coping with my mental and work conditions. Professor Frank Leferink, was my primary supervisor in my master study, and my promotor in my PhD study. His experience, and unique knowledge and enthusiasm in the EMC field have always been my support.

Dr. Henk Polinder, was my daily supervisor in the first two years. He gave me lectures to fill my gaps in the knowledge of machine and power electronics and support me in the anxiety during the beginning stage of my research. He also helped me to find a suitable apartment for my family which really saved me at that time.

I would like to thank my doctoral examination committee for studying the draft of the thesis and giving their valuable comments.

I would like to acknowledge the staff members in the EPP research group, Rob Schoevaars, Bart Roodenburg, Sjoerd de Haan and Paul Bauer for their help in the laboratory and their lectures.

I would like to thank the people who sit on the IOP-EMVT coaching committee. We had conferences twice a year and it was valuable to learn from your comments and suggestions. Thank you, Jasper Goedbloed and Lex van Deursen.

Thank you to my ex-colleagues in NEDAP, who helped me to find the chance

to do the PhD research at TU Delft and sent me to the interview. These include Randolph Browne, Ton Scharenborg, Richard Hogenkamp, Gerben Hoeksma, Gerhard van Eerden and many people. I do not remember all their names but thank you!

I would also like to thank Anne Roc'h, the fellow researcher with whom I have spent three years. We had many times of discussion, went together on industry investigations several times and co-operated in writing several papers.

Also, I want to thank many authors and specialists who I had communicated with. Special thanks go to Jin Meng, David Gonzalez, Christoph Keller, Peter van Duijsen and Norbert Hanigovszki. Furthermore, to the partners in industry, Evert Raaijen from Exendis in Ede, Jan-Kees van der Ven from Imtech Marine in Rotterdam and Jan Zinger from Eekels Elektrotechniek in Hoogezand for their hospitality during my visits to their companies.

It has been a great pleasure to work with so many talented colleagues and ex-colleagues in the EPP research group. I would especially like to thank Yi Zhou, Xun Gong, Deok-Je Bang, Zhihui Yuan, Yi Wang, Ghanshyam Shrestha, Marcelo Gutierrez-Alcaraz, Ivan Josifovic, Aleksandar Borisavljevic, Dalibor Cvoric, Johan Wolmarans, Hung Vu Xuan, Sam Ani, Frank van der Pijl, Johan Morren, Evandro Meurer, Milan Hajder, Jenela Popovic, Mark Gerber, Eric de Jong and Martin Pavlovsky. We are roommates, co-workers and classmates that I have worked, talked and lunched with over the years. I treasure the memories. I would like to thank Leo Breebaart. The LaTeX typesetting of this thesis is based on his public code. I would like to thank Ralf, Neil and Jan for their help in grammar check. A special word of gratitude goes to Tjerk Steenstra. Thank you for translating my proposition and summary into Dutch.

Moving towards more personal acknowledgements, I would like to thank many friends, especially Ankie, Erdogan, Bo Cui, Dazhao Xu, Ziye Han, Erwa Ke, Qian Xu and Chen Liu. Last but not the least; I would like to thank Oma, Jan, Edith, Jianguang, my parents and my brother, for their monumental, unwavering support and encouragement on all fronts. Finally, and most importantly, I would like to thank my wife, Ran, for her love, understanding, support and sacrifice during all the stages of my PhD studies. Thanks to my lovely sons, Chengji and Xingqi, who bring me the pride and happiness of being a father.

Dongsheng Zhao

Contents

Chapter 1

Introduction

1.1 The growth of power electronic converters

After the continuous technological evolution of the last five decades, power electronics has become completely indispensable in our everyday lives. Power converters are present wherever there is a need to modify form of the electrical energy in every corner of industrial, commercial, residential environments [Bos00].

One of the principal advantages of power electronics is that it improves efficiency during the energy form conversion. Higher efficiency means that less energy is lost during the conversion. Less energy is dissipated today in the conversion compared to conventional methods. It has been estimated that roughly 15% - 20% of electricity consumption can be saved by the extensive application of power electronics [Bos00].

Another advantage of using power electronics is that it makes many functions or features possible. Examples of such improvements include the following:

- Flexibility
  - a wider range of input voltage provided by a universal power adapter,
  - a programmable output voltage of an uninterruptible power supply (UPS),
- Controllability
  - an accurate positioning capability provided by a servo system,
  - a variable output frequency provided by a variable speed drive (VSD),
- Efficiency

- optimized operating points for the fluorescent lamp powered by an electronic ballast,
- energy regenerated from a braking motor.

Because of these outstanding benefits, the market of power electronics keeps growing and extending to many new application fields. The market penetration is surprisingly unbalanced in different application fields. Almost 100% of AC-DC power supplies for information technology (IT) equipment use power electronics. In contrast, approximately 5% of motors are controlled by VSD [Onl05]. Hence, there is still a large potential market for power electronics.

1.2 The EMC requirements

The benefits gained are due to developments in the field of solid state devices. Power electronic applications are working at a high switching frequency to transfer the input energy to its output by bursts. The size of many passive components can be reduced because the intermediate stored energy becomes less or not necessary. Some side effects appear, for instance, the switching loss increases with the switching frequency. To limit the total switching losses per unit time, the switching losses during each switching transient must be reduced. To achieve this goal, the switching transient time needs to be very short. The insulated gate bipolar transistors (IGBTs) can switch much faster than conventional bipolar junction transistor (BJTs). Reducing dissipation has many advantages, including higher reliability and smaller heat sink. But, many side effects emerge with the high switching frequency and the short switching transient time. The high switching frequency lifts the level of electromagnetic interference (EMI) and the short switching transient time extends the EMI to a high frequency range.

EMI may cause degradation of performance of the converter or other devices [Ott88]. It is a critical design aspect today. Designers must do more things than just make their products workable. The converter needs to be functionally compatible with other electronic systems in the same electromagnetic environment, and must avoid any interference effects. This work is called electromagnetic compatibility (EMC) design.

It is mentioned above that converters are becoming a main EMI source. This is the main reason for controlling the EMI of converters. There are more reasons to apply stringent standards to control EMI. For instance, the modern electronic circuits around the power electronics have become more and more sensitive since the general working voltage of the embedded logical devices is reducing from 5V to about 0.9 V - 3.3 V. Another reason is that the noise can be coupled more easily from the noisy power electronics circuit to the electronics circuit around it since these circuits are being crowded into smaller spaces.

Many regulations or standards are imposed by authorized departments to limit EMI levels. The requirements on EMC are not endless, actually, consideration

must be given to many other aspects, including functionality, volume and thermal performance. Otherwise, the cost may exceed the benefit obtained.

At the end of 2004, the Delft University of Technology and the University of Twente, both of them in the Netherlands, began a joint research project entitled ''Multi-domain Optimization of Power Electronics (MOPE)''. This project is funded by the IOP-EMVT which supports research and collaboration among academia and industry. The study is dedicated to the multi-domain design of power electronics, taking into account the major constraints of EMI, and considering also the thermal and spatial issues, using state of the art technologies.

1.3 Problem description and research object

The first problem is that there is no systematic approach to designing for EMC, especially in a complex power electronic system. Most EMC engineers may have experienced situations whereby a solution may suppress the noise in some frequency ranges but lift the noise level in other frequency ranges. The trial-and-error method is very time-consuming for this kind of application.

Because it is so easy to access advanced computing capability, there is a trend towards solving the problem using numerical methods. For a complex EMC issue, many factors come together simultaneously to determine the final EMI level. It is not an easy task to figure out a solution without logical thinking.

Circuit simulation is used widely to predict the EMI of a converter [Won01; Gra04]. Before the simulation, an accurate model must be built including all the components inside a converter. These models are entered into the simulation program and then the simulation runs in the time domain. The simulation may take several minutes before the final result is available. The result is unknown until the simulation is finished and then it is transformed to the frequency domain. A troublesome thing is that the simulation has to be run again from the beginning if any component inside the system changes its value.

Therefore, attempts are also made in the frequency domain, for instance, the work in [Ran98]. The noise source is translated to the frequency domain first by including the finite switching time, and then the equivalent circuits for the common mode (CM) and differential mode (DM) are introduced individually. Spectra of the noise received by the line impedance stabilization network (LISN) can be calculated in the frequency domain. It is mentioned in [Ran98] that a very large error is possible if the pulse rise times are not taken into account. In [Gon03], the impedance matrix is used to calculate the disturbance. An unavoidable prerequisite using this method is that the whole equivalent circuit must be time invariant.

Because of the shortcomings listed above, the present methods for EMC design need improvement. This is the first objective of this project.

The second problem is that the remedies for EMC suppression are limited. Literatual study shows that there are at least 14 kinds of remedies are proposed

by acadamy, but only passive filter approach becomes the most widely adpated solution. For the rest solutions, the benefits achived are not attractive enough for industry to compensate the costs.

The second objective of this project is clarified as: finding innovative EMI suppression methods which are:

- effective in improving EMC performance,
- easy to implement,
- able to reduce the volume and weight of the power conversion systems,
- not having significant impact on functional and thermal issues.

1.4 Research method

To achieve the goal, the hierarchical procedures are first established to replace the trial-and-error method. These are utilized to analyze the motor drive system. Possible solutions are then proposed and discussed.

The methodology used in this thesis is a hierarchical method. It divides the whole problem into three levels. For each level, models are built in different ways to reach a compromise between the accuracy and speed.

The first level is the functional level. On this level, parasitic parameters are omitted. The circuit can be modeled by switch function and all switches are idealized. Power electronics engineers are quite familiar with this level. The voltage and current waveforms are calculated by the fastest method. On this level, the computation speed needs to be as fast as possible to support a relatively long period of simulation. We want the ‘‘worst-case scenario’’ can be included in the simulation.

The second level is the transient level. Detailed behavior models of switches are utilized to get the voltage and current waveform of the very fast transient. The calculation is based on the information of operating points obtained on the functional level. On this level, only the parasitic inductors and capacitors around the switch are taken into account because they have an impact on the behavior of the switch. The analysis on the transients level obtains the details around the transient. The spectrum of the noise source is known using the analysis based on the functional level and the transient level.

The third level is the propagation level. All parasitic components are part of the propagation path. The ratio between the noise source and the measurement result is defined as a transfer ratio. The transfer ratio considers all possible topologies of different switching patterns.

With this method, much intermediate data is generated. This helps us to find the deviation in the middle way by comparing the intermediate data with additional measurements. The improvement of the EMC design is also traceable.

Although the functional, spatial and thermal issues are mentioned in this objective, the functional issue is considered the most closely related to the EMC issue. The design interdependency will be studied in this thesis. The volume and weight requirements are only analyzed qualitatively. This means a traditional suppression method with bulky filters cannot be applied and an innovative method is necessary. Thermal issues are not defined in this research.

In this research, VSDs are chosen for investigation. The first reason is that in industrial applications, a large part of energy is consumed in this form. It is estimated that 60% - 65% of generated electricity in the United States is consumed in motor drives, and of those motors, 60% operate pumps and fans [Bos00]. For such kind of applications, optimizing motor speed can benefit the most. With VSD, the motor would not run at full speed all the time. There is a great potential to utilize power electronics to upgrade these motor drives to variable speed motor drives since the market penetration of VSD is only 5% at present. That is, the research is practical. Another consideration is that the high rated power and the fast switching transient make the EMC issue unavoidable.

In this research, the focus is narrowed down to control the *conducted EMI* of *inverters in motor drive systems*, within a frequency range of interest from 9 kHz to 30 MHz.

1.5 Thesis layout

Chapter 2 considers the configurations of the AC-AC converter. The mechanisms of noise sources are identified and analyzed. Chapter 3 begins the main contribution of the thesis. The hierarchical EMC design procedure is established and it is used for the modeling of an existing motor drive. The motivation and procedure to implement this approach are presented. Chapter 4 presents the observations in the time domain. After understanding how noise is propagated, a DC-bus filter is proposed to suppress the noise along the propagation path. The design procedures and benefits of this remedy are presented. Chapter 5 clarifies the EMC noise sources. A relationship is established between calculated results and compliance measurement results. Chapter 6 reviews firstly various EMC remedies which are implemented on the noise source side. A new active filter approach called ''fourth leg compensator'' is proposed. Its principle and simulation results are presented. Finally, Chapter 7 gives the conclusions and recommendations for future development.

Chapter 4 has been partly published in the IEEE Transaction on Power Electronics [Zha09] and at the EPE Aalburg conference in 2007 [Zha07]. Chapter 3 and 5 have been partly presented at PESC 2008 Greece conference [Zha08a]. Chapter 6 has been partly presented at EMC Europe 2008 Hamburg conference [Zha08b].

Chapter 2

Configurations of AC-AC converters

2.1 Introduction

In many industrial or commercial applications, the loads need provision of AC power. The loads include motors, sodium vapor lamps, induction heating coils, and many other miscellaneous components. The power requirements are all in AC form but with different amplitudes, frequencies or phases. Normally, these values are variable during operation of the load. Also, the power distribution network has different standards around the world. AC-AC conversion is necessary when the requirements of the load are not compatible with the electric power provided by the public power grid. One good example is when a yacht is moored in a harbor. To use the local power network, the functions of the converter in the yacht should include voltage scaling, frequency conversion and galvanic isolation. The galvanic isolation is required especially for safety reasons and to prevent corrosion of the ship's hull.

Even though AC-AC converters are built for the same purpose, this is to bridge the different AC forms of the electric utility source and the load, many configurations exist due to various design specifications and requirements of the source and the load. The differences in the configurations have many aspects, including topology, rectifier, grounding, DC-bus, inverter and load type.

In this chapter, we first discuss the possible AC-AC converter topologies. They are ordered from the simplest to the most complicated. There can be one to five conversion stages. The bus types used in the power conversion process are illustrated with diagrams. Three topologies are selected for case study. After that, the noise source generation mechanisms are identified and the noise propagation paths are pointed out.

The influences of diverse configurations are discussed from the EMC point of view. The impact on EMC of different rectifiers, ground configurations, DC-

bus and inverters are discussed. These configurations are specially defined for functional, safety and other requirements. At the same time, they have significant impact on the modes of noise propagation and the EMI level.

The discussion ends with the requirement of a new approach to analyze the EMC performance for AC-AC converters.

2.2 Topologies of AC-AC converters

In AC-AC converters, the alternating currents and alternating voltages appear both on the source side and on the load side. The converters change amplitude, frequency and phase of the AC current and voltage waveforms between the source and the load. The conversion is normally controlled to reach the optimal operating points of the load. For an ideal AC-AC converter, the input voltage and the input current are in phase on the source side, and the relationship between the output voltage and the output current is according to the property of the load. The converter with sinusoidal waveforms is illustrated in Figure 2.1.

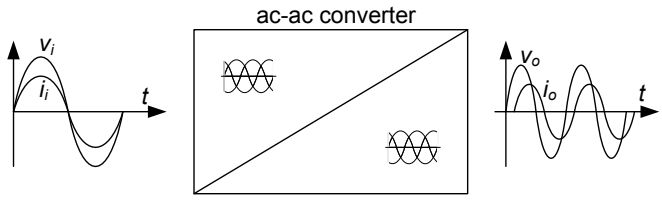


Figure 2.1: Voltage and current waveforms in an AC-AC converter

However, the voltage and current waveforms are not limited to be sinusoidal. The waveforms can be arbitrary provided they contain essential fundamental component. This gives much more freedom as long as the following conditions are satisfied for different applications:

- emissions stay below the limits for harmonics and EMI,
- the input power factor satisfies standards,
- efficiency requirements are met,
- specific requirements, for instance, the galvanic isolation can be provided.

Many topologies are available for AC-AC converters. Each of them has advantages and disadvantages, and is suitable for a particular range of applications.

2.2.1 Single-stage AC-AC converter topologies

A conventional 50 Hz transformer is probably the simplest device that performs the AC-AC voltage scaling function. It is irreplaceable in the voltage scaling application due to its high efficiency and reliability, but strictly speaking, a transformer is not a converter.

The conventional AC-AC transformer cannot be used for frequency conversion since the variable voltage scaling depends on movable mechanical contacts and its limitations are evident. Therefore, power electronics devices are used in AC-AC conversion, which is called AC-AC converters.

AC phase-controlled voltage controllers use TRIACs (TRIode for Alternating Current) or thyristors to conduct the load. The conducting angle depends on the firing angle and the load angle because a half-controlled switch can only turn off when the current returns to zero. Figure 2.2 shows the converter in block diagram form. The main drawback of this controller is that it draws distorted current from the supply line, and the input power factor is poor.

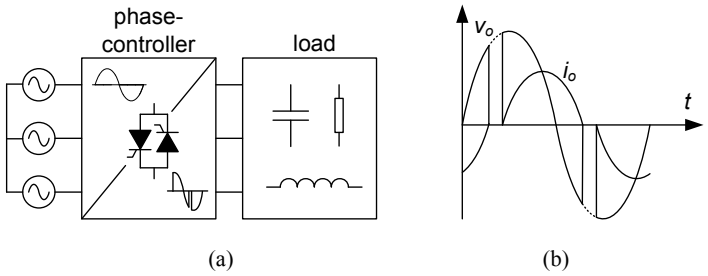


Figure 2.2: AC phase-controlled voltage controller; (a) diagram, (b) output voltage and current waveforms

The AC-AC chopper, illustrated in Figure 2.3 allows for controlling the output voltage. The variable output voltage scaling can be achieved by changing the duty cycle of the chopper circuit. For the AC-AC chopper, fully-controlled bidirectional power switches are necessary to turn off the current at an arbitrary moment. The output frequency stays the same as the input frequency. Low-pass filters are connected to both the input and output side of the AC chopper circuit in order to remove the switching ripples and harmonics. The ripples can also be filtered by load inductance itself.

Cycloconverters can convert an AC source to another AC waveform of a lower frequency. They are normally used in a fixed input frequency and amplitude application with very high power rating. Both the amplitude and the frequency of the output voltage can be variable. The diagram and output voltage waveform are shown in Figure 2.4. The turn-off is normally by natural commutation. The limitation of the output frequency range exists.

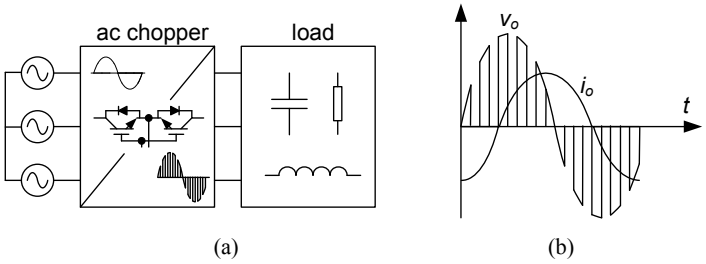


Figure 2.3: AC-AC chopper; (a) diagram, (b) output voltage and current waveforms

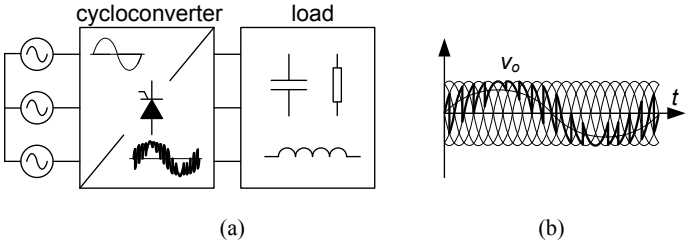


Figure 2.4: Cycloconverter; (a) diagram, (b) output voltage waveforms

By replacing the natural commutation components with full controllable bidirection switches, the cycloconverter evolves into a matrix converter. The diagram is shown in Figure 2.5.

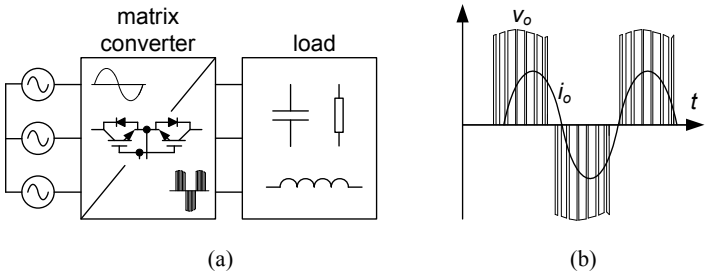


Figure 2.5: Matrix converter; (a) diagram, (b) output voltage and current waveforms

A single-stage AC-AC converter does not use energy storage components. It is a type of direct converter. The concept is simple and elegant. However, a main intrinsic drawback is that the output voltage is limited to 87% of the input voltage. Also it cannot ride through a voltage sag and the conduction losses are inherently high. The unavailability of fully controllable bidirectional semiconductor switches is the main limit of this topology.

2.2.2 Two-stage AC-AC converter topologies

Another class of AC-AC converters is the compound converter. A voltage or current link is used for energy storage. The converter changes input AC to an intermediate form of voltage or current and then converts the intermediate form to output AC with variable amplitude and frequency. The intermediate link decouples these two conversion stages, therefore, two conversions need not to be extractly synchronized and the control is simplified. Although the average energy flow is equal between input and output, the instantaneous input power does not need to be equal to the instantaneous output power. The difference between the instantaneous input and output power can be absorbed or delivered by the energy storage element in the intermediate link. The energy storage element can be either a capacitor or an inductor according to the control scheme.

Figure 2.6 shows the diagram of an AC-AC converter with DC voltage as the intermediate link. A capacitor is used as the energy storage element.

2.2.3 Three-stage AC-AC converter topologies

To realize galvanic isolation function, the most common solution is using a transformer. Because the DC components cannot pass through the transformer, the

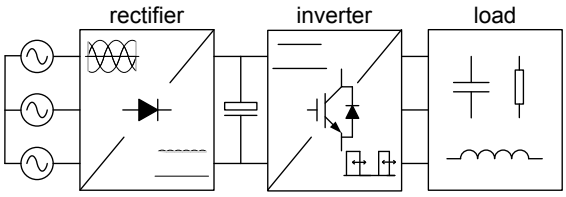


Figure 2.6: Block diagram of voltage source DC-bus converter

previous topologies are not feasible to provide galvanic isolation function.

One possibility is converting the DC intermediate form to an AC high frequency square wave. Then, the square wave passes through the high frequency transformer to achieve galvanic isolation. The high frequency AC square wave is available at the transformer secondary side and is synthesized to low frequency AC using a cycloconverter [Wik07; Kre02]. The topology is shown in Figure 2.7.

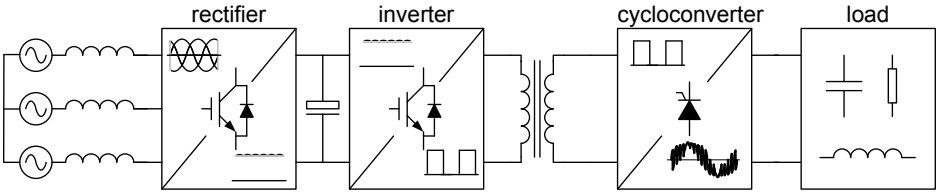


Figure 2.7: Block diagram of three-stage AC-AC converter with galvanic isolation

2.2.4 Four-stage AC-AC converter topologies

If a cycloconverter is not used in the previous topology, the AC square wave is rectified to DC voltage firstly, then a pulse width modulation (PWM) inverter is used to generate the fundamental component of the AC waveform. The topology is shown in Figure 2.8.

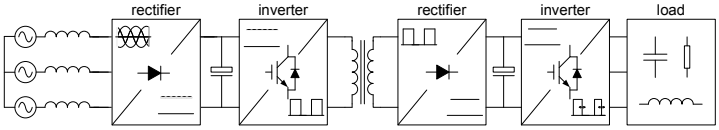


Figure 2.8: Block diagram of four-stage AC-AC converter with galvanic isolation

2.2.5 Five-stage AC-AC converter topologies

In some applications, a unity power factor input is required. This is realized by adding a boost DC-DC converter behind the diode rectifier. The boost converter is used to step up the DC-bus voltage, so that the DC-bus current is reduced. The topology of this popular configuration in AC-AC converters is shown in Figure 2.9.

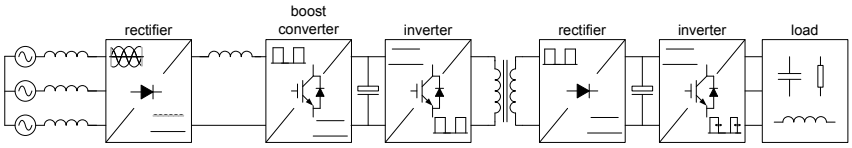


Figure 2.9: Block diagram of five-stage AC-AC converter with galvanic isolation and a unity power factor

When using an active rectifier to replace a diode rectifier, one can achieve the same functions. An additional benefit is that it supports bidirectional power flow, but it needs more active components.

2.2.6 Selected topologies for case study

In this project, three representative topologies are selected as study objects. The three selected objects have different numbers of conversion stages.

A voltage source inverter with a DC-bus capacitor and a diode rectifier front end is the most popular AC-AC converter used for motor drives. Its complete diagram is shown in Figure 2.10.

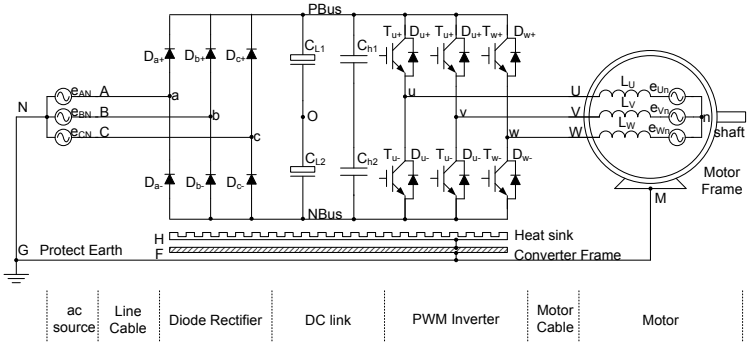


Figure 2.10: Block diagram of DC-bus voltage source inverter

A resonant pole inverter is shown in Figure 2.11. This inverter is working by

zero voltage switching (ZVS) at variable switching frequency. It is also used as a study object.

The third topology used in investigation is a four-stage AC-AC converter with galvanic isolation. It is used as a power interface between a public power grid and an offshore application. Because sinusoidal input currents with a unity power factor and bidirectional power flow are required, a three-phase PWM boost rectifier is included. In addition, it also includes DC capacitor banks on the primary and secondary side, a three-phase inverter system that is able to generate variable frequency and variable voltage, a DC-DC converter with isolation transformer, sinusoidal and EMC filters, a DC power supply, control circuits and sensors, protection circuits, a cooling system and a start up circuit to limit the current charging the DC-bus capacitor. The diagram is shown in Figure 2.12.

2.3 The capacitive coupling mechanism

Capacitive coupling is caused by a varying voltage source. It occurs between adjacent conductors or circuits. Since the dimensions of most components inside the drive system are substantially smaller than one wavelength at 30 MHz, the capacitive coupling mechanism can be modeled by lumped components when we consider the conduction emission issues of AC-AC converter systems.

The varying voltage source is called a capacitive coupling point if it has a fast transient voltage, and it has parasitic capacitances with surrounding circuits. A fast transient implies the presence of many high frequency components. In the high frequency range, parasitic capacitances form low impedance paths for the current.

Inside a converter system, there are numerous capacitive coupling points. The switches are components that form such points which generate the noise current by the capacitive coupling mechanism. Inevitable parasitic capacitances normally exist between these points and ground. The reason for using ground as reference is because we are investigating the noise current that flows between the phase lines and the ground.

Figure 2.13 illustrates how current is generated by the capacitive mechanism in a drive system.

The noise current depends not only on the voltage transient, but also on the impedance of the current loop. The loop impedance includes the coupling impedance and the return impedance from ground back to the coupling point. The return impedance includes the impedances of ground, the power source and the input stage of the converter. Ground in the current loop may be the safety ground cable or the ground plane. In [Nav91], they are named as CM type I and CM type II. The impedance value can influence the noise current significantly.

For instance, for the coupling points of the output terminals of the transistor, coupling impedances exist between the die of the transistors and ground. The transistors are normally mounted on a heat sink. Because the cooling fin of the

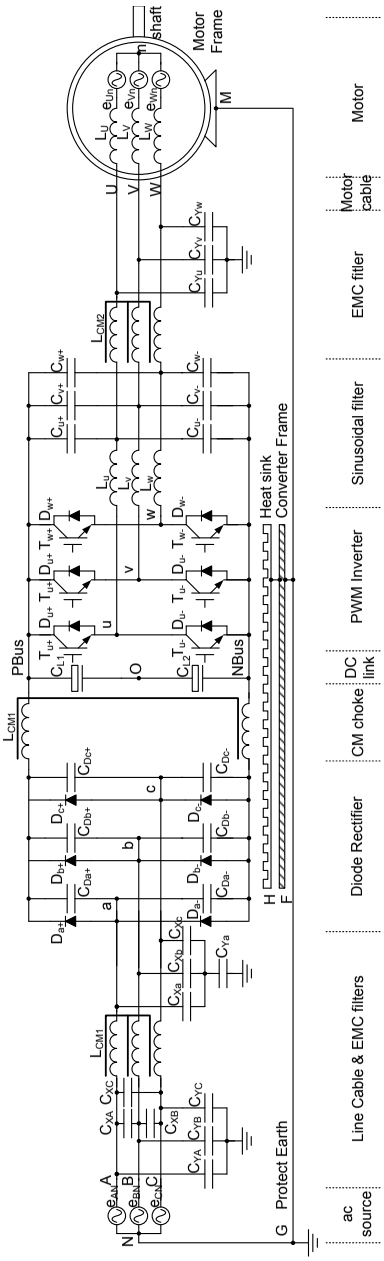


Figure 2.11: Block diagram of resonant pole inverter

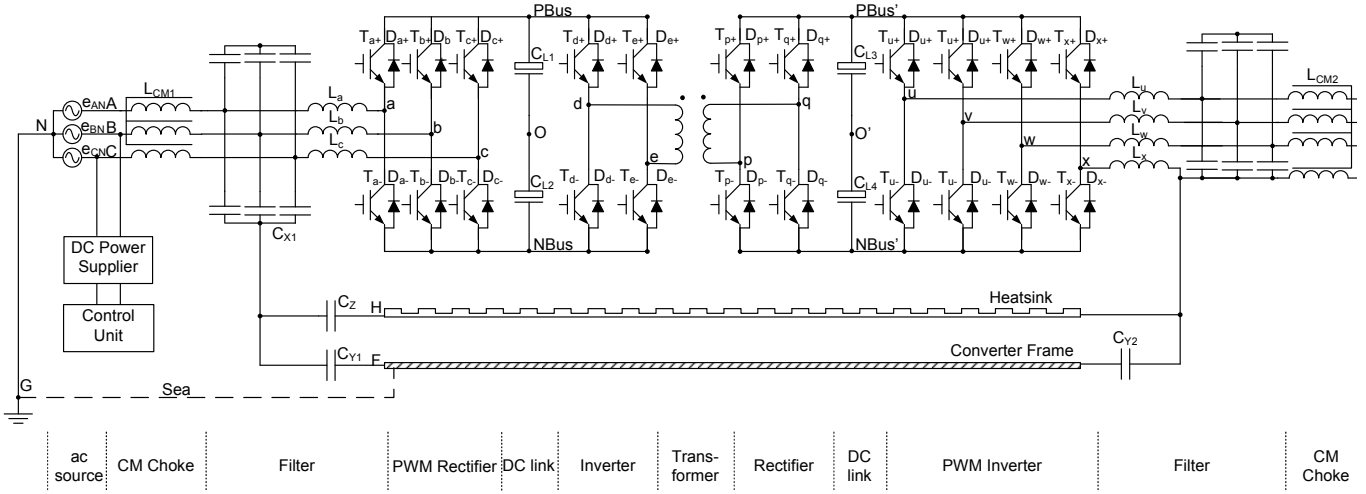


Figure 2.12: Block diagram of four-stage AC-AC converter with galvanic isolation

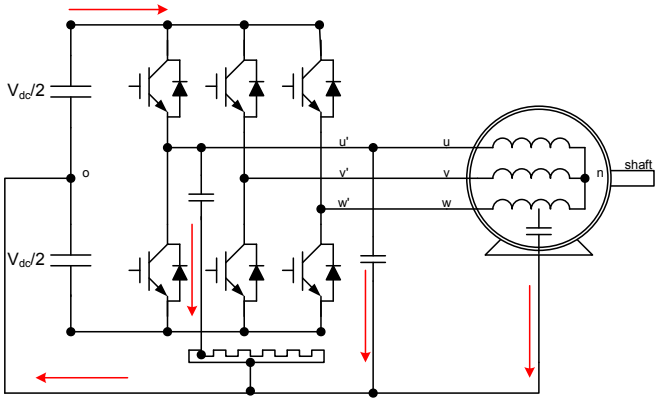


Figure 2.13: Capacitive coupling in a motor drive system

heat sink is exposed to the outside, it is commonly grounded for safety reasons. With the grounding of the heat sink, the coupling impedance has two parts. The first part is the impedance of the capacitor formed by the die of the transistors and the heat sink which are separated by a high thermal conductivity insulating film. The second part is the impedance of the wire connecting the heat sink to ground.

For motor drive applications, the capacitive coupling points also include the motor cable and the motor windings. This is because of the parasitic capacitances between the cable wire and ground. Also, there exists a capacitive coupling between the motor winding and the motor frame.

The fast voltage transients are generated by the switching of the transistors. In most cases, the transistors are not switched at the same time, otherwise the converter has no purpose because no load currents are built up with synchronized switching of transistors. In other words, the voltage transients at different capacitive coupling points have different waveforms.

If the coupling impedances are the same in three phases of the circuit and the circuit are exactly symmetrical, one approach to simplify the analysis is to decompose the voltage sources into CM and DM components. Assuming we have voltage source v_1, v_2 and v_3 for three switches. The symbols $v_{\mathrm{DM}(1,2,3)}$ and $v_{\mathrm{CM}(1,2,3)}$ are used to represent the DM and the CM voltage sources. Ideally, we have,

$$v_{\mathrm{CM1}} = v_{\mathrm{CM2}} = v_{\mathrm{CM3}} = \frac{v_1 + v_2 + v_3}{3} \tag{2.1}$$

$$v_{\mathrm{DM(i)}} = v_{(i)} - v_{\mathrm{CM(i)}}, i = 1, 2, 3 \tag{2.2}$$

$$v_{\mathrm{DM1}} + v_{\mathrm{DM2}} + v_{\mathrm{DM3}} = 0 \tag{2.3}$$

The DM components would not make any contribution to the flow of current through the ground. They produce the DM current flowing between phase lines. The CM components drive the current flowing through ground, and the currents flowing through the phase lines are evenly distributed. By combining CM and DM components, we find that the currents flow unevenly through the phase lines even for this capacitive coupling mechanism. For the DM component, it is called a mixed mode (MM) component in literature since it is a capacitive coupling mechanism and represents a differential format [Men04a; Men04b].

An easy approach to validate the existence of the MM component is to compare the DM components with and without the grounding strap of the LISN. The MM component should disappear when the CM current loop is broken. However, the DM component which is caused by functional switching should stay at the same level even if the grounding configuration changes.

The decomposition approach is based on an assumption that the values of the parasitic components in each phase are the same and fixed. If the symmetry condition does not exist, then the decomposition approach is not valid. Considering that the parasitic values of the components change with operating point, the coupling impedances are time-variant. The decomposition approach is limited to giving an intuitive explanation for qualitative analysis. To get a precise prediction, the decomposition approach is not enough.

2.4 The inductive coupling mechanism

Together with the capacitive coupling mechanism, the inductive coupling is another main mechanism. A source current loop with a fast transient current can couple noise through the mutual inductance to a victim loop. The induced noise sources can be modeled as controlled voltage sources according to Faraday's law of induction.

Inductive coupling is introduced by a varying current source. It can be modeled by mutual inductance between two inductor when the distance between two adjacent loops is shorter than one wavelength at 30 MHz. An inductive coupling mechanism is a major mechanism of noise generation for drive system since current abruptly changing is quite normal due to the operation principle of power electronics.

In an AC-AC converter investigated in [Roc07], a current loop is formed by bypass capacitors connecting the output neutral wire to the input neutral wire. Noise current with the same resonance frequency is found at the entrance of the AC-DC converter which provides power for controller and sensors. It can be explained through the inductive coupling mechanism. Figure 2.14 illustrates the inductive coupling in this AC-AC converter.

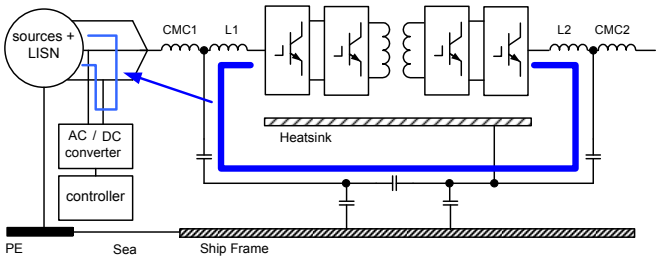


Figure 2.14: Inductive coupling in an AC-AC converter

Two aspects determine the effectiveness of the coupling. One is the value of the mutual inductance. We use the mutual inductance equation of a pair of loops to show what factors have an influence on the coupling efficiency:

$$M = \frac{\mu_0 N_1 N_2 (\pi r_1^2)(\pi r_2^2) \cos\theta}{2\pi h^3} \tag{2.4}$$

Here N_1 is the number of turns of the source loop, N_2 is the number of turns of the victim loop, r_1 is the radius of the source loop, r_2 is the radius of the victim loop, h is the distance between the centers of two loops, θ is the angle that the axis of the source loop makes with the axis of the victim loop.

The source loop or the victim loop can be a component, for instance, an inductor, the parasitic inductance of a capacitor [Che06], a CM choke [He05]. The loop can also be a printed circuit board (PCB) trace loop, a motor winding [Mue04], or ground loop. The induced voltages become the source of DM noise [He05]. If the victim loop includes ground, then CM noise is also generated [Poo03; Men08].

According to the equation above, the coupling effect can be significant when there are many turns in the source or the victim loop. This is the reason that placing a component has significant influence on the EMC performance [Che06]. In [Wan05], inductive coupling is used to cancel the parasitic inductance of a capacitor.

The second aspect that determines the effectiveness of the coupling includes the geometry and relative position of these two loops. With large areas and a small angle between the source and the victim, the coupling can also be aggravated. This extreme situation arises when two loops are placed concentrically.

To reduce stray inductance, the loop area can be minimized or be twisted in a clever way [Ros00]. While in some cases, hidden noise sources cannot be easily deduced. Some noise sources with subtle coupling paths can present a major source of EMI. For instance, a snubber circuit which is helpful in functional improvements can be a harmful EMI noise since the loop that is formed by the snubber and the transistor is accompanied by fast current transients [Poo03].

2.5 Rectifier configurations

There are two types of rectifier circuits that convert an AC supply into a DC voltage, namely, line-commutated rectifiers and self-commutated rectifiers. The main difference is in the commutation cells, which work under uncontrolled and controlled modes, respectively.

The rectifier with a diode front-end is line-commutated. Ideally, the diodes can be regarded as switches operating in neutral switching mode [Onl07]. That is, the diode is turned on when the voltage across the diode reaches the turn-on voltage and is turned off when the switch current is zero. Its commutation process depends on other components.

The diodes are often simplified as ideal switches, i.e., they have zero forward voltage drop and zero reverse bias current. From the EMC point of view, the transient phenomena and high frequency characteristics have significant impacts. The components cannot be idealized in EMC analysis. The typical turn-on and turn-off waveforms of a diode are presented in Figure 2.15.

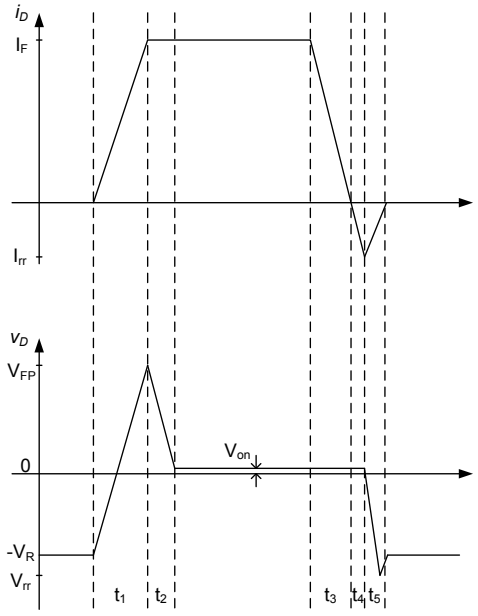


Figure 2.15: Voltage and current waveforms for a power diode during turn-on and turn-off

For a diode-bridge three-phase rectifier with a filter capacitor connected on the output side, the commutations of diodes need to be calculated in steps. Firstly, the waveforms of the currents flowing through diodes are calculated numeri-

cally [Moh03]. With large capacitor or light load, the output current of the rectifier can be discontinuous. In this case, the currents through the diodes become zero prior to each commutation. Because no reverse recovery occurs, the EMI generated by a diode is quite low. In a continuous output current operation condition, the diodes need to commutate from one to another every 60 degrees. The diode now becomes a main high frequency noise source due to the reverse recovery current. The transient waveform is determined by the amplitude of the flowing current before the commutation and also the AC-side inductance and resistance.

When an extra finite inductor is used to improve the current waveforms and the ripple in the DC voltage output, the commutation can be much smoother. Another solution is using paralleled small capacitors with the diodes. In Figure 2.11, this strategy is used in the rectifier.

The diode bridge rectifier also brings voltage fluctuation of the DC-bus as referred to the neutral point of the AC-source. The voltage ripple is a triangular voltage with a frequency of 150 Hz. The amplitude is around 20% of the DC-bus voltage. This voltage increases the possibility of breakdown of the bearing lubrication when the motor is used as load. This mechanism generates the electrical discharge machining (EDM) bearing current. For the capacitive bearing current and ground leakage current, the influence of the diode rectifier can be ignored due to its very low frequency.

To achieve the capability of delivering sinusoidal input currents, the power factor corrector (PFC) rectifier uses a PWM mode. There is a tendency towards more and more PWM rectifier converters being used in power supply systems. They can be classified as voltage source rectifier (VSR) and current source rectifier (CSR) according to their energy-storage components. Compared to the diode rectifiers, PWM rectifiers have much faster transients. Also, these transients repeat more frequently than the diode rectifier. This makes the PWM rectifier a main noise source for EMI.

Figure 2.16 shows the PWM inverter with boost PWM rectifier. The three-phase AC input source is star connected. The neutral point of the AC-source (point ''N'' in Figure 2.16) is connected to ground (point ''G'' in Figure 2.16). The voltage difference between the rectifier input terminals and ''N'' is described by

$$\begin{cases} v_{aN} & = v_{aA} + e_{AN} & = i_a sL_a + e_{AN} \\ v_{bN} & = v_{bB} + e_{BN} & = i_b sL_b + e_{BN} \\ v_{cN} & = v_{cC} + e_{CN} & = i_c sL_c + e_{CN} \end{cases} \tag{2.5}$$

The switching functions of the boost rectifier and inverter are defined using $s_i (i = a, b, c, u, v, w)$, where s_i=1 when the upper switch is turned on and the lower switch is turned off, and s_i=0 when the upper switch is turned off and the lower switch is turned on. The voltage difference between the DC-bus midpoint (point ''O'' in Figure 2.16) and the rectifier input terminals can be expressed by

Figure 2.16: Block diagram of PWM inverter with boost PWM rectifier

$$\begin{cases} v_{Oa} &= (\frac{1}{2} - s_a)V_{\rm dc} \\ v_{Ob} &= (\frac{1}{2} - s_b)V_{\rm dc} \\ v_{Oc} &= (\frac{1}{2} - s_c)V_{\rm dc} \end{cases} \tag{2.6}$$

From Equation (2.5), (2.6) and the assumption that the three-phase source is balanced, v_{ON} can be expressed as

$$\begin{aligned} v_{ON} &= \tfrac{1}{3}(v_{aG} + v_{bG} + v_{cG}) + \tfrac{1}{3}(v_{Oa} + v_{Ob} + v_{Oc}) \\ &= \tfrac{1}{3}(i_a sL_a + i_b sL_b + i_c sL_c) + (\tfrac{1}{2} - (\tfrac{s_a+s_b+s_c}{3}))V_{\rm dc} \end{aligned} \tag{2.7}$$

Normally, the boost inductors have the same value. The first term of Equation (2.7) is the voltage drop across the boost inductors when conducting CM current. The second term is caused by switching on and off of the transistors in the PWM rectifier.

Using the same procedure to model the inverter part of this PWM inverter, the voltage difference between the neutral point of the load (point "n" in Figure 2.16) and the DC-bus midpoint (point "O" in Figure 2.16) can be expressed as

$$v_{nO} = \tfrac{1}{3}(i_u sL_u + i_v sL_v + i_w sL_w) + ((\tfrac{s_u+s_v+s_w}{3}) - \tfrac{1}{2})V_{\rm dc} \tag{2.8}$$

A simplified high frequency equivalent circuit of this kind of rectifier can be drawn in Figure 2.17, here,

Z_{OG} is the impedance between the DC-bus and ground,
Z_{nG} is the impedance between the load (the motor in this case) and ground,
L_u is the winding inductance of the motor.

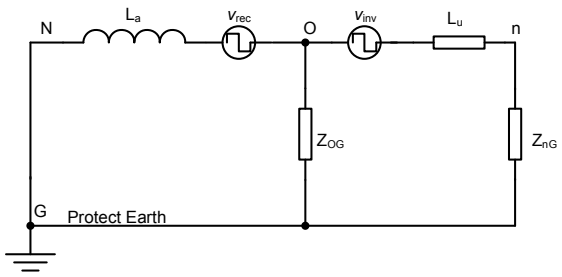


Figure 2.17: Equivalent circuit of PWM inverter system with PWM boost rectifier

Because the CM current is determined by the difference between CM voltages $v_{\rm rec}$ and $v_{\rm inv}$, a strategy is proposed in [Lee00; Lee01] to reduce the CM current, by synchronizing the control signals of the rectifier and the inverter.

From the EMC point of view, the CM EMI produced by a rectifier will overwhelm that produced by the inverter due to the shorter distance to the mains power. The DC-bus midpoint potential fluctuation range is very large with a PWM front end. The CM voltage in the inverter output imposes on the DC-bus midpoint potential fluctuation, which doubles the amplitude of the CM voltage in the load. The increasing CM voltage drastically increases the possibility of bearing deterioration if the motor is used as the load. Also, these transients have very high dv/dt and di/dt, causing interference sources with a very wide spectrum.

2.6 Grounding configurations

There are many grounding methods in drive systems. They are chosen to ensure various requirements, for instance, meeting safety standards, limiting the transient overvoltage to ground, or riding through interrupted processes. In addition, one important aspect of grounding method consideration is its impact on EMC performance.

As explained above, the voltage and current noise sources are affected by the configuration of the rectifier and the inverter. The following discussions are based on the general and idealized grounding method. Changing the grounding configuration will not significantly change the characteristics of the noise sources. Actually, the grounding configuration has impact on the EMC performance by changing the path for high frequency current circulation.

2.6.1 Possible grounding methods

In Figure 2.18, the impedance between the neutral point of AC-source and ground is designated by Z_{NG}. Also, the impedance between the converter frame and ground and the impedance between the motor frame and ground are notated as Z_{FG} and Z_{MG}. Different choices of these impedances give different grounding configurations.

Reference [Das98] discusses the various possibilities of grounding methods for low-voltage and medium-voltage drive systems. Four grounding methods are discussed according to Z_{NG}. They are solidly grounding, low-resistance grounding, high-resistance grounding, and ungrounded systems. Generally, the solidly grounding method is adopted, because of its simplistic structure. The ungrounded system is not a standard due to its uncertain capacitance between phase lines and ground. It is advised in [Das98; Nel99] that a properly implemented high-resistance grounding system should become an industry standard.

In most cases, the motor frame is grounded. Inserting a damping resistor between the motor frame and ground is also an option for Z_{MG} [Mut02].

The grounding configurations mainly influence the current flowing through ground. Therefore, the CM noise is of the most concern. The simplified CM

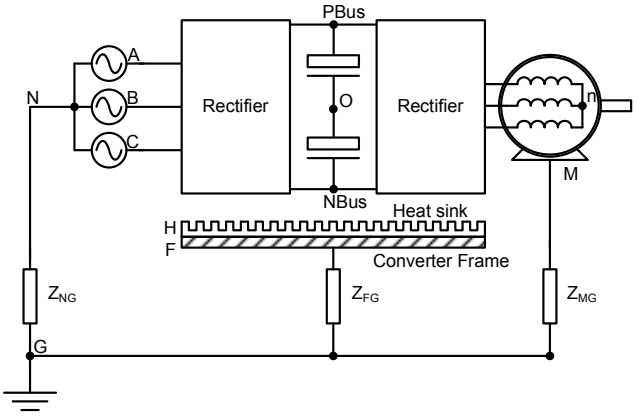


Figure 2.18: Diagram of possible grounding methods

equivalent circuit in Figure 2.19 can be achieved. For this figure, the symbols and relative components are explained in Table 2.1.

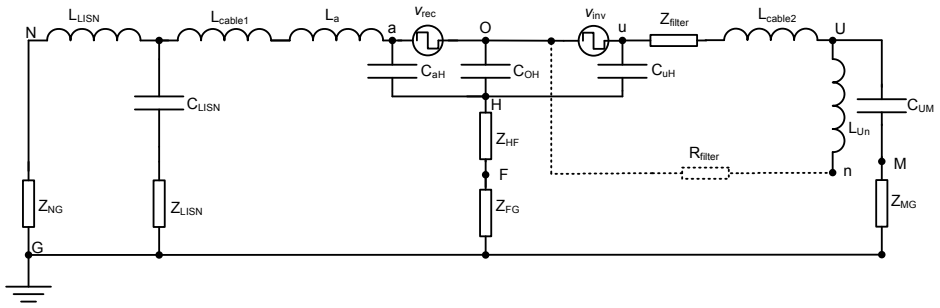


Figure 2.19: CM equivalent circuit used including grounding configuration parameters

2.6.2 The impact on the noise propagation path

EMI is a high frequency noise, and the measurement is normally done with LISN inserted between the mains and the equipment under test (EUT). According to the suggestion in the measurement standard [CIS99b], the earth of the LISNs needs to be tightly connected to the ground plane. The high frequency noise generated by the EUT is bypassed through the LISN, therefore, the Z_{NG} has no influence on the noise propagation path.

Table 2.1: Explanation of the symbols in the CM equivalent circuit

Symbols	Modeled components
L_{LISN}	High frequency blocking inductor in the LISN
Z_{LISN}	Constant measuring impedance in the LISN
C_{LISN}	Bypassing capacitor in the LISN
L_{cable1}	Inductance of the mains cable of converter
L_{cable2}	Inductance of the motor cable of converter
L_a	Boost inductance of the rectifier
L_{Un}	Winding inductance of the motor
C_{aH}	Capacitance between the rectifier input terminals and the heat sink
C_{OH}	Capacitance between the DC-bus and the heat sink
C_{uH}	Capacitance between the inverter output terminals and the heat sink
C_{UM}	Capacitance between the motor winding and the motor frame
Z_{FG}	Impedance between the converter frame and ground
Z_{HF}	Impedance between the heat sink and the converter frame
Z_{NG}	Impedance between the system neutral and ground
Z_{MG}	Impedance between the motor frame and ground
Z_{filter}	Impedance of the output filter of converter
R_{filter}	Resistor between the motor neutral point and the mid-point of DC-bus

On the contrary, Z_{FG} and Z_{MG} have significant impacts on the noise propagation path. When a solid connection is used between the motor frame and the ground, the high frequency current flows through the motor winding to the motor frame and then to ground efficiently. One approach to suppressing the CM current flowing on the motor side is adding the damping impedance in Z_{MG} [Mut02]. Adding damping impedance in Z_{FG} is also helpful when a PWM rectifier is used instead of a diode rectifier. The noise generated by voltage source v_{rec} can be mainly damped by Z_{FG}, while compromises are expected when choosing the right value of Z_{FG} and Z_{MG} since a large Z_{FG} degrades the effect of the Y capacitor installed inside the converter and the value of Z_{MG} is limited by the safety standards of industry.

2.6.3 The impact on the generation of bearing current

The grounding method has impact on the generation of the bearing current. There are several mechanisms which take effect simultaneously in the generation of bearing current. One is called circulating bearing current which is caused by capacitive and magnetic coupling effects [Mue04]. For this parasitic coupling phenomenon, it can be modeled as an equivalent lumped parameter network [Che96]. The grounding method affects this kind of bearing current by changing the component values in the noise propagation path.

The equivalent circuit of the generation of shaft voltage is shown in Figure 2.20. The shaft voltage can be derived easily from the figure,

$$v_{SM} = \frac{C_{US}}{C_{US} + C_{SM}} v_{UM} = K v_{UM} \tag{2.9}$$

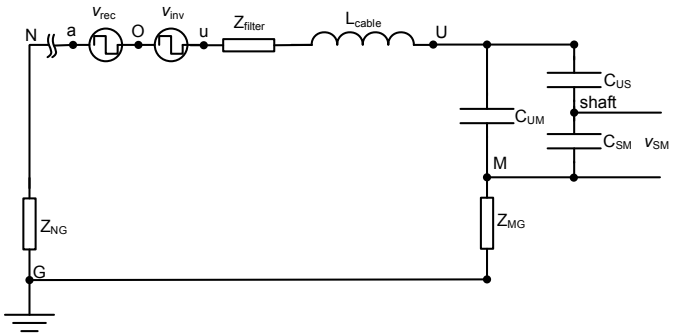


Figure 2.20: The impact of grounding method to circulating bearing current

The coefficient K is a constant according to the motor size and geometry. The voltage v_{UM} is rather dependent on the grounding method. Taken together, the grounding method determines the ratio between the shaft voltage and the

CM voltage of the inverter. With large Z_{MG}, the the circulating bearing current becomes much smaller.

Contrary to circulating bearing current which is caused directly by the high frequency component of CM voltage, the EDM bearing current has another mechanism. It is produced when the amplitude of the CM voltage drop over the motor bearing exceeds the breakdown voltage of the bearing lubricant.

With large Z_{NG} and Z_{MG}, the v_{UM} becomes much smaller, and so does the shaft voltage. This decreases the possibility of the occurrence of an EDM bearing current. It is noted that the impedance of LISN is not included in the equivalent circuit when considering the EDM bearing current. This is because the LISN is equivalent to open circuit in the low frequency range. On the contrary, the LISN impedance conceals the influence of Z_{NG} when considering the circulating bearing current.

2.7 DC-bus configurations

The DC-bus exists in multi-stage AC-AC converters. It can be galvanically connected by filter capacitor or filter inductor. To provide galvanic isolation between the input and the output, a high frequency transformer is sometimes used in the DC-bus.

In a DC-bus with capacitor, the potentials of the two rails of the DC-bus change simultaneously, and so does the midpoint of the DC-bus. The voltage differences between them are fixed as the DC voltage dropped on filter capacitors. Therefore, the DC-bus rails and the midpoint are modeled as the point ''O'' in Figure 2.19.

DC-bus configuration has influence on bearing current by changing the precondition of the generation of the second level effects, for instance, the EDM bearing current. The point ''O'' can be used for suppressing EMI noise. By adding a low impedance R_{filter} between the point ''O'' and the point ''n'', the v_{UM} is much smaller because most of v_{inv} appears across Z_{filter}. This approach is followed by [Aka04a; Aka04b]. Most of the CM noise generated by the inverter can be suppressed. A main drawback as the author mentioned is that the point ''n'' in the motor is not always accessible. For the rectifier, the same idea can be applied. For a diode rectifier, it is not a problem because the noise generated by a diode has a much lower level. For the PWM rectifier, by connecting point ''N'' and ''n'' with a low impedance path, the same goal can be achieved. The point ''N'' is accessible by the star point of the input filter.

When a high frequency transformer is used on the DC-bus, one more inverter and one more rectifier are used. The noise sources created by them are named v_{pri} and v_{sec}. The high frequency model of the DC-DC converter part is shown in Figure 2.21. $L_{\sigma 1}$ and $L_{\sigma 2}$ are the primary and secondary leakage inductance. The coupling capacitor $C_{\text{pri-sec}}$ plays a very important role in the noise current. The noise current may flow through this coupling capacitor between the primary

side and the secondary side of the transformer. As a remedy, a metallic shield winding may be used to reduce the coupling. This arrangement creates the capacitance $C_{\text{pri-sh}}$ between the primary winding and the shield winding, and also the capacitance $C_{\text{sec-sh}}$ between the secondary winding and shield winding. This remedy is helpful if the shield is grounded on the mains side by guiding the noise currents directly to ground [Pau06]. Therefore, less v_{sec} and v_{inv} are transferred to the mains side.

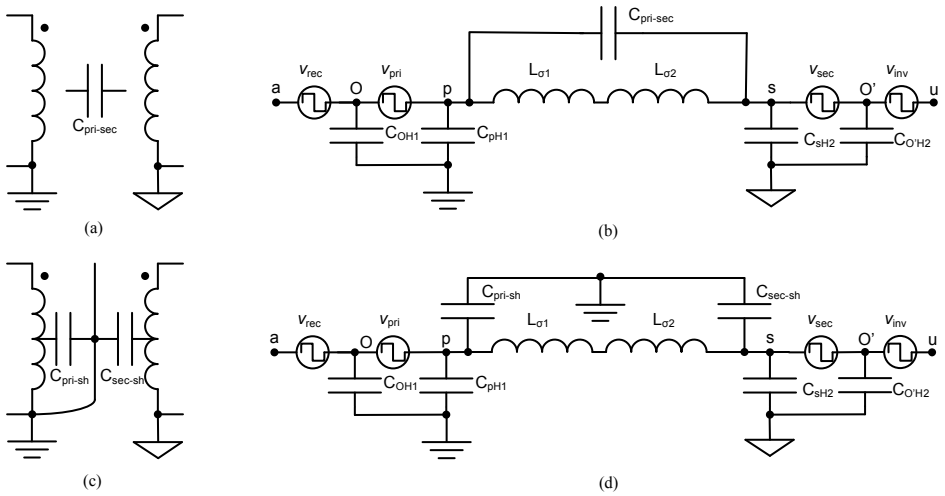


Figure 2.21: The diagram of the model of HF transformer in the DC-bus: (a) without shield winding; (b) model of the transformer without shielding winding; (c) with shield winding; (d) model of the transformer with shielding winding.

2.8 Inverter configurations

In all PWM DC-DC and DC-AC converters listed in Section 2.2, the switches are operated in different modes to turn on and turn off. Hard switching can produce a much higher EMI level than ZVS and zero-current switching (ZCS). The configuration of the converter has an impact on the EMC performance in the noise source.

In hard switching operation mode, the di/dt and dv/dt is largely due to the factor that the switches are turned on when the switch voltage is not zero and turned off when the switch current is not zero. Overvoltage and reverse recovery current of diodes are also causes of EMI.

The ZVS and ZCS conditions can be created by adding resonant components

or snubber circuits. The former is letting the switch load be a resonant circuit, and the latter is shifting stress voltage or current to snubber circuits.

In [Jon90], a new switch control method is proposed by adding a LC-filter between the bridge and the load. The filter lets the transistor current fall back to zero in every switch cycle, so that the ZVS condition is satisfied.

In Figure 2.22, an inverter leg of the ZVS inverter is shown. Initially, i_o is assumed to be flowing through T_+ and L_f, and $v_u = v_{PBus}$. The current i_o is increasing according to

$$\frac{di_o}{dt} = \frac{v_{PBus} - v_{u'}}{L_f}$$

When i_o exceeds a preset value (when the preset value is positive), T_+ is turned off. The current flowing through the freewheel diode D_{T-} decreases, and $v_u = v_{NBus}$. As long as the current falls back to zero, T_- is turned on at zero voltage (ZVS condition), and the diode D_{T-} is turned off at zero current. Therefore, the reverse recovery current is minimized. The benefit of the LC-filter here not only provides ZVS conditions but also filters the pulsating voltage to become a sinusoidal waveform.

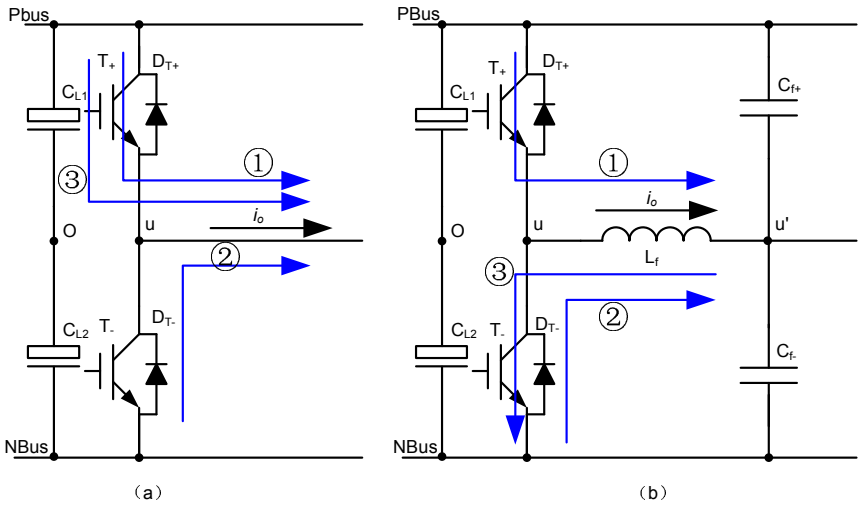


Figure 2.22: Diagram of an inverter leg of: (a) a hard switch inverter; (b) a ZVS switch inverter.

2.9 EMC modeling

From the discussion above, we conclude that the influence of changing the configurations has two effects. One is the impact on the noise source, and the other is on the modification of the propagation path. The noise sources change their amplitude and repetition cycles according to the control scheme and the operating point. Any parasitic components formed by particular configurations can produce essential coupling paths even though the values are small.

The configurations have a significant influence on the final result. Choosing the most suitable EMC design is not an easy task. Previous methods need complete models including the full circuit before achieving EMC prediction. Any evaluations of changes to the configurations requires the calculation to be run from the beginning to end. The interactions between the configurations and the final result are not direct and easy to understand. Therefore, a hierarchical approach is required for an EMC analysis of such complicated, mutable AC-AC converter systems.

2.10 Summary

In this chapter, various configurations of AC-AC converters are considered. The purpose of using AC-AC converters are introduced in Section 2.1. The classification is based on the number of cascaded stages. These are described in Section 2.2 and can be summarized as:

1. Single-stage AC-AC converter topologies (AC-AC)
2. Two-stage AC-AC converter topologies (AC-DC-AC)
3. Three-stage AC-AC converter topologies (AC-DC-AC-AC)
4. Four-stage AC-AC converter topologies (AC-DC-AC-DC-AC)
5. Five-stage AC-AC converter topologies (AC-DC-DC-AC-DC-AC)

The transformation of the voltage forms are indicated between parentheses. The basic conversions of AC-DC and DC-AC are done by a rectifier and an inverter. The DC-DC conversions are inserted in the chain of conversion to change the DC-bus voltage. The AC-AC conversion is adopted in a three stage AC-AC converter to reduce the high frequency to output frequency only. For AC-AC conversion in a single stage AC-AC converter, not only the frequency, but also the amplitude and phases are controlled. The conversion is done by switching and keeps the fundamental components required.

Two mechanisms of coupling are introduced in Section 2.3 and Section 2.4. For analysis of EMI, these subtle coupling paths present the main mechanisms beside the tracks and components shown up explicitly in the circuit. The mechanisms are

explained so that the equivalent circuits and models can be built in the following chapters.

Various configurations of rectifier are used to achieve the same purpose of converting AC to dc. The impact on EMI is considered in Section 2.5. In Section 2.6, the possible grounding methods and their influence on EMI are discussed. There are two DC-bus configurations, with and without a high frequency transformer which change the noise source and propagation path. These are discussed in Section 2.7. The different types of inverters are considered in Section 2.8.

In Section 2.9, the necessity of using a hierarchical approach for EMC analysis is briefly discussed. This is because of the variable and complex interaction characteristics of the AC-AC converter system. The hierarchical approach is proposed in detail and implemented in Chapter 3.

Chapter 3

Hierarchical EMC design procedures

3.1 Introduction

The topologies of various AC-AC converters are described in Chapter 2. Emphasis is placed on how these topologies relate to EMC issues and the mechanisms of noise generation inside AC-AC converters. Available suppression remedies are reviewed.

In this chapter, a hierarchical approach for better EMI modeling in AC-AC converters is presented. The approach is based on dividing the causal chain into segments, in order to avoid the bi-directional interaction between cause and result. Therefore, straightforward calculation becomes possible and it gives more insight into how the noise level can be suppressed. It is not necessary to start from the beginning to calculate the EMI level after some parameters have been modified. This helps us to compare several setups within a reasonable time-frame.

In Section 3.2, the difficulties of EMI modeling of the AC-AC converters due to the special characteristics of the applications are pointed out. Present methods of EMC design are reviewed next, and advantages and disadvantages are compared.

The feasibility of the proposed hierarchical approach is discussed in Section 3.3. The assumptions of using the approach are figured out and proven to be acceptable. The steps to applying this approach are also laid out in this section.

The concrete steps are described from Section 3.4 till Section 3.6. The chapter is summarized in Section 3.7.

3.2 Present EMI modeling methods

In an AC-AC converter, several timescales exist.

In the filtered output voltage and load current, the concerned time constants are in the range as long as 20 ms and as short as 500 μs. In the frequency domain, it corresponds with the range between 50 Hz and 2 kHz (40th harmonic of fundamental frequency). This timescale is important to determine the overall mission of the system, for instance, the working frequency and amplitude of the power supply for load. It is concerned by specifications, for instance, the harmonic requirements of EMC and the power factor requirement. The time constant on this level can last even longer than several seconds or hours if we consider long term effects, such as acceleration process or the temperature rising before stabilization.

Inside the converter, the time constant ranges from the sampling time to generate the switching waveform to the switching period. The value is in the range as long as 500 μs and as short as 2 μs (depending on PWM frequency) and corresponds to a frequency range between 2 kHz and 500 kHz. This timescale is important for the duty cycle calculation and switching waveform generation. It concerns the low frequency range part of the EMC requirement.

In this thesis, these two timescales are named ''functional level'' because they relate to the function realization of a converter.

For components of the converter, the time constant ranges from 2 μs to 10ns for normal applications of AC-AC converters. The corresponding characteristic frequency ranges from 500 kHz to 100 MHz. In this range, the phenomena of interest include turn-on and turn-off transients and ringing. It concerns the high frequency range part of the EMC requirement.

The level using this timescale is called transient level because transient is most concerned.

In power electronic applications, we are facing the difficult task of EMI modeling in the presence of large differences between the time constants which span several orders of magnitude.

The present methods used in EMI modeling can be classified into two kinds according to the working domain: time domain method and frequency domain method. The time domain method is based on a switch model and the frequency domain method is based on a noise source model.

3.2.1 Time domain method

In a time domain method, the switching devices are modeled by ideal switches and other components to simulate the behavior of the switches.

This method is applied to the EMC analysis of DC-DC converters [Lab96; Lee99; Xu91; Swa95] and seldom used in AC-AC converters. This is due to the long time constants on the functional level of an AC-AC converter compared to a DC-DC converter. The time constant of an AC-AC converter is normally several

milliseconds, which means that the simulation must run for a long time to avoid missing the ''worst'' situation of interference.

The large difference between the time constants implies that we need to take very small time steps to get a sufficiently accurate EMI model at high frequencies. Assuming the calculation lasts for 5 periods, which is 100 ms for 50 Hz working frequency, at least 100 ms/10 ns= 1×10^7 points are needed to calculate the final result. This requires huge amounts of space for data storage and a long computation time to process the data. This makes it almost impossible to evaluate the impact of EMC performance if there is a slight change in component values, because the calculation has to then be done from the beginning which makes the optimization of components values very difficult.

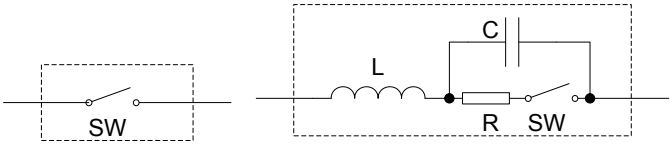
In reference [Won01], the switch model is used for a three-phase motor drive. This simulation was repeated on a generally configured desktop computer and it took 53 minutes to get a set of simulation results that include a detailed spectrum in the full conducted emission frequency range.

One extreme approach is to assume that the transient time is instantaneous and the switches are idealized. An ideal switch in ''on'' state is an ideal conductor and in ''off'' state it is an ideal isolator. This property can be described as:

$$R_{SW} = \begin{cases} 0 & \text{on} \\ \infty & \text{off} \end{cases} \tag{3.1}$$

Actually, the idealized diode and transistor do not exist in the real world. The idealization makes the analysis much simpler. Unfortunately, it distorts the waveform of voltage and current in the commutation period. What is missing is a very important part for EMC analysis and prediction.

Therefore, some papers propose an updated switch model by adding a few passive elements around the ideal switch [Mug01]. A comparison between the idealized switch model and enhanced switch model are shown in Figure 3.1.



(a) Idealized switch (b) Enhanced switch model

Figure 3.1: Switch model of EMI modeling time domain methods

The benefit is that the state-variable method can still be applied for analysis. The disadvantage is that the shape of the waveforms of the voltage and current during the transient time are not exactly the same as that in measurement. For instance, in an inverter leg such as the one illustrated in Figure 3.2, the voltage

waveform v_{ds} and current waveform i_d change exponentially, which is not realistic. Also, many details, for instance, the reverse recovery current, are missing using this approach, as shown in Figure 3.3.

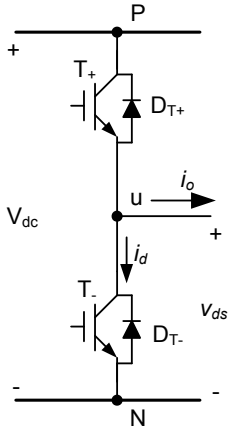
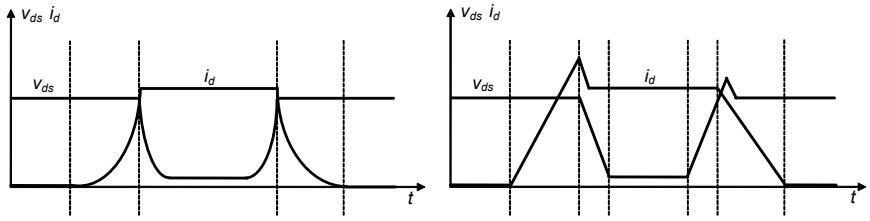


Figure 3.2: An inverter leg of voltage-source inverter



(a) Using switch model (b) In measurement

Figure 3.3: Comparison between typical current and voltage waveforms during commutation

Therefore, to achieve an accurate simulation, complex behavior models not only for switches but also for all components inside the inverter are needed. This needs to be done in an analytical or numerical way [Han05; Che03]. It requires quite a time-consuming time-domain analysis with tiny steps. The noise spectrum is calculated with a fast Fourier transform (FFT). The time domain simulation needs to run for a long time to reach a steady state first. As we know, in circuit simulation, the network equation contains an increasing amount of variables as the number of the circuit elements increases. Therefore, a pure time domain approach has an unavoidable disadvantage.

3.2.2 Frequency domain method

Due to the limitation of the time domain method, the trend of EMI modeling is work in the frequency domain. In [Nav91], the frequency domain method is used for a DC-DC converter. The CM noise is modeled as a voltage source and the DM noise is modeled as a current source. The model is quite simple and many parasitic parameters are not considered. In [Ran98], the frequency domain model is used for the first time in a motor drive. The voltage source is used as the source of DM noise instead of the current source. The voltage source must include the source impedance according to the mechanism of DM generation. In [Hua04], the frequency domain EMI prediction method is introduced considering all parasitic parameters. It is a pity that the motor drive is connected to a DC power supply in the model and validation measurement, which is different from the real installation situation. In the extended work done by [Liu05], the same setup as in [Hua04] is used. To make the analysis simpler, the connection to an AC-grid is avoided. It shows the limitations of the present method, that is, only the worst case is considered.

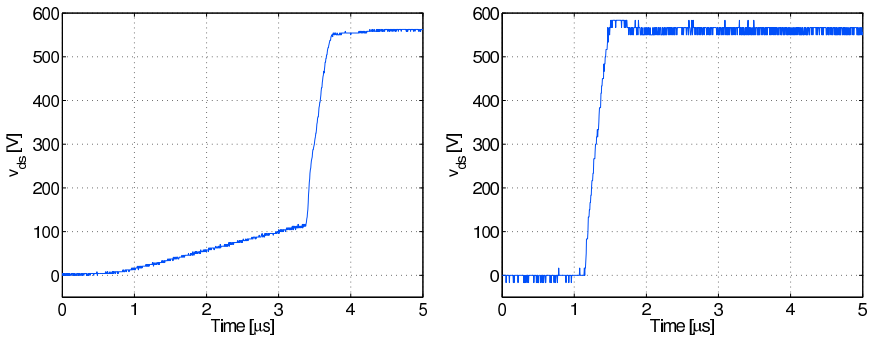
The components other than the noise source can be modeled by an experimental approach, which uses the network analyzer to provide the signal propagation property. Therefore, the EMI modeling process skips the analysis of noise propagation, and only the noise source is left for EMI modeling. The problem with this method is that it is only feasible after that a prototype is built. This method was first introduced in [Che98] and [Che00]. In [Gon03] and [Liu05], the noise source and the propagation paths are modeled in the frequency domain. The propagation paths are expressed by an impedance matrix. This method is named ''modular-terminal-behavioral (MTB) equivalent EMI noise source''.

A shortcoming of the frequency domain method is that the noise source is always modeled as a trapezoidal periodic waveform which is just an approximation. The turn-on and turn-off are idealized. In reality, the turn-on and turn-off dynamics are a nonlinear transient consisting of several stages [Men06], and the di/dt and dv/dt are not constant, but change with the load situation.

In Figure 3.4, the voltage waveform during a commutation of a PWM VSI is measured. The trigger is set to different current levels. It can be easily observed that dv/dt changes significantly with the load current. In Figure 3.4(a), the transient consists of a fast slope and a slow slope. The slow slope transient occurs when a transistor is turned off with a low load current. This results in a transient that is even longer than the deadtime. This causes the terminal voltage to be rapidly driven to the bus voltage by the turn-on of complementary transistor at the end of the dead time. In this case, the fast slope determines the EMI level. Simplified noise source would not give accurate results.

Another limit on using the pure frequency domain method is that the propagation path is fixed. In reality, the propagation path changes with the operating point [Men04b].

A new topology of ZVS PWM converter has been introduced in motor drives [Jon90].



(a) load current is 0.5A (b) load current is 6.6A

Figure 3.4: Variation of the voltage transient waveforms

The switching frequency is not a fixed value for this topology. A quantitative investigation has never been done on the EMC performance of such motor drives because the noise source is no longer periodic. The design of a proper filter is a challenge for such variable frequency converters. The pure frequency domain method has its limitations for such applications.

3.2.3 Demand of new approach

In a word, the time domain method assumes that the system is linear between two switching events, while the frequency domain method assumes the system is invariable all the time. The frequency domain method cannot be used for modeling on the functional level. Comparing the time domain method with the frequency domain method, the frequency method has a shorter computation duration while time domain method is more accurate with a small time step. Finally, the frequency domain method is much easier to be verified by measurement.

We would like to build a hierarchical method for analyzing the EMC problem of AC-AC converters in this thesis. This method is a combination of the time domain method and frequency domain method. The purpose is to achieve accurate EMI modeling and prediction for wider AC-AC converter applications by applying the most suitable methods under different conditions.

3.3 Approach to a hierarchical EMC design procedure

There are several reasons for using the hierarchical method to analyze EMC issues in AC-AC converters. This is because of the following properties of AC-AC converters:

- The voltage and current waveforms over a large timescale can be approximated by straight line segments.
- In a small timescale, the edges of the voltage and current waveforms have variable rise and fall times. They consist of several straight line segments with different slopes. The transient times of these edges are much shorter compared to the switching periods.
- Most of the transient waveforms are accompanied by a ringing phenomenon.
- The ringing signal lasts much shorter than the switching period or fundamental period. Mostly, the ringing signal decays to zero before the next transient event.
- The ringing signal generated by parasitic elements has much smaller amplitude than the working voltage or current. The working voltage or current are in the order of 100 V and 10 A, and the ringing signals are in the order of 10 V and 0.1 A [Cos94].

Therefore, we do not need to consider the ringing phenomenon when we calculate the transient. The transient is the noise source that generates the ringing signal, but the ring signal has a negligible influence on the transient. The shape and amplitude of the transient are determined on the functional level. One exception occurs when the next transient comes so early that the previous transient has not decayed completely. Under this situation, the parasitic signals are overlapping. This gives us a criterion to simplify the circuit when we calculate the transient, that is, the components with a much shorter time constant than the switching period can be ignored. The models of the transistors can be entirely simplified on the functional level. The result obtained by a simplified model should be the same as the result obtained by complicated models.

On the functional level, the state of transistors and their operating points can be determined. The transients on the functional level are idealized with a zero transient time. On the transient level, the slopes during the transients can be calculated based on the information obtained on the functional level. The shapes and slopes of the transients have impacts on the final EMC result. It can enhance or decrease the EMI level at certain frequencies. The transient waveform can be expressed by the convolution of two waveforms in the time domain. The first one is the piecewise linear waveform obtained on the functional level. The second one is the normalized derivative of the transient. The spectrum of the first waveform can be efficiently obtained by using an analytical approach. Due to its aperiodic nature, the spectrum of the second term is obtained by using the Laplace transform. The convolution in the time domain brings about a multiplication in the frequency domain. The multiplication can be simplified to an addition because a logarithmic scale is used on the noise level axis. The determination of the shapes and slopes of the transients is a task on the transient level.

Figure 3.5 illustrates general current and voltage waveforms of a switch in an inverter leg. As indicated, the time axis is divided into three kinds of zones: edge, ringing and steady state. One thing to keep in mind is that the time axis is truncated in the figure during the steady zone due to its long duration. The value of the voltage or current during the steady zone is not necessarily constant, but compared to the edge, the amplitude changes really slowly. Therefore, it can be regarded as unchanged.

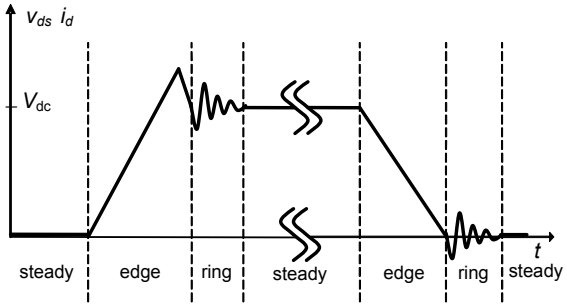


Figure 3.5: General current and voltage waveforms in one inverter leg of a three-phase inverter

On the propagation level, the noise measured at the LISN and at the noise source are related closely in the frequency domain. For multi-phase applications, the time is divided into shorter time intervals by taking the transients in each phase into account. The inverter legs provide a noise propagation path for the noise source. The propagation path is the time-invariant linear network between two adjacent switching events. On the other hand, the path changes at each switching event due to the state changing of the switches in the inverter legs. In Figure 3.6, it is illustrated how inverter legs take part in noise propagation. The switch event occurs at one inverter leg at a given moment. It spreads out through the propagation path inside the inverter system. Therefore, waveforms with similar shape appear in other two inverter legs. The influence of this switching event decays and then the next switching event occurs in another inverter leg.

We have the following reasons to develop a new approach:

- The topology changes with the transients when the switch turns on or turns off. This changes the propagation path. If diodes are included in the propagation path, the topology is also changed by the conduction of the diodes. The variable topology causes great difficulty for a pure frequency domain method.

- The parameters of components are not fixed. The voltage and current amplitudes are not constant for AC-AC application. Many parasitic pa-

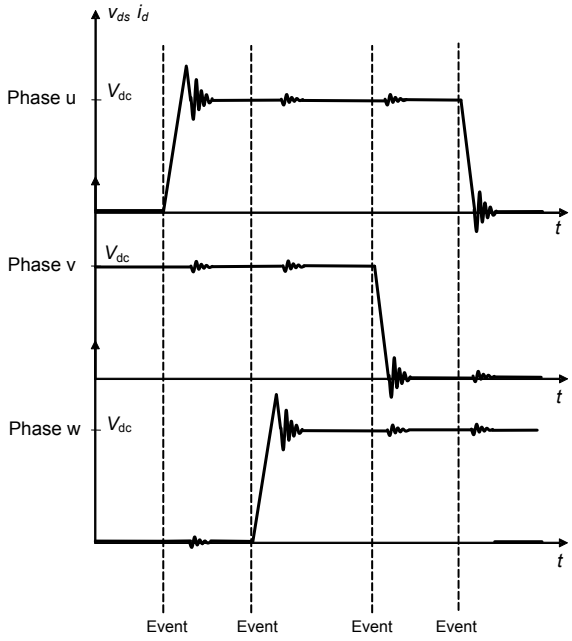


Figure 3.6: General current and voltage waveforms in each inverter leg of a three-phase inverter

rameters are affected by the values of voltage and current. This can have a significant impact on the noise propagation path.

Therefore, the frequency spectrum can be obtained in each time interval between switching events. In previous work [Ran98], to simplify the analysis, conduction patterns are identified, and one worst-case scenario is used to predict the EMI level. The result of using a peak (Pk) detector can be obtained using this ''worst-case scenario'' approach with overestimation, but the EMI receiver with average (Av) and quasi-peak (QP) detectors, which are also used as a standard measurement setup cannot be simulated. Using the hierarchical method, the results of the Av and QP detectors can also be provided.

The procedures of hierarchical EMC analysis approach are summaried in Figure 3.7 shown below. In the following sections, the hierarchical EMC analysis approach is explained in detail. This approach is applied to predict the EMI level of a variable speed motor drive system.

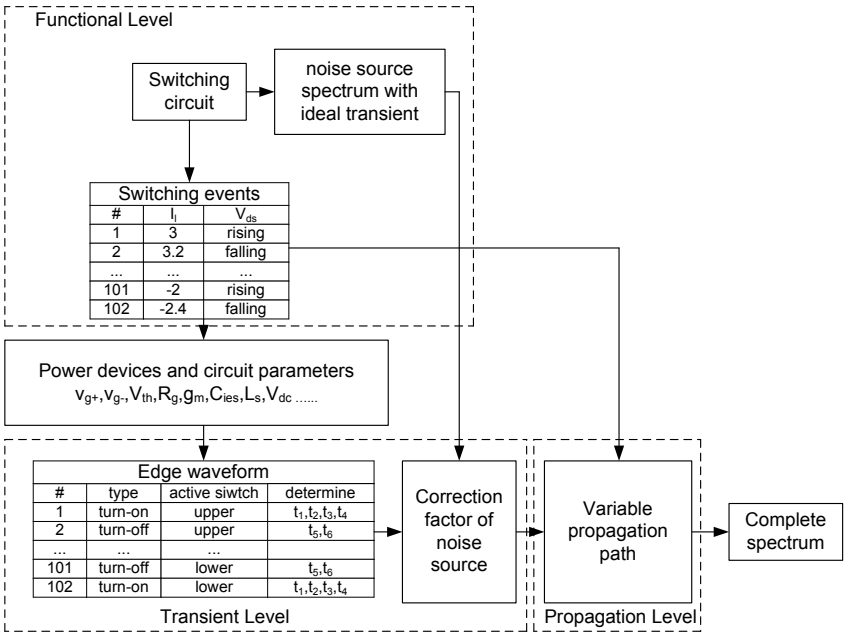


Figure 3.7: Flow chart of hierarchical EMC design procedures

3.4 Functional level

On this level, the main purpose is to obtain the operation condition of the steady period. It also gives the frequency spectrum of the lower frequency part.

Here, it is proved that replacing the edge with an infinite slope will not change the spectrum in the low frequency part. The boundary of a low frequency part is also derived.

As we know, any signal can be treated as the convolution of a step signal and the normalized derivative of the signal itself, as shown in Figure 3.8. The narrow pulses in the derivative signal $f_1'(t)$ can be approximated by the impulses $f_2'(t)$ at the bottom of Figure 3.8(b). This approximation is valid for a given frequency range when the maximum width τ_{max} of these replaced pulses satisfies the following criterion:

$$\pi f \tau_{max} < 1 \tag{3.2}$$

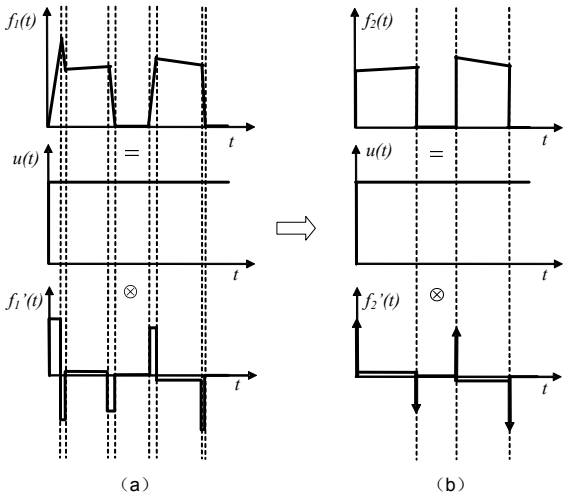


Figure 3.8: A typical waveform treated by the convolution of two waveforms

Two wider pulses are not replaced by impulses. Otherwise τ_{max} will be much larger. The waveform is convoluted again with the step signal and we obtain the signal $f_2(t)$. That means that the transient can be replaced by an ideal edge with an infinite slope rate. This approximation is valid in the frequency range up to f_{max}. By rewriting Equation (3.2) to Equation (3.3), we get:

$$f_{max} < \frac{1}{\pi \tau_{max}} \tag{3.3}$$

In the low frequency range, when Equation (3.3) is satisfied, the signal can be approximated by an infinite slope edge. The calculation of the spectrum in the low frequency range can be simplified and be calculated separately.

On the functional level, we need to obtain the information by the fastest approach since the timescale is the longest. Several approaches are available for this purpose. The first approach is the switching function method. The switches are modeled as switching functions. These switching functions are used as inputs to calculate the load current and voltage. As shown in Figure 3.9, this method is valid only for an open loop controlled inverter.

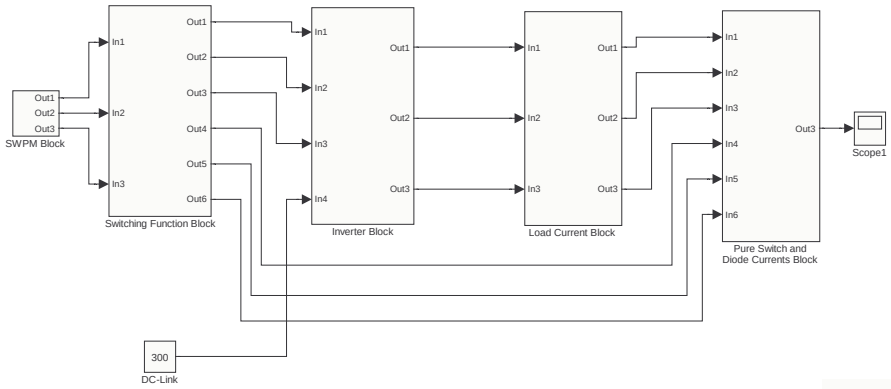


Figure 3.9: The switching function method on the functional level

The second approach is the idealized switch model, which was introduced in Subsection 3.2.1 as the time domain method.

These two methods achieve the result in the time domain and then transfer the result to frequency domain. In the next section, analytical and FFT approaches are also introduced.

3.4.1 PWM output voltage spectrum

The procedure to calculate the harmonic components of the PWM output voltage in an analytical way can be found in much research literature, like [Hol03; Gon03]. The benefit is that the amplitude of harmonic components can be expressed by closed-form equations.

Observing the PWM switched waveform $f(x, y)$, it is a time-varying waveform that contains two time variables, $x(t) = \omega_c t + \theta_c$ and $y(t) = \omega_0 t + \theta_0$, here

ω_c is the carrier angular frequency,
ω_0 is the fundamental angular frequency,

θ_c is the phase offset angle for carrier waveform,
θ_0 is the phase offset angle for fundamental waveform.

For a double time-variable periodic signal, the double Fourier integral approach is used to calculate the harmonic components. The PWM switched waveform can be expressed by an infinite series of two-dimensional sinusoidal harmonics,

$$\begin{aligned} f(x,y) &= A_{00} + \sum_{n=1}^{\infty}[A_{0n}\cos(ny) + B_{0n}\sin(ny)] \\ &\quad + \sum_{m=1}^{\infty}[A_{m0}\cos(mx) + B_{m0}\sin(mx)] \\ &\quad + \sum_{m=1}^{\infty}\sum_{n=-\infty,n\neq 0}^{\infty}[A_{mn}\cos(mx+ny) + B_{mn}\sin(mx+ny)] \end{aligned} \tag{3.4}$$

here,

$$A_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\cos(mx+ny)\mathrm{d}x\mathrm{d}y \tag{3.5}$$

$$B_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\sin(mx+ny)\mathrm{d}x\mathrm{d}y \tag{3.6}$$

The integral can be solved using the Jacobi-Anger expansion and expressed by the first kind of Bessel function.

In PWM schemes, instead of a sinusoidal reference signal, zero sequence signals of the third harmonic frequency are added to the reference signals to reduce current ripple and increase the amount of line-to-line voltage. For such continuous and discontinuous modulation, the integration must be done in segments. Normally, the inner interval $[-\pi, \pi]$ is replaced by a function of $y(t)$ according to different modulation schemes. The harmonic coefficients calculated by (3.5) and (3.6) change from one PWM strategy to another. The derivation procedures are quite complex. It aggravates the complexity of the closed-form expression.

An alternative approach uses the FFT method, which has been proven to be faster and more efficient. The waveform can be calculated according to the particular PWM scheme. Then, the waveform is converted to frequency domain using FFT. The FFT module is very efficient because the algorithm has already been optimized to support large problem calculations.

3.4.2 Induction motor operating point determination

When an induction motor is used as a load, the equivalent circuit in the fundamental frequency is shown in Figure 3.10, here

X_1 is the stator leakage reactance,
X_2 is the rotor leakage reactance referred to the stator,

R_1 is the stator effective resistance,
R_2 is the rotor resistance referred to the stator,
R_c is the core-loss resistance,
X_m is the magnetizing reactance,
s is the fractional slip.

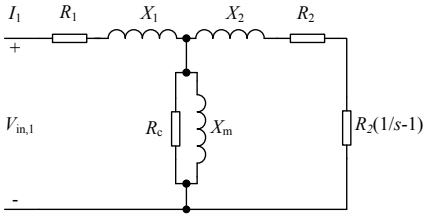


Figure 3.10: Per-phase equivalent circuit of the fundamental voltage

The values of the parameters of the induction model can be extracted using an experimental method. A standard test procedure for this measurement is suggested by [IEE04].

The torque-slip relationship can be expressed by [Fit02],

$$T_{\text{mech}} = \frac{1}{\omega_s}\left[\frac{n_{\text{ph}} V_{1,\text{eq}}^2 (R_2/s)}{(R_{1,\text{eq}} + (R_2/s))^2 + (X_{1,\text{eq}} + X_2)^2}\right] \tag{3.7}$$

here,

T_{mech} is the electromechanical torque,
n_{ph} is the number of stator phases,
$V_{1,\text{eq}}$ is the Thévenin-equivalent source voltage,
$R_{1,\text{eq}}$ is the resistance part of Thévenin-equivalent stator impedance,
$X_{1,\text{eq}}$ is the reactance part of Thévenin-equivalent stator impedance,
ω_s is the synchronous mechanical angular velocity.

In the equation, $V_{1,\text{eq}}$, $R_{1,\text{eq}}$ and $X_{1,\text{eq}}$ are calculated by

$$V_{1,\text{eq}} = V_{\text{in},1}\left(\frac{jX_m}{R_1 + j(X_1 + X_m)}\right) \tag{3.8}$$

here,

$V_{\text{in},1}$ is the fundamental component of source voltage.

$$R_{1,\mathrm{eq}} = \mathrm{Re}\left(\frac{jX_m(R_1 + jX_1)}{R_1 + j(X_1 + X_m)}\right) \tag{3.9}$$

$$X_{1,\mathrm{eq}} = \mathrm{Im}\left(\frac{jX_m(R_1 + jX_1)}{R_1 + j(X_1 + X_m)}\right) \tag{3.10}$$

The curve is drawn with load characteristic in Figure 3.11.

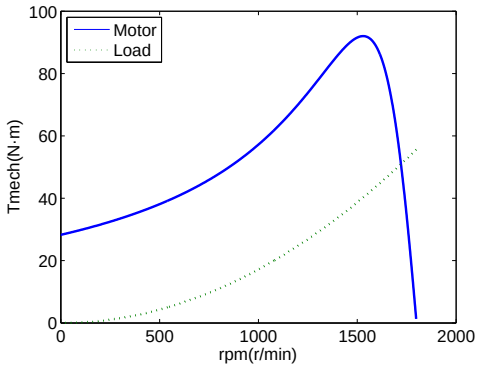


Figure 3.11: Torque-speed characteristics of the induction motor and the load

The cross point is the operating point when steady-state is reached. Since the asynchronous mechanical angular velocity ω_m is given, then s can be derived. This completes the model for the fundamental frequency.

3.4.3 PWM output current spectrum

The fundamental component of PWM output current is derived. For each harmonic component, the PWM output current can be calculated using the equivalent circuits of the motor in harmonic frequencies shown in Figure 3.12.

At harmonic frequencies, the magnetizing components can be neglected. the rotor slip relative to the synchronous speed at harmonic frequency is

$$s_h = \frac{h - (1 - s)}{h} \approx \frac{h - 1}{h} \approx 1 \tag{3.11}$$

Therefore,

$$I_h = \left(\frac{V_h}{R_1 + hX_1 + hX_2 + R_2}\right) \tag{3.12}$$

Here the motor leakage reactances X_1 and X_2 are assumed to be invariant with the frequency [Moh03].

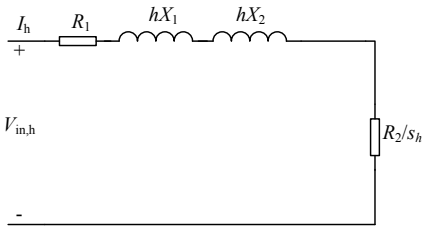


Figure 3.12: Per-phase equivalent circuit of h-th harmonic frequencies

With the frequency spectrum and phase information of the output current, the waveform of the output current can be reconstructed by summing up all harmonics.

$$i(t) = \sum_{h=1}^{\lfloor N/2 \rfloor} I_h e^{jh\omega t} \tag{3.13}$$

The output current can also be reconstructed by inverse FFT. The speed of these two approaches is compared below. It is based on a PWM inverter working at f_0=50 Hz and the frequency modulation ratio m_f is 99. The sampling time interval T_s is set to 1/20 of the switching period, that is 1.0101 μs. The harmonics are assembled at the end and compared with the original signal.

Table 3.1: Time cost comparison for calculating the output current waveform

Steps	Analytical Approach	FFT Approach
Step1: Preparing data (s)	0.03	0.64
Step2: Calculating spectrum (s)	1.78	0.13
Step3: Reassembling signal (s)	48.03	0.31

We notice from the table that the analytical approach uses much more time than the FFT approach to reassemble all harmonics of the output current waveform. The cost of the FFT approach is using a bit more time in preparing the original data. Of course, the analytical approach can be speeded up by increasing the coding efficiency.

3.4.4 Switching events

We obtain the current and voltage waveforms. In the voltage source inverter, the switching events occur at each voltage transient. The information of operating points is recorded for each switching event.

A partial example of a switching events file is given in Table 3.2. The current and voltage at the moments when transients occur are recorded.

Table 3.2: An example of switching events list

Event	i_{load}	v_a	v_b	v_c	Type	v_u	v_v	v_w
10	-22.0	24.8	-281.0	256.2	turn-on	-253.8	253.8	253.8
11	8.1	29.7	-283.1	253.4	turn-off	-253.8	-253.8	253.8
12	22.8	33.0	-284.4	251.4	turn-off	-253.8	-253.8	-253.8
13	18.5	35.1	-285.3	250.2	turn-on	253.8	-253.8	-253.8
14	-4.0	38.2	-286.5	248.2	turn-off	253.8	-253.8	253.8
15	-24.7	43.3	-288.5	245.2	turn-off	253.8	253.8	253.8

3.5 Transient level

In literature, the modeling of a converter is normally done in two steps. The first step is to build the model including all parasitic elements, ensuring the model is accurate. The second step is to simplify the detailed model. The purpose of the simplification is to find the ''worst-case scenario'' for the whole circuit and also to reduce the computation tiime. A good understanding of the mechanism of noise generation and propagation is necessary for the first step. In addition, a lot of experience is needed to know which elements can be omitted, and which elements are crucial to get an acceptable result.

To simplify the analysis, conventional approaches use a voltage source to derive the CM equivalent circuit and a current source to derive the DM equivalent circuit. This is a realistic approximation. In [Zha98; Men04a], it is shown that the voltage source can also generate DM noise, which is named MM noise. Also, the current source can generate CM current flowing through ground [Hua04].

These cross conversions are understandable since the propagation path is not symmetric. This factor is very common in an AC-AC converter application. Actually, simplification is not necessary if the noise conversion can be calculated efficiently. We do not need to treat the noise mode into CM and DM respectively. Here the basic noise cell is proposed for this purpose.

3.5.1 Basic noise cell model

An inverter leg is used to illustrate the basic noise cell model. The basic noise cell is shown in Figure 3.13. The model is described here,

- The switching active components are the noise sources. The high di/dt and dv/dt associated with the switching actions are the main cause of emissions. They are modeled as voltage and current sources corresponding to the fast transients of voltage and current.

- The freewheel diodes connected to the active components are modeled as controlled sources.
- All parasitic components are included.
- For each basic noise cell, the operating points when the switching occurs are applied for transient analysis of the noise.

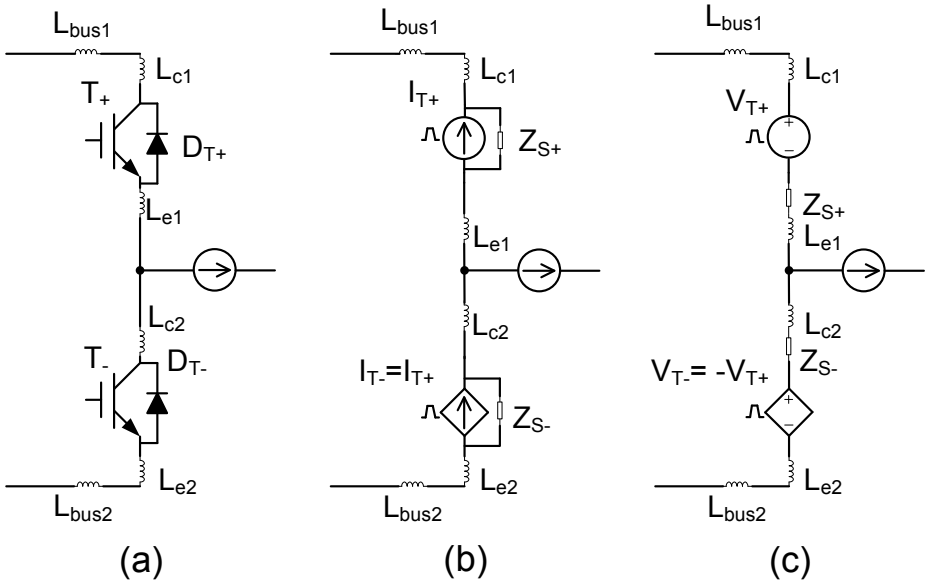


Figure 3.13: Noise cell model; (a) diagram of inverter leg, (b) current noise source model, (c) voltage noise source model

The reason for modeling the freewheel diode as a current controlled current source as shown in Figure 3.13 is because of the following equation:

$$i_{T-} = i_{T+} + i_{\text{load}} \tag{3.14}$$

i_{T-} and i_{T+} have the same polarity of variation. Therefore, the coefficient of the control source is 1.

The coefficient -1 in the voltage controlled voltage source of the freewheel diode is because the voltage dropping on the upper switch satisfies the follow equation,

$$v_{T-} = V_{\text{dc}} - v_{T+} \tag{3.15}$$

v_{T-} and v_{T+} have the reverse polarity of variation.

3.5.2 Slope of the transients

We know the current and voltage waveforms from the analysis on the functional level. The switching devices are then replaced by voltage and current sources. Traditionally, the switching transients are modeled as voltage and current sources with fixed dv/dt and di/dt slopes. Actually, these switching transients are a superposition of several transients with different slopes [Men06], and the slopes of the transients also change with the load current and the parameters of the switching devices. This means the model of the noise source in high frequency should take the operating points into account.

The current waveform can be derived from this expression:

$$i_{\text{up\_sw}} = \begin{cases} i_{\text{load}} & v_{\text{output}} > 0 \\ 0 & v_{\text{output}} = 0 \end{cases} \tag{3.16}$$

$$i_{\text{lo\_sw}} = \begin{cases} 0 & v_{\text{output}} > 0 \\ i_{\text{load}} & v_{\text{output}} = 0 \end{cases} \tag{3.17}$$

The transient edges of the current and voltage are replaced according to the following rules:

- If the load current $i_{\text{load}} > 0$, then the active switch is the upper one. When v_{output} rises from low to high, the current and voltage edges are replaced by the turn-on transient waveforms. When v_{output} drops from high to low, the current and voltage edges are replaced by the turn-off transient waveforms.

- If the load current $i_{\text{load}} < 0$, then the active switch is the lower one. When v_{output} rises from low to high, the current and voltage edges are replaced by the turn-off transient waveforms. When v_{output} drops from high to low, the current and voltage edges are replaced by the turn-on transient waveforms.

For each IGBT switching event, the transient waveforms are sketched in Figure 3.14. The nonlinear behavior model is based on the discussion in [Men06]. The slow tails of the transients are ignored because it has been proved by simulation that ignoring these tails with slow slopes would not has significant influence on the noise frequency spectrum. The turn-on transient waveform which is illustrated on the left of Figure 3.14 is first analyzed.

During t_1, the i_d increases linearly with a slope which can be calculated by

$$\left(\frac{di_d}{dt}\right)_{t_1} = \frac{g_m(v_{g+} - V_{th})}{R_g C_{ies} + g_m L_s} \tag{3.18}$$

here,

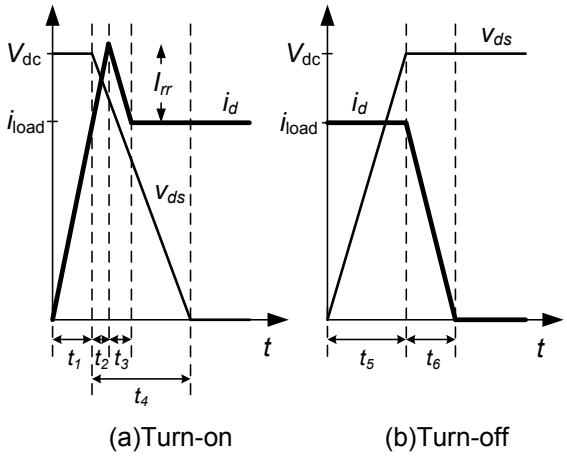


Figure 3.14: Transient switching waveforms

v_{g+} is the on-state gate voltage,
V_{th} is the gate threshold voltage,
R_g is the IGBT gate resistor,
C_{ies} is the IGBT input capacitance,
L_s is the IGBT stray inductance,
g_m is the IGBT transconductance.

The g_m can be derived from the typical transfer characteristic curve in datasheet by

$$g_m = \frac{\Delta i_d}{\Delta v_{ge}} \tag{3.19}$$

The duration of t_1 is calculated by,

$$t_1 = i_{\text{load}} / \left(\frac{di_d}{dt} \right)_{t_1} \tag{3.20}$$

here,

i_{load} is the inductive load current,

In most datasheets of IGBT, the diode reverse recovery time t_{rr0} and peak reverse current I_{rr0} are measured under a standard test configuration with fixed load current I_F and change ratio of the load current $\frac{dI_F}{dt}$. From [Moh03], the following relationships exist,

$$t_{rr}, I_{rr} \propto \sqrt{i_d} \tag{3.21}$$

$$1/t_{rr}, I_{rr} \propto \sqrt{\left(\frac{di_d}{dt}\right)_{t_1}} \tag{3.22}$$

We can calculate the diode reverse recovery time t_{rr} and peak reverse current I_{rr} by,

$$I_{rr} = I_{rr0}\sqrt{\frac{i_{\text{load}}\left(\frac{di_d}{dt}\right)_{t_1}}{I_F(\frac{dI_F}{dt})}} \tag{3.23}$$

$$t_{rr} = t_{rr0}\sqrt{\frac{i_{\text{load}}\left(\frac{dI_F}{dt}\right)}{I_F(\frac{di_d}{dt})_{t_1}}} \tag{3.24}$$

During t_2, the i_d changes from i_{load} to $i_{\text{load}} + I_{rr}$ with the same slope.

$$\left(\frac{di_d}{dt}\right)_{t_2} = \left(\frac{di_d}{dt}\right)_{t_1} \tag{3.25}$$

The time duration for i_d rushing to the top is

$$t_2 = I_{rr}/\left(\frac{di_d}{dt}\right)_{t_2} \tag{3.26}$$

The time for i_d backing to the i_{load} is

$$t_3 = t_{rr} - t_2 \tag{3.27}$$

During t_4, the v_{ds} decreases to zero in a slope of

$$\left(\frac{dv_{ds}}{dt}\right)_{t_4} = \frac{-1}{C_{cg}}\left\{\frac{v_{g+} - V_{th} - i_{\text{load}}/g_m}{R_g} + \frac{C_{ge}}{g_m}\left(\frac{di_d}{dt}\right)_{t_1}\right\} \tag{3.28}$$

The duration of t_4 is calculated by,

$$t_4 = V_{\text{dc}}/\left(\frac{dv_{ds}}{dt}\right)_{t_4} \tag{3.29}$$

here,

V_{dc} is the voltage in DC-bus.

The turn-off transient which is illustrated in the right-hand figure is analyzed below. During t_5, the v_{ds} increases from zero to $V_{\rm dc}$, the slope is,

$$\left(\frac{dv_{ds}}{dt}\right)_{t_5} = \frac{V_{th} - v_{g-} + i_{\rm load}/g_m}{R_g C_{cg}} \tag{3.30}$$

here,

v_{g-} is the off-state gate voltage.

The duration of t_5 is calculated by,

$$t_5 = V_{\rm dc} / \left(\frac{dv_{ds}}{dt}\right)_{t_5} \tag{3.31}$$

The overvoltage of v_{ds} is ignored in the noise model. If the v_{ds} reaches $V_{\rm dc}$, then the switch current i_d decays to zero.

$$\left(\frac{di_d}{dt}\right)_{t_6} = \frac{g_m(v_{g-} - V_{th} - i_{\rm load}/g_m)}{R_g C_{ies} + g_m L_s} \tag{3.32}$$

The duration of t_6 is calculated by,

$$t_6 = i_{\rm load} / \left(\frac{di_d}{dt}\right)_{t_6} \tag{3.33}$$

The ‘‘tailing” of the drain current of IGBT is ignored here due to its low transient slope.

3.5.3 The impact of a noise source

Here a square wave with rise- and falltimes is used to show how the transient level affects on the spectral content of the noise source. The ringing phenomenon is also included to make the noise signal more general. This is illustrated in Figure 3.15(a).

The original signal can be expressed in this equation,

$$f(t) = \begin{cases} 0 & t < 0 \\ \frac{V_0}{\tau} t & 0 \le t < \tau \\ V_0 + K_1 e^{-\alpha_1 t} \sin(\omega_{r1}(t-\tau)) & \tau \le t < T/2 \\ V_0(1 - \frac{t - T/2}{\tau}) & T/2 \le t < T/2 + \tau \\ K_1 e^{-\alpha_1 t} \sin(\omega_{r1}(t - T/2 - \tau)) & T/2 + \tau \le t < T \end{cases} \tag{3.34}$$

Here, τ is the rise- and falltimes. The α_1 is the damping coefficient and $f_{r1} = \omega_{r1}/2\pi$ is the ringing frequency. K_1 describes the amplitude of the ringing

signals. The behavior around the transient is similar to the real behavior after the convolution of two signals in the time domain, shown in Figure 3.15(b) and Figure 3.15(c). The former is the piecewise linear waveform obtained on the functional level, expressed by this equation.

$$f_1(t) = \begin{cases} 0 & t < 0 \\ V_0 & 0 \le t < T/2 \\ 0 & T/2 \le t < T \end{cases} \tag{3.35}$$

The latter is the normalized derivative of the transient.

$$f_2(t) = \begin{cases} 0 & t < 0 \\ 1/\tau & 0 \le t < \tau \\ \frac{K_1}{V_0} e^{-\alpha_1 t}(\omega_{r1}\cos(\omega_{r1}(t-\tau)) - \alpha_1 \sin(\omega_{r1}(t-\tau))) & \tau \le t < T/2 \end{cases} \tag{3.36}$$

The Laplace transform of $f_2(t)$ is the correcting factor,

$$\begin{aligned} CF(s) &= \tfrac{1-e^{-\tau s}}{\tau s} + \tfrac{K_1}{V_0}\left(\tfrac{\omega_{r1}(s+\alpha_1)}{(s+\alpha_1)^2+\omega_{r1}^2} - \tfrac{\alpha_1\omega_{r1}}{(s+\alpha_1)^2+\omega_{r1}^2}\right)e^{-\tau s} \\ &= \tfrac{1-e^{-\tau s}}{\tau s} + \tfrac{K_1}{V_0}\left(\tfrac{\omega_{r1} s}{(s+\alpha_1)^2+\omega_{r1}^2}\right)e^{-\tau s} \end{aligned} \tag{3.37}$$

Here, s represents Laplacian operator. In Figure 3.15, T =2 ms, τ=100 μs, K_1 =0.1, V_0 =1, f_{r1} =30 kHz, α =1000.

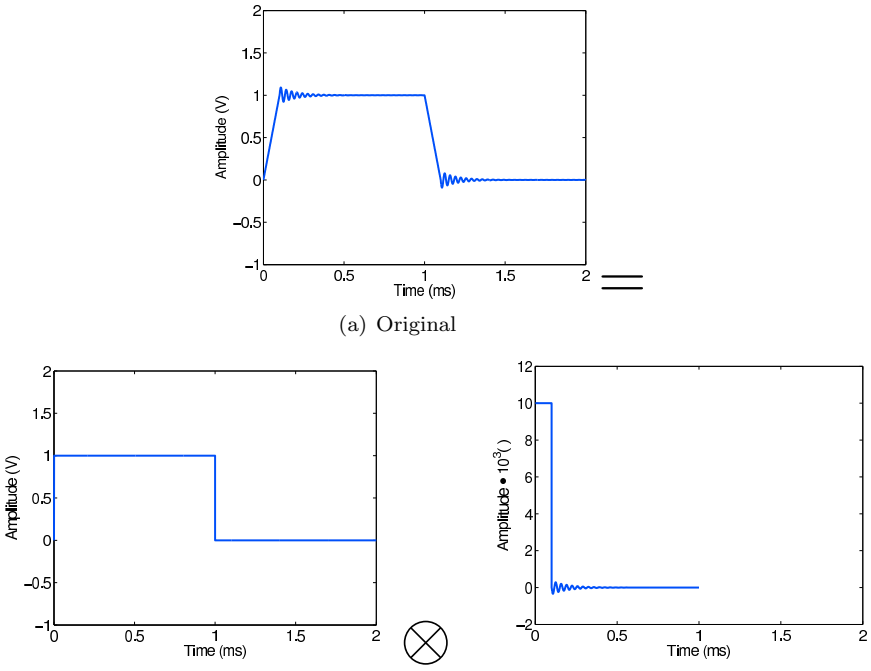
Three simulations are run to compare the correcting factors of the edges on the transient level. The first one is an ideal rectangular signal with $\tau = 0$ and $K_1 = 0$; the second signal is a signal with finite rise- and falltimes τ but without ringing; last of all, the third signal includes a ringing signal in the ege. The result is shown in Figure 3.16. With the ideal edge, i.e., $\tau = 0$, the spectral content in the high frequency part is overestimated. Without the ringing signal, the increased level in the ringing frequency is missed. The correcting factors can thus reflect the impact of the transient clearly.

To calculate the influences of the transient edges in Figure 3.14, the derivatives of the edges are first transformed to s domain. The results are the correcting factors to correct the overestimated or underestimated high frequency spectrum of the noise source. The type of transient edges needs to be identified first, then the correcting factors are then calculated by Equation (3.38) - (3.41).

$$CF_{\text{ion}}(s) = \frac{(1 + I_{rr}/i_{\text{load}})(1 - e^{-(t_1+t_2)s})}{(t_1+t_2)s} - \frac{(I_{rr}/i_{\text{load}})(1 - e^{-t_3 s})}{t_3 s} e^{-(t_1+t_2)s} \tag{3.38}$$

$$CF_{\text{von}}(s) = -\frac{1 - e^{-t_4 s}}{t_4 s} e^{-t_1 s} \tag{3.39}$$

$$CF_{\text{ioff}}(s) = -\frac{1 - e^{-t_6 s}}{t_6 s} e^{-t_5 s} \tag{3.40}$$



(a) Original

(b) Functional level

(c) Transient Level

Figure 3.15: The transient can be described by convolution of two signals

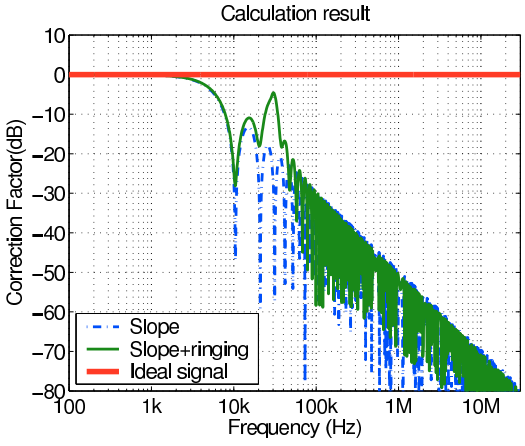
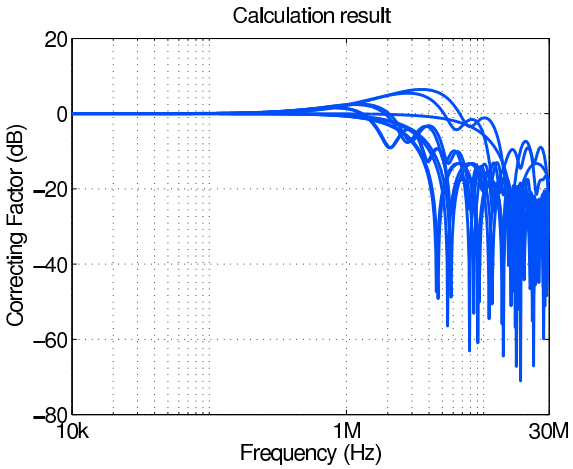


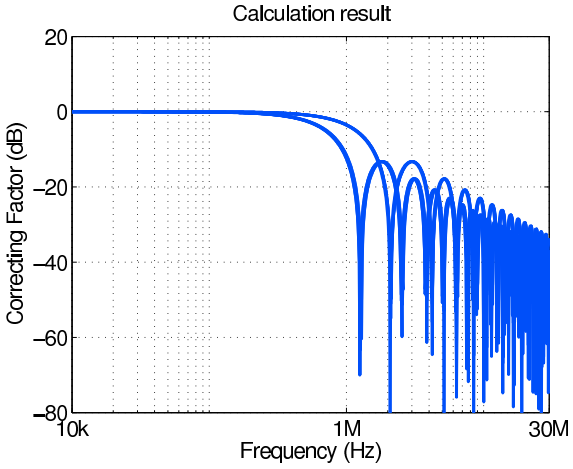
Figure 3.16: Illustration of the effect of the transient on the spectral content of noise source

$$CF_{\text{voff}}(s) = \frac{1 - e^{-t_5 s}}{t_5 s} \tag{3.41}$$

In Figure 3.17, the correcting factors in many switching events are calculated and plotted. We do find the influence in different switching events.



(a) current source



(b) voltage source

Figure 3.17: Correcting factors of switching events considering the variation of edges

3.6 Propagation level

In [He04], it is shown that the equivalent capacitances of rectifier diodes have significant influence to the characteristics of EMI coupling paths in the conducted EMC frequency range. Also, all the switching devices and loads have internal passive parasitic components that are included as a part of the propagation path. The transfer ratio is defined as the ratio between the voltage drop over the LISN 50 Ω resistor and the amplitude of the noise source.

In Figure 3.18, the main parasitic components are included in a schematic diagram of a voltage source inverter. It has been proved that the switching behavior of the power device depends strongly on the operating points and gate drive circuit. The transient characteristics of turn-on and turn-off are represented by equations in the previous section, and the parasitic elements of the switches are determined by the operating points.

In the high frequency range, the IGBTs, which are widely used as switches in AC-AC converters, must take into account input, output and reverse transfer capacitors. These parasitic capacitances have large influence on the propagation path. The body diode model can be used to calculate these nonlinear variable capacitances based on the reverse voltage.

In [Bus05], the IGBT output capacitance C_{oss} is considered as a parallel drain-gate capacitance C_{dg} and internal diode depletion capacitance C_{ds}. When the IGBT is turned on, C_{oss} is not important because a path with much smaller impedance exists. On the other hand, the junction capacitance is important when the IGBT is turned off. C_{oss} is expressed by Equation (3.42),

$$C_{oss} = \frac{C_{jds0}}{(1 + \frac{v_{ds}}{V_{jds}})^{M_{ds}}} + \frac{C_{jdg0}}{(1 + \frac{v_{ds} - V_{th}}{V_{jdg}})^{M_{dg}}} \tag{3.42}$$

here,

C_{jds0}	is the zero-bias drain-source capacitance,
C_{jdg0}	is the zero-bias drain-gate capacitance,
M_{ds}	is the drain-source grading coefficient,
M_{dg}	is the drain-gate grading coefficient,
V_{jds}	is the built-in potential of the drain-source (diode) junction,
V_{jdg}	is the built-in potential of the drain-gate junction,
v_{ds}	is the voltage across the drain-source junction,
V_{th}	is the drain-source threshold voltage.

The nonlinear regression method can be used to solve for the coefficient using the C_{oss} from the datasheet. This step is necessary, because the measurement is always done below 20 V, and we need to know the capacitance of this variable capacitor when the IGBT is reversed biased by DC-bus voltage.

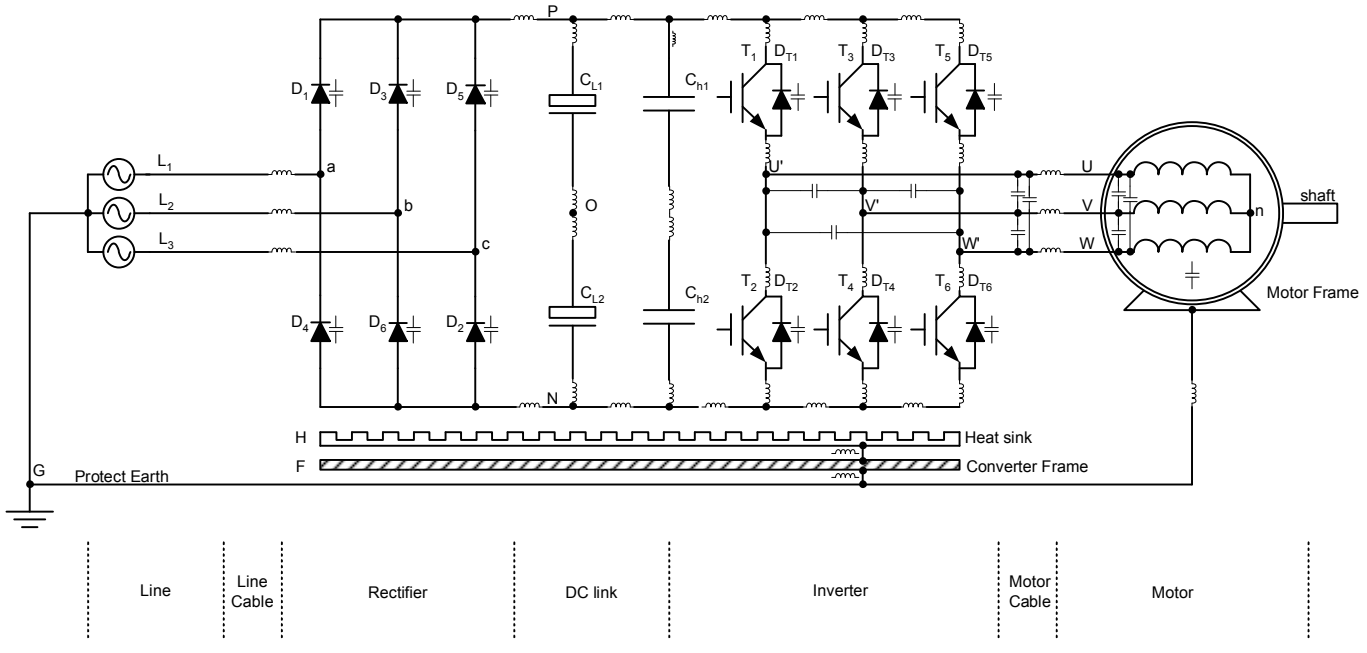


Figure 3.18: Block diagram of DC-bus voltage source inverter including parasitic components

In Figure 3.19, the curve fitting result of C_{oss} is compared to the data from the datasheet. Using the derived coefficient, the C_{oss} is known as 419pF when $v_{ds} = V_{\rm dc}$.

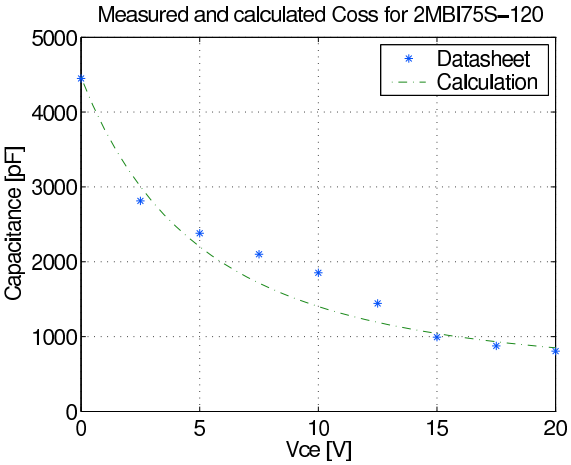


Figure 3.19: Output capacitance curves of 2MBI75S-120 IGBT

The diodes in the rectifier have a large influence on EMI. During the period when the diodes are reverse biased, the diodes can be modeled as a variable capacitor. The capacitance value changes with the reverse voltage.

Equation (3.43) represents junction capacitance. C_j dominates in the reverse bias and is small in the forward bias.

$$C_j = \frac{C_{j0}}{(1 + \frac{V}{V_j})^M} \tag{3.43}$$

here,

C_{j0} is the zero-bias diode junction capacitance,
V_j is the built-in potential of the diode juction,
M is the diode junction grading coefficient.

In Figure 3.20, the transfer ratio is calculated for different conducting patterns of the rectifier diodes.

Based on the circuit above, the transfer ratio is calculated for current noise source and voltage noise source when the active switch is the upper switch.

In each transfer ratio plot, the voltage source or current source is set to 1 V or 1 A. The voltage drops in the three 50 Ω resistors in LISN are calculated. It

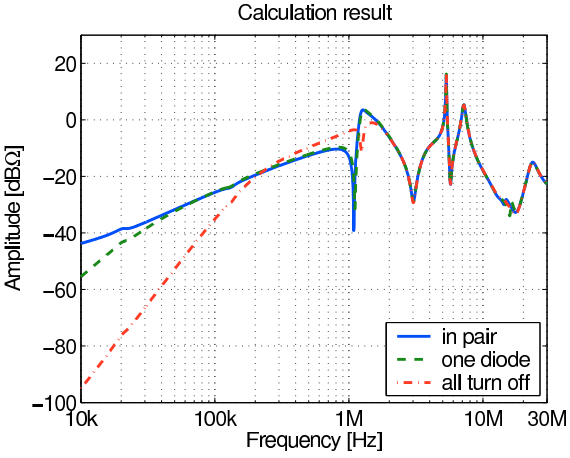
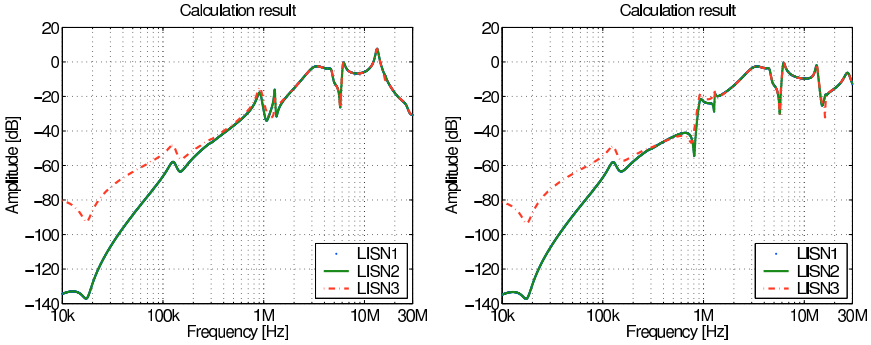
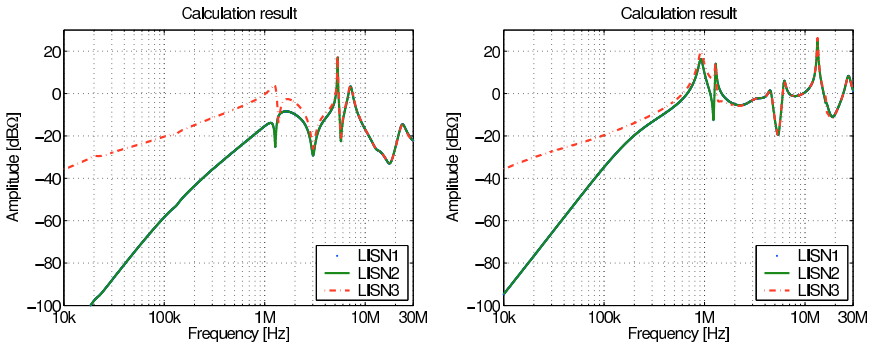


Figure 3.20: The influence of conducting pattern of diodes



(a) when active sw. turns on (b) when active sw. turns off

Figure 3.21: Voltage source transfer ratio



(a) when active sw. turns on (b) when active sw. turns off

Figure 3.22: Current source transfer ratio

is observed that the conduction states of the rectifier diodes do have significant impact on the transfer ratio in the frequency range below 500 kHz.

3.7 Summary

In this chapter, a hierarchical approach for modeling the conducted EMI emission of power electronic applications is presented. In the introduction, the necessity of predicting conducted EMI of power electronic converter and the difficulties associated with this are discussed. An approach is proposed to rapidly predict the EMI level with sufficient accuracy and it is implemented using a hierarchical method. On the functional level, large time constants are used to get the operating points of each switching device. The switching devices are then replaced by a noise cell model including current and voltage noise sources. On the transient level, the transient edges of the noise source are replaced by piecewise linear lines using the nonlinear behavior model. The operating point information achieved during the previous level calculation is used to determine the transient slope. On the propagation level, thanks to the established information of operating points, the accuracy of the propagation path model can be improved.

This approach can be used to predict the EMI level of a voltage source inverter feeding an induction motor. It can also be used for a ZVS inverter.

Chapter 4

Suppression along the propagation path

4.1 Introduction

In Chapter 3, a hierarchical approach for analyzing EMC problem is developed. All parameters or factors relating to the EMC performance can be divided into three levels. On the functional level, realizing the preset function is the main purpose. All parameters on the functional level seldom change for the purpose of getting better EMC performance, but, the parameters on the functional level have a direct and indirect influence on the EMC performance. The direct impact is in the low frequency range. For indirect impact, the parameters on the functional level determine the operating point first. Then, on the transient level, these transient slopes are influenced by the operating points of the switches determined on the functional level. Suppression in the noise source is related to the design on the transient level. Correspondingly, suppression along the propagation path is done by changing the parameters on the propagation level. All the components positioned between the LISN receiver and noise source form part of the propagation path. In this chapter, how noise propagates is investigated. Possible design parameters and their influence to the noise propagation path are identified.

A motor drive is a typical AC-AC application. It is used as a case study to identify the propagation paths in the frequency domain and the time domain. The switch inside the converter is modeled as the current noise source and voltage noise source when the switch is turned on or turned off. The switching switch is called ‘‘active’’ one. In the same inverter leg, the freewheel diode of another switch providing the current when the switch is turned off is modeled as a ‘‘controlled’’ source. The other switches in other inverter legs are ‘‘inactive’’ ones, because they remain in on or off states during switching transient of ‘‘active’’ switch. The

''inactive'' switches are modeled as passive components.

The ''active'' switch and the freewheel diode operate as a pair of noise sources. The freewheel diode noise source is controlled by the ''active'' switch noise sources. Meanwhile, the ''inactive'' switches, the DC-bus, the rectifier and the rest of the converter system provide the propagation path to spread the noise generated by the ''active'' switch to the LISN receiver. The diagram of the generation and progagation of the EMI noise is shown in Figure 4.1. Along with the operation of the converter, the switches change their states between the ''active'', ''controlled'' and ''inactive''. In other words, they are changing their roles between noise sources and propagation paths.

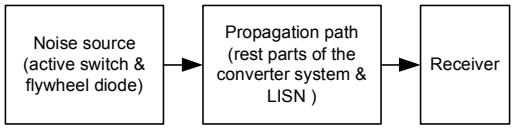


Figure 4.1: EMI noise generation and propagation

Unlike the models of previous work [Liu05], the ''inactive'' switches are also treated as a part of the propagation path in this thesis. This is necessary because the source impedances of these ''inactive'' switches have an influence on the noise propagation in the high frequency range.

The efficiency of the propagation path is defined as the transfer ratio. This conversion efficiency serves as a criterion to evaluate EMC. A high transfer ratio means that more noise goes to the LISN receiver. In practice, the CM current on the line side can be considered as the results which are converted from the CM currents on the motor side. It is a simple measurement to make. Models are built and used to determine the transfer ratio.

When we analyze the models, we see that the transfer ratio is independent of the motor and the cable and is only related to the converter itself if the measurement setup conforms to the standard. It is verified experimentally and it is shown that it is meaningful to compare the EMC performance of different converters by comparing transfer ratios even if they have different loads [Zha06a].

The transfer ratio can be measured by the signal injecting method proposed in [Che00]. Using this approach, the transfer ratio is measured when the converter is powered off. The result is consistent with the measurement result when the converter is powered up [Zha06b]. An evident advantage of this method is preventing system damage or personal injuries.

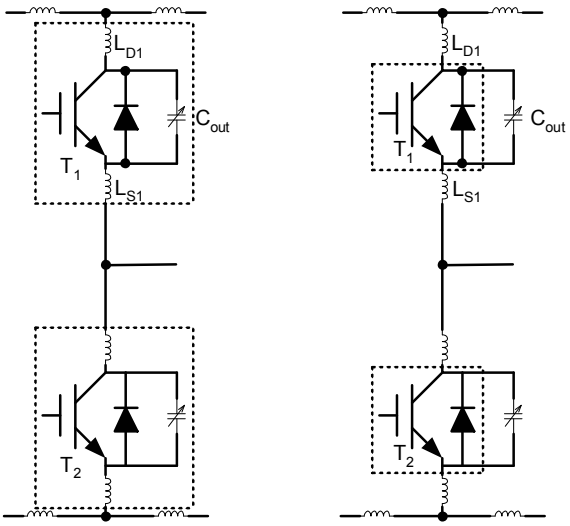
4.2 Decoupling the propagation path and the noise source

In Chapter 3, the hierarchical approach is proposed for EMC analysis. The basis of the approach is that the propagation path and the noise source can be decoupled.

In this section of the chapter, the reason for doing this is discussed. The feasibility is considered, and the steps for analysis are presented.

In [Gra97], the influence of high frequency parasitic components is discussed. To get an accurate EMC analysis result, it is necessary to include all high frequency parasitic components. The parasitic components have a slight influence on the waveforms of the noise sources on the transient levels. However they strongly affect the efficiency of noise propagation and the final EMI spectrum received by LISN. The main reason for this is that these parasitic components modify the propagation path between the noise source and the LISN receiver on the propagation level. By contrast, it is not necessary to consider the influence of parasitic components on the functional level. A few parasitic components around the switches need to be included in the analysis to get the accurate transient waveform on the transient level.

There is some freedom in the way to divide the whole converter into two parts, the noise source part and the propagation path part. In Figure 4.2, two different boundaries to distinguish the noise source from the propagation path are illustrated by dotted line boxes.



(a) on the DC-bus

(b) on the die pads of switches

Figure 4.2: Division boundary between the noise source and the propagation path

In Figure 4.2(a), the boundary is placed at the DC-bus interconnects. Therefore, the noise sources need to include the output capacitances C_{out} and the stray inductances of the interconnect wires and the transistors leads, denoted as L_{d1} and L_{s1}. According to the Thévenin theorem, the noise source including parasitic

components is equal to an ideal noise source v_{eq} with a Thévenin resistance Z_{TH}. v_{eq} and Z_{TH} can be derived from the equations below by using the impedance of parasitic capacitances and inductances.

$$Z_{TH} = \frac{1}{sC_{\text{out}}} + s(L_{d1} + L_{s1}) \tag{4.1}$$

$$v_{eq} = i_d \frac{1}{sC_{\text{out}}} \tag{4.2}$$

Evidently, there is a series resonance due to the capacitance and inductances. This is the reason why the voltages or currents measured at the output terminals of an inverter leg are normally accompanied by parasitic ringing. The waveform of the noise source changes with the values of parasitic components. As known from Equation (3.43), the values of the parasitic components are not fixed. This conflicts with the prerequisite to use a hierarchical approach, namely that the noise source depends very little on the parasitic components.

Another approach is shown in Figure 4.2(b). The parasitic components are excluded from the noise source and considered as part of the propagation path. The noise sources can be treated as ideal voltage sources or current sources without source impedance. Therefore, it is desirable to put the boundary between the noise source and the propagation path as close as possible on the die pads of the transistor. It should be noted that the impact of the diode reverse recovery is considered in the noise source by including the peak of the reverse recovery current in the waveform.

4.3 Analysis of the propagation path

When using the conventional method for EMI analysis, the noise received by LISN can be decomposed into the DM and CM noise components. The DM noise is the noise that occurs between the phase lines. For the CM noise, the ground and phase lines form the path for the noise propagation. The noises in each phase line have the same amplitude and phase.

The noise source can be modeled in the form of voltage and current. Therefore, we have four kinds of transformations:

- voltage source → CM noise,
- current source → DM noise,
- voltage source → DM noise,
- current source → CM noise.

The first two types of noise sources are most commonly known. They are the sources of the CM and DM current on the line side. The DM noise generated by

the voltage source is ignored because $v_1 + v_2 \approx V_{\mathrm{dc}}$ when the parasitic inductances of the DC-bus are negligible. Similarly, no CM noise is generated by the current source in the conventional model since $i_2 - i_1 \approx i_{\mathrm{load}}$. This is true when the parasitic capacitance to ground is neglected.

Aside from these assumptions, the symmetric characteristic of the propagation paths is also taken into account for simplification. Under the assumption that the propagation path between the CM noise voltage source and the phase lines are symmetric to ground, the positive and negative rails of the DC-bus are treated as identical paths, and the three-phase lines as well. The simplified CM circuit is then achieved.

To simplify the DM circuit, we also need the following three assumptions:

- two rails of DC-bus are symmetric to the mid-point of the DC-bus,
- three-phase lines are symmetric to the neutral point of the phase lines,
- the diodes in the bridge rectifier always conduct in pair.

Under these assumptions, the ground is ignored and we get the simplified DM circuit.

In short, the voltage source and the current source generate the CM noise on the DC-bus and the DM noise in the phase lines respectively. No cross conversion exists between CM and DM. This is true only under the above assumptions.

The limitations of the conventional approach are evidently due to the simplifications made for simplification. Firstly, all the parameters in the three inverter legs must be the same. This is generally not true, according to a real measurement [Hua04]. Secondly, the inductive and capacitive coupling between inverter legs cannot be considered in the simplified model, and these parasitic parameters are not negligible [Hua04; Ker03]. Thirdly, the simplification is only applicable in an inverter with a diode rectifier. For a complex converter with active rectifier, the simplified model is not available. A quantitive analysis of EMC performance for such power electronics application is still desirable.

Simulations are run to find the inaccuracies due to these simplifications:

- the components in the different inverter legs are identical,
- there are no inductive couplings between inverter legs,
- there are no capacitive couplings between inverter legs.

Four simulations are run to observe how the transfer ratio calculated by simplified models compares to the detailed models. The first simulation is of the most simplified circuit that meets all these three assumptions. The assumptions are then removed one by one in this sequence:

- adding the deviation of the component values in inverter legs,
- adding the inductive coupling between inverter legs,

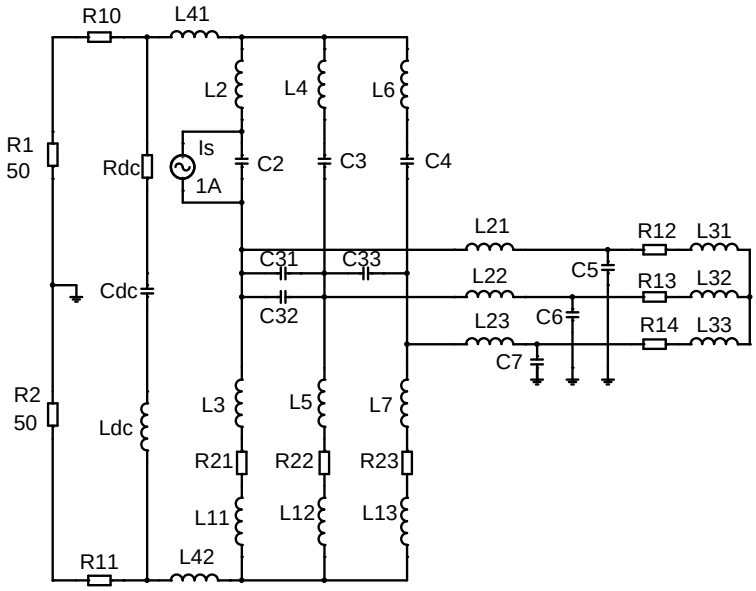


Figure 4.3: Circuit used to calculate transfer ratio of current source during switching transient in one inverter leg

- adding the capacitive coupling between inverter legs.

The parameters in the most simplified circuit are $L_{11} = L_{12} = L_{13}$=18 nH, $L_{41} = L_{42}$ =20 nH. The motor high frequency parameters are derived from a measurement of an experimental motor. To evaluate the deviations of the component values in inverter legs, L_{11} is set to 10 nH, and L_{13} is set to 33 nH, and the bus rail inductances L_{41}, L_{42} are set to 15 nH and 25 nH respectively. Inductive coupling is included by setting the coupling coefficient between L_{11}, L_{12}, L_{13} as 0.3. Capacitive coupling is included by putting capacitors $C_{31} = C_{32} = C_{33}$ =0.1 nF between phases.

The rest parameters in the circuit are constant. They are listed in Table 4.1.

The transfer ratio is defined as the ratio of the voltage drop over the LISN resistors to the current provided by the current noise source. It can be obtained by solving the equivalent circuit shown in Figure 4.3. We observe the transfer ratio in two parts,

$$T_{\text{iCM}} = \frac{v_{R1} + v_{R2}}{i_s} \tag{4.3}$$

$$T_{\text{iDM}} = \frac{v_{R1} - v_{R2}}{i_s} \tag{4.4}$$

Table 4.1: Parameters in the model

C_{dc}	620 μF
R_{dc}	15 mΩ
L_{dc}	45 nH
C_2, C_3, C_4	0.9 nF
R_{10}, R_{11}	1 Ω
$L_2, L_3, L_4, L_5, L_6, L_7$	20 nH
L_{21}, L_{22}, L_{23}	3 μH
C_5, C_6, C_7	0.4 nF
R_{12}, R_{13}, R_{14}	900 Ω
L_{31}, L_{32}, L_{33}	1.9 mH

The CM transfer ratio and DM transfer ratio of the current source are drawn in Figure 4.4.

The CM transfer ratio and the DM transfer ratio of voltage source are also defined as the ratio of the voltage drop over the LISN resistors to the voltage provided by the voltage noise source. We observe the transfer ratio in two parts,

$$T_{\mathrm{vCM}} = \frac{v_{R1} + v_{R2}}{v_s} \tag{4.5}$$

$$T_{\mathrm{vDM}} = \frac{v_{R1} - v_{R2}}{v_s} \tag{4.6}$$

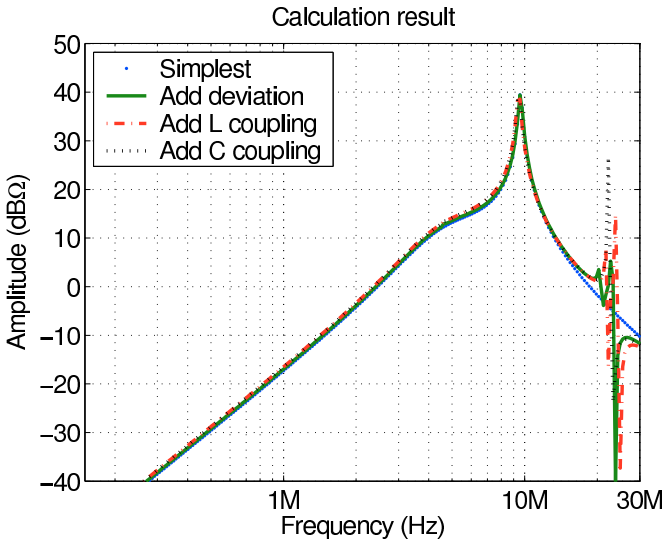
The CM transfer ratio and DM transfer ratio of the voltage source are drawn in Figure 4.5.

It can be observed from the figures that the inductive coupling and capacitive coupling have an impact on the noise received by LISN. There are deviations of the transfer ratio for different levels of simplifications. The influence is significant above 10 MHz, which is still within the band of conducted emission. We can say that the simplification is a good approximation only below 10 MHz.

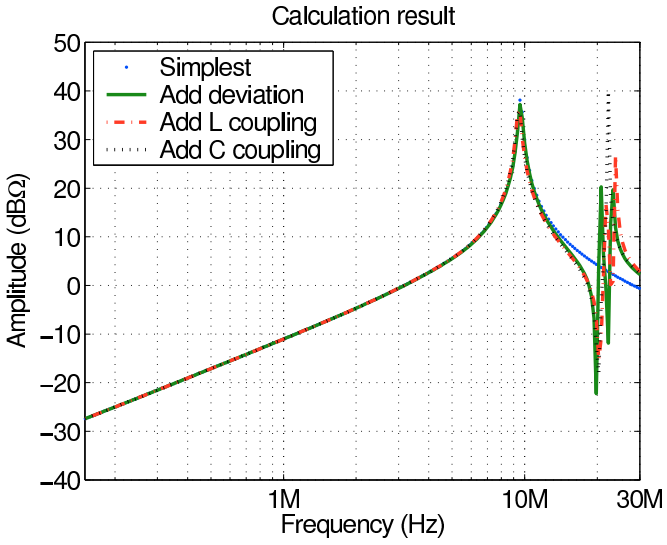
Also observing from the figures, it is confirmed that the CM transfer ratio is lower than the DM transfer ratio for the current noise source up to 2 MHz. This means that the current noise source mainly transfers to the DM noise until 2 MHz. Beyond that, the CM transfer ratio has the same order of magnitude as the DM transfer ratio. The cross conversion takes place above 2 MHz.

Another conclusion can be obtained for the voltage noise source. The voltage noise sources convert mainly to the CM noise in the whole frequency range.

Although the conventional approach has limitations, it is still a powerful tool for the design of an EMI filter for a simple converter [Shi96]. A new approach is needed when the conventional approach encounters its limits.

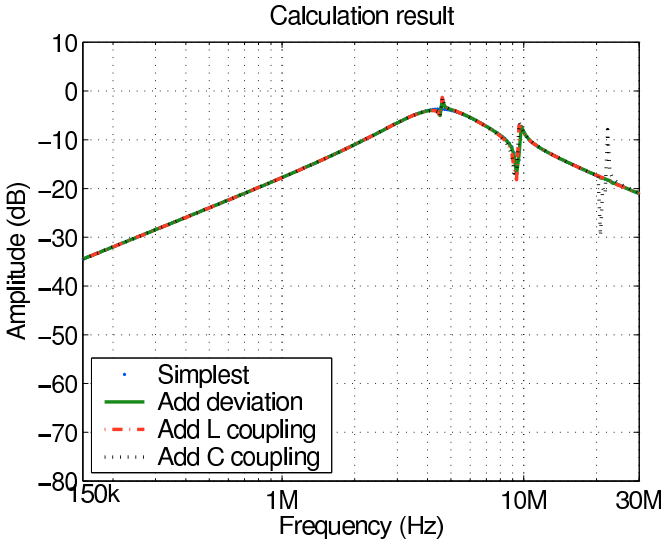


(a) CM transfer ratio

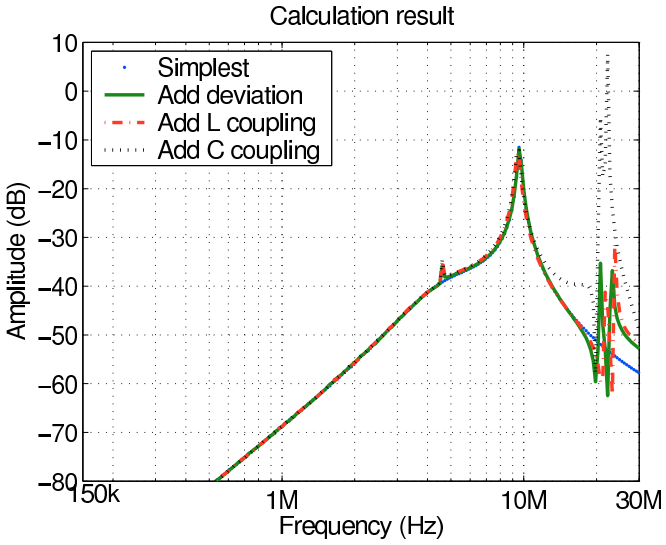


(b) DM transfer ratio

Figure 4.4: CM and DM transfer ratio of current source with different details included



(a) CM transfer ratio



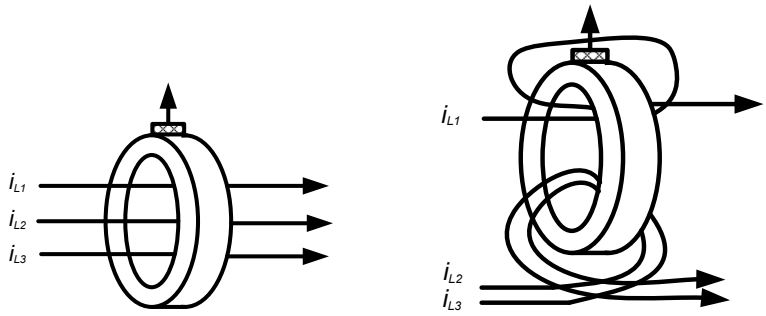
(b) DM transfer ratio

Figure 4.5: CM and DM transfer ratio of voltage source with different details included

4.4 The observation in the time domain

In the frequency domain, the observation is limited to time-invariant systems. Therefore, we have several assumptions and simplifications. Through the observations in the time domain, how the propagation path varies is understood.

The noise current is generated and propagates to the line side. We use two current probes to measure the current on the line side of the converter. Using the different wiring configurations depicted in Figure 4.6, we can get two measurement results. i_{CM1} is the CM current on the line side of the inverter. i_{DM1} is the DM current on the line side of the inverter.



(a) $i_{\mathrm{L1}} + i_{\mathrm{L2}} + i_{\mathrm{L3}} = 3i_{\mathrm{CM1}}$ (b) $2i_{\mathrm{L1}} - i_{\mathrm{L2}} - i_{\mathrm{L3}} = 3i_{\mathrm{DM1}}$

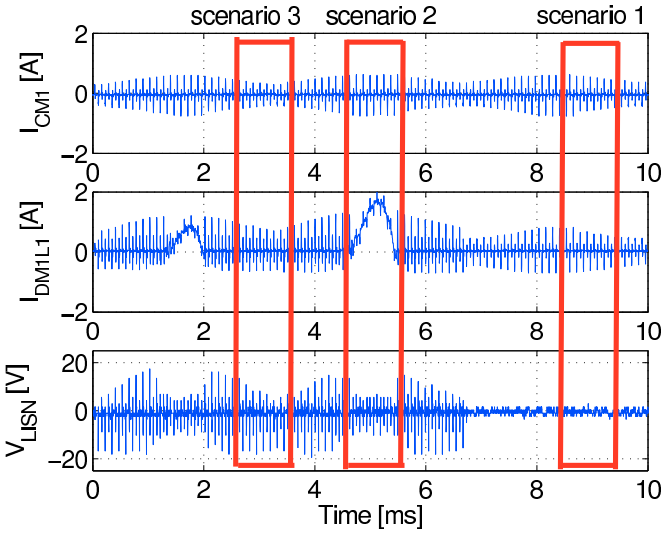
Figure 4.6: Using current probe to separate CM and DM

The measurement is recorded during half of the AC power period. It is presented in Figure 4.7(a). To get more details, we zoom in for the different scenarios, as shown in Figure 4.7(b)-4.7(d). By observing these figures, the features of these figures are summarized below for different scenarios.

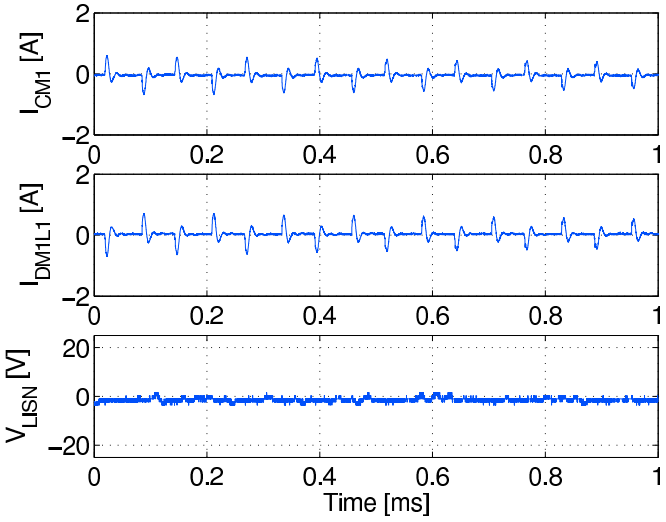
By observing the relationships between these waveforms, as tabulated in Table 4.2 and Table 4.3, we know directly how the diode conduction patterns correspond to the scenarios we measured.

Table 4.2: The relationship between i_{CM1} and i_{DM1} in different scenarios

Scenario	Relationship between i_{CM1} and i_{DM1}
1	i_{DM1} = - i_{CM1}
2	$i_{\mathrm{DM1}} = 0.5\ i_{\mathrm{CM1}}$
3	$i_{\mathrm{DM1}} = 2\ i_{\mathrm{CM1}}$ and i_{DM1} = - i_{CM1} by turns
4	$i_{\mathrm{DM1}} = 0.8\ i_{\mathrm{CM1}}$

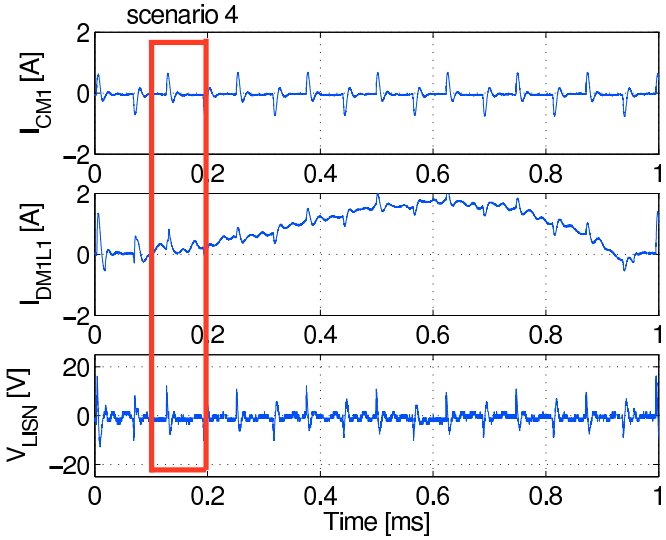


(a) measured waveform and scenarios

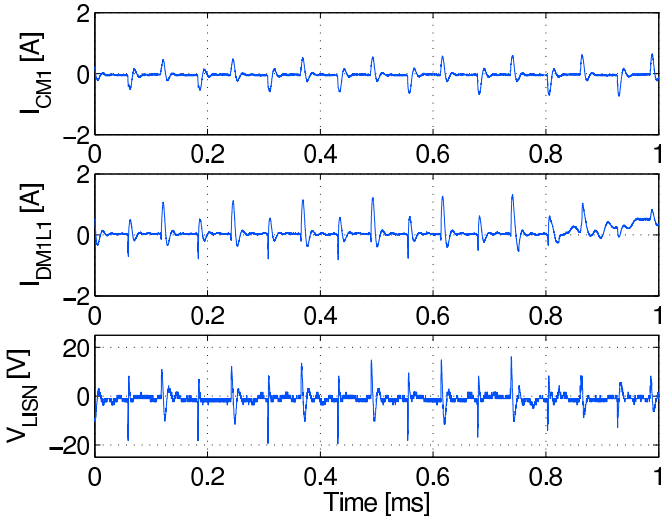


(b) zoom in of scenario 1

Figure 4.7: Time domain waveforms measured on the line side of converter (to be continue)



(c) zoom in of scenario 2



(d) zoom in of scenario 3

Figure 4.7: (cont.)Time domain waveforms measured on the line side of converter

Table 4.3: The relationship between i_{CM1} and v_{LISN} in different scenarios

Scenario	Relationship between i_{CM1} and v_{LISN}
1	$v_{LISN} = 0$
2	$v_{LISN} = 25\ i_{CM1}$
3	$v_{LISN} = 50\ i_{CM1}$ and $v_{LISN} = 0$ by turns
4	$v_{LISN} = 30\ i_{CM1}$

Scenario 1 occurs when diode pair D2/D3 or diode pair D5/D6 pair are conducting. No current flows through D1 or D4, therefore, no noise voltage drop is present on the LISN in phase L1.

Scenario 2 is also a very familiar situation. When the diode pair D1/D2, or D3/D4, or D4/D5, or D6/D1 are being turned on, the CM current flows through the diode pair as Figure 4.8 shows. The CM current ripple is superimposed on the rectifier input DM current.

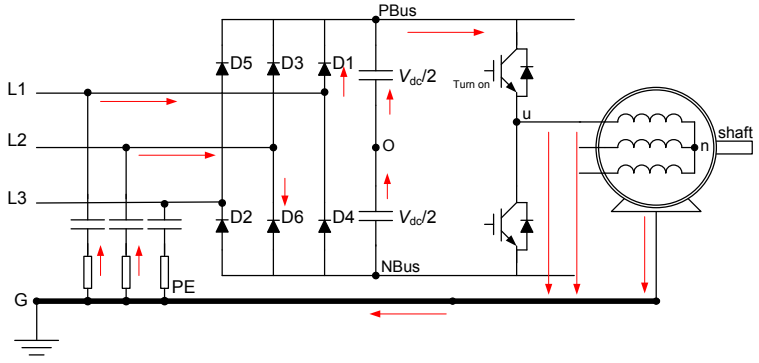


Figure 4.8: The loop of CM current of scenario 2

Scenario 3 is introduced by [Men04b; She04; Qu02]. At the instant when the gate signal turns on the upper switch or turns off the lower switch, the potential of the inverter terminal u is still low because of the parasitic capacitance. The D1 goes in conduction to this positive bias voltage while D2 or D6 are reverse biased because the voltage of the DC-bus capacitor clamps their anodes at a voltage value lower than the voltage at their cathodes. As a result, the current flows only through L1. The loop of the CM current is illustrated in Figure 4.9. A similar situation occurs when the gate signal turns off the upper switch or turns on the lower switch, and then the potential of the inverter terminal u is equal to the positive DC-bus. This causes all the current to flow through L2 or L3, keeping the D1 reverse biased. One observes that the mixed mode current will disappear when X capacitors are installed. This causes the current to be distributed evenly

between the phase lines. Because the values of the X capacitors are limited, there is always some unbalance. Therefore, mixed mode current needs to be considered especially at low frequencies.

Scenario 4 is observed during the transit time between scenario 2 and scenario 3. It is illustrated in Figure 4.7(c). This scenario happens when the only conducting diode is handing over part of the CM current to another diode which then starts conducting.

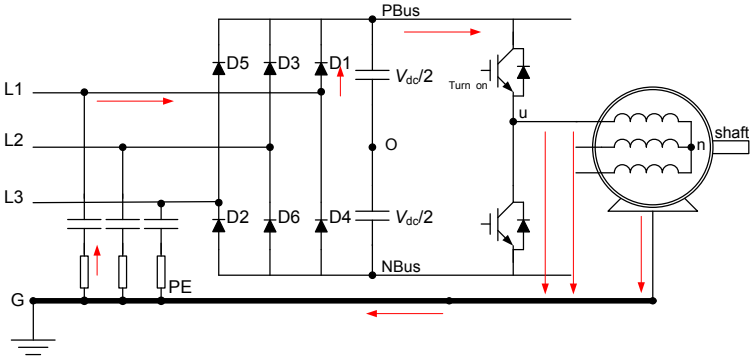


Figure 4.9: The loop of CM current of scenario 3

In the measured waveforms shown in Figure 4.7(a), it is easily seen that the envelope of the CM noise presents a periodic ripple. The ripple period is exactly 1/6 times the mains voltage period. This confirms that the CM current is generated by voltage transient and is proportional to this transient voltage change ratio.

From the above observation, it is clear that the noise propagation path is not fixed but it changes with the conducting pattern of the diodes. Therefore, over a very short time interval we can calculate the transfer ratio for a propagation path in the frequency domain. This helps to prevent convergence problems and the result can be achieved faster and reliably. This calculation of the transfer ratio needs to be updated at each new switching event to reflect the influence of the variation of the propagation path.

4.5 Passive filter for noise suppression and the influence of installation

Using filters is a well-known solution to suppress the EMI of drive systems [Shi96; Han04; Aka08]. The filters should work efficiently according to the datasheets provided by filter manufacturers. However, the effect of filters may change significantly depending on how they are installed. Grounding methods or interconnect methods have a large impact on the real attenuation provided by the filter. A

node in a schematic diagram may be a wire or a mounting screw in the real application. For example, in one converter provided by industry, the heat sink and the Y capacitors on the PCB board are connected to the converter frame by 20 cm long wires (see Figure 4.10). Although in some well designed products the long wires are replaced by shorter interconnects or mounting screws, the parasitic elements still play a role in the interconnects. These parasitic parameters affect the EMC performance of the drive system [Gra97; Wan02].

In [Zha06b], the transfer ratio is defined as the ratio of the CM current i_{CM1} on the line side to the CM current i_{CM2} on the motor side. It is used to indicate how efficiently the filter blocks the noise propagation. There are three reasons why the transfer ratio is defined in this way,

1. The CM current can be easily measured with a current probe because the electrical contact is not necessary. The transfer ratio can possibly be measured with low-cost current probes [Rid99], even when the conversion factors of these low-cost current probes are unknown, or the probes are not calibrated.

2. The installation methods, including the grounding configuration and interconnect methods, have little effect on the DM noise conversion. The DM noise is dominant in the low frequency range, where the values of the discrete components are significant compared to that of the parasitic components. By contrast, the main part being influenced is CM noise.

3. CM currents may flow in any of the phases in the three-phase lines [She04; Men04b]. There are DM components produced by CM currents when the CM currents are not evenly distributed in the three phases. For the same CM currents with different distributions in the three phase lines, LISN measurement in one particular phase gives an uncertainty up to 9.5 dB ($20\log_{10}3$), because the LISN cannot distinguish the CM components from the DM components. Using current measuring to measure the CM current can avoid the DM components by adding the currents in the three phase lines together.

In the next section, the relationship between transfer ratio and parasitic parameters is derived by using a model. The parameters can then be extracted from significant points on the curve of the transfer ratio measurement result. The suppression efficiencies when placing the Y capacitors on different places are also compared using the model. The transfer ratio is used to evaluate the suppression efficiency.

During the study, a commercial PWM VSI with diode rectifiers is selected for the case study. Its power rating is 12 kW. An induction machine is fed with this converter. The measurements are made in unloaded condition. It is believed that the transfer ratio is determined mainly by the passive components and not affected by the load condition.

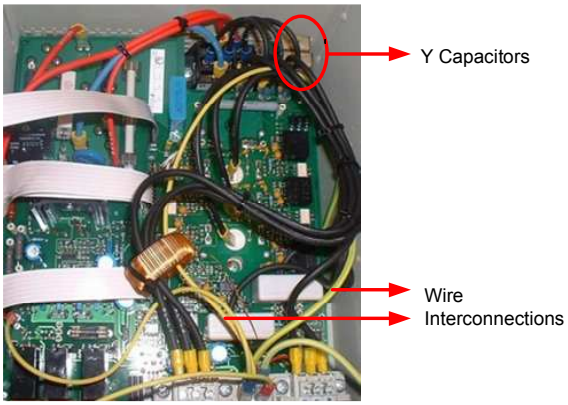


Figure 4.10: Photo shows the real installation inside a converter

Figure 4.11 illustrates the whole experimental setup. In the original design, the AC-Y capacitors are placed between the AC line and the converter frame. The dashed lines represent the real installation wires which cannot be idealized in the model for EMC analysis. Also in Figure 4.11, it is proposed to place the DC-Y capacitors between the DC-bus and the converter frame or the heat sink. Two circles indicate the positions where the CM currents are measured to derive the transfer ratio.

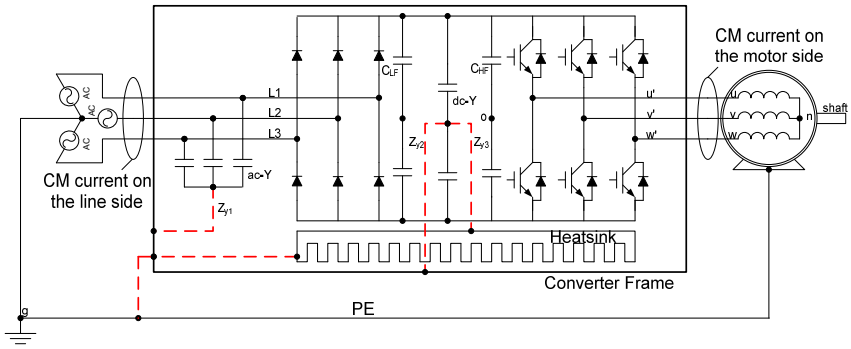


Figure 4.11: Circuit diagram of the converter under test

4.5.1 CM equivalent model

In [Gon03], a frequency domain model is proposed to calculate the CM noise generated by the switched power converter. Based on the CM equivalent circuit, the model is expanded by including the parasitic parameters introduced by in-

stallation. It is then further simplified by applying reasonable assumptions. We assume that the parameters of the three inverter legs are the same. The arbitrary voltage noise sources can be treated as three superimposed identical CM voltage sources and three DM voltage sources. The DM voltage sources will not produce a current flowing through ground. Therefore, they can be removed if we want to calculate the CM current. The three identical CM voltage sources can be further reduced to one CM voltage source after changing the CM impedance of the load and the stray impedance between the output terminal and the heat sink to 1/3 of their original value. The equivalent circuit used to calculate the transfer ratio is shown in Figure 4.12.

The generated CM currents flow through the DC-bus to the line side. The CM current will be evenly distributed in positive and negative DC-bus bars by the high frequency DC-bus capacitors C_{HF}. Therefore, two DC-bus bars are considered as one node in the model. Z_{y1}, Z_{y2} and Z_{y3} represent the three possible places for placing the Y capacitors. They are identified by dashed lines in Figure 4.11 and 4.12. Z_{y1} represents the AC-Y capacitors connected between the AC line input and the converter frame. Z_{y2} represents the DC-Y capacitors added between the DC-bus and the converter frame. Z_{y3} represents the DC-Y capacitors whose one terminal is connected to the heat sink instead of the converter frame. The impedance of the AC line, the rectifier and the DC-bus are indicated as Z_{line}, $Z_{\mathrm{rectifier}}$ and Z_{dc}. In addition, the following notations have been adopted:

- Z_{p1}: the impedance of the interconnect between the converter frame and the heat sink,
- Z_{p2}: the impedance of the interconnect between the motor frame and ground,
- Z_{p3}: the impedance of the interconnect between the converter frame and ground,
- $Z_{o(1,2,3)}$: the CM impedance of the load, including the cable and the motor in the present example,
- $Z_{p(A,B,C)}$: the impedance between output terminals of the converter legs and the heat sink,
- Z_L: the impedance of the LISN.

4.5.2 Extraction of parasitic parameters

The transfer ratio T is defined as the ratio of the CM current i_{CM1} on the line side to the CM current i_{CM2} on the motor side. In the conventional way, AC-Y capacitors are placed between the AC line input and converter frame as indicated

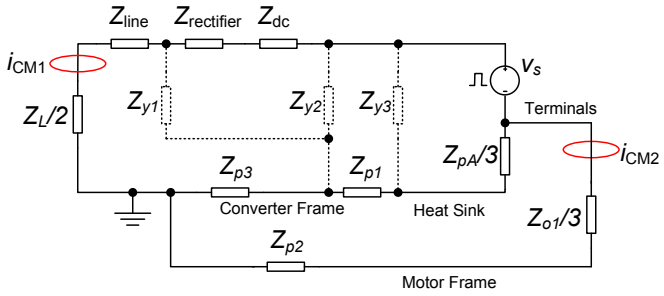


Figure 4.12: CM equivalent circuit

by Z_{y1} in Figure 4.12. This model can further be simplified by Y-Δ conversion because it is easy to apply the current divider rule. The simplified model is shown in Figure 4.13, and the transfer ratio can be expressed in a concise form,

$$T = \left|\frac{i_{\mathrm{CM1}}}{i_{\mathrm{CM2}}}\right| = \left|\left(\frac{Z_A}{Z_5 + Z_A}\right)\left(\frac{Z_C + Z_4}{Z_C}\right)\right| \tag{4.7}$$

here,

$$Z_4 = (Z_{o1}/3 + Z_{p2}) \tag{4.8}$$

$$Z_5 = (Z_L/2 + Z_{\mathrm{line}}) \tag{4.9}$$

$$Z_A = (Z_{y1} + Z_{p3}) + \frac{Z_{y1}Z_{p3}}{Z_{pA}/3 + Z_{p1}} \tag{4.10}$$

$$Z_C = (Z_{pA}/3 + Z_{p1} + Z_{p3}) + \frac{(Z_{pA}/3 + Z_{p1})Z_{p3}}{Z_{y1}} \tag{4.11}$$

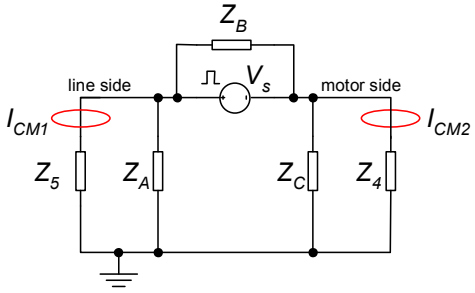


Figure 4.13: CM equivalent circuit after Y-Δ conversion

It is not easy to obtain the values of the parasitic parameters. In most cases, it is done by a direct measurement [Che98] or time domain reflectometry (TDR) method [Zhu99]. Here, a method to derive the parasitic parameters from the transfer ratio measurement results in particular situations is introduced.

First, the high frequency CM behavior of the motor and the cable is modeled using the method introduced in [Sch06; Bog07]. The model is illustrated in Figure 4.14. The values of these components are found using the curve fitting method. The impedances of the motor and the cable correspond to the impedance of $Z_{o1}/3$ and Z_{p2} in Figure 4.12. Figure 4.15 compares the final curve fitting result and the CM impedance amplitude measurement.

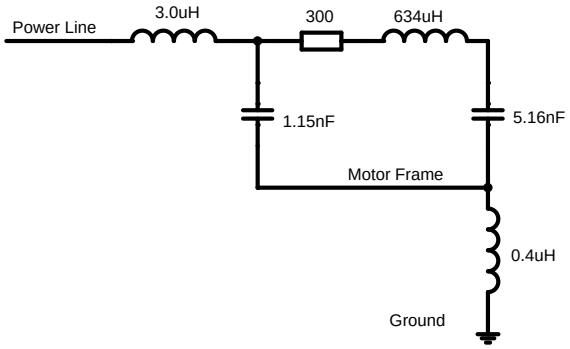


Figure 4.14: High frequency CM model of the motor and the cable

After this, the transfer ratio of the test setup is measured in three situations,

1. the AC-Y capacitors are installed at AC line input (AC-Y);
2. the AC-Y capacitors are not installed (W/O AC-Y);
3. the AC-Y capacitors are installed at the AC line input and the motor is ungrounded (AC-Y, motor floating).

The results are shown in Figure 4.16. The next step involves deriving the parameters of the model from the measurement data. From Equation (4.7), the transfer ratio apparently reaches its minimum value when Z_A reaches a minimum or $Z_C + Z_4$ reaches a minimum. In the first situation, a minimum is found around 370 kHz (see Figure 4.16 point A). This is because Z_A approaches a minimum as mentioned before. It can be approximated by the series resonance of $Z_{y1} + Z_{p3}$. The values of the AC-Y capacitors are already known to be 100 nF. Therefore, the stray inductance to produce the Z_{p3} is calculated by $1/(4\pi^2 f^2 3C_Y)$, i.e., 0.7 μH. Although the impedances Z_4 and Z_5 may shift the resonance frequency slightly, it provides a method to determine a first guess at the parasitic parameters of the model.

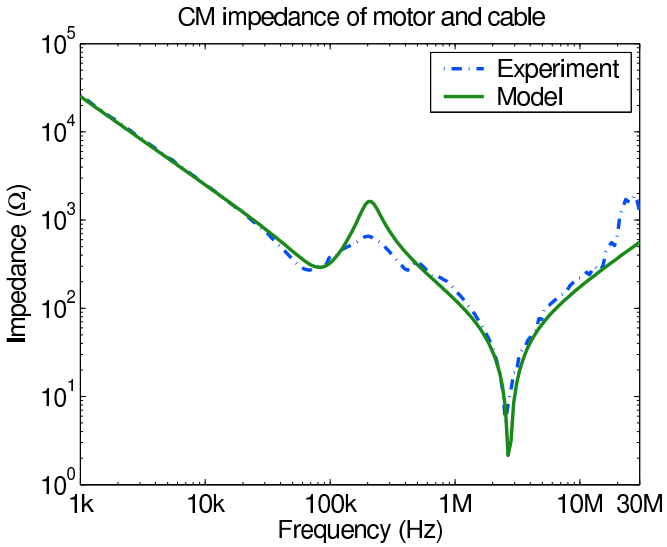


Figure 4.15: Calculated impedance of the model vs. measured CM impedance of the motor and the cable

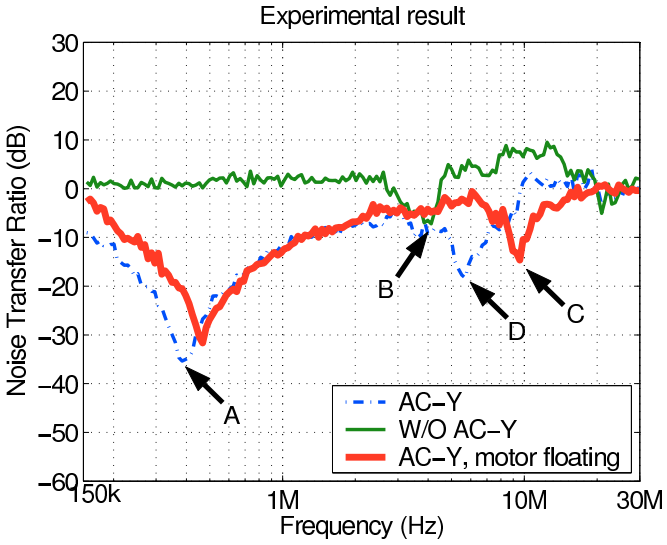


Figure 4.16: Experimental results of the transfer ratio

In the second situation, the Y capacitors are disconnected, which makes Z_{y1} quite large and $Z_C + Z_4$ can be approximated as $Z_{pA}/3 + Z_{p1} + Z_{p3} + Z_{o1}/3 + Z_{p2}$. This determines the second minimum observed at around 3.6 MHz (see Figure 4.16 point B). The inductive part of impedance in this loop is 3.4 μH+0.7 μH=4.1 μH, while the capacitive part should be around 470pF. In this frequency range, only C_{g1} (1.15 nF) dominates $Z_{o1}/3$. The $Z_{pA}/3$ is calculated from the capacitive impedance produced by the 800 pF capacitor to get this resonance frequency.

During the measurement done in the third situation, the motor is ungrounded, and the resonance moves to 10 MHz (see Figure 4.16 point C). The reason for this is that the capacitive part in the loop is dominated by the parasitic capacitance between the motor frame and ground. Z_{p2} is replaced by a 100pF capacitor to create the resonance.

Comparing the first and the third situation, the point D and the point C in Figure 4.16 are caused by the same resonance. The minimum point shifts slightly due to the variation of Z_{p2}. By fine adjustment of Z_{p1} and Z_{p3}, the resonance frequency can be matched to the measurement result. In the last step, some damping resistances are added to adjust the quality factor of the resonance. The ratio curves by calculation comes even closer to the measurement results.

By now, the parameters for the proposed CM model are extracted by the transfer ratio measurement. They are listed in Table 4.4. With the model, the transfer ratio calculated by the model shown in Figure 4.17 shows a good agreement with the measurement result in Figure 4.16. Because the calculation is done in the frequency domain, it is an efficient way to calculate the transfer ratio even for a complex model [Ran98].

Table 4.4: Parameters in the model

Z_L	50 Ω
Z_{y1}	300 nF+0.2 μH
Z_{p1}	0.2 μH+6 Ω
Z_{p2}	0.4 μH+5 Ω
Z_{p3}	0.5 μH+0.8 Ω
$Z_{o1}/3$	3.0 μH+1.15 nF$\|$(300 Ω+634 μH+5.16 nF)
$Z_{pA}/3$	800 pF
$Z_{\text{rectifier}}$	ignored
Z_{line}	ignored
Z_{dc}	0.5 μH+8 Ω

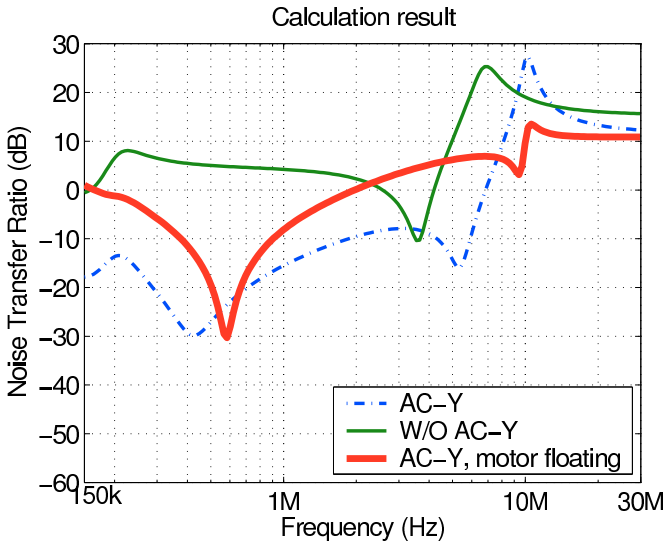


Figure 4.17: Transfer ratio as calculated with the model

4.6 DC-bus filter

The suppression on the propagation path is actually the suppression of the transfer ratio. EMI mitigation method which is widely adopted in industry is passive filtering as yet. Discrete elements are used to increase the impedance of the noise current loop or to constrain the noise current in a local area. The filters are installed on the AC line side or the output side.

Various topologies include these basic elements:

- CM capacitor,
- CM inductor,
- DM capacitor, star or delta interconnect,
- DM inductor.

By combining these basic elements, many variations are possible. The L type filter is frequently used. Looking at commercial products, most of them consist of one stage or multi-stage L type filters. To obtain a combined DM and CM filtering effect, the common capacitor star point can be grounded [Jue07], while the value of the capacitor is limited by the leakage current value. The alternative is to connect to the DC-bus mid-point [Ren98] as a virtual "ground". The main disadvantage is that the DC-bus mid-point is not always available. In [Pal02; Aka04b], the DC-bus rails are used as virtual ground. It is proven in [Aka04a] that the extra

interconnect between the motor neutral point and the DC-bus mid-point makes the CM inductor works more efficiently. A main concern of passive filter design is avoiding the saturation of the filter core. By adding an extra winding with a resistor, this arrangement reduces both the peak value and duration of unwanted oscillations [Oga96] with a smaller core.

In Figure 4.11, three possible positions to place Y capacitors are shown in dashed line. They are represented by three dashed symbols in the equivalent circuit in Figure 4.12. The approach proposed by this thesis is for the Y capacitors to be connected to the DC-bus, as indicated by Z_{y2} or Z_{y3} in the figure. The method of calculating the transfer ratio then requires modification.

When the Y capacitors are placed at the position of Z_{y2} or Z_{y3}, Equation (4.9) need to be changed to

$$Z_5 = (Z_L/2 + Z_{\text{line}} + Z_{\text{rectifier}} + Z_{\text{dc}}). \tag{4.12}$$

When the Y capacitors are placed at the position of Z_{y3}, the (4.10) and (4.11) need to be changed to (4.13) and (4.14).

$$Z_A = (Z_{y1} + Z_{p1} + Z_{p3}) + \frac{Z_{y1}(Z_{p1} + Z_{p3})}{Z_{pA}/3} \tag{4.13}$$

$$Z_C = (\frac{Z_{pA}}{3} + Z_{p1} + Z_{p3}) + \frac{(Z_{pA}/3)(Z_{p1} + Z_{p3})}{Z_{y1}} \tag{4.14}$$

These closed-form equations can be used to calculate the transfer ratio in the frequency domain directly. Based on the established model, the noise suppression efficiency of three possible methods can be compared. Some conclusions are drawn below:

1. In Figure 4.18, the transfer ratio is calculated using the built model. When the Y capacitors are placed at position Z_{y1} or Z_{y2}, the two interconnect methods cause a slight difference in the transfer ratio because the DC-bus impedance is small. For the third interconnect method, the DC-Y capacitors are connected to a heat sink. Z_A and Z_C are calculated using (4.13) and (4.14) instead of (4.10) and (4.11). It can be seen that the EMC performance becomes slightly worse in the low-frequency range and improves in the high-frequency range. For all these positionings of the Y capacitors, the suppression effects are almost the same.

2. As opposed to the AC-Y capacitors, the DC-Y capacitors are placed at positions Z_{y2} or Z_{y3}. Z_5 is calculated by (4.12) instead of (4.9). The increasing value of Z_5 can decrease the transfer ratio, which means that by inserting a CM choke between the rectifier and DC-Y capacitors, the noise will be better suppressed. On the other hand, inserting the CM choke into the DC-bus has no effect on the transfer ratio when AC-Y capacitors are connected to the AC line input. In Figure 4.19, this is shown by the transfer ratio calculated using the built model.

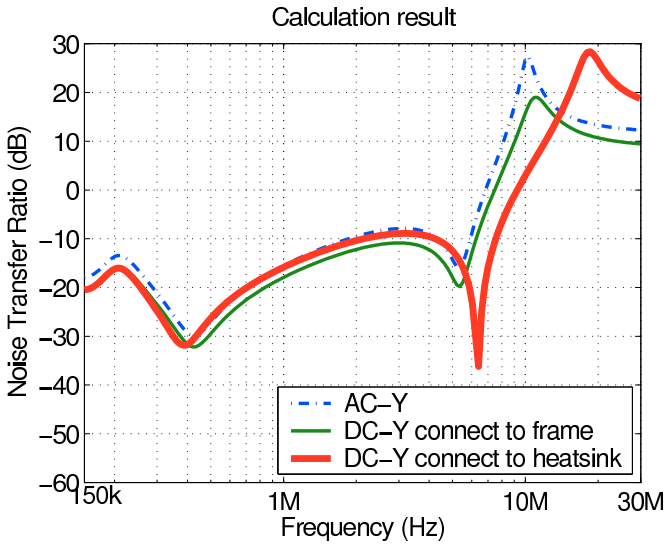


Figure 4.18: Transfer ratio comparison by inserting Y capacitors in different positions (calculated result)

3. The interconnect between the heat sink and ground and the interconnect between the Y capacitors and the heat sink are vital to the suppression efficiency. They must *all* be kept as short as possible. By decreasing Z_{p1}, Z_{p3} and the inductive part of Z_{y1}, the suppression effect is significant improved. In Figure 4.20, the transfer ratio is first calculated assuming that the interconnect wires are two times shorter. The result shows that the transfer ratio is improved by 10 dB in the frequency range 1-6 MHz, where some EMC problems often show up. The calculation is also done assuming that the parasitic components of the interconnect wires are reduced to one-tenth of the original values. This is possible when screw mounting is used instead of wire interconnect. Here the Y capacitor is also increased three times although it contributes additional leakage current. By this arrangement, 20 dB improvement is achieved around 1-6 MHz; there is also a 10 dB improvement in the low frequency range.

It is worthwhile mentioning here that the addition of the filter not only changes the transfer ratio, but also changes the level of the noise source. The changes might be for better or for worse, and sometimes take place in opposite directions. These two effects can be considered separately and there is a trade-off between them. The transfer ratio is affected by the passive components only, while the noise source level is determined by both the active and passive components. Here, we study the transfer ratio solely because we consider only the influence of the installation methods.

The experiments are done on the test setup to verify the model further and the conclusions are drawn in the last section. The components employed in the experiments are listed in Table 4.5. The first experiment is done to show the effects of inserting a CM choke into the DC-bus. Compared with the transfer ratio of using AC-Y solely, inserting the CM choke into the DC-bus does not make a big difference, which is consistent with the calculation. However, the combination of DC-Y and DC-CMC improves the suppression effect in 1-4 MHz, as shown in Figure 4.21.

Table 4.5: Components used in experiments

Qty.	Components	Specification
3	AC-Y	100 nF
2	DC-Y	47 nF
1	DC-CMC	Rasmi RS-OC/2, AL=12 μH, 2 turns

The second experiment shows the importance of short interconnects. The transfer ratios are compared between the test setup originally designed (20 cm), half length interconnect (10 cm) and screw mounted filter. The benefit is significant for a well designed installation. Compared to the calculated results from Figure 4.22, the trends are the same, and the minimum point moves towards a higher frequency as predicted, and the transfer ratio is lower after the resonance frequency. The transfer ratio does not improve much beyond 10 MHz and it even becomes a positive value. That means that a new resonance loop occurs, because of the resonance of the DC-Y capacitors and the stray inductance of the DC-bus. Because the noise source level is much lower in this frequency range, it would not be a problem, even though the transfer ratio is increasing.

When we compare the experimental results of Figures 4.21 and 4.22 to the calculated results of Figures 4.19 and 4.20, a deviation exists. The deviation between the experimental results and the calculated results are due to the very simple model. In the experimental results, the transfer ratio approaches 0 dB in the high frequency range. This is because the noise measurements are close to the noise floor in the high frequency range. The application of the transfer ratio method is limited by the measurement in the high frequency range. More accurate measurements of the transfer ratio can be achieved if a preamplifier is available to lower the noise floor.

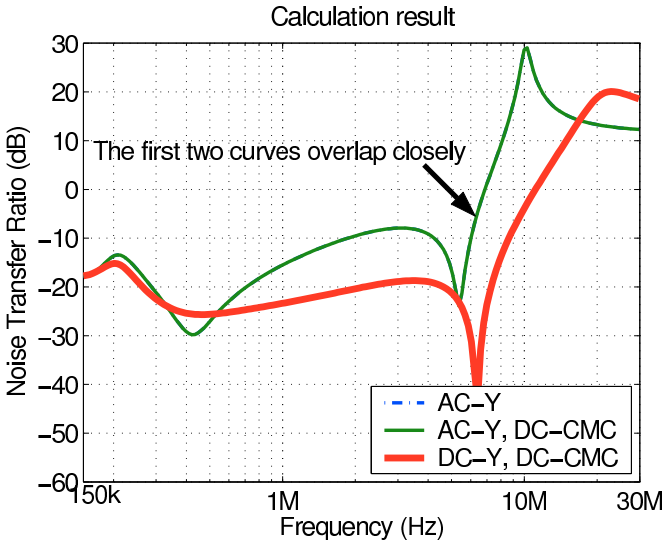


Figure 4.19: Transfer ratio comparison for the effect of DC-bus CM chokes after inserting Y capacitors in different positions (calculated result)

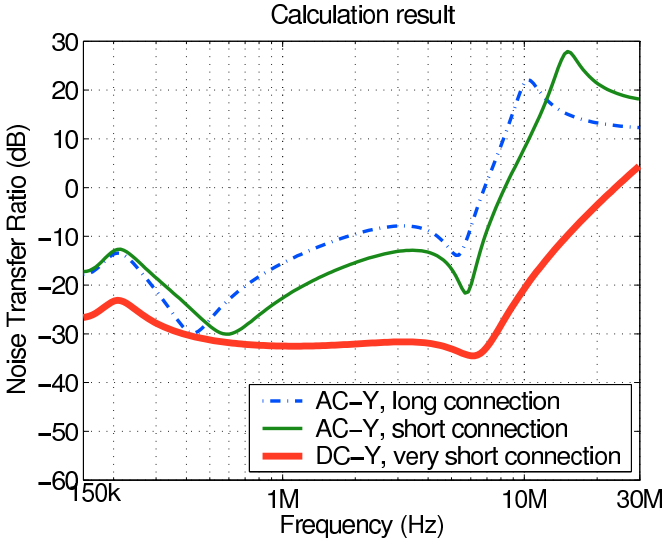


Figure 4.20: Transfer ratio using DC-bus filter with very short interconnect (calculated result)

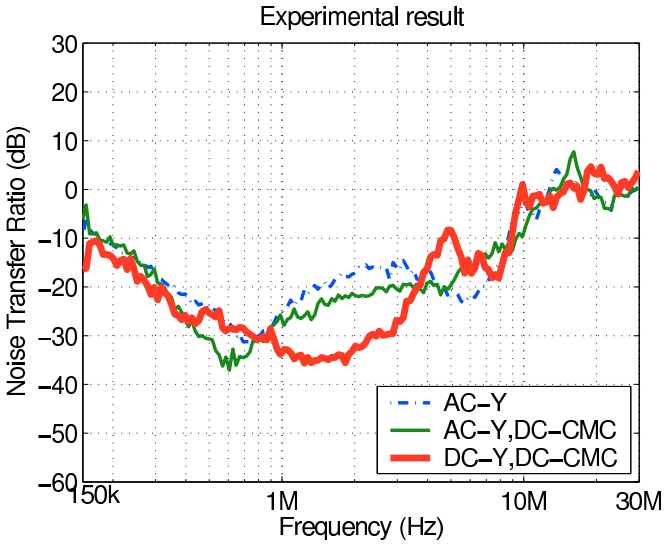


Figure 4.21: Transfer ratio comparison for the effect of DC-bus CM chokes after inserting Y capacitors in different positions (experimental result)

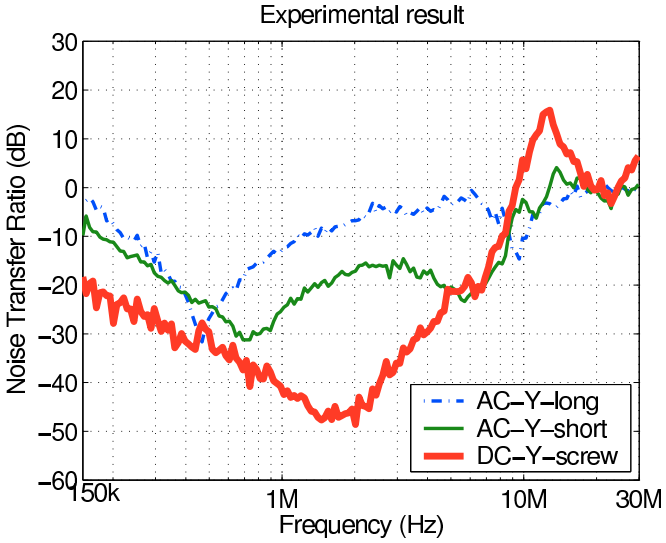


Figure 4.22: Transfer ratio using DC-bus filter with very short interconnect (experimental result)

4.7 Summary

In this chapter, the propagation of noise is investigated. It corresponds to the propagation level of the hierarchical approach. The efficiency of the propagation path is defined as the transfer ratio. This approach also considers the cross conversion between CM and DM. The limitation of the simplified conventional approach is described. Observations in the time domain confirm that the propagation path is not fixed. In practice, the CM on the line side can be regarded as the results which are converted from the CM currents on the motor side. The CM transfer ratio can be measured with a low-cost current probe. The parasitic parameters of the model can be extracted based on the transfer ratio measurement results.

Based on the established model, it is proposed to connect the DC-Y capacitors between the DC-bus and the heat sink and to put the common mode choke (CMC) between the rectifier and the DC-Y capacitors. The improvement due to inserting a DC-bus CM filter can be calculated efficiently in the frequency domain. The filter is installed inside the converter and the interconnects can be made very short. This improves the suppression performance significantly and avoids the tricky task of designing or selecting a filter afterwards. The noise level is suppressed partly inside the converter if the DC-bus filter is included in the design. For some critical EMC requirements, the additional external filter needed would be much smaller.

Chapter 5

Noise source analysis

In this chapter, the characteristics of the noise source are described. The relationship is established between calculated results and compliance measurement results by correcting factors. This approach is used in the analysis of the noise source of a resonant converter where the switching frequencies and transient slopes are not fixed. The prediction of the noise level is compared with experimental results.

5.1 Noise source characteristics

The noise source has two kinds of parameters in the time domain used to evaluate its influence on the victim. The first kind of parameter includes the repetition frequency of the impulses. The frequency shows how often the switching events occur. For aperiodic impulses, the impulse interval time is used instead of the frequency. The second kind of parameter includes the impulse amplitude, width and waveform. These parameters are related to the strength of the impulses.

5.1.1 Periodic noise source

A periodic noise source is a signal that repeats itself every period all the time. The phrase ''all the time'' is theoretically not possible since a signal cannot last forever. Actually, ''all the time'' refers to the time period when the measurement takes place. The measure times are in the order of milliseconds to seconds for different detectors according to the requirements of the CISPR standard [CIS99a]. The condition that the noise source is periodic is much more easily satisfied in a DC converter, since the output voltage and current are relatively constant during the measurement. Therefore, the time intervals between switching events are constant as well, and the transient waveforms are also fixed. In most cases, the noise sources are treated as periodic signals in analysis.

The assumption that the noise sources are periodic rectangular waveforms is very common in EMC analysis, for example, the work done in [Ran98; Che03]. In [Men06], the nonlinear transient waveforms are taken into consideration. This approach is applied to a DC converter. The transient waveforms during turn-on and turn-off of the transistors are calculated based on the operating conditions. Compared to the results obtained by a rectangular waveform model, a more precise result can be achieved by the nonlinear transient waveform model, especially in the high frequency range. Because it is a DC converter, the transient waveform is periodic. This approach is not applicable to an AC-AC converter where the noise is not periodic during measurement since the operating conditions are varying.

5.1.2 Aperiodic noise source

There are several differences between periodic and aperiodic noise sources. The spectrum consists of discrete frequencies for a periodic noise source, while the discrete spectral components are continuously spread for an aperiodic one. During measurement, an aperiodic noise source does not repeat itself or repeats at a low repetition frequency. To achieve the spectra of the compliance measurement of the aperiodic noise, both the characteristics of the noise source and the compliance measurement system must be taken into account.

The compliance measurement setup consists of a band pass filter, a quasi-peak detector and an indicator instrument. The result using the peak and average detector can be calculated from the envelope at the output of the band pass filter [Pet94]. All these components inside the measurement system can be modeled by circuit elements. A general approach is to do the computation in the time domain with very short time steps. Obviously, it requires extensive computation. Another method is deriving the waveform in the time domain by an analytical method [Pet94]. In this thesis, we use the detector pulse response characteristic curve from CISPR standard [CIS99a] to speed up the computation.

5.2 An improved method to analyze noise sources

EMI signals are always considered as a superposition of stationary and transient signals. The stationary signals are normally functional signals. They determine the low frequency part of noise spectra. On the other hand, the transient signals determine the high frequency part of noise spectra.

There are many ways to model noise sources. Four of them are listed below in the order of complexity.

1. Periodic rectangular pulses;
2. Periodic trapezoidal pulses;
3. Periodic pulses with multiple slope approximation;

4. Aperiodic pulses with multiple slope approximation.

The first method can obtain good results in the low frequency range. The second and third methods can achieve improvement in the high frequency range. The first three models can be done in the frequency domain using a fast Fourier transformation (FFT). For an AC-AC converter, the most accurate way to model the noise source is the fourth method.

In [Kru03], a new measurement concept called time-domain EMI measurement (TDEMI) is proposed. It is also called fast emission measurement in the time domain (FEMIT) system in [Kel07]. The intelligent recording part works in a special mode called fast frame mode. It captures the transient part of the noise when the oscilloscope is triggered by pulses. The time intervals between two pulses are also recorded. Short time fast Fourier transformation (STFFT) is used to calculate the spectra. After the measurement, errors are corrected by signal processing, and the values of all kinds of detectors are calculable. The diagram of the TDEMI concept is repeated in Figure 5.1.

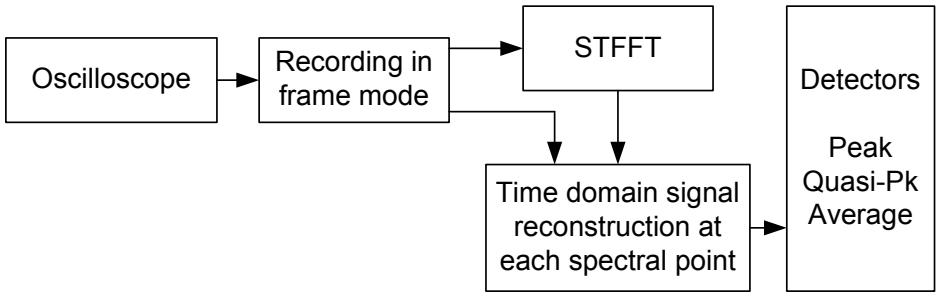


Figure 5.1: TDEMI measurement concept

The purpose of this approach is to reduce the measurement time drastically compared to the traditional sweep frequency measurement receiver, while keeping the maximum deviation acceptable for a compliance measurement result within the range specified by the CISPR standard [CIS99b].

In the TDEMI measurement system, this method is used to speed up measurement. In the hierarchical analysis approach, the same principle is followed. The time intervals between switching events are recorded and then the frequency response correction is considered. With this approach, we can achieve compliance measurement results with the following expected improvements:

1. It achieves accurate results from very low frequency to very high frequency;

2. It is applicable to aperiodic signals;

3. It achieves the result within a short time-frame;

4. It obtains the compliance measurement results not only for peak detectors but also for quasi-peak and average detectors.

5.3 Compliance measurement correction

As emphasized in the previous chapter, the rising and falling edges often show different shapes and slopes. Therefore, the different spectra for each transient are calculated on the functional and transient levels with the hierarchical approach. After that, the spectra must be corrected to get conformity with the compliance measurement receiver.

Undoubtedly, the correction must be carried out according to particular standards, because the measurement parameters have a significant influence on the final measurement result. In this thesis, the calculated result is corrected for full compliance to the international EMC standard CISPR 16-1 [CIS99a].

According to the standard, the basic measurement parameters of the test receiver are defined in Table 5.1.

Table 5.1: The measurement parameters of the test receiver according to CISPR16-1

Band	Frequency	Step	IF bandwidth	M-Time
A	9 kHz - 150 kHz	200 Hz	200 Hz	50 ms
B	150 kHz - 30 MHz	5 kHz	9 kHz	20 ms

The time intervals between them are variable. To superpose several pulses with different repetition frequency, the spectrum is calculated as described below:

Firstly, the operating points are achieved using the functional level analysis. Then, the spectra of the edges are calculated using the Laplace transform. The reason for using the Laplace transform is because the transient waveform is piecewise linear most of the time and is suitable for Laplace transform calculation.

The result in the 's' domain is converted to the frequency domain for narrow band noise. That is when the repetition frequency is higher than IFBW. The conversion follows this equation:

$$U(j\omega) = 2fU(s)|_{s=jn\omega} \tag{5.1}$$

The time interval T_0 between the present transient and the next transient is used to determine the repetition frequency f_0.

In the spectrum calculation, the signal is always truncated for a finite time T. Therefore, no matter how long the time interval T_0 between two pulses is, the calculation is always done as if only one transient is present during T. The pulse response curve for the spectrum calculation is independent on the pulse repetition frequency T_0, but it depends on the finite time T. The correcting factor can be derived as:

$$C_1 = 20\log_{10}(\frac{1}{TB_{6dB}}) \tag{5.2}$$

Therefore, the spectrum calculated from the transient waveform is corrected by taking the repetition frequency and selected detector into account. The finite time T for each transient and the bandwidth of the measurement receiver are both parameters for correction.

The noise in the receiver is calculated based on the spectrum of the noise source and the transfer ratio from source to receiver. The noises in the receiver caused by each transient are combined together to get the final spectrum after the superposition of narrowband and broadband spectra.

In Figure 5.2, the diagram of the algorithm to get the final spectrum is shown.

5.3.1 Detector correction

Based on the calculated results on the functional level, the following characteristics of the transient noise are known:

- the transient waveform,
- the arrival time t_a.
- the interarrival time t_{ia}

The spectrum of each transient waveform can be derived from the transient waveform. This gives the result for a peak (Pk) detector. Many compliance standards require the measurement to be done with a quasi-peak (QP) or an average (Av) detector . The correction curve for using each kind of detector is a function of detector type and repetition frequency.

$$C_2 = f(detector, f_0) \tag{5.3}$$

The theoretical pulse response curves for QP detector receiver and Av detector receiver can be found in the standard [CIS99a].

The pulse response curve in [CIS99a] clearly shows the linear relationship between indicated level of the Av detector receiver and the pulse repetition frequency. The indicated level of the average detector is linear to the pulse repetition frequency with a gradient of 20 dB per decade. The indicated level of the QP detector receiver decreases with the lower repetition frequency nonlinearly. For the peak detector, the level stays constant with the variation of the repetition frequency. When the repetition frequency is higher than the bandwidth of the measurement receiver, the level stays constant with the variation of the repetition frequency for all these three detectors. High repetition frequency in the time domain means larger frequency intervals between narrowband signals in the frequency domain. Because only one narrowband signal falls into the bandwidth of the receiver, the indicated level stays constant.

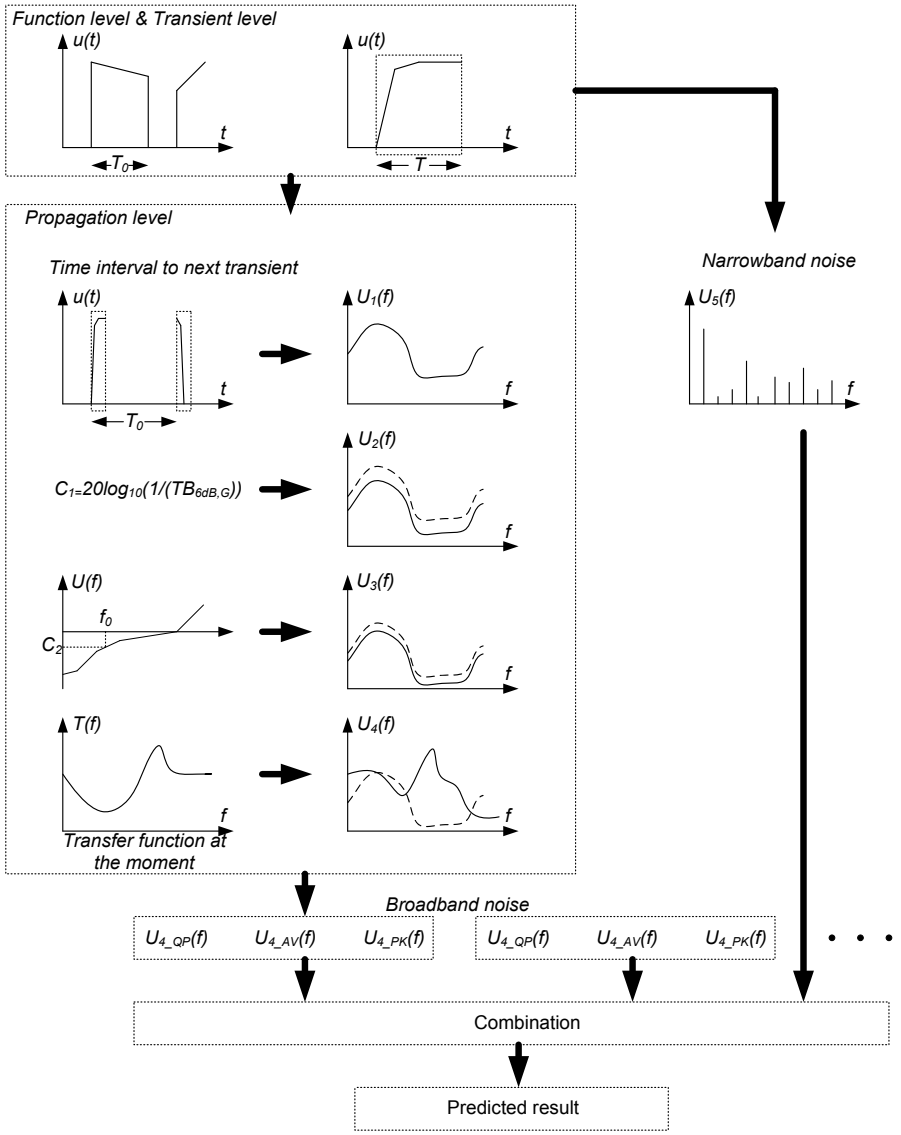


Figure 5.2: The diagram of the algorithm for spectrum calculation

The curves are redrawn in Figure 5.3 and Figure 5.4 for different frequency bands of conducted emission.

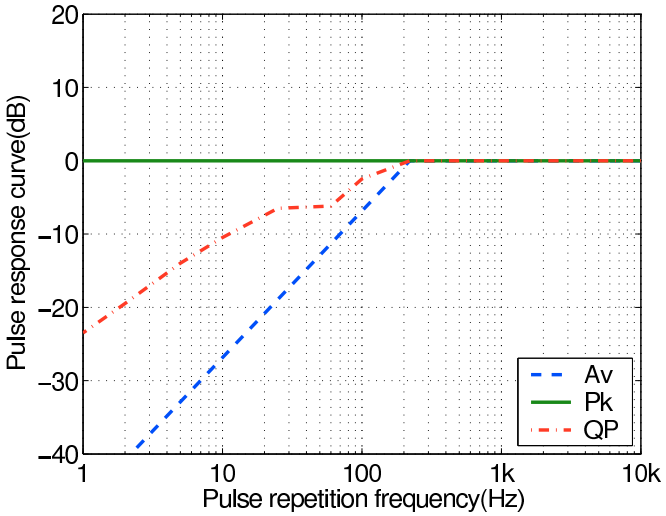


Figure 5.3: Pulse response curves of the measurement receiver for the peak detector, the quasi-peak detector, and the average detector in band A

5.3.2 Signal spectrum reconstruction

The signal spectrum of each transient t_i is already obtained. They include the broadband noise for each transient and narrowband noise for the low frequency part.

The Pk and QP detectors keep the maximum value are each frequency of the signal for a relatively long time when they scan the spectrum. The mathematics can be summarized in Equation (5.4) and (5.5)

$$Pk(f_k) = \max(Pk(f_k, t_i)) \tag{5.4}$$

$$QP(f_k) = \max(QP(f_k, t_i)) \tag{5.5}$$

The result using the average detector is the average result of the spectrum at each transient time. Equation (5.6) shows the result of the Av detector.

$$Av(f_k) = \text{average}(Av(f_k, t_i)) \tag{5.6}$$

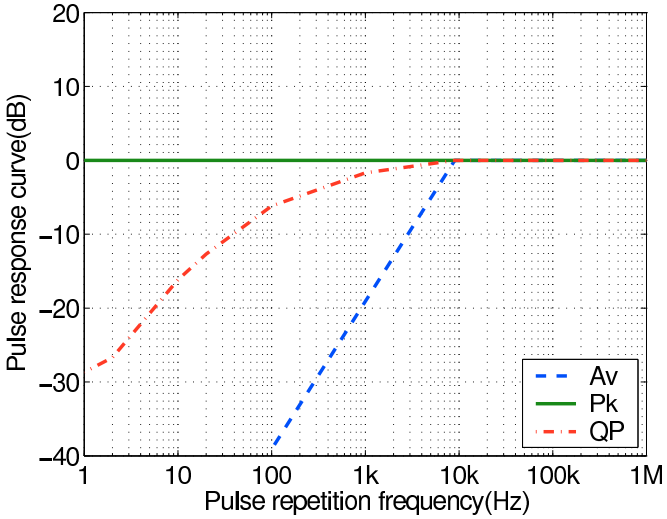


Figure 5.4: Pulse response curves of the measurement receiver for the peak detector, the quasi-peak detector, and the average detector in band B

5.4 Noise source of a resonant converter

The circuit diagram of the resonant pole inverter is shown again in Figure 5.5. This inverter is working under ZVS condition and has a variable switching frequency. It is also used as a case study.

In this new topology, an LC-filter is connected between the bridge and the motor. The motor is the load. A smaller inductor in the LC-filter is connected to the output terminal of the bridge, Therefore the output current of the bridge can change very rapidly. The output current even changes its direction in each switching period. The high frequency current generated by the bridge is smoothed by the filter. Because of the large value of the capacitors in the LC-filter, the filter provides a slow-change output voltage feeding the motor. In summary, the LC-filter is an essential component in the topology that not only provides resonance condition, but also blocks the high frequency noise from reaching the load.

The benefit of this topology is the special mode during commutation. In a conventional hard switching inverter, it is commonly known that when the transistor is turned on, it must provide the opposite diode a reverse recovery current to turn off the diode. The transistors must have a high rating to bear this current. The fast transient of the recovery current is a well-known EMI noise source. In a resonant converter, the current flowing through the diode is not turned off by hard switching. The current always decreases naturally to zero and changes its flowing direction. It is then taken over by the parallel transistor.

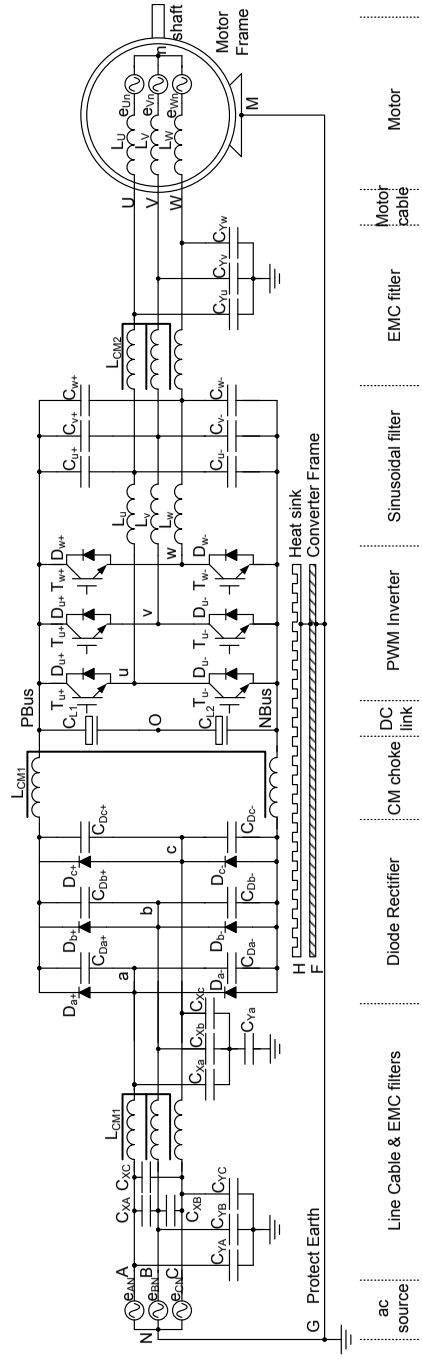


Figure 5.5: Block diagram of resonant pole inverter

Therefore, the diode is turned off at zero current and the transistor is turned on at zero voltage.

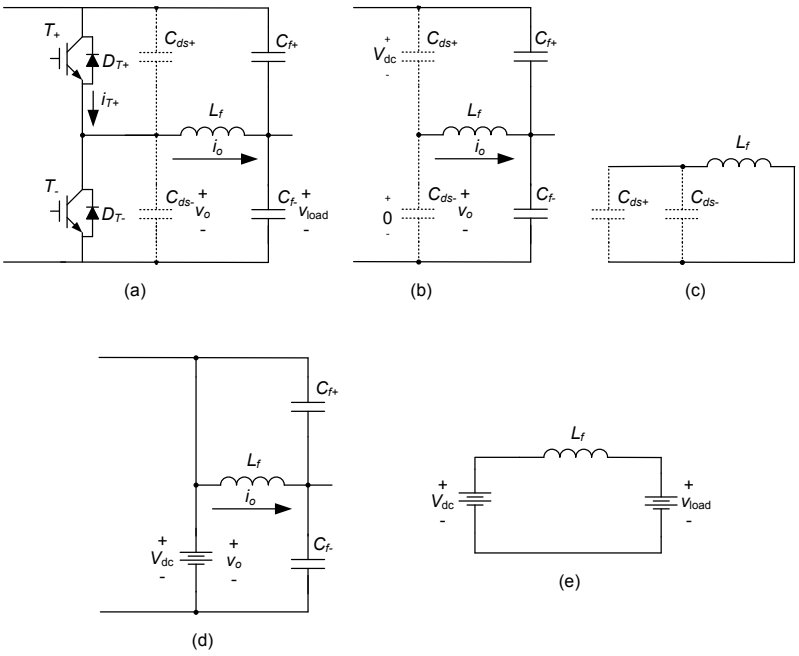


Figure 5.6: An inverter leg of a resonant converter and its equivalent circuit at different moments; (a) circuit diagram, (b) T_- turns off, (c)equivalent circuit when T_- turns off, (d) D_{T+} turns on, (e)equivalent circuit when D_{T+} turns on

For this resonant converter, the current and voltage waveform are analyzed using an equivalent circuit for each mode in the switching cycle. One inverter leg is drawn in Figure 5.6. The drain-source capacitance shown in Figure 5.6(a) affects the switching waveforms. Initially, before t_0, T_- is conducting a negative output current i_0. At time t_0, T_- is turned off. Before T_+ is turned on, the circuit is equivalent to Figure 5.6(b). The initial voltages on the drain-source capacitors of T_+ and T_- are shown in this figure. The voltage across C_{ds+} is $V_{\rm dc}$ and the voltage across C_{ds-} is 0. Since the filter capacitors have much larger capacitances than the drain-source capacitors, the filter capacitors are regarded as short-circuited in the AC equivalent circuit. The simplified circuit is drawn in Figure 5.6(c). The resonant frequency $f_0 = 1/(2\pi\sqrt{L_f(C_{ds+} + C_{ds-})})$. The voltage across C_{ds-} reaches $V_{\rm dc}$ at t_1 and is then clamped to $V_{\rm dc}$ because of the conducting of D_{T+}. The waveforms are shown in Figure 5.7. It should be noted that the time axis is expanded specifically around transients to show the details.

Beyond t_1, this circuit is equivalent to Figure 5.6(d) and is simplified to Fig-

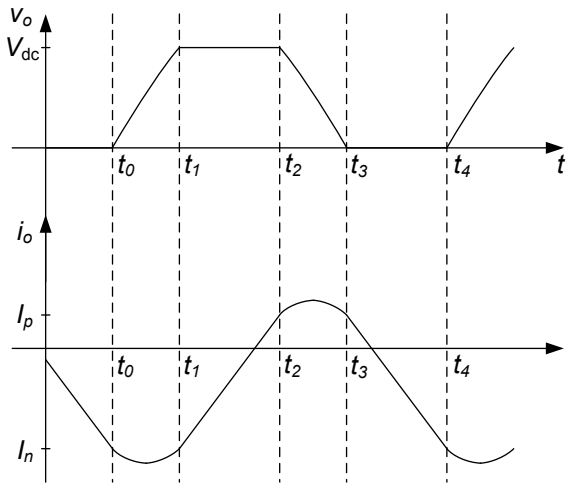


Figure 5.7: Output current and voltage waveform in a resonant converter

ure 5.6(e). The load current increases linearly until it exceeds a preset value I_p at t_2.

As long as D_{T+} begins to conduct, T_+ is gated on. When the load current changes the flowing direction, it flows through T_+ instead of D_{T+}. This arrangement avoids the reverse recovery current of D_{T+} which is a main noise source in a hard switching converter.

At t_2, the T_+ is turned off, which is conducting the positive output current i_o. In the time interval between t_2 and t_3, the voltage across C_{ds-} falls from $V_{\rm dc}$ to 0 by the resonance between the drain-source capacitors and the filter inductors. At t_3, the voltage is clamped at 0 volt since D_{T-} is conducted. Then the load current decreases linearly to a preset value I_n at t_4.

The slopes of the transient at t_0 and t_2 are determined by the amplitude and frequency of the resonances. No matter what the initial voltage values on the capacitor are, the dv/dt of the output voltage can be expressed by:

$$\left(\frac{dv}{dt}\right)_{t_0} = \frac{1}{C_{ds+} + C_{ds-}} I_0 \tag{5.7}$$

Therefore, the dv/dt of the output voltage transient is not constant. It is low at a low output current and increases with a high output current. The value of drain-source capacitances can be derived by the following equation,

$$C_{ds} = C_{oss} - C_{rss} \tag{5.8}$$

here,

C_{oss} is the output capacitance,
C_{rss} is the reverse transfer capacitance.

C_{oss} and C_{rss} can be obtained from the manufacturer's datasheet or experiment-based parameter extraction. Actually, the value of C_{oss} and C_{rss} provided by the datasheet is the measurement in a particular test condition. It varies as a nonlinear function of the drain to source voltage v_{ds}. The effective C_{oss} in [IRF] is defined as a capacitance that would give the same charging time as the output capacitance of a MOSFET while v_{ds} is rising from zero to 80% $V_{\rm dc}$ at $v_{gs} = 0$V.

Next, a validation is done to calculate the dv/dt in transient time. The transistor type is APT8024LF. The measured voltage and current waveforms are shown in Figure 5.8.

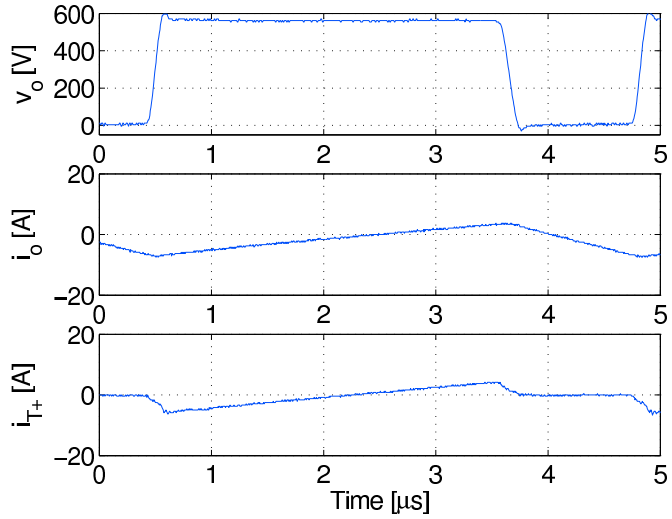


Figure 5.8: Measured output current and voltage waveform in a resonant converter

Measurements are done for different values of the output current v_o. The comparison in Table 5.2 shows a good agreement.

An exception occurs when the output current level is very low. If the condition in Equation (5.9) is satisfied, the peak of the resonance output voltage cannot reach $V_{\rm dc}$ during t_0 and t_1'. At t_1', T_+ is turned on at the end of the deadtime. The output is connected to the bus voltage by T_+, the time diagram is shown in Figure 5.9. This voltage transient is a hard switching with a much higher dv/dt which can be calculated using the approach in the last chapter.

Table 5.2: Comparison of the dv/dt by calculation and measurement

output current(A)	dv/dt by calculation (V/ns)	dv/dt by measurement (V/ns)
18	12.77	11.40
12	8.51	7.60
7	4.96	4.56
4	2.84	2.28

$$I_o < \frac{V_{\rm dc}}{\sqrt{\frac{L_f}{C_{ds+}+C_{ds-}}}} \tag{5.9}$$

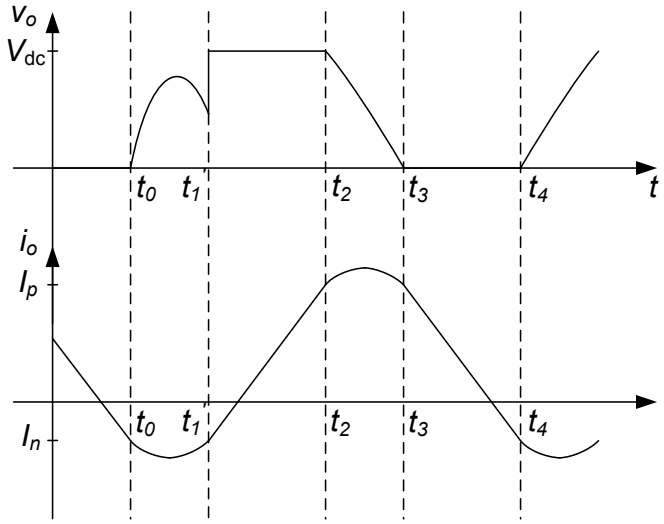


Figure 5.9: Output current and voltage waveform in a resonant converter when output current is very low

The transients are very important for EMI analysis. If the time axis is expanded to a large scale, the output current is a triangle waveform. The fundamental component of the output current i_{o1} is a sinusoidal signal which is required on the functional level. The preset value I_p and I_n to turn on the transistor T_+ and T_- are set according to Figure 5.11. A tolerance band exists for I_p and I_n to let the bridge current reach zero and change direction in each switching cycle. This fulfills the condition for resonant switching. To determine the right moment to

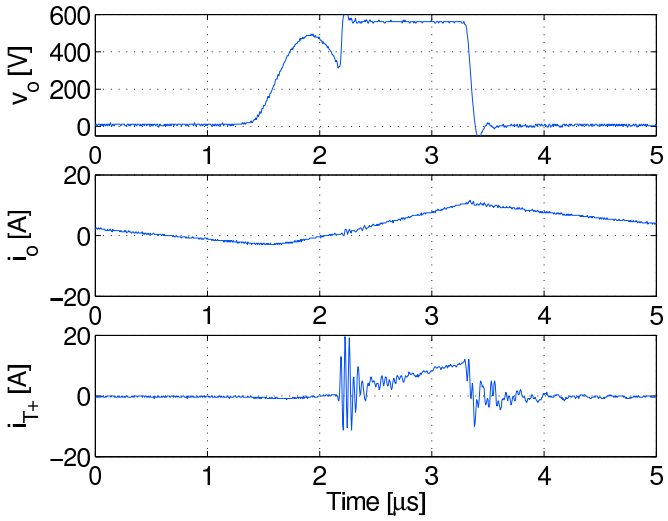


Figure 5.10: Measured output current and voltage waveform in a resonant converter when output current is very low

switch the transistors, the current through the inductance of the LC-filter needs to be measured.

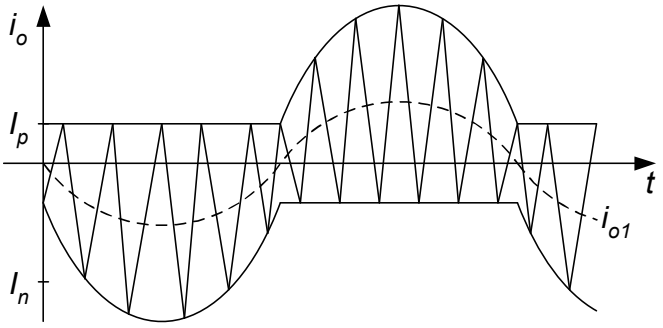


Figure 5.11: Output current and voltage waveform in a resonant converter

For very high switching frequency, the relationship between I_p, I_n and i_{o1} follows,

$$i_{o1} = \frac{I_p + I_n}{2} \tag{5.10}$$

For the simplest realization, I_p and I_n are determined by,

$$\begin{cases} I_p &= \max(I_b, 2i_{o1} + I_b) \\ I_n &= \min(-I_b, 2i_{o1} - I_b) \end{cases} \tag{5.11}$$

here, I_b is the lowest current for switching to take place.

The output voltage can be calculated by the output current and the impedance of the load.

$$V = IZ_l + V_{\mathrm{dc}}/2 \tag{5.12}$$

The time interval taken for the output current increasing from I_n to I_p is

$$t_r = \frac{L_f(I_p - I_n)}{V_{\mathrm{dc}} - V} \tag{5.13}$$

Similarly, the time interval taken for the output current decreasing from I_p to I_n is

$$t_r = \frac{L_f(I_p - I_n)}{V} \tag{5.14}$$

here, the capacitances of the output filter are considered large enough.

In Figure 5.12, the probability density function calculated over the switching period of a resonant converter is plotted. The switching period is varying in a wide range from 3.2 μs to 32 μs. The probability of the switching period is not evenly distributed. The maximum probability occurs at 32 μs.

The hierarchical approach is used here to calculate the noise spectrum of the resonant converter. The result of predicted noise spectrum on the functional level is shown in Figure 5.13. Some peaks in the spectrum correspond to the switching period with maximum probability.

After applying the correcting factors of the edges, the final result of the calculated noise spectrum is shown in Figure 5.14.

5.5 Experimental verification

The resonant converter is also measured by compliance EMC measurement equipment. The experimental result is shown in Figure 5.15.

Comparing with the predicted result, there are some differences. Here are the explanations for the differences.

- The differences in the low frequency range may be due to the possible value deviation of the components, especially due to the inductance of the resonance inductor. In the variable switching frequencies, the inductance value is no longer fixed. The variable inductance can spread the resonance frequency to wider frequency range.

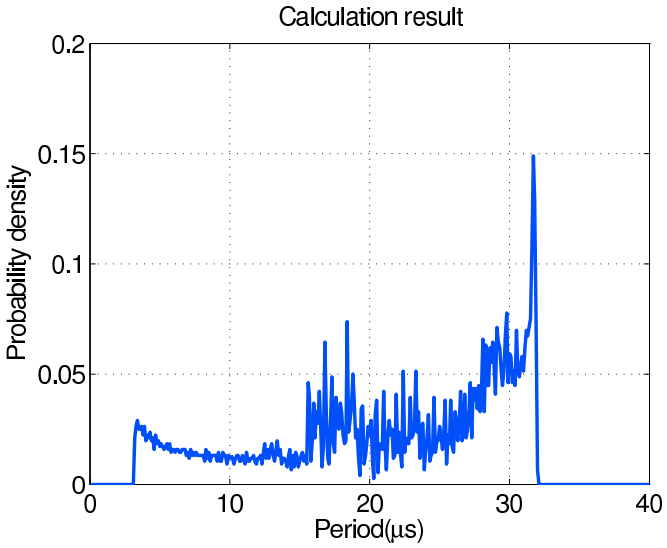


Figure 5.12: Probability density calculated over the switching period of a resonant converter

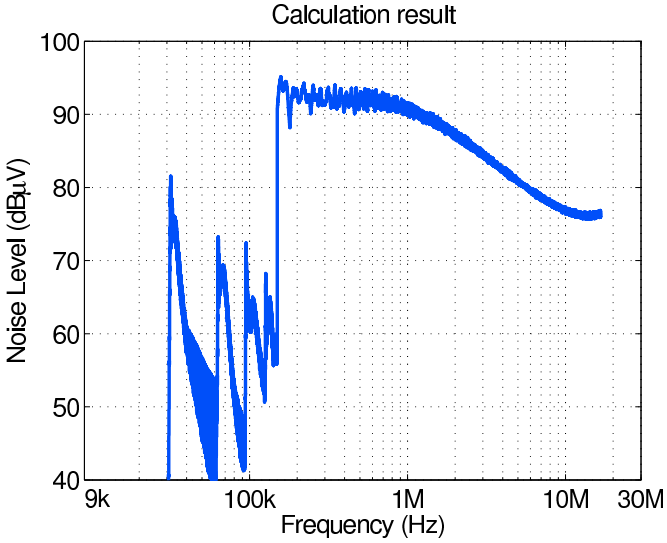


Figure 5.13: The predicted noise spectrum of a resonant converter before applying the corecting factors

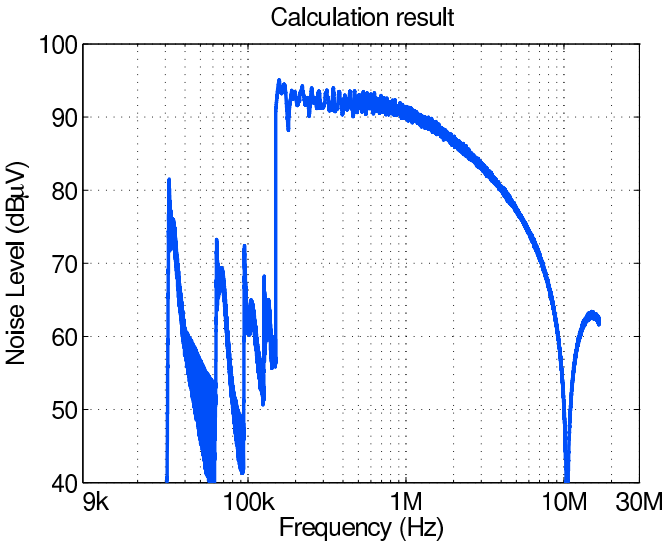


Figure 5.14: The predicted noise spectrum of a resonant converter after applying the corecting factors

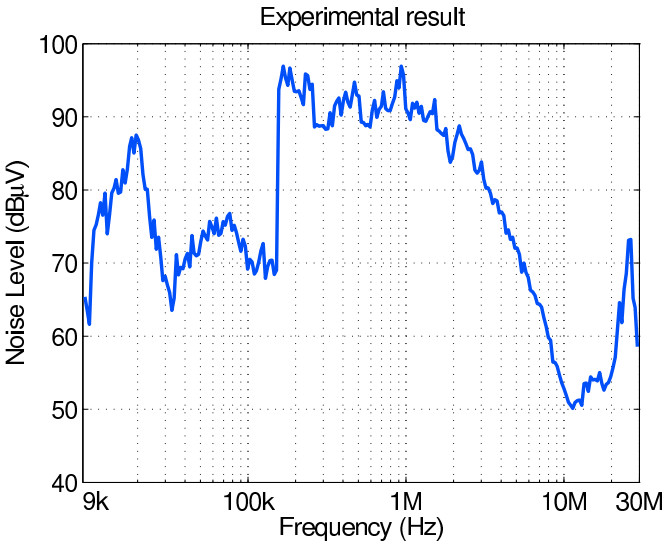


Figure 5.15: Experimental verification of the noise spectrum of a resonant converter

- The difference in the high frequency range may be due to the not detailed model of propagation path. This can be improved by detailed modeling or through experimentation [Che98].
- A peak appears around 28 MHz in the measured spectrum. It is caused by the occasional hard switching which is shown in the time domain in Figure 5.10. Although the lowest switching current I_b is set in the converter to 4 A, and it is already higher than the condition given by (5.9) to avoid hard switching, the current sensor circuit may be disturbed causing the switching to occur at the wrong moment. This can be avoided by improvements in the control circuit.

5.6 Summary

In this chapter, a new approach to model the noise source is explained. This approach overcomes the limitations of previous methods. It can be used to model the noise source with variable interval times between transients and variable transient waveforms. This approach is applied to a resonant converter that operates under ZVS conditions. The experimental result is compared to a calculated result. This method of noise source modeling is especially for AC-AC converters due to their variable operating points on the functional level.

Chapter 6

Suppression in the noise source

In this chapter, suppression approaches which are implemented on the noise source side are discussed. Firstly, the remedies in the literature and their limitations are reviewed. A new active filter approach called ''fourth leg compensator'' is proposed. Its principles are introduced. How the values of components in the compensator are determined to obtain the satisfying suppression effect is explained. The simulation results are presented. It is shown that the new active filter overcomes limitations of previous approaches and can be a potential solution to solve EMI issues in motor drive systems.

6.1 Introduction

As we discussed in Chapter 3, the noise level received at the victim is decided by the noise level of the noise source and the conversion efficiency at the propagation path. The suppression approaches can be divided into two categories according to where the mitigations are taking place. For the approaches which are implemented in the noise source, the mitigations are realized in three ways:

- reducing the noise spectrum by changing the transient waveform,
- decreasing the repetition frequency of the switching events,
- creating additional noise sources which are anti-phase to the original noise sources.

The first type of the suppression approaches modifies the shape of the waveform at each transient. In [Hol04], the edges of each hard switching transient are controlled to become optimized shapes to mitigate the noise spectrum. The improvement is only in the high frequency range. The resonant converter is another solution which is studied in Chapter 5. The transient edges are replaced

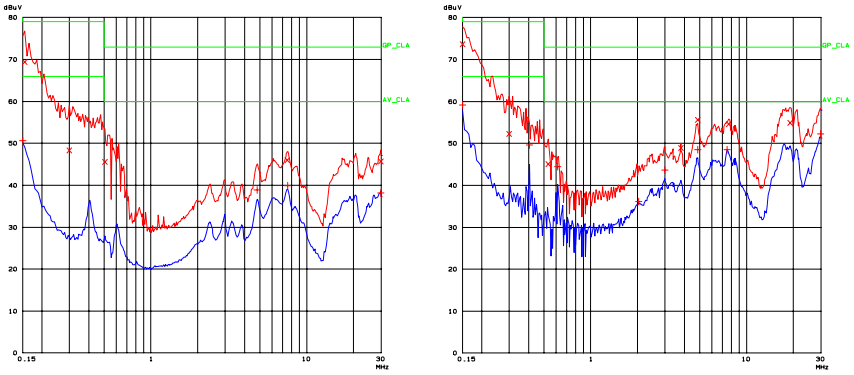
by the resonances. The resonances make the commutations much smoother than with hard switching. The resonance frequency changes with the load current. For very low load current, once the condition in Equation (5.9) is satisfied, a hard switching occurs next to the resonance. Because these hard switching transients occur occasionally, the overall EMI level is not suppressed as expected. In [Kim97; Hab02; Han04], diodes are used to limit the output voltage to the DC-bus voltage. The amplitude of the CM voltage is decreased. The main drawback is that the voltage transient slope is not changed. Therefore, the EMC performance is improved in the low frequency but not in the high frequency range.

The second factor that influences the final EMI spectrum is the time interval between transients. It relates to the PWM modulation strategy or the switching frequency of the converter. In [Cac99], it is shown that by choosing a suitable PWM method, the common mode current can be reduced by reducing the amount and amplitude of common mode voltage transients. This method can be further enhanced by including a small common mode inductor [Hav08]. For modern motor drive systems, the switching frequency is normally above 4 kHz. The switching frequency is close to or larger than the intermediate frequency band width (IFBW) of the measurement receiver. For the compliance receiver, there is only one sideband centered around harmonics hf_c falling into the IFBW. The noise source is a kind of narrow band source. As known from the Equation (5.1), higher repetition frequency brings a higher spectrum level for the noise sources having the same transient waveforms.

For most compliance measurements using a QP detector, there is a correcting factor between the QP detector result and Pk detector result. A lower repetition frequency means a longer discharge time for the QP detector, therefore, there is a larger correlation factor to adjust the QP detector result to a lower spectrum level. The QP measurement result can be much lower with a lower switching frequency. Observing Figure 5.3 and Figure 5.4, for power switching converters, the correlation factor takes effect when the converter works with a switching frequency less than 9 kHz. For a converter with a 16 kHz switching frequency, the correcting factor is 0 dB. For 4 kHz switching frequency, the correcting factor can be -6 dB.

In Figure 6.1, the spectra of a converter running under 4 kHz and 16 kHz switching frequencies are compared. Since the switching frequency is increased by 4 times, the spectrum should be lifted 12 dB. This is consistent with the graphs. It can also be observed that the difference between the QP detector result and Pk detector result is larger for the converter running under 4 kHz than the converter running under 16 kHz.

Most parts of the spectrum follow the ‘‘shifting vertically’’ rule, but an exception occurs around the frequency range 300 kHz - 600 kHz. The transient waveform is unavoidably changed by the changing of switching frequency. To reduce the current ripple and the size of energy storage elements, high switching frequency is required. Decreasing the repetition frequency of switching events is always accompanied by side effects.



(a) (b)

Figure 6.1: Spectrum of measured noise in LISN; (a) 4 kHz switching frequency, (b) 16 kHz switching frequency; upper trace: prescan Pk detector, lower trace: prescan Av detector, x point: final measurement QP detector, + point: final measurement Av detector

The third approach is creating anti-phase sources to compensate the noise sources.

In [Coc03], an auxiliary anti-phase winding has been added to compensate for the noise source. Passive canceling circuits are also reported in [Mur92; Swa01; Mei03]. All these circuits include voltage detecting and voltage compensation parts. Because they are passive filters, the control scheme can only be the feed-forward method. The detection circuit always needs to draw current since the input impedance of the voltage compensator cannot be infinite. The voltage dropping along the detecting circuit brings the error of the compensating voltage [Mei03]. In [Son06], general active filters that can be applicable to the EMI filter are reviewed. For active filters, the control scheme can be feed-forward or feed-back and the compensating signal has a much smaller error. In [Son02], such mitigation circuits have been described. In [Sho03], the balanced switching converter circuit is proposed to reduce the CM noise. In [Jau99], an approach called ‘‘dual-bridge inverter’’ uses three extra inverter legs to create extra noise sources to mitigate CM noise. In [Jul99], only one inverter leg is used instead of three inverter legs to reduce the CM voltage to zero. In ideal situations, the CM voltage can be compensated completely to constant zero. The CM current is eliminated. The drawback is that the zero state in the PWM pattern is not allowed. To get rid of zero vector states, a specific modulation technique has to be chosen. It brings side effects, for instance, reduction of the maximum modulation index, increased amount of switching and power loss, increased current ripple.

A new approach is proposed to suppress the CM voltage generated in motor drive systems. The strategy is trying to suppress both the transient slope and amplitude of CM voltage using only one additional inverter leg. It is a compromise between complexity of additional circuits and efficiency of mitigation.

6.2 Operation principle

The diagram of this approach is shown in Figure 6.2. Here the extra winding of the CMC is connected between the fourth leg compensator and the middle point of the DC-bus. The inductor L_y is used when the CM transformer is not ideally coupled.

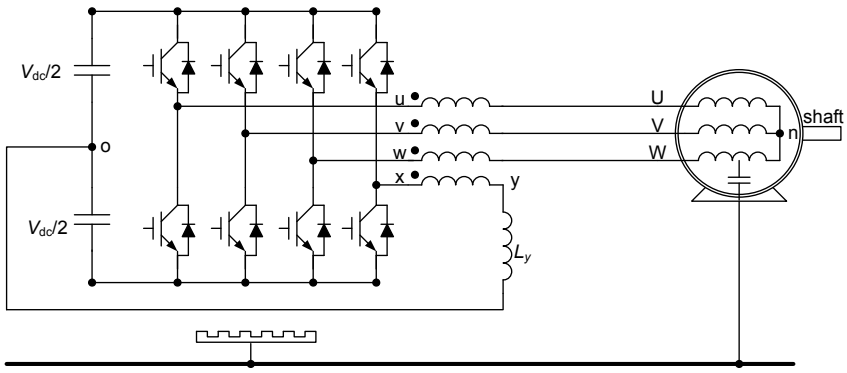


Figure 6.2: The diagram of the fourth leg approach

The strategy is summarized as below:

1. Synchronize the voltage in the fourth leg jumps with the voltage jumps in any other three inverter legs.

2. Reset the voltage in the fourth-leg with a slow slope if the voltages of the other three inverter legs change sequentially in the same direction (0→1 or 1→0).

The voltage waveforms of all inverter legs are illustrated in Figure 6.3. The converter is using SPWM modulation. The reference vector state v_r is supposed in sector 1. The complete period of PWM voltage signal is composed of two active vector states (V_1 and V_2) and two zero vector state (V_0 and V_7). v_u, v_v and v_w are the terminal voltage outputs in three inverter legs. The waveform v_{CM0} represents the CM voltage waveform when no suppression is applied. It is obvious that the peak-to-peak amplitude of the v_{CM0} is V_{dc}, and the CM current i_{CM} is unavoidable because of the fast transient edge of v_{CM0}.

The output voltage of the fourth leg compensator is represented by the waveform v_x in Figure 6.3. By applying the voltage v_x on the extra winding of the CM transformer, the peak-to-peak amplitude of the CM voltage v_{CM} is reduced to $V_{\mathrm{dc}}/2$ and the CM current i_{CM} is suppressed because of the slow transient edge of v_{CM}. The CM current i_{CM} is almost eliminated.

In Figure 6.3, the v_x changes states when one of the v_u, v_v and v_w changes its states. The v_x always needs to reset its states slowly and prepares for next compensation since the v_u, v_v and v_w change sequentially from 0 to 1 or from 1 to 0. The reset procedure must be much slower than the original transient of the terminal voltage signal to avoid generating new noise sources.

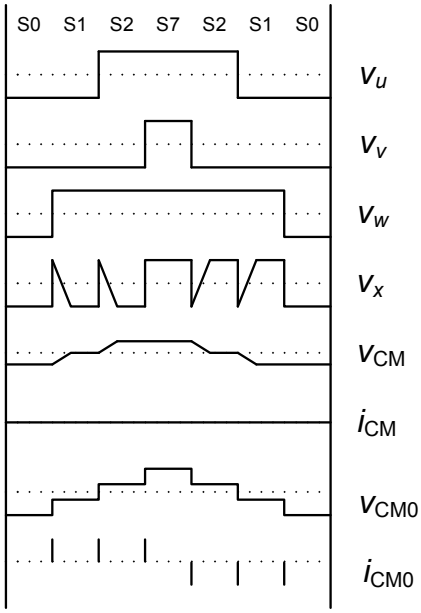
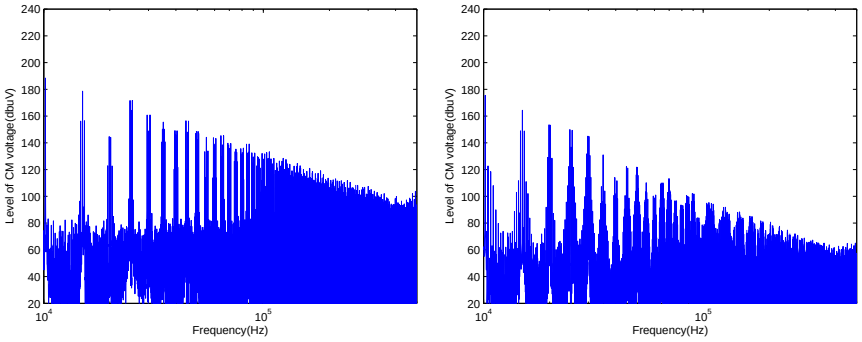


Figure 6.3: The voltage waveform of the fourth leg approach

The simulated spectra of CM voltage are shown Figure 6.4. In this simulation, the compensation is supposed to be perfect, it is an idealized situation.

With this approach, we use only one extra inverter leg to balance the CM voltage, and the zero vector states of the PWM modulation are still available. No special PWM modulation is necessary. This overcomes the limitation of the active filtering method in [Jau99; Jul99]. The amplitude of the CM voltage is reduced to 50% of the CM voltage before mitigation. As explained in Subsection 2.6.3, the EDM bearing current is produced when the amplitude of the CM voltage exceeds a threshold voltage, therefore, the decreasing of the CM voltage can mitigate EDM in most case.



(a) (b)

Figure 6.4: Spectrum of the CM voltage; (a) before adding the fourth leg compensator, (b) after adding the fourth leg compensator

The CM high frequency current can also be reduced. It benefits from the compensation of the fast transients. The newly created slow transients have much less high frequency components than fast transients.

6.3 The determination of the values of magnetic components

Here, we explain how to determine the magnetic component values to minimize the CM current flowing through the CM path. The magnetically coupled windings can be modeled and simplified as a CM transformer as shown in Figure 6.5. A set of voltage-current equations is given by

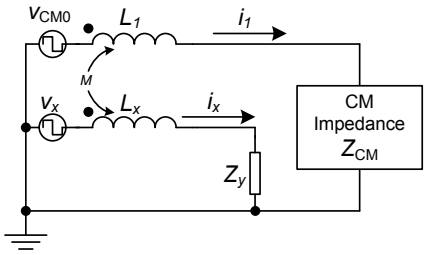


Figure 6.5: The diagram of the fourth leg approach

$$\begin{cases} v_{\mathrm{CM0}} &= (sL_1 + Z_{\mathrm{CM}})i_1 + sMi_x \\ v_x &= sMi_1 + (sL_x + Z_y)i_x \end{cases} \tag{6.1}$$

here,

v_{CM0}	is the inverter output CM voltage,
v_x	is the compensation voltage in the fourth leg,
i_1	is the flowing current in the CM path,
i_x	is the flowing current in the fourth leg path,
L_1, L_x	is the coupled windings in the CM path and the fourth leg path,
Z_{CM}	is the impedance of the CM path,
Z_y	is the impedance of the extra winding in the fourth leg path.

Here i_1 can be derived by Equation (6.1),

$$i_1 = \frac{(sL_x + Z_y)v_{\mathrm{CM0}} - sMv_x}{(sL_1 + Z_{\mathrm{CM}})(sL_x + Z_y) - s^2M^2} \tag{6.2}$$

To let the CM current be zero in a wide frequency range, the numerator of Equation (6.2) has to be equal to zero.

6.3.1 Ideal coupling

To achieve $i_1 = 0$, the corresponding component values in the compensator are derived. The deriving starts with the assumption of ideal coupling between the windings in the CM transformer. We have $L_x = (\frac{N_x}{N_1})^2 L_1$ and $M = (\frac{N_x}{N_1})L_1$. Here N_x and N_1 are numbers of turns of the windings of the CM tranformer. If the condition $\frac{v_{\mathrm{CM0}}}{v_x} = \frac{N_1}{N_x}$ is satisfied, then i_1 can be zero.

Here, extra winding providing Z_y is not necessary in the fourth leg. On the contrary, the Z_y must be zero. Therefore, a hidden condition is that the leakage inductances of the CM transformer must be zero. The condition to achieve $i_1 = 0$ with ideal coupling condition is consistent with the conclusion derived in [Mei03].

6.3.2 Nonideal coupling

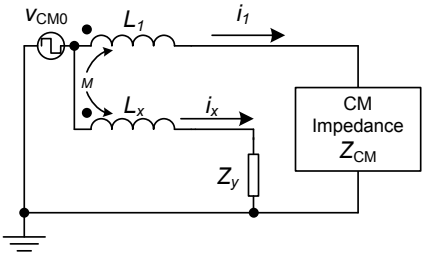
In real situations, the coupling cannot be idealized. Actually, under nonideal coupling conditions, we can still achieve $i_1 = 0$ by extra winding providing Z_y.

If the coupling coefficient is a constant k which is smaller than 1, then $M = k\sqrt{L_1 L_x}$. To let i_1 be zero, we need the following condition,

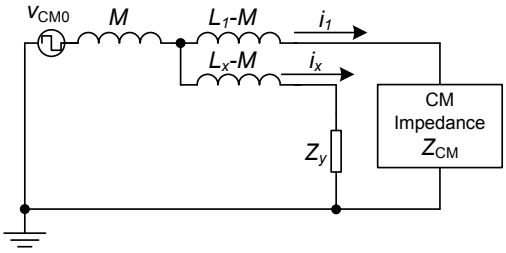
$$L_y = \frac{v_x}{v_{\mathrm{CM0}}} M - L_x \tag{6.3}$$

As long as the condition $N_x < kN_1 \frac{V_x}{v_{\mathrm{CM0}}}$, the L_y calculated by Equation (6.3) is larger than 0. Satisfying this condition is feasible. In the special condition when $v_{\mathrm{CM0}} = v_x$, the Equation (6.3) is simplified to $L_y = M - L_x$. How compensation takes place can be explained clearly by the equivalent circuit method.

Two voltage sources can be replaced by one source when $v_{\mathrm{CM0}} = v_x$ as shown in Figure 6.6(a). Then T-Equivalent tranformer is used to eliminate the mutual inductance. The Figure 6.6(b) shows the equivalent circuit. When $\frac{N_x}{N_1} < k$, $Lx - M$ is a negative inductance. With $L_y = M - L_x$, the impedance in the branch of the fourth leg is zero and the entire CM current is bypassed through the fourth leg path instead of the CM path which is exactly our goal.



(a) $v_{\mathrm{CM0}} = v_x$



(b) T-Equivalent transformer

Figure 6.6: Simplified diagram of fourth leg approach to show the mitigation principle in the special condition $v_{\mathrm{CM0}} = v_x$

If the leakage inductance L_σ of the CM transformer is not zero, the extra winding inductance L_y can be the value of $\frac{v_x}{v_{\mathrm{CM0}}} M - L_x - L_\sigma$ to achieve a good compensation.

6.4 The control method

In the fourth leg compensator, there is a drive circuit between the logic control and the output terminal voltage with controllable slope. For this key circuit, the following specifications are required:

1. It is connected to the DC-bus of the motor drive. The voltage ratings of transistors are the same as that of the other three inverter legs.

2. The dv/dt slope and the transient time of the output voltage need to be controlled. Two fixed slopes of the dv/dt are necessary. The fast one (200 ns-500 ns) is used to compensate the transients of the other three phase lines. The slow one (2 μs-5 μs) is used to reset the compensator for the next transient if it is required.

3. The gate signal and slope control signal are provided by the DSP board and the interface utilizes plastic optic fibers for galvanic isolation.

In Figure 6.7, the circuit diagram of the fourth leg compensator is illustrated.

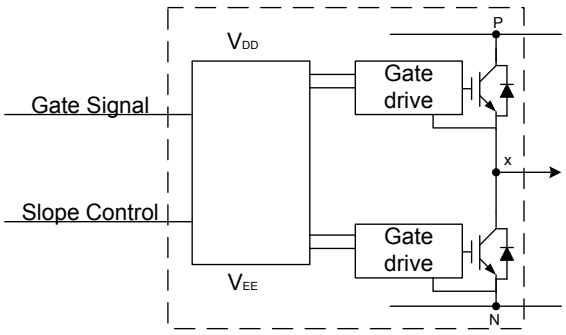


Figure 6.7: The circuit diagram of the fourth leg compensator

For three-phase PWM VSD systems, there are $2^3 = 8$ switching vector states. The number N of the inverter outputs which are connected to the positive bus rails can be (0,1,2,3). The corresponding relationships between the switching vectors and the CM voltage are given in Table 6.1. Here, the algorithm to calculate the gate signal and slope control signal is presented in Figure 6.8. Figure 6.9 shows the waveforms of all control and terminal voltages of the fourth leg compensator.

Table 6.1: The corresponding relationships between the switching vectors and the CM voltage in a three-phase motor drive

Vector	v_u	v_v	v_w	v_{CM0}	N
0	0	0	0	$-V_{\mathrm{dc}}/2$	0
1	1	0	0	$-V_{\mathrm{dc}}/6$	1
2	1	1	0	$V_{\mathrm{dc}}/6$	2
3	0	1	0	$-V_{\mathrm{dc}}/6$	1
4	0	1	1	$V_{\mathrm{dc}}/6$	2
5	0	0	1	$-V_{\mathrm{dc}}/6$	1
6	1	0	1	$V_{\mathrm{dc}}/6$	2
7	1	1	1	$V_{\mathrm{dc}}/2$	3

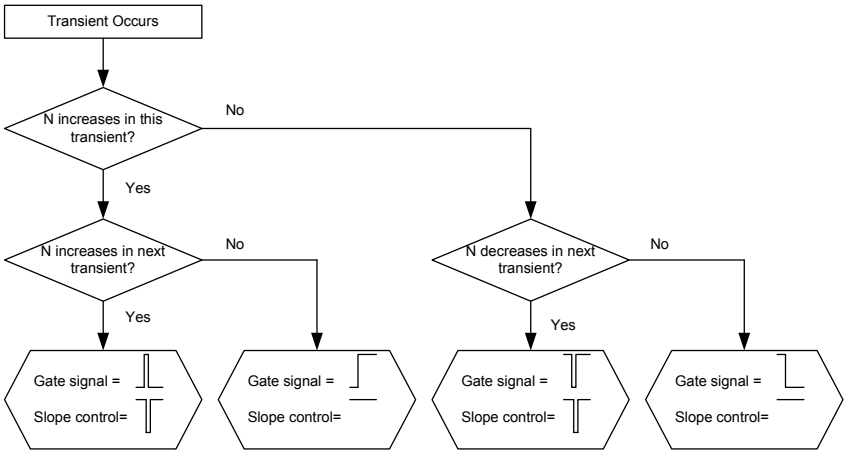


Figure 6.8: The algorithm to generate the gate signal and slope control signal for the fourth leg compensator

6.5 The method to generate variable voltage transient slopes

As known from the previous sections, the variable voltage transient slope is a key issue in this fourth leg compensator approach. Actually, we need a transient with a fast slope to compensate the transient of the other inverter legs, and we use a transient with a slow transient slope to reset the state of the fourth leg compensator before the next compensation if it is required.

Several approaches are proposed to control the voltage transient slopes. In [Par01], The principle is using the effective miller capacitance between gate and drain to adjust the slope electronically. In [Con96], auxiliary current source and auxiliary current sink are used to change the variation of the drain voltage during the turn-on and turn-off transient. Another main contributor in active gate control method suggests adding a precondition bias to the demand reference waveform shifts the IGBT into the active region for dv/dt control [Pal04]. We use the approach [Par01] in a simulation to show the feasibility using the simplified diagram shown in Figure 6.10.

By adjusting the gain of the current controlled current source, the slopes changes from approximately 1420 V/μs to 6960 V/μs for turn-off and from approximately 994 V/μs to 6960 V/μs for turn-on. The simulation result is shown in Figure 6.11.

Further simulation is done in a full circuit. The control signal is calculated and fed to the fourth leg compensator. In Figure 6.12, the voltage transient slope is changed according to the requirements. The average power dissipation is estimated as 15.5 W for a 15 kW motor drive working at 8 kHz switching

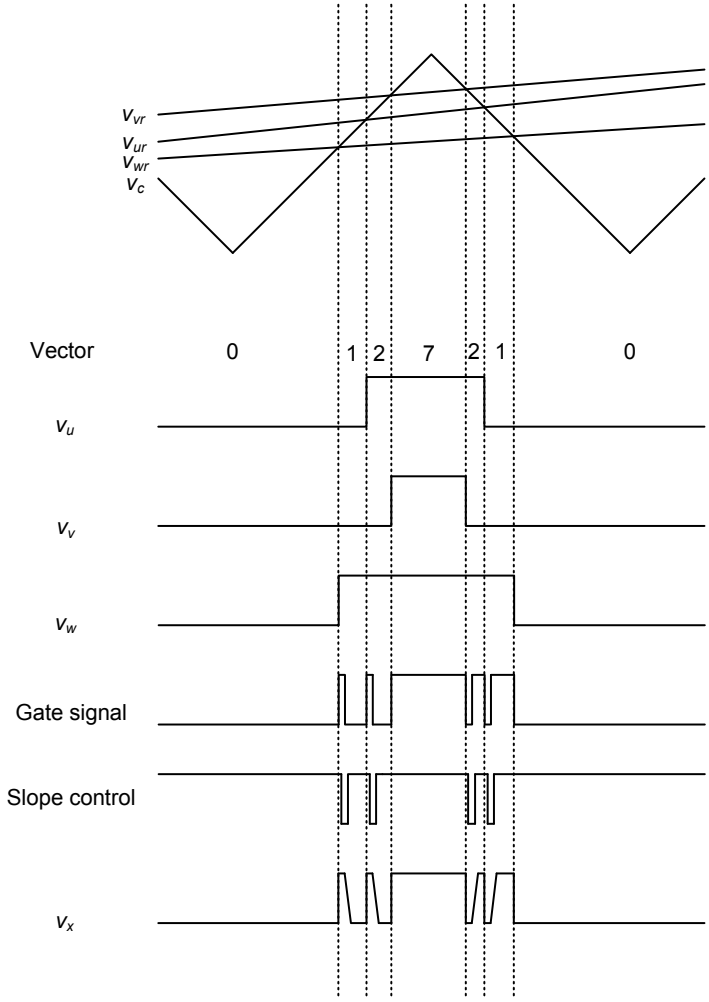


Figure 6.9: Voltage waveforms of control and output terminals in the fourth leg compensator

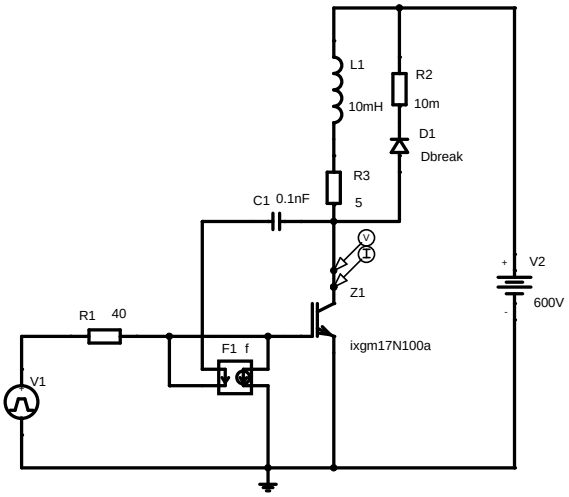
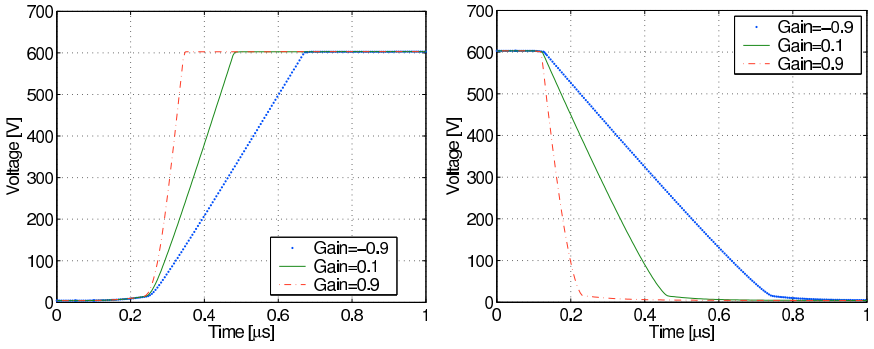
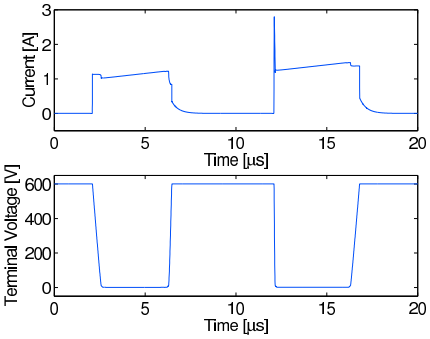


Figure 6.10: The equivalent circuit to control the voltage transient slopes

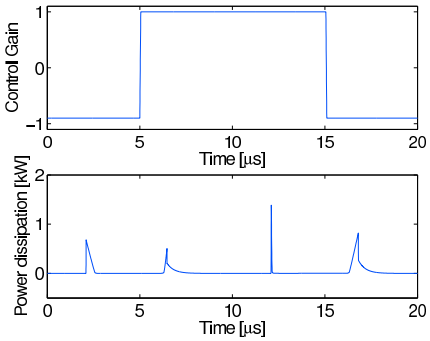


(a) Turn off (b) Turn on

Figure 6.11: Simulation results showing the controllable transient waveforms using active gate control



(a) Transient voltage and current waveform



(b) Control signal and power dissipation

Figure 6.12: Upper: simulation results showing the voltage and current switching waveforms of a transistor (IXGM17N100A) which is controlled by the flexible dv/dt control method. Lower: the control signal used for slope control and the calculated power dissipation

frequency. This is acceptable.

The influence of deadtime should be considered [Cir06; Cac09]. The deadtime is introduced to prevent a short circuit at the inverter leg in the commutation moment. The real moment of transients then depends on the polarity of the load current. This introduces the error in compensation. The influence of the deadtime can be mitigated if the polarity of the load current in each inverter leg can be measured and the fourth leg compensator can be controlled by an accurate digital circuit.

6.6 Summary

The EMC issue is a main concern before further improvement of motor drive systems can be made. The present solutions are always accompanied by drawbacks. This is the reason why the industry still uses traditional passive filters as their solution. Based on previous research results, a new CM noise suppression method is proposed called a ''fourth leg compensator''. Two main modifications bring benefit compared to previous remedies. One is achieved by adding an extra winding in the fourth leg path. This arrangement can compensate the CM voltage, even with nonideal coupling in the CM transformer and when leakage inductance is present. The second improvement is the arrangement of the switching pattern of the fourth inverter leg. Two slope rates exist in the turn-on and turn-off of the compensator. The high slope rate is used to compensate the transient of the other three inverter legs, while the low slope rate is used to reset the state of the fourth leg for the next transient if it is required. By this arrangement, zero vector states of the PWM modulation are not allowed, the amplitude of the CM voltage is reduced by 50%, and the CM voltage transients with high dv/dt are successfully compensated. This approach results in an increase of the number of active components, but a decrease in overall size and weight due to the smaller and lighter CMC can be used.

Chapter 7

Conclusions and recommendations

7.1 Conclusions

In this thesis, a hierarchical approach is proposed for analyzing the EMC problem of power electronics applications. This thesis focuses on two main issues. The first is to develop an approach which makes modeling and prediction of the EMI level in power electronic applications possible. The second is to develop suppression approaches for EMI noise.

When approaching the first issue, the main goal is to develop a design process. A hierarchical approach is proposed and demostrated in this thesis. The previous approaches to model the noise are based on many simplification assumptions. However, in many applications, this is not sufficient due to many recent developments in the field. These include variable switching frequency and variable transients of switches, hence, a hierarchical approach is proposed. The proposed approach has three steps. In the first step (functional level), a simple model of switches in the system is developed. The operating points of each switching transient and all time intervals are derived and the narrowband signals of the EMI noise can be derived. In the second step (transient level), the result contains detailed transient waveforms which take the variation of the nonlinear switching transient into account. In the third step (propagation level), the noise propagation through the system is described by the transfer ratio, and the EMC performance is evaluated.

In order to validate the hierarchical approach, it is applied to predict the noise in a resonant converter, which has not been done before. The major challenge for the AC-AC converter is that the operating points of voltage and current are not fixed as in a DC-DC converter and the current varies over a large range. This makes the transient slope of the current and voltage waveforms vary over a large range. It is very important to take this into account when predictiing

the associated EMI. Also, the time interval between transients is not fixed. The assumption used in the conventional approach, namely, periodic noise sources and a fixed propagation path, is then, not valid. This makes the hierarchical approach desirable for analyzing the EMI in power electronics, especially for an AC-AC converter.

The analysis on the functional level gives the noise source in the low frequency range. The detailed result achieved from the transient level is used in the propagation level analysis to get the noise source in the high frequency range. The final spectrum of the noise source is based on the combined results of narrowband noise and broadband noise.

To conclude the first issue addressed, this thesis presents a hierarchical approach which is applicable to analyze the EMC issue in power electronic applications. These aspects are presented together in a framework which demonstrates how to obtain operating points, how to obtain transient waveforms, how to predict noise levels in the low frequency range and the high frequency range respectively, and how to get the final noise source level. The predicted result is extended from a peak detector to an average detector and quasi-peak detector, which has not been included before.

The second issue is the development of suppression approaches for EMI noise. There are two proposed approaches for EMI suppression in this thesis. The first approach is by inserting a passive filter into the DC-bus. It can be concluded that the same noise suppression performance can be achieved using a DC-bus filter as the conventional AC side filter. The advantage of this approach is that the connections can be made very short which can improve the suppression significantly.

The transfer ratio is defined and can be measured by a low-cost current probe. The parasitic parameters of the model can be extracted based on the transfer ratio measurement results. Based on the established model, the benefit of using a DC-bus CM filter can be calculated efficiently in the frequency domain. The filter is installed inside the converter and the interconnections can be made very short. This can improve the suppression performance significantly and avoids the tricky task of designing or selecting a filter afterwards. The noises are suppressed partly inside the converter if the DC-bus filter is included in the design. For some critical requirements, the additional filter needed would be much smaller.

A new active filter is proposed as the second solution. The so called ''fourth leg compensator'' generates a signal to compensate the transients of the other three legs. This approach results in an increase of the number of active components, but a decrease in overall size and weight due to the decrease in passive components which would otherwise be needed for filters. The fourth leg approach is compared with another state of the art active approach viz., the double inverter bridge. For comparison, the previous fourth ''pseudo phase'' cannot use the zero vector states, which leads to undesirable secondary effects. This includes a reduction of the maximum modulation index, an increased number of switching transients, an increased current ripple and an increasing power loss. The fourth leg compensator suppresses the fast transient of CM voltage while reducing the

amplitude of the common mode voltage by 50%. A method to determine the values of the additional components is described. It is shown that the CM voltage can be compensated for even with nonideal coupling in the CM transformer and when leakage inductance is present.

7.2 Outlook towards future development

7.2.1 Systematic EMC design tool

The hierarchical approach is developed because the final EMC performance relies greatly on the result of the transient level analysis. The transient level analysis is based on the operating points obtained on the functional level analysis. The parts of the analysis based on the transient and functional level are familiar to power electronics specialists, but not to an EMC expert. Conversely, power electronics specialists are not familiar with the EMC standard and noise propagation paths. The hierarchical approach gives a clear way of task division for the whole problem. Therefore, a systematic EMC design tool based on the hierarchical approach could be realized by software programmers, power electronics engineers and EMC experts. The fundamental building blocks of this systematic tool are already available. For instance, simulation software for education purposes or design purposes can be used for functional analysis. The circuit simulation can be used for transient analysis if the libraries of components are added. The additional efforts include developing an extra interface to provide the details of the transients which can be used for EMC design.

7.2.2 Statistical method

To describe an aperiodic noise source, the present method creates a switching event list. For EMC analysis over a long period, for instance, the acceleration and deceleration process of the motor drive, the amount of collected data could be of a huge size. For this kind of problem, statistical approaches can be a solution. The characteristics of transients are analyzed, and the EMC performance can be linked to the probability distribution of the amplitudes and the time interval between the switching events.

7.2.3 Circuit realization

In Chapter 6, the fourth leg approach to compensate the CM voltage of the PWM motor drive is proposed. The theory and circuit simulation are presented. Due to time limitations, the circuit realization of the fourth leg approach was not done. It would be of great interest to start an experimental implementation of the fourth leg approach in order to investigate whether it can replace passive filters. The key point of the circuit is letting the transistor work in switching mode with variable

transient slopes. Letting transistors work in active mode is another possibility, but the power dissipation is increased.

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List of publications

This thesis is based on the works described in the following journal and conference papers

1. D. Zhao, J. Ferreira, A. Roc'h, and F. Leferink. Common-Mode DC-Bus Filter Design for Variable-Speed Drive System via Transfer Ratio Measurements. *IEEE Trans. Power Electronics*, vol. 24(2):pp. 518--524, 2009.

2. D. Zhao, J. Ferreira, A. Roc'h, and F. Leferink. New Common Mode EMI filter for motor drive using a fourth leg in the inverter. *in Proc. EMC Europe Int. Symposium on Electromagnetic Compatibility (EMC-Europe)*, pp. 741--746, 2008.

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6. A. Roc'h, D. Zhao, F. Leferink, H. Polinder, and J. Ferreira. Investigation of the Coupling Paths of a Galvanically Isolated AC/AC Converter. *in Proc. IEEE Symposium on Electromagnetic Compatibility (EMC)*, pp. 1--6, 2007.

7. D. Zhao, J. Ferreira, H. Polinder, A. Roc'h, and F. Leferink. Using transfer ratio to evaluate EMC design adjustable speed drive systems. *in Proc. EMC*

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The list of papers below are other collaborated works which are not included in the thesis

1. A. Roc'h, H. Bergsma, D. Zhao, J. Ferreira, and F. Leferink. Performances optimization aspects of common mode chokes. *in Proc. Int. Zurich Symposium on Electromagnetic Compatibility (EMC-Zurich)*, vol. 1: CDROM, 2008.

2. A. Roc'h, H. Bergsma, F. Leferink, D. Zhao, H. Polinder, and J. Ferreira. A new predictive model for performances evaluation of common mode chokes. *in Proc. Int. Zurich Symposium on Electromagnetic Compatibility (EMC-Zurich), Singapore*, vol. 1: CDROM, 2007.

3. A. Roc'h, H. Bergsma, D. Zhao, J. Ferreira, and F. Leferink. A new behavioural model for performance evaluation of common mode chokes. *in Proc. Int. Zurich Symposium on Electromagnetic Compatibility (EMC-Zurich)*, vol. 1: CDROM, 2007.

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5. A. Roc'h, H. Bergsma, F. Leferink, D. Zhao, H. Polinder, and J. Ferreira. Design of an EMI output filter for frequency converters. *in Proc. EMC Europe Int. Symposium on Electromagnetic Compatibility (EMC-Europe)*, pp. 123--127, 2006.

6. D. Zhao, J. van Duijn, F. Leferink, and W. van Etten. EMI synthesis and preventive methods for PWM driven DC motors. *in Proc. EMC Europe Int. Symposium on Electromagnetic Compatibility (EMC-Europe)*, vol. 1: CDROM, 2004.

Summary

Hierarchical EMC Design for Inverters in Motor Drive Systems

Power electronics applications are usually accompanied by high voltage and current amplitudes, and steep voltage and current transients. The EMI (Electromagnetic Interference) issue is regarded as the main side effect of power electronics applications. Noise level prediction is a vital task for filter design, but many difficulties are encountered. For instance, a large amount of experience is needed to build equivalent circuits, the use of simplified models often requires sacrificing details in the high frequency range, individual approaches must be developed for various topologies, etc. A new method for EMI prediction of power electronics applications is thus desirable.

The new method should overcome the following common characteristics of power electronics circuits: (a) the large difference between the time constants, and (b) the long time required to reach steady state. The time domain approach is very time-consuming. The assumptions used in the frequency domain approach, namely, periodic noise sources and a fixed propagation path, are also not valid. For example, the slopes of voltage and current transients depend on the operating points, and the assumption of periodic noise sources does not apply. Because the junction capacitors of power rectifiers and switches change with the reverse voltage, the values of the components in the noise propagation path also change.

In this thesis, a hierarchical approach is proposed for the EMC design of inverters in motor drive systems. It combines the advantage of the time domain and frequency domain approach to achieve a fast, universal and accurate result. The approach is validated by observations in the time domain and the frequency domain. The proposed approach has three steps. In the first step (functional level), a simple model of switches in the system is developed. The operating points of each switching transient and all time intervals are derived and the narrowband signals of the EMI noise can be derived. The second step (transient level) results in detailed transient waveforms which take the variation of the nonlinear switching transient into account. In the third step (propagation level),

the noise propagation through the system is described by the transfer ratio, and the EMC performance is evaluated.

The approach is described in detail, and then a PWM voltage source inverter feeding an induction motor is analyzed using this approach. This approach is also applied to a resonant converter that operates under ZVS conditions. The experimental results are compared to calculated results.

Two approaches are proposed for EMI suppression in this thesis. The first approach is by inserting a passive filter into the DC-bus. It can be concluded that the same noise suppression performance can be achieved using a DC-bus filter as the conventional AC side filter. The advantage of this approach is that the connections can be made very short which can significantly improve the suppression.

A new active filter called the ''fourth leg compensator'' is proposed in this thesis. The fourth leg inverter generates a signal to compensate the transients of the other three legs. It can suppress the fast transients of common mode voltages while reducing the amplitude of the common mode voltage by 50%. A method to determine the values of the additional components is described. It is shown that the CM voltage can be compensated for even with nonideal coupling in the CM transformer and when leakage inductance is present.

Dongsheng Zhao

Samenvatting

Hiërarchisch EMC Ontwerp voor Inverters in Motoraandrijfsystemen

Een vermogenselektronische toepassing gaat meestal gepaard met grote spannings- en stroomamplitudes en steile spannings- en stroomtransiënten. De EMI (Elektromagnetische Interferentie) kwestie wordt beschouwd als een belangrijk neveneffect van vermogenselektronische toepassingen. Het voorspellen van het ruisniveau is een essentiële taak bij het ontwerpen van filters, maar men komt hierbij veel moeilijkheden tegen. De voorspelling vraagt bijvoorbeeld veel ervaring in het bouwen van equivalente circuits, het gebruik van een vereenvoudigd model leidt vaak tot verlies van hoogfrequente details, individuele benaderingen moet ontwikkeld worden voor verschillende topologieën, etc. Daarom is een universele methode om de EMI van vermogenselektronische toepassingen te voorspellen wenselijk.

De universele methode zou de volgende karakteristieken van vermogenselektronische schakelingen moeten overwinnen: (a) het grote verschil tussen de tijdconstanten, (b) de lange tijd die nodig is voordat de stabiele toestand bereikt is. Simulaties uitvoeren in het tijddomein is zeer tijdrovend. De veronderstellingen die in het frequentiedomein gebruikt worden, namelijk dat ruisbronnen een periodiek signaal genereren en dat het propagatiepad vast is, zijn niet geldig. De hellingen van spannings- en stroomtransiënten hangen bijvoorbeeld af van de werkpunten en de veronderstelling van een periodieke ruisbron is niet correct. Omdat de junctiecapaciteiten van gelijkrichters veranderen met het omkeren van de spanning is het ruispropagatiepad ook niet vast.

In dit proefschrift wordt een hiërarchische benadering voorgesteld voor het EMC (Elektromagnetische Compatibiliteit) ontwerp van inverters in motoraandrijfsystemen. Het combineert de voordelen van de tijddomein- en de frequentiedomeinbenadering om een snel, universeel en accuraat resultaat te bereiken. De geldigheid van de benadering wordt door de waarnemingen in het tijddomein en het frequentiedomein bevestigd. De voorgestelde benadering heeft drie stappen. In de eerste stap (functioneel niveau) wordt een eenvoudig model met schakelaars van het systeem ontwikkeld. De werkpunten van elke schakeltransiënt en elk

tijdinterval worden afgeleid en de smalbandige signalen van de EMI ruis kunnen afgeleid worden. De tweede stap (transiënt niveau) resulteert in gedetailleerde transiëntgolfvormen waarin rekening gehouden is met de variatie van de niet-lineaire schakeltransiënt. In de derde stap (propagatie niveau) wordt de ruispropagatie door het systeem beschreven door de overdrachtsverhouding en wordt het EMC gedrag geëvalueerd.

De benadering wordt in detail beschreven, waarna een PWM (pulsbreedtemodulatie) spanningsbron inverter die een inductieve motor voedt, geanaliseerd wordt aan de hand van deze benadering. Deze benadering wordt toegepast op een 'resonant inverter' die de spanning omschakelt tijdens de nuldoorgangen van de spanning. De experimentele resultaten worden vergeleken met berekende resultaten.

Twee benaderingen voor EMI onderdrukking worden in dit proefschrift voorgesteld. De eerste benadering houdt het toevoegen van een passief filter op de gelijkspanningsbus in. De conclusie kan getrokken worden dat door toevoeging van dit filter dezelfde onderdrukking van de ruis bereikt kan worden, als met het toevoegen van een conventioneel filter aan de wisselspanningskant. Het voordeel van deze benadering is dat de verbindingen zeer kort gemaakt kunnen worden, wat de onderdrukking drastisch kan verbeteren.

Een nieuw actief filter, dat ''fourth leg compensator'' (vierde tak compensator) genoemd wordt, wordt in dit proefschrift voorgesteld. De inverter met een vierde tak genereert een signaal om de transiënten van de andere drie takken te compenseren. Het kan de snelle transiënten van de common mode spanning onderdrukken, terwijl het de amplitude van de common mode spanning met 50% laat afnemen. Een methode wordt beschreven om de waardes van de toegevoegde componenten te bepalen. Het wordt aangetoond dat de common mode spanning , zelfs met niet-ideale koppeling van de common mode transformator en het voorkomen van parasitaire inductiviteit, gecompenseerd kan worden.

Dongsheng Zhao

Curriculum Vitae

Dongsheng Zhao was born in Yining city, China on February 12, 1975. He moved with his family to Wenzhou city, when he was five years old.

He received the B.Sc degree in Electronic Engineering from Shanghai Jiao-Tong Univeristy, Shanghai, China, in 1993. Then he joined industry for 9 years. He worked as a technical engineer in Wenzhou postal, telegraph and telephone office, served as a vice general manager in Zhejiang GuoXin Telecommunication company Wenzhou branch, and was a manager in the mobile department in China Unicom Corporation Wenzhou branch. During his work, he got a MBA (Master of Business Administration) degree from Zhejiang University, Hangzhou, China in 2001.

He went to the Netherlands to continue his technical education in 2002. He completed his master degree of Electric engineering in 2004 in University of Twente, Enschede, the Netherlands. He did his master assignment in specials division, at Nedap N.V., Groenlo involving the EMC issues in an automotive application. He did internship after his graduation at the power supply division, at the same company.

He was a Ph.D. researcher (in Dutch: *Assistent in Opleiding* or AIO) with the electrical power processing group at the faculty of Electrical Engineering, Mathematics and Computer (in Dutch: *Elektrotechniek, Wiskunde en Informatica* or EWI) at Delft, the Netherlands during November 2004 till October 2008.

Since November 2008, he is a research scientist in research and development department, at VSL, Dutch Metrology Institute, at Delft, the Netherlands. His tasks include realization, maintenance and development of the national primary standards for electromagnetic fields, power and other electrical quantities.

Dongsheng is married to Ran since the 27th of December, 2002 and they have two sons, Chengji and Xingqi, born at the 26th of June, 2003 and the 11th of August, 2008.