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Towards Health Monitoring of SiC MOSFETs by Precise Junction Temperature Profiling

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***Abstract*—Silicon-Carbide (SiC) MOSFETs are widely used in high-power and high-efficiency applications such as electric vehicles and power supplies. However, long-term reliability remains a critical concern, particularly under extreme operating conditions. This work aims to explain the health monitoring of SiC metal oxide-semiconductor field effect transistors (MOSFETs) through precise junction temperature (T_j) profiling based on performed measurements. The study focuses on the temperature-dependent behavior of the on-resistance ($R_{DS(on)}$), a key parameter that varies with the aging, degradation, and temperature of the device. By systematically measuring $R_{DS(on)}$ at different temperatures and at various stages of the operating life of the device, we can establish a predictive model to assess the health of SiC MOSFETs. The importance of pulse duration of the drain current is stressed to avoid the self-heating effect with some device physics insights. The proposed methodology enables better understanding of the SiC MOSFET performance for future real-time condition monitoring, facilitating early failure detection and lifetime estimation. This approach provides valuable information for improving reliability and optimizing maintenance strategies in power electronics systems. Experimental results validate the effectiveness of the proposed method and give direction for future research opportunities.**

***Index Terms*—SiC MOSFET, wideband-gap, Health Monitoring, Realibility, Electrical characterization.**

I. Introduction

Silicon-carbide (SiC) based wide band gap semiconductor power devices have emerged as an alternative to conventional silicon-based (Si) devices for higher switching frequency, operating temperature and efficiency [1]. For example, it is shown that the use of SiC-based inverters reduced the average junction temperature by almost 35% considering improved system efficiency of more than 20% as compared to Si in the same cooling conditions [2]. Furthermore, SiC Metal Oxide-Semiconductor Field-Effect Transistors (MOSFETs) can be designed to have a much higher Drain-Source Blocking Voltage ($V_{DS,block}$) due to lower losses in its drift region as compared to Si MOSFET. With higher voltages, comes more challenges related to thermal management, due to higher temperatures. For this reason, precise determination of the junction temperature while operating is critical, especially in short-circuit events because the short-circuit current can generate a significant amount of heat on a very short time scale [3]. Research is carried out to extract the junction temperature online using the on-state voltage [4], gate resistance [5], on-resistance - forward voltage combination [6], or through measuring the forward voltage [7], which is often a parameter used by power cycling. In [8] the extracted quasi-threshold voltage has a high linearity with the junction temperature. Some parameters are more sensitive to the temperature change for example the trans-conduction gain K_n, which is linear only at some interval [9]. Some work use a method of determining the junction temperature by using the saturation current [10]. Another junction temperature measurement method based on the inherent electroluminescence (EL) in the body diode is presented in [11]. We investigate a method to determine the junction temperature via the on-resistance, which has been explored as a linear dependency in [12]. We further explore making a custom 3D plot that can be used as information when modeling and switching the device, while measuring the on-resistance $R_{DS(on)}$ to detect early degradation before catastrophic failure. To verify this approach, a custom PCB is designed to measure the $R_{DS(on)}$, in addition to controlling the temperature and changing the pulse width of the drain current. By varying the pulse width of the drain current for different gate voltages, it is observed that the dependency between $R_{DS(on)}$ and T_j is non linear.

A. On-resistance in SiC MOSFET

The on-resistance of a SiC MOSFET is temperature-dependent due to various intrinsic semiconductor effects [13], [14]. It consists of multiple resistive components, some of which exhibit significant temperature dependence. These components are presented in Figure 1 [15], on a cross section of a SiC MOSFET. Based on these components, the total $R_{DS(on)}$ is given by (1), wherein each component is explained in Table I.

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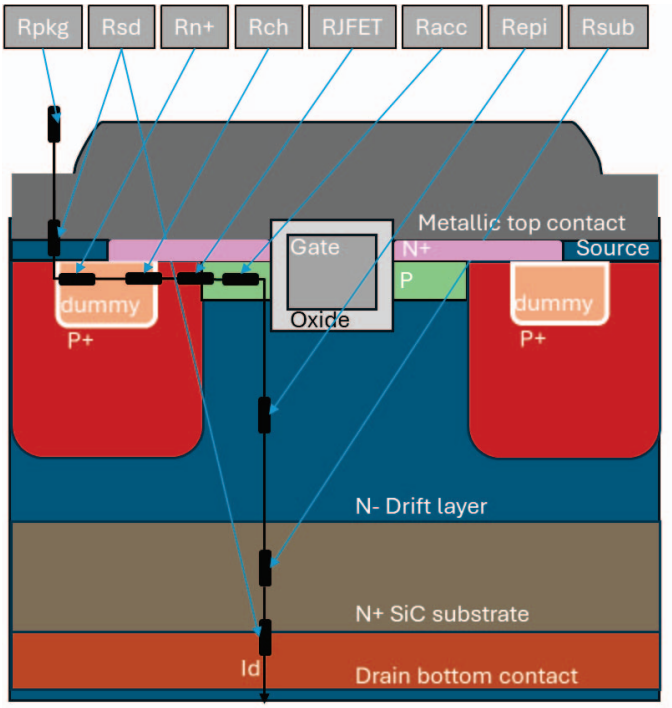

Fig. 1. $R_{\text{DS(on)}}$ components in vertical SiC power MOSFET

$$R_{\text{DS(on)}} = R_{\text{pkg}} + R_{\text{sd}} + R_{\text{acc}} + R_{\text{n+}} + R_{\text{ch}} + R_{\text{JFET}} + R_{\text{epi}} + R_{\text{sub}} \tag{1}$$

TABLE I
BREAKDOWN OF $R_{\text{DS(ON)}}$ IN A SIC MOSFET

Resistance	Description
R_{pkg}	Package, wire bonds, contact resistance
R_{sd}	Source/Drain metal/semiconductor interface resistance
R_{acc}	Accumulation region-resistance
$R_{\text{n+}}$	Heavily doped n+ source region
R_{ch}	Channel Resistance
R_{JFET}	JFET region-resistance, between P-well regions
R_{a}	Accumulation region-resistance
R_{epi}	Drift region (epitaxial layer) resistance
R_{sub}	Substrate resistance

[a] The accumulation-resistance R_{a} is sometimes combined with R_{acc}.

This representation can slightly vary for different devices with different fabrication techniques, such as planar or trench gate, type of SiC crystal structure or channel width to length ratio. In this work the vertical, trench, 4H-SiC is analyzed. The use of vertical trenches in the gate structure reduces the $R_{\text{DS(on)}}$ and improves efficiency. Latest generations of these switches take into account gate oxide longevity by keeping the oxide layer further from the blocking voltage energy field. Understanding dielectric breakdown in gate oxides is crucial for predicting the reliability of semiconductor devices [16]. However, the biggest contributions to the total $R_{\text{DS(on)}}$ is given by (2).

$$R_{\text{DS(on)}} \approx R_{\text{ch}} + R_{\text{acc}} + R_{\text{epi}} \tag{2}$$

Each of these components responds differently to temperature changes. It is known that the $R_{\text{DS(on)}}$ is a Temperature Sensitive Electrical Parameter (TSEP) [17]. In the next subsection we will discuss how the major contributors to the $R_{\text{DS(on)}}$ are temperature dependent.

B. Temperature Dependence of $R_{DS(on)}$ components

The dominant factor influencing $R_{\text{DS(on)}}$ is the R_{epi}, which increases due to the reduction in electron mobility μ_{n} and increase in total impurity density N_{i} at higher temperatures [18]. R_{epi}, given by (3), increases significantly with temperature due to the rise in resistivity ρ_{epi}, which is influenced by carrier mobility degradation and increased phonon scattering. At low temperatures, with the main contribution to carrier scattering coming from ionized impurities, the mobility grows with increasing temperature. In contrast, at high temperatures, where the scattering is affected by phonons, the mobility decreases with increasing temperature [19].

$$R_{\text{epi}} = \frac{\rho_{\text{epi}} L_{\text{epi}}}{A} \tag{3}$$

wherein, L_{epi} is the thickness of the epitaxial layer and A is the cross-sectional area of the current flow. R_{ch}, given by (4), increases with temperature due to the reduction in effective carrier mobility μ_{eff}. The channel resistance depends also on the threshold voltage V_{th} which has a negative temperature coefficient [9].

$$R_{\text{ch}} = \frac{L_{\text{ch}}}{W \mu_{\text{eff}} C_{\text{ox}} (V_{\text{GS}} - V_{\text{th}})} \tag{4}$$

wherein, L_{ch} is the channel length, W is the channel width, C_{ox} is the gate oxide capacitance per unit area and V_{GS} is the gate-to-source voltage. Similar to (4), in (5) the R_{acc} increases with temperature due to reduced carrier mobility μ_{acc}, which decreases with increasing phonon scattering. μ_{eff} is also temperature dependent.

$$R_{\text{acc}} = \frac{L_{\text{acc}}}{W \mu_{\text{acc}} C_{\text{ox}} (V_{\text{GS}} - V_{\text{th}})} \tag{5}$$

wherein, L_{acc} is the accumulation region length.

C. Junction temperature of SiC MOSFET

Junction temperature (T_{j}) is a critical factor in determining both the immediate performance and long-term reliability of SiC MOSFETs. Among the existing TSEPs in literature, the $R_{\text{DS(on)}}$ is load dependent requiring recalibration as the load current changes [20]. The work in [21] proposes a datasheet-driven method for the sensorless estimation of the junction temperature of SiC MOSFETs based on $V_{\text{DS}} > 0V$. Extracting from the datasheet we can plot 3D lookup table for the on-resistance value, while changing the temperature and the drain current.

$R_{\text{DS(on)}}$ of the device increases with T_{j}, typically modeled by a temperature coefficient α, given by (6).

$$R_{\text{DS(on)}}(T) = R_{\text{DS(on)}}(T_0) \times (1 + \alpha(T - T_0)) \tag{6}$$

wherein, $R_{\text{DS(on)}}(T_0)$ is the on-resistance at a reference temperature T_0. At lower operating temperatures up to 100 °C, $R_{\text{DS(on)}}$ increases almost linearly with respect to T_{j} for most SiC power MOSFETs, however, at higher temperatures 100 °C to 175 °C, the increase becomes more pronounced and nonlinear, partially due to the saturation of carrier mobility reduction [22]. This correlation depends primarily on the structure of the device, doping concentration, and manufacturing technology.

Self-heating in (7) is another crucial aspect which creates a temperature rise ΔT [23],

$$\Delta T = P \times R_{\text{th}} \tag{7}$$

wherein, R_{th} is the thermal resistance and P device's power dissipation. This self-heating effect creates a feedback loop—elevated T_{j} further increases $R_{\text{DS(on)}}$, which in turn can lead to even higher temperatures under load. Over time, repetitive thermal cycles and sustained high temperatures accelerate aging, introducing defects and modifying the properties of the material that further enhance the increase in $R_{\text{DS(on)}}$ [24]. Therefore, lookup tables for each Vgs taking aging into account can be developed to determine the junction temperature. The devices under test (DUT) are model IMW65R107M1H SiC MOSFET described in Section II.

II. Methodology

This section describes the experimental setup built to investigate the identified possibility of using the junction temperature as a health monitoring parameter. Few measurement procedures are presented, with variation of parameters. The designed circuit is presented in Figure 2.

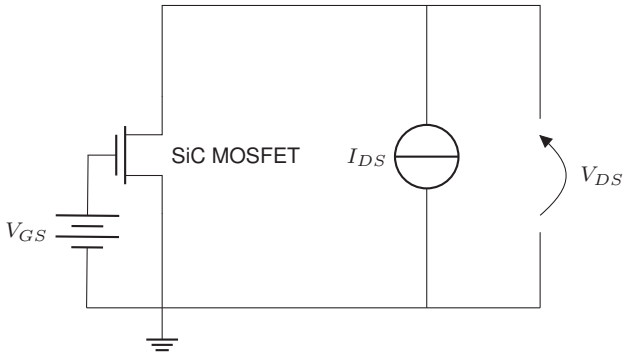

Fig. 2. Rdson measurement, with 2 SMU, four wire method for Drain-Source

This experiment combines the standard approach for precise electrical control with systematic thermal variation to characterize the SiC MOSFET's performance. It is important to mention that 4-wire configuration is used for the Drain-Source voltage sense and current force to reduce the conduit losses. The dual-SMU configuration enables accurate setting of V_{GS} and measurement of the drain voltage during a current sweep, facilitating the calculation of $R_{\text{DS(on)}}$ across a range of operating conditions. By mounting the device on a hotplate and varying the temperature from 25°C to 175°C, the experimental setup provides comprehensive insight into the effects of both gate voltage and thermal stress on the device behavior. The custom made PCB and the hotplate are given in Figure 3. Each different sample is mounted using the same thickness of thermal paste for better thermal contact and fixed with thermal resistant cable ties.

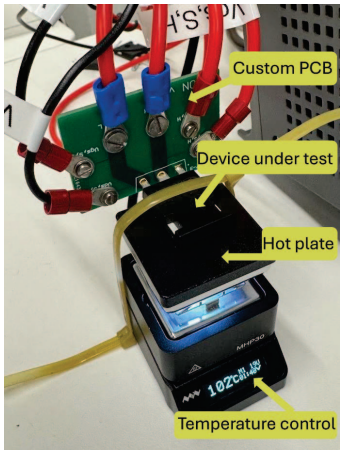

Fig. 3. SiC MOSFET mounted on PCB and temperature control

The resulting data not only confirm the expected performance at room temperature but also reveal the critical influence of elevated temperatures on device degradation and self-heating phenomena. The output characteristics is replicated for a new device at given temperatures and it matches closely the datasheet values. The measurements are done for a range of gate voltages: 8, 10, 12, 15, 18, and 20V. This step ensures that the MOSFET is appropriately biased during the current sweep. This multi-point approach allows for the evaluation of how different V_{GS} levels influence the device's conduction characteristics and also the internal $R_{\text{DS(on)}}$. If we take a reference point from the datasheet given from the manufacturer at $V_{\text{GS}} = 18V$,$I_{\text{D}} = 8,9A$ and $T_{\text{j}} = 25°C$, the resistance is $107\,\text{m}\Omega$, with maximum being $142\,\text{m}\Omega$. Our setup gives $113,5\,\text{m}\Omega$ average and overal great overlap with datasheet values. The output characteristics at room temperature are given at Figure 4. To study the impact of temperature on device performance, we clamped the same switch onto a hotplate equipped with a temperature control unit. The temperature is varied by few discrete values, starting from a room temperature baseline of 25°C and increasing to 100°C, 125°C, 150°C and 175°C. The switch is left at this temperature long enough to ensure that the junction temperature is very close to the value of the temperature controlled hotplate. This thermal arrangement ensures uniform heating of the device, thereby enabling accurate measurement of temperature-dependent parameters such as $R_{\text{DS(on)}}$. At each temperature, the above steps: gate voltage change, I_D sweep and V_D measurement are repeated. All data are logged through software that provides a user-friendly interface to automate measurement sequences and ensure reproducibility. The acquired data, including V_D, I_D, and the derived data $R_{\text{DS(on)}}$, are analyzed to observe the

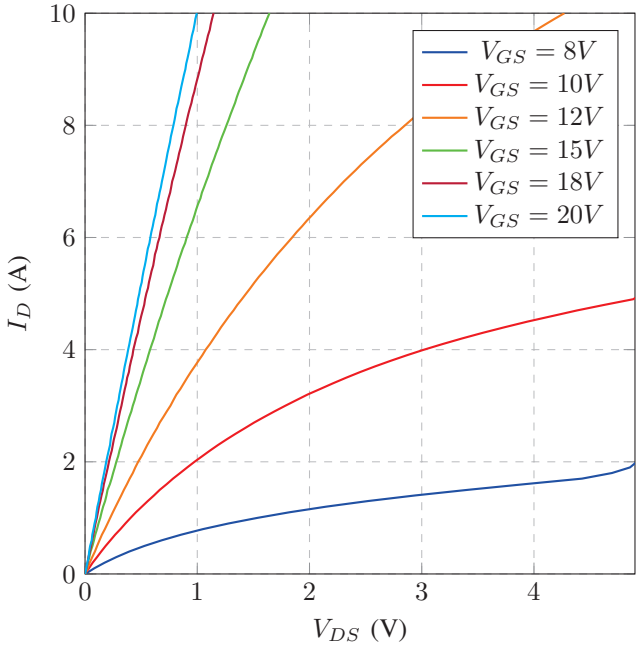

Fig. 4. Output Characteristics for $T_j = 25°C$ with different V_{GS} values

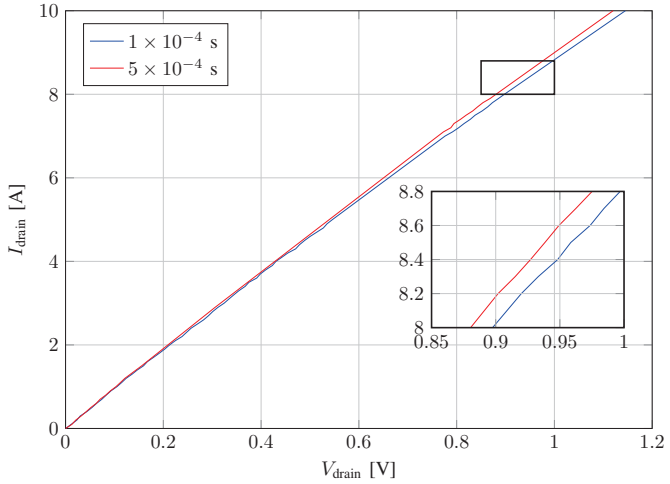

Fig. 5. Drain current versus drain voltage slope, indicating the influence of different pulse widths for same device, showing quantifiable self-heating effects

variation in the output characteristics with temperature and gate voltage. A typical analysis involves plotting $R_{\text{DS(on)}}$ as a function of temperature for each gate voltage setting. The plots reveal that the output characteristics at room temperature match the datasheet values and clearly illustrate the influence of varying V_{GS} on the current conduction. Furthermore, the temperature-dependent plots highlight the self-heating effects and how thermal stress accelerates degradation over time. One of these examples is given in Figure 5, for $V_{\text{GS}} = 18V$ and $T_{\text{j}} = 25°C$, where varying the pulse duration for Id shows a self-heating effect and a change in the on-resistance value for same drain current and temperature rating. It's very important to mention that both of these pulses are lower than 1ms and that transient thermal impedance does not change drastically.

In summary, this methodology combines precise electrical control with systematic thermal variation to characterize the SiC MOSFET's performance. The dual-SMU configuration enables accurate setting of V_{GS} and measurement of the drain voltage during a current sweep, facilitating the calculation of $R_{\text{DS(on)}}$ across a range of operating conditions. By mounting the device on a hotplate and varying the temperature from 25°C to 175°C, the experimental setup provides comprehensive insight into the effects of both gate voltage and thermal stress on device behavior. The resulting data not only confirm the expected performance at room temperature but also during elevated temperatures.To be able to predict the $R_{\text{DS(on)}}$ at certain T_{j} we use the Least Squares Method, which minimizes the sum of squared errors and gives the dependence in (8).

$$R_{DS(on)}(T_j) = -8.392 \times 10^{-11} T_j^4 - 6.469 \times 10^{-8} T_j^3 + 3.463 \times 10^{-5} T_j^2 - 1.590 \times 10^{-3} T_j + 1.019 \quad (8)$$

For future experiments, we plan to decrease the stepsize and also include temperatures below 25 degrees. The fitted data and the measurement points are given in Figure 6.

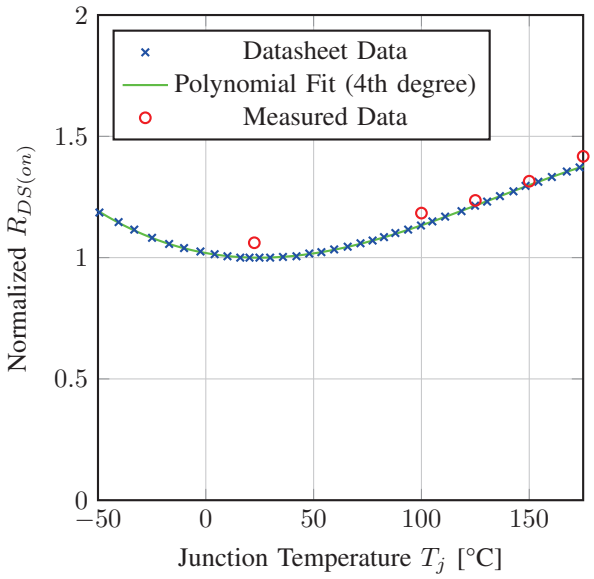

Fig. 6. Normalized $R_{DS(on)}$ vs Junction Temperature T_j, where we can see that the measurement data matches closely to fitted datasheet values

III. Discussion and Analysis

This section discuss the experimental results obtained from T_{j} profiling of SiC MOSFETs. The analysis primarily focuses on the extraction of $R_{DS(on)}$ values at different gate voltages V_{GS} and T_j, highlighting their significance in predicting device reliability and potential degradation trends. However, it is necessary to determine a calibration curve and measure at high temperature and higher I_D to obtain better sensitivity. It was observed that the DUTs sample size should be large

enough, as different devices show different values, despite being from the same fabrication batch, which can compromise the fitting models, if they are based on too few samples. The resulting output characteristics confirm the expected MOSFET behavior, showing increased current conduction at higher gate voltages. These results align well with the manufacturer's datasheet values, validating the accuracy of the experimental setup. We plan to use this setup to monitor health and quantify levels of deterioration in future work, using data fitting and predictive data models. The difference between the datasheet values and our experimental results is less than 5% for each temperature and current rating. To minimize and analyze the self-heating effect, the pulse duration of the drain current was carefully controlled and in the future larger data will be collected to make reference to JEDEC 24-3 [25], where the magnitude for the heating current I_M is not specified. Another point of investigation can be t_H, which is recommended to be 10ms for TO-39 and TO-3 packages, but not for TO-247. The initial experiments minimize the influence of temperature on $R_{DS(on)}$, which is crucial for reliable temperature-dependent characterization.

A. Implications for Aging and Reliability Prediction

Although direct aging experiments were not performed in this study, the observed temperature dependence of $R_{DS(on)}$ provides a strong foundation for predicting long-term degradation. Some recent publications [26]–[28] clearly show this dependency, but do not take the pulse width of the drain current into account. Over time, thermal cycling or electrical stress introduces defects in the MOSFET channel and drift region, leading to a permanent increase in $R_{DS(on)}$. The magnitude of this increase is an aging precursor. By establishing a baseline relationship between temperature and resistance in unused devices, future aging studies can compare post-stress measurements to these initial results to quantify degradation. The standardized $R_{DS(on)}$ values obtained from this study can serve as a reference for real-time health monitoring in power electronic applications as well. By continuously monitoring deviations in $R_{DS(on)}$ under known operating conditions, early signs of device wear can be detected, allowing predictive maintenance strategies.

B. Summary of Findings

The experimental results confirm that:

- The output characteristics at room temperature align reasonably well with the datasheet values, ensuring measurement accuracy.
- $R_{\mathrm{DS(on)}}$ exhibits a strong temperature dependence, increasing with elevated junction temperature.
- Controlled pulse duration is essential for minimizing self-heating effects and isolating true temperature-dependent behavior. The possibility arrises to systematically quantify the correlation between pulse drain current duration and self-heating effects.
- These findings provide valuable insights for reliability assessment, as future comparisons with aged devices can reveal degradation trends.

Overall, the methodology and results presented here establish a foundation for future investigations into the aging mechanisms of SiC MOSFETs and their implications for long-term reliability.

IV. Conclusion

This paper shows the importance of precise junction temperature profiling in evaluating the health of SiC MOSFETs. The experimental results demonstrate a strong correlation between the temperature variations and changes in the device's electrical characteristics. The increase in $R_{DS(on)}$ with temperature emphasizes the importance of thermal management in inverters, especially in the application of high-power electric vehicles, where excessive heating can lead to efficiency losses and accelerated aging. Controlled duration of the drain current pulse ensured that self-heating effects were minimized and taken into account, allowing for accurate extraction of temperature-dependent parameters. Despite following the recommended values, we can see a shift in Figure 6. The measured characteristics at room temperature closely matched the datasheet specifications, validating the experimental setup that will be used to get more data. This conclusion provides a baseline for future studies focusing on long-term reliability and degradation analysis. The results contribute to the development of predictive maintenance strategies for SiC power electronics. By continuously monitoring $R_{DS(on)}$ during operation, early wear indicators can be identified, allowing proactive measures to extend device lifespan. Further research will investigate accelerated aging tests and real-time monitoring techniques to refine predictive models for industrial applications within SiC MOSFETs for automotive high-power application.

Future work may also involve integrating advanced data analysis methods, such as machine learning or artificial intelligence algorithms, to enhance predictive accuracy. Using historical performance trends, it may be possible to develop more robust lifetime estimation models, optimizing reliability and efficiency in power semiconductor applications.

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