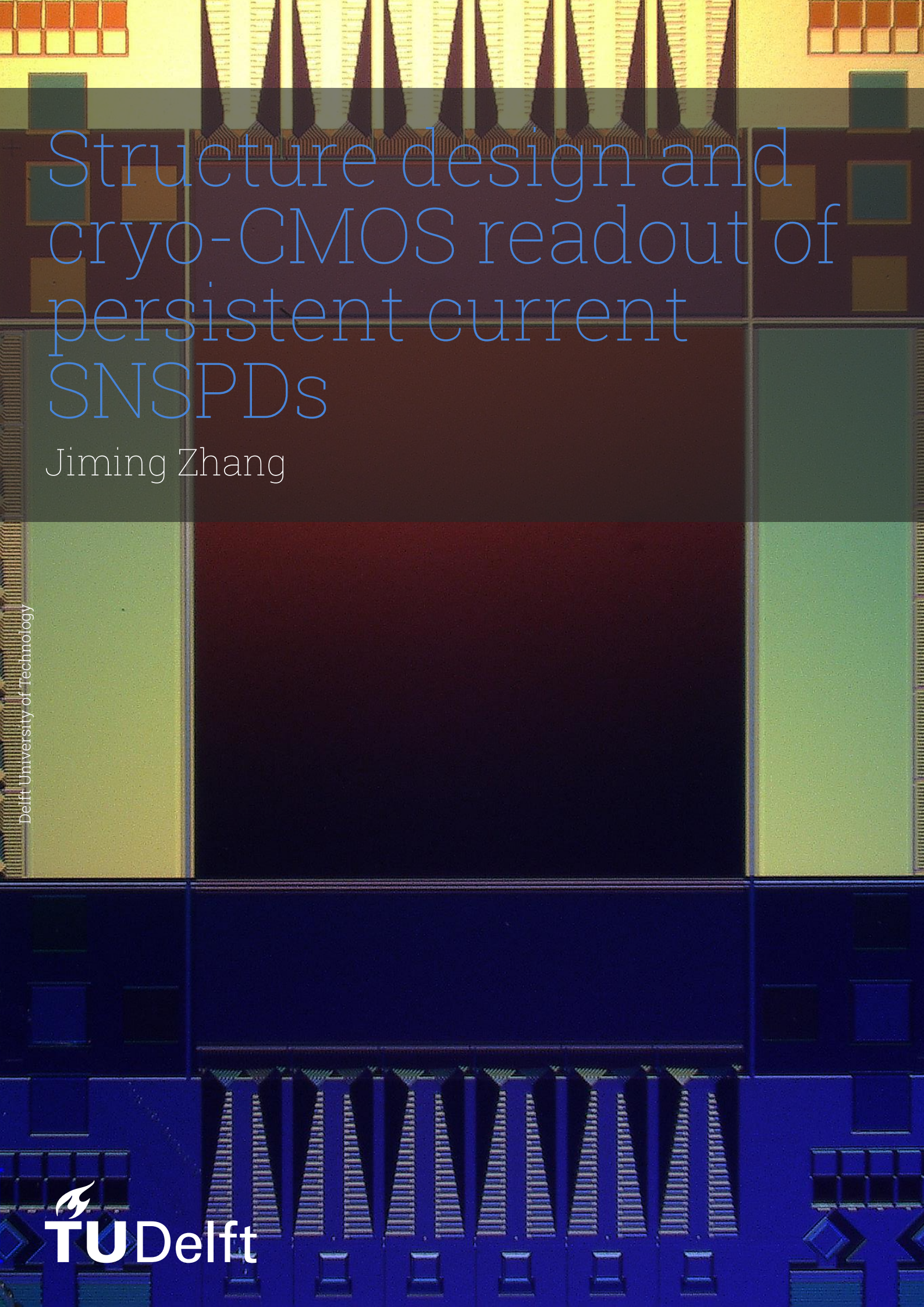


Structure design and cryo-CMOS readout of persistent current SNSPDs

Jiming Zhang

Delft University of Technology

TU Delft

Structure design and cryo-CMOS readout of persistent current SNSPDs

by

Jiming Zhang

Student Name	Student Number
Jiming Zhang	5696453

Instructor:	Dr. Fabio Sebastiano
Teaching Assistant:	Luc Enthoven
Project Duration:	09, 2023 - 08, 2024
Faculty:	Faculty of Electrical Engineering, Mathematics & Computer Science, Delft
Thesis Committee:	Dr. F. Sebastiano, TU Delft, supervisor
	Dr. T. Costa, TU Delft
	Dr. Esmaeil Zadeh, TU Delft

Cover:	Ultralow-noise Superconducting Camera for Exoplanet Searches by NASA
Style:	TU Delft Report Style, with modifications by Daan Zwaneveld

TU Delft

Abstract

Superconducting Nanowire Single-Photon Detectors (SNSPDs) are characterized by high detection efficiency, high counting rates, low dark count rates, and minimal timing jitter, making them indispensable in fields such as quantum information science, free-space optical communication, and fundamental physics. Conventional SNSPD architectures, however, require the superconducting nanowires to be biased with a constant current and necessitate continuously operating readout circuits to capture the output signals. This leads to efficiency issues under prolonged low-load conditions and poses significant challenges for the development of multi-pixel SNSPD arrays. This thesis begins by examining conventional SNSPD designs, critically analyzing the shortcomings of previous active quenching methods, and proposing improvements to the digital sub-circuit. The introduction of a differential amplifier in place of the original single-ended main amplifier successfully addresses output offset issues, pushing the count rate beyond 50MHz. Moreover, this work introduces a novel persistent current SNSPD that leverages the memory characteristic of persistent currents in a superconducting loop, enabling photon detection without the continuous drive from interface circuits, and allowing for unified readout. A design methodology for SNSPD loops is proposed based on various simulation techniques and the physical and electrical characteristics of SNSPDs. This methodology was applied to design multiple samples tailored to different loop coupling scenarios. Additionally, the thesis outlines the biasing and readout logic for the persistent current SNSPD, ensuring independent photon detection without external circuit interference. In the demonstration system, the energy consumption per detection event was measured at 7pJ, with the average power consumption dependent on the frequency of rebias operations.

Acknowledgements

I would like to express my sincere gratitude to my supervisor, Dr. Fabio Sebastiano, for introducing me to this fascinating topic that allowed me to explore a new field. His guidance and suggestions during our weekly discussions have been invaluable. I am especially thankful to my daily supervisor, Luc Enthoven, for his patient support throughout the past year. He has been an outstanding advisor and provided me with immense help. I would also like to extend my thanks to the members of the CoolGroup for their assistance and for making the work environment enjoyable. Finally, I am deeply grateful to my family for their constant encouragement and motivation.

Contents

1

Introduction

1.1. Photon Detectors

A photon detector is a crucial device designed to detect and measure photons, the fundamental units of light. The operation of photon detectors typically involves the conversion of incident photons into an electrical signal that can be quantitatively analyzed. This process relies on the interaction between photons and the detector material, where the energy from the photons is absorbed and subsequently generates a measurable response. A single photon detector (SPD) represents a specialized category of photon detectors, distinguished by its capability to detect individual photons with high sensitivity. Their design and optimization are key to enhancing sensitivity and time resolution, reducing noise and dark counts, and improving overall performance in the detection of photons.

In recent years, SPD technology has emerged as a critical tool across many cutting-edge scientific domains. As research deepens and technology advances, the types and applications of photon detectors continue to expand. These detectors play a vital role not only in fundamental scientific research but also in a wide range of applications, including quantum communication, quantum computing, deep-space communication, astrophotonic detection, fluorescence lifetime imaging, etc.

To meet the diverse requirements across various applications, several types of photon sensors have been developed, including Single-Photon Avalanche Diodes (SPADs), transition edge sensors (TESs), microwave kinetic inductance detectors (MKIDs), and superconducting nanowire single-photon detectors (SNSPDs). Among these, SPADs and SNSPDs have garnered significant attention due to their exceptional performance. When a SPAD is biased above its breakdown voltage, an incident photon would creates an electron-hole pair, and triggers a self-sustaining avalanche, producing a measurable current pulse detected by readout circuits. SNSPDs, as the name suggests, rely on superconducting nanowires to detect photons. When a single photon is absorbed by the superconducting nanowire close to its switching current, it disrupts the superconducting state, creating a localized resistance that produces a detectable electrical signal. Their exceptionally high count rates, precise timing accuracy, and low dark count rates make them outstanding in cutting-edge applications.

1.2. Challenges for Multi-pixel Detectors and Motivation

However, when attempting to array these sensors, SNSPDs face limitations due to the readout circuit, especially when compared to the more mature design of SPAD arrays. The most straightforward approach is to add a dedicated readout circuit for each pixel, but this leads to unacceptable wiring complexity and power consumption. Various large-scale readout schemes for SNSPD arrays have been proposed, such as row-column multiplexing [1], pulse amplitude multiplexing [2], time domain multiplexing [3][4], etc.

Here, we propose a novel SNSPD architecture, which we refer to as the persistent current SNSPD. This structure introduces a memory characteristic not present in conventional SNSPDs, eliminating the need for continuous bias current. The readout of the SNSPD is integrated with the biasing process, enabling

a discrete-time readout design. The sensor's biasing and readout occur in fixed cycles, allowing the SNSPD to independently detect photons without continuous connection to the interface circuitry during each cycle. This theoretically enables a single set of biasing and readout circuits to alternately control multiple sensors, facilitating unrestricted multi-pixel biasing and readout operations.

1.3. Thesis Object

This thesis aims to model and explore the use of a SNSPD in a persistent current manner, and provide parameters for an initial batch of samples based on its physical characteristics for validating the concept. For this, the project uses the TSMC 40nm process technology to design biasing and readout circuits for the sensor, enabling the successful operation of the system in simulation.

Given that no published work closely resembles the design proposed in this thesis and no physical samples have yet been manufactured, the study will employ various simulation tools to qualitatively and quantitatively analyze the sensor. This approach will help assess the sensor's performance and guide its further development. This thesis is conducted in collaboration with Single Quantum, a company specializing in SNSPDs.

1.4. Thesis Outline

This thesis will begin with Chapter 2, which covers the operational principles of traditional SNSPDs and the design of their readout circuits. One specific design example will be analyzed in detail to evaluate its performance and suggest potential improvements.

Chapter 3 will explore the structure and operational principles of the persistent current SNSPD. It will utilize various simulation tools to thoroughly investigate the electrical and physical characteristics of the sensor from multiple perspectives. This analysis will yield relevant parameters and establish a model to describe the sensor's behavior, leading to the formulation of a design approach for the sensor and recommendations for sample fabrication.

Chapter 4 will integrate the findings from Chapter 3 to design the biasing and readout interface circuits. These circuits will be used to enable the initial operation of the SNSPD system, followed by performance and power consumption analyses.

2

Traditional SNSPD Mechanisms and Readout Design

This chapter first introduces the background information on traditional SNSPD devices and reviews different types of readout techniques. Then a previously designed active quenching readout system is analyzed in detail, and suggestions for improvement are proposed. Part of the content of this chapter is the result of the work carried out for the course ET4399.

2.1. SNSPD Structures and Detection Mechanism

The typical implementation of SNSPD is a superconductor thin film nanowire pattern deposited by nanofabrication process, as shown in figure 2.1. The nanowire usually has a thickness of around $5\,\mathrm{nm}$ to $10\,\mathrm{nm}$, a width of $50\,\mathrm{nm}$ to $100\,\mathrm{nm}$, and forms a meandering structure for better optical coupling, which is usually called an active area [5].

The SNSPD detection mechanism is shown in figure 2.2, (I) The superconducting nanowire is biased with a bias current I_b in the ready-to-detect state. I_b is close to but smaller than the switching current I_{sw}, which is defined as the maximum current the nanowire can conduct while remaining superconductive. (II) When a photon hits the superconductor, its carried energy may break hundreds of Cooper pairs, generate a hotspot without superconductivity in the nanowire, and repel the current to the path around the hotspot. (III) Since the current is repelled and exceeds the switching current density of the nanowire, the hotspot will expand and continue to be enlarged by the Joule heat generated by the current and large resistivity in the hotspot. Thermal energy also dissipates through the substrate during this step.

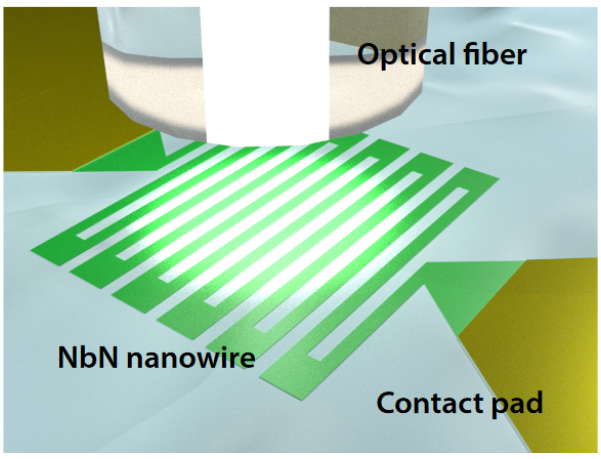


Figure 2.1: Typical SNSPD configuration[6]

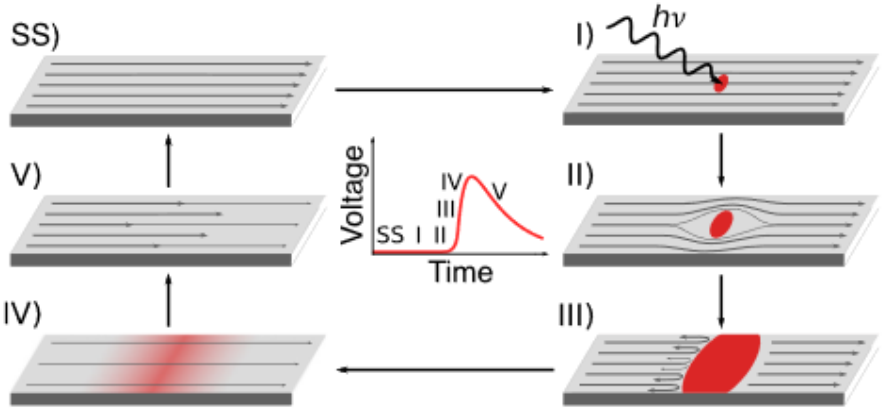


Figure 2.2: SNSPD detection mechanism [5]

(IV) While the hotspot is expanding, the current in the nanowire (I_d) will also be suppressed lower and lower (in traditional readout with a load resistor) until the heat generation power is below the heat dissipation power from the SNSPD to the substrate. At this moment, the hotspot will cool down, and (V) the current will return to the original level. Given the elongated shape of SNSPD devices, usually, they have a large kinetic inductance[1]. This results in a large time constant when combined with the load resistor, leading to a slower voltage decay on the output compared to the faster rising. As a result, the voltage across the nanowire will provide an asymmetric pulse signal [5][7]. To represent the hotspot resistance and kinetic inductance in the circuit, the SNSPD can be modeled as a series combination of a variable resistor R_n and an inductor L_k, as shown in figure 2.3.

2.2. Performance and State of the Art

The performance of the SNSPD system is determined by both the SNSPD device and the readout circuit, it could be judged by the following parameters, including system detect efficiency, dark count rate, afterpulsing, recovery time, latch, and jitter.[8]

System detection efficiency (SDE): As one of the most important parameters, SDE indicates the effectivity of photon detection for the SNSPD system, including all the losses and non-idealities.

$$\eta_{SDE} = \eta_{coupling} \times \eta_{absorption} \times \eta_{intrinsic}$$

$\eta_{coupling}$ is the optical coupling efficiency through the active area of the SNSPD, depending on the structure and optical characteristic of the nanowire thin firm and the substrate. $\eta_{absorption}$ is the absorption efficiency of the photon to the nanowire, $\eta_{intrinsic}$ is the triggering efficiency of the absorbed photons that can generate a detectable electric signal, highly depending on the superconducting quality, geometric design and fabrication precision of the superconducting nanowire. It is also affected by the operation temperature and bias current, usually a high bias current (closer to the switching current) would make the sensor more sensitive [7, 9]. As one of the photon detectors with the highest detection efficiency, SDE of SNSPD can be up to 90% , as shown in table 2.1.

Dark count rate (DCR): The DCR indicates the number of times the detector is triggered without photon incident per unit time. Dark count includes intrinsic dark count and background dark count, which the intrinsic dark count is related to the spontaneous vortex motion in the nanowire, and the background dark count is caused by black body radiation. A lower bias current can effectively reduce the DCR, but also reduce the SDE. We can determine the optimal bias current for a device by identifying the point where the ratio of SDE to DCR is maximized. In 2015, Shibata et al. reported an SNSPD system with an extremely DCR of as low as 1×10^{-4} Hz, achieving a SDE of 1.5% at this minimal DCR [17].

Afterpulsing: After the detector is triggered by one photon, the SNSPD system may output two or even more pulses. The extra pulses cause incorrect triggering and hence dark counts, while possible

[1] Kinetic inductance in superconductors represents the inertial mass of charge carriers as an equivalent series inductance, which can be considered an intrinsic parasitic inductance.

Table 2.1: High SDE SNSPD

Material/temperature	SDE/jitter	Wavelength (nm)	Reference
WSi/120 mK	93%/150 ps	1550	[10]
NbN/1.8-2.1 K	90%–92%/79 ps	1550	[11]
NbTiN/2.5 K	92%/14.8 ps	1310	[12]
MoSi/700 mK	95%/unknown	1520–1550	[13]
MoSi/700 mK	98%/unknown	1550	[14]
NbN/800 mK–2.1 K	95%–98%/65.8–106 ps	1530–1630	[15]
NbTiN/2.5–2.8 K	94%–99.5%/15.1 ps	1290–1500	[16]

physical mechanisms causing afterpulsing are not fully understood yet. The back action of the readout circuit could be a possible reason [18][19]. Oscillations in the bias current I_b or other electrical effects can cause additional pulsing in the readout circuitry.

Recovery time: The recovery time ($t_{recover}$) indicates the time required for the SNSPD system to return the output voltage to the original level. After the SNSPD is triggered, the output voltage cannot immediately be reduced, because the large kinetic inductance (L_k) and the load resistance of the readout circuit will generate a large electrical time constant $\tau_e = L_k/R_L$. **Count Rate** is the counting frequency of the SNSPD system. The rising time is usually much smaller than falling, so the maximum count rate fits: $CR_{max} \leq 1/t_{recover}$. A large input resistance of the readout circuit will decrease the recovery time. Usually, the load resistor would be set at 50 ohms.

Latching: Although a large load resistor in the readout circuit can reduce the recovery time by making τ_e small, increasing R_L too much can make τ_e smaller than the thermal time constant τ_h, which describes the rate of heat dissipation from the nanowire to the substrate, meaning that the thermal energy cannot be fully dissipated. Once the hotspot resistance decreases, the current increases and eventually reaches a steady state where the Joule heating power equals the dissipation power. Consequently, the output voltage latches at a high level.

Jitter: Jitter in the SNSPD system indicates the time uncertainty of the photon arrival time, which can be described by the full width at half maximum (FWHM) of the distribution. The sources of jitter include the intrinsic jitter of the SNSPD, jitter from the optical system, and jitter from the electrical system. In conventional readout systems, the output signal of the SNSPD is amplified and fed into a comparator. When the amplified pulse reaches the comparator's threshold, the triggered event is recorded. To reduce jitter, in addition to lowering the input noise of the main amplifier, increasing the slope of the signal's rising edge is also effective. A steeper slope translates the same noise-induced uncertainty in the comparator voltage into a smaller time jitter. This steeper slope can be achieved by reducing the input capacitance of the amplifier or by using a faster amplifier. Korzh et al. have demonstrated an SNSPD system with jitter less than 3 ps [20].

2.3. Basic Structure of SNSPD Readout

In a basic readout system, when the sensor is triggered, the bias current flows through the load resistor, generating a pulse (e.g., approximately $1\,\mathrm{mV}$ for a 20 µA bias current with a $50\,\Omega$ resistor). This pulse is then amplified and sent to a comparator, which determines whether an event has occurred. The timing information from the comparator's 1-bit output signal is digitized by a Time-to-Digital Converter (TDC). The section preceding the TDC needs to trade-off between latching, signal amplitude, and jitter performance according to the output characteristic of the SNSPD. For readouts illustrated in figure 2.3, the load R_L is either DC or AC coupled to the SNSPD to shunt the current while the hotspot is generated. In this case, the output signal amplitude depends on $I_L \times R_L$, and the recovery time is the time constant $\tau_e = L_k/R_L$. Given that a larger load resistor provides a smaller time constant but also increases the risk of latching, careful attention must be paid to the selection of the load resistor. The AC-coupled uses a bias tee to separate the high-frequency part of the signal and the load resistor here would be the input resistance of the amplifier. Instead of the tradeoff on RL, it has a DC deviation problem since there is no DC path to ground from the SNSPD output node. As a result, when the system operates at a high frequency, the static state voltage will deviate to the negative side to keep the average value at

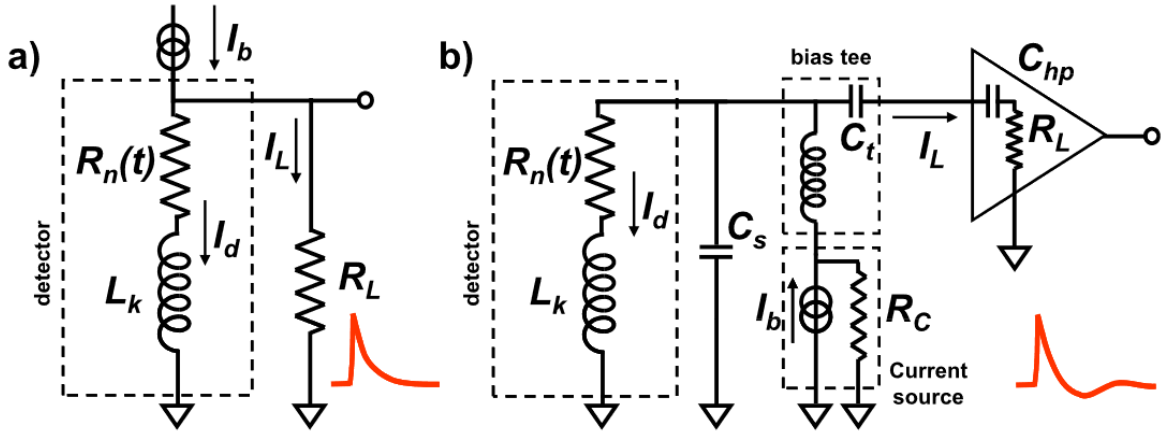


Figure 2.3: Typical SNSPD readout with (a) DC coupled and (b) AC coupled [21]

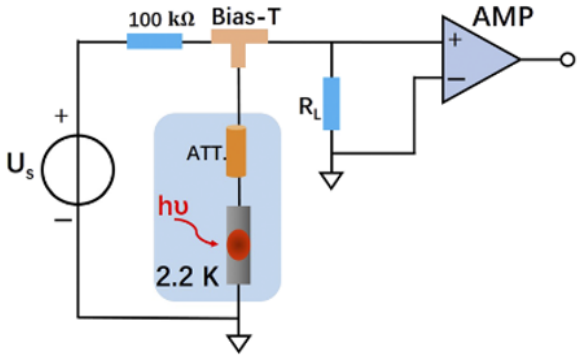


Figure 2.4: SNSPD readout with attenuator [22]

0.

2.4. Readout Improvement

Since most of the problems emerge when people are looking for a higher count rate and lower recovery time (which is one of the parameters that is most affected by the readout circuit), several methods have been proposed. A straightforward improvement is developed by Lv et al. [22] using an attenuator to lower the signal amplitude generated by SNSPD, which is shown in figure 2.4. Therefore, the DC deviation in the AC coupling circuit will also be reduced since a smaller pulse contains less net charge accumulated at the output node. But the amplitude loss would also cause degradation to subsequent signal detection and jitter performance.

Zhao et al. [23] introduced a pulse-shaping technique, shown in figure 2.5. It uses an SMA tee to separate the output signal into two equal parts, one directly goes to the input node of the low noise amplifier, while the other part is reflected by the coaxial cable and adds on the first part with 1ns delay and reverse polarity. In this case, two pulses would mostly canceled at the input node of the low noise amplifier and eliminate the long falling edge, resulting in a lower but much shorter pulse. The coax cable also creates a DC path to the ground, which releases the accumulated charges in the basic AC coupling circuit.

Compared to the attenuator proposal, this design does not sacrifice too much amplitude and pulse rising slope. However, the need for an SMA tee and coaxial cable makes this design cannot be implemented fully on-chip.

In addition to addressing the readout part, researchers also focus on the bias module. A non-DC bias current has been proposed to fundamentally solve the latching issue [23][24]. The Quasi-DC operation

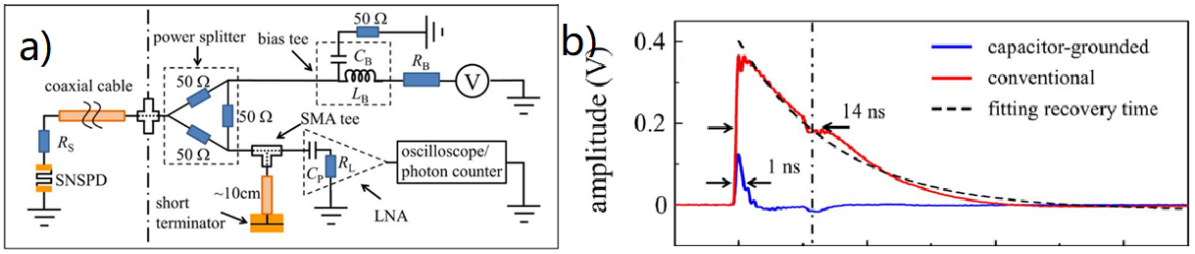


Figure 2.5: (a)pulse shaping readout schematic, (b)output signal compared to the conventional case 2.5

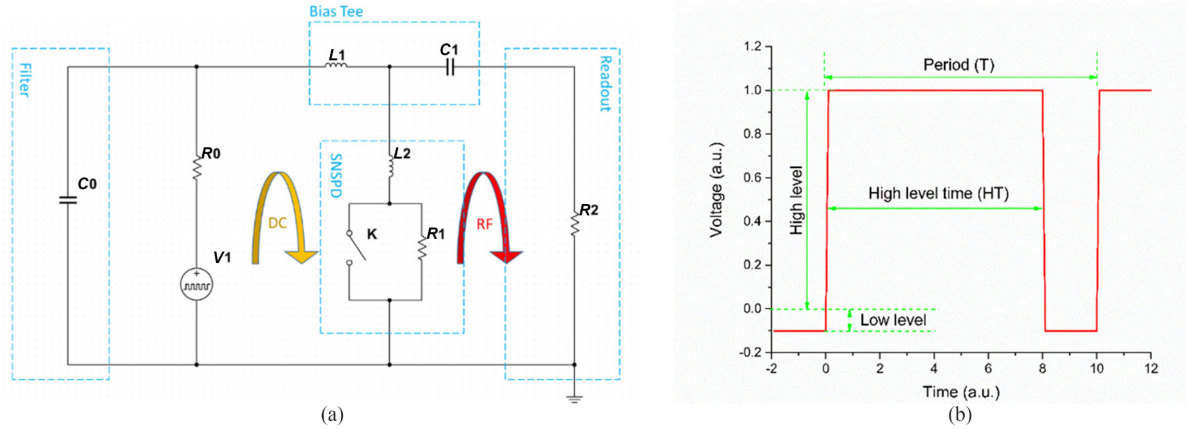


Figure 2.6: SNSPD bias with quasi-DC operation [24]

presented by Zhang et al. only activates the bias source within a limited duty cycle, resetting the SNSPD state when the source is turned off. Consequently, this design eliminates the need to consider the latching problem, and the load resistor is not restricted. The detection frequency largely depends on the quasi-DC operation frequency. However, a significant drawback of this design is that during the resetting period, the detector is not ready for detection, lowering the SDE. If the load resistor is large enough to cause latching, each cycle can detect only one photon. Zhao et al. employ an AC biasing method to reset the SNSPD at the trough of the sine wave, which shares similar advantages and disadvantages with the quasi-DC operation.

2.5. Active Quenching

The active quenching readout can be considered an improved version of non-DC biasing. To maintain characteristics unaffected by latching, the bias current of the SNSPD is adjustable. Instead of resetting periodically, the current source is turned off only after the detector is triggered. Consequently, there will be no periodic ”blind time”. This approach necessitates a feedback path. The first active quenching readout was proposed by Ravindran in 2019 [25]. In their research, the passive quenching (traditional readout) SNSPD with kinetic inductances of $250\,\mathrm{nH}$ and $1\,\mu\mathrm{H}$ achieved count rates of $25\,\mathrm{MHz}$ and $7\,\mathrm{MHz}$, respectively. In contrast, the same devices with the same settings, but with active quenching readout, achieved maximum count rates of $95\,\mathrm{MHz}$ and $12\,\mathrm{MHz}$, respectively, representing a significant improvement.

In this section, the thesis project **Cryo-CMOS Readout of SNSPDs** [8] from Li that implements active quenching will be discussed and analyzed.

2.5.1. System schematic

Figure 2.8 shows the overview schematic of the active quenching readout system proposed by Li. The system schematic contains an SNSPD chip model which is connected to the readout chip by bond wires (represented by the parasitic pad capacitance C_{pad} and wire inductance $L_{bondwire}$). The circuit features a 7-bit current DAC with $0.1\,\mu\mathrm{A}$ least significant bit (LSB) that enables programming the SNSPD current.

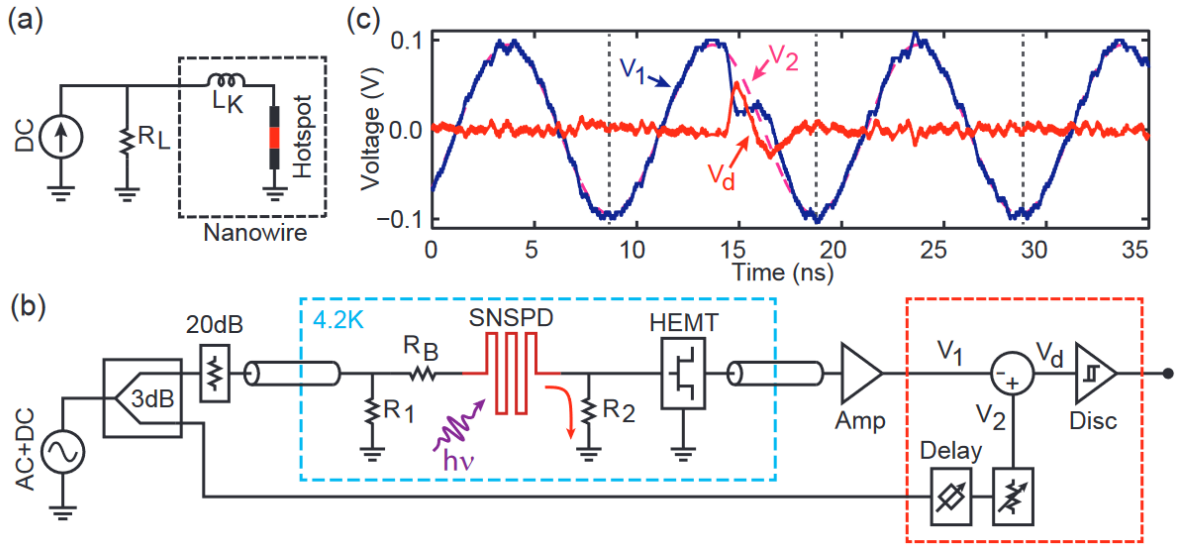


Figure 2.7: SNSPD AC biasing [23]

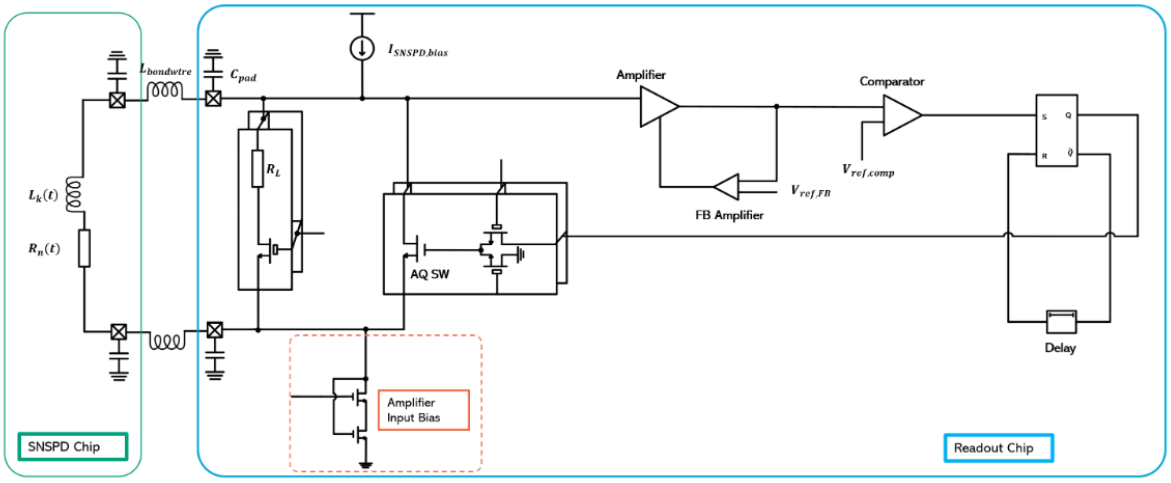


Figure 2.8: Active quenching readout system schematic

A programmable R_L allows comparing the active quenching to the passive quenching operation.

At steady state, all the current from the current source $I_{SNSPD,bias}$ flows into the SNSPD as the AQ (active quenching) switch is open. A diode-connected transistor is used to raise the SNSPD output to the correct biasing level of the main amplifier. When the SNSPD loses superconductivity, a voltage peak is generated that is limited by the hotspot resistance since no load resistor R_L is present to redirect the current [2]. This peak is amplified and causes the comparator to trigger. After the comparator triggers, the result is stored in an SR latch, turning into a one-bit signal that includes time information. An active quenching signal will turn on the AQ switch to short the SNSPD for reset. After a short time set by the delay line in the digital sub-circuit, the SNSPD will get back to the steady state. The AQ switch is turned off, and the whole circuit is returned to its original state.

2.5.2. Circuit Implementation

As mentioned in section 2.2, the bias current of the SNSPD has a significant impact on the SDE and DCR. Since a higher bias current brings a more sensitive sensor, which means higher SDE and DCR, the current level needs to be set at a sweet point that generates a high enough SDE and acceptable DCR. The number is usually around 80% of the switching current.

In this readout circuit, the core component is the main amplifier. To meet the time jitter and dead time requirements, the amplifier must have sufficient bandwidth and low noise for low power consumption. Given that $\sigma_{jitter} \geq \frac{v_{n,rms}}{SR_{t=t_{decision}}}$, the bandwidth and transconductance of the amplifier and comparator can be determined by calculating the slew rate of the amplifier output at the decision time, details of which can be found in [8].

Since the input signal from the SNSPD is a continuous, transient signal and the required gain is approximate ly$A_{amp} \approx 30dB, A_{comp} \approx 17dB$, a cascode amplifier and a five-transistor operational transconductance amplifier (OTA) are used in an open-loop configuration.

To ensure the main amplifier operates within the proper region and has a known output level across PVT and mismatch, a feedback amplifier is added that regulates the open loop amplifier bias current and equates the output of the main amplifier to a reference voltage. Given that negative feedback would reduce the closed-loop gain of the single-ended main amplifier, one potential solution is to use slow feedback to suppress the pulse signal generated by the SNSPD. However, slow feedback would also result in a long recovery time, and the small changes in the feedback signal would accumulate if the SNSPD triggers repeatedly, leading to a significant deviation in the amplifier's operating point as shown in figure 2.9.

Hence, a newly introduced trade-off in this design is to determine the appropriate bandwidth for the feedback amplifier, ensuring it provides sufficient gain for the pulse signal from the SNSPD at a higher frequency while maintaining an acceptable DC deviation. The final closed-loop frequency response of the main amplifier is shown in figure 2.10, with the low gain at low frequency is caused by the feedback suppression.

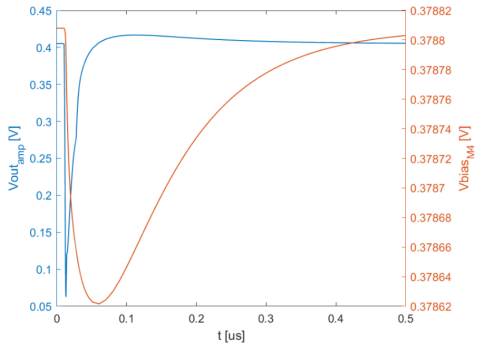
The digital logic needs to generate an active quenching signal for a sufficiently long duration for SNSPD resetting. Therefore, an SR latch with a delay chain connecting the $\sim Q$ and R nodes is used to generate the AQ pulse. When the voltage pulse from the comparator is input to the latch, both S and $\sim Q$ transition from 1 to 0, and Q (the active quenching signal) changes from 0 to 1. After S returns to 1, following the comparator output, Q remains at 1 for t_{delay} due to the delay chain. Once Q returns to 0 and $\sim Q$ returns to 1, the active quenching operation is completed. R will return to 1 after an additional t_{delay}.

Figure 2.11 shows the overall system performance at 20 MHz, table 2.2. When operating at a 20 MHz count rate, the amplifier's DC drift is acceptable and meets the requirements.

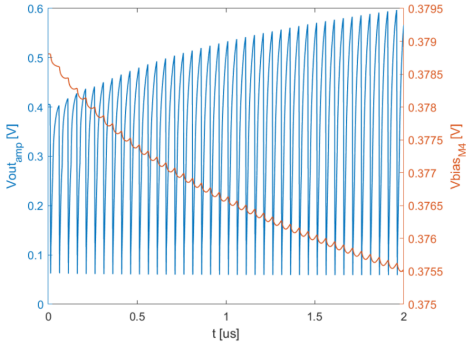
2.5.3. Readout Circuit Defect Analysis

While requirements are met, some improvements for this circuit can be proposed to improve readout-related performances, i.e., jitter and count rate. Jitter can be improved by using an amplifier with a

[2] note that the design features a programmable R_L for testing purposes, and is ideally off when testing with active quenching.



(a) Closer look at the response in a 500 ns period for settling.



(b) The system can not porperly function after several detecting operations.

Figure 2.9: Amplifier output response with the slow feedback

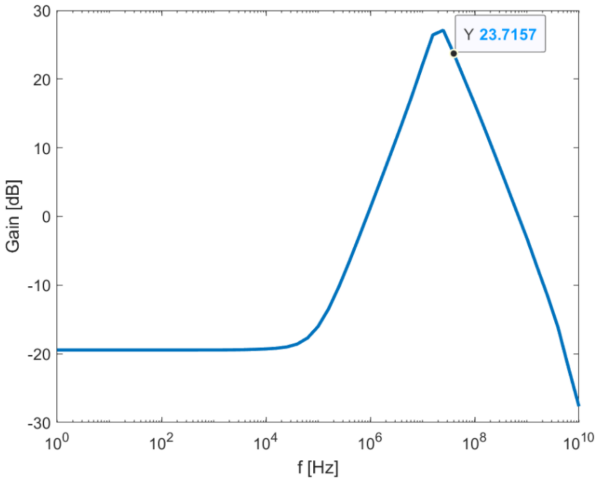


Figure 2.10: Main amplifier closed-loop frequency response

Table 2.2: SNSPD Cryo-CMOS Readout System Performance

Specification	Required	Preference	Simulated
Dead Time	<100 ns	<50 ns	<50 ns
Count Rate	>10 MHz	>20 MHz	>20 MHz
Jitter	<100 ps_{FWHM} (□ 40psrms)		25 psrms
SNSPD bias Current	<20 µA for NbTiN	with ±1 µA tolerance	
Supply Voltage	1.1 V & 2.5 V		
Power Consumption	<100 µW	As low as possible	36.49 µW
Area (for readout electronics)	<1 mm 2		<1 mm 2

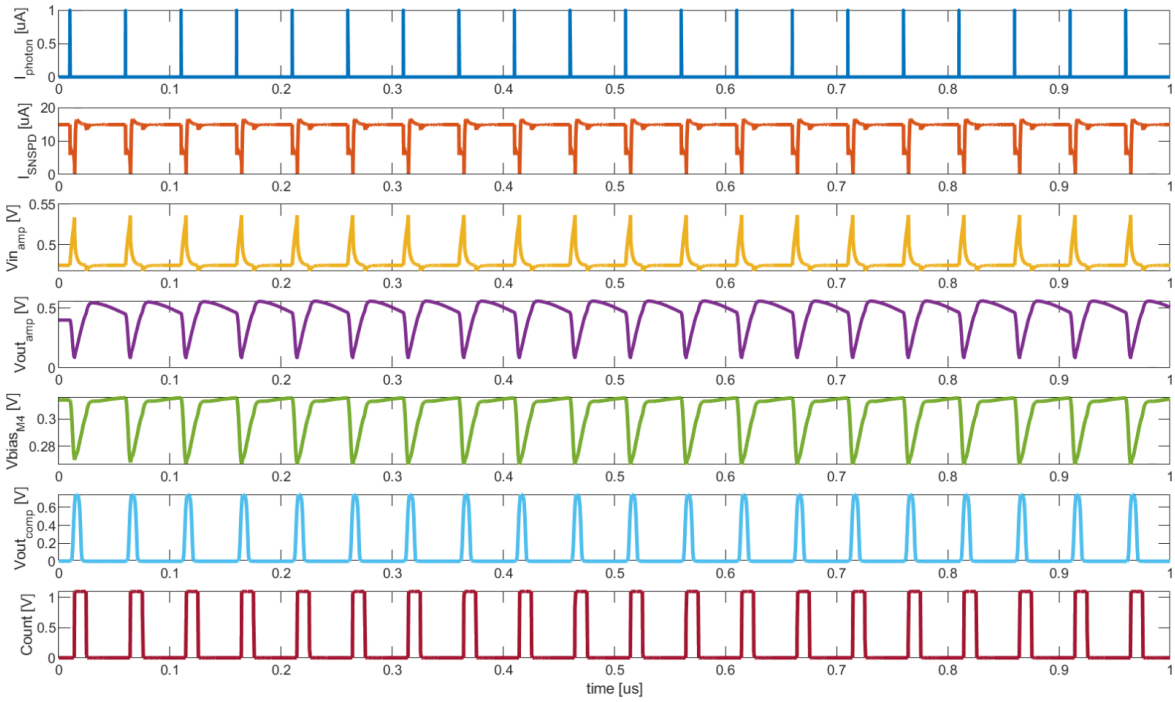


Figure 2.11: Overall system performance. I_{photon} is the incident photon signal that triggers SNSPD; I_{SNSPD} is current in SNSPD; Vin_{amp} is the input of the main amplifier, also the output of SNSPD; $Vout_{amp}$ is the output of the amplifier; $Vbias_{M4}$ is the output of the feedback amplifier; $Vout_{comp}$ is the output of the comparator; Count is the count signal Q, also the active quenching signal

higher slew rate and lower noise, having a trade-off with the power consumption. The 20MHz count rate in this design is relatively low since the structure eliminates the conflicts between long recovery time and latch problem. Figure 2.12 and 2.13 show the system performance comparison at 20MHz and 50MHz. At 50MHz, the drift worsens because the one-way pulse raises the amplifier's average output level. This reduces the feedback voltage before photon detection from 0.38V to 0.24V, possibly pushing the amplifier's current source into a linear region and reducing gain.

From figure 2.12, we can also find that the rising slope of the pulse at $Vout_{amp}$ is reduced from 129 mV/ns to 87 mV/ns (taking 10% changing of the $Vout_{comp}$ as the trigger time), potentially increasing the jitter on the output slope.

Besides, afterpulses are also found in both the main amplifier output and Q in the digital subcircuit. Since the SNSPD model used in the simulation does not have an afterpulse generation mechanism, it must be caused by the readout circuit. As shown in figure 2.13(b), the active quenching signal Q does not hold for t_{delay} before dropping to 0 at the second quench, and the second pulse of Q does not correspond to a pulse at Q. This is because the second flip of the delay line caused by the first quench, mentioned in the last section, is not finished before the second quench is coming. The R is still at 0, which is not ready for the next trigger, and the delay would not take effect.

2.5.4. Readout Circuit Improvement

The issue on the analog side is systematic, as the pulse generated by the SNSPD passes through the DC feedback loop. To separate the pulse from the feedback loop, one possible solution is to build an independent bias sub-circuit. This can be achieved by creating a duplicate of the main amplifier and feedback amplifier for the actual main amplifier, as illustrated in Figure 2.14. However, in this scenario, if any error σ is introduced at the output of the dummy amplifier, the error, after being suppressed by the loop gain of that bias sub-circuit, would be magnified back to σ at the final output. This implies that the accuracy of the bias circuit is entirely dependent on the mismatch between the main and dummy amplifiers. This bias only becomes effective when the inaccuracy caused by mismatch is smaller than that caused by PVT issues in direct biasing.

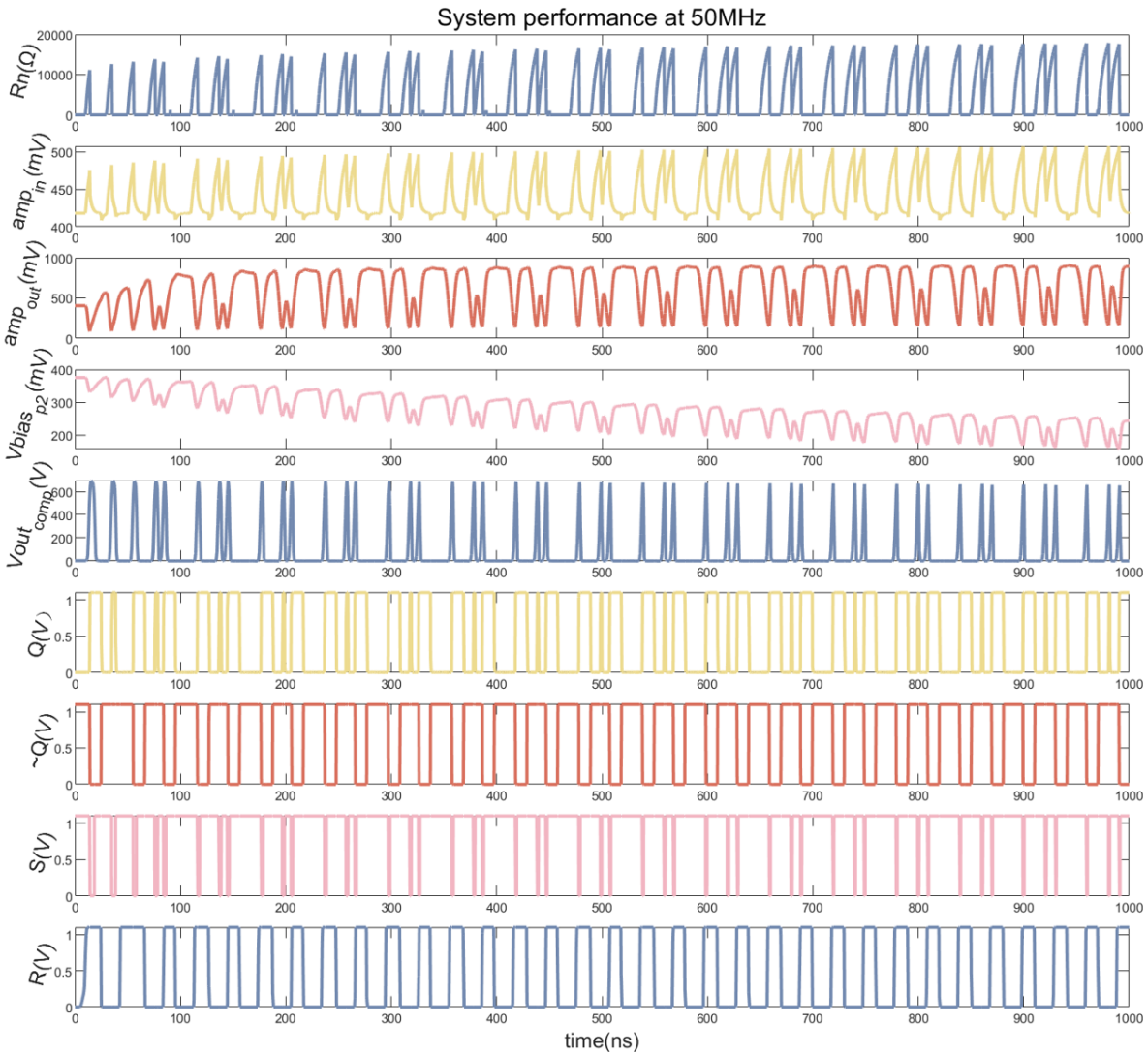


Figure 2.12: System performance at 50MHz

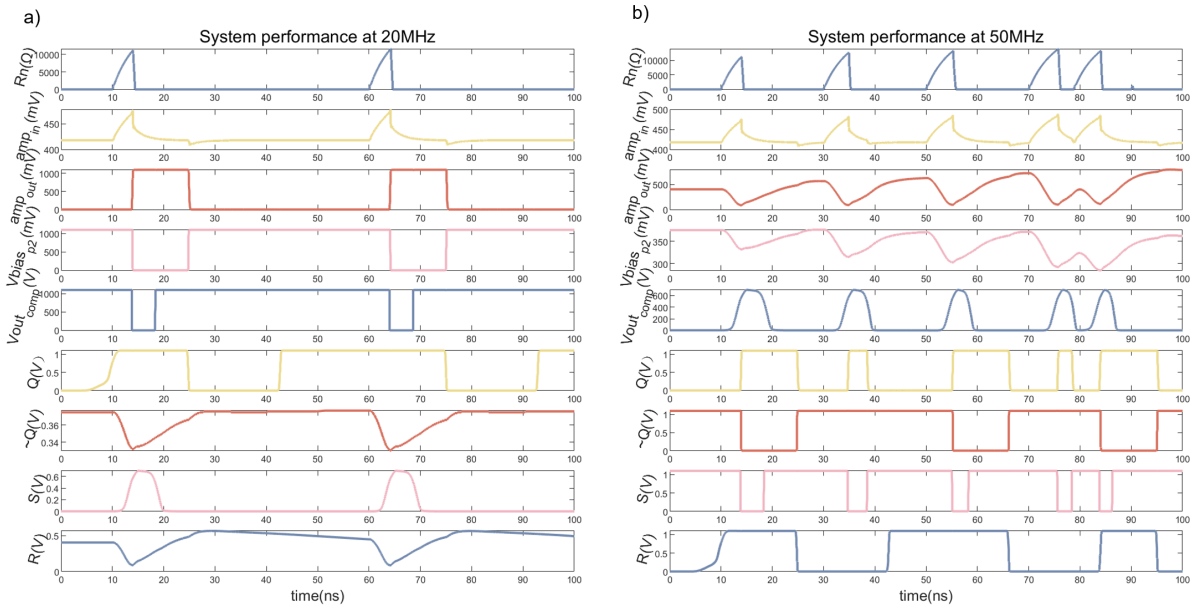


Figure 2.13: System performance at (a)20MHz (zoomed), (b)50MHz (zoomed)

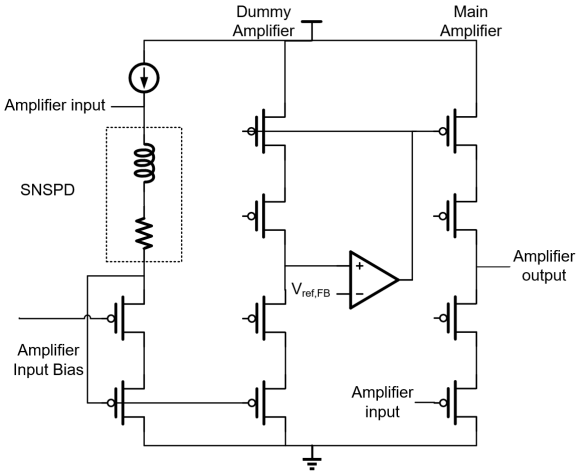


Figure 2.14: Replica bias

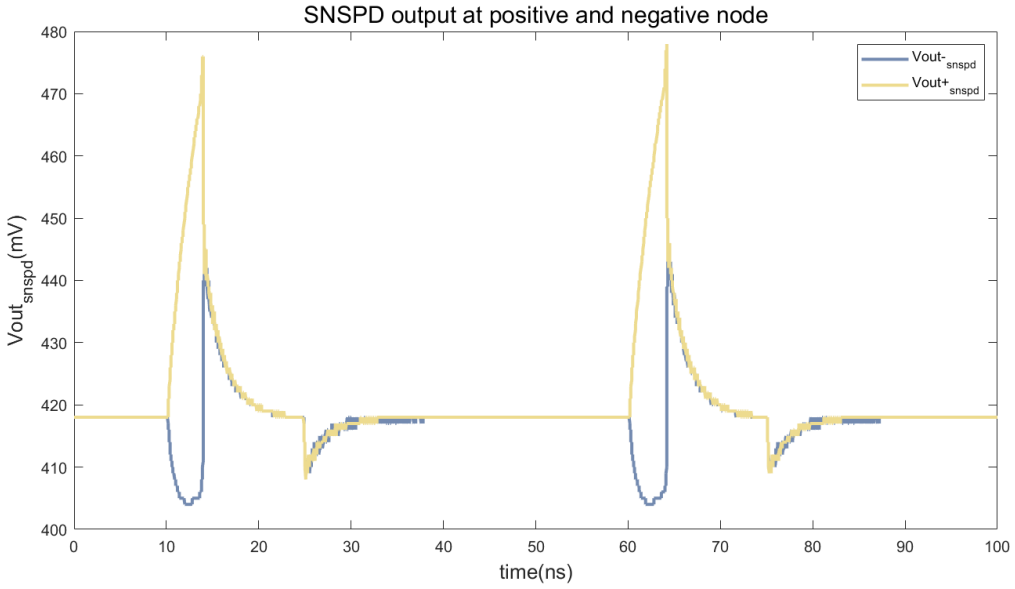


Figure 2.15: SNSPD output at positive and negative node

Another possible solution is to use a differential amplifier. Figure 2.15 provides a detailed view of the voltage on both sides of the SNSPD. Although the negative node connected to the input bias block should remain fixed due to the constant input current, it exhibits considerable fluctuation when pulses are generated. This could provide a larger input signal to the amplifier compared to the single-ended case. Leveraging the characteristic that the common-mode feedback does not contain differential output signals, fast common-mode feedback can be employed to maintain system stability.

As shown in Figure 2.16, a folded cascode amplifier is constructed based on the original design, using similar-size transistors to achieve the same performance. It has a similar bandwidth and slightly lower gain, causing. The common-mode output is directly connected to Vb1 to provide sufficiently fast feedback. Both output nodes are connected to the original comparator. This folded cascode amplifier consumes $59\,\mu\mathrm{W}$, a telescopic structure could be more energy efficiency.

On the digital side, the SR latch could be replaced by a D flip-flop with node D connected with node Q, as shown in figure 2.17. The output from the comparator is connected with the clock node, when every single pulse appears at the CLKin, D and Q would flip from 1 to 0 or 1 to 0 for only one time. An OR gate with a delay line would collect this flip and generate an output holding for t_{delay}. On the digital side, the SR latch can be replaced by a D flip-flop, with the D node connected to the Q node, as shown in Figure 2.17. The output from the comparator is connected to the clock node. With each pulse that appears at the CLKin, D and Q will flip from 1 to 0 or from 0 to 1 for only one cycle. An OR gate with a delay line collects this flip and generates an active quenching signal that holds for t_{delay}.

After applying all the changes, the system performance at 50 MHz is illustrated in Figure 2.18. In this case, the dead time limitation of the system is determined by the active quenching holding time and the comparator recovery time. To further improve the detection frequency, a faster amplifier and comparator are needed.

2.6. Conclusion

This chapter reviewed the operating principles of SNSPDs and various readout circuit designs proposed to enhance the count rate and reduce dead time. A previous work employing active quenching was analyzed in detail, and its issues were identified. Subsequently, an improved delay circuit was implemented to address the ineffective delay problem, and a differential amplifier was used to replace the original main amplifier to resolve output signal offset issues at high operating frequencies. The final system's count rate was increased to $50MHz$.

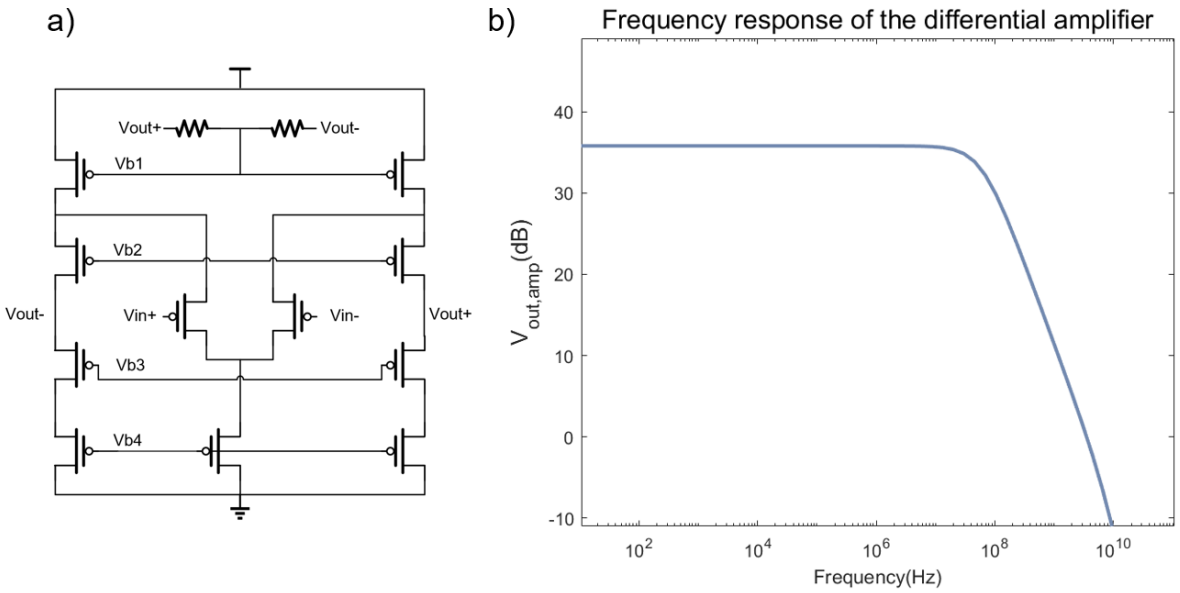


Figure 2.16: (a) Differential main amplifier (b) Frequency response

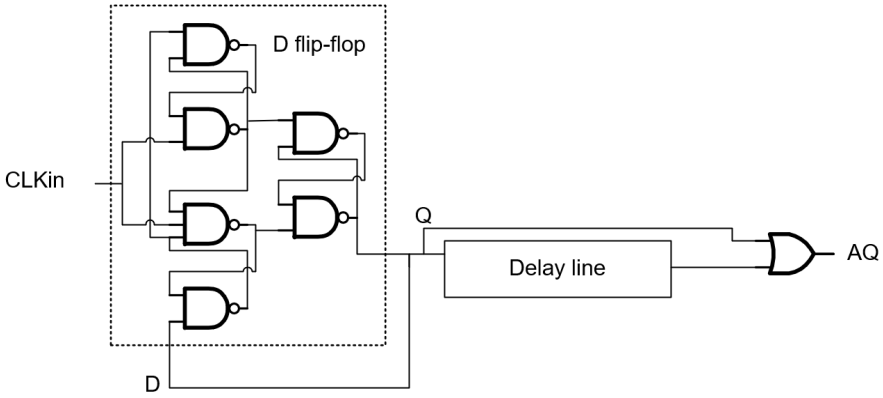


Figure 2.17: Digital sub-circuit with D flip-flop

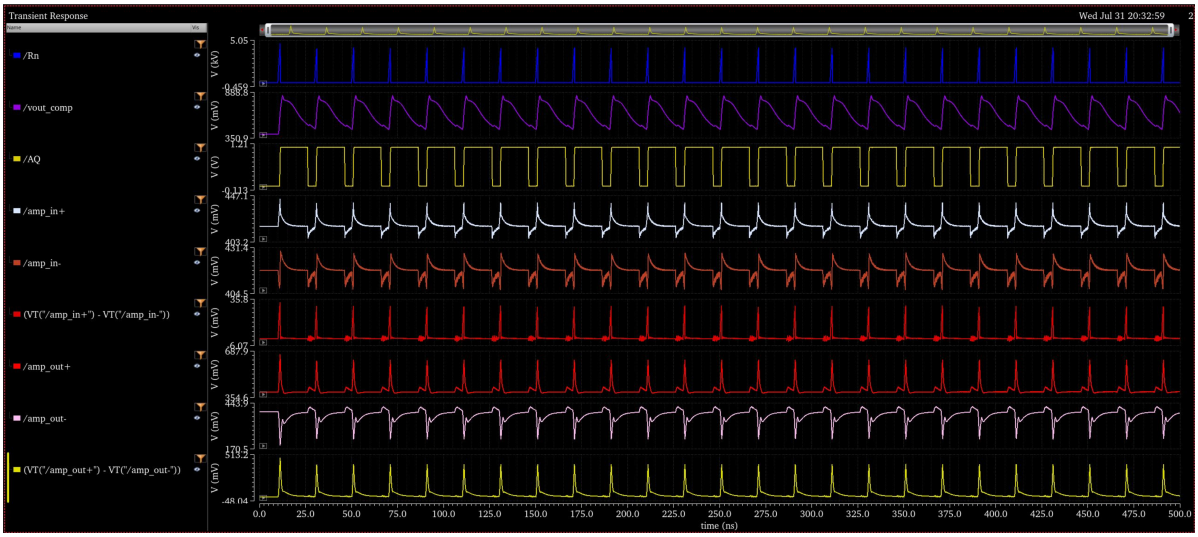


Figure 2.18: System performance at 50MHz after improvement

3

Persistent Current SNSPD Modeling and Structure Design

The conventional way of using SNSPDs is as single-photon detectors, which offer high accuracy, low noise and high count rates. However, since each sensor needs a current source for biasing, a string of amplifier, comparator, and time-to-digital converter (TDC) for readout, it is hard to integrate multiple sensors in array as pixels together to form an image sensor. This chapter introduces and models the persistent current SNSPD structure, utilizing the lossless current properties of its superconducting loop to avoid the issues in conventional design.

3.1. Persistent Current SNSPD

A persistent current SNSPD is a design utilizing the memory feature of the persistent current in the SNSPD loop to generate zero loss during detection and low power consumption when working at low frequency. Since the sensor does not need current support during detection and can memorize the state of detection, it demonstrates great potential in multi-pixel expansion.

The exploration of generating persistent currents in superconducting loops has a long history. As early as 1938, the concept of a flux pump was proposed. In 1981, Van de Klundert and others introduced a flux pump design that uses two superconducting loops alternately to accumulate current in a coil [26]. However, in terms of applications, most flux pumps have been designed for larger-scale superconducting coils, such as those used to generate magnetic fields in Magnetic Resonance Imaging (MRI) systems [27], while they are rarely seen at the microscopic scale. The electromagnetic properties of superconducting circuits may differ between macroscopic and microscopic scales, a topic that will be discussed in subsequent chapters. In 2019, Onen et al. [28][29] made a promising exploration of photon detection using superconducting loops and persistent currents, the sensor structure is shown in figure 3.1. Unlike our approach, they employed a shunted constriction and a Y-shaped current combiner as the driving and readout components of the sensor. This enabled them to generate current efficiently and perform non-destructive, repeated readouts of the current state. However, the shunted detector introduced uncertainties and complexities by altering the loop characteristics. In this work, the design of SNSPD nanowire is compatible with conventional devices' parameters.

The initial idea of the persistent current SNSPD is depicted in figure 3.2. The green circle in figure 3.2(a) represents the superconducting SNSPD loop without any electrical connection with any circuit, while the red circle is the input coil that is connected to the driving source. These two loops are in close proximity and are considered magnetically coupled. Consequently, changes in current in either loop induce variations in the magnetic flux within the loop area, and these flux changes, in turn, affect the current. When the current in the input coil, driven by a current source, increases as shown in Figure 3.2(b), the current in the SNSPD loop also increases due to the coupling, as illustrated in Figure 3.2(c). The current is increased until the current in the SNSPD reaches the critical current density of the superconducting nanowire. At this point, the nanowire temporarily reverts to a normal, non-superconductive, state due

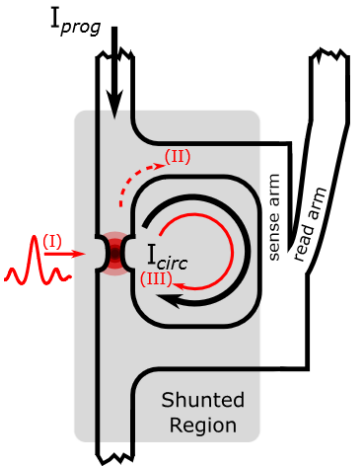


Figure 3.1: Single-Photon Single-Flux Coupled Detectors [28]

to the critical current being exceeded, resulting in a large resistance similar to the hotspot formation in traditional SNSPDs. Consequently, the current in the SNSPD loop drops rapidly. If the current in the input coil subsequently decreases, the current in the SNSPD loop will initially decrease and then increase in the opposite direction due to the magnetic field change. When the current in the input coil reaches zero, we achieve a state where no current is being input to the sensor, yet the SNSPD can maintain a relatively high current bias level without loss (in the case of an ideal superconductor) until triggered by an incident photon. Upon photon incidence, the SNSPD loop generates a hotspot and quenches the current, similar to a traditional SNSPD. This requires the aforementioned biasing process to be repeated to prepare the sensor for the next photon detection. Regarding detection, given that the SNSPD loop is electrically isolated, we can only investigate the coupling effects of the magnetic field changes on the input coil caused by the current drop in the SNSPD loop. This aspect will be discussed in subsequent sections.

The primary innovation of this design lies in introducing a persistent current to the SNSPD, with the aforementioned driving method being the core of this idea.

3.2. Modeling

To translate the design of a magnetically coupled persistent current SNSPD from concept to implementation, it is essential to model the sensing system. The developed model should reflect the overall operational logic, the physical and electrical characteristics of the system, and how parameter settings affect performance during detailed sensor design. Given that this system involves electronic, electromagnetic, and electrothermal processes, this section will address modeling and simulation from these three perspectives.

3.2.1. Coupling Analysis

COMSOL Analysis

In this design, the driving and state readout of the SNSPD are both achieved through magnetic coupling, making the coupling coefficient between the two loops critically important. Using COMSOL, it is possible to effectively explore the coupling performance and magnetic field distribution of different loop configurations. In this section, the input coil and the SNSPD loop will be considered as two coupled inductors, with an investigation into their individual self-inductances and mutual inductance.

Before simulation, we need to determine the approximate shape of the SNSPD loop. As shown in Figure 2.1, a traditional SNSPD includes a serpentine active area covering a large surface to receive photons, which essentially determines the total length of the nanowire. To achieve a higher magnetic coupling coefficient, the SNSPD loop needs to encompass a larger area to collect the magnetic flux changes generated by the driving coil. Although theoretically, more turns could enhance coupling, superconducting nanowires cannot be fabricated in multiple layers in SNSPD fabrication, so we can

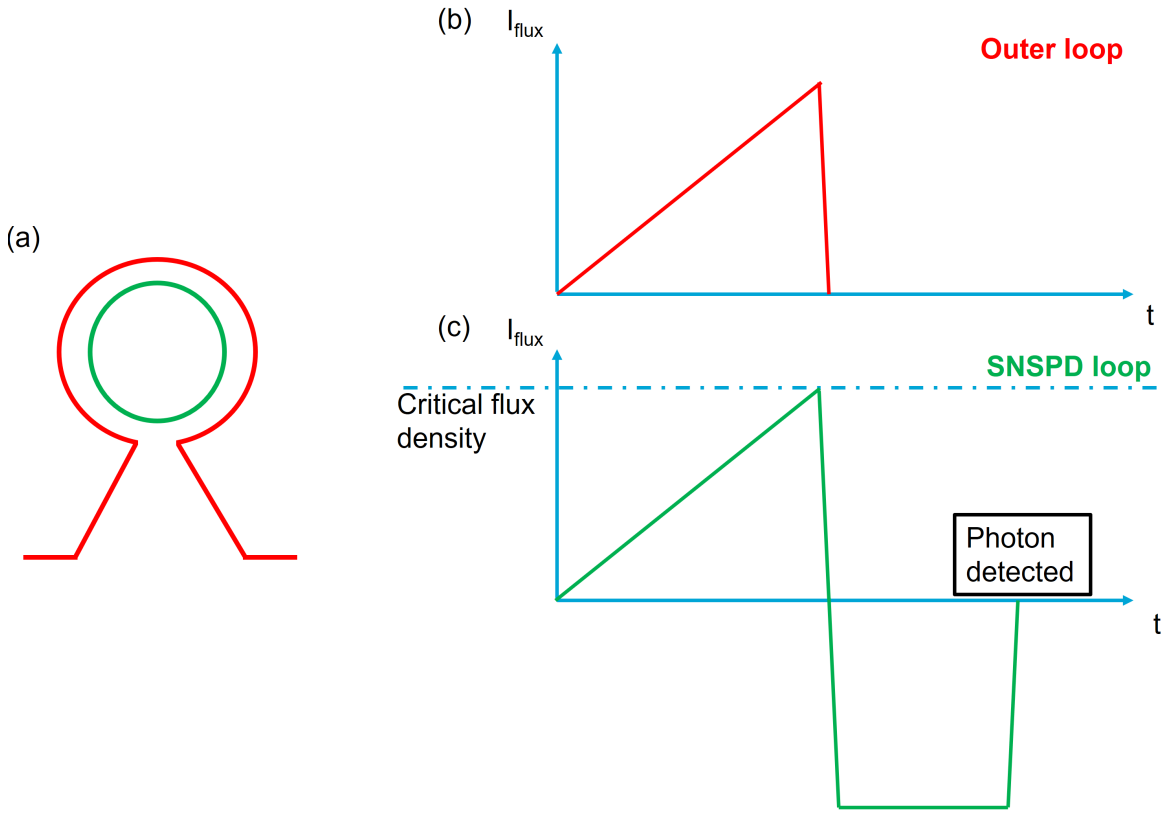


Figure 3.2: Original idea of persistent current SNSPD explored in this work. (a) shows the biasing coil (red) and superconducting sensing coil (green) magnetic coupling with each other. (b) shows the current in the biasing coil over time. (c) shows the introduced current in the superconducting sensing coil. The key idea of this approach is to use the persistent current in a superconducting loop as the bias current for the SNSPD. Coupling coils are employed to control the superconducting loop.

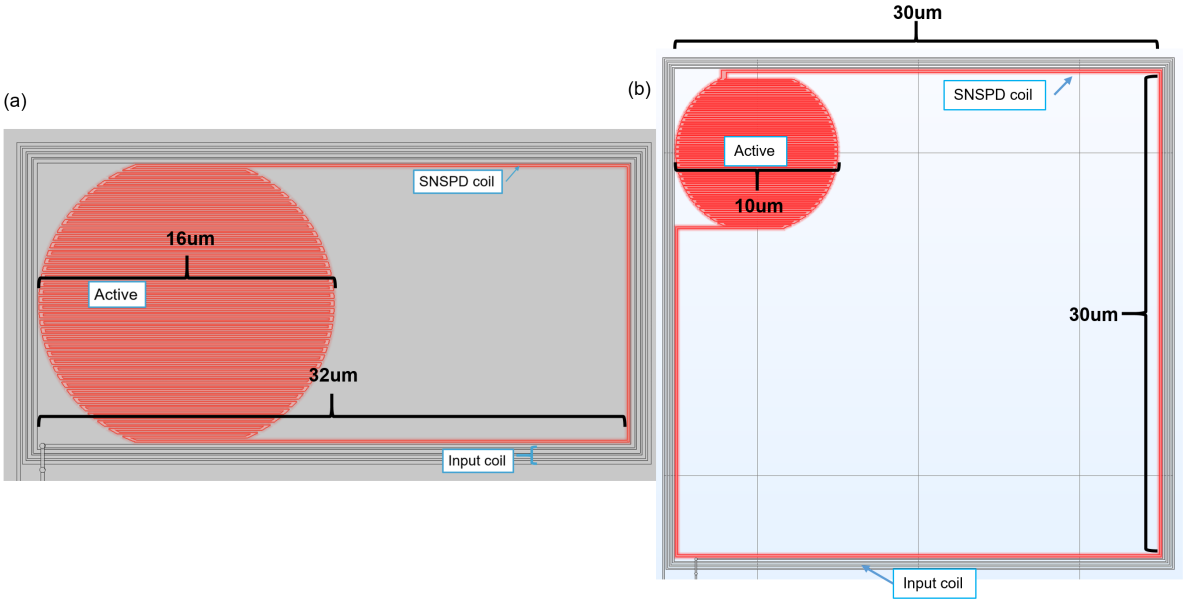


Figure 3.3: SNSPD structure in Active area ratio of (a) 1/2 (b) 1/9

Table 3.1: COMSOL simulation result

Active area ratio	1/2	1/9
Wire width	70nm	
Wire thickness	10nm	
Wire pitch	100nm	
L_{coil} [nH]	1.25	1.74
L_{snspd} [nH]	0.42	0.29
Mutual inductance M [nH]	0.17	0.3
Coupling coefficient k	0.23	0.42
Inductance ratio n	2.98	5.94

only have a single turn to form a closed loop. Therefore, the sensor design is as shown in Figure 3.3. The width and thickness of the nanowire and the diameter of the circular structure in the active area are taken from the typical values of mature products by Single Quantum, the SNSPD manufacturer collaborating on this project.

In a single structure, a larger active area ratio implies a higher photon reception probability, so the blank area for magnetic coupling should not be too large. Additionally, the magnetic flux density is higher in the region close to the wire, so further increasing the blank area would result in only marginal improvements in coupling, making this approach ineffective. Figures 3.3 (a) and (b) show cases where the total area is twice and nine times that of the active area, respectively, to explore the differences in coupling performance under different ratios and sizes.

Since the geometrical inductance is only determined by the shape of the loop, and is the only inductance that could be simulated by COMSOL, both loops are modeled using Copper (Cu) in the simulations to simplify the process since COMSOL does not provide a mature superconductor model. The influence of superconducting materials on the coupling will be discussed in the next section. The simulation results are shown in Table 3.1, which includes the self-inductance and mutual inductance of each loop pair. In the table, k is the coupling factor, n is the ratio of L_{coil} and L_{snspd} The data indicate that using larger coils does indeed result in greater mutual inductance, but only has a marginal improvement. For typical SNSPD lengths, both the self-inductance and mutual inductance of the loop pair are in the nanohenry (nH) range. Increasing the number of turns in the input coil can enhance both its self-inductance and mutual inductance, but it also poses a risk of increased coil resistance, which will be discussed in detail in the following calculations.

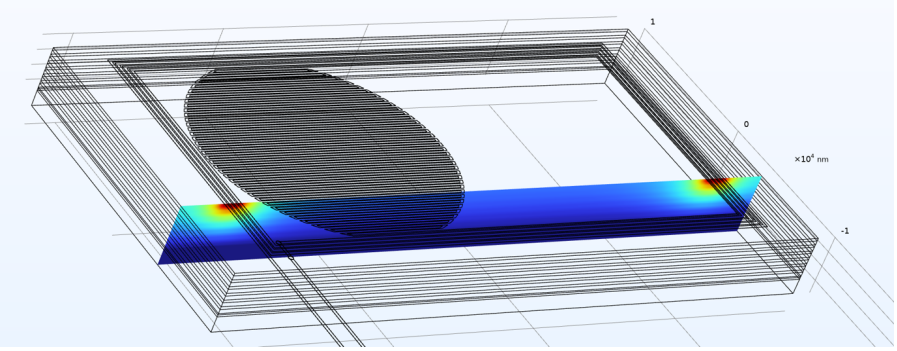


Figure 3.4: Parasitic capacitor simulation

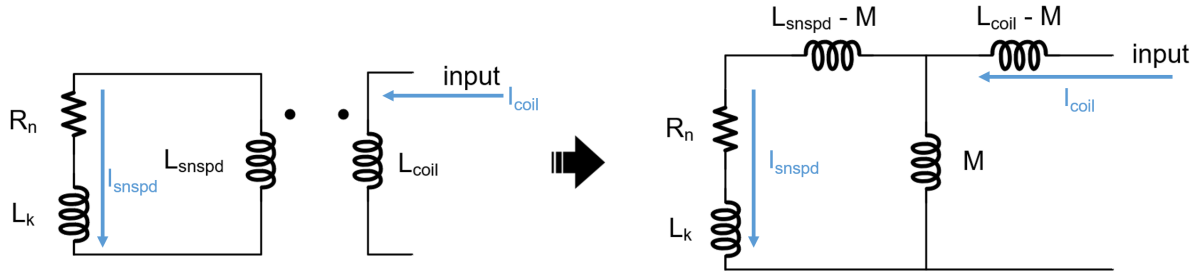


Figure 3.5: Transformer model and equivalent T circuit, M is the mutual inductance, $L_{coil} - M$ and $L_{snspd} - M$ are the leakage inductance

The parasitic capacitance of the loop structure was also explored through simulations, with both loops modeled using Cu as the material and the substrate set according to Single Quantum's standard structure, shown in figure 3.4. The simulation, based on the configuration shown in Figure 3.3(a), was conducted to estimate the order of magnitude. The input coil's capacitance to the substrate is $7.7\,\mathrm{fF}$, the SNSPD loop's capacitance to the substrate is $8.3\,\mathrm{fF}$, and the capacitance between the input coil and the SNSPD loop is $9.4\,\mathrm{fF}$. These capacitances are almost negligible compared to the estimated $125\,\mathrm{fF}$ parasitic capacitance from the pad and bonding wire.

Superconductor Coupling Feature

The above simulations treated the two loops as normal metals, without accounting for their superconducting properties. In this case, the coupling feature of the loops could be modeled as a transformer connected in series with the SNSPD, and have a T-shaped equivalent circuit, shown in figure 3.5. At this point, the ratio of the total current entering the input coil to the current flowing into the SNSPD is:

$$\frac{I_{snspd}}{I_{coil}} = \frac{M}{L_k + L_{snspd} - M} \tag{3.1}$$

(with R_n being zero during the current increase in the biasing process). Given that the typical value of L_k in the SNSPD (around $1\,\mathrm{uH}$) is much larger than the mutual inductance M in the T circuit (in table 3.1), the current coupled into the SNSPD loop will be much smaller compared to the total input current.

However, during discussions with Single Quantum, it was noted that a superconductor, being an ideal lossless conductor, will convert all received magnetic flux changes into changes in the loop current. Consequently, from the moment the superconducting closed loop is established, the net magnetic flux within it will remain constant (flux conservation). This has been shown in literature, the flux pump design by Lacy et al. leverages this property as illustrated in figure 3.6 [30]. This design alternately disconnects two thermal switches to transfer magnetic flux into the target loop via a pumping loop. Each time a thermal switch re-closes, the total magnetic flux in the newly established superconducting loop remains constant. By ensuring that the pumping loop encloses a higher magnetic flux density when it becomes superconducting and then distributes this flux to the target loop, it achieves flux accumulation.

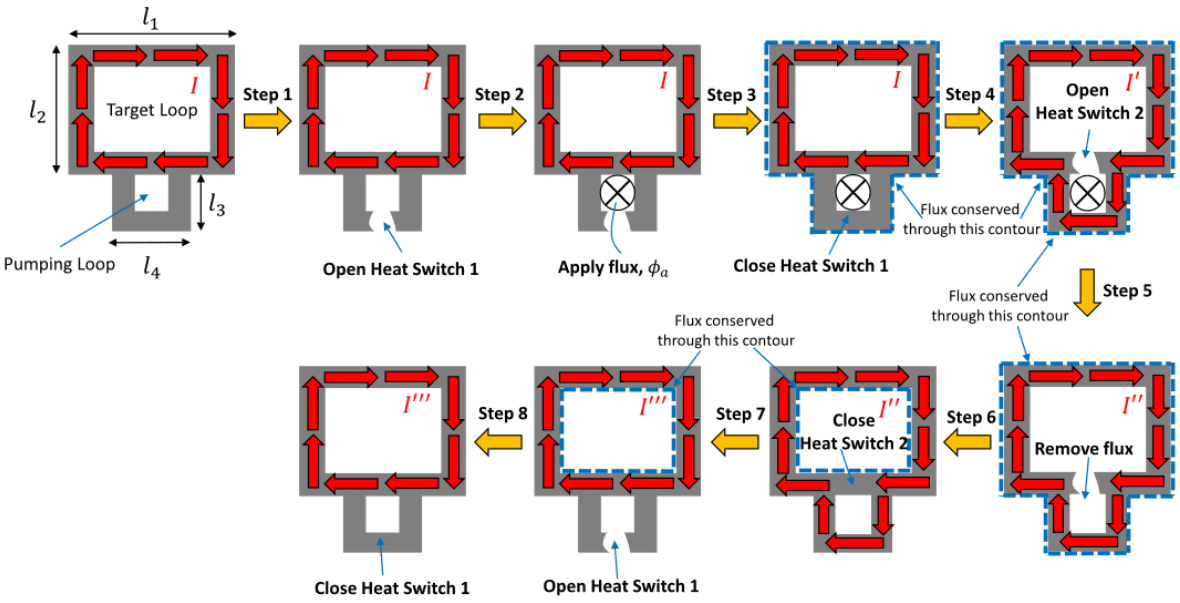


Figure 3.6: Flux pump using flux conservation in superconducting loop [30]

Back to our case, the large ratio of I_{snspd} and I_{in} still holds even if the coupling is ideal, which means all the flux generated by L_{coil} is accepted by L_{snspd}. So, what causes the conflict between these two theories? To identify the point of divergence, we need to trace back to the origins of the theories. The T-model transformation of the transformer is derived from Maxwell's equations, while the flux conservation, as mentioned in [30], is based on the Ginzburg-Landau theory. In this theory, a closed superconducting loop, defined by a contour C, with transport current density J, and internal flux φ' obeys:

$$\varphi' = \oint_C \mu_0 \lambda^2 J dl + \int BdS + \varphi_a = constant \tag{3.2}$$

where λ is the London penetration depth, B is the self-field of the closed loop, S is the surface defined by the contour C. For the high-temperature superconducting material (HTS) used for the flux pump of Figure 3.6, the first term in the equation can be neglected due to $\lambda^2/S_{section} << 1$ ($S_{section}$ is the cross-section area of the superconductor, at $1\,\mathrm{mm}^2$ in this research, while $\lambda \approx 100nm$) [31]. As a result, the sum of the self-induced magnetic field (B) and the externally applied magnetic field φ_a remains constant, ensuring that the magnetic flux within the closed loop is conserved.

However, SNSPDs are much thinner, averaging a sensor thickness of around 10 nm, while NbTiN has a penetration depth of approximately 200 nm [32]. For $I_b \approx 20\mu A$ we get:

$$\oint_C \mu_0 \lambda^2 J dl = 1.44 \times 10^{-12} Wb \tag{3.3}$$

$$\int BdS = I_{bsnspd} = 3 \times 10^{-14} Wb \tag{3.4}$$

The first term in the equation cannot be neglected.

Besides, [33] also mentioned that the kinetic inductance function can be rewritten as:

$$L_k = \frac{\lambda^2 \mu_0 C}{S_{section}} \tag{3.5}$$

The larger the ratio $\frac{\lambda^2}{S_{section}}$ is, the more likely the kinetic inductance is to dominate. Based on the above considerations, we can preliminarily speculate that the flux conservation may not fully apply to nanoscale SNSPD loops. However, due to the lack of precise computational and simulation methods, we are unable to obtain accurate coupling data. What we can infer is that the actual coupling should

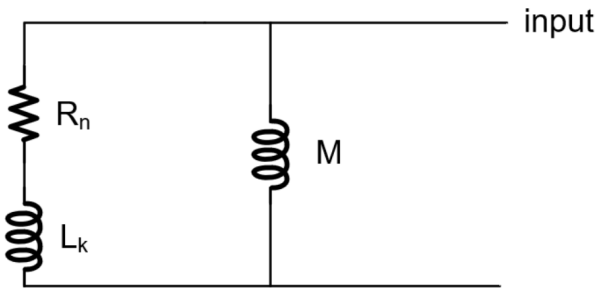


Figure 3.7: Coupling model for superconducting loop

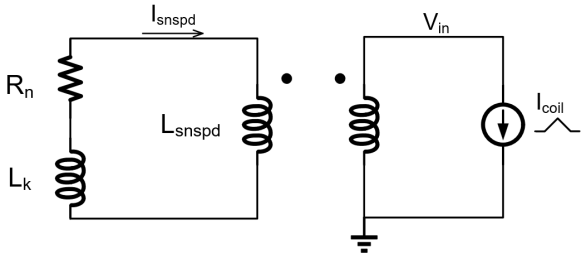


Figure 3.8: Basic circuit model

fall between the ideal scenario (where all flux is perfectly converted) and the worst-case scenario (fully aligned with the mutual inductance simulation results from COMSOL). Therefore, in the subsequent calculations and sample designs, we will address different assumptions with corresponding strategies.

Assuming that the coupling between the two loops is tighter due to the presence of superconductivity, the standard T-model may no longer be applicable. We will need to make certain modifications to better align the model with the more ideal coupling scenario.

Considering that the main characteristic of an ideally coupled superconducting loop is flux conservation—where all magnetic flux changes are converted into changes in the loop current, resembling an ideal transformer—this would manifest in our project as a higher ratio of $\Delta I_{snspd}/\Delta I_{coil}$. However, from the T-model, we see that this current ratio is primarily limited because the L_k is much larger than M, preventing significant current from entering L_k, requiring a large current in the bias coil and increasing losses.

During the design of the electronics, various coupling ratios will be tested. Since we don't know which ratio fits the reality, we would start from a midrange value and explore both ideal and non-ideal scenarios. Here, an increased $\Delta I_{snspd}/\Delta I_{coil}$ ratio can be created with a larger M value. For instance, when $L_k = 1\,\mathrm{uH}$, assuming $M = 100\,\mathrm{nH}$ would yield a 1/10 current ratio. In terms of circuit modeling, this scenario can be simplified as shown in Figure 3.7, where different M values are used to simulate various conditions. Given that the magnitudes of L_k and M are relatively large in this model, to simplify the model, the leakage inductance in series with L_k in Figure 3.5 is neglected here.

3.2.2. Initial Circuit Model Analysis and Calculation

Now that we have some insights into the coupling between the loops, it is time to investigate the overall operation of the system further. In this section, all investigations and calculations will be based on the worst-case scenario for magnetic coupling, where both loops are considered ordinary metals in coupling, as discussed in the previous section. This will serve as the starting point for estimating the coupling performance under more ideal conditions.

Basic Circuit Model

The initial model will be constructed using Cadence, with the magnetic coupling between the loops represented by a pair of coupled ideal inductors. An ideal current source will be used to input the current ramp, and all parasitic effects will be temporarily ignored, as shown in figure 3.8. The SPICE

model of the SNSPD will follow the dynamic model proposed by Berggren et al. in 2018 [34], with implementation details consistent with the work of Li [8]. The model uses the electrical and thermal parameters of the SNSPD nanowire material to configure the switches and controlled resistors. This setup accurately models the signal rise time, signal amplitude, device reset, and nanowire latching when the nanowire is triggered. A detailed analysis and configuration of this model will be discussed later.

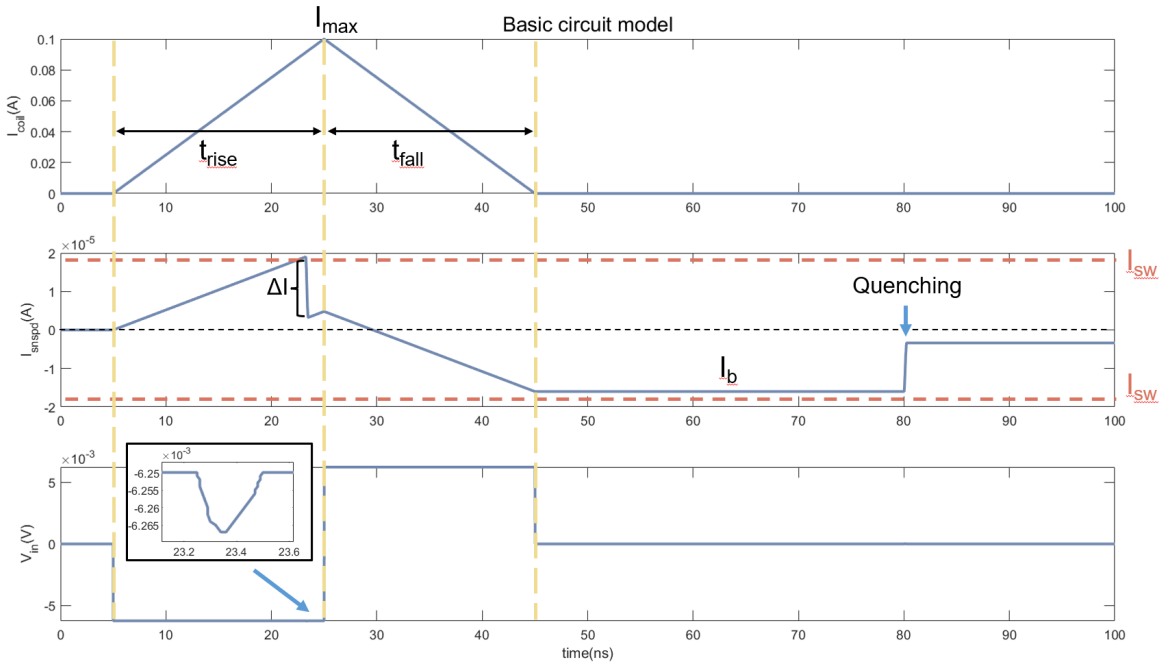


Figure 3.9: Basic circuit model characteristic. Insert illustrate the voltage spike caused by quenching at the input node

Figure 3.9 illustrates the currents within the input coil and the SNSPD under this model, as well as the voltage observed at the input node. The values for L_{coil} and L_{snspd} are set according to the scenario where the active area is 1/2 of the total area, as specified in table 3.1. The L_k is set to $800\,\mathrm{uH}$.

The figure shows the various currents and behaviors, confirming the assumption made in Figure 3.2. The current in the input coil increases from 0 to I_{max} (0.1 A) and then returns to zero. The current in the SNSPD rises to I_{sw} ($20\,\mu\mathrm{A}$), but it suddenly drops due to hotspot formation. After the SNSPD cools down, the current briefly rises again, following the input coil's current, then decreases to zero before increasing in the opposite direction to complete the biasing process. It is important to note that the I_{snspd}'s increase after quenching, driven by I_{coil}, is followed right after by a decrease due to I_{coil}'s falling. Therefore this small rise and fall theoretically does not affect the final bias current as long as the current in the SNSPD does not quench again. Finally, the large ratio between I_{max} and I_{snspd} originates from the poor coupling and kinetic inductance.

As shown in Figure 3.5, in the equivalent T-model, the input current I_{coil} is split between the paths defined by M (mutual inductance) and L_k (kinetic inductance). The current distribution ratio is primarily determined by the ratio of these two inductances, with the leakage inductance being negligible compared to L_k. Therefore, the changing current in the input coil and the SNSPD will maintain a fixed ratio:

$$\frac{\Delta I_{snspd}}{\Delta I_{coil}} = \frac{M}{L_k + L_{snspd}} = \frac{kL_{snspd}\sqrt{n}}{L_k + L_{snspd}} \tag{3.6}$$

$$\Delta I_{coil} \approx \frac{\Delta I_{snspd} L_k}{kL_{snspd}\sqrt{n}} \tag{3.7}$$

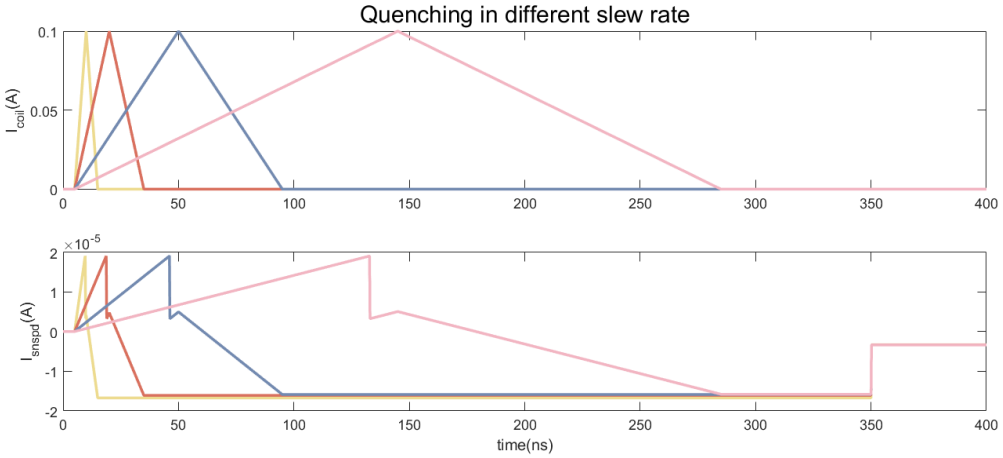


Figure 3.10: Quenching in different current slew rate

Table 3.2: ΔI and I_b at different slew rate

Slew of I_{snspd} (uA/ns)	4.16	1.39	0.46	0.15
ΔI (μA)	16.77	15.74	15.81	15.77
I_b (μA)	16.74	16.09	15.88	15.81

Referring back to Figure 3.9, we can observe that since I_{coil} starts and ends at 0, the current I_{snspd} would also return to 0, assuming no quenching occurs. However, during quenching, I_{snspd} experiences a drop of ΔI. As a result, the final bias current I_b is also reduced by ΔI relative to 0. This indicates that:

$$I_b = \Delta I \tag{3.8}$$

assuming the quenching duration is negligible.

For the biasing of an SNSPD, the most critical factor is the magnitude of the bias current I_b after a single biasing operation, as it significantly impacts the sensor's SDE and DCR. Therefore, it is crucial to further investigate the factors influencing I_b. Theoretically, quenching in the nanowire is a thermal process, involving the current reaching I_{sw} and generating a large resistance, and the dissipation of heat into the substrate. If the current drop during quenching is sufficiently fast compared to the increase in current driven by I_{coil}, the driving current will have minimal impact on the quenching process.

Figure 3.10 illustrates different scenarios where the slew rate (SR) of the SNSPD current I_{snspd} varies from $4.16\,\mathrm{uA/ns}$ to $0.15\,\mathrm{uA/ns}$. The relationship between the current slope, ΔI, and I_b is summarized in table 3.2. In the simplified SPICE model, ΔI is stable compared to the I_{snspd} slew rate, suggesting that the values of ΔI and I_b are likely determined primarily by the intrinsic physical properties of the nanowire, with minimal influence from the biasing operation. However, given that the SPICE model used in the circuit simulation is overly simplified and may not accurately capture all the characteristics of the nanowire, a more precise simulation and modeling approach is required. This advanced method will be discussed in detail in section 3.2.3.

Regarding detecting the SNSPD state, since the superconducting loop has no electrical connections, we need to detect the event through the change in magnetic flux during a quench. When the current in the SNSPD loop suddenly drops, a voltage spike is generated at the input terminal of the coupled input coil—this is the signal we need to detect. The width of this spike depends on the quenching time, while its amplitude is determined by ΔI and the mutual inductance M.

$$V_{spike} = M\frac{dI_{snspd}}{dt} \tag{3.9}$$

For the pessimistic scenario with M in the order of nH as shown in Figure 3.9, the spike amplitude can be as low V level (for $\Delta I \approx 15\,\mu\mathrm{A}$, $\Delta \approx 0.3\,\mathrm{ns}$), making potential detection difficult. A larger M value

improves the spike amplitude, so achieving a higher coupling is desired to have a larger signal for any potential detector.

Analysis for Performance and Limitation

From equation 3.6 and 3.7, we can see that the ratio $\Delta I_{snspd}/\Delta I_{coil}$ is determined by the ratio of M/L_k. Given that we always need the current increase in the SNSPD to slightly exceed I_{sw} (to trigger quenching during the bias operation), a larger M value reduces the required input current, thus lowering the power consumption per bias operation. Equation 3.12 illustrate a loop design with a large coupling factor k and more turns of coil (n) both helps get a low I_{max}. In this design, theoretically, no energy input is needed from the completion of one bias operation until the sensor is triggered. Therefore, the power consumption of the biasing circuit depends on the frequency (f) of the bias operations. The energy consumption of a single bias operation, at a fixed V_{dd}, is determined by the maximum input current I_{max} and the rise and fall times of the current t_{rise} and t_{fall} (assuming a constant current slope). Assume $t_{rise} = t_{fall}$:

$$P = \int_{t_{rise}+t_{fall}} V_{dd} I_{coil}(t) dt \tag{3.10}$$

$$= V_{dd} I_{coil,max} t_{rise} f \tag{3.11}$$

$$I_{max} \approx \frac{I_{sw} L_k}{k L_{snspd} \sqrt{n}} \tag{3.12}$$

For the same superconductor at a given temperature, the switching current (I_{sw}) is proportional to its cross-sectional area. The value of kinetic inductance is also related to the cross-sectional area and the length of the superconductor:

$$Isw = J_{sw} dw \tag{3.13}$$

$$L_k(T) = \frac{m}{2e^2}(\frac{l}{wd})(\frac{1}{n_s(T)}) \tag{3.14}$$

w, d, and l are width, thickness and length of the nanowire, respectively, J_{sw} is the switching current density, m is the mass of an electron, and $n_s(T)$ is the temperature-dependent Cooper pair density [35].

$$I_{max} = (J_{sw} \frac{m}{2e^2 n_s} l) \frac{1}{k L_{snspd} \sqrt{n}} \tag{3.15}$$

By deriving equation 3.15 from equations 3.12, 3.13 and 3.14, the resulting expression for I_{max} shows that the width and thickness of the nanowire cancel out. This is because a wider and thicker nanowire decreases L_k while simultaneously increasing I_{sw}. The terms J_{sw}, m, and n_s are dependent on the ambient temperature and the physical properties of the nanowire. Therefore, there are two ways to achieve a lower I_{max}. First, the coupling between the bias coil and superconducting coil can be improved by using more turns in the input coil and secondly, we can reduce the total length of the SNSPD and make pixels with smaller active area (for a specific I_{sw}).

To determine the required V_{dd}, the material of the bias coil becomes important. The first option is to fabricate the coil using a superconductor, which would eliminate parasitic resistance in the coil itself. During the biasing operation, the voltage across the bias inductor creates a changing current. The equivalent impedance seen from the supply is a combination of the kinetic inductance of the input coil and the kinetic inductance of the nanowire parallel with the mutual inductance (geometrical inductance could be ignored compared to the others):

$$Vdd \geq \frac{dI_{coil}}{dt}(M // L_k + L_{k,coil}) \tag{3.16}$$

Unlike the SNSPD, where the width and thickness are constrained by optical performance, the input coil's kinetic inductance is expected to be much lower than that of the SNSPD because the on-chip superconductors are limited to single-layer fabrication, preventing the creation of multi-turn coils (it

needs the wire overlapping). And the input coil does not have the meandering structure, which saves the total length and results in a relatively small inductance (if added in the model in Figure 3.7, it should be connected in series with $M//L_k$).

In scenarios where $\Delta I_{snspd}/\Delta I_{coil}$ is large and hence there is a good coupling, L_k of the SNSPD will primarily determine the voltage headroom (based on Equation 3.16, when $\lim_{M\to\infty}$, $L_k \gg L_{k,coil}$):

$$Vdd \geq \frac{dI_{coil}}{dt}(L_k + L_{k,coil}) \tag{3.17}$$

In contrast, with poor coupling ($\Delta I_{snspd}/\Delta I_{coil}$ being low), the coupling will be mainly determined by the geometrical inductance of the two loops (reflected in the value of M) and the bias coil kinetic inductance:

$$Vdd \geq \frac{dI_{coil}}{dt}(M + L_{k,coil}) \tag{3.18}$$

In this case, a single-turn input coil would result in weak coupling and require a much higher I_{max}. However, the superconducting input coil also has a switching current, and when the switching current exceeds I_{max}, the input coil's cross-sectional area would be much larger than that of the SNSPD. For instance, with $I_{max} = 100mA$ and $I_{sw} = 19\,\mu\mathrm{A}$ (as shown in Figure 3.9), the cross-section ratio could reach 5000:1, making it challenging to fabricate the sensor. Therefore, a superconducting input coil is only suitable under conditions of good coupling.

For input coils made from conventional metal materials, parasitic resistance becomes the primary factor limiting V_{dd}. Taking the structure parameters from Figure 3.3 (a) as an example, the total length of the input coil is simplified to $(16 + 32) \times 2 \times 4 = 384\,\mu\mathrm{m}$, with the width and thickness assumed to be the same as those of the SNSPD nanowire: $w = 70\,\mathrm{nm}$ $d = 10\,\mathrm{nm}$. Gold (Au) is chosen as the coil material. At cryo temperatures, the resistivity of gold decreases compared to room temperature, although this reduction is influenced by the material's purity. Here, we use the mid-range value from the data provided in [36]: $\rho = 1 \times 10^{-9}\,\Omega\mathrm{m}$. Under these conditions, the total resistance of the coil is approximately $550\,\Omega$. Using thicker and wider wires can effectively reduce the resistance, but can also make the fabrication of multi-layer coils more complex.

In the case of poor coupling, the inductance seen from the input end is given by $M//(L_k + L_{snspd} - M) + L_{coil} - M$, which is at the sub-nH level. At this scale, the voltage headroom consumed by the inductance is minimal and negligible compared to the resistance. As a result, the load on the driving circuit can be approximated as the resistance of the input coil. Therefore, the necessary energy for driving the SNSPD is given by the integral:

$$E = \int I_{coil}(t)^2 R_{coil} dt = 2\int_0^{t_{rise}} (\frac{I_{max}}{t_{rise}} \times t)^2 R_{coil} dt = \frac{2}{3} I_{max}^2 R_{coil} t_{rise} \tag{3.19}$$

Assuming the coil resistance R_{coil} is reduced to 50 ohms by making the gold wider and thicker, a V_{dd} of 5V would be required. To further reduce V_{dd}, it is necessary to either decrease I_{max} or find an input coil design with lower internal resistance. If t_{rise} is 10ns and the bias operation frequency is $10\,\mathrm{kHz}$, the necessary power consumption due to the bias operation is at least 16μW. A shorter t_{rise} is preferable, but it depends on the design of the bias circuit, which will be discussed in the next chapter.

In traditional SNSPD designs, an SNSPD with $I_{sw} = 19\,\mu\mathrm{A}$ requires a bias power of at least $19\,\mu\mathrm{W}$ at $V_{dd} = 1V$ (assume the nanowire is biasing with a current source supplied by Vdd), which already exceeds the estimated power consumption in the above calculation. Moreover, the parameters used in this estimation have not yet been optimized, leaving significant room for improvement. This indicates that the design proposed in this project holds strong potential for low-frequency, low-power applications.

3.2.3. SNSPD Finite Element Electrothermal Analysis

To effectively control the final biased current I_b in the biasing operation, it is essential to thoroughly investigate the quenching characteristics of the SNSPD. The SPICE model used in the last subsection does not account for the detailed electrothermal processes involved. In this subsection, we will utilize a finite element simulator to get a more accurate result of the biasing behavior such as ΔI, exploring the influence of SNSPD device geometry, and trying to find out the relationship between the parameters

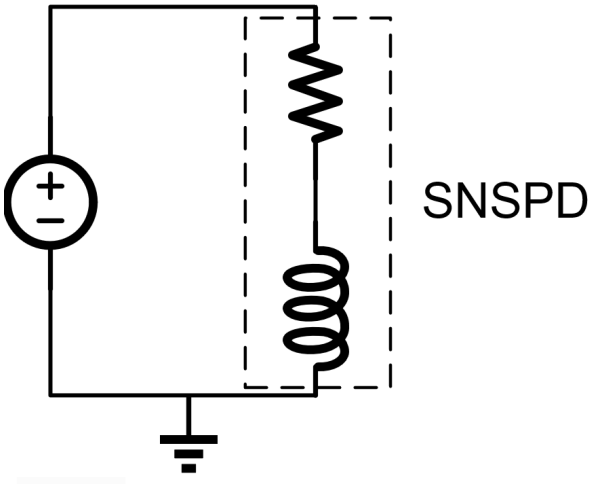


Figure 3.11: Circuit in Pyspice simulator

we can edit to the final bias current I_b. The simulator, which is developed by Single Quantum, uses Python and Ngspice to explore quenching in detail and develop a comprehensive design methodology for SNSPDs. The model is constructed using Pyspice modules to build the circuit and can output transient simulation results for SNSPD current, voltage, resistance, and temperature.

Quenching in an SNSPD involves the entire process from the onset of hotspot resistance R_n to the dissipation of heat and the return of the nanowire to its superconducting state. The decrease in current during this process is a key result of interest, and the physical properties and design of the nanowire influence quenching. The physical parameters of the SNSPD are provided with the simulator, and the parameters we can change in the design include the nanowire's length (l), width (w), thickness (d), switching current (I_{sw}), kinetic inductance (L_k), and the slew rate of I_{snspd} rising. The quenching result of I_{snspd} can be described by the change in current ΔI and the duration Δt. It is essential to identify the relationship between input and output variables to investigate factors affecting I_b. Additionally, to prevent the bias from being solely dependent on the physical process, methods for actively controlling I_b are also being explored. In this simulation, the SNSPD circuit is simplified to a voltage source connected directly across the SNSPD to create a constant current slope, as shown in Figure 3.11. When a constant voltage V_{in} is applied across the SNSPD, the current I_{snspd} will increase linearly. Given that the properties of the nanowire are uniform throughout the simulator, once the current reaches I_{sw}, the entire nanowire will transition to the normal state and exhibit a very high resistance, as illustrated in the heat map shown in Figure 3.12 (b). In reality, due to inevitable manufacturing imperfections, the nanowire's cross-sectional area will vary, and the smallest cross-sectional areas are likely to transition to the normal state first. This hotspot formation process is similar to that occurring with photon incidence, as shown in Figure 3.12 (a). Therefore, in the simulation, a photon will be introduced at the moment the current increases to I_{sw} to trigger the sensor. Simultaneously, the voltage source will be turned off to eliminate its effect on the quenching process.

In a given material-based SNSPD, once the width w, length l, and thickness d are determined, the kinetic inductance L_k and switching current I_{sw} should also be fixed. However, in the simulator, these five parameters can be configured independently. A typical set of values will be used as a starting point: $w = 70\,\mathrm{nm}, d = 10\,\mathrm{nm}, I_{sw} = 20\,\mu\mathrm{A}, l = 800\,\mu\mathrm{m}$, and $L_k = 800\,\mathrm{nH}$. These parameters will first be scanned individually to explore their respective influences on ΔI and Δt. These analyses are crucial for understanding the upcoming simulations. Subsequently, all parameters will be scanned in combination to investigate the real case.

Figure 3.13 shows the results of the individual scans of the five parameters in the electrothermal simulation. Figures 3.13 (a) and 3.13 (b) illustrate the impact of varying the width and thickness of the nanowire, respectively, on ΔI and Δt, while keeping the other parameters at their initial values. We can clearly observe that a wider nanowire significantly reduces ΔI and extends the quenching time. This is likely because increasing the width reduces the hotspot resistance per unit length, weakening

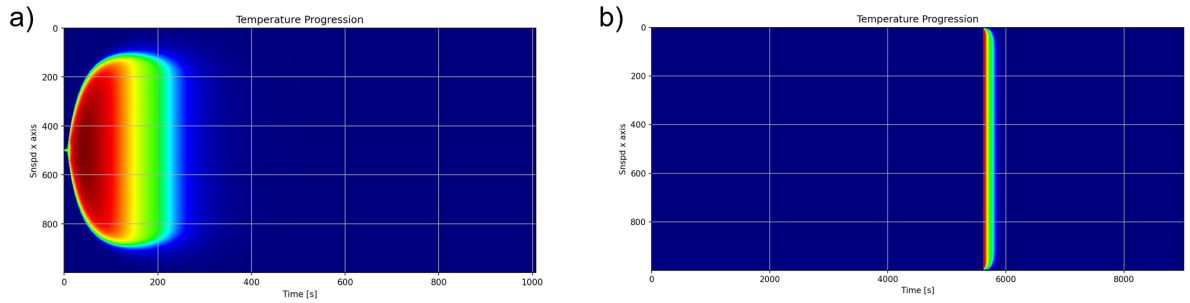


Figure 3.12: Heat map example of SNSPD quenching, with red indicates high temperature, blue represents low temperature, the x-axis corresponds to time, and the y-axis represents the length of the SNSPD. (a) Photon imitate quenching: photon incident at t=0 (b) Direct quenching: quench at the time when I_{snspd} reach I_{sw}

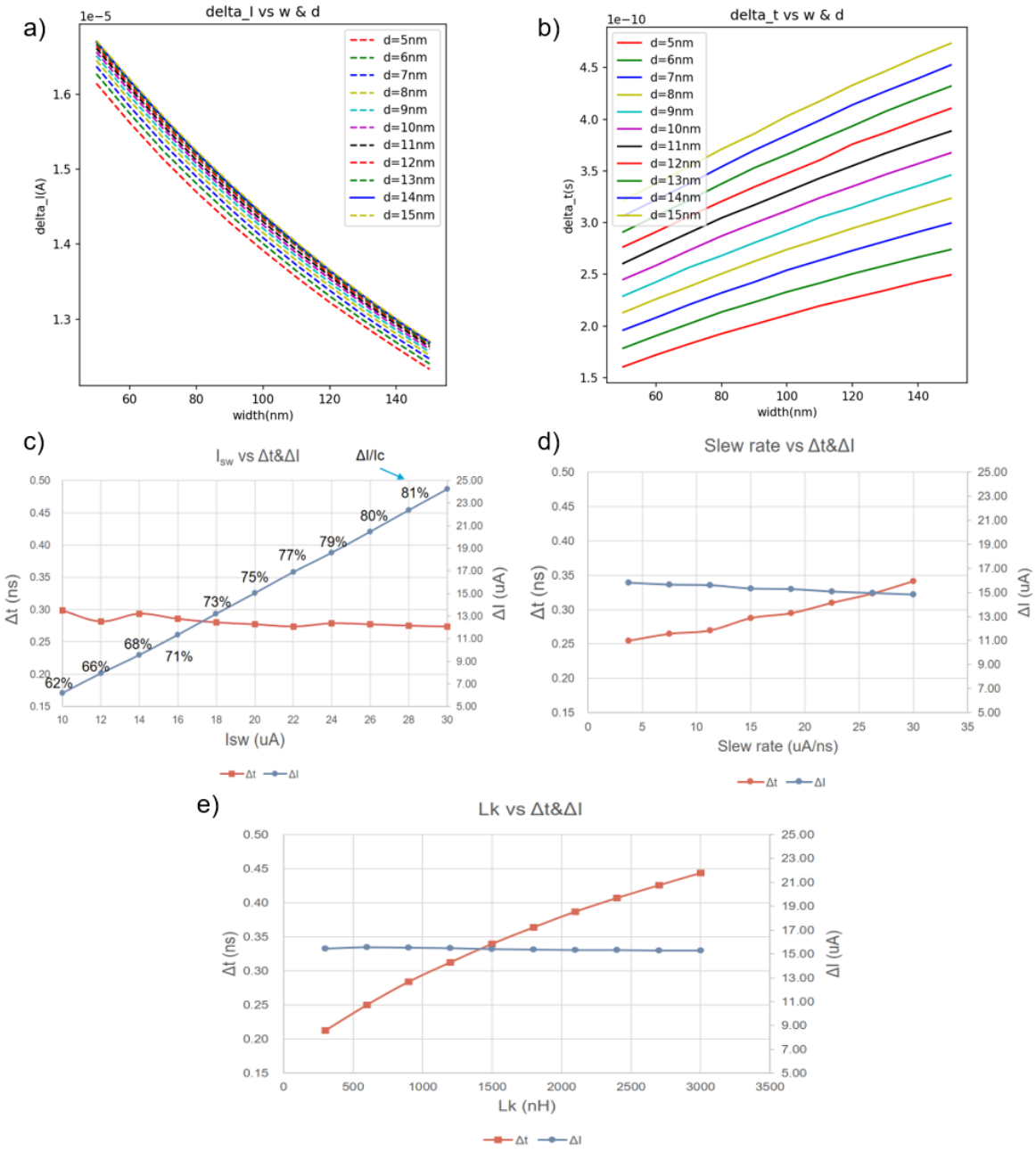


Figure 3.13: Parameter sweeps, (a) plots w and d versus ΔI, (b) plots w and d versus Δt, (c) plots I_{sw} versus Δt and ΔI, the percentages are the ratio of $\frac{\Delta I}{I_{sw}}$, (d) Slew rate of the input current versus Δt and ΔI and (e) L_k versus Δt and ΔI

Table 3.3: $I_{sw}(\mu\mathrm{A})$ vs w & d ($l = 800\,\mu\mathrm{m}$)

d(nm)/ w(nm)	50	100	150
5	7.2	14.3	21.5
10	14.3	1.86	42.9
15	21.5	42.9	64.4

its ability to suppress the current. Similarly, increasing the thickness also decreases the hotspot resistance, but unlike the width, it does not increase the surface area in contact with the substrate. As a result, the faster accumulation of heat may actually enhance the suppression of the current.

Figure 3.13 (c) demonstrates that increasing I_{sw} alone causes $\Delta I/I_{sw}$ to increase. This occurs because the nanowire must reduce its current to a certain threshold where its heating power becomes lower than its cooling power in order to return to the superconducting state. As a result, the value of $I_{sw} - \Delta I$ should remain relatively constant. A higher I_{sw} indicates that more current needs to be suppressed during quenching, and the larger I_{snspd} will also cause the hotspot resistance R_n to expand more rapidly. These two effects counterbalance each other, leading to a relatively stable quenching time Δt.

Figure 3.13 (d) illustrates that while the slope of I_{snspd} changes, the variation in ΔI remains relatively small, whereas Δt increases slightly as the slope grows. Even with a sixfold increase in the slope, the change in Δt is still less than 50%, indicating that both ΔI and Δt remain relatively constant during the entire quenching process. This suggests that the driving current's influence on I_{snspd} is somewhat shielded during quenching, and this characteristic can be leveraged for active control of I_b. The premise for the Equation 3.8 in section 3.3.2 to hold is that Δt is negligibly small. If Δt is accounted for, it indicates that during the rise of I_{coil}, there is a period, Δt, during which I_{coil} does not affect I_{snspd}. However, during the fall of I_{coil}, this absence of effect does not occur. Thus, we can obtain a complete description of the biased current I_b:

$$I_b = \Delta I + \Delta t \times SR \tag{3.20}$$

We can actively control the bias current I_b by adjusting the slope of I_{coil} during the quenching process, which alters the slope of I_{snspd} accordingly. The minimum value of I_b is set by ΔI. Therefore, this operation can only increase I_b beyond this minimum, allowing for limited control over the final biased current.

In Figure 3.13 (e), when L_k is increased independently, it is evident that Δt significantly increases, while ΔI remains stable. This phenomenon can likely be attributed to the larger L_k, which stores more kinetic energy, thereby prolonging the energy dissipation time. The extended duration of dissipation enhances the suppression of the current, resulting in little change in the overall current during the quenching process.

The unique characteristic of L_k compared to other parameters is that changing the length of the nanowire affects only L_k without influencing other parameters. This makes L_k the only independently controllable factor. However, as shown by Equation 3.15, the length of the nanowire is a key determinant of I_{max}, meaning that It is unlikely that we can adjust I_b effectively by tuning L_k.

When we combine all the parameters, the effects of different widths and thicknesses of the nanowires on ΔI and Δt will be investigated. The starting point remains $w = 70\,\mathrm{nm}, d = 10\,\mathrm{nm}, I_{sw} = 20\,\mu\mathrm{A}, l = 800\,\mu\mathrm{m}, and L_k = 800\,\mathrm{nH}$. Since L_k is inversely proportional to the cross-sectional area of the nanowire, we can calculate the kinetic inductance per unit length A using $L_k = \frac{l}{wd}A$, giving $A = 6.9 \times 10^{-19}\,\mathrm{H/m}$. From I_{sw} and w, we can calculate the switching current density $J_{sw} = 2.86 \times 10^{10}\,\mathrm{A/m^2}$. Thus, we can derive values for I_{sw} and L_k under different w and d combinations, as shown in Table 3.3 and Table 3.4. Due to the necessity of manually compiling the Cython package for the simulation tool used in this section, large-scale automated scans are difficult to perform. Therefore, only nine data points have been selected to qualitatively explore the quenching characteristics of the SNSPD.

The nine data points corresponding to $\Delta I/I_{sw}$ and Δt are shown in Figure 3.14. Remarkably, we observe that the width of the nanowire has almost no impact on either parameter, which can be approximated as "placing two identical nanowires side by side does not affect their performance." In contrast,

Table 3.4: $L_k(H)$ vs w & d ($l = 800\,\mu m$)

d(nm)/ w(nm)	50	100	150
5	2.24×10^{-6}	1.12×10^{-6}	7.47×10^{-7}
10	1.12×10^{-6}	5.60×10^{-7}	3.73×10^{-7}
15	21.5×10^{-7}	3.73×10^{-7}	2.49×10^{-7}

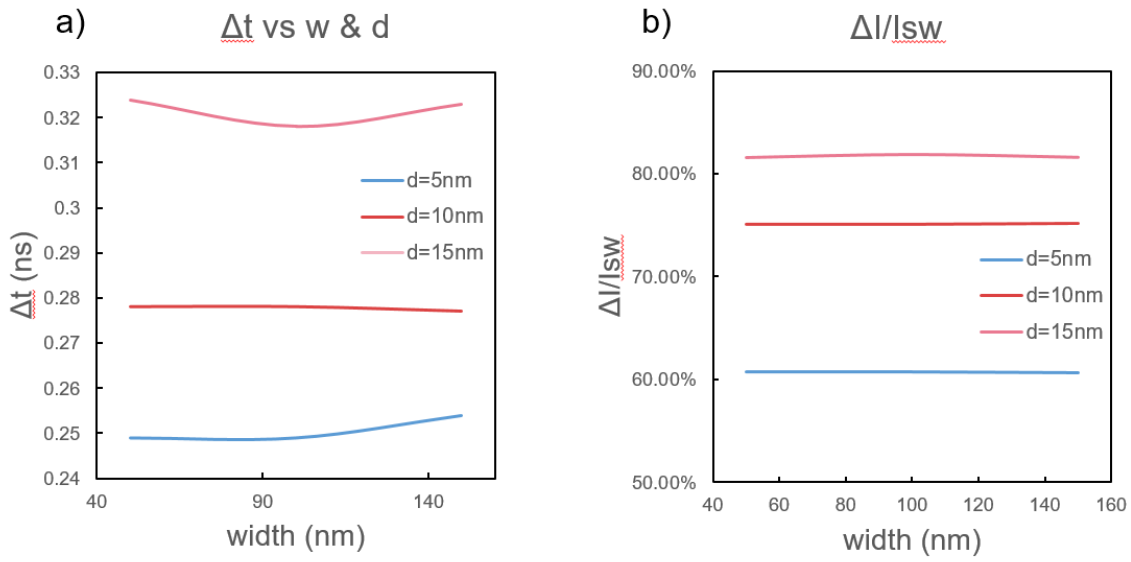


Figure 3.14: Parameter sweeping interlinked

the thickness of the nanowire is the primary parameter influencing performance. As the thickness increases, both Δt and $\Delta I/I_{sw}$ increase significantly. Thus, the effects of various parameters on Δt and ΔI have been clearly demonstrated. Based on these characteristics, we can formulate a design approach for the SNSPD:

1. The length of the nanowire, as it directly determines the value of I_{max}, is critically related to the overall feasibility of the sensor design. Therefore, it should be prioritized when setting design parameters. In cases of poor coupling, the length should be minimized as much as possible without compromising the SNSPD's optical performance. In cases of good coupling, there are fewer restrictions on length. According to equation 3.20, a larger Δt is needed to enhance the effectiveness of active I_b control. A longer nanowire length can be used to increase Δt, thereby improving control over the bias current I_b.
2. As the primary determining parameter for I_b, the thickness d should be decided to set an appropriate ΔI. Based on previous SNSPD test data, the optimal bias current typically lies around $80\% I_{sw}$. Therefore, the goal is to find the thickness that corresponds to $\Delta I = 0.8 I_{sw}$.
3. The width of the nanowire has minimal impact on both ΔI and Δt, but it is directly related to I_{sw}. Within the same I_{snspd} slew rate range, if Δt remains constant, the portion of $\Delta t \times SRf$ actively controllable through the electrical input remains constant. However, by using a smaller width to achieve a lower I_{sw}, the ratio of this actively controllable portion to the total current $\frac{\Delta t \times SR}{I_{sw}}$ increases, thereby expanding the range of active control. Therefore, selecting a smaller width would enhance active control over I_b. However, considering the equation 3.9, which describes that under the same coupling conditions, a larger ΔI can increase the spike that needs to be detected by the readout circuit, a wider nanowire is also desirable. The determination of the nanowire width must therefore balance between these two factors: increasing ΔI for stronger signal detection and optimizing the overall coupling performance.

3.3. Samples Design

This section focuses on the parameter design of the first batch of persistent current SNSPD samples, with which the presented model can be verified and further improved. The design methods discussed in the previous section will be applied to ensure that the samples can provide effective test data.

When considering superconducting loop coupling, flux conservation is only possible when the loop is made of a superconductor. Therefore, when the input coil is made of a conventional metal, the bias operation driven by the input coil may exhibit good coupling. However, when the SNSPD undergoes quenching, the spike generated by the input coil may not follow the large mutual inductance (M) dictated by flux conservation. As a result, the ideality of both biasing and readout will need to be considered separately. The structural parameters of the SNSPD will be designed based on different idealized assumptions.

3.3.1. Case 1 [Ideal bias and readout]

In the most ideal case, the input coil uses superconductor and we get both ideal biasing and ideal detection since the magnetic flux conservation phenomenon is assumed to happen on both the inner and outer loops. In this case, the thickness should be determined by the I_b requirement, multiple numbers would be chosen to make sure a proper I_b could be obtained, based on Figure 3.14. The width should be smaller to increase the potential adjustment range caused by different slew rates, since the large M, in this case, could generate a large enough spike for the readout. There are no special requirements for L_k. For easy driving, a shorter nanowire with a smaller L_k could be better, a relatively small typical value would be chosen.

Possible parameters for samples:

- Thickness: 8nm, 10nm, 12nm
- Length: $500\,\mu\mathrm{m}$
- Width: $50\,\mathrm{nm}$

3.3.2. Case 2 [Ideal bias, non-ideal readout]

In this case, the input coil is made of normal metal (with the lowest possible resistance), because of the need for a multi-turn input coil. Only the bias process benefits from the good coupling, the spike we need to detect would be weak. The thickness should be still determined by the I_b requirement. A large width is needed to generate large I_{sw}, and large ΔI as well since the feasibility of detection is more important than the I_b controlling. A long nanowire is preferred to form a better geometrical coupling with the input coil, so it is set to a relatively large typical value for SNSPD.

Possible parameters for samples:

- Thickness: $8\,\mathrm{nm}$, $10\,\mathrm{nm}$, $12\,\mathrm{nm}$
- Length: $1500\,\mu\mathrm{m}$
- Width: $150\,\mathrm{nm}$

3.3.3. Case 3 [Non-ideal bias, non-ideal readout]

In this case, both the input coil and SNSPD loop would be treated as only having a geometrical inductance. The length of the nanowire should be as small as possible to reduce the I_{max} and reduce the power consumption. Thickness is set the same as above. The width should be large to make detection easier.

Possible parameters for samples:

- Thickness: $8\,\mathrm{nm}$, $10\,\mathrm{nm}$, $12\,\mathrm{nm}$
- Length: $100\,\mu\mathrm{m}$
- Width: $150\,\mathrm{n}$

3.4. Conclusion

This chapter begins with the original idea of the persistent current SNSPD, aiming to establish a model for the SNSPD through theoretical derivation and various simulators. COMSOL simulations and theoretical derivations are employed to explore the magnetic coupling within the superconducting loop, while a basic circuit model is used to clarify the electrical behavior of the SNSPD during operation. A finite element simulator is utilized for precise simulation of the SNSPD's characteristics during quenching. Based on these results, a design methodology for the persistent current SNSPD is proposed, and corresponding sample groups are designed according to different coupling scenarios.

4

Design of the Bias and Readout Circuit

Up to this point, we have explored the physical properties and design methods of persistent current SNSPDs. This chapter aims to explore the optimal structural design of biasing and readout circuits to fully leverage the unique characteristics of a well-designed persistent current SNSPD. As described in Section 3.2.1, the actual coupling efficiency of SNSPD loops still needs to be experimentally verified. The system feature will be investigated in the same condition in Section 3.2.2. The circuit design in this chapter will based on $\frac{I_{snspd}}{I_{coil}} = \frac{1}{10}$ and give considerations for both good and bad coupling scenarios. A TSMC 40nm technology will be used in circuit simulation.

4.1. System features

Figure 3.9 in Section 3.2.2 illustrates the fundamental behaviors required for the biasing and readout circuits of this design: generating current ramps with finite slopes during both rising and falling transitions and detecting spikes caused by quenching events. It is important to note that after quenching, I_{snspd} does not reset to zero, but has some hysteresis and reduces to $I_{residual}$. When the same bias operation is applied again, as shown in Figure 4.1, the increase in I_{snspd} begins from $-I_{residual}$ (where $I_{residual} + \Delta I = I_{sw}$). The increase and decrease in I_{snspd} during the bias operation are identical, as described by Equation 4.1:

$$\begin{aligned} |I_1| + |I_2| &= |I_3| + |I_2| \\ |I_1| &= |I_3| \end{aligned} \tag{4.1}$$

I_{snspd} will quench again and stop at $I_{residual}$, failing to succesfully bias the SNSPD. However, if the polarity of I_{coil} can be reversed during the second bias operation, as shown in Figure 4.2 and Equation 4.2:

$$\begin{aligned} |I_4| + |I_5| &= |I_5| + |I_6| \\ |I_4| &= |I_6| \\ I_b &= \Delta I - I_{residual} \end{aligned} \tag{4.2}$$

the increase in I_{snspd} will start from $+I_{residual}$ and end at $I_{sw} - 2I_{residual}$. When $I_{residual}$ is small, $I_{sw} - 2I_{residual}$ can still serve as a usable bias current, but the system detection efficiency compared to the first detection will be reduced.

In terms of detection, traditional SNSPDs use continuously enabled amplifiers and comparators to capture the spikes generated during quenching and provide accurate time information, as described in Chapter 1. This design can also employ such an approach. However, considering the continuous monitoring power consumption and the adaptation for multi-pixel sensors, a more power efficient approach would be to detect the triggering status of the SNSPD during the previous operational cycle while performing the bias operation.

When detection is only performed during the bias operation, it is necessary to discern whether the sensor was triggered in the previous cycle based on the characteristics of the detected spike. The

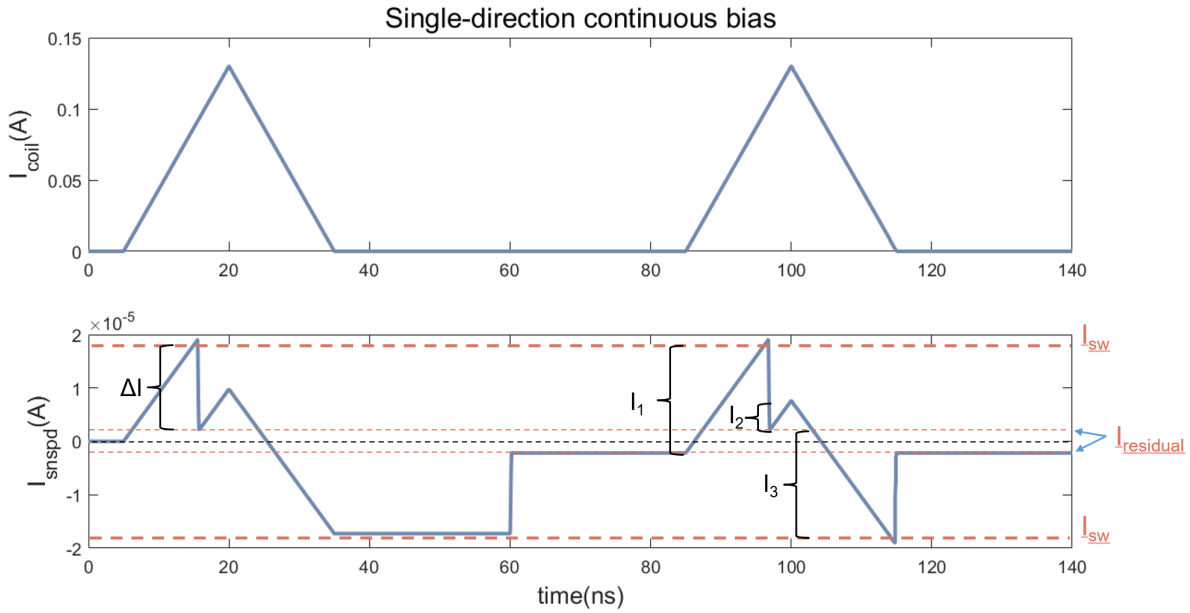


Figure 4.1: Example of single-direction continuous bias

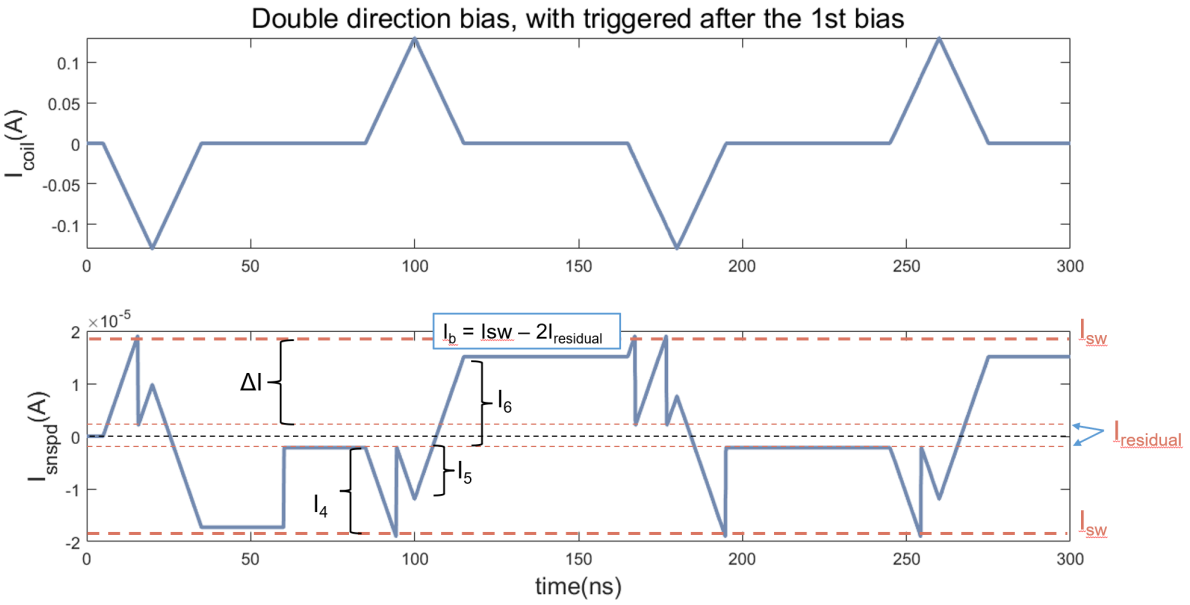


Figure 4.2: Example of double-direction continuous bias

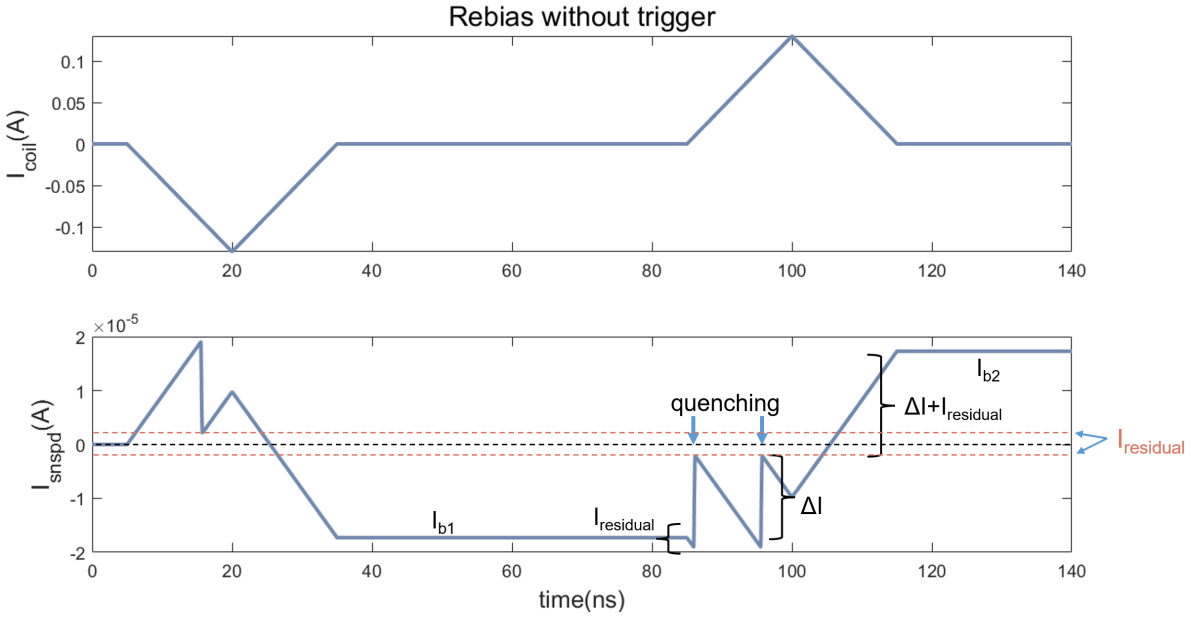


Figure 4.3: Example of rebias without triggered

scenario in Figure 4.2 represents the effect when the sensor was triggered, while Figure 4.3 shows the effect when the sensor was not triggered. If the sensor was not triggered in the previous cycle, the growth of I_{snspd} will start from I_b and increase with $I_{residual}$ after which it will quench, then it will continue increasing with ΔI and quench again given that I_{max} is set appropriately. Consequently, the SNSPD will have the same bias current I_b in the opposite direction, as described by the following equation:

$$I_{b2} = I_{residual} + \Delta I = I_{residual} + \Delta I = I_{b1} \tag{4.3}$$

It can be easily observed that in the case of a rebias without triggering, the first spike is output earlier, and a total of two spikes are generated. This can be used as a criterion for reading out the state of the SNSPD.

Changing of the start point in the current of I_{snspd} can cause more difficult situations with biasing as shown in Figure 4.2. Here, after the SNSPD is triggered in the first cycle and then undergoes a second bias, it will have a bias current of $I_b = I_{sw} - 2I_{residual}$. When performing a rebiasing cycle from this point, the change in current will be $2I_{residual} + \Delta I$, causing it to trigger again when returning the I_{coil} to 0 and causing I_{snspd} to be biased at $I_{residual}$. Fortunately, after a fourth bias cycle, I_b will return to $I_{sw} - 2I_{residual}$. Therefore, an SNSPD that has been triggered will require two bias operations in an empty cycle to be ready for detection again.

Based on the above analysis, the decision logic for the bias and readout circuit is as follows: In a system with a sufficiently long runtime (where the SNSPD has been triggered at least once), after one cycle, if a single spike is detected during the rebias, it indicates that the sensor was triggered within the cycle, and only this bias operation should be performed. If two spikes are detected during the rebias, it indicates that the sensor was not triggered within the cycle. After this rebias, another bias cycle should be performed to ensure the correct bias point.

4.2. SPICE model optimization

As mentioned in Section 3.2.2, the model used for the SNSPD in the circuit simulation is based on the dynamic model in [8], which is designed based on [34] and illustrated in Figure 4.4. In this model, the Drain and Source correspond to the nodes that are connected to the current source and readout amplifier in a conventional SNSPD setup. The kinetic inductance is represented by L_k, and $R_{n,max}$ represents the maximum resistance of the hotspot. The voltage source B_1, which is in parallel with

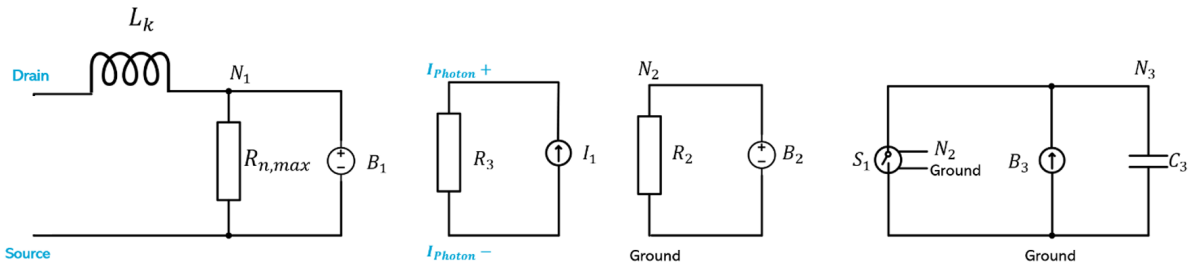


Figure 4.4: SPICE schematic of SNSPD dynamic model

$R_{n,max}$, provides the voltage

$$V_{B1} = \frac{V_{N3} + |V_{N3}|}{2} \times I_{B1} \tag{4.4}$$

representing the increase in the hotspot resistance R_n when the sensor is triggered. The current source I_1 and resistor R_3 are used to mimic a photon event. When I_1 switches from 0 to I_{photon}, and the current in the SNSPD exceeds I_{sw}, the voltage source B_2 will be activated. The source B_2 and resistor R_2 display the SNSPD's state; when the SNSPD is triggered by a larger bias current or I_{photon}, B_2 will switch from 0 to 1. The switch S_1, B_3, and capacitor C_3 simulate the growth of R_n. When B_2 switches to 1, S_1 disconnects, and B_3 begins to charge C_3 with a current shown in equation 4.5. The size of C_3 is also depends on the physical properties of the SNSPD, shown in equation 4.6. The voltage across C_3 is numerically equal to the total hotspot resistance.

$$I_{B3} = \frac{\psi \frac{I_{snspd}^2}{I_{sw}^2} - 2}{\sqrt{\psi \frac{I_{snspd}^2}{I_{sw}^2} - 1}} \tag{4.5}$$

$$C_3 = \frac{w}{2R_{SH}v_0} \tag{4.6}$$

$$\psi = \frac{\rho I_{sw}^2}{h_c w^2 d(T_d - T_s)} \tag{4.7}$$

$$v_0 = \frac{\sqrt{h_c \kappa / d}}{c} \tag{4.8}$$

In equation 4.5, 4.6 and 4.7, I_{snspd} is the current through the L_k. The parameters h_c, κ, c, T_d and ρ are all denpendents on the physical properties of SNSPD; T_s is the substrate temperature; w is the width of the nanowire. Since the primary focus of this project is on the quenching characteristics of I_{snspd}, which are not within the design scope of the original SPICE model, and because we have utilized an SNSPD simulator based on finite element analysis (which offers higher accuracy than this SPICE model), the model requires modification to fit our application better.

In this project, quenching events can be fully described using ΔI and Δt, as discussed in Section 4.1. Since the SPICE model mimics the change in R_n by charging a fixed capacitor with a variable current source, the adjustments should focus on capacitor C_3 and source B_3. As illustrated in Figure 4.5, the relationship between ψ, C_3 and the variations in ΔI and Δt shows that C_3 primarily determines the charging duration, which corresponds to the quenching time Δt, while ψ dictates the final current level at which the quenching stops. Based on this principle, we can independently adjust ΔI and Δt to align them with the performance characteristics observed in the finite elements model. Finally, the parameters of the SPICE model used in this chapter will be set to $I_{sw} = 19\,\mu\text{A}$, $\Delta I \approx 85\% I_{sw} = 16\,\mu\text{A}$ and $\Delta t \approx 3\,\text{ns}$.

4.3. Bias design

The bias circuit of persistent current SNSPD needs to generate a current pulse for the bias coil. Before diving into circuit details, it is essential to clarify the requirements of the bias current I_{coil}. Although the

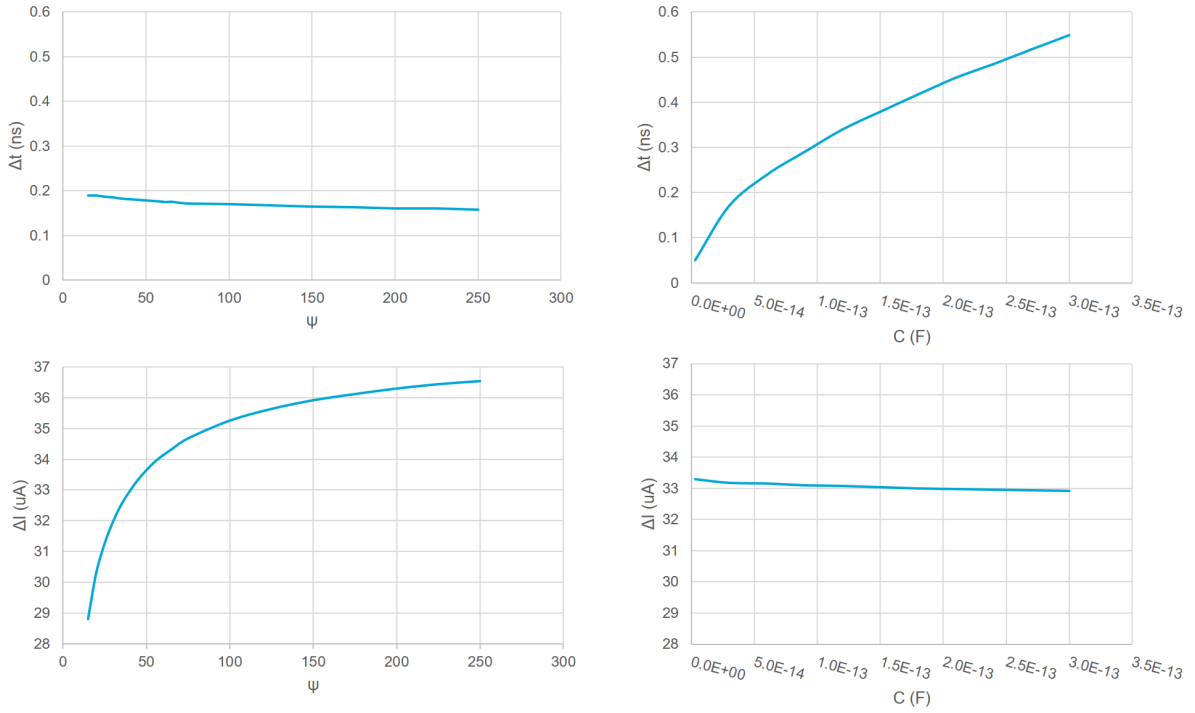


Figure 4.5: Simulated ΔI & Δt as a function of ψ & $C3$, taking $I_{sw} = 38\,\mu\text{A}$ as an example.

basic circuit model shown in Figure 3.9 depicts a linear increase and decrease of I_{coil}, this linearity is not necessary. Since I_{coil} and I_{snspd} always change proportionally, and assuming that the I_{sw} of the nanowire and the current ratio in the two loops can be obtained through testing, the key requirement is that the maximum input current I_{coil} must be sufficient to trigger the sensor.

Given that in this chapter the ratio $\frac{I_{snspd}}{I_{coil}} = \frac{1}{10}$, a current of $I_{coil,max} > 190\,\mu\text{A}$ is required. With a $1.1V$ voltage supply, this would result in a large instantaneous power consumption. The optimal way to reduce power consumption is to increase the slew rate of I_{snspd} and I_{coil}, thereby shortening the time of each operation. However, increasing the slew rate presents two challenges:

1. Excessive Bias Current (I_b): According to Equation 3.20, a slope that is too steep can result in an excessively large I_b, potentially causing additional quenching events that would lead to a failure in biasing the SNSPD.
2. Excessive Voltage on Inductor: As shown in Figure 3.7, the persistent current SNSPD, when not generating a hotspot, presents an inductance slightly smaller than M as its output impedance. A large slope would induce a large voltage across the SNSPD. Since the spike produced during quenching is superimposed on this induced voltage, a larger slope can make the spike more difficult to detect.

Additionally, concerning detection, the quenching-induced spike is output from the SNSPD to the output terminal of the bias circuit. To obtain a clear spike and reduce detection difficulty, the bias circuit should have as large an output impedance as possible.

Summary of bias circuit design requirements:

1. The current should start from zero, increase, decrease, and then return to zero.
2. The slopes of I_{coil} and I_{snspd} should not be too large.
3. The input current I_{coil} should be capable of changing polarity.
4. Power consumption should be minimized.
5. The circuit should have a high output impedance to ensure clear spike detection.

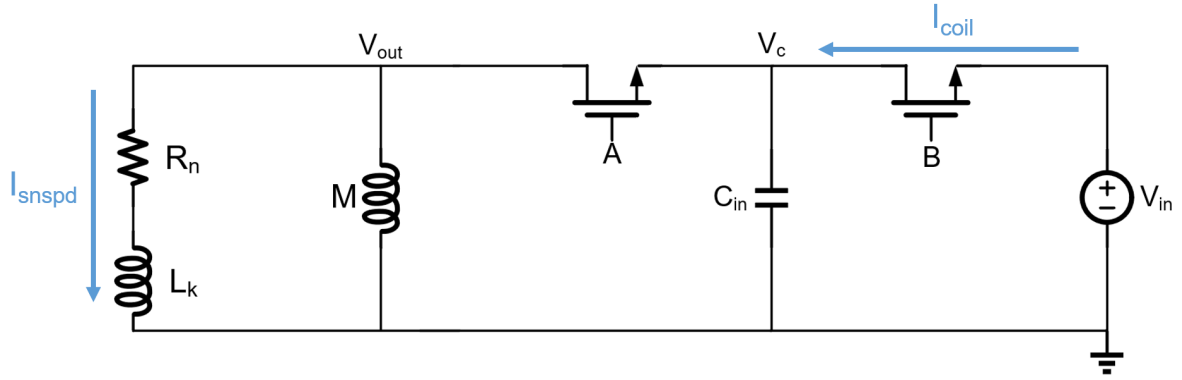


Figure 4.6: LC bias circuit schematic

4.3.1. LC biasing

When a current pulse is required with controlled rise and fall times, independent of parasitic effects, one can use a DAC or passive components (such as inductors or resistors) to extend the rise and fall edges. Given that the current pulse in this design does not carry information and does not need to be modified, passive components should be selected. Notably, the SNSPD, which serves as the load for the bias circuit, inherently exhibits a large inductance ($\approx 73\,\mathrm{nH}$ for $L_k = 800\,\mathrm{nH}$), and this characteristic can be utilized.

A straightforward approach would be to directly apply a fixed voltage across the SNSPD. But for a device with total output inductance $L_{total} = 73\,\mathrm{nH}$, generating $\Delta t \times slewrate < 2\,\mu\mathrm{A}$ (based on equation 3.20) we need a voltage supply that can provide $V_{in} = 0.49\,\mathrm{mV}$ and $I_{coil,max} > 190\,\mu\mathrm{A}$. It would be quite difficult.

A more effective approach would be to use a capacitor that is charged during the detection period to store energy, this allows the voltage supply not to have to output a high current. During the bias operation, this capacitor would be connected to the SNSPD, causing them to oscillate and generate a current pulse. Since the I_{coil} needs to eventually return to zero, the oscillating LC circuit should be interrupted at the precise moment, which requires highly accurate zero-current detection. However, using a switch with a high on-resistance could solve this issue by introducing a low quality factor to the resonator and dissipating the energy.

The circuit is shown in Figure 4.6. Here, the SNSPD is connected to the capacitor C_{in} via the main switch A, which is also connected to the voltage supply V_{in} through switch B. During the detection period, the voltage supply can gradually charge C_{in} to V_{in} via switch group B (or C). During the bias operation, switch B is opened, and switch A is closed, forming a series RLC circuit with C_{in}, L_{total}, and $R_{on,A}$. When $R_{on,A}$ is appropriately set, the circuit achieves critical damping (damping factor, shown in equation 4.10, equals to 1), allowing I_{coil} to quickly return to zero after peaking. After opening switch A and closing switch B, the system enters the next detection cycle

For oscillation in RLC circuit, the current over time is described by equation 4.9. When disregarding damping (with $R = 0$), and assuming $I_{coil,max} = 300\,\mu\mathrm{A}$, we can calculate the necessary C_{in} and V_{in} for different resonance periods, as shown in Figure 4.7. Taking a resonance period of approximately 10 ns as an example, the values of C_{in} are within a reasonable range, but the required V_{in} is very small, and decreases as the period increases, which complicates the design of the power supply. When $R_{on,A}$ is considered, the peak of the RLC oscillation current will be reduced, and the time for the current to return to zero will be longer than the LC resonance period.

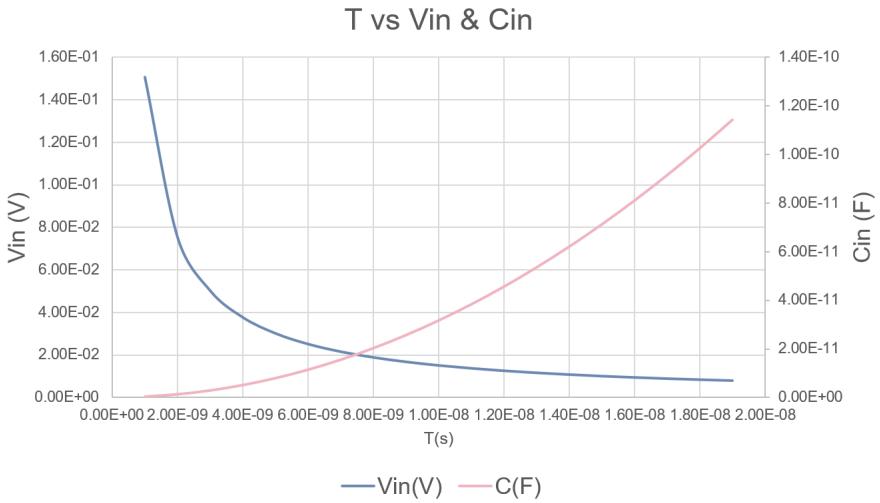


Figure 4.7: Resonance period vs V_{in} and C_{in}

$$
\begin{aligned}
I(t) &= Ae^{-\alpha t}sin(\omega_d t + \phi) \\
\omega_d &= \sqrt{\omega_0^2 - \alpha^2} \\
\alpha &= \frac{R_{onA}}{2L_{total}} \\
\omega_0 &= \frac{1}{\sqrt{L_{total}C_{in}}} \\
A &= \frac{V_{in}}{L_{total}\omega_d d}
\end{aligned}
\tag{4.9}
$$

$$
\varsigma = \frac{R_{onA}}{2}\sqrt{\frac{C_{in}}{L_{total}}} \tag{4.10}
$$

Using the SNSPD model with $M = 80\,\mathrm{nH}$, I_{snspd} decreases by $\Delta I = 0.85 I_{sw} = 16.15\,\mu\mathrm{A}$ over $\Delta t = 0.3\,\mathrm{ns}$ during quenching. As a result, it produces a spike of approximately $4.3\,\mathrm{mV}$, calculated by Equation 3.9. In the RLC circuit, when switch A is closed at $t = 0$, the current's slew rate immediately reaches its maximum, causing the voltage across L_{total} to peak. Figure 4.8 shows this scenario, using ideal components in the simulation. To facilitate the detection of the spike, this voltage should be as small as possible. However, when the voltage across t_{total} at $t = 0$ is around $5\,\mathrm{mV}$, at relatively same level with the spike, C_{in} already reaches $1\,\mathrm{nF}$.

In this example, C_{in} is charged to $5\,\mathrm{mV}$, and release all the energy during bias process. For each bias operation, $\frac{1}{2}C_{in}V_{in}^2 = 1.25 \times 10^{-14}\,\mathrm{J}$ is consumed, not including the voltage supply efficiency and readout part. For bias process time at $50\,\mathrm{ns}$, the average power is $0.25\,\mu\mathrm{W}$, which is extremely low even without considering about the duty cycle of the biasing time and the exposure time. However, from Figure 4.8 we can find that the spike generated by quenching is very small compared to the theoretical value. This might because during the biasing process, the circuit's output impedance is C_{in}, which is not big enough. Alternatively, the readout circuit could be always enabled to ensure detection outside of the biasing process, but this would cancel the low power advantage of this biasing topology.

4.3.2. Current source biasing

To ensure that the circuit maintains a high output impedance during the bias operation, a current source can be selected as the output for I_{coil}. The static current of the current source is set to the desired $I_{coil,max}$. By adding a capacitor to the gate of the transistor, the current source can be gradually turned on and off, resulting in a lower slew rate when the current source is activated or deactivated.

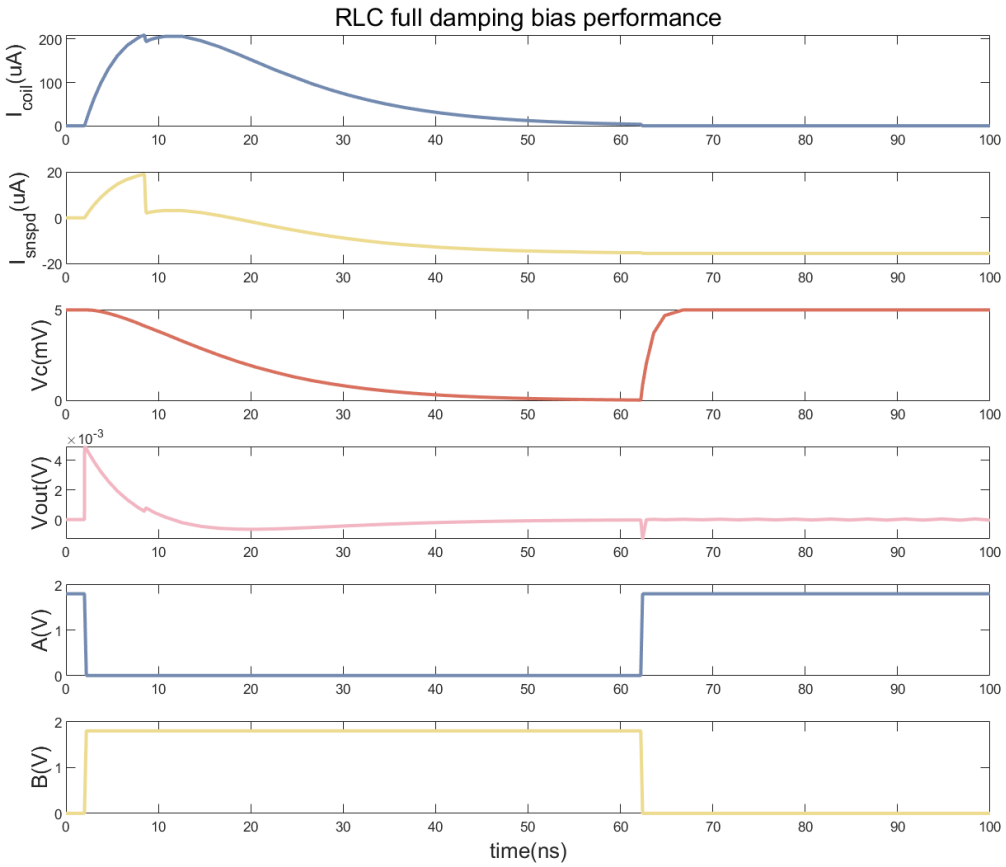


Figure 4.8: RLC full damping bias circuit performance at $C_{in} = 1\,\mathrm{nF}$

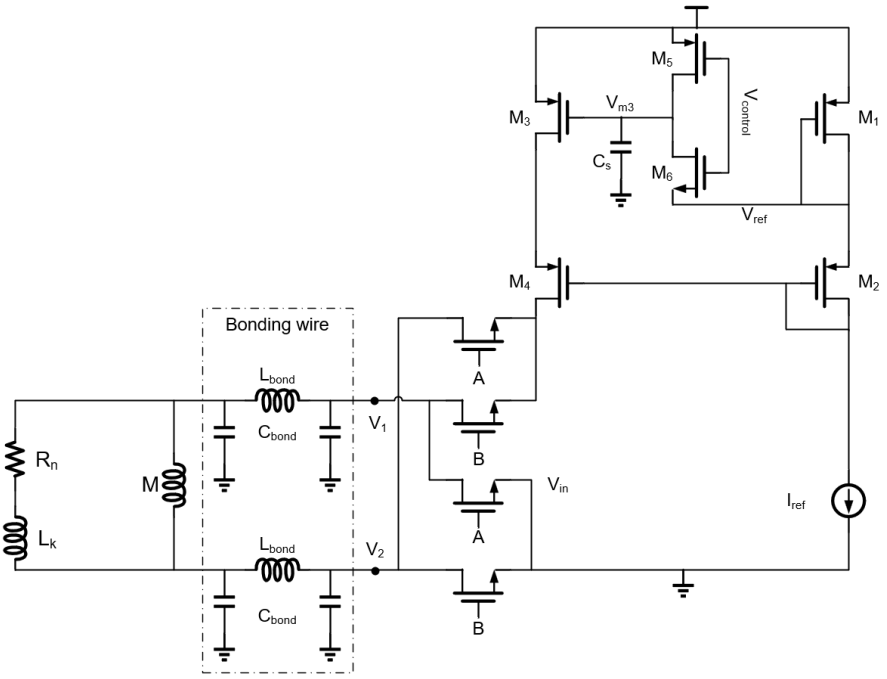


Figure 4.9: Current source bias schematic

The circuit is shown in Figure 4.9. The SNSPD is connected through bonding wires to switch groups A and B, which are used to invert the polarity. Bonding wire represented by a set of capacitors and inductors, with $C_{bond} = 125\,\mathrm{fF}$, $L_{bond} = 2\,\mathrm{nH}$ C_{in} On the right side, M_1, M_2, and M_3, M_4 form a cascode current mirror pair, where the gate of M_3 is controlled by switches M_5 and M_6, connecting to either V_{dd} or the gate of M_1. When $V_{control}$ switches from low to high, the gate of M_3 disconnects from V_{dd} and links to V_{ref}. At this point, the on-resistance $R_{on,6}$ of M6, together with the capacitor C_s, creates a time constant τ that slows the decrease of V_{m3}, causing the current output by the M_3 M_4 current source to gradually increase. When $V_{control}$ switches from high to low, the process is repeated, and the bias circuit's output current gradually decreases to zero. The width of M_3 and M_4 is N times that of M_1 and M_2 to reduce power consumption in the I_{ref} path.

Because C_3 and the on-resistance R_{on} of M_5 and M_6 form a first-order RC circuit, the step response of V_{m3} follows an exponential equation where the current slope rate gradually decreases. When $I_{coil,max}$ is set such that I_{snspd} increases only slightly after quenching, the quenching will occur during the later part of the exponential curve, where the current slew rate is lower, which is exactly what we need. Meanwhile, the higher slew rate in the earlier stage allows the current to change rapidly, reducing the overall pulse width and thereby lowering the energy consumption of each bias operation.

Because the output impedance of the SNSPD is purely inductive, it will cause oscillations with the parasitic capacitance C_{bond} on the bonding wire after each quenching event. To eliminate these oscillations, large resistors need to be added to the circuit to dissipate the energy. The polarity-reversing switch groups A and B are set with a high on-resistance ($800\,\Omega$) to dampen these oscillations. The maximum current flowing through these switches is approximately $230\,\mu\mathrm{A}$, so they would not affect the voltage headroom of the current source.

Figure 4.10 shows a simulation of this design, and Figure 4.11 illustrates the first two cycles of the operation. The simulation was conducted with a switch buffering time constant $\tau = 6.5\,\mathrm{ns}$, resulting in a $3.6\,\mathrm{mV}$ pulse at V_{out} (corresponding to $V_1 - V_2$ in Figure 4.9) induced by L_{total}. This pulse has a smaller amplitude compared to the spike caused by quenching, but a large FWHM (full width at half maximum). This indicates that the spike contains higher frequency components compared to the pulse generated by L_{total}. In the readout circuit, this can be suppressed by using a high-pass filter to improve detection.

Figure 4.10 also shows the transition from the control signal $V_{control}$ to I_{coil}, where V_{m3} follows a stan-

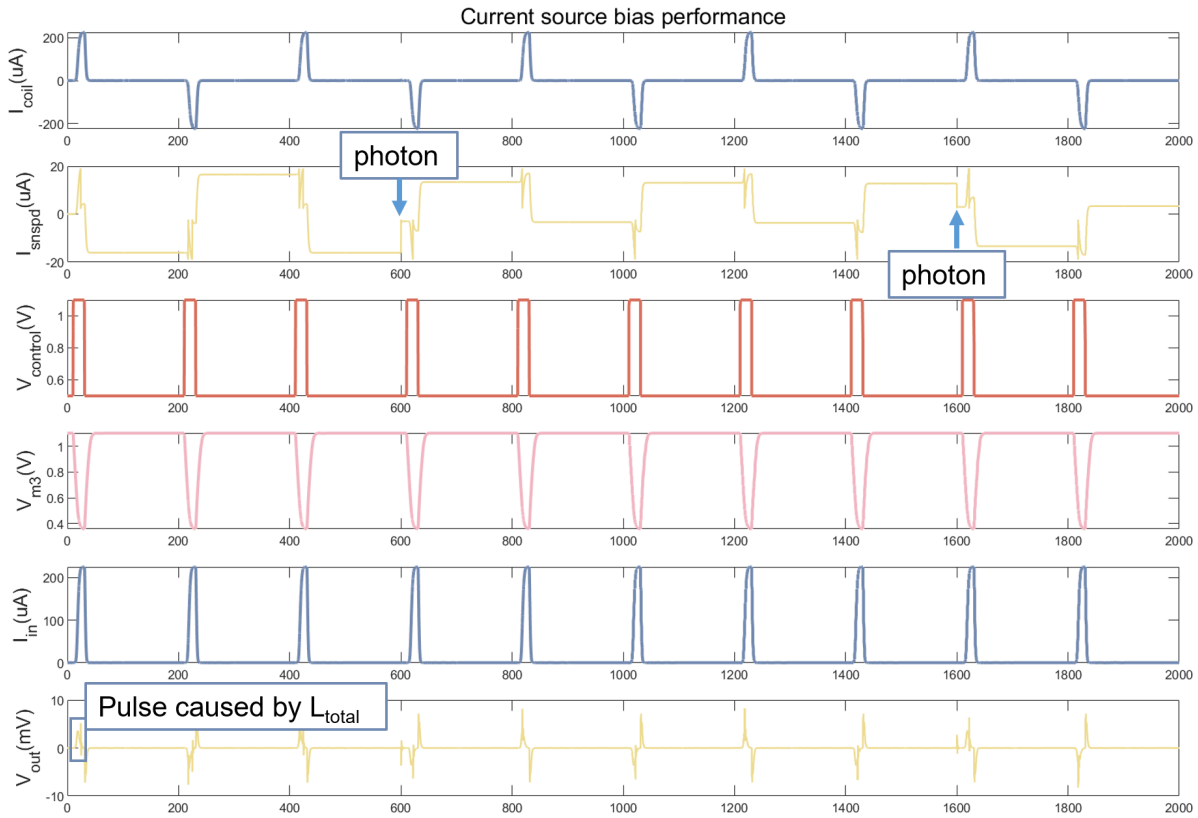


Figure 4.10: Current source bias performance

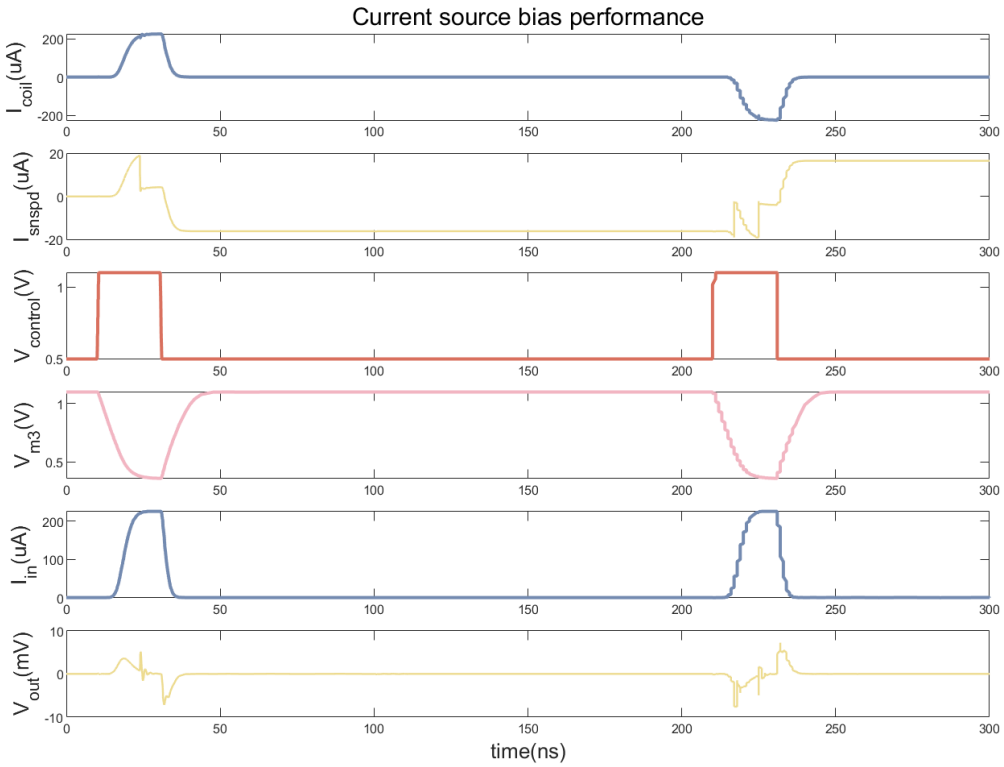


Figure 4.11: Highlight the performance of the system during the first two cycles.

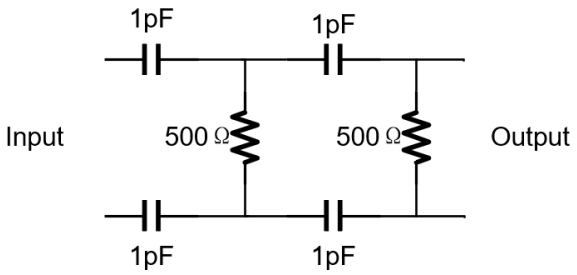


Figure 4.12: 2 cascaded first order RC filters

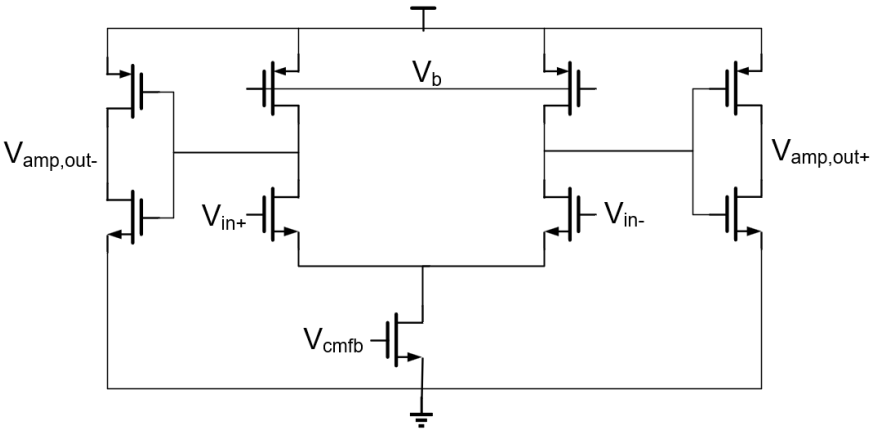


Figure 4.13: Cascade amplifier schematic

dard exponential curve. The current I_{in} (output of the current source) shows some delay and distortion due to the conversion through M_3. I_{ref} is $55\,\mu\mathrm{A}$, leading to an $I_{coil,max} = 230\,\mu\mathrm{A}$, resulting in a peak power consumption of $313\,\mu\mathrm{W}$. A more comprehensive power consumption analysis will be provided in Section 4.5.

4.4. Readout design

An overview of the SNSPD readout can be seen in Figure 4.21. The primary requirement is to amplify the spike generated by quenching in V_{out}, eliminate any remaining oscillation, and perform a comparison for detection. Theoretically, the spike's amplitude and width are approximately $4.3\,\mathrm{mV}$ and $0.3\,\mathrm{ns}$, respectively. However, due to parasitic elements in the circuit, as shown in Figure 4.10, the spike's amplitude and width increase to around $5\,\mathrm{mV}$ and $0.6\,\mathrm{ns}$. Considering the width as half of a sinusoidal signal's period, the frequency range of the spike can be estimated to be around 1 GHz.

Similarly, the voltage pulse originating from applying the bias current on L_{total} has a width of approximately $7.4\,\mathrm{ns}$ and an amplitude of around $3.6\,\mathrm{mV}$, which corresponds to an estimated frequency of about $68\,\mathrm{MHz}$. Using a larger C_s would extend the rising time and result in that pulse at a lower frequency that is easier to be filtered, but also cost more power. To suppress this pulse, a high-pass filter can be considered. Given that the difference between the frequencies is less than two decades, two cascaded first-order RC filters with a cutoff frequency at $1.76\,\mathrm{GHz}$ would be used to ensure filtering, as shown in Figure 4.12, Figure 4.16 illustrate it's frequency response. The filtered and non-filtered V_{out} is shown in Figure 4.17.

Next, the signal is fed into a cascaded, two-stage, differential amplifier as shown in Figure 4.13, which is then fed into an operational transconductance amplifier (OTA), illustrated in Figure 4.14, to sufficiently amplify the spike and convert it into a single-ended signal for input into the digital subcircuit. A common mode feedback using the same 5 transistors OTA is employed to maintain the amplifier's common-mode output at $0.55\,\mathrm{V}$. In this design, the logic gate module has a threshold voltage of approximately

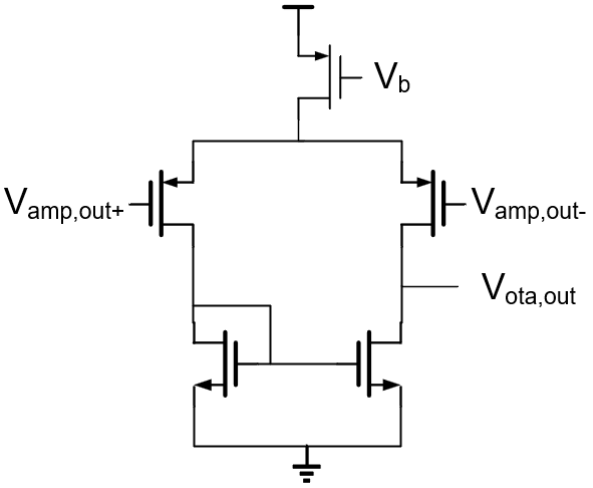


Figure 4.14: OTA schematic

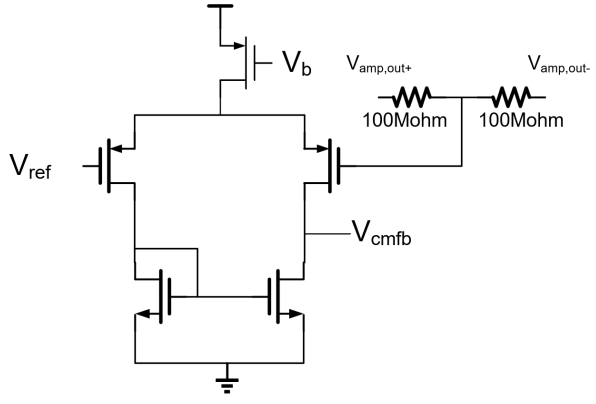


Figure 4.15: Amplifier common feedback

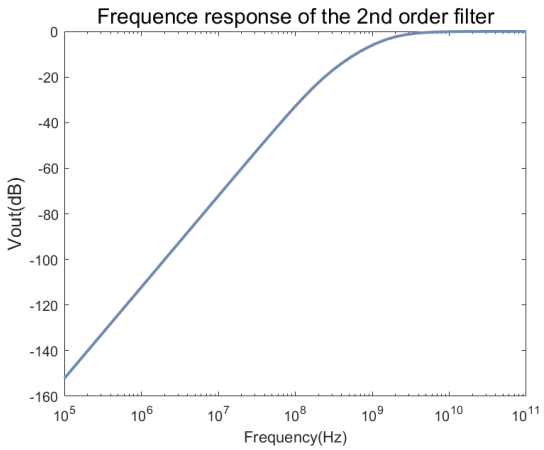


Figure 4.16: Frequency response of the 2nd order filter

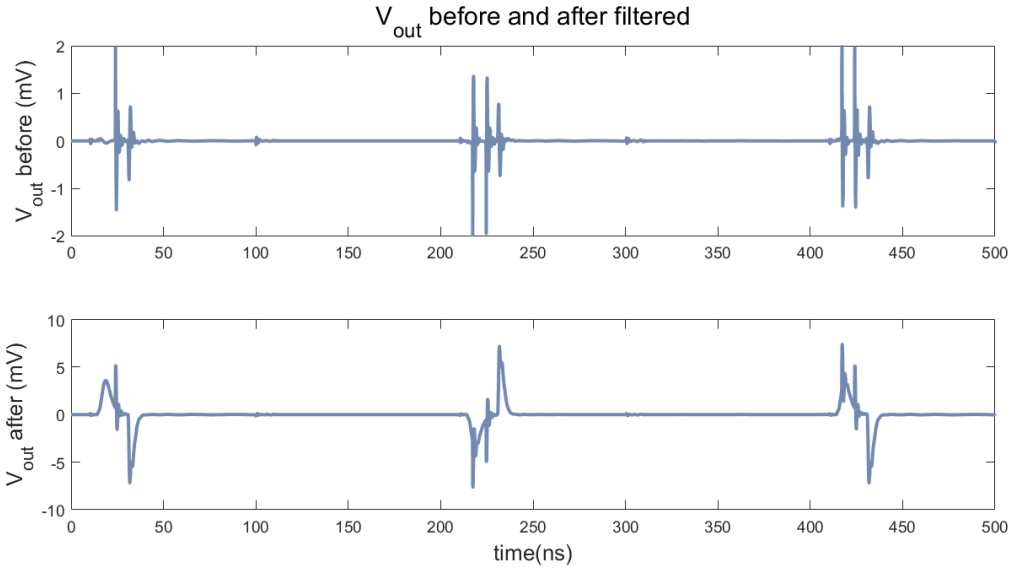


Figure 4.17: V_{out} before and after 2nd order RC filter

$500\,\mathrm{mv}$, so the OTA's steady-state output is set to $600\,\mathrm{mv}$, and it generates a negative pulse greater than $100\,\mathrm{mv}$ upon the spike's arrival to trigger the logic gate. To reliably trigger the logic gate, the required OTA output amplitude is set to $150\,\mathrm{mv}$. As shown in Figure 4.17, the filtered Vout has an amplitude of approximately $1.5\,\mathrm{mv}$, necessitating a combined gain of 40 dB at 1 GHz from the cascade amplifier and OTA. The low frequency pulses are also well suppressed.

In Figure 4.18, the simulated frequency response from the input of the cascade amplifier to its output, as well as to the OTA output, is plotted. The simulation is running at $-40\,\mathrm{C}$. The first stage of the amplifier provides a gain of $21\,\mathrm{dB}$, with the input transistor pair operating in weak inversion to enhance gain. The second stage delivers a $17\,\mathrm{dB}$ gain, with a common-mode feedback circuit made from a five-transistor OTA used to maintain the output common-mode voltage at $500\,\mathrm{mV}$. Due to the use of an inverter (for getting higher transconductance) in the second stage, it is challenging to precisely tune its bandwidth to around $1\,\mathrm{GHz}$, resulting in a lower gain bandwidth. At $1\,\mathrm{GHz}$, the amplifier achieves a gain of $31.8\,\mathrm{dB}$, and the OTA output reaches a gain of $48.1\,\mathrm{dB}$, sufficient to amplify the spike to a detectable level. Figure 4.17 demonstrates that the pulse caused by L_{total} has been suppressed by the filter to approximately $50\,\mu\mathrm{V}$, requiring at least $66\,\mathrm{dB}$ of gain for it to be detectable; thus, this pulse has effectively been eliminated by the readout circuit.

An overall frequency response including the high pass filter, cascade amplifier and OTA is illustrated in

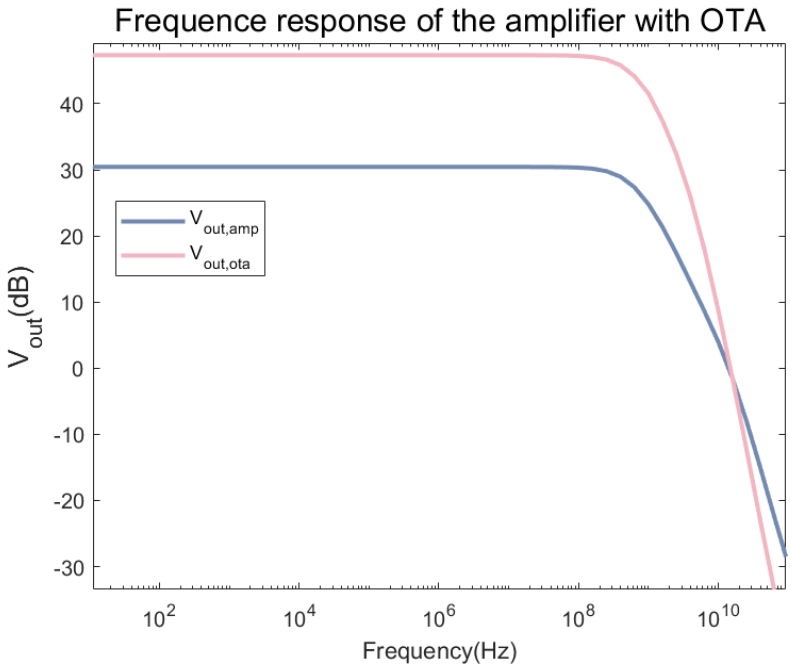


Figure 4.18: Frequency response of the amplifier with OTA

Figure 4.19, showing its effect as a band pass filter which has its largest gain at $\approx 1\,\mathrm{GHz}$.

In the digital logic section, as discussed in Section 4.1, the status of the SNSPD needs to be determined based on the occurrence of spikes during the bias operation. This is accomplished by detecting the timing of the first spike. When an SNSPD has been triggered, its current during bias starts from a lower value, whereas an untriggered SNSPD's current starts increasing from ΔI. Consequently, if the sensor has not been triggered, the spike will occur immediately after the bias operation begins; if it has been triggered, the spike will appear later in the bias operation. Therefore, by detecting spikes only during the first half of the bias operation, the status of the SNSPD can be accurately determined.

An SR latch is used to detect the output of the OTA. As illustrated in Figure 4.20, when the $Latch\_enable$ signal transitions from 0 to 1, the latch starts accepting input signals. Initially, $Latch\_Q$ and $Latch\_Q'$ are set to 1 and 0, respectively. Since the input terminal R is fixed at 1, when $Latch\_in$ receives a 1-to-0 spike, $Latch\_Q$ and $Latch\_Q'$ are set to 0 and 1, respectively, and they will no longer be influenced by $Latch\_in$.

The delay logic, shown in Figure 2.17, is repurposed here. When the bias operation begins, the CLK_{in} port simultaneously receives a signal, causing AQ to transition from 0 to 1. AQ is connected to the SR latch's $Latch\_enable$ to activate it. After a delay of $t_{delay} \approx 0.5t_{rise/fall}$, the delay circuit sets $Latch\_enable$ back to 0, thereby disabling the latch. During the exposure cycle of the SNSPD, the latch, which is in a disabled state, will receive a 0-1-0 pulse at the $Latch\_reset$ input. This pulse acts as an asynchronous reset signal to reset $Latch\_Q$ and $Latch\_Q'$ to 1 and 0, respectively.

4.5. Overall system performance

The overall system schematic is shown in Figure 4.21. we have a $V_{dd} = 1.1\,\mathrm{V}$ power supply and a $55\,\mu\mathrm{A}$ reference current for bias generation. The circuits in this project are designed to explore the feasibility of the structural design rather than to be ready for actual production. Therefore, they have not been fully optimized. All control signals are provided by ideal sources, and the logic described in Section 4.1, which states that "if the sensor was not triggered in the previous cycle, two consecutive bias operations are required," has not been incorporated. The circuit does not yet include compatibility with multi-pixel configurations, but given the characteristics of this design, such compatibility is entirely feasible.

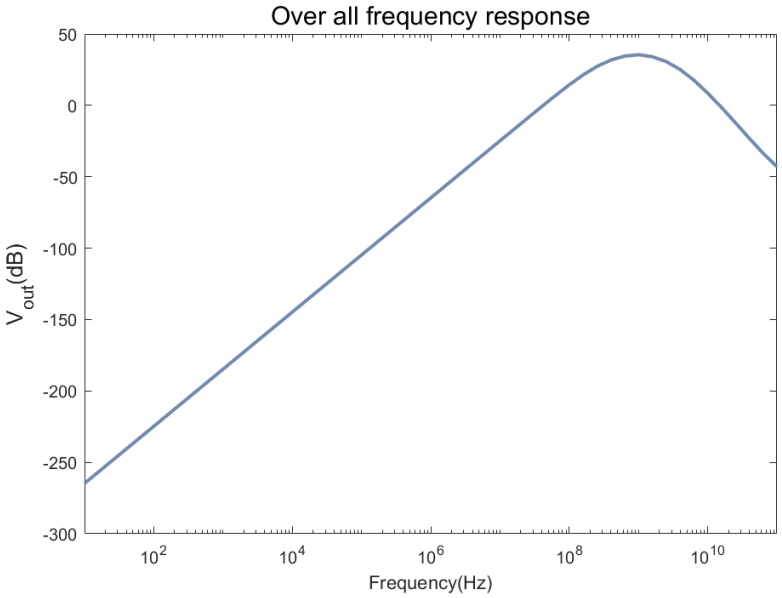


Figure 4.19: Overall frequency response

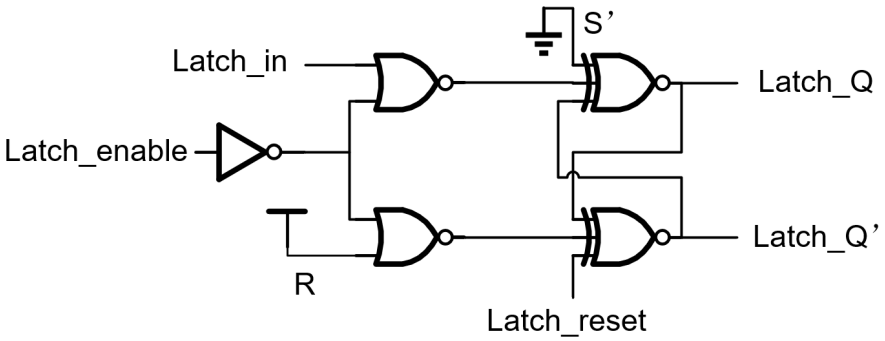


Figure 4.20: SR latch

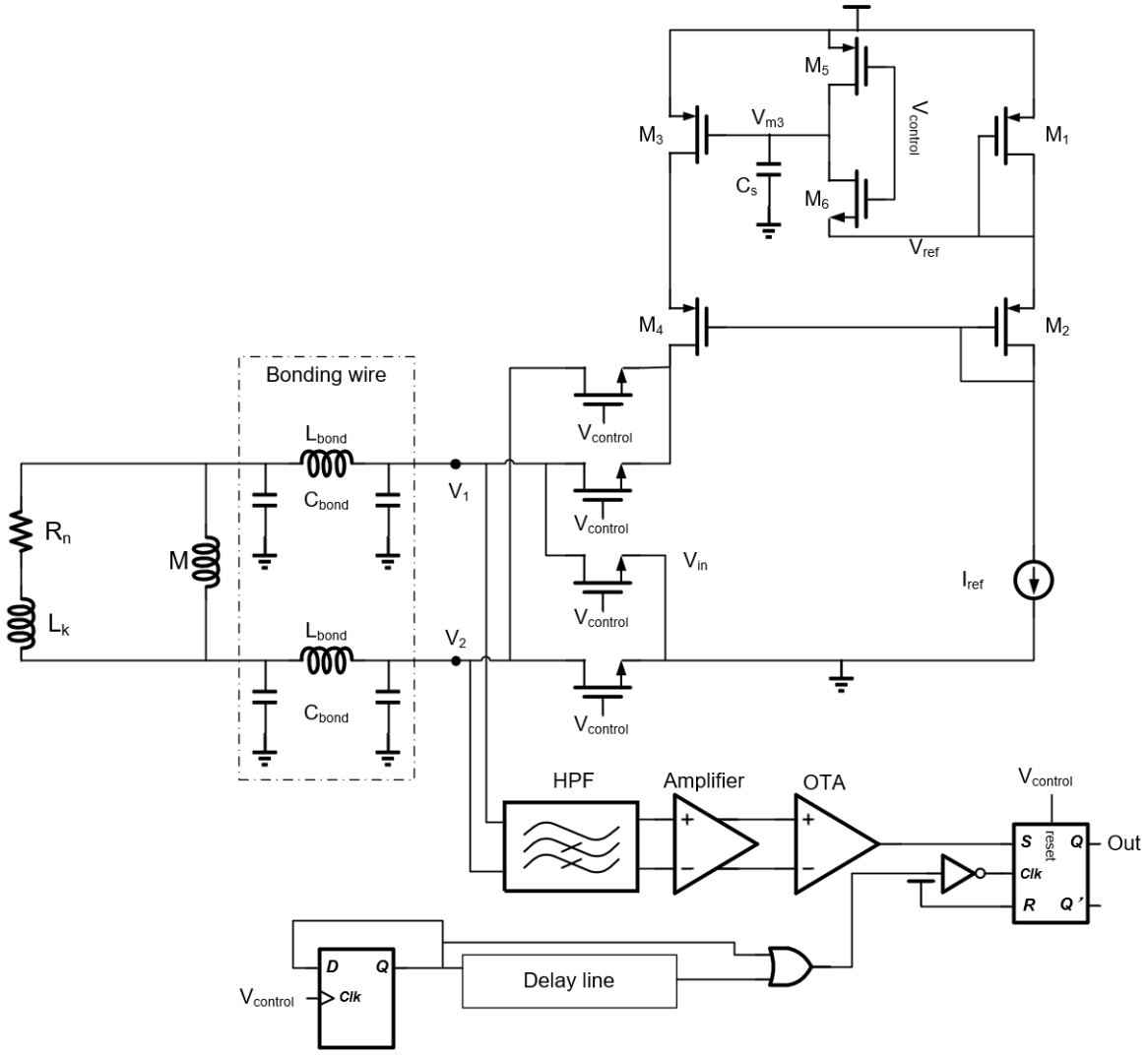


Figure 4.21: Overall schematic of persistent current SNSPD system

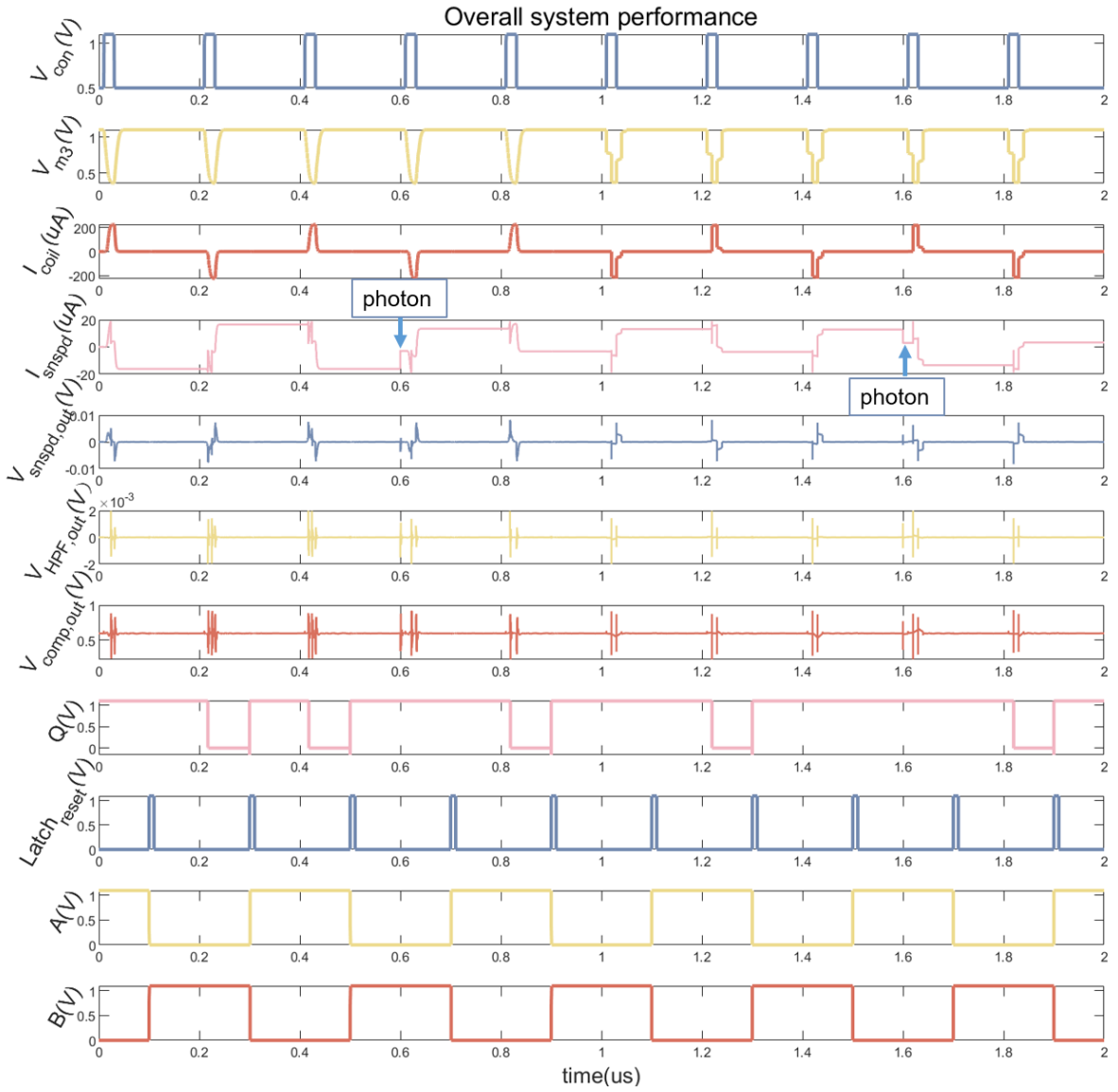


Figure 4.22: Overall performance of persistent current SNSPD system

The bias circuit generates a current pulse with a slow rise and fall edge by employing slow switching, which is used to bias the SNSPD. The spike produced by quenching is amplified by the cascade amplifier and OTA to a level that can trigger logic gates, after passing through a high-pass filter that removes low-frequency pulses generated during biasing by L_{total}. The SR latch detects the spike, and the detection time is controlled by a delay line.

The overall system performance of this design is shown in Figure 4.22, and a highlight of photon incident is illustrated in Figure 4.23. The Q terminal of the SR latch represents the final output result. Upon detecting that the sensor was triggered in the previous cycle, Q switches from 1 to 0 and returns to 1 during the exposure cycle.

Figure 4.24 illustrates the average power consumption of the system's three main components during each cycle, as well as the energy consumption per bias operation for these components, where the "analog sub-circuit" refers to the amplifier and OTA. In Figure 4.24 (a), the highest power is observed in I_{ref} path of the biasing circuit, whose current can be adjusted to some extent. In low-power applications, the biasing circuit and analog sub-circuit do not need to operate during the static state, so an enable control can be added to turn them off during this period to reduce power consumption. In multi-pixel applications, the same biasing and readout circuit are continuously reused by differential pixels, thereby

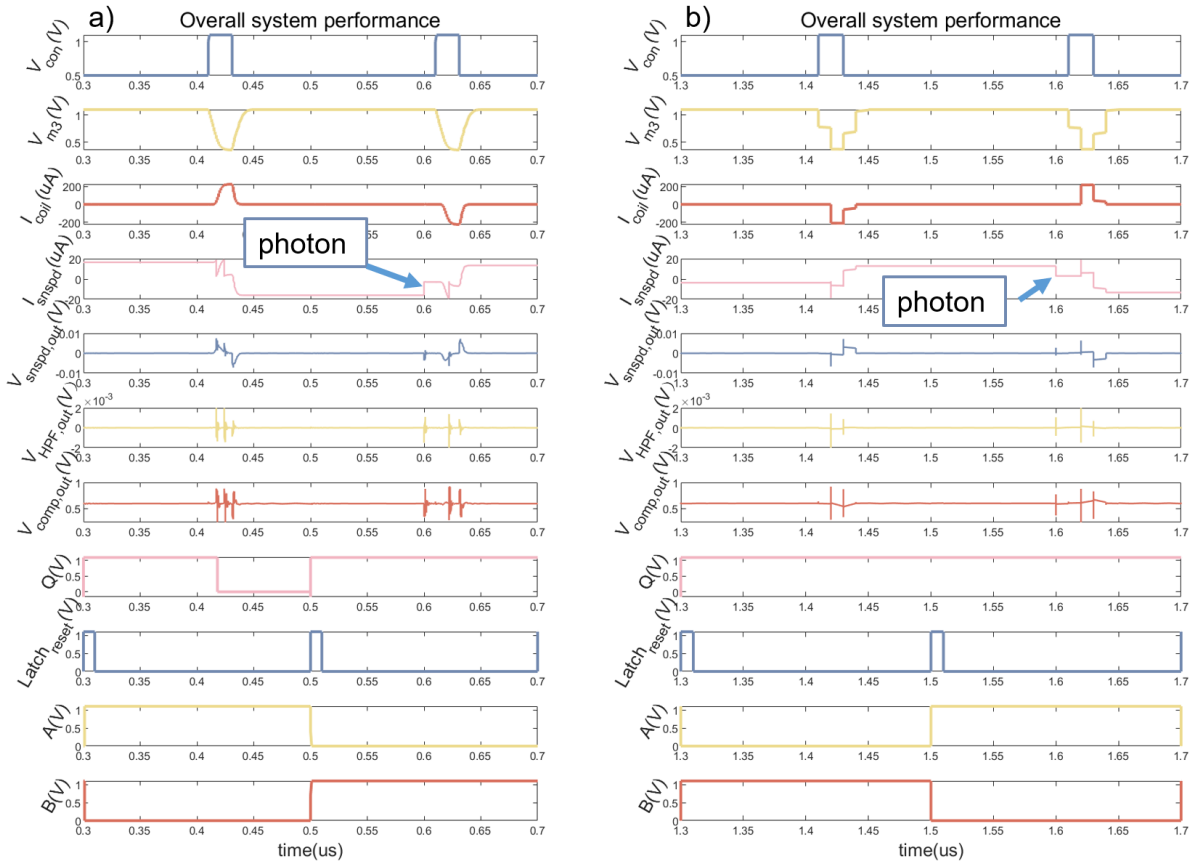


Figure 4.23: Overall performance (a) First photon incident (b) Second incident

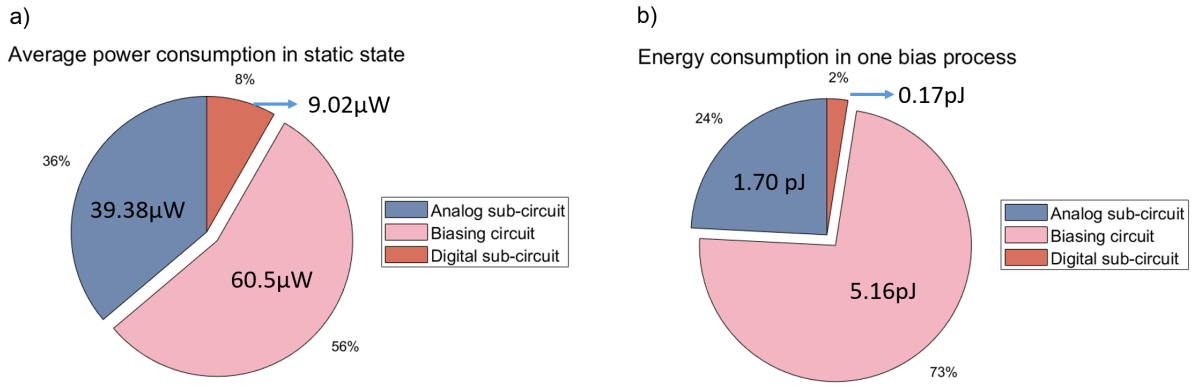


Figure 4.24: Power consumption in (a) static state, (b) one bias process

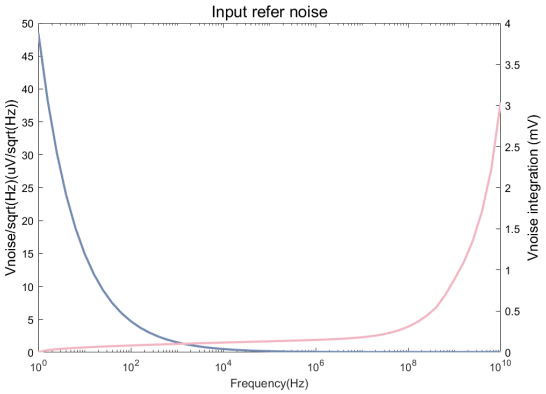


Figure 4.25: Noise performance

avoiding unnecessary power consumption.

In Figure 4.24 (b), the biasing circuit still accounts for the largest portion of the energy consumption due to the high peak power caused by the large $I_{coil,max}$ being drawn directly from Vdd. This can be mitigated by shortening the bias operation time ($30\,\mathrm{ns}$ operation time is used in this calculation).

Now let's consider the system performance under varying coupling conditions. When the coupling approaches an ideal state, I_{snspd}/I_{coil} increases, leading to a decrease in $I_{coil,max}$. This means that the biasing can be achieved with a lower current, resulting in reduced power consumption. As the mutual inductance M becomes larger, the spike generated by quenching will also increase, making the amplifier requirements less stringent. However, it is important to note that L_{total} will also increase under these conditions (in the most ideal scenario, L_{total} will equal L_k). This increment will cause the low-frequency pulse generated by the changing current to have a significantly higher amplitude, potentially requiring a longer bias operation to ensure sufficient voltage headroom.

When the coupling becomes non-ideal, the ratio I_{snspd}/I_{coil} decreases, leading to an increase in $I_{coil,max}$. This necessitates a larger current to drive the SNSPD. In this scenario, the spike generated by quenching will significantly diminish, and may even depend entirely on the geometrical inductance of the two loops. Given the voltage fluctuations caused by parasitic inductance or resistance during the biasing process, any spike superimposed on these fluctuations will be extremely challenging to detect.

A noise simulation encompassing the amplifier, common-mode feedback, and OTA was conducted to investigate the input-referred noise of the analog sub-circuit. As shown in Figure 4.25, after integration, the input-referred noise is approximately 3mV. This results in a signal-to-noise ratio (SNR) of about 14dB when compared to the SNSPD output spike, which is around 15mV (as shown in Figure 4.17.

4.6. Conclusion

In this chapter, we proposed a persistent current SNSPD state detection scheme that combines the quenching characteristics observed in SNSPD current behavior with biasing and outlines the requirements for the interface circuitry. Initially, an LC bias circuit was explored due to its theoretically low power consumption. However, the circuit's low output impedance made it challenging to accurately read the spike signals. Consequently, a bias circuit generating current pulses via a slow-switching current source was implemented using the TSMC 40nm process. In this design, the majority of the power consumption was attributed to the path generating the I_{coil}. To reduce steady-state power consumption, enable controls could be added to each sub-circuit.

5

Conclusion

5.1. Main Conclusion

This thesis proposes and models a novel type of superconducting nanowire single-photon detector (SNSPD) that leverages the characteristics of a superconducting loop. The design aims to utilize the memory-like properties of the persistent current within the superconducting loop to achieve a long-lasting, low-power biasing, while also demonstrating significant potential for arrayed configurations.

The thesis begins by examining the readout architecture of traditional SNSPDs. Through in-depth analysis, it identifies issues in previous designs, specifically the ineffective inversion in the digital sub-circuit of the active quenching structure's delay line, and the unavoidable DC offset drift in the output of the main amplifier. By implementing a new delay circuit logic and switching the main amplifier to a differential configuration, the counting rate was successfully increased to $50\,\mathrm{MHz}$.

In the following chapter, the thesis introduces the concept and operation of using a persistent-current SNSPD and investigates the coupling between the superconducting coil and the input coil through COMSOL simulations. Theoretical derivations indicate that the flux conservation property of the superconducting loop may not hold effectively at the nanometer scale, prompting a detailed discussion of possible scenarios. The establishment of a basic model clarifies the electrical behavior of the sensor. Theoretical calculations reveal that the performance limitations of the SNSPD are primarily influenced by the coupling between the two loops, the length of the superconducting wire, and the parasitic parameters of the input coil. These findings provide a theoretical foundation for the subsequent sample design.

A finite element electrothermal simulator is employed to accurately simulate the variations in SNSPD characteristics under different dimensions and electrical parameter settings. This simulator also identifies factors affecting quenching behavior and methods for adjusting the final bias current, culminating in a comprehensive design approach for the persistent current SNSPD. Based on this approach, three sets of samples suitable for different coupling scenarios were designed.

The circuit for biasing and reading out the SNSPD is then investigated. The biasing can be performed using a capacitor as a battery or by using a current source. While the capacitor would enable lower power consumption, the thesis proposes instead to generate the low slew rate bias current pulses for the SNSPD by using a current mirror. By using a slow-switching approach and leveraging the high output impedance of the bias circuit and the quenching behavior of the SNSPD during biasing, a readout circuit is designed that can detect a quenching SNSPD while filtering bias signals. The overall system achieved successful operation, with the main power consumption occurring in the I_{coil} path. This can be mitigated by reducing the proportion of time spent on biasing within each detection cycle. Power consumption in other sub-circuits can be eliminated by adding enable controls to deactivate them during non-detection periods.

5.2. Further Improvement

As exploratory research on a novel SNSPD structure, this thesis acknowledges that there are several areas requiring further improvement:

1. Fabricate persistent current SNSPD samples and conduct coupling characteristic tests to determine whether the coupling coefficient is solely dependent on the geometric inductance.
2. Test the quenching behavior of SNSPDs with different design parameters to verify the effectiveness of the quenching adjustment methods proposed in this thesis.
3. Design and fabricate a complete circuit incorporating all control logic and enable controls, and conduct tests in conjunction with the SNSPD samples to explore the performance of the full system.
4. Design a circuit multiplexing method for this structure under multiple pixels to enable the array configuration of the sensor.

References

[1] Emma E. Wollman et al. “Kilopixel array of superconducting nanowire single-photon detectors”. en. In: *Optics Express* 27.24 (Nov. 2019), p. 35279. ISSN: 1094-4087. DOI: 10.1364/OE.27.035279. URL: https://opg.optica.org/abstract.cfm?URI=oe-27-24-35279 (visited on 08/24/2024).

[2] Qingyuan Zhao et al. “Superconducting-nanowire single-photon-detector linear array”. en. In: *Applied Physics Letters* 103.14 (Sept. 2013), p. 142602. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.4823542. URL: https://pubs.aip.org/apl/article/103/14/142602/935545/Superconducting-nanowire-single-photon-detector (visited on 08/24/2024).

[3] Qing-Yuan Zhao et al. “Single-photon imager based on a superconducting nanowire delay line”. en. In: *Nature Photonics* 11.4 (Apr. 2017), pp. 247–251. ISSN: 1749-4885, 1749-4893. DOI: 10.1038/nphoton.2017.35. URL: https://www.nature.com/articles/nphoton.2017.35 (visited on 08/24/2024).

[4] Di Zhu et al. “A scalable multi-photon coincidence detector based on superconducting nanowires”. en. In: *Nature Nanotechnology* 13.7 (July 2018), pp. 596–601. ISSN: 1748-3387, 1748-3395. DOI: 10.1038/s41565-018-0160-9. URL: https://www.nature.com/articles/s41565-018-0160-9 (visited on 08/25/2024).

[5] Iman Esmaeil Zadeh et al. “Superconducting nanowire single-photon detectors: A perspective on evolution, state-of-the-art, future developments, and applications”. en. In: *Applied Physics Letters* 118.19 (May 2021), p. 190502. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0045990. URL: https://pubs.aip.org/apl/article/118/19/190502/1062620/Superconducting-nanowire-single-photon-detectors-A (visited on 09/13/2023).

[6] Simone Ferrari. “Inaugural-Dissertation zur Erlangung des Doktorgrades der Naturwissenschaften im Fachbereich Physik der Mathematisch-Naturwissenschaftlichen Fakultät der Westfälischen Wilhelms-Universität Münster”. en. In: ().

[7] Lixing You. “Superconducting nanowire single-photon detectors for quantum information”. en. In: *Nanophotonics* 9.9 (July 2020), pp. 2673–2692. ISSN: 2192-8614, 2192-8606. DOI: 10.1515/nanoph-2020-0186. URL: https://www.degruyter.com/document/doi/10.1515/nanoph-2020-0186/html (visited on 07/03/2024).

[8] Maoran Li. “Cryo-CMOS Readout of SNSPDs”. en. In: ().

[9] Chandra M Natarajan, Michael G Tanner, and Robert H Hadfield. “Superconducting nanowire single-photon detectors: physics and applications”. en. In: *Superconductor Science and Technology* 25.6 (June 2012), p. 063001. ISSN: 0953-2048, 1361-6668. DOI: 10.1088/0953-2048/25/6/063001. URL: https://iopscience.iop.org/article/10.1088/0953-2048/25/6/063001 (visited on 07/03/2024).

[10] F. Marsili et al. “Detecting single infrared photons with 93% system efficiency”. en. In: *Nature Photonics* 7.3 (Mar. 2013), pp. 210–214. ISSN: 1749-4885, 1749-4893. DOI: 10.1038/nphoton.2013.13. URL: https://www.nature.com/articles/nphoton.2013.13 (visited on 05/31/2024).

[11] WeiJun Zhang et al. “NbN superconducting nanowire single photon detector with efficiency over 90% at 1550 nm wavelength operational at compact cryocooler temperature”. en. In: *Science China Physics, Mechanics & Astronomy* 60.12 (Dec. 2017), p. 120314. ISSN: 1674-7348, 1869-1927. DOI: 10.1007/s11433-017-9113-4. URL: http://link.springer.com/10.1007/s11433-017-9113-4 (visited on 05/31/2024).

[12] Iman Esmaeil Zadeh et al. “Single-photon detectors combining high efficiency, high detection rates, and ultra-high timing resolution”. en. In: *APL Photonics* 2.11 (Nov. 2017), p. 111301. ISSN: 2378-0967. DOI: 10.1063/1.5000001. URL: https://pubs.aip.org/app/article/2/11/111301/122783/Single-photon-detectors-combining-high-efficiency (visited on 05/31/2024).

[13] Dileep V. Reddy et al. “Exceeding 95% system efficiency within the telecom C-band in superconducting nanowire single photon detectors”. en. In: *Conference on Lasers and Electro-Optics*. San Jose, California: OSA, 2019, FF1A.3. ISBN: 978-1-943580-57-6. DOI: 10.1364/CLEO_QELS.2019.FF1A.3. URL: https://opg.optica.org/abstract.cfm?URI=CLEO_QELS-2019-FF1A.3 (visited on 05/31/2024).

[14] Dileep V. Reddy et al. “Superconducting nanowire single-photon detectors with 98% system detection efficiency at 1550 nm”. en. In: *Optica* 7.12 (Dec. 2020), p. 1649. ISSN: 2334-2536. DOI: 10.1364/OPTICA.400751. URL: https://opg.optica.org/abstract.cfm?URI=optica-7-12-1649 (visited on 05/31/2024).

[15] Peng Hu et al. “Detecting single infrared photons toward optimal system detection efficiency”. en. In: *Optics Express* 28.24 (Nov. 2020), p. 36884. ISSN: 1094-4087. DOI: 10.1364/OE.410025. URL: https://opg.optica.org/abstract.cfm?URI=oe-28-24-36884 (visited on 05/31/2024).

[16] J. Chang et al. “Detecting telecom single photons with 99.5−2.07+0.5% system detection efficiency and high time resolution”. In: *APL Photonics* 6.3 (Mar. 2021), p. 036114. ISSN: 2378-0967. DOI: 10.1063/5.0039772. URL: https://doi.org/10.1063/5.0039772 (visited on 09/25/2023).

[17] Hiroyuki Shibata et al. “Ultimate low system dark-count rate for superconducting nanowire single-photon detector”. en. In: *Optics Letters* 40.14 (July 2015), p. 3428. ISSN: 0146-9592, 1539-4794. DOI: 10.1364/OL.40.003428. URL: https://opg.optica.org/abstract.cfm?URI=ol-40-14-3428 (visited on 08/08/2024).

[18] Viacheslav Burenkov et al. “Investigations of afterpulsing and detection efficiency recovery in superconducting nanowire single-photon detectors”. en. In: *Journal of Applied Physics* 113.21 (June 2013), p. 213102. ISSN: 0021-8979, 1089-7550. DOI: 10.1063/1.4807833. URL: https://pubs.aip.org/jap/article/113/21/213102/371499/Investigations-of-afterpulsing-and-detection (visited on 07/08/2024).

[19] Sebastian M. F. Raupach, Mariia Sidorova, and Alexej D. Semenov. “Photon number dependent afterpulsing in superconducting nanostrip single-photon detectors”. en. In: *Physical Review B* 108.5 (Aug. 2023), p. 054507. ISSN: 2469-9950, 2469-9969. DOI: 10.1103/PhysRevB.108.054507. URL: https://link.aps.org/doi/10.1103/PhysRevB.108.054507 (visited on 07/08/2024).

[20] Boris Korzh et al. “Demonstration of sub-3 ps temporal resolution with a superconducting nanowire single-photon detector”. en. In: *Nature Photonics* 14.4 (Apr. 2020). Number: 4 Publisher: Nature Publishing Group, pp. 250–255. ISSN: 1749-4893. DOI: 10.1038/s41566-020-0589-x. URL: https://www.nature.com/articles/s41566-020-0589-x (visited on 09/25/2023).

[21] Andrew J. Kerman et al. “Readout of superconducting nanowire single-photon detectors at high count rates”. en. In: *Journal of Applied Physics* 113.14 (Apr. 2013), p. 144511. ISSN: 0021-8979, 1089-7550. DOI: 10.1063/1.4799397. URL: https://pubs.aip.org/jap/article/113/14/144511/689023/Readout-of-superconducting-nanowire-single-photon (visited on 09/13/2023).

[22] Chaolin Lv et al. “Improving maximum count rate of superconducting nanowire single-photon detector with small active area using series attenuator”. In: *AIP Advances* 8.10 (Oct. 2018), p. 105018. ISSN: 2158-3226. DOI: 10.1063/1.5049549. URL: https://doi.org/10.1063/1.5049549 (visited on 09/25/2023).

[23] Qingyuan Zhao et al. “Counting rate enhancements in superconducting nanowire single-photon detectors with improved readout circuits”. en. In: *Optics Letters* 39.7 (Apr. 2014), p. 1869. ISSN: 0146-9592, 1539-4794. DOI: 10.1364/OL.39.001869. URL: https://opg.optica.org/abstract.cfm?URI=ol-39-7-1869 (visited on 09/13/2023).

[24] *Quasi-Gated Superconducting Nanowire Single-Photon Detector*. en-US. URL: https://ieeexplore.ieee.org/document/7820152/ (visited on 09/25/2023).

[25] Prasana Ravindran et al. “Active Quenching of Superconducting Nanowire Single Photon Detectors”. en. In: *Optics Express* 28.3 (Feb. 2020). arXiv:1911.11941 [physics], p. 4099. ISSN: 1094-4087. DOI: 10.1364/OE.383649. URL: http://arxiv.org/abs/1911.11941 (visited on 09/13/2023).

[26] L.J.M. Van De Klundert and H.H.J. Ten Kate. “On fully superconducting rectifiers and fluxpumps. A review. Part 2: Commutation modes, characteristics and switches”. en. In: *Cryogenics* 21.5 (May 1981), pp. 267–277. ISSN: 00112275. DOI: 10.1016/0011-2275(81)90002-3. URL: https://linkinghub.elsevier.com/retrieve/pii/0011227581900023 (visited on 12/08/2023).

[27] T. A. Coombs. “Superconducting flux pumps”. en. In: *Journal of Applied Physics* 125.23 (June 2019), p. 230902. ISSN: 0021-8979, 1089-7550. DOI: 10.1063/1.5098384. URL: https://pubs.aip.org/jap/article/125/23/230902/156148/Superconducting-flux-pumps (visited on 10/19/2023).

[28] Murat Onen et al. “Single-Photon Single-Flux Coupled Detectors”. In: *Nano Letters* 20.1 (Jan. 2020). arXiv:1910.11435 [physics], pp. 664–668. ISSN: 1530-6984, 1530-6992. DOI: 10.1021/acs.nanolett.9b04440. URL: http://arxiv.org/abs/1910.11435 (visited on 10/16/2023).

[29] Murat Onen et al. “Design and characterization of superconducting nanowire-based processors for acceleration of deep neural network training”. en. In: *Nanotechnology* 31.2 (Jan. 2020), p. 025204. ISSN: 0957-4484, 1361-6528. DOI: 10.1088/1361-6528/ab47bc. URL: https://iopscience.iop.org/article/10.1088/1361-6528/ab47bc (visited on 10/16/2023).

[30] John H. Lacy et al. “Superconducting Flux Pump for a Planar Magnetic Field Source”. en. In: *IEEE Transactions on Applied Superconductivity* 30.8 (Dec. 2020), pp. 1–12. ISSN: 1051-8223, 1558-2515, 2378-7074. DOI: 10.1109/TASC.2020.3004768. URL: https://ieeexplore.ieee.org/document/9124694/ (visited on 08/09/2024).

[31] George A. Levin et al. “Persistent current in coils made out of second generation high temperature superconductor wire.” en. In: *Applied Physics Letters* 93.6 (Aug. 2008), p. 062504. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.2969798. URL: https://pubs.aip.org/apl/article/93/6/062504/322980/Persistent-current-in-coils-made-out-of-second (visited on 08/09/2024).

[32] D. J. Thoen et al. “Superconducting NbTiN Thin Films with Highly Uniform Properties over a 100 mm diameter Wafer”. en. In: *IEEE Transactions on Applied Superconductivity* 27.4 (June 2017). arXiv:1609.01526 [astro-ph, physics:cond-mat, physics:physics], pp. 1–5. ISSN: 1051-8223, 1558-2515. DOI: 10.1109/TASC.2016.2631948. URL: http://arxiv.org/abs/1609.01526 (visited on 08/09/2024).

[33] Jacob B Hudis. “PERSISTENT CURRENT DYNAMICS IN ASYMMETRIC SUPERCONDUCTING NANORINGS”. en. In: ().

[34] Karl K Berggren et al. “A superconducting nanowire can be modeled by using SPICE”. en. In: *Superconductor Science and Technology* 31.5 (May 2018), p. 055010. ISSN: 0953-2048, 1361-6668. DOI: 10.1088/1361-6668/aab149. URL: https://iopscience.iop.org/article/10.1088/1361-6668/aab149 (visited on 09/13/2023).

[35] Anthony J Annunziata et al. “Tunable superconducting nanoinductors”. en. In: *Nanotechnology* 21.44 (Nov. 2010), p. 445202. ISSN: 0957-4484, 1361-6528. DOI: 10.1088/0957-4484/21/44/445202. URL: https://iopscience.iop.org/article/10.1088/0957-4484/21/44/445202 (visited on 12/05/2023).

[36] F Villa et al. “Planck-LFI flight model feed horns”. en. In: *Journal of Instrumentation* 4.12 (Dec. 2009), T12004–T12004. ISSN: 1748-0221. DOI: 10.1088/1748-0221/4/12/T12004. URL: https://iopscience.iop.org/article/10.1088/1748-0221/4/12/T12004 (visited on 01/21/2024).