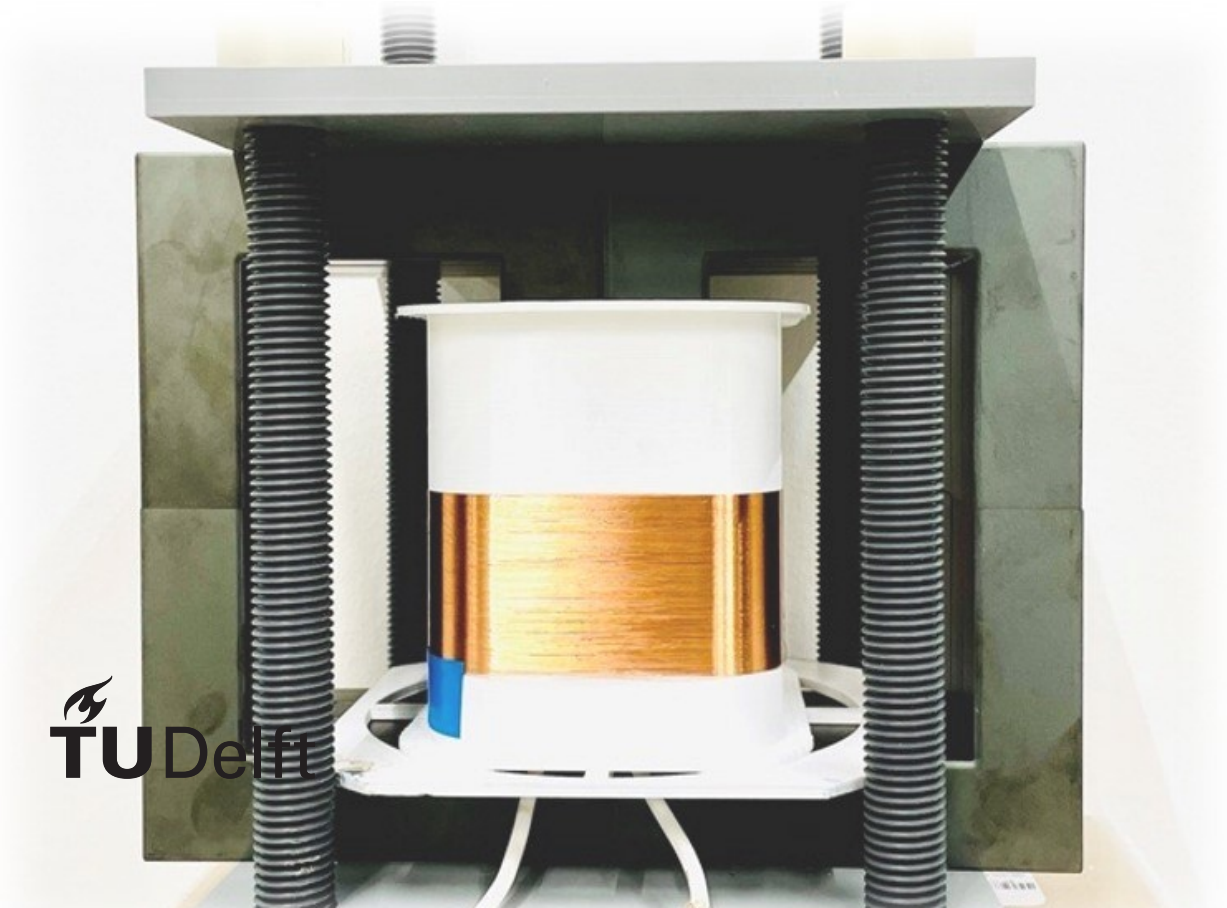
Design and Implementation of a Pulse Transformer and Study on Ageing of Oil Impregnated Paper under Pulsed Stresses

Ravi Kumar Kaparapu



TU Delft

Design and Implementation of a Pulse Transformer and Study on Ageing of Oil Impregnated Paper under Pulsed Stresses

by

Ravi Kumar Kaparapu

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This thesis is confidential and cannot be made public until August 31, 2024.

TU Delft

Abstract

Energy consumption keeps increasing, and more than three-quarters of the EU's greenhouse gas emissions stem from it. Hence, it is important to reduce or stop burning fossil fuels to limit the temperature rise to 1.5°C according to the Paris agreement target. Nowadays, renewable energy sources and distributed generation are increasingly integrated into the electric power system to achieve the ambitious target of the energy transition. Renewable energy sources are inherently fluctuating in their power. Whereas the grid is stable. The interface between these two can be made smooth based on a medium-frequency DC-DC converter. The advantages of increasing frequency are high power density, significant weight and size reduction, dynamic power flow control, and power quality management. All these are possible mainly because of advancements in power electronics in the recent decade. However, these power electronics induce harmonics across insulations, which are fast rising voltages and are repetitive. The dielectric strength of insulations under these fast-rising pulses is to be understood. This thesis project studied oil impregnated paper behavior under pulsed stresses.

To test the Oil Impregnated Paper samples, a source capable of generating repeating pulses with fast rising and lower overshoots is required. This source comprises an AC-DC converter that will power the H-bridge. The pulses from the H-bridge are then fed into a 1:50 pulse transformer to step up the voltage, which is then delivered across OIP (Oil Impregnated Papers) through test components that regulate the pulse's rising time and overshoot. The process began with identifying critical factors to consider while developing a pulse generator. Following that, a random transformer prototype is created along with another transformer to extract the parameters, which are then modeled in the circuit simulator and COMSOL to predict the pulse. An algorithm was created to optimize the transformer design. Finally, this design method creates a pulse transformer that generates the necessary output.

The OIP samples are then tested at frequency $50kHz$ and at various voltages with a rise time $T_r \approx 1.3\mu\ s$. A lifetime curve was obtained using the data of ageing tests at five field strengths. The results showed that the lifetime was reduced with the increase in frequency. At lower fields, a transition was seen, indicating a shift in the ageing process.

Acknowledgements

I want to express my deepest gratitude to my supervisor ***Mohamad Ghaffarian Niasar*** for his motivation and the vast information he shared with me. When a gate driver burned, he used humor to make the surroundings joyful, relieving tension. He was patient even while answering the most simple questions for all of his teaching.

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I am particularly grateful for the assistance provided by our lab personnel. ***Wim*** For meticulously crafting everything required for the project and warning me anytime I violated safety regulations. ***Geert*** for printing all of the bobbins for this project. ***Luis*** for explaining VNA to me and reminding me that there is life outside of the lab.

I am also appreciative to all of the Ph.D. students, particularly ***Tianming*** for his assistance throughout the simulations and patience when instructing. ***Weichuan*** who designed the PCBs for the gate drivers and H-bridge. *Reza*, who fixed several of my issues with gate driver overshoots. ***Dhanashree*** assisted me with the power electronics section. ***Christian*** helped me measure the transformer's capacitances.

Special thanks to my lab mates, who are also my friends ***Ashutosh, Uwais, Nitish, Ayan, and Hassan*** for riding this roller coaster with me and for all the hours we spent in the library helping each other. The most crucial emotional support I received from these friends will never be forgotten.

I could not have started my journey without the encouragement of my family friends ***Akil, Sasi, Vinny, and Swathy*** who also cared for my wife and kid while I was away. I would want to thank my closest friend ***Swathy*** in particular for her positive encouragement while I was feeling down.

Words cannot explain how grateful I am to my wife ***Sarala*** and my daughter ***Sarah*** for living alone for the last two years without bothering me. This accomplishment is also yours, and I will do everything I can to make you proud. Thanks should also go to my ***mother, father, sisters, and brother***, who shaped me into who I am now.

Finally, I thank my mentor, ***Ram Gopal Varma***, who taught me about life and the importance of never giving up.

Ravi Kumar Kaparapu

Contents

1 Introduction

Ageing, break-down tests, and obtaining lifetime curves have been done on oil-impregnated papers for many decades. However, there is an overall lack of research regarding how the oil-impregnated papers behave under fast-rising voltage pulses. This research aims to identify the behavior of oil-impregnated paper under pulsed stresses. This chapter will introduce the study by first discussing the background and context, followed by the research problem, the research aims, objectives and questions, the significance, and finally, the structural outline.

1.1. Context

The electric power grid is the world's most giant man-made machine. The grid is made up of thousands of spinning turbines powered by fossil fuels and wind, many square miles of solar collectors that convert sunlight into electrons, enough high-voltage wires to wrap around the earth eight times, and even more low-voltage wires that reach to the back of our TV and refrigerator. Because we cannot store power on a vast scale, every time someone microwaves popcorn or operates their washing machine, those turbines or solar panels must quickly ramp up their output to keep the massive machine running smoothly[1]. The ability of power systems to maintain stability and to ensure a continuous supply of electrical power to customers in the event of a disturbance is of critical importance[2][3][4]. Unfortunately, unpredictable faults and cascading events usually lead to a blackout which might affect modern life[5]. The insulation system can fail unexpectedly because electric circuits contain fast switching electronic components. For many advantages and freedom offered by Power Electronic switches, power electronics have been incorporated into the grid in the recent past. Power electronics devices can synthesize these power waveforms. However, any new improvement can also cause new problems, and power electronics are no exception. Power electronic devices must operate

at higher speeds to synthesize the power frequency, usually in the kHz range. Because of these speeds, high-speed voltage transients are created[6]. Moreover, due to these transients, the insulation system may fail due to dielectric heating and partial discharges[7].

1.2. Research Problem

A study on dielectrics provides knowledge of particular insulation and how it performs in use. Usually, accelerated ageing will be done, and then breakdown tests will be conducted on aged samples, and then the lifetime of that particular insulation can be predicted[8]. Numerous studies have investigated the behavior of oil-impregnated paper in different environments; some examples are in [9][10][11][12]. However, these studies have traditionally focused on 50-60 Hz power frequency, thermal, humidity, and foreign particles.

Higher frequency applications have had a specific niche for some time, especially in isolated electrical systems like ships, airplanes, and spacecraft. Fast voltage transients are created by network switching and lightning. Nevertheless, these continuous fast voltage transients with high repetition rates are not of concern before including power electronics in the grid. The effect of these transients on oil-impregnated paper is largely unknown.

1.3. The research aim, objectives, and questions

Given the lack of research on the oil impregnated paper under fast voltage transients with high repetition rates, this study aims to investigate the oil impregnated paper under fast pulses and obtain the life-time curves at various frequencies and various voltages.

The research objectives were set as follows:

- **RO1**: To design an H-Bridge along with gate drivers.
- **RO2**: To design and implement a pulse transformer.
- **RO3**: To predict the lifetime of OIP under fast-rising pulses at various frequencies.

The research questions are summarised as:

- **RQ1**: What are the essential factors to consider when selecting a switch and building a gate driver for an H-Bridge?
- **RQ2**: Can the pulse transformer's pulse shape be predicted before manufacturing it?
- **RQ3**: Can Oil Impregnated Paper be used as an insulation in medium-frequency applications?

1.4. Significance

High-capacity Transformers are one of the most expensive and vital elements in a power system [13]. The voltage rating of transformers increases with the distance of transmission. High voltage cables are also used in the power system for its applications. Oil impregnated paper is widely used in high voltage transformers and cables due to its excellent electrical and mechanical performance [14]. The already existing high voltage transformers and cables, because the power electronic devices are incorporating rapidly, these fast voltage transients might degrade their insulation system much faster. With the help of this study, the remaining life of these critical devices can be predicted, and plan outages accordingly. Moreover, the understanding and consensus in designing insulation systems for repetitive fast voltage transients can be achieved.

1.5. Structural Outline

The following is an overview of this thesis.

- The second chapter discusses the fundamental principles of Oil Impregnated Paper, Pulsed Power, and Pulse Generator Topologies.
- Chapter 3 discusses the test setup, the development of the pulse generator, and its testing.
- The pulse transformer is the focus of Chapter 4. It starts with core selection, then describes how to extract pulse transformer parameters, optimize the transformer, and finally build the transformer.
- The fifth chapter discusses the testing of oil-impregnated papers, including the test process, Weibull analysis, and getting lifetime curves.
- Chapter 6 discusses the key findings and future recommendations based on the results.

2

Literature Review

The theoretical understanding of the ideas employed in this thesis will be explored in this chapter. First, a quick introduction to the oil-impregnated paper, its qualities, and ageing will be detailed. The second section will provide a quick review of pulsed power, its applications, and the topologies needed to produce it. This chapter ends with an analysis of the topologies.

2.1. Properties and ageing of Oil-Impregnated Paper

Power Transformers are an essential part of today's electricity grid. A transformer comprises two fundamental components: primary and secondary coils, employed in the basic functioning. Insulation materials are employed to separate these two coils. A sufficient amount of insulation between the transformer's active sections is required for safe operation. Mineral oil and oil-impregnated paper are power transformers' most popular insulating materials. Layers of oil-impregnated paper are wrapped around HV and LV windings[15]. For a long time, cellulose insulation, in conjunction with oil, has served as the primary insulation method for transformers. They have good dielectric strength and acceptable dielectric loss with great flexibility during manufacturing. Paper insulation made from pure cellulose has a remarkable capability of being impregnated with oil, greatly enhancing its insulating qualities.

Furthermore, such solid insulating materials are simple to mould and wrap around coils and may be manufactured in various sizes to meet specific needs. The biggest issue with using dry paper as an insulator is that it is highly hygroscopic (i.e., readily absorbs moisture); also, voids exist since it is a porous material, which causes PD. To compensate for this shortcoming, it must be dried and treated (impregnated) with some liquid (oil, varnish, resins) to limit moisture penetration, remove all air pockets, and retain dielectric strength. These treatments fill the gaps between the fibres and improve dielectric

strength.

Kraft paper is the most often used paper in transformers. Kraft paper is a brown, unbleached paper created from softwood coniferous trees such as spruce and pine[16]. Kraft paper can be thermally upgraded to strengthen its resistance to thermal deterioration. Modifications are made during the pulping process[17]. First, kraft pulp is manufactured from finely powdered wood chips by digesting them with a combination of sodium hydroxide and sodium sulphide, which removes undesirable components such as lignin, polysaccharides, and waxes[18][19]. The pulp is then carefully rinsed with water to eliminate residual chemicals from the process[19]. After that, the individual fibres are crushed and polished to enhance their surface area and reinforce the hydrogen bonds between the cellulose. Following multiple cleaning cycles, the pulp is continually fed onto a moving mesh belt on revolving drums, where paper is produced using both pressing and drying procedures. fig 2.1 shows the Schematic of paper production process[20].

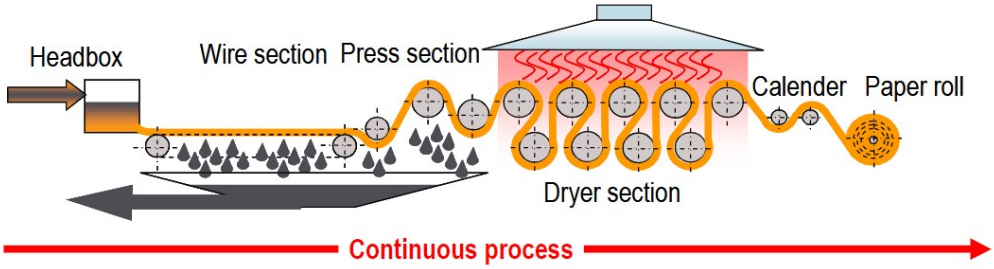


Figure 2.1: Schematic of paper production process[20]

Kraft paper's chemical composition is composed of roughly 95% cellulose. As seen in Fig. 2.2, cellulose is an organic polymer with a molecular structure. The structure in Fig. 2.2 shows the cellulose monomer. This monomer is repeated in long chains to produce polymer cellulose molecules, and polymer molecule chains with lengths of around 1000-1500 monomer units are present in new kraft paper.

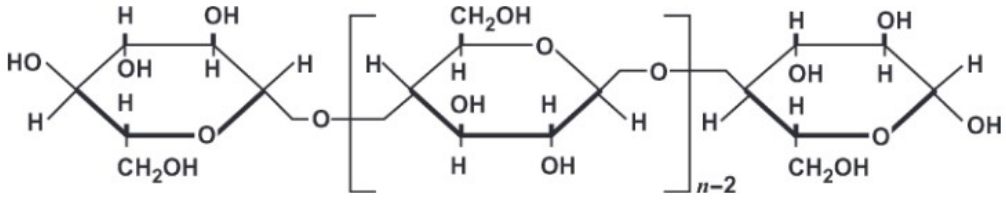
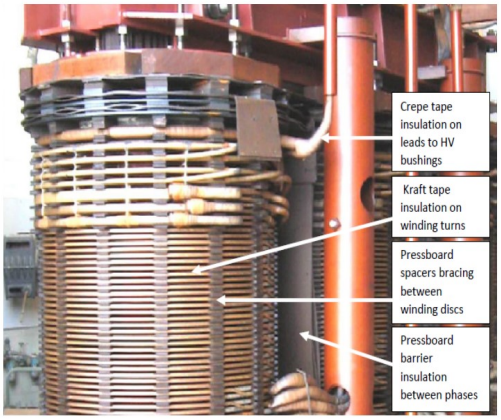
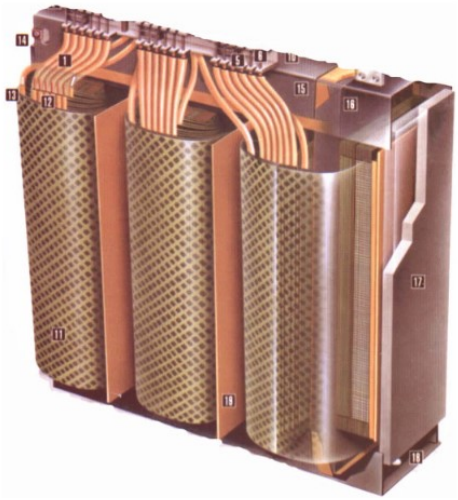


Figure 2.2: Chemical structure of cellulose[18]

Intermolecular linkages are established between neighbouring cellulose molecules in groups of about 2000 molecules in kraft paper. The groups form fibrils, the cell walls of individual paper fibres. The threads are interlaced in a network in the final kraft paper. The fibres and their interwoven network determine many physical qualities of kraft paper, which are significant for their usage in power transformers. For example, the density of the paper network structure can alter its porosity for insulating oil impregnation and mechanical strength[15]. Aside from regular kraft paper, various varieties of paper are used for specific reasons. Thermally enhanced paper, diamond-dotted press paper, crepe paper, and highly extensible paper are examples[19]. Thermally enhanced paper is a form of paper that has a longer lifespan than regular kraft paper. The paper is treated to either minimize deterioration by partly neutralizing the chemicals that cause water or to limit water formation by applying stabilizing agents. Both processes use nitrogen-containing chemicals such as melamine, dicyandiamide, polyacrylamide, acrylonitrile, and others. There is diamond-dotted and crepe paper, which covers special parts such as connections in leads[19]. All these paper's application can be seen in the figure 2.3a,2.3b.



(a) Use of different papers [19]



(b) diamond shaped paper [19]

Figure 2.3: Types of paper used in Transformer

It is commonly understood that paper degrades owing to the interaction of elements such as temperature, water, oxygen, and acids. Paper ageing has been attributed to three distinct mechanisms: oxidation, hydrolysis, and pyrolysis[21]. The chemical changes in the paper due to temperature were first shown by Dakin[22]. He said that the most prevalent type of degradation is gradual oxidation, which inserts acid groups into the insulation, increasing its conductivity and power factors. The oxidation process also breaks apart polymer chains and reduces tensile strength. The degree of Polymerization refers to the number of D-glucose monomers in cellulose fibre (DP). Individual monomers in new

oil-impregnated cellulose generally range from 100 to 1100. At its commonly regarded end of life, cellulose has a DP of 150 to 200[23]. F.M.Clark explained the mechanical deterioration of cellulose insulation. He said significant essential factors are the temperature applied and the presence of oxygen and moisture.

The ”eight-degree-centigrade rule” indicates that the rate of mechanical deterioration doubles for each eight-degree centigrade increase from a base temperature of 120 degrees centigrade[24]. [25] and [26] have conducted recent research on the thermal effects of oil-impregnated paper. Potao Sun [26] explained that the electrical properties of old oil-impregnated paper improved over time. Furthermore, in [27], and [28], it was demonstrated that breakdown strength increased following thermal ageing, which contradicts the common finding for many solid-insulating materials. However, some researchers discovered that the breakdown voltage of OIP samples falls as the ageing time and temperature rise [29]. According to certain researchers, age does not influence the breakdown properties[30][31][32]. The answer for this is given by[26]; he indicated that the breakdown strength is growing due to micro globules that occur in the OIP throughout the ageing process. This modification directly enhances the electric field distribution in the OIP sample, raising the breakdown voltage. The formation of micro globules due to ageing can be seen in the figure 2.4.

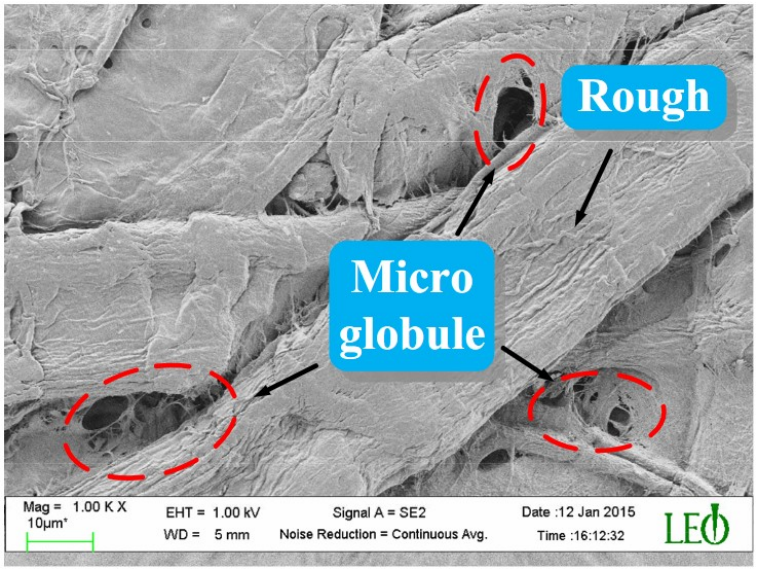


Figure 2.4: Formation of micro globule[26]

The oil-impregnated kraft paper contains a substantial quantity of water, which interferes with the material’s insulating function. The difference in weight between the usual material and the same material after drying is one way of assessing the quantity of water

in the paper. Karl Fisher's approach is another way of determining water. The integrated area of the IR peaks displays the absolute value of the water content in the insulation, making it reasonably simple to quantify the water content in the paper[33]. [34] concludes that when oxygen is present, water in oil production increases with temperature for all papers. For high temperatures, non-upgraded papers produce more water than upgraded papers. Hydrolysis activation energies appear to be greater in non-upgraded paper than in upgraded paper. Niasar in [35] explained the effect of electrical and thermal ageing on Oil Impregnated Paper. A study of PD activity in new and thermally aged papers reveals no significant difference in time to the breakdown between thermally aged and unaged paper. Dielectric spectroscopy on new and thermally aged paper reveals that the imaginary part of permittivity rises for thermally aged paper compared to unaged paper, indicating that PD byproducts created in the cavity irreversibly impact the real and imaginary parts of permittivity.

Few researchers also did work on Oil Impregnated Paper under impulse voltages; for example, in [36] it is mentioned that the breakdown strengths were lower for steep front impulses than for lightning impulses and the breakdown strength can lower than 100 kV/mm. The author in [37] said that if the steepness of the wave increases, breakdown voltage decreases due to a higher rate of change of voltage (dv/dt). However, for varying tail times. The breakdown voltages remain the same. The author in [38] reiterated that due to repeated impulse stresses on oil-impregnated paper, a translucent gelatinous substance was detected, and the colour of OIP changed on the surface. Also, roughness increased by 1.6 times for 200 times lightning impulses. The same author in [39] measured space charge on an oil impregnated paper using pulsed electro-acoustic technique after applying repeated impulses. Charge injection and transport occurred during lightning impulse accumulation. A large number of positive charges accumulated. Only research on impulse stresses is available, but not on continuous pulses, which are critical at this level of power electronics integration into the grid. This will be the focus of this research.

2.2. Pulsed Power

The definition of *pulsed power technology* is the ability to store energy for relatively long periods and then compress and deliver huge power pulses to the load in a short time. As much as the power may be measured in GW, the energy is only available in the ns pulse width range. As a result, while the pulse power might be pretty high, their energy is somewhat modest. The late John Christopher Martin and his colleagues at the Atomic Weapons Establishment planted the root for modern pulsed power in the 1960s[40]. Because the author could not locate an X-ray radiography source of interest, he began creating a new generation of radiography sources based on high-power Marx generators. Thus was the born of modern pulsed power. The four main two-terminal electrical passive components used in pulsed power circuits are resistors, capacitors, inductors, and ideal switches. A closing switch in a pulsed circuit is open at $t < 0$ and short at $t > 0$. A resistor is a device that transforms electrical energy into thermal energy; it does not store

energy. While a capacitor and an inductor store electrical and magnetic energy, respectively. The figure 2.5 describes a broad description of the pulse power subsystem. It is composed of a power source that produces quasi-steady pulses, such as batteries, generators, and fuel cells. For needed pulse formation, there may be one or more stages. At the other end, a dynamic load such as a laser, particle beam, X-ray, or electromagnetic gun is connected[41].

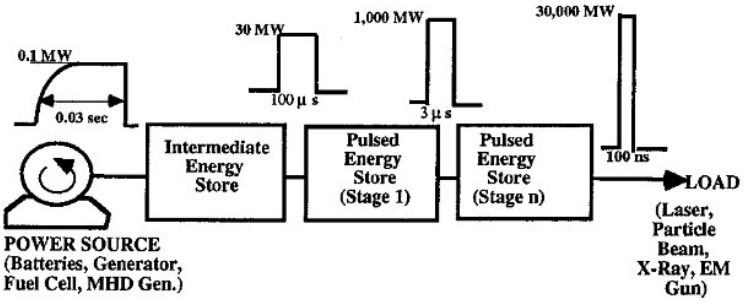


Figure 2.5: General description of pulse power subsystem[41]

2.2.1. Definitions of pulse wave

The terms used for pulse waveform in this study will be discussed here. These definitions are standardised in IEEE standard for pulse transformers [42]. In the figure 2.6 the shape of the pulse waveform is shown with the parameters mentioned.

- **Peak working Voltage:** The maximum instantaneous voltage stress that can occur while operating over the insulation under consideration, including abnormal and transient situations.
- **Pulse Amplitude, A_M:** When a straight line is drawn from 10% to 90% of A_M, and when a straight line is drawn which best fits the pulse top region (visually rather than numerically). The intersection point of these two lines is pulse amplitude A_M. Several approximations may be necessary to determine the A_M for pulses that are not straight on the pulse top.

  The following steps can be followed to get pulse amplitude for pulses deviating from the ideal trapezoidal shape

  - *Step 1:* Draw a best straight line on the top pulse region, then extend this straight line into the leading-edge region.
  - *Step 2:* The first intersection of the pulse with the straight line drawn on the pulse top yields an initial estimate of A_M.

  - *Step 3:* Calculate 0.1 A_M and 0.9 A_M using the estimated A_M and draw a straight line joining these two points.
  - *Step 4:* The intersection of 0.1 A_M and 0.9 A_M straight line and pulse top straight line gives a better estimate of A_M.
  - *Step 5:* Iterate until the estimate does not deviate. This estimate is the pulse amplitude A_M.

- **Rise time, t_r:** In the total time interval of the leading edge, the period between 0.1 A_M and 0.9 A_M is called rise time. In exceptional cases, these limits could change.
- **Pulse duration, t_p:** The time interval between 90% of pulse amplitude A_M on the leading edge and 90% of trailing edge A_T is denoted as pulse duration.
- **Fall time, t_f:** In the pulse trailing edge, the time intervals between 90% of A_T to 10% of A_T is known as fall time.
- **Trailing edge amplitude, A_T:** The straight line drawn on the pulse to estimate pulse amplitude A_M, and a straight line drawn connecting 0.9 A_T and 0.1 A_T. The intersection of these two straight lines is determined as trailing edge amplitude A_T.
- **Droop, A_D:** A droop or tilt is the difference between pulse amplitude A_M and trailing edge amplitude A_T.
- **Overshoot, A_{OS}:** A straight line is already drawn to determine pulse amplitude A_M, and the amount from that straight line to the first maximum of the pulse is called overshoot.
- **Backswing, A_{BS}:** Following the fall time, the maximum amount below the zero axis is determined as the backswing.
- **Return swing, A_{RS}:** Following the back swing, the maximum amount below the zero axis is determined as the return swing.
- **Ringing, A_{RI}:** The maximum that deviates from the straight line drawn on the top of the pulse to determine the pulse amplitude following overshoot is called ringing.

2.2.2. Pulse generators

There exist different types of pulse generators. Some of them are Pulse Forming Network, Pulse Forming Line generators, Marx-generators, Blumlein Line, Generator using power semiconductor devices, and Transformer based systems. The combinations of the above systems will be known as hybrid systems. The optimum modulator type typically depends on the application. Finally, the selected system for this project will be discussed with reasons.

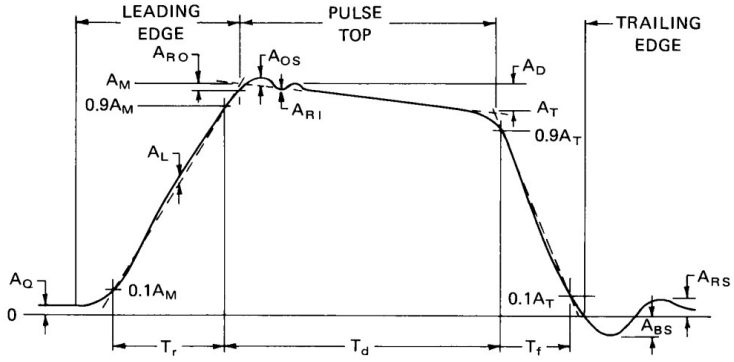
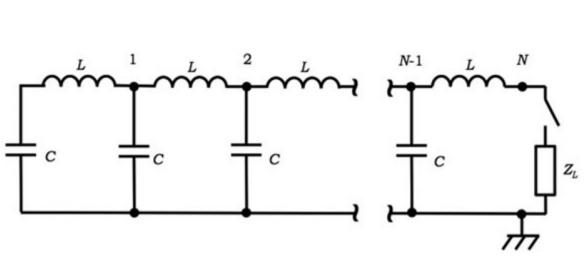


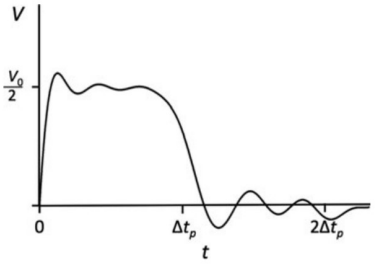
Figure 2.6: Pulse shape [42]

Pulse Forming Network [43]

Transmission line theory enables the Pulse Forming Network. Transmission lines, on the other hand, are only suited for short pulses, generally in the nanosecond range; pulse lengths greater than one second is impracticable. A transmission line, which consists of a finite number of inductor-capacitor units coupled as shown in the picture 2.7a, may deliver a pulse with a nearly constant voltage. PFN is created using discrete element circuits. The transmission line's characteristic impedance is $Z_0 = \sqrt{(L/C)}$. L and C are the network's inductances and capacitances. Figure 2.7b shows the output of the PFN with five elements. Although the output seems to be a regular pulse, there is a significant overshoot at the pulse's leading edge, and an undershoot at the pulse's trailing edge. There is also ringing in the output caused by the coupling of inductances and capacitances. However, the pulse top should be flat for most applications, although wave droop can be permitted. A significant number of components must be connected in the circuit if a somewhat steady output voltage is required. This increases parasitics and slows the wave.



(a) Pulse Forming Network based on Transmission Line [43]

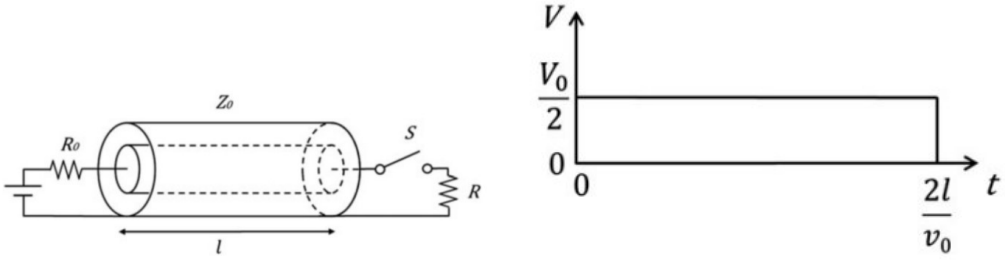


(b) Pulse output of PFN [43]

Figure 2.7: Pulse Forming Network

Pulse Forming Line [43]

Like Pulse Forming Network, Pulse Forming Line is based on a transmission line. It does have a coaxial line with inner and outer conductors separated by an insulator. Figure 2.8a depicts a primary pulse power generator made of a pulse forming line. To ensure 100% reflection of the wave at the supply, the resistance R_0 is significantly greater than the characteristic impedance of the network $Z_0 = \sqrt{(L/C)}$, where L and C are the inductance and capacitance of the coaxial cable. The charging voltage V_0 appears on the coaxial line's inner conductor. The line's characteristic impedance Z_0 is matched to the characteristic impedance of the output load. If the impedances are matched, reflections from the load are avoided, and therefore the amount of energy stored in the line can be transmitted to the load during the pulse. The figure 2.8b depicts the voltage waveform at the load. As the load resistance, $R = Z_0$, a pulse voltage with an amplitude of $V_0/2$ and a pulse width of $2l/v_0$ occurs. The pulse forming line is the most basic pulsed power generator.



(a) Pulse Forming Line Pulsed power generator [43] (b) Voltage Waveform at load R [43]

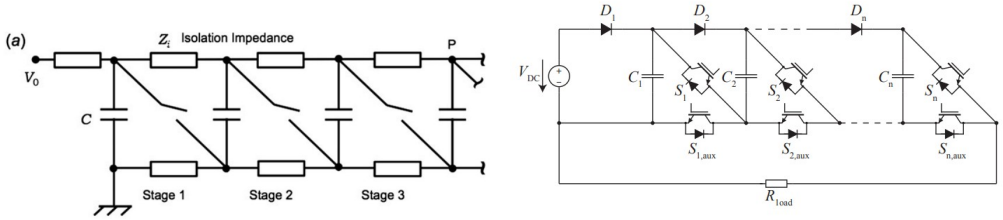
Figure 2.8: Pulse Forming Line

Marx-generators [43]

A pulse can be created using a single capacitor modulator. However, large voltages cannot be created because of the modulator's capacitor tolerance constraints. The greater the voltage required, the greater the insulation required. The Marx-generator, on the other hand, may readily create higher pulse voltages. In these generators, low voltage capacitors can be employed. Figure 2.9a depicts a typical arrangement of a Marx generator. The capacitors in the circuit were charged in parallel at low voltages. They are fired in series after being switched simultaneously. In this series design, the charged voltages of each capacitor add up. The current flows via the isolation resistors when charging, which are open-circuited while discharging.

On the load, the voltage rapidly rises from 0 to NV_0, where N is the number of stages, and V_0 is the charging voltage of each capacitor. The generator's inductance is proportional to

the number of switches. The total capacitance is C/N because the capacitance is proportional to the number of capacitors linked in series. As a result, the overall characteristic impedance increases according to the number of stages. The higher the voltage required, the higher the stages and the impedance, which slows down the output wave. Characteristic impedance can be reduced using high-energy dense capacitors and short connections. The discharge current, however, must pass through inductive spark plugs. Recently, semiconductor power devices have been used in pulsed power modulators; figure 2.9b depicts a Marx generator employing semiconductors. This type can reduce inductance, but the switches must withstand high voltages, which raises the cost. One advantage of the Marx generator is that the voltage may be routed through the diodes rather than having to activate all of the switches at once. In the event of a module failure, the modulator remains active.



(a) Typical Marx generator [43]

(b) Solid state Marx generator [43]

Figure 2.9: Marx Generator

Pulse Transformer based generator

Pulse transformers are used to increase the voltage to hundreds of kilovolts. Pulse transformer works on the Faraday law of electromagnetic induction and Lenz law. High voltages may be created using Marx generators and Pulse Forming Networks; however, as previously noted, they get bulkier as the voltage increases. Pulse transformers, on the other hand, have a compact construction and great repetitiveness. Most applications require a rapid pulse, a wider pulse width, and a high energy transmission efficiency. Magnetic cores with high permeability and saturation magnetic flux densities should be used to achieve this. There are two pulse transformers based on their operating conditions: single pulse and repeat pulse.

The former seeks high pulse voltage and massive pulse current, whereas the latter seeks high frequency and high average power. The downside of a pulse transformer is that it cannot create a pulse on its own. Thus it must be fed a low voltage pulse. On the other hand, the pulse transformer has a compact construction and a tiny volume. Figure 2.10 shows the schematic representation of a pulse transformer application. In pulsed power applications, pulse transformers are often step-up transformers with a large number of turns on the secondary winding; this high turn ratio, together with the gap maintained

between the primary and secondary windings, increases the parasitic elements. With the energy stored in magnetic and electric fields, leakage inductance and distributed capacitance may be estimated. The parasitic components must be minimized to transmit the voltage with the least amount of pulse distortion, particularly during the rising time. The mechanical parameters of the transformer, i.e. the spacing, heights, and lengths of the windings, can be varied to reduce parasitic components; this will be covered in depth in chapter 4. These parasitic elements contribute to overshoot and oscillations and increase the pulse rise time. As a result, extreme caution is required while designing a pulse transformer.

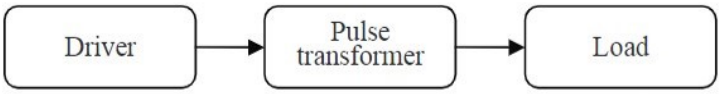


Figure 2.10: Schematic diagram of application of pulse transformer [44]

Pulse transformer-based modulators can be divided into two types: those with a single core and those with multiple cores. One magnetic core and multiple windings can be present in a single-core transformer. The two windings are coupled through the magnetic core with μ. The primary and secondary voltages for the transformer with cross-section area A_C are

$$v_p = -\frac{d\psi_P}{dt} = -N_P \frac{d\phi_p}{dt} = -N_P A_C \frac{dB}{dt} \tag{2.1}$$

$$v_s = -\frac{d\psi_S}{dt} = -N_S \frac{d\phi_S}{dt} = -N_S A_C \frac{dB}{dt} \tag{2.2}$$

If the core is considered ideal, the permeability $\mu \rightarrow \infty$, the flux density B is constant on both windings. Equation 2.1 and equation 2.2 can be solved to

$$\frac{v_P}{N_P} = \frac{v_S}{N_S} \tag{2.3}$$

The primary current and secondary current are derived by Ampere's law:

$$N_P i_P - N_S i_S = \oint_C \vec{H} dl \tag{2.4}$$

Where C is the closed integration path of the core. With ideal condition $\mu \rightarrow \infty$, the magnetic field intensity H becomes 0 and hence

$$N_P i_P = N_S i_S \tag{2.5}$$

2.2.3. Topology Analysis

The Pulse Forming Network and Pulse Forming Line are pulse generators that use transmission line theory. There is substantial overshoot in the pulse forming network and ringing at both the leading and trailing edges. This phenomenon can be mitigated by increasing the number of stages of inductor-capacitor components; however, this raises the cost. Increasing inductors and capacitors may help to decrease overshoot and ringing. However, when the inductances and capacitances in the circuit rise, additional parasitics can be introduced, making the pulse slower, which is not advantageous for the application of this work. The pulse width cannot be increased beyond a few nanoseconds in the pulse forming line. Because the materials employed should have a low permittivity, the length of the coaxial cable should be increased to create larger pulses, making the setup bulkier. Although the pulse forming line is a simple generator, it cannot be employed since manufacturing repeated pulses is difficult. It is feasible to reduce the size of PFL by employing de-ionized water as an insulator material and by adopting non-coaxial forms. Even with these strategies, the pulse width can only be somewhat improved. Marx generators may create quick pulses and a high repetition rate when solid-state switches are utilized.

Nevertheless, the building of the Marx generator is hard to adapt to this application. Finally, a solid-state feed pulse transformer can generate pulses with a high repetition rate and the ability to modify the pulse. The parasitics of the transformer should be minimized to produce quicker pulses. The computation of parasitics and how to reduce them will be covered in Chapter 4.

3

Pulse Generator

Three crucial factors are required to meet the research aims of this thesis. The pulse generator, which supplies low-voltage pulses to the pulse transformer, comes first. Second, a pulse transformer raises the pulse voltage to a sufficient level for testing. Finally, the oil paper samples were tested to determine their ageing under these high-frequency pulses. The whole test topology will be explained first in this chapter, followed by the pulse generator. The pulse generator aims to produce quick, low-voltage pulses with little noise. Because parasitics are an issue when building a pulse transformer, the pulse generator output must be quick and free of ringing. This chapter discusses switch selection as well as the H-bridge with gate driver. Finally, the critical considerations to be taken in a gate driver circuit to attain the output for this particular application will be discussed.

3.1. Test setup

The test setup is shown in the picture 3.1. It begins with an alternating current source and is connected to an AC/DC converter. The output of the rectifier contains ripples. They are minimized by using a DC link capacitor. At this point, a DC supply is given to the H-bridge, which has four switches, as shown in the picture. With appropriate dead time, gate drivers control each switch's gates. In this setup, an Arduino uno microcontroller is used to provide control logic to the gate drivers. The output of the full bridge inverter is a series of sharp pulses with a frequency determined in the MCU. These sharp pulses are fed into a pulse transformer with a 1:n turn ratio. The voltage is increased by n times the pulse input. This pulse transformer output voltage is used to test the oil paper samples, shown as a capacitor in the diagram. The pulse rise time and overshoot can be controlled by two variable passive components, R_t, and C_t [45].

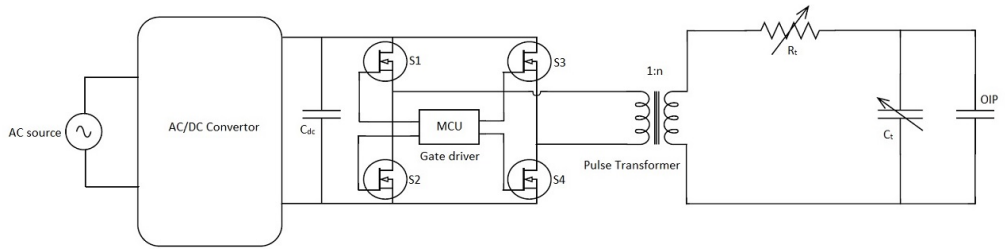


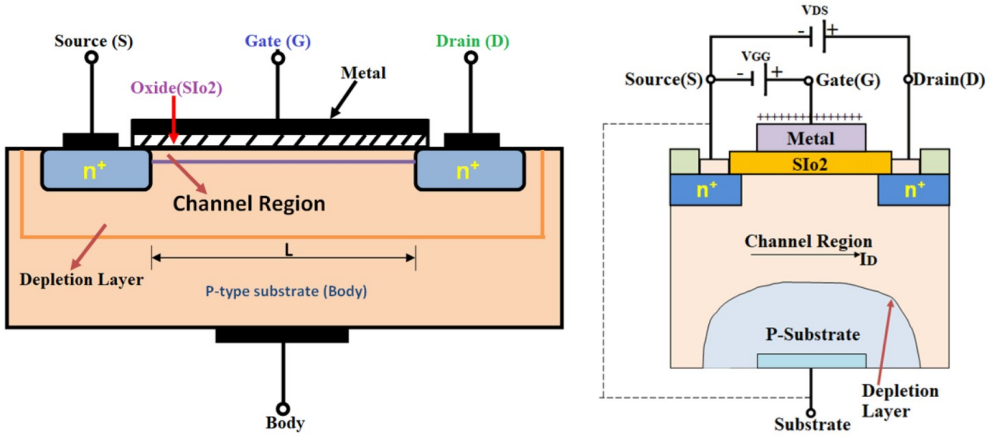
Figure 3.1: Test setup

3.2. Switches

3.2.1. MOSFET theory and mechanisms

Several switches such as BJT, IGBT, SCR, TRIAC, and MOSFET are utilized in power electronics. BJT is the most fundamental of them all. MOSFET is the most common type of power switch, followed by BJT. MOSFETs can handle higher power levels compared to BJTs. As a result, it is popular in high-power applications. It solves the drawbacks of FETs, such as high drain resistance, moderate input impedance, and slower operation. MOSFETs are voltage-controlled devices; when a voltage is supplied to the gate, it begins to conduct through the Drain to the Source pin. MOSFETs have three terminals: Drain (D), source (S), and gate (G). They are classified into several categories based on their manufacture and function. The N-channel MOSFETs are the most commonly used [46].

Knowing the basic operation of a MOSFET requires first understanding its construction. The figure 3.2a depicts the MOSFET's internal construction. The gate terminal is attached to a thin metal layer shielded from the semiconductor by a layer of Silicon Dioxide (SiO2). The MOSFET's drain and source are connected to two N-type semiconductors installed in the channel area. Figure 3.2b depicts the MOSFET block diagram. MOSFETs are typically used as switches. The MOSFET regulates voltage and current via the drain and source. When voltage is applied to a semiconductor surface between the source and drain, it acts as a capacitor, also known as a MOS capacitor. A MOSFET may be converted from p-type to n-type by providing a positive or negative gate voltage. When a positive voltage is connected to the drain and a negative voltage is applied to the source, the PN junction at the drain is reverse biased, and the PN junction at the source is forward biased. No current will flow between the drain and the source. When we apply a positive voltage (V_{GG}) to the gate terminal, the minority charge carriers (electrons) in the P substrate begin to gather on the gate contact, forming a conductive bridge between the two n+ areas owing to electrostatic attraction. The quantity of free electrons collected at the gate contact is determined by the strength of the supplied positive voltage. The larger the applied



(a) Internal structure of MOSFET [46]

(b) Block diagram of the MOSFET [46]

Figure 3.2: MOSFET

voltage, the wider the n-channel formed by electron accumulation, which increases conductivity and causes the drain current (I_D) to flow between the Source and Drain. When no voltage is provided to the gate terminal, no current flow except for a small amount of current due to minority charge carriers, the threshold voltage is the lowest voltage at which the MOSFET begins to conduct [46].

3.2.2. SiC MOSFET

The most prevalent power transistors in recent years have been Si-MOSFETs, IGBTs, and SiC-MOSFETs, which can handle a wide range of frequencies and power. The figure 3.3 depicts the frequency and power handled by these three main power transistors. IGBTs can withstand high power but not high frequencies. On the other hand, Si MOSFETs can function at high frequencies but have a lower power capacity than IGBTs. SiC MOSFETs, on the other hand, are ideally suited for both high-speed operation and better power handling capacity.

The energy necessary to shift an electron from its outer shell so it may flow freely inside the material is defined as wide-bandgap. Wide-bandgap is the next generation, with everything new, from manufacturing to operating devices. Wide-band gap material-based switching devices such as Silicon Carbide (SiC) MOSFETs, Gallium Nitride (GAN), and high electron mobility transistors (HEMTs) have received much interest in recent years due to their benefits, replacing (Si) MOSFETS [48].

In the end, it primarily comes down to speed. The speed at which these devices are

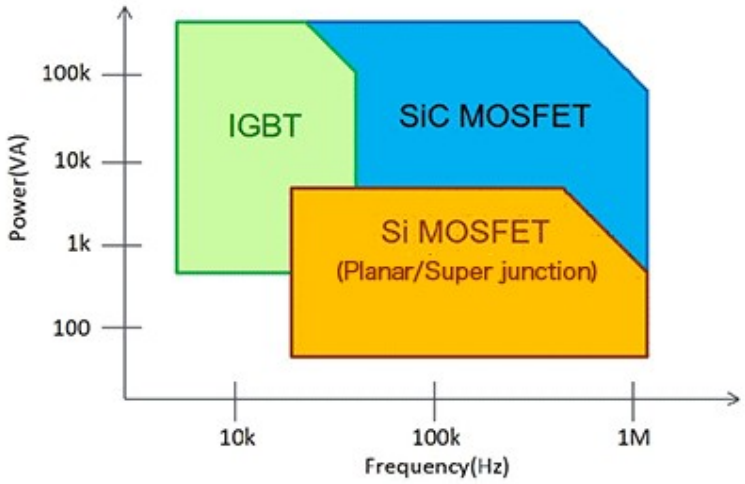


Figure 3.3: Power and switching capabilities of Si and SiC devices [47]

switched is directly proportional to the losses in the system. A Si MOSFET has a lot of loss and a reverse recovery charge (Q_{rr}) of approximately 1000 nC. whereas for Sic, the loss and recovery charge are less; in the range of hundred nc. The switching frequencies can go into the megahertz range for SiC-MOSFET. The benefits of SiC are higher breakdown field strength, electron saturation velocity, energy bandgap, and thermal conductivity.

Silicon carbide is made by simply placing sand and coal into a reactor and heating it with electricity. It is generated in the chamber over a few days. A significant portion of the SiC MOSFET is the wafer. Because of the material's brittleness and hardness, the entire process chain is more expensive. The wafers typically have a diameter of 4 to 6 inches. If a SiC MOSFET is compared to a Si MOSFET with an equal rating, First, for the same R_{DSon} value, the dye size of SiC MOSFET is substantially less than that of Si MOSFET. Second, a slew of system advantages may be realized, including higher efficiency due to lower power losses, higher power density, higher frequency operation, and higher temperature operation, which leads to the third advantage, application advantages. The device-level impact is that SiC MOSFETs can withstand high voltages with low specific on-resistance (R_{sp}) and reduced switching losses. The result at the system level is that it can function with high-frequency switching and requires less cooling. End applications benefit from their tiny size, lightweight, and outstanding efficiency.

3.2.3. Selection of the switch

The switch characteristics should be carefully chosen since they can significantly affect a pulse transformer's output. Certain critical parameters must be examined between switches, and trade-offs must be considered. Although SiC MOSFETs are the superior choice for high-frequency applications, Si MOSFETs are also being explored due to their lower cost. In addition, due to the pandemic, there are just a few switches on the market that are available to buy. Two Infineon switches and one ST life augmented switch are being investigated. Several specifications for a MOSFET switch are given in their respective data sheets. The following are the critical specifications for this application:

- The continuous drain current rating I_D of the MOSFET is crucial because the switches in the H-bridge must be able to handle the current taken by the primary of the pulse transformer. This should be in the 8 to 10 Amp range.
- The Drain to Source withstand voltage V_{DS}, which defines the pulse generator's reliability. If this number is low, the switch may burn when transients reflect on it. This value should be more than 900V.
- Switching delays, such as on-time delay $t_{d(on)}$ and off time delay $t_{d(off)}$, should be kept to a minimum. It is preferable if it is in the range of 10 ns. If this value rises, switching losses will rise due to the charging of the internal capacitance.
- It is preferable to have a low on-resistance $R_{DS(on)}$. It is desirable if it is in the milliohm range. In other words, less resistance creates less heat, making dissipation measures easier to execute.
- It is preferable to have a low internal gate resistance $R_{G(int)}$. If this value is too high, the switch will be slow.
- When a switch functions, it generates heat, which must be dissipated to avoid thermal runaway. Using heat sinks is one method for keeping the switch within thermal limitations. As a result, a through hole package is also required.
- A cost-effective switch would be considered.

Model	I_D	V_{DS}	$t_{d(on)}$	$t_{d(off)}$	$R_{DS(on)}$	t_r	t_f	$R_{G(int)}$	V_{GS}	C_{iss}	C_{oss}	C_{rss}	P_D	Price
	A	V	Ns	Ns	mΩ	Ns	Ns	Ω	V	pF	pF	pF	W	€
STB34N65M5	28	710	59	59	90	8.7	7.5	1.95	±25	2700	75	6.3	190	4.94
IMW120R220M1H	13	1200	5	10	220	1.4	14	22	±20	289	16	2	75	11.775
IPAN80R360P7	13	800	10	40	310	6	6	1	±20	930	16	4	30	2.86

Figure 3.4: Comparison between three switches with their models

The three switches' relevant parameters were obtained from their individual data sheets and are shown in the picture 3.4. The first switch has a high continuous drain

current, but not a high Drain-Source withstand voltage. The other two switches each have an I_D rating of 13 amps. The pulse transformer's typical current capacity for this application is expected to be around eight amps. As a result, the other two switches can also be considered. Because several transients are predicted during testing, V_{DS} should be higher for this application. The second switch has a V_{DS} of 1200 V, but the other two can also be considered because their prices are substantially lower. The second switch excels in terms of delay and rising time. These are critical for our application since the faster these timings are, the pulse output from the H-Bridge will also be faster. The table also includes the parasitic capacitance. This chapter goes into further detail on why these capacitances should be considered. The prices of the switches are also provided, with the third switch being the cheapest and the second switch is the most expensive. Although the second switch is the most appealing for this application, the other switches are still being considered due to their low cost. Further analysis was conducted using the lab's sample switches of all three types.

All three switches were tested once the gate drivers and H-bridge were built. The output of the switches is resonating at a particular voltage—for example, the *STB34N65M5* switch resonated at around 40 V. Figure 3.5 depicts the output of this switch at resonance. During the resonance, the output is severely disturbed, which may cause the switches to fail. This resonance is because MOSFETs contain parasitic capacitance, as seen in the image 3.7. This capacitance is voltage-dependent, as seen in the figure 3.6. As a result, input capacitance must be considered a significant parameter. The switch *IMW120R220M1H* is chosen out of the three since it has the lowest capacitance and no resonance.

3.2.4. Switching characteristics

The switching characteristics of the selected switch were simulated in LT spice. This simulation is to check whether the switch is following the datasheet. Mainly the delay times and rise and fall times are examined in this simulation. Spice models can be downloaded from their respective websites and then converted into LT spice models. The figure below shows the LTspice model of the switch, rise time, and fall time characteristics.

The gate voltage of 20V was given, required for the switch to turn on. A frequency of 10 kHz was applied. The data sheet gives a rise time of 1.4 ns, while the simulation gives a rise time of 3.27 ns, which is three times slower than expected. The simulation's on-time delay $t_{d(on)}$ is 2.30 ns, but the data sheet's is 5 ns. In the fall time characteristics, the off-time delay on the simulation is 10.47 ns, but it is 10 ns in the datasheet. The fall time in the simulation is 20 ns, but it is 14 ns on the datasheet. This disparity yet relative values is because the spice model characteristics are always not accurate, as confirmed in the spice model lib file. However, these simulations can be used to predict the characteristics of a switch before buying. Gate drivers are required to drive these switches, and their circuits should be designed based on the switch characteristics. The same will be covered in the next section.

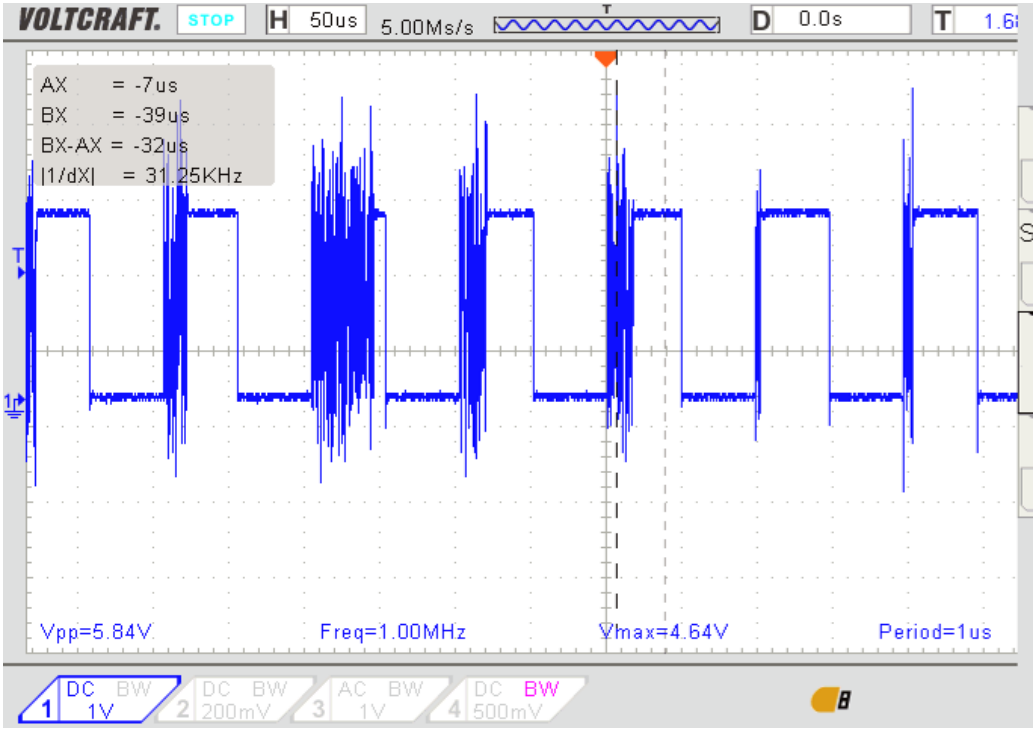


Figure 3.5: Sic MOSFET H-bridge output at resonance

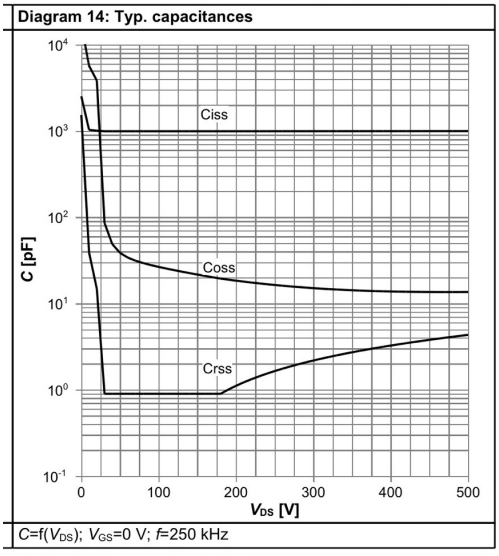


Figure 3.6: Voltage dependent capacitance [49]

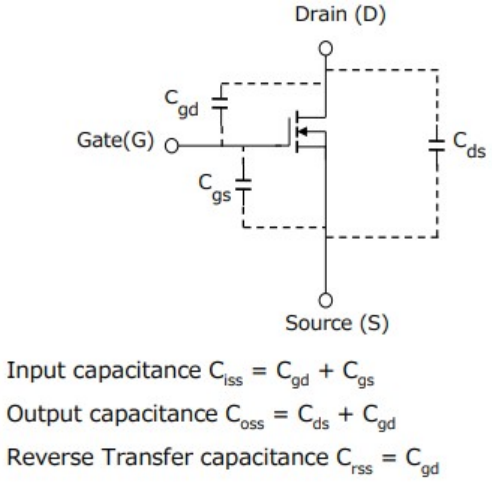


Figure 3.7: Parasitic model of a MOSFET [50]

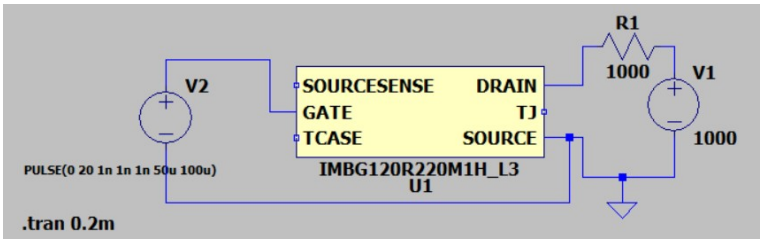
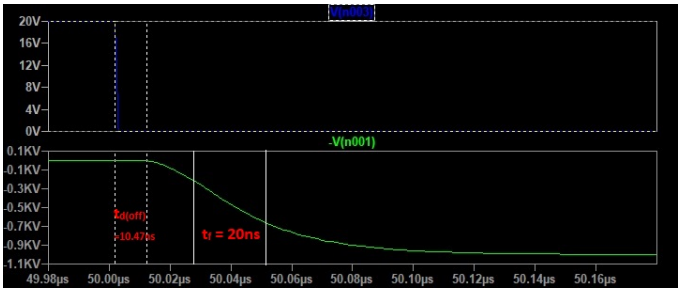
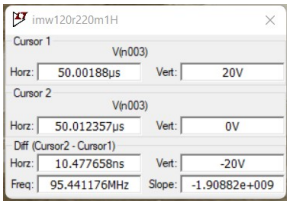


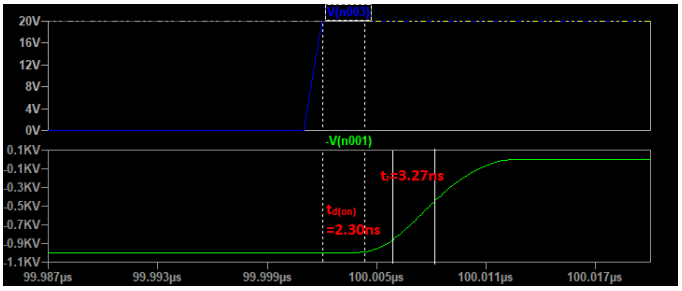
Figure 3.8: LTspice model of IMW120R220M1H



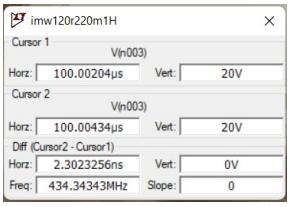
(a) fall time characteristics



(b) cursor value of fall time



(c) rise time characteristics



(d) cursor value of rise time

Figure 3.9: Simulation results of IMW120R220M1H

3.3. Gate Driver and H-Bridge

3.3.1. What is gate driver?

The vast number of topologies and the increasing complexity of applications, such as switching power supplies, are at the heart of nearly all modern electrical systems. Automotive systems use switching power supplies to maintain an increasingly complex ecosystem of batteries, motors, chargers, etc. Modern switching power supplies frequently use a microcontroller or other ASIC to orchestrate the carefully timed switching of an array of high-power transistors. This method can be challenging since most microcontroller outputs are not optimized to drive power transistors.

It is obvious that the properties of high-power transistors are rarely equivalent to those of other transistors used in analog signal chains or digital logic. Power transistor breakdown voltages range from around 40 Volts to an impressive 1700 Volts or more. Because of the necessity for greater drain currents and smaller conduction losses, drain-source resistance is reduced to tens of milliohms or less. Gate capacitance is inversely proportional to drain-source resistance in nanoscale farads. The gate drive voltage and current requirements are heavily influenced by the transistor construction and drain current rating, with typical values ranging from 8 to 30 volts and 1 to 5 amps. As the gate capacitance charges and discharges, a transition time occurs between the switch's completely ON and completely OFF states, during which a voltage appears across the switch, and a current flows through the switch. Because of the existence of both higher voltages and higher currents, switching losses result in significant power dissipation, often tens of watts. It is thus desirable to shorten the transition period by rapidly charging and discharging the gate capacitance.

Most microcontrollers' low-current digital signaling is prohibitively slow and inefficient for driving high-power transistors, even if the output voltage is high enough to switch the transistor ON. So, to answer the question,*"what is a gate driver"* - a gate driver is a circuit used to amplify a control signal from a microcontroller or other source so that it may be utilized to operate semiconductor switches efficiently and effectively.

3.3.2. Requirements and selection of the gate driver

The gate driver used fundamentally determines the switch's operation and performance. The gate driver's requirements must be considered to maximize power efficiency. When selecting a gate driver, the following are the most important factors to consider:

- The first requirement for the gate driver is a high output drive voltage of 25 to 30 volts; typically, silicon MOSFETs are driven with only 15 to 20 volts, and this extra drive voltage allows the driver to endure more supply surges and is more noise-resistant.

- Faster switching causes greater noise in the system, needing high dv/dt immunity or common mode transient immunity (CMTI). CMTI is the maximum tolerated rate of rise or fall of the common mode voltage between two isolated circuits.

- A smaller propagation delay. A shorter propagation delay equals less dead time, which reduces power loss through the MOSFET's body diode.

- The reinforced isolation voltage is the following criterion. An isolation barrier between the primary and secondary sides is required to prevent undesired AC or DC impulses from moving from one side to the other. Furthermore, the control side may be accessible by people, necessitating high voltage separation to prevent electric shock.

- Another critical criterion is peak output current capability. The current required to turn on a silicon carbide MOSFET is determined by the MOSFET switch's properties, such as its gate charge.

The gate current, also known as drive strength, governs how quickly the device's input capacitors charge and discharge. However, the miller plateau area is vital because the gate voltage remains constant during the switching transient while the gate to source capacitor charges. To decrease switching losses, the switch requires greater current in this area, which the gate driver should supply [51]. The SiC switch's gate current may be estimated using the following simplified formula:

$$I_G = \frac{\Delta V_{GS,datasheet}}{R_{G,datasheet} + R_{G,int}} \tag{3.1}$$

where

$$\Delta V_{GS,datasheet} = |V_{GS(on)}| + |V_{GS(off)}|$$

This calculation ignores the internal resistance of the gate driver of choice. The datasheet has all of the required parameters with the selected switch *"IMW120R220M1H"*. The suggested turn-on gate voltage is 18 Volts, and the recommended turn-off gate voltage is 0 Volts, according to the datasheet. The external gate resistance for a $1.4ns$ rise time is given by 2Ω. 2.2Ω is the internal gate resistance. As a result, the gate current is computed as follows:

$$I_G = \frac{18}{2 + 22} = 0.75Amps \tag{3.2}$$

The selected gate driver's typical output current value should be equal to or greater than the computed value.

The power dissipation by the gate driver can be calculated as:

$$P_D(Power\ dissipation) = Q_G \cdot f_{sw} \cdot \Delta V_{GS} \tag{3.3}$$

The calculations are simplified by assuming power losses during switching are solely dissipated in the gate driver's output stage. In actuality, gate resistance absorbs part of the losses as well.

$$P_D(Power\ dissipation) = 8.5nc \cdot 50kHz \cdot 18V = 7.65mW \tag{3.4}$$

The gate driver *STGAP2SICSN* was chosen based on the specifications described above. There was a chip shortage due to the pandemic, and there were relatively few gate drivers on the market. This specific gate driver meets all essential requirements while also being cost-effective. The following are the characteristics of the chosen gate driver:

- High voltage rail up to 1700 V.
- Driver current capability: 4 A sink/source $25°C$
- dv/dt transient immunity ±100 V/ns in the entire temperature range
- Overall input-output propagation delay: 75 ns
- Separate sink and source option for easy gate driving configuration
- UVLO function
- Gate driving voltage up to 26 V
- $4.8kV_{PK}$ isolation

Figure 3.10 shows the schematic diagram. It is comprised of two single-output gate drivers. Two of these modules were required since the H-bridge (full bridge inverter) requires four gate drivers to drive four switches. Each gate driver has two DC/DC converters to supply the voltage. No bootstrap capacitor was employed to acquire the freedom to modify the duty cycle, which cannot be done if a bootstrap capacitor is employed. Four LEDs were connected to indicate power. The following components are connected in this circuit:

- At the logic inputs, a tiny input filter is attached to filter out ringing caused by parasitics generated by non-ideal layout or lengthy PCB traces. The top gate driver module filters were $R3$ and $C10$. Resistance and capacitance values are typically in the range of 0Ω to 100Ω and 10 pF to 100 pF. It was 51Ω and 10 pF connected in this circuit. The propagation delay increases when large values for this filter are used. As a result, there is a trade-off between noise immunity and propagation delay.
- Two resistors, $R5$ and $R6$, were connected at the output side. These are external gate driver resistors that will be used to do the following:
  - Limit ringing caused by parasitic inductances/capacitances.
  - Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.

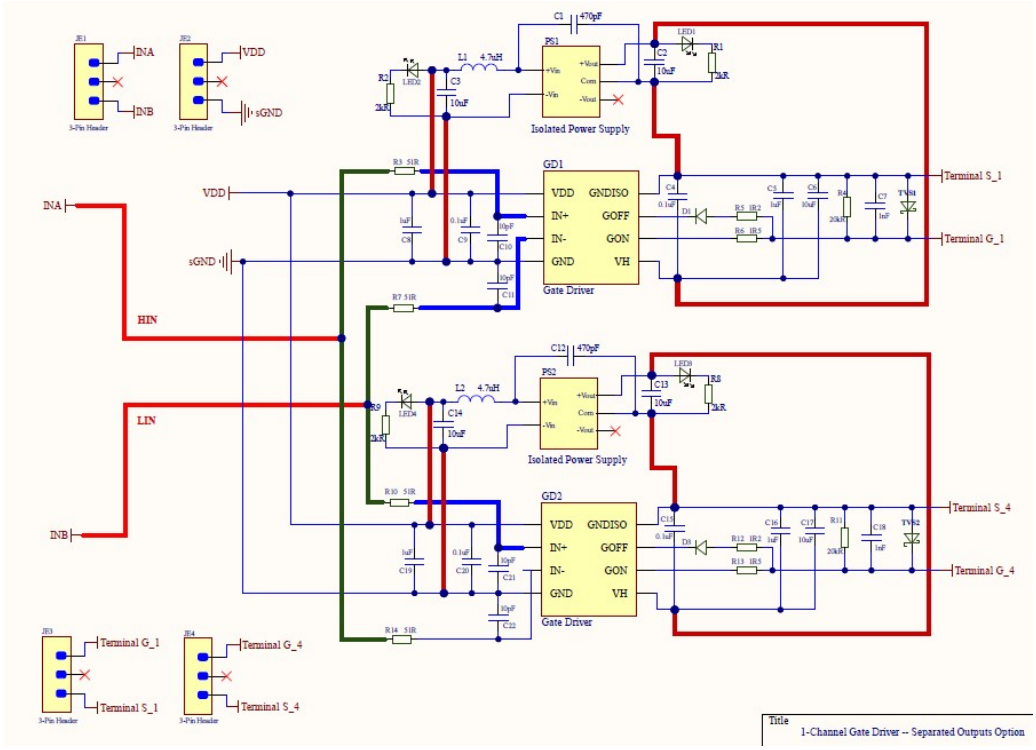


Figure 3.10: Schematic of the gate driver connections

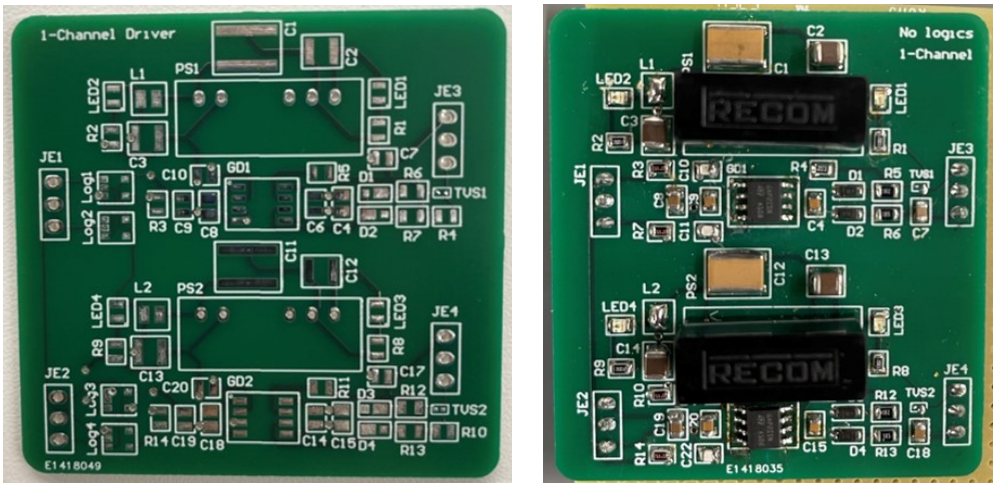
  - Fine-tune gate drive strength, peak sink, and source current, to optimize the switching loss.
  - Reduce electromagnetic interference (EMI).

  The values of $R5$ and $R6$ were 2Ω and 5Ω, respectively. When the H-Bridge and load are connected, these parameters can be changed based on the peak and ringing of the output.

- A gate-source resistor is connected to make the voltage zero when the switch is not turned on. This resistor also aids in actively pulling down before the Miller current turns on. This resistor's average values range from $5.1k\Omega$ to $20k\Omega$. In this circuit, a $20k\Omega$ resistor was connected and labeled $R4$.

- To support the transient current required by the primary logic and the total current usage, a bypass capacitor is placed between VDD and the ground. The average value is more than $100\,nF$, and in this circuit, $1.1\mu\,F$ was connected in parallel using $C8$ and $C9$ capacitors.

- A capacitor is linked between GNDISO and VH, which are isolated ground and positive input voltage, respectively, to maintain a consistent driving voltage for the transistor. It is advised that more than $100nF$ be used, and in this circuit, $11.1\mu\ F$ is connected with the combination of $C4, C5$, and $C6$.



(a) Gate Driver PCB

(b) Soldered gate driver PCB

Figure 3.11: Printed Circuit Board of the Gate Driver

A TVS diode and a capacitor were also connected across the gate and source, designated as $TVS1$ and $C7$. The TVS diode (Transient Voltage Suppressor) aids in the suppression of peaks induced by parasitic inductance introduced by circuit loops linked to the load. A gate to source capacitor is used to add capacitance to the natural gate to source capacitance, which reduces the power transistor's rise time while increasing switching losses. However, this aids in reducing peaks and ringing induced by high dv/dt or di/dt. This circuit was printed on a PCB, and all the components were soldered as shown in the diagram 3.11.

The gate driver was tested to find out its performance. The test setup is shown in the figure 3.12. A "Voltcraft plus Vsp 1410 HE" is a voltage source that supplies $5V$ to the gate driver. The logic inputs were given from an Arduino (MCU). A "pico technology TA057" differential probe was used to measure the output. A "Tektronix DPO 3034 Digital Phosphor Oscilloscope" is an oscilloscope used to display the output.

The response of the gate driver is shown in the figure 3.13. The rise time of the gate driver output was measured with cursors, and it was 18.8 ns.

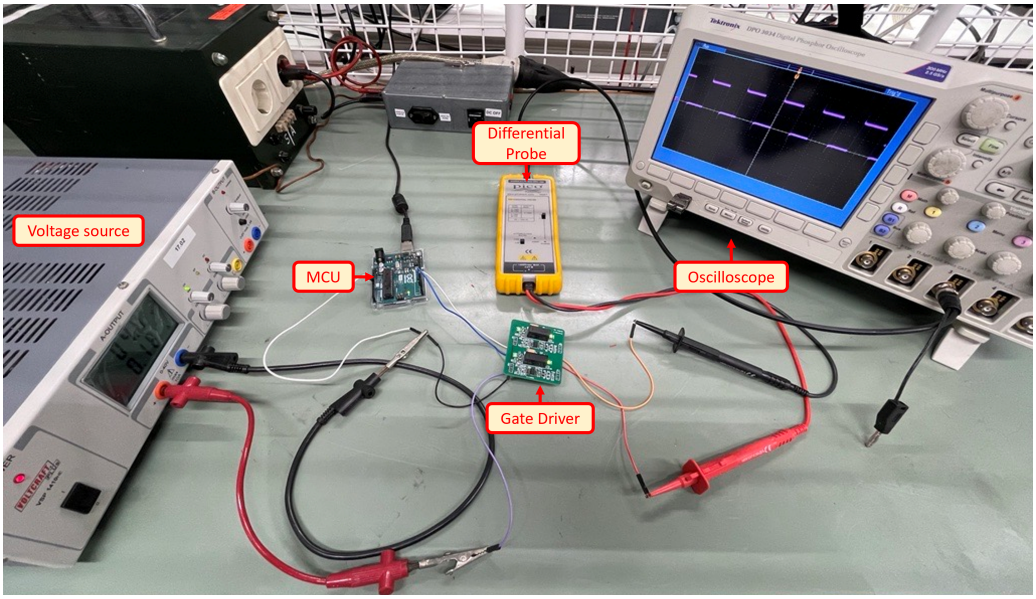
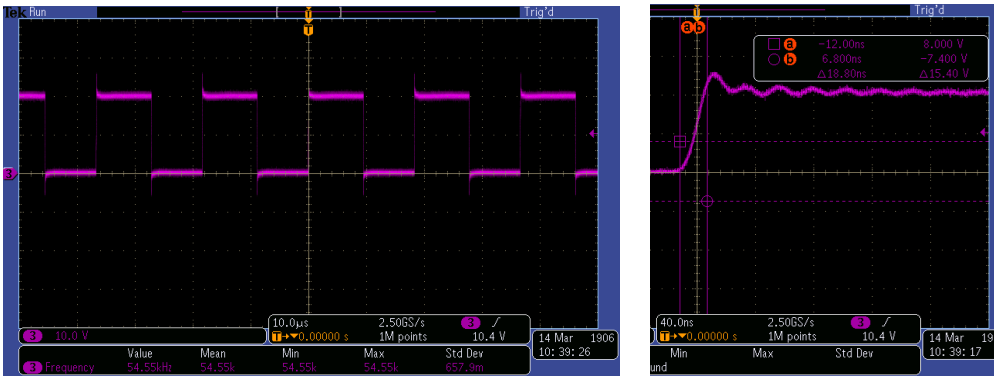


Figure 3.12: Gate driver test setup



(a) Gate pulses (b) gate driver response

Figure 3.13: Gate driver output response

3.3.3. H-Bridge

Figure 3.14 depicts the H-bridge circuit connections. The input terminals were labeled *HV_Input1* and *DC_Ground1*. The use of the integrated commutation capacitances *C45* and *C46* is to minimize inductance for high-frequency applications, which aids in lowering voltage spikes during the power device switch-off cycle [52]. In the H-bridge configuration, four switches are connected. The gate driver circuits generate the gate signals. +*V_out1* and -*V_out1* were used to identify the output terminals.

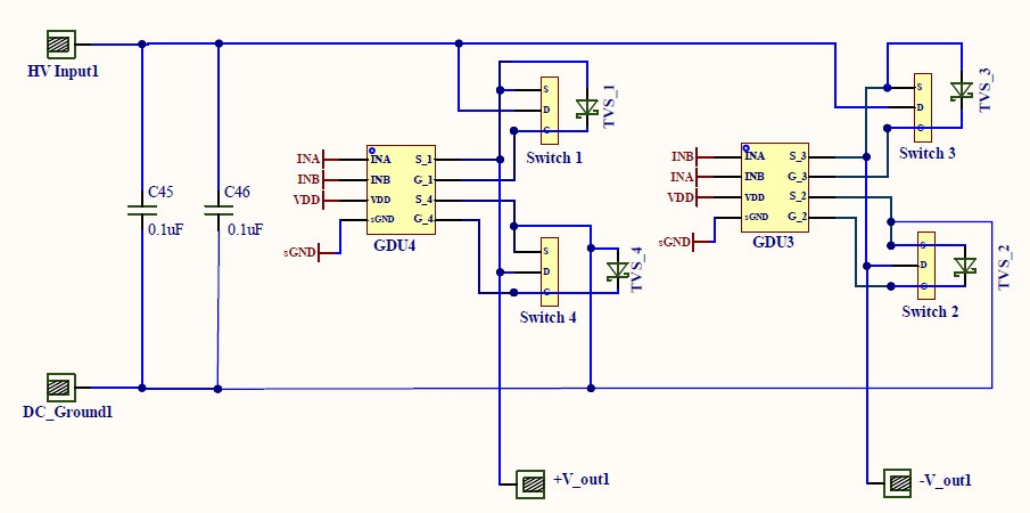


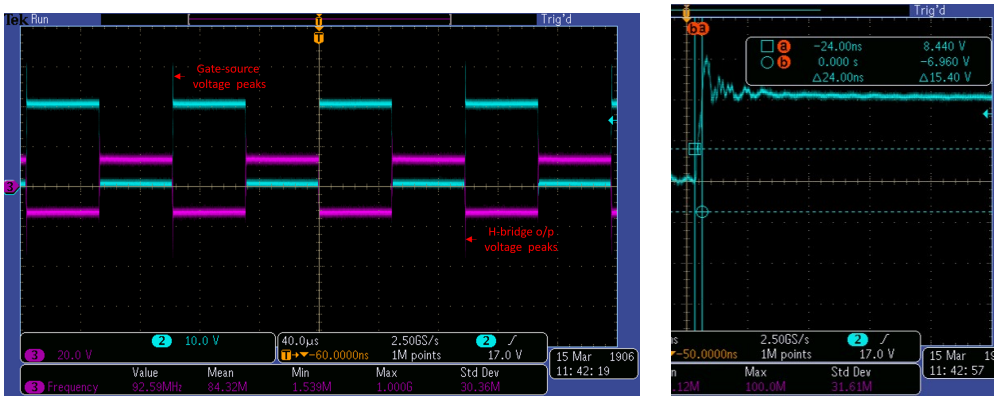
Figure 3.14: Schematic of H-bridge inverter

3.4. Pulse Generator Testing

The gate drivers and the H-bridge were interconnected. The output of the H-bridge was measured while one of the gate driver pulses was monitored. This was done to see how the gate to source voltage (gate driver output) behaves when the DC input to the H-bridge is increased. The voltage spikes at the gate to source terminals rise depending on the voltage because the power transistor's capacitance varies as the voltage changes. This variation in capacitance is shown in the figure 3.6 from the datasheet of the power transistor. The findings of this evaluation are discussed in the sections that follow.

3.4.1. Initial testing

In this testing, only the initially designed circuits such as the gate drivers and H-bridge were tested. There is no load connected to the H-bridge output. The output of this circuit is shown in the figure 3.15.



(a) Gate to source voltage, and H-bridge output

(b) Gate to source voltage peak

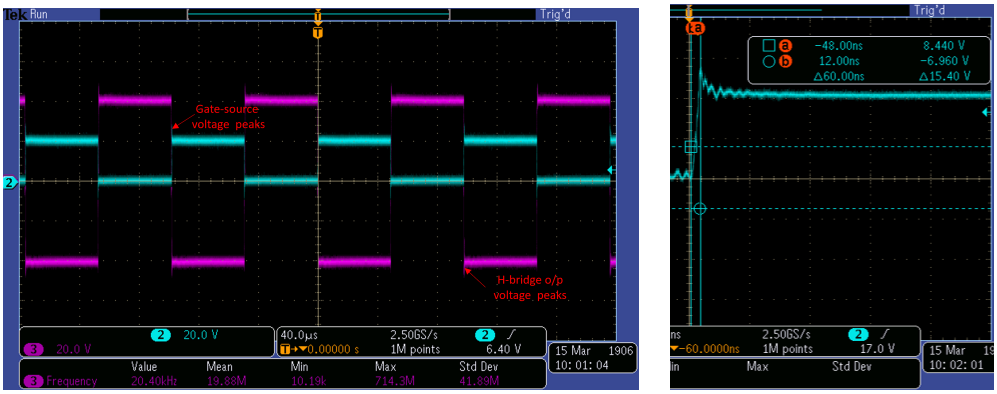
Figure 3.15: Initial testing results

The blue output in the picture 3.15a is the gate to source voltage, whereas the pink output is the H-bridge output. The figure shows that the voltage spikes on the gate to source voltage reached $30V$ for only the H-bridge output of $13V$. Many gate drivers were burned before this phenomenon was known when the H-bridge output voltage was approximately reached 40V. This is because, at higher frequencies, the di/dt and dv/dt rates rise due to stray inductances and parasitic capacitances, resulting in current and voltage overshoots [53]. If the PCB design layout is optimized, stray inductances may be decreased, reducing EMI concerns [54]. The PCB designs were completed at this point. There were several inductive loops in the current design to give flexibility in changing the switches and gate drivers to be able to test different switches and gate drivers. Furthermore, at fast switching rates, the gate-source voltage on the complementary switch surges while turning on and off a switch, which is inevitable [55]. The figure 3.15b shows that the rising time is $24ns$, and the peak reached $30V$ for a $13V$ H-bridge output.

3.4.2. With gate resistor and TVS diode

The first step in addressing the voltage spikes is to reduce the switching speed. This is accomplished by increasing the turn-on gate resistance. As a result, a gate resistor of 22Ω is connected in series. A Transient Voltage Suppressor (TVS) is also connected across the gate driver's output. TVS are electronic components that shield sensitive electronics from high voltage transients. Figure 3.16 depicts the gate driver's response and the H-bridge

output for this scenario.



(a) Gate to source voltage, and H-bridge output

(b) Gate to source voltage peak

Figure 3.16: With gate resistor and TVS testing results

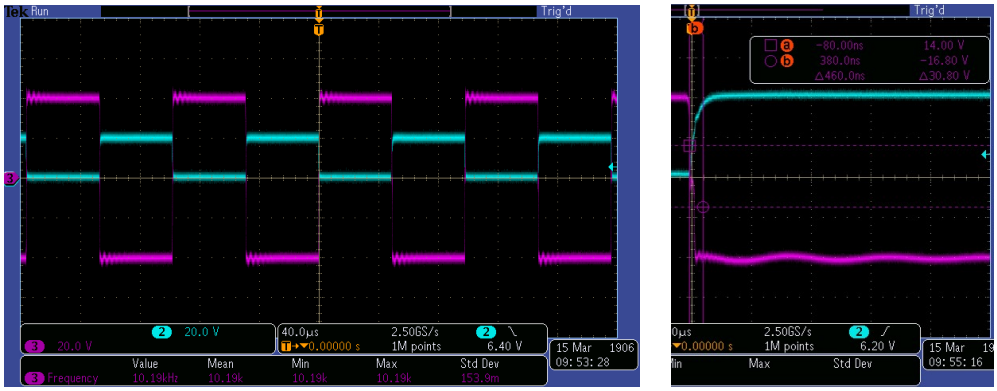
If a large resistor is employed, the overshoots can be decreased significantly. However, the losses increased too. Conversely, if the gate resistor is small, the voltage overshoots will increase, which introduces EMI problems [56]. Additionally, if a large resistor is employed here, the current required for the switch to turn on may be decreased. The figure 3.16a shows that the output voltage has reached $40V$ and can still increase. The gate to source voltage peaks is reduced. This is due to a decrease in the speed of the gate driver output, which is now $60ns$ as opposed to $24ns$ in the previous case. However, it was discovered that only $80V$ output could be achieved with this setup, and anything more caused the gate drivers to burn out. The gate driver's speed should still be reduced. This is done in the next section.

3.4.3. With gate-source capacitance

The gate driver sees a capacitance between the gate and the source terminals. Figure 3.7 depicts the parasitic capacitance model of any MOSFET. The MOSFET's gate voltage does not increase until the input capacitance is completely charged [57]. Adding an additional gate to the source capacitance increases the rising time of the gate driver pulses. A $6.6nF$ is connected in this scenario. This number was obtained by experimenting with several appropriate capacitance values for this particular application. The greater the capacitance value, the lower the peaks are and the greater the losses, and vice versa. The ringing was introduced into the H-Bridge output as capacitance was increased. This is due to the resonance of the PCB's capacitance and loop inductances. Because the capacitance value has increased, resonance begins at lower frequencies.

An extra gate to source resistor ($15k\Omega$) is added to help draw down the gate to the source voltage, lowering the dv/dt induced turn-on owing to Miller current [58]. In addition,

a TVS diode ($24V$) is connected near the switches to clip any transients present. Figure 3.17 depicts the response when extra capacitance, a TVS diode, and a resistor were connected.



(a) Gate to source voltage, and H-bridge output

(b) Gate to source voltage peak

Figure 3.17: With gate to source capacitance, resistor and TVS testing results

As predicted, the gate driver's output rise time increased from $60ns$ to $460ns$, as indicated in the figure 3.17b. At the $40V$ H-bridge output, there are no peaks in the gate to source voltage. There is some ringing in the output, but it does not impact the transformer since it serves as an inductance, filtering out the ringing. With this configuration, the output exceeds $150V$, sufficient to supply the pulse transformer.

3.5. Pulse generator Summary

The pulse generator generates pulses that are fed into the transformer. This pulse generator comprises gate drivers that control four H-Bridge switches. The switch selection was initially evaluated. It was discovered that the output was substantially disrupted owing to resonance; hence the input capacitance should be considered while selecting a switch.

The gate driver and H-bridge circuits were then discussed. The gate drivers burned owing to voltage peaks at the gate to source terminals as the voltage across the switches increased. This is due to the fast switching rates. Several extra components were connected as indicated to reduce the speed of the switches. This raises the losses, but the gate drivers survive considerably longer during testing.

3.6. Conclusion

The first research question *"What are the most essential factors to consider when selecting a switch and building a gate driver for an H-Bridge?"* was addressed in this chapter.

- While selecting a switch, its input capacitance should be considered to avoid resonance in the output.
- The gate driver speed should be lowered by adding extra components such as a gate resistor, gate to source capacitance, and a TVS diode, according to the application. This reduces peaks across the gate to source voltage and improves the reliability of the gate drivers. This also reduces peaks in the H-bridge output.

Recommendations: The PCB should be optimized so that inductive loops are minimized. This reduces the bill of materials and results in fewer losses. The optimization was not completed correctly due to time constraints. To eliminate stray inductances, even the additional lengths of the switches should be removed. To decrease lengthy traces, all components should be close to one another on the PCB. The ground plate (copper) of the PCB should be distributed entirely, not simply traces. This aids in lowering the inductance.

4

Pulse Transformer

The pulse transformer will receive low voltage pulses from the H-bridge output. It increases the voltage based on the turn ratio n. This pulse voltage is utilized to test the OIP, which is the overall goal of this thesis. The transformer's input voltage is 200 volts pulsed at different frequencies, while the output voltage is 10 kV at the same frequencies. To produce the same output pulse shape as the input, the transformer parasitics must be kept to a minimum. This chapter describes how to measure parasitics, model them on two sample transformers, and approximate the output pulse of the transformer. The lumped parameters derived from this data are used to create a Matlab-Simulink model. Finally, an optimizing flow chart is presented for this specific application. Before constructing a transformer, the parameters were extracted using COMSOL. A transformer prototype was built using simulations that attained the needed pulse parameters.

4.1. Literature on Pulse Transformers

The primary goal of a pulse transformer is to boost the voltage supplied by the pulse generator. Its construction, appearance, and function are comparable to conventional transformers. On the other hand, the rectangular pulses are steep and generally linked with high-frequency components. As a result, its design is comparable to that of a high-frequency transformer. The challenges and benefits of higher frequencies also apply to the pulse transformer. A magnetic pulse transformer comprises three parts: a primary winding, a secondary winding, and magnetic cores. The transformer operates based on Faraday's law of electromagnetic induction. The flux in the magnetic core is determined by the equation 4.1 according to flux conservation. While functioning, the core should not become saturated.

$$\phi = \int v(t)dt = N\Delta B A_c \tag{4.1}$$

Where N denotes the number of turns, Δ B denotes the change in magnetic induction, and A_c is the cross-sectional area of the transformer core. The voltage-second product is $\int v(t)dt$. To protect the cores from becoming saturated, the voltage-second product of a pulse transformer should be less than the intended magnetic flux. [59].

Until late 1941, no pulse transformer was developed that could transfer a 1- μs rectangular pulse delivered to its secondary. This is primarily because of the scarcity of high permeability cores capable of providing relatively high saturation densities [60]. Bell Telephone Laboratories, Westinghouse Electric Corporation, and General Electric Companies created high permeability cores for pulse transformers in 1942 [61]. Analytical studies on potential core materials were also conducted concurrently. This aided designers in making designs more straightforward, [62]. Since 1942, the power rating for applications has risen, as has the size of the pulse transformer. The growth of semiconductors and the shrinking of control and logic circuits has necessitated the creation of considerably smaller and more power-dense pulse transformers.

During World War II, pulse transformers were used in radar applications. Pulse transformers now have a wide range of applications that are not limited to the high power industry. Because of their high repetition rate, pulse transformers are utilized in applications such as X-rays, plasma technology, food sterilization, and air pollution management. Many of these applications have stringent criteria for pulse characteristics such as rise time, fall time, overshoot, and pulse top flatness. Despite the continuous advancement of semiconductor switches, transformers remain an essential component in the majority of high-voltage applications. The cost of a semiconductor capable of handling high voltages, like a pulse transformer, will be extremely expensive. As a result, semiconductor switches are utilized in pulse generators, and their output is sent to pulse transformers, reducing voltage stress in the pulse generating circuit [63]. IEEE developed a standard for pulse transformers, [42], which described the definitions of the pulse, performance tests performed on a pulse transformer to obtain the lumped parameters, and the equivalent circuit of the pulse transformer, which consists of both complete and partial circuits. It also explained extracting the pulse transformer's equivalent circuit elements and concluded with alternate test techniques. This standard is quite beneficial to many designers, including this study. H.S.Kirschbaum established the methodology for designing the pulse transformer in 1949 [64]; he highlighted the necessity of estimating the fields in terms of lumped circuit parameters. The suggested technique is simple and results in an optimal design given an appropriate set of transformer requirements. P.R.Gillette studied the response of the front pulse of the transformer using a T circuit having three inductances and a capacitor in [65], which yields an accurate prediction compared to the basic half-T circuit that was routinely utilized at the time. Until this time, design engineers employed numerous separate mathematical calculations, which had to be repeated several times to produce the optimal design. This way is time-consuming and tiring. P.E.Lego pioneered the use of digital computers in the design of pulse transformers. He designed the transformer using computer programs and provided a flow diagram on how to do so.

This enabled designers to reduce computation times dramatically [66]. M.Akemoto created a pulse transformer prototype for the NLC Klystron pulse modulator in 1997. His study demonstrated a simple equivalent circuit to predict the pulse output, as illustrated in Figure 4.1. He employed a basic L-L-C model for a non-parallel plate capacitor on the primary and secondary windings [67]. Because the author primarily studied distributed electrical energy between primary and secondary windings only, the results are somewhat inaccurate. J.Biela [68] took on this problem by considering areas for the distributed capacitance of a pulse transformer, as illustrated in the figure 4.2. He proposed an equivalent circuit and analytic equations for determining the parameters, as shown in the figure 4.3.

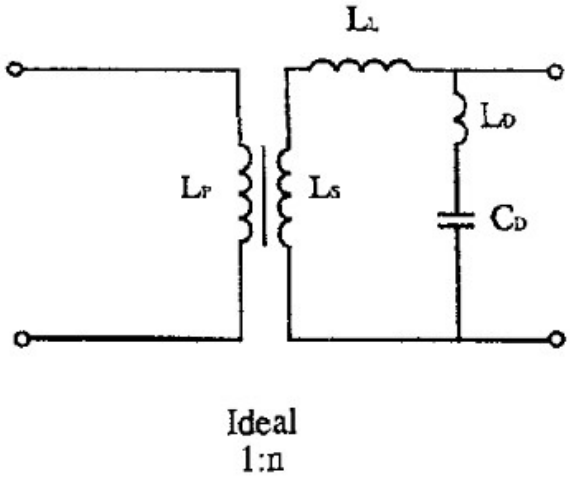


Figure 4.1: equivalent circuit presented in [67]

Luis Manuel Redondo employed two auxiliary windings to decrease leakage inductance. He connected two subtractive windings with the same number of turns as seen in the figure 4.4. The current flowing through them creates a magnetic field, which decreases the leakage flux and, as a result, the leakage inductance. The author provided a mathematical model based on the theory of electromagnetic coupled circuits [69]. The author created an active reset circuit in [70] to improve the pulse rising time. This optimizes core material utilization; it is demonstrated in this research that the active circuit balances the flux swing in the transformer core. He also demonstrated a unique and easy way of controlling the premagnetization interval, which results in symmetric flux swings. Figure 4.5 depicts the active reset circuit. D.Bortis, the same author, provides a detailed design procedure for compact pulse transformers with rectangular pulse shapes and quick rise times in a separate publication [71]. He demonstrated the method step by step. Different transformer topologies are examined to obtain parasitic components, and the impact of the core material was also discussed. He demonstrated that the pulse

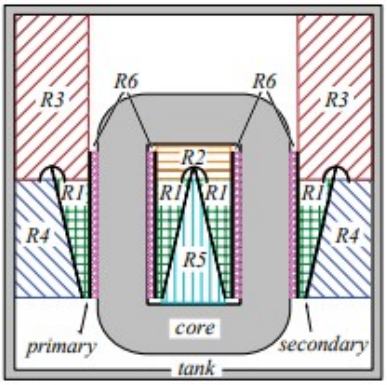


Figure 4.2: Regions considered to calculate distributed capacitance in [68]

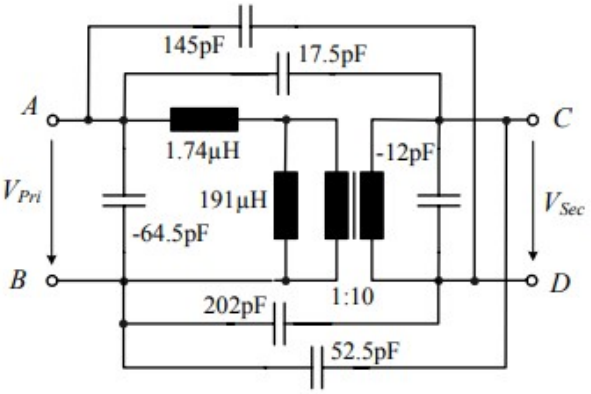


Figure 4.3: Calculated equivalent circuit by [68]

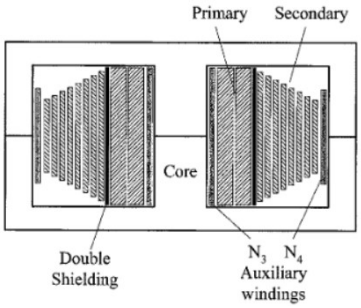


Figure 4.4: Auxiliary windings proposed by L.M.Redondo [69]

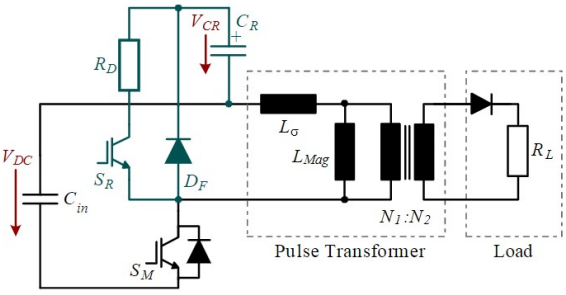


Figure 4.5: Active reset circuit proposed by D.Bortis [70]

overshoot is proportional to the ratio of leakage inductance to distributed capacitance.

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma}{C_d}} \tag{4.2}$$

Whereas the rise time is proportional to the product of leakage inductance and distributed capacitance.

$$T_r = 2\pi T_{10\%-90\%}\sqrt{L_\sigma C_d} \tag{4.3}$$

However, these equations are for a resistive load, but the load in this thesis is highly capacitive. As a result, the equations below give the overshoot and rise times for capacitive loads. The capacitance of the load should be added to the transformer's distributive capacitance. To obtain the desired rise times, the parasitics of the transformer should be reduced as much as possible while considering high voltage performance.

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma}{C_d + C_{load}}} \tag{4.4}$$

$$T_r = 2\pi T_{10\%-90\%}\sqrt{L_\sigma C_d + C_{load}} \tag{4.5}$$

He found that cone-shaped secondary winding will provide the quickest rising time compared to parallel and foil winding approaches. Many of the approaches described in this paper were employed in this thesis.

4.2. Design of the Pulse Transformer

According to the literature, the pulse transformer has parasitic inductance and distributed capacitance. These parasitic components dictate the output pulse's rising time and overshoot. The pulse transformer's minimum cut-off frequency f_u is determined by non-ideal core material features such as finite permeability ($\mu \neq \infty$) or maximum flux density (B_{max}). Furthermore, the magnetic coupling between primary and secondary is not ideal, resulting in a certain leakage inductance. There will also be distributed capacitance owing to the voltage differential between the primary and secondary. As a result, a good design must be applied to obtain the transformer's required output.

Before proceeding with the design, the output pulse parameters must be defined. Because the maximum output voltage of single-phase mains in the Netherlands is 230 V, the transformer input should be less than this value. The highest output voltage to test the oil impregnated papers is approximately 10 kV. If the input voltage is set to 200 V, the turn ratio is 50. The frequency for testing the samples 50 kHz, which a microcontroller can control. Because the breakdown voltage of the samples is dependent on these sharp overshoots, the pulse overshoot should be kept to a minimum. The transformer should provide repeating pulses with no interruptions. This will improve the testing qual-

ity. Variable resistance and capacitance were connected as indicated in figure 3.1 to provide uniformity in the shape of the pulse output when the parameters are changed. High voltage performance should be adequate; to minimize output wave disruptions caused by discharges between primary and secondary or windings to the core. The desired transformer parameters are listed in the table 4.1.

Specifications	**value**
DC link Voltage V_in	200 V
Output Voltage V_{out}	10 kV
Pulse Duration T_p	100 - 20 µs
Frequency f_s	10-50 kHz
Rise Time T_r	2%
Overshoot ΔV_{max}	0-5%
Turns ratio n	1:50

Table 4.1: Specifications of pulse transformer

4.2.1. Core material

As previously stated, the frequency used for this application is 50 kHz. The magnetic material under consideration must be high-frequency compatible. The choice of core materials is critical since it determines cost, volume, and efficiency. As a result, it is essential to realize magnetic material characteristics. Properties such as relative permeability and saturation flux density are critical for this application since they determine the possible bandwidth and hence the performance of the pulse transformer. However, for high-frequency applications, core loss density should also be addressed. If the material has a greater saturation flux density, the cross-section of the material can be lowered, resulting in fewer parasitics and hence faster rising times. [71]. Ferrite, silicon steel, amorphous, and nanocrystalline materials are common in high-frequency applications. The common properties of the materials indicated above are listed in the table. 4.2.

Ferrite is a typical material used in high-frequency applications. It has a low satura-

Parameter	**Ferrite**	**Silicon Steel**	**Amorphous**	**Nanocrystalline**
P_{fe}(W/kg) @ 20 kHz, 0.2 T	19	420	45	10
B_{sat}(T)	0.48	1.52	1.55	1.3
Permeability @ 20 kHz,	2000	8000	10k-150k	25k

Table 4.2: Comparison of typical properties of magnetic material

tion flux density, which results in a bulkier transformer. The advantage, though, is its

low cost. Silicon steel has a higher saturation flux and permeability than ferrite, but core losses are significant in high-frequency applications because of eddy current. Some manufacturers provide cores constructed of advanced silicon steel with very thin laminations suitable for medium-frequency applications. Amorphous materials appeal to high-frequency applications because they have higher saturation flux, loss core loss density, and permeability; they offer a superior blend of reduced losses and high permeability. Finally, nanocrystalline materials have the best properties, with a high saturation flux and a low core loss density. However, due to the production process, nanocrystalline is pricey. Most nanocrystalline cores are toroidal, which is inconvenient for this purpose. Specific nanocrystalline core forms are possible with a unique manufacturing technique, which raises the cost. Considering all the factors mentioned above, the ferrite core is the cheapest and most widely accessible material, whilst other materials are either prohibitively expensive or unavailable. This thesis uses the TDK N87 (MnZn ferrite) core, which is the only core available on the market suitable for this thesis. The dimensions of the core are given in the figure 4.6. The relative permeability of this core is 1900.

■ For power transformers >1 kW (20 kHz)

Magnetic characteristics (per set)

	UU 126/182/20	UI 126/119/20	
$\Sigma l/A$	0.86	0.63	mm^{-1}
l_e	480	354	mm
A_e	560	560	mm^2
A_{min}	560	560	mm^2
V_e	269000	198000	mm^3
m	1300	950	g/set

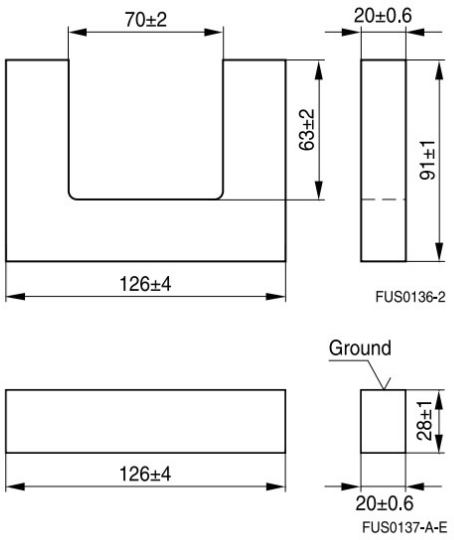


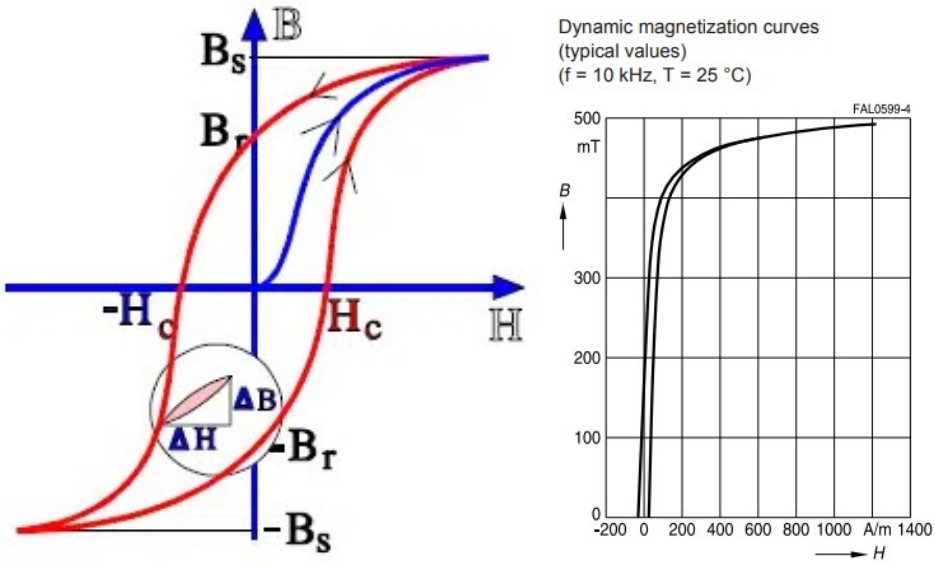
Figure 4.6: Dimensions of TDK N87 core, [72]

Core Losses

High-frequency losses in the core are caused mainly by hysteresis and eddy current. When a voltage is applied to the primary, the flux created will be alternating due to the alternating pulse nature of the source. During the source shift, the magnetic domains re-orient

themselves. When the core is subjected to a magnetic field of strength H, As illustrated in the figure 4.7a, the flux increases and approaches saturation B_{sat} by following the path (1). When the field is withdrawn, the flux does not return to zero but instead settles at the location B_r, known as residual flux. A coercive field H_c must be provided to make this flow zero. If the field is raised further in the negative direction, the flux approaches saturation again, but this time in the negative direction. The path is followed until it reaches the point H_c and closes the hysteresis loop. Each time the magnetic field reverses direction, there is energy loss known as hysteresis loss.

Eddy-current losses are another sort of loss in the core. These losses are caused by the voltage produced inside the core due to electromagnetic induction, as indicated by Faraday's law, which is comparable to the voltage induced across the windings. However, because the conductivity of the ferrite core is low, these losses are minimal for this core. Because the application for this thesis is just using pulses till breakdown, which is not a continuous operation, losses are not an issue, although few samples can take long time than expected. On the other hand, ferrites do not dissipate much energy since they are explicitly designed for high-frequency applications. The TDK N87 data sheet provided a graph showing relative core losses with respect to frequency, and the losses were displayed as shown in the figure 4.8. If the loss density at $20kHz$ is $200kW/m^3$, the total core loss is $0.645kW$, however, loss can be low with increase in temperature and when the flux density is less.



(a) Typical hysteresis loop of a magnetic core [73]

(b) Hysteresis loop of N87 by TDK [74]

Figure 4.7: Hysteresis loop

$$P_{Total} = Relative\ coreless \times Total\ volume\ of\ the\ core \tag{4.6}$$

$$P_{Total} = 300kW/m^3 \times 269000 \times 10^{-9} \times 8 = 0.645kW \tag{4.7}$$

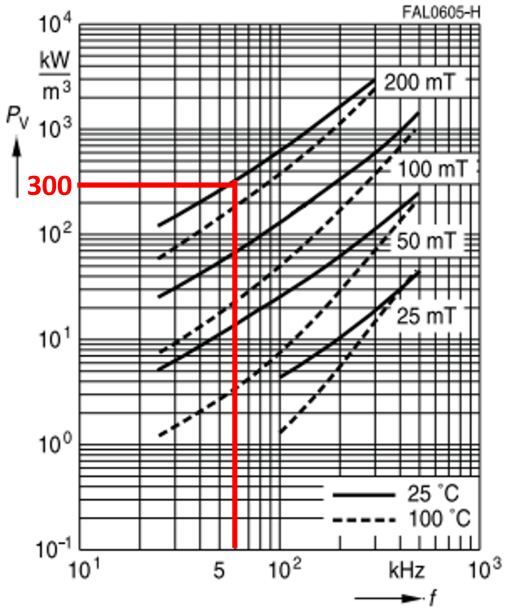


Figure 4.8: Realtive coreloss vs frequency by TDK [74]

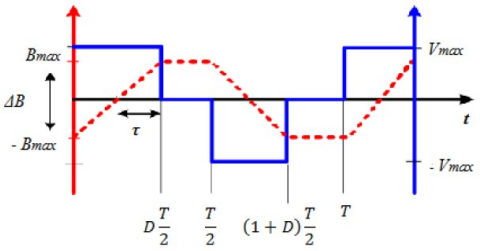


Figure 4.9: magnetic flux swing under bipolar pulse excitation [44]

Methods to avoid core saturation

The flux swings with bipolar pulse input as shown in the figure 4.9. The peak to peak flux density ΔB is given in the equation 4.8 [44].

$$\Delta B = \frac{V_{pri} \cdot T_{on}}{N_1 \cdot A_c} \tag{4.8}$$

Where ΔB represents the flux swing from peak to peak, which equals $2B_{max}$, the transformer's primary voltage is V_{pri}. T_{on} is the output pulse width, which is 50 µs for 10 kHz. The number of primary turns is N_1, and the core size is A_c. This equation may calculate the minimal number of turns of the primary side. According to the TDK N87 data sheet, the maximum saturation flux density for the material used is about $480mT$. The picture 4.7b depicts the hysteresis loop of this material at $25°C$ and frequency $10kHz$. It is usually preferable to select a saturation flux density somewhat less than the maximum saturation flux to guarantee that the core does not attain saturation in any situation. As a result, the

chosen saturation flux is $400mT$. The minimum number of primary turns that can be wound is.

$$N_1 = \frac{V_{pri} \cdot T_{on}}{2B_{max} \cdot A_c} \tag{4.9}$$

$$N_1 = \frac{200 \times 50 \times 10^{-6}}{2 \times 0.4 \times 560 \times 10^{-6}} \approx 23 \tag{4.10}$$

This indicates that the primary turns must be greater than 23 to avoid core saturation. The primary turns determine the secondary turns, and the secondary turns required to achieve 10 kV for a primary voltage of 200 V are $23 \times 50 = 1150$. The literature well documented that fast-rising times demand low leakage inductance and low distributed capacitance. The leakage inductance increases as the number of secondary turns increases, although the core size and hence the transformer volume may be lowered. However, a slightly larger pulse transformer is permitted for this application to obtain the fast rise required for testing. As a result, the leakage inductance may be minimized by reducing the secondary turns. To do this, the primary turns need to be reduced as well. This can only be accomplished by expanding the cross-section area of the core. As a result, 16 cores are stacked to enhance the effective cross-section of the core. The lower half of the arrangement can be seen in the figure. 4.10.

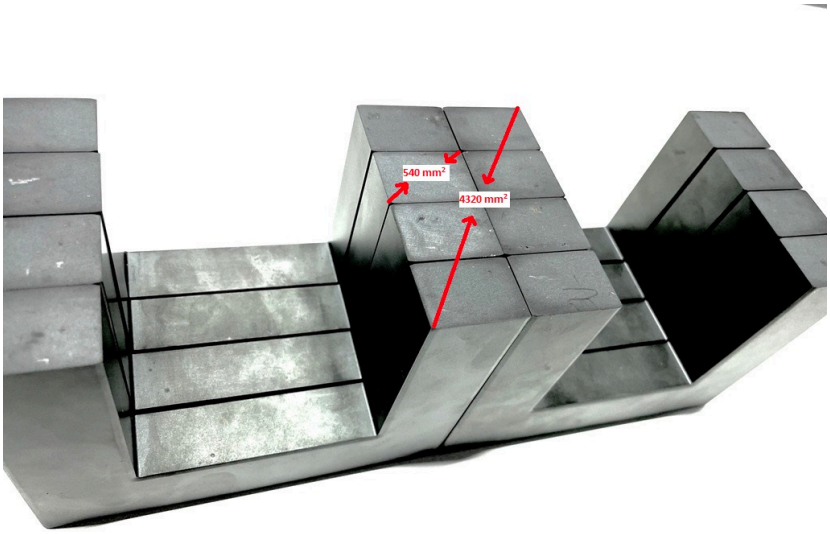


Figure 4.10: Lower half of the 16 core arrangement

The core's effective cross-section area rose from $540mm^2$ to $4320mm^2$. The minimal number of primary turns is now three, resulting in secondary turns of 150 while retaining a turn ratio of 50. By expanding the cross-section area of the core, the number of turns was reduced significantly.

$$N_1 = \frac{200 \times 50 \times 10^{-6}}{2 \times 0.4 \times 560 \times 10^{-6} \times 8} \approx 3 \tag{4.11}$$

4.2.2. Prediction of the Pulse

A pulse transformer is typically step-up; therefore, the secondary turns are inherently larger. Along with increased secondary turns, a space between primary and secondary windings should be maintained to provide better high voltage performance, such as avoiding discharges that would distort the output waveforms. These two requirements impact transformer parasitics; leakage inductance and distributed capacitance. These parasitics have an influence on the transformer's output, increasing the pulse rise time, overshoot, and oscillations. To achieve the required performance for this application, the transformer parameters that significantly impact performance must be extracted. The transformer transmits transient pulses; these parameters are critical in determining transformer performance. Maxwell's equation may be employed in terms of magnetic and electric fields to realize the parameters. However, this technique is rigorous and not practical for complicated geometries like that in this application. [75] provided simpler formulae for leakage inductance and distributed capacitance. These equations cannot be generalized since they only apply to specific geometries. The most straightforward technique to simplify the problem is to approximate the fields using a lumped circuit. Overall, the lumped circuit parameters must be extracted before building the transformer to predict the pulse shape. This saves time and money in transformer design by eliminating numerous trial and error iterations and avoiding material waste throughout iterations.

4.2.3. Equivalent circuit

The IEEE standard for pulse transformers [42] defines the lumped circuit, which is also an equivalent pulse transformer circuit. The fields can be approximated using this circuit. The circuit is depicted in the figure 4.11. Because both types of transformers transmit waveforms with a wide variety of frequencies, this circuit may be utilized for both pulse and wide-band transformers. The primary distinction is that the pulse transformer performance is evaluated in the time domain. The majority of the characteristics are the same for both types of transformers. On the other hand, capacitances are determined owing to voltage distribution, which is determined by the type of excitation. As a result, the capacitance should be extracted very carefully.

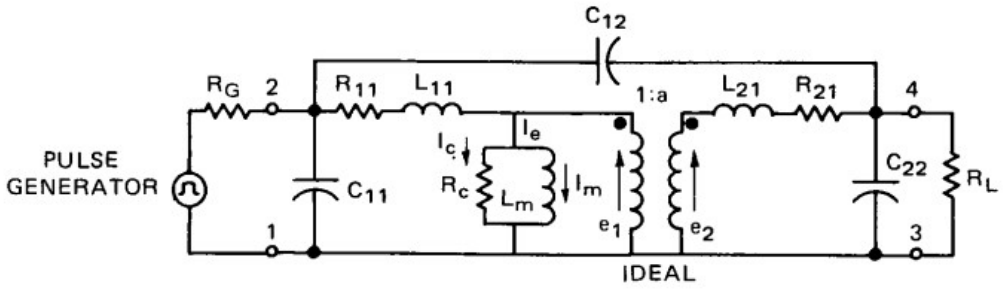


Figure 4.11: Equivalent circuit of Pulse Transformer [42]

Symbol	Term Denoted
R_{11}	Primary winding Resistance
L_{11}	Primary winding Leakage Inductance
C_{11}	Primary intra winding Capacitance
R_C	Core Resistance
L_m	Magnetising Inductance
C_{12}	Inter winding capacitance
L_{21}	Secondary winding Leakage Inductance
R_{21}	Secondary winding Resistance
C_{22}	Secondary intra winding Capacitance

Table 4.3: Parameters of the Pulse Transformer equivalent circuit

4.2.4. Extraction of the equivalent circuit parameters

A pulse transformer model is required to retrieve the parameters. As a result, a random transformer (T1) is built. All parameters retrieved using this transformer and how they are extracted are detailed in this section. The same approach was used on the other pulse transformer (T2), which was available in the lab to validate the results. T1 is a random transformer with 267 turns on the secondary and four on the primary. The secondary of the second transformer (T2) has 200 turns while the primary has four turns.

On the other hand, the volume of the transformers is highly different, and each transformer has different winding distances and diameters. The transformers are depicted in the diagram 4.12. The first random transformer (T1) is tested using bipolar excitation, and the results are given in Figure 4.13. According to the figure, random design produces terrible results. The output is ringing and is not the desired output for the application.

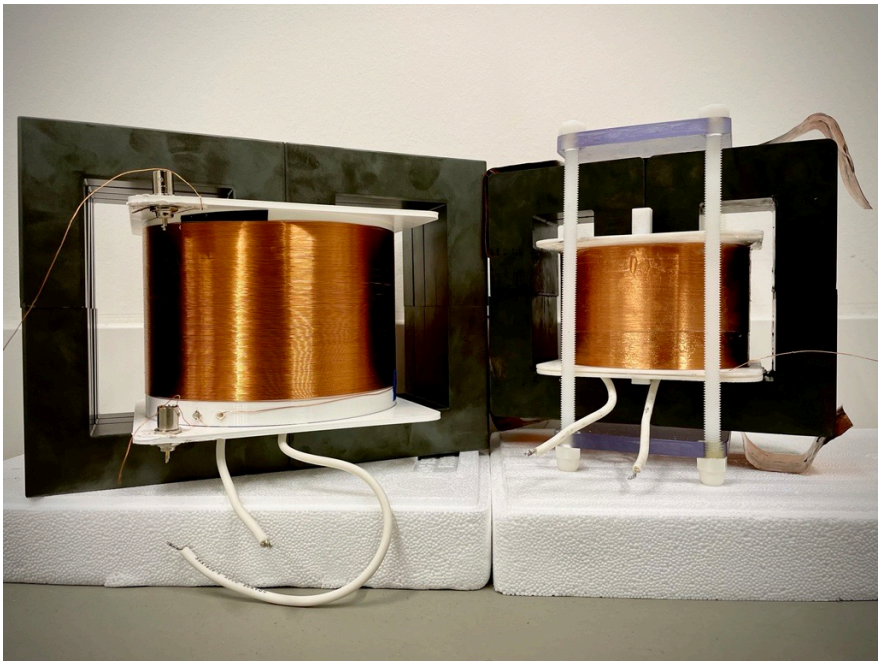


Figure 4.12: Transformers used to extract the parameters

Frequency Domain Impedance data using Vector Network Analyser (VNA)

This method is based on an analytical approximation of frequency-based impedance data from a no-load test with a secondary winding that is open-circuited. Four distinct fre-

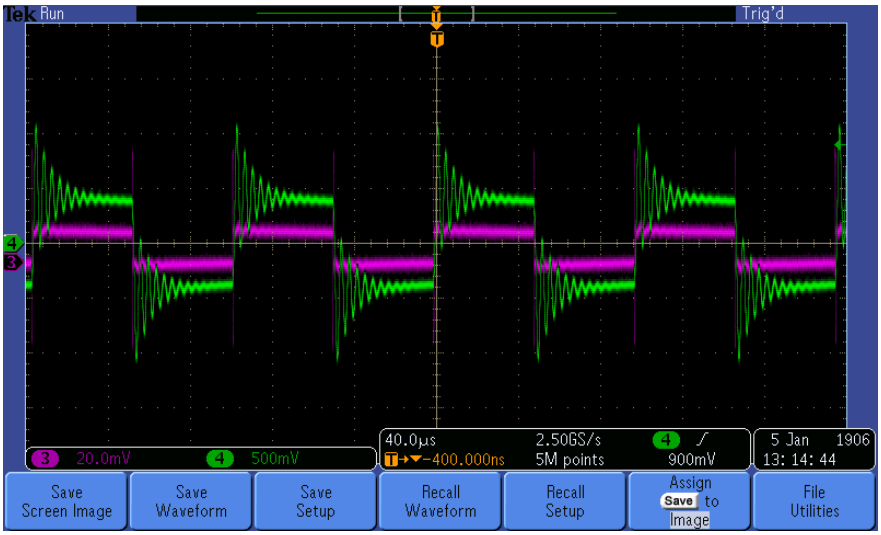


Figure 4.13: Output of the Transformer (T1)

quencies resonate with different components of the lumped circuit. Except for primary intra-winding capacitance, this method can measure all parameters. However, according to [76], primary intra-winding capacitance is not crucial in the pulse transformer design. The parameters obtained by this method are for the equivalent circuit that is referred to the primary side, as seen in the figure 4.14. Capacitances, as previously indicated, play an essential role in shaping pulse form. The primary capacitances can be calculated by equating the electrostatic energy of the referred circuit to the standard equivalent circuit.

$$C_{11}V_1^2 + C_{12}(V_2 - V_1)^2 + C_{22}V_2^2 = C'_{11}V_1^2 + C'_{12}(aV_2 - V_1)^2 + C'_{22}(aV_2^2) \tag{4.12}$$

This relationship is true regardless of the applied voltage. As a result, equivalent capacitances on the primary side can be calculated.

$$(C_{11} + C_{12})V_1^2 + (C_{12} + C_{22})V_2^2 - 2V_2V_1C_{12} = (C'_{11} + C'_{12})V_1^2 + (aC'_{12} + aC'_{22})V_2^2 - 2aV_2V_1C'_{12} \tag{4.13}$$

The following capacitance values can be obtained by solving equation 4.13.

$$C'_{11} = C_{11} + C_{12}\frac{a-1}{a} \tag{4.14}$$

$$C'_{22} = \frac{C_{22}}{a^2} + C_{12}\frac{1-a}{a^2} \tag{4.15}$$

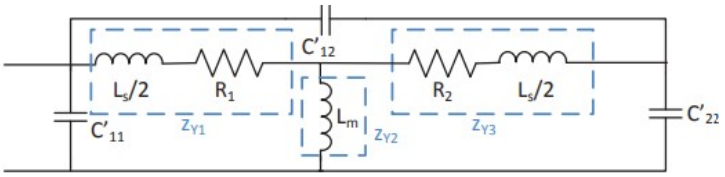


Figure 4.14: Equivalent circuit referred to primary [76]

Frequency	Expression
f_o	$\frac{R_1}{2\pi L_m}$
f_1	$\frac{1}{2\pi\sqrt{L_m C'_{22}}}$
f_2	$\frac{1}{2\pi\sqrt{L_s C'_{22}}}$
f_3	$\frac{1}{2\pi\sqrt{L_s C'_{12}}}$

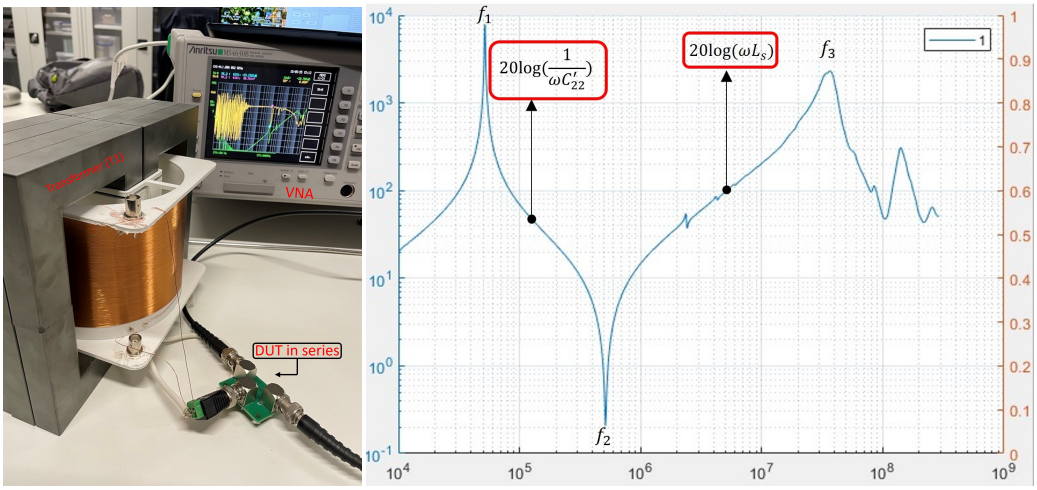
Table 4.4: Expression of the frequencies in function of the parameters

$$C'_{12} = \frac{C_{12}}{a} \tag{4.16}$$

The frequencies at which these parameters resonate are listed in the 4.4 table. The first frequency f_0 is used to calculate the primary resistance. The frequency f_1 is the resonant frequency between magnetising inductance and secondary intra-winding capacitance, referred to the primary side, and other frequencies resonate similarly, as given in the table 4.4. Below f_1, which is relatively lower frequency, magnetising inductance and secondary intra-winding capacitance resonate since they are typically higher values. On the other hand, the primary and secondary intra-winding capacitances resonate at higher frequencies since their values are often smaller.

This method is applied to the transformer (T1) using the Vector Network Analyzer (*Anritsu MS4630B*). The setup and result are shown in the picture 4.15. As can be seen from the results, the response began at 10 kHz and terminated at 300 MHz. There is a linear part in the response after each resonance. For example, the frequency f_2 resonates between leakage inductance and secondary intra-winding capacitance. The response before this frequency is mostly due to capacitance, which can be calculated using the linear portion of the response as indicated in the figure; similarly, the response after this frequency is inductive. The response is distorted after a frequency of about 30 MHz. This phenomenon occurs because parasitic capacitance's impact at these frequencies is relatively high, as are the capacitances across windings to air. Because this distortion occurs

after the resonance frequency f_3, which should be between total leakage inductance and inter-winding capacitance, calculating c_{12} is difficult. The value c_{12} is crucial in transformer design. As a result, while this approach is simple for measuring parameters, it cannot be used on this transformer.



(a) Test setup (b) Result on Transformer (T1)

Figure 4.15: Frequency domain impedance measurement

Individual extraction of parameters using VNA

Leakage inductances can be measured directly by an LCR or VNA. Normal LCR, on the other hand, cannot be used to measure capacitances, and that can only be done with VNA but with different configurations. This section provides two examples of how to measure the parameters (one inductance and one capacitance), the challenges encountered during measuring and how to overcome them.

Leakage Inductance referred to primary

The leakage inductance can be measured on either the primary or secondary sides. Both procedures are the same. Figure 4.16 depicts the connection and analytical solution for measuring the leakage inductance on the primary side. When measuring from the primary, secondary terminals were short-circuited. When referring to the primary side, the resistance of the secondary winding can be neglected because its value is nearly as short-circuited. The core loss resistance can also be ignored because its value is very high as core losses are low in the case of ferrite cores. When referred to the primary, the secondary leakage inductance L_2 will be connected in parallel to the magnetizing inductance L_{mag}. The equivalent inductance is the parallel combination of the magnetizing

inductance, and secondary inductance referred to primary. This equivalent inductance is almost equal to the secondary inductance, referred to primary, since the value of secondary inductance is too tiny compared to the magnetizing inductance. When connected across VNA terminals, this connection measures the series combination of primary resistance R_1, inductance L_1, and the equivalent inductance of the parallel combination of magnetizing inductance and secondary leakage inductance referred to the primary side. The frequency applied is relatively low to keep the influence of parasitic capacitors small. The total leakage inductance referred to on the primary side is the inductance value when the phase angle is 90 degrees. Similarly, magnetizing inductance L_{mag} may be determined by repeating the method when the secondary is open-circuited. These values can also be measured with an LCR meter; in this case, the *keysight U1733C* was utilized.

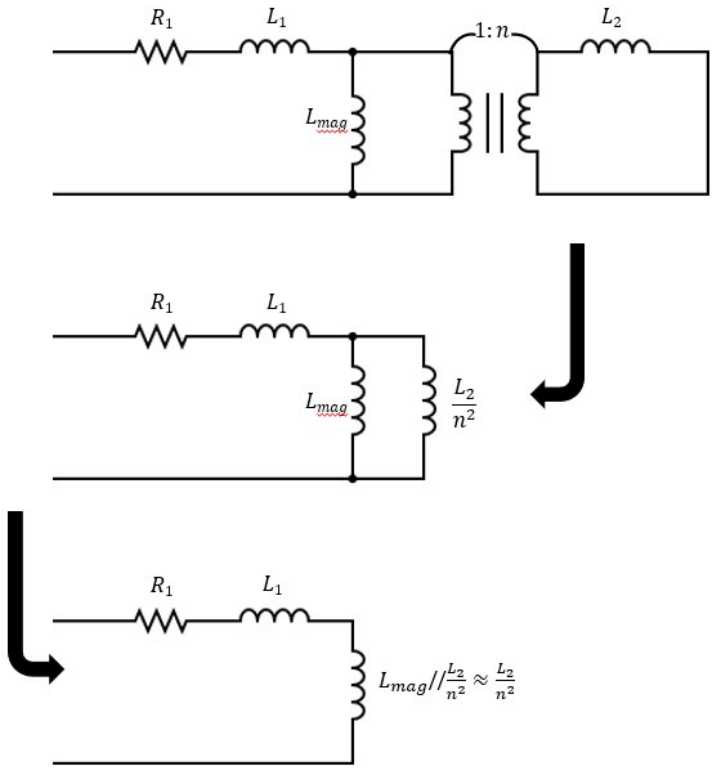


Figure 4.16: Equivalent circuit when Leakage inductance referred to primary

Secondary intra-winding capacitance C_2

Before measuring the secondary intra-winding capacitance C_2, the interwinding ca-

pacitance C_{12} should be measured first. C_{12} can be directly measured by shorting the primary winding terminals together, and secondary winding terminals together and measuring the capacitance as per [42]. Because the transformer is shortened on both sides, the impact of the other parameters is minimal. The capacitive elements are measured using the frequency sweep technique. At higher frequencies, capacitance can be measured more accurately.

The primary must be short-circuited in order to determine the secondary's intra-winding capacitance. Both the primary and secondary cold ends are shortened. Following these connections, the equivalent circuit of the device under test is shown in the figure 4.17. The resistance of the windings was ignored because of the relatively high frequencies employed for this test. As a result, the winding impedance is many orders of magnitude bigger than its resistance.

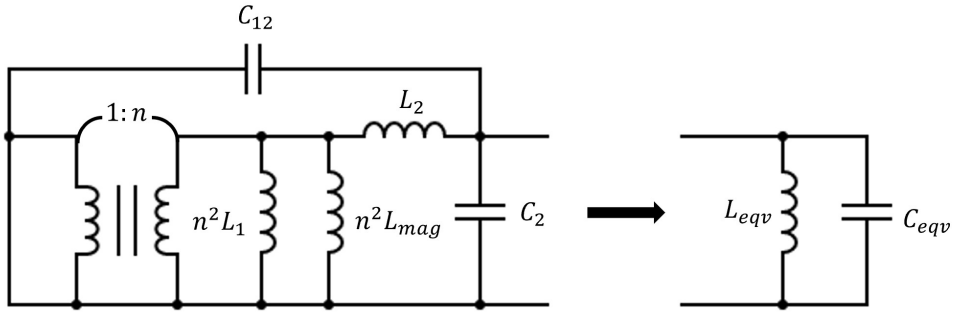


Figure 4.17: Equivalent circuit for secondary intra-winding capacitance C_2 and its equivalent parallel resonant circuit.

As illustrated in the figure 4.17, the equivalent circuit may be consolidated as a parallel resonant circuit. The L_{eqv} is a combination of three inductances: the primary leakage inductance, the magnetising inductance, which are connected in parallel, and the secondary leakage inductance, which is connected in series. The parallel combination of inter-winding capacitance C_{12} and secondary intra-winding capacitance C_2 is C_eqv.

$$C_{eqv} = C_{12} + C_2 \tag{4.17}$$

$$L_{eqv} = L_2 + \frac{n^2 \cdot L_{mag} \cdot L_1}{L_{mag} + L_1} \tag{4.18}$$

When this parallel resonant circuit impedance is measured, the inductance and capacitance resonate at a resonant frequency. The resonant frequency is depicted in the figure. 4.18.

$$\omega_r = \frac{1}{\sqrt{L_{eqv}C_{eqv}}} \tag{4.19}$$

Using the equation 4.19, the C_{eqv} can be calculated.

$$C_{eqv} = \frac{1}{\omega_r^2 \cdot L_{eqv}} \tag{4.20}$$

Finally, the secondary intra winding capacitance is:

$$C_2 = C_{eqv} - C_{12} \tag{4.21}$$

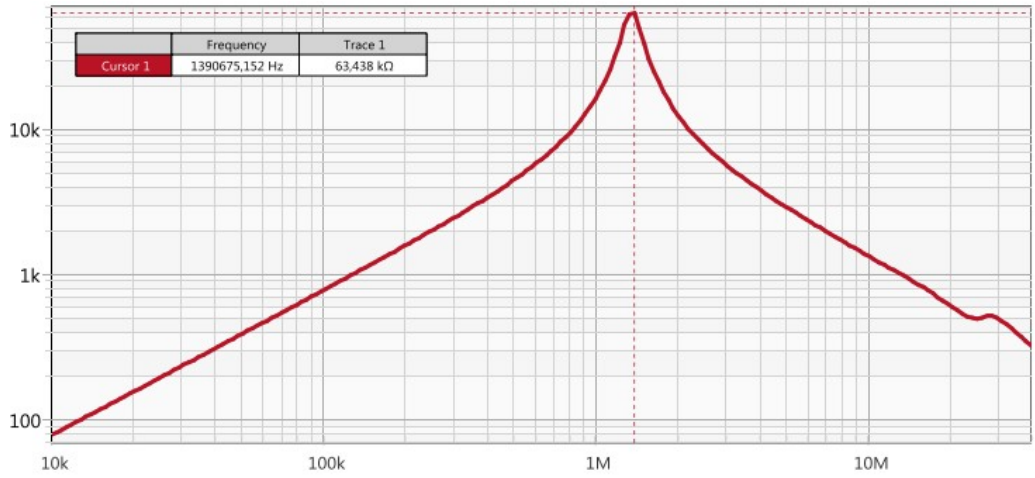


Figure 4.18: Resonant peak of the parallel resonant circuit.

The issue with this approach is that the C_{eqv} value is smaller than C_{12}, which should not be the case. This phenomenon returns the negative value of C_2. This problem might be because, at higher frequencies, where capacitances are often measured, other parasitics may contribute to the existing capacitor, lowering the total value. This phenomenon occurred with both transformers. This issue is resolved in the section that follows.

Solution to find Secondary intra-winding capacitance C_2

The secondary winding wound on a bobbin took out from the core. This was done to eliminate the effects of other parameters within the transformer. The inductance of this winding should be measured without the core, as it will be different to the inductance when the core is present. The resultant equivalent circuit is also a parallel resonant circuit. The resistance of the winding can be neglected as high frequency is used while measuring

capacitance. A resonant frequency can be obtained when the impedance is measured on this resonant circuit, similar to the previous case. Since the inductance of the winding has already been measured, the secondary intra-winding capacitance can be calculated by:

$$C_2 = \frac{1}{\omega^2 L} \tag{4.22}$$

Typically, the capacitance of the secondary intra-winding capacitance is relatively tiny [70]. In the case of the transformer, it is comparable to the capacitance of the connector used to connect the Device Under Test (DUT) in series. So the calculated capacitance is the combination of secondary intra-winding capacitance and the connector's capacitance. This problem can be avoided by shorting the connector while calibrating. When the connector is included in calibration by shorting, as shown in the figure 4.19, the capacitance of the connector will be included in calibration and not be measured along with the DUT. Now the same procedure is followed, and capacitance C_2 was calculated. As stated earlier, capacitances cannot be measured using LCR, so how can this value be validated? To answer this, COMSOL was used. The following section discusses COMSOL modelling.

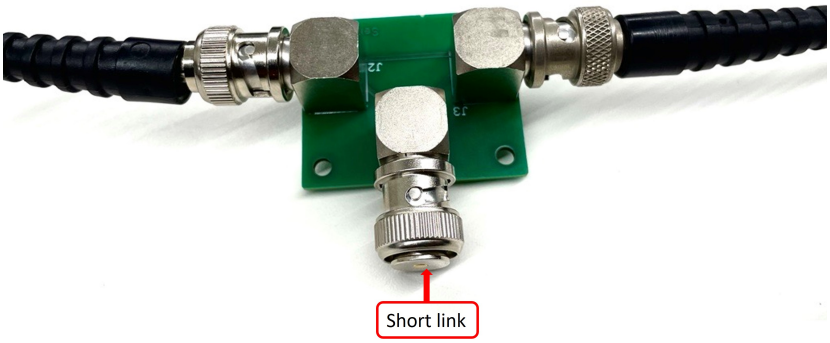


Figure 4.19: VNA connector calibration by a short link.

COMSOL modelling

COMSOL can simulate a wide range of physics, including magnetic fields and electrostatics, which are utilized to extract parameters. In the solution domain of time-invariant magnetic problems, COMSOL fulfils the following equations.

(Amperes Circuital Law)

$$\nabla \times H = J \tag{4.23}$$

(Gauss's Law for Magnetism)

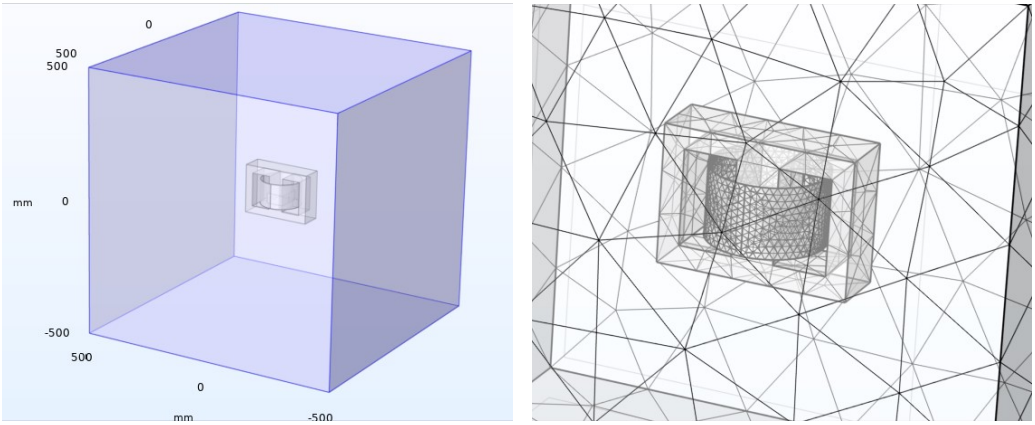
$$\nabla \cdot B = 0 \tag{4.24}$$

$$\mu = \frac{B}{H(B)} \tag{4.25}$$

$$B = \nabla \cdot A \tag{4.26}$$

Where A is magnetic vector potential.

The geometry for all the above equations will be solved in COMSOL. It is essential to understand the equations. COMSOL, on the other hand, executes all of the essential computations. Because the whole magnetic energy to determine leakage inductance is only present between the two windings, 3D geometry was designed to obtain the parameters. Estimating leakage inductance in 2D is inaccurate. In the 2D-axis, the leakage inductance might be near-accurate, but not the capacitances, since the core will spin together with the windings and the electric field cannot escape outside the core in this scenario, which is not the case in practice. The created 3D geometry is illustrated in the image.4.20a. The coil model is a homogeneous multi-turn coil because a single conductor coil requires a dense mesh to achieve the skin effect, which takes a long time to solve. The electrical conductivity for ferrite and air is given non-zero values in the "materials" module to prevent difficulties in converging, which is essential for 3D simulations. The windings are densely meshed for accuracy, whereas the core is somewhat less densely meshed than the coils. Because it is not expected that the air would have a large magnetic field farther from the transformer, it is coarsely meshed. The meshing can be seen in the image 4.20b.



(a) 3D geometry used for COMSOL simulation

(b) Meshing of the geometry

Figure 4.20: COMSOL geometry and meshing

The skin effect and the influence of the magnetic field in the core considerably en-

hance the value of resistance at higher frequencies; extracting resistance using COMSOL is challenging. Because the coil type employed was homogenous multi-turn, which does not result in skin effect, extracting resistance with COMSOL is inaccurate. Extraction of precise resistance is not required for this type of transformer since it simply affects the dampening of the output wave and has a negligible influence on the pulse rise time. LCR and VNA can be used to measure resistance at higher frequencies. With LCR, the resistance value fluctuates, and it is not easy to establish a consistent value. In contrast, using VNA, a constant resistance value may be obtained by increasing the number of measuring points and averaging the value. To get correct resistance values in COMSOL, the coils should be 3D single-conductor models, and after simulation, the total losses on each winding may be estimated and resistance extracted using the equation 4.27.

$$P = \frac{U^2}{R} = I^2 R \tag{4.27}$$

The physics *Magnetic Fields (mf2)* was used to extract leakage inductance. For the primary and secondary windings, homogeneous multi-turn coils were applied. The secondary should be short-circuited to extract the leakage inductance referred to the primary. The secondary coil is excited with voltage to replicate the short circuit, and the value is set to zero. The primary is excited with the current. The leakage inductance, referred to the secondary, can be extracted by doing the same, but in the opposite direction. The number of turns for both windings can be specified in the coil settings. The current direction should be the same as the voltage direction on the secondary coil. If the model is not converging, including *Gauge Fixing For A Field* might help. A *coil geometry analysis* must be performed before the study, which estimates the geometry of the coils, such as length and resistance. After simulation, the leakage inductance may be estimated by integrating the stored magnetic energy in the leakage field. The figure 4.21 illustrates the magnetic flux density norm 3D plot 4.21.

$$E_{mag} = \frac{1}{2} L I^2 \tag{4.28}$$

In COMSOL, under Derived values, volume integration was done, as follows.

$$L_{11} = \int\int\int (2 * mf.Wmav)/(1[A^2]) \tag{4.29}$$

From the figure 4.21, it can be seen that the magnetic flux density is almost confined within the core, and the leakage is present significantly between the coils. From this, it can be concluded that the gap between primary and secondary should be minimal to achieve less leakage inductance. However, if we go very near to primary, the voltage difference between the coils might cause high voltage problems. In addition, the inter-winding capacitance will also increase with a minimized distance. A trade-off analysis should be done for the optimum distance between primary and secondary.

The *Electrostatics (es)* physics was utilized to obtain capacitances. The conductor's per-

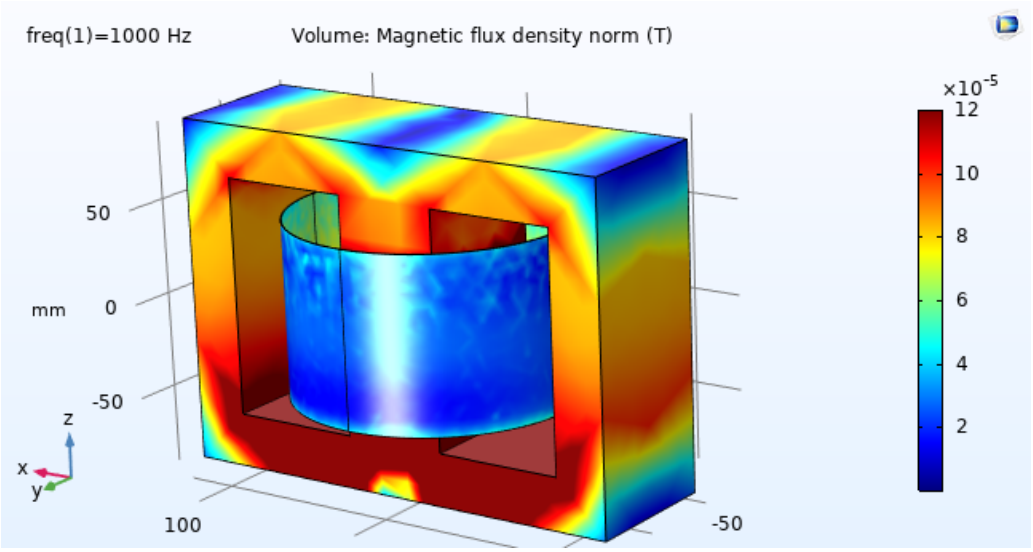


Figure 4.21: Magnetic Flux Density Norm

mittivity should be given a very high value in the materials section so that COMSOL recognizes it as a conductor. To obtain the inter-winding capacitance C_{12}, the primary and secondary windings should be short-circuited, with the primary excited with voltage and the secondary excited with the ground. To mimic this, the top and bottom boundaries of the primary winding should be provided with the same voltage. The secondary top and bottom boundaries should be grounded. The capacitance may be computed after simulation by integrating the electric energy. The graphic 4.22 depicts the electric potential distribution after electrostatic simulation.

$$E_{elec} = \frac{1}{2}CV^2 \tag{4.30}$$

In COMSOL, under Derived Values, volume integration was done as follows.

$$C_{12} = \int\int\int (2 * es.Weav)/(1[V^2]) \tag{4.31}$$

The figure 4.22 shows that the core induces voltage owing to its conductivity, known as floating potential. It is usually best to ground the core to eliminate such floating potential. For the same reason, grounding will be provided to the final transformer while testing.

To avoid the impact of other parameters while calculating intra-winding capacitance C_2, just the coil without a core should be simulated. The voltage should be applied linearly

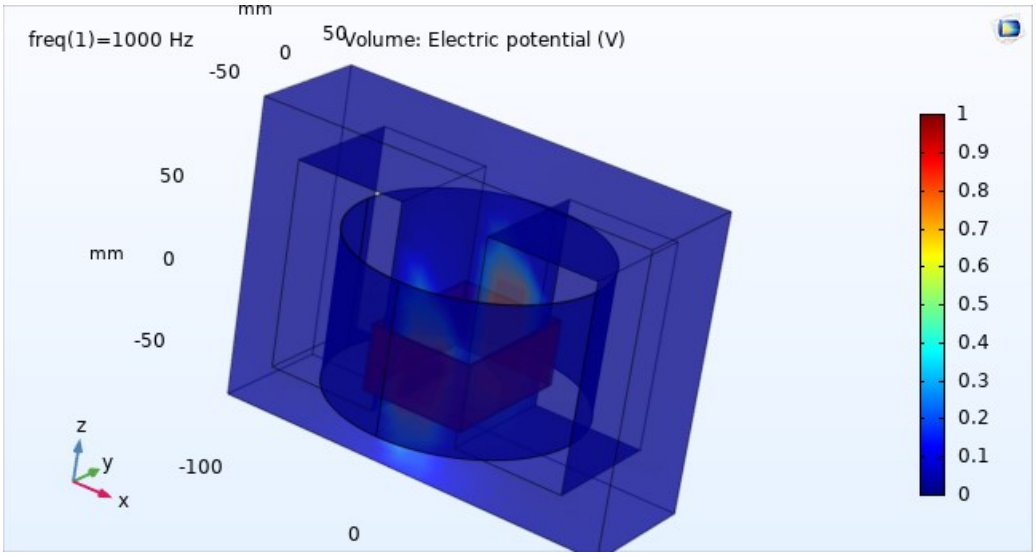


Figure 4.22: Electric potential (V)

from top to bottom; to achieve this, the top boundary should be provided with voltage and the bottom boundary with the ground. The figure 4.23 depicts the linear voltage distribution. When integrating the electrical energy to compute capacitance, the conductor domain should not be included since the conductor contains most of the electrical energy, and only the energy between turns is required to obtain the intra-winding capacitance value.

4.2.5. Simulink Model

The extracted parameters from the preceding section were utilized to simulate the pulse transformer output. The replication of the typical equivalent model displayed in 4.11 is a simulation model. The simulation model's output will be compared to the laboratory test output on the real transformer. In this design, the leakage inductance is either wholly referred to the primary or secondary side; this is due to the increased precision and the fact that measuring individual leakage inductances for both primary and secondary is more complex than measuring or computing leakage inductance referenced to either side. The Simulink model is depicted in the picture 4.24.

Because the core employed in this model is ferrite and losses are expected to be minimal, core loss resistance was ignored. This parameter has the minimum effect on the pulse output. The leakage inductance can also be connected on the secondary side; the results are similar in both situations. However, it is found that referring the leakage in-

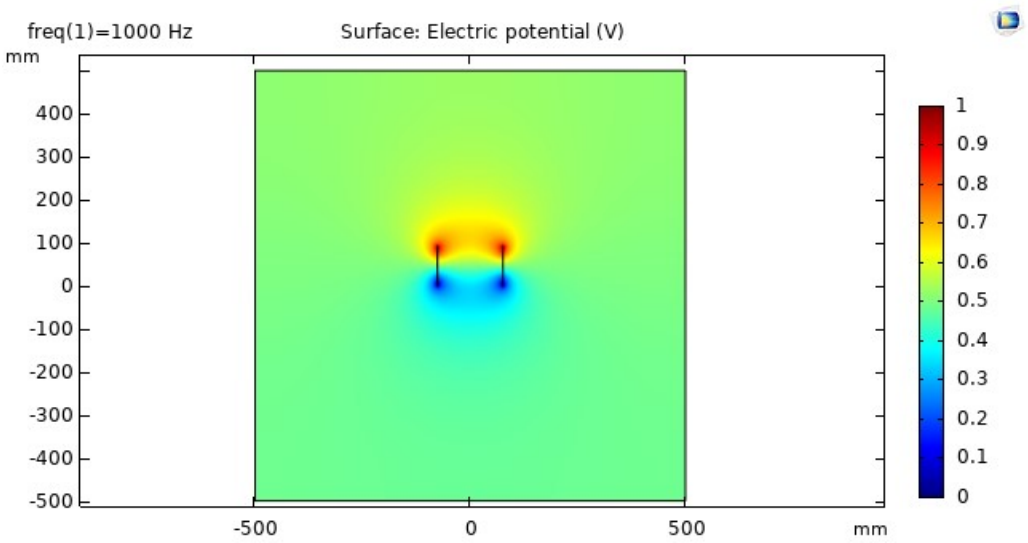


Figure 4.23: linear distribution of Electric potential (V)

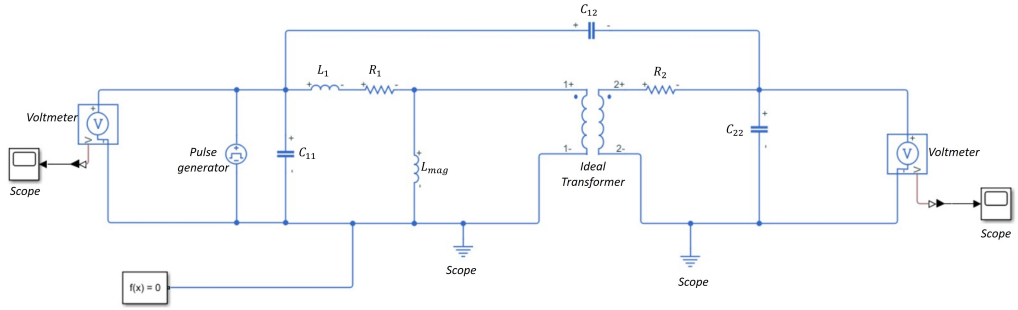


Figure 4.24: Simulink model to predict the pulse

	R_1	R_2	$L_{11}(\mu H)$	$L_{mag}(\mu H)$	$C_{12}(pF)$	$C_{22}(pF)$
LCR	0.46	600-1200	3.6	304	17.78	-NA-
VNA	0.51	750	3.5	296	16.17	2.2
COMSOL	-NA-	-NA-	3.8	292	17.224	1.646

Table 4.5: Parameters of Transformer T1

	R_1	R_2	$L_{11}(\mu H)$	$L_{mag}(\mu H)$	$C_{12}(pF)$	$C_{22}(pF)$
LCR	0.4	100-400	3.4	230	15.43	-NA-
VNA	0.45	350	3.6	233	14.12	1.8
COMSOL	-NA-	-NA-	3.78	236	14.42	1.18

Table 4.6: Parameters of Transformer T2

ductance to the secondary side provides more freedom when modifying the values during optimization because the value on the secondary side is significantly bigger than the value on the primary side due to the higher number of turns. The ideal transformer model was selected since all the elements that cause losses are already modelled as inductances, resistances, and capacitances. A pulse generator is connected to give repeating pulses with the possibility of changing the rise and fall timings, frequency, and amplitude. The results were read and shown using voltmeters and scopes, respectively.

4.2.6. Results of parameter extraction and Simulink model

Parameters for the two transformers, T1 and T2, were extracted using various approaches, such as an LCR meter, a Vector Network Analyzer, and simulation with COMSOL. Three approaches were employed to validate the results; specific parameters can only be measured using any two of them. Resistances were not modelled in COMSOL since they require a long time to simulate. Also, resistance has no substantial influence on pulse output, which primarily aids in dampening the output pulse, which can be modified later by using the test resistance. Higher frequency resistance is difficult to measure using LCR. This problem may be handled with the Vector Network Analyzer by averaging and increasing the number of measurement points until a constant value is obtained. Leakage inductance can be measured using all three techniques, but capacitances, particularly intra-winding capacitances, cannot be measured using LCR since they are frequency sensitive. As a result, they were measured and validated using VNA and COMSOL. The results of both transformers used in the Simulink model are shown in the tables 4.5 and 4.6.

The two transformers were tested physically, as the setup is shown in the figure 4.25. It does not contain test parameters such as R_t and C_t and load. An oscilloscope is connected to the transformer's terminals to acquire the transformer's response. The frequency was set at 10 kHz in the Micro Controller Unit (MCU).

The response from the oscilloscope and the output from the simulink of two trans-

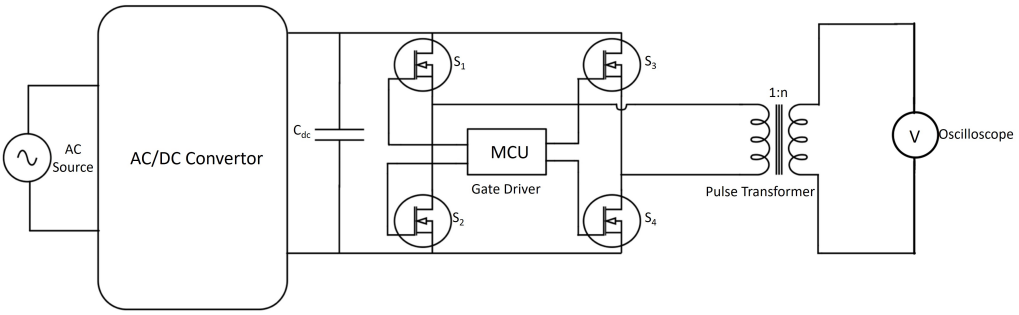
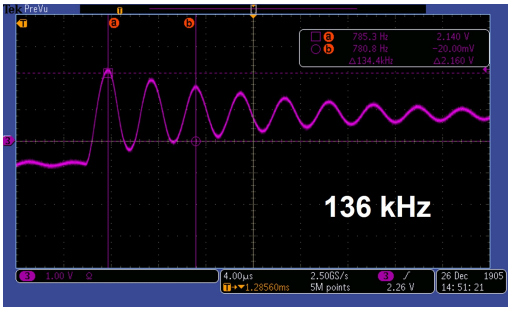
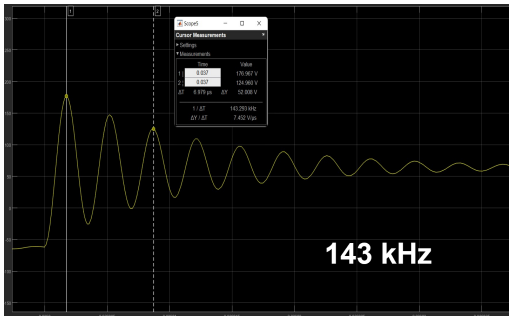


Figure 4.25: Test setup used to find the response of transformer

formers is shown in the figures 4.26 and 4.27



(a) Response of physical Transformer T1 from Oscilloscope

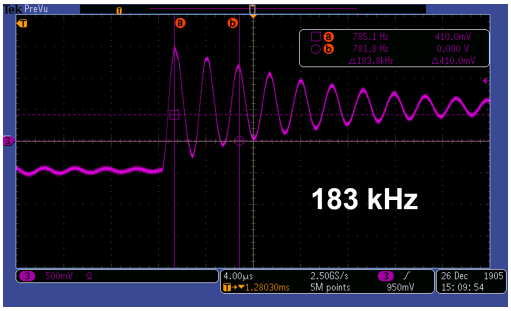


(b) Simulink Output for T1

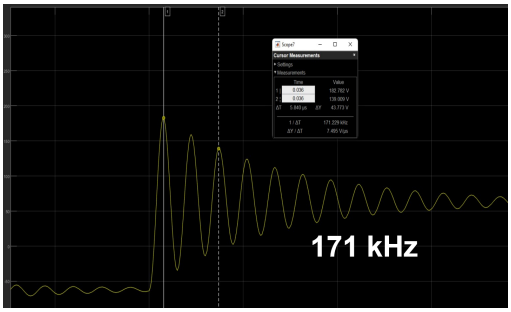
Figure 4.26: Transformer T1 Results

4.3. Optimization of the pulse Transformer

The goal of pulse transformer optimization is to design the pulse transformer so that manufacturing costs and time are minimized. Repeated printing of bobbins used as primary and secondary insulation can be avoided. The goal of transformer design is to obtain the dimensions of all transformer parts to provide the desired output, particularly the pulse output characteristics, with the available materials. For example, the chosen transformer



(a) Response of physical Transformer T2 from Oscilloscope



(b) Simulink Output for T2

Figure 4.27: Transformer T2 Results

core is the only one available on the market suitable for this application. A core with a greater relative permeability may be more favourable in reducing transformer size and parasitics. However, such cores were not available. Optimization of the transformer is the process of designing a transformer using available materials to achieve suitable output parameters. The following algorithm in the figure 4.28 is the design approach to optimize the transformer.

The initial stage in the design process is to specify the output characteristics of the pulse output, which were previously established in earlier chapters. Because the core was previously selected, just the core dimensions were accessible at this time. With these dimensions, the distance between the primary and secondary windings should be established while keeping parasitics and high voltage performance in mind. The next step is to extract the parameters using COMSOL. Several iterations are required to achieve the desired spacing between the windings. Initially, the easiest thing to do is to extract the parameters for two windings very near and far apart. The leakage inductance reduces as the windings come closer, while the inter-winding capacitance C_{12} increases. The opposite happens with the windings moving far.

The following step is to simulate the extracted parameters in Simulink. Test components such as test resistance R_t, test capacitance C_t, and capacitance of the load (OIP) were included at this point for simulation. The Simulink model is used to examine the impact of each parameter while all the other parameters were kept constant. The picture 4.29 depicts the model used to replicate the setup.

The impact of each parameter while all the other parameters were kept constant was simulated using the Simulink model. The analysis is described as follows.

- ***Primary inter-winding capacitance*** C_{11}**:** The primary inter-winding capacitance has no effect. The figure 4.30a shows that the output pulse does not vary despite the large variation in values, such as $1pF$ and $1000pF$. As a result, the C_{11}

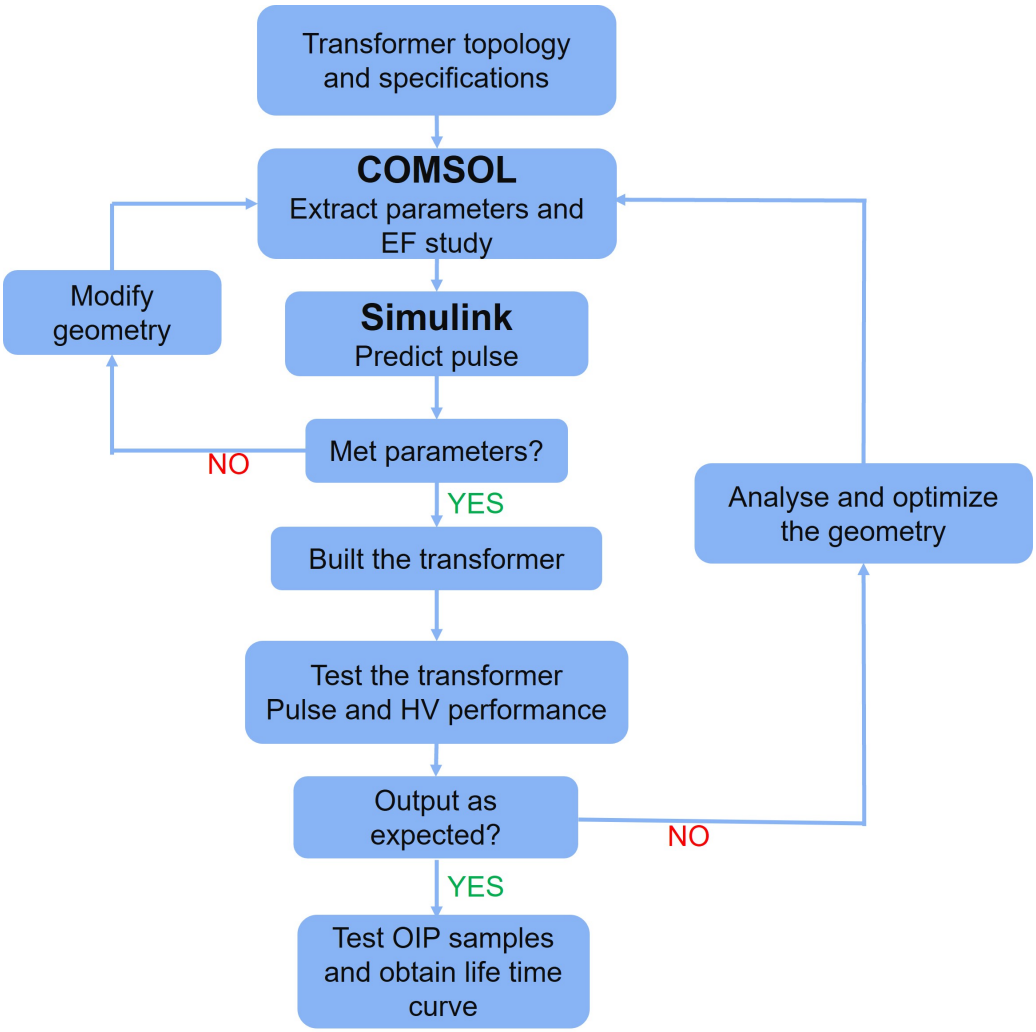


Figure 4.28: Algorithm for the optimization of the pulse transformer

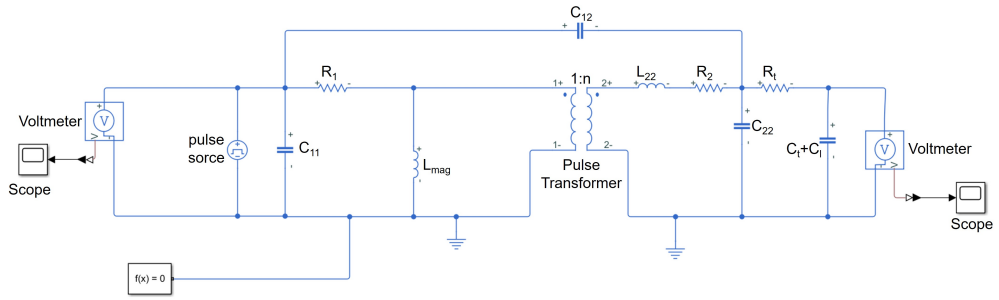
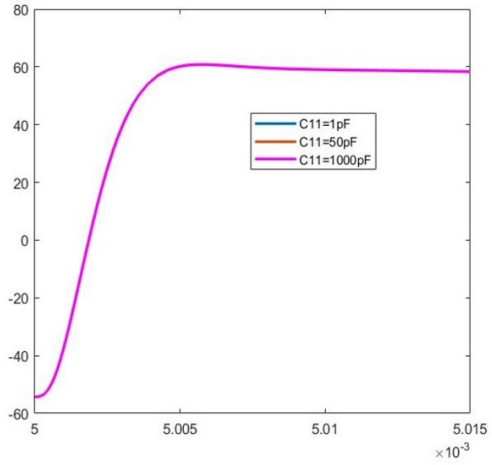


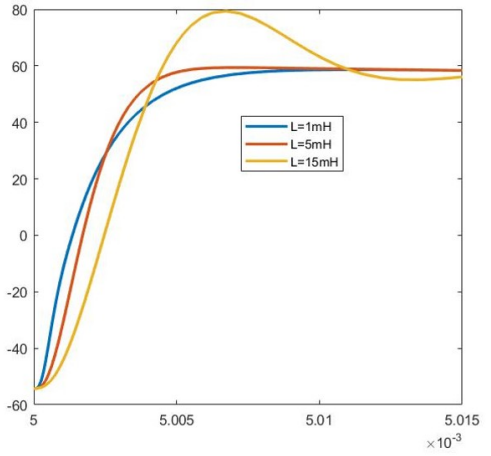
Figure 4.29: Simulink model used for optimization

does not need to be extracted using COMSOL before fabricating the physical pulse transformer.

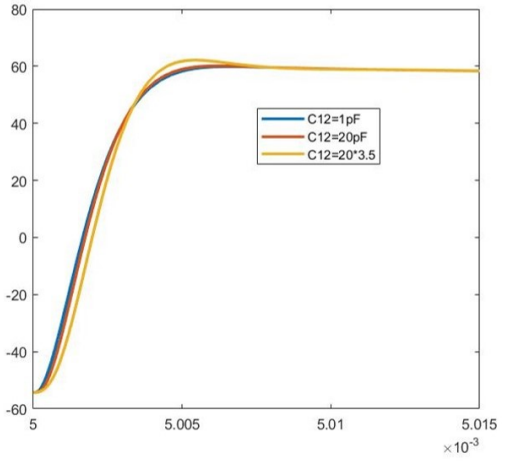
- ***Leakage Inductance referred to secondary*** L_{22}**:** The influence of the leakage inductance on the output may be observed in the picture 4.30b. The pulse rise time is faster when the leakage inductance is low, but the overshoot is excessively damped. However, this is due to the other values remaining constant, which is not the case in practice. The inter-winding capacitance increases as the leakage inductance decrease. This simulation is intended to demonstrate how leakage inductance and other pulse transformer parameters affect the output wave. The leakage inductance is the most sensitive parameter affecting pulse rise and fall times. The simulated numbers were not very varied, but the impact was considerable. The leakage inductance should be as low as achievable; nevertheless, the influence on the output wave is minimal after a certain low value. Inductance can be minimized by making the distance between the two windings as short as feasible while considering the transformer's inter-winding capacitance and high voltage performance. The number of turns on the windings can also be lowered to reduce leakage inductance. However, the transformer's primary winding should have a minimal number of turns while meeting the core saturation requirements described in previous chapters. Because the transformer ratio must be kept constant to achieve the same output voltage level, the secondary winding turns must also be lowered. Also, the two winding's positions should be such that the coupling is maximized; for example, the center points of the two windings can be equal. Overall, by selecting a core with a greater saturation flux density B_{sat}, the winding turns may be minimized, lowering the leakage inductance.
- ***Inter winding capacitance*** C_{12}**:** The figure 4.30c depicts the effect of inter-winding capacitance on the pulse. It can be shown that as the capacitance increases, so does the pulse rising time. When the difference in value is in the tens of orders, the impact is minimal. If the transformer is submerged in oil to improve high voltage performance, this capacitance will raise the oil's permittivity times. The permit-



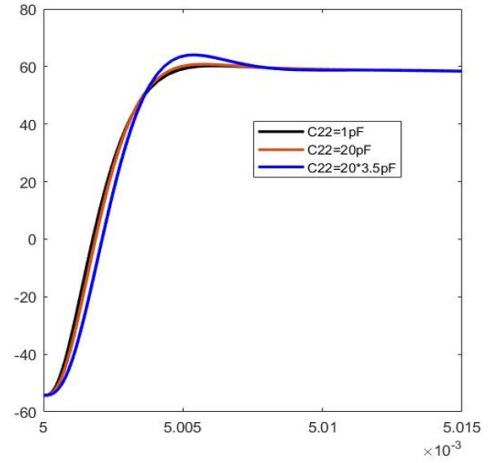
(a) Impact of Primary inter-winding Capacitance



(b) Impact of Leakage Inductance referred to the Secondary

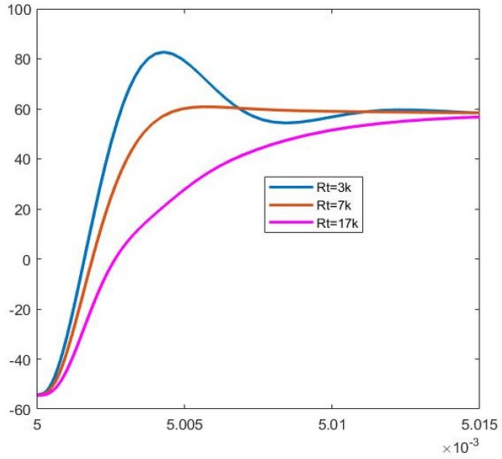


(c) Impact of Intra winding Capacitance

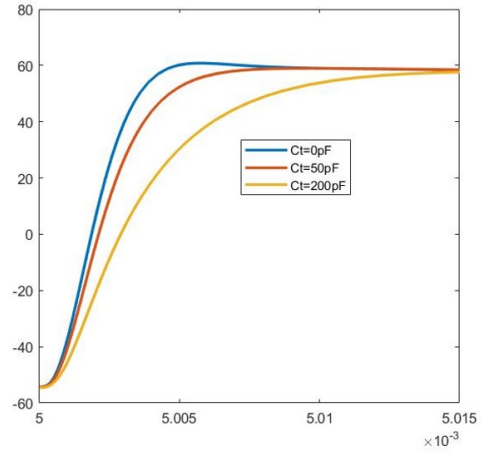


(d) Impact of Secondary inter-winding Capacitance

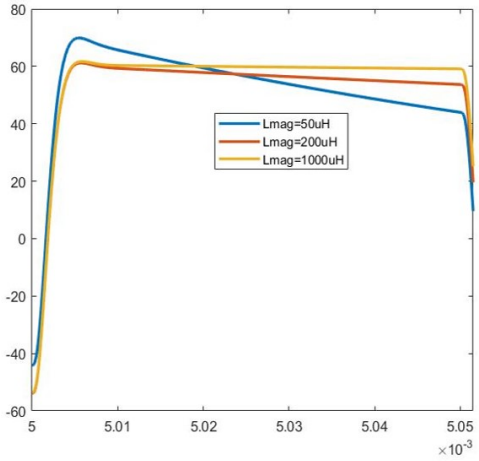
Figure 4.30: Impact of the Parameters in the equivalent circuit



(a) Impact of test element resistance



(b) Impact of test element Capacitance



(c) Impact of the magnetising inductance

Figure 4.31: Impact of the parameters in the equivalent circuit

tivity of oil is generally 3.5. It is obvious from this that immersing the transformer in oil considerably increases the rising time. If the transformer must be immersed for an application, the rise time should be reduced without oil. This may be accomplished by selecting a core with high permeability and a high saturation flux density. This capacitance can be lowered by separating the two windings. However, this increases the leakage inductance. A trade-off analysis should be performed, which is simple to execute with COMSOL. The optimal distance may be determined before fabricating the transformer by modeling the geometry in COMSOL.

- ***secondary intra-winding capacitance*** C_{22}**:** Secondary intra-winding capacitance has the same impact as the inter-winding capacitance stated above. The impact is seen in the figure 4.30d.

- ***Test element resistance*** R_t**:** Test components such as test resistance R_t and test capacitance $C - t$ will be useful in fine-tuning the output waveform shape. These parts are required because the pulse output varies with load and frequency. These test items will be used to keep the pulse shape consistent under all scenarios. This is required to obtain consistent findings when testing OIP samples at different frequencies. Figure 4.31a depicts the fluctuation in output wave shape with variations in test resistance. Lower test resistance levels cause considerable overshoot in the output. The resistance value can be raised to dampen the overshoot. However, increasing the resistance value too much causes the output wave to be overdamped and the rise time to increase. Variable resistance with the flexibility to modify the resistance value is required to retain the same output shape regardless of the load or frequency.

- ***Test element capacitance*** C_t**:** The test capacitance C_t serves the same purpose as the test resistance. The influence of the test capacitance element is seen in the figure 4.31b. The rising time reduces as the value of test capacitance increases. This is a high voltage variable capacitance.

- ***Magnetising inductance*** L_{mag}**:** When it comes to magnetizing inductance, much cannot be modified because the core has already been chosen. On the other hand, this simulation is valuable for understanding how the magnetizing inductance affects the output pulse. By increasing the magnetizing inductance, the droop of the pulse output may be reduced. This may be accomplished by increasing the number of cores and choosing the core with the high permeability and saturation flux density. The influence of magnetizing inductance is seen in the image 4.31c.

If the output of the Simulink model meets the specifications, the transformer may be built using the geometry designed in COMSOL. If, on the other hand, the output does not satisfy the pulse's criteria, the geometry in COMSOL should be adjusted until the desired shape is attained. After constructing the transformer, it should be checked to ensure that its output matches the simulation. The transformer should also be evaluated for high voltage performance to ensure no discharges occur. If everything works as intended, the

set-up may be used to test OIP samples; otherwise, the optimization must be restarted from the COMSOL simulation.

4.4. Building the final pulse Transformer

4.4.1. COMSOL

Before developing the final transformer, several iterations in COMSOL must be performed to obtain the optimum geometry. The distance between primary and secondary must be varied to get the final geometry. With COMSOL, it was noticed that if the distance between two windings is very close, the leakage inductance is minimal, with the intra-winding capacitance maximal and vice versa. With a few iterations, an optimal geometry may be produced. The completed geometry is depicted in the figure 4.32. The parameters extracted for this topology of the transformer are given in the table 4.7. The geometry

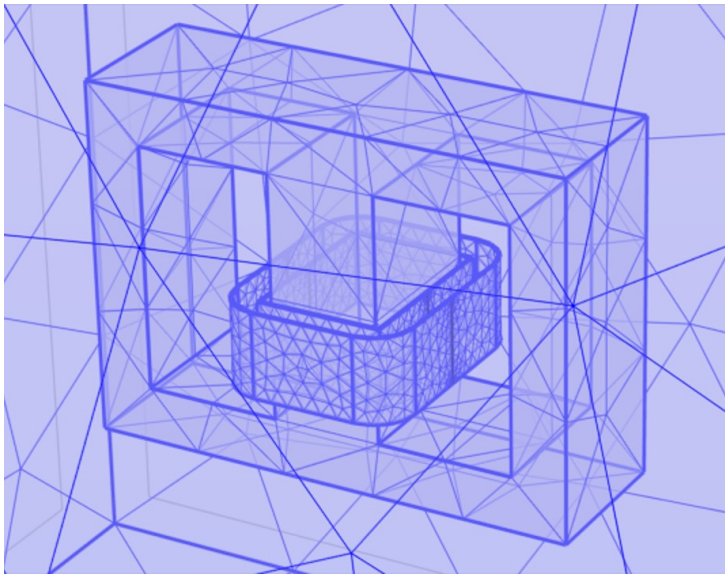


Figure 4.32: final transformer COMSOL simulation

shows that the winding does not take up the entire window. This is because the chosen core is the only available material suitable for this application and has a saturation flux density of just $0.4mT$. If sixteen cores were stacked, the number of primary turns required to avoid core saturation was four. The secondary winding turns total of 200 when the transformation ratio is 50. Because the secondary winding does not carry much current, the conductor's diameter is 0.2 mm. As a consequence, the secondary winding's

height is ($0.2 \times 200 = 4cm$). The coupling is improved when the primary winding height matches the secondary winding height. This reduces the leakage inductance. The secondary winding shape is identical to the primary winding shape, which is essentially the core shape. This design is preferable to the circular shape because the spacing between the two windings is continuous throughout. When contrasted to a circular form, this improves coupling.

Parameter	Value
L_{22}	5.26 mH
C_{12}	18.53 pF
C_{22}	1.49 pF
L_{mag}	375.10 uH

Table 4.7: parameters extracted from COMSOL for the final transformer

This geometry was simulated for high voltage performance. The maximum electric field is depicted in the diagram 4.33. Electrostatics physics was used to model the electric field. The voltage is applied linearly, with high voltage at the top and ground at the bottom. The secondary is given by $\sqrt{2} \times 10kV$, and the primary is given by $\sqrt{2} \times 200V$. The electric field is simulated using a "cutplane" at the top of the two windings, which is predicted to have the maximum electric field. The highest electric field between the two windings, shown in the figure 4.33, is $2.05kV/mm$, which is less than the breakdown voltage of the air, which is $3kV/mm$. The highest field occurred at the primary coil's edges. It is anticipated that no discharges will occur in the physical transformer.

4.4.2. Simulink

The COMSOL simulation parameters were utilized in the Simulink model. Figure 4.34 depicts the output result. The frequency was set at $50kHz$. The output is measured using *Cursor Measurements* to determine the rising time. This pulse's peak-to-peak rise time was $2.460\mu\ s$, which meets the criterion for this application.

4.4.3. Physical Transformer realisation

According to the flowchart in Figure 4.28, it is at the point when the parameters of the Simulink model's output pulse satisfy the requirements for this application. The actual transformer is now being built. Only the windings were simulated in COMSOL, but insulation, called bobbins, should be given to support them, and two of them are required. The dimensions used were identical to the COMSOL geometry model, as shown in the diagram 4.35. This was accomplished with *Shapr3D*, a 3D software. The bobbin designs were saved as ".STL" files. "Cura" software was used to convert this to G-code, which was then printed on a Creality CR-10s Pro printer.

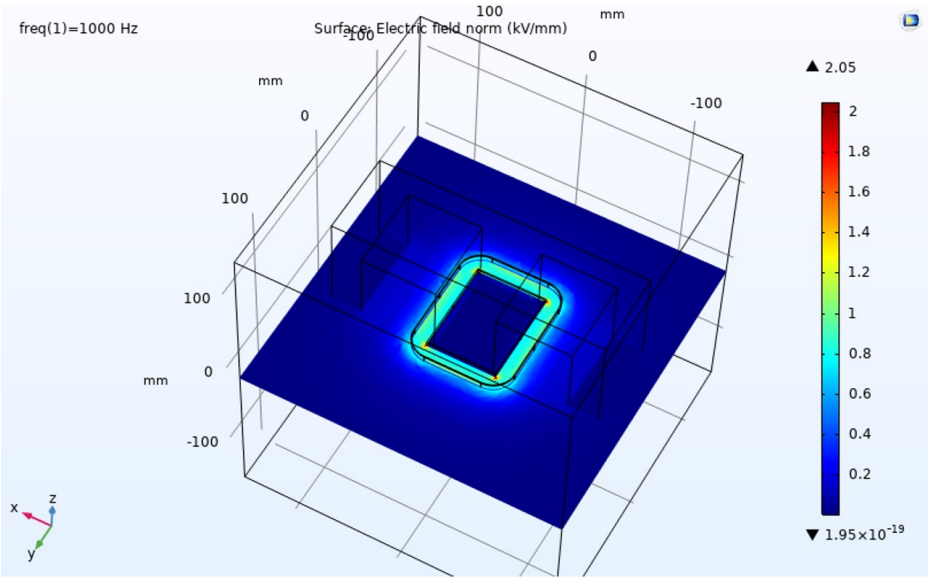


Figure 4.33: Electric field between the two windings

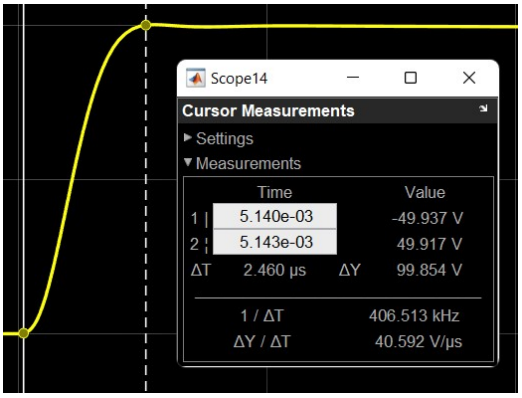


Figure 4.34: output of the simulink model

The printed bobbins were wound by hand. A winding machine may be utilized for

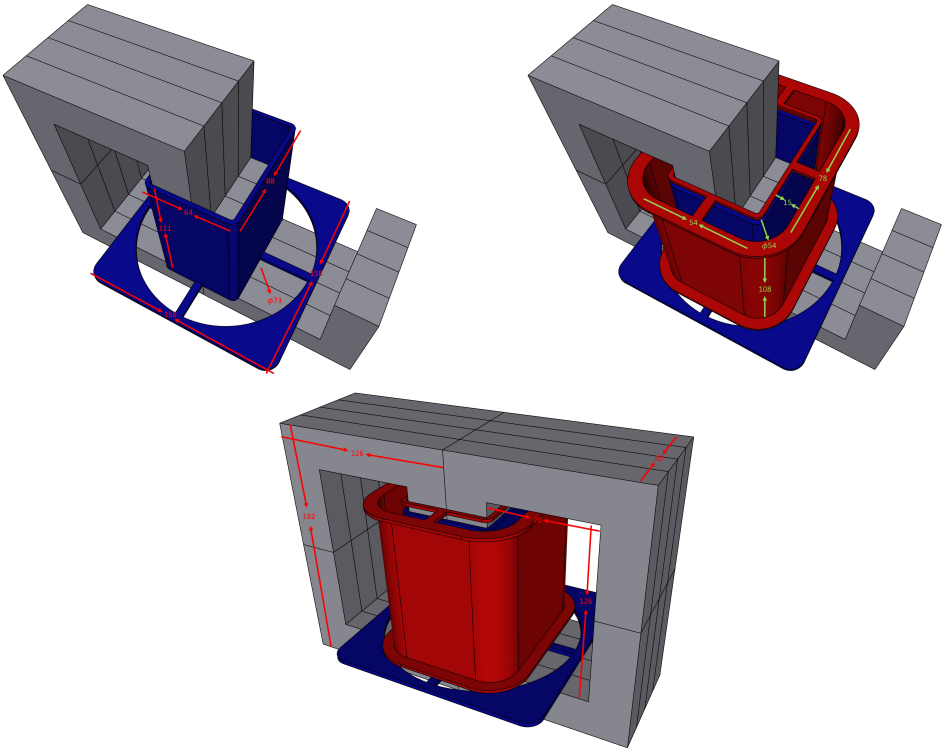
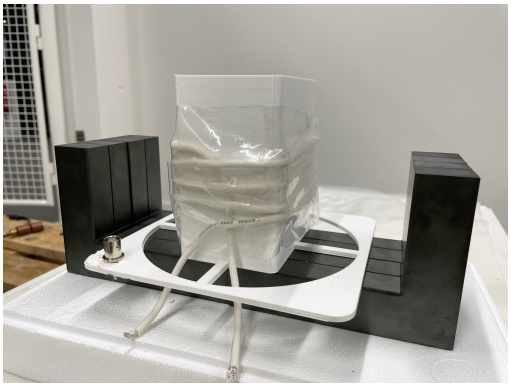
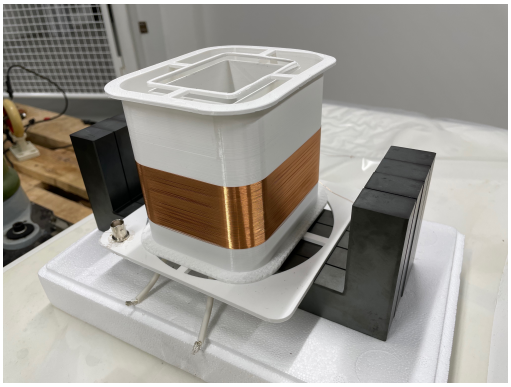


Figure 4.35: 3D design of the bobbins with dimensions (in mm)

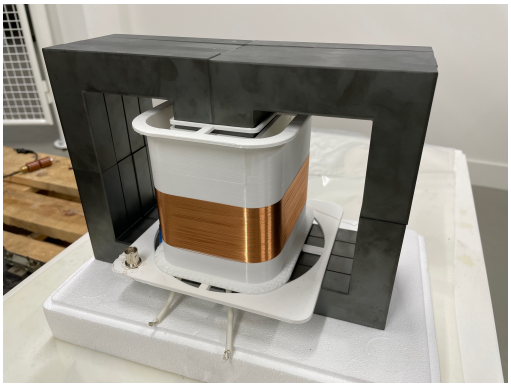
complicated geometries as well. For better high voltage performance and to minimize unexpected discharges, the primary was coiled with four turns of silicone insulated cable. The primary winding was formed with gaps between layers to match the height of the secondary winding, which improves coupling and reduces leakage inductance. To prevent the winding from moving, an extra piece of tape was wrapped around it. Figure 4.36a depicts the physical primary winding. The secondary winding has 200 turns and was wound using 0.2 dia copper wire. The secondary winding was mounted on top of the primary winding. A guide was built on top of the secondary winding bobbin to accommodate the cores. Figure 4.36b depicts the implementation of the secondary winding. Finally, the cores were closed to finish the transformer's construction. The finished transformer is depicted in Figure 4.36c.



(a) Physical Primary winding



(b) Physical Secondary winding



(c) Final physical transformer

Figure 4.36: Realisation of the pulse transformer

4.4.4. Testing of physical Transformer

The physical pulse transformer's performance was evaluated. The test setup comprises the test resistance and capacitance simulated in the Simulink model. The exact resistance and capacitance values were connected. A single-layer oil-impregnated paper sample was kept as a load. An oscilloscope *Tektronix DPO 3034 Digital Phosphor Oscilloscope* was used to measure the transformer's output pulse.

The essential objective now is to determine whether the output of the pulse transformer, measured with an oscilloscope, matches the output of the Simulink model. Both output waves should be plotted on the same plot for this comparison. The oscilloscope output was downloaded as a *.CSV* file to achieve this, and Matlab can be used to plot this file. Similarly, the Simulink model's output may be exported to Matlab. Both waveforms can be plotted on the same graph. However, the time period should be consistent with both

data sets. This may be accomplished by simply changing the time of one of the waveforms. The end outcome of all of this is depicted in the figure 4.37.

The figure 4.37 shows that both outputs matched quite well. This result is a reasonably

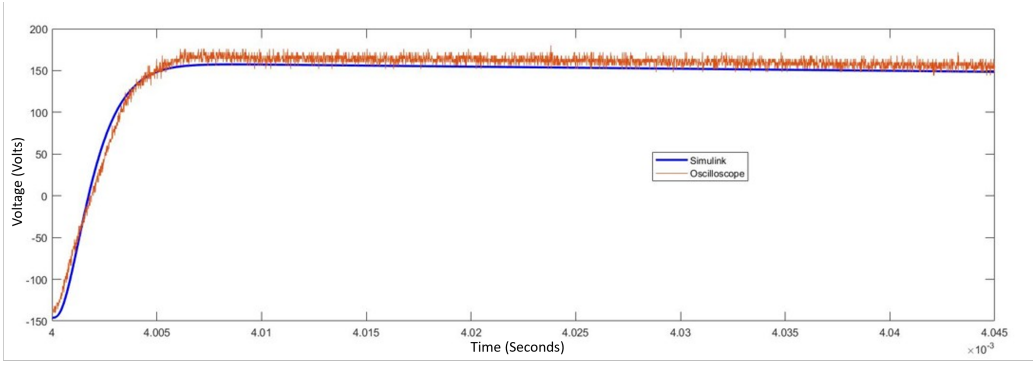


Figure 4.37: Comparison of outputs from Simulink and Oscilloscope

decent outcome in terms of anticipating the pulse. The blue line represents the Simulink output, while the red line is the oscilloscope output. A minor variance can be ascribed to the COMSOL simulation. In the COMSOL, the coils employed were homogeneous multi-turn coils that were not the same as in the physical transformer. As a result, the leakage inductance does not account for the skin effect. When compared to the real transformer, the capacitance measurement will also alter. Other parasitics will add up during physical transformer testing, such as the cables measuring, the cables connecting the transformer, and wherever those cables that were set apart will contribute some parasitic inductance at high frequencies.

The physical transformer parasitics were measured and compared to the parasitics retrieved from COMSOL. The comparison may be seen in the table 4.8. The discrepancy in these numbers is due to the reasons stated above, which may be the source of variation in the two outputs. Overall, this result may be used to anticipate the output of the pulse transformer before it is manufactured.

4.5. Pulse Transformer Summary

The pulse transformer multiplies the pulse generated by the pulse generator by a factor of 50. Without systematic design, transformer realization is exceptionally challenging since parasitics significantly influence the shape of the output pulse. The primary goals of this design are to save time by eliminating many iterations, and to save money by using fewer resources, particularly when printing bobbins. If the correct geometry is uncertain,

parameter	COMSOL	Physical
L_{22}	5.26 mH	5.72 mH
C_{12}	18.53 pF	18.77 mH
C_{22}	1.49 pF	2.63 pF
L_{mag}	375.10 uH	307.6 uH

Table 4.8: Final comparison of the parameters from COMSOL and Physical transformer

the printing must be repeated numerous times, using a significant amount of time and resources. The following is the design process:

- **Core material:** Because the frequency for this application is 50 kHz, the magnetic material used must be high-frequency compatible. Four materials were compared in terms of core losses, saturation flux density, relative permeability, and cost: ferrites, silicon steel, amorphous, and nanocrystalline. Ferrite was selected for this application for the reasons stated in the *Core material* section. Using 16 cores increased the cross-section area of the cores, which aids in reducing leakage inductance.

- **Primary and secondary turns:** To avoid core saturation constraints, the minimum number of primary winding turns computed for 16 cores was three. Four turns were chosen for the safety factor. The secondary turns resulted in 200 turns to maintain the turn ratio of 50.

- **Prediction of pulse:** The transformer's output should be anticipated before production to save money and time. It began by explaining the equivalent circuit specified in the IEEE standard for pulse transformer [42]. All of the approaches for extracting all of the transformer's parameters were investigated. A simulation model is generated to replicate the equivalent circuit. This process was done on two transformers that were available in the lab. Once the desired results were obtained, the transformer was optimized using a flow chart.

- **Building the final pulse transformer:** A final pulse transformer was developed using the techniques described in this chapter. This transformer was checked to ensure that its output corresponded to the simulation results. Both results match, as seen in the image 4.37.

4.6. Conclusion of the Pulse Transformer

The second research question *"Can the pulse shape of the pulse transformer be anticipated before producing it?"* was addressed in this chapter. The transformer's output

could be predicted, and the objective was met.

Recommendations: Due to a lack of suitable high saturation flux density cores, the transformer was large in size. When a superior high permeability, high saturation flux density, and low loss core is employed, a compact footprint transformer can be produced, and parasitics are decreased. High flux density leads to fewer turns, reducing leakage inductance and enabling faster pulses. This deficiency, however, aided the author in understanding how to use the sources and maximize what was available.

5

Cellulose Insulation Testing

Earlier chapters discussed creating a source to test the oil-impregnated papers. The pulse generator at the source provides repetitive pulses to the pulse transformer. The pulse transformer multiplies the voltage by fifty times, owing to its turn ratio. The OIP samples will be tested using these high voltage pulses. The final goal of this thesis study is to determine how these samples behave under continuous pulses. The following sections address the final test setup, theory relating to the Weibull distribution and the inverse power law model, and sample preparation. Finally, the outcomes of the tests on ageing are discussed.

5.1. Theory on Weibull distribution and inverse power law model

The insulation in any electrical device deteriorates gradually and eventually becomes unstable. Lifetime analysis of electrical insulation may be performed using data from the breakdown of the electrical insulation owing to high electrical stresses. This lifetime study can provide statistical information on the insulation, such as failure probability and lifetime characteristics, under typical operating settings. Obtaining life data under normal operating conditions is unrealistic; it takes a long time and is expensive. As a result, electrical insulation design engineers and material scientists employ approaches that cause the insulation to fail in shorter periods of time. The stress levels in these procedures are substantially higher than the regular operational stresses. The accelerated ageing data will be used to extrapolate the lifetime under normal operating conditions over a relatively long period of years.

5.1.1. Weibull distribution

In breakdown testing of solid dielectric insulation and in reliability studies, the Weibull distribution is the most common distribution [77]. Its popularity comes from the numerous shapes it can achieve for varying shape parameter values (β). It can model a broad range of data and life characteristics. The breakdown strength of the insulation can be estimated by applying ramp fields. The data acquired can then be plotted on the Weibull probability graph.

$$F(E) = 1 - e^{-\left(\frac{E}{\eta}\right)^{\beta}} \tag{5.1}$$

In the equation 5.1, $F(E)$ is the cumulative probability of breakdown, η is the scale parameter, and this is the electric field strength at which 63.2% of components population will fail. In the equation 5.1, if the E is replaced with η.

$$F(E) = 1 - e^{-\left(\frac{\eta}{\eta}\right)^{\beta}} = 1 - e^{-1} = 0.632 \tag{5.2}$$

The β is the shape parameter that shows the dispersion of data. Physically it indicates the ageing mechanism (failure mode) and/or population stage of life. There is another critical parameter called correlation factor ρ. This parameter is obtained through the goodness of fit test, indicating how well the distribution with parameters chosen fits the data. In [78], the author plotted Weibull for ramp breakdown for one and two layers of OIP at 50 Hz and 1500 Hz. The η value at 50 Hz for one layer OIP was 77.0, whereas, at 1500 Hz, it was 59.9. This means the breakdown strength at 50 Hz was significantly higher than at 1500 Hz. The β value for one layer OIP at 50 Hz was 16.85 and at 1500 Hz was 7.29. This indicates that the data is widely spread at higher frequencies, which means that weaker samples perform poorly. This thesis study is at much higher frequencies and with continuous pulses.

5.1.2. Inverse power law model

At various electric field stresses, the time to breakdown should be determined. The Weibull distribution is used to determine the electric field stress. For better statistics, the ageing test should be repeated numerous times for each electric field stress. The median of the data is chosen for each electric field strength. All of the medians for the electric fields will create a trend. This well-known empirical inverse power law is used to generate the lifetime curve by connecting all of the medians.

$$t = k\left(\frac{E}{E_0}\right)^{-n} \tag{5.3}$$

The equation 5.3 expresses the remaining lifetime. According to this expression, the remaining life is inversely proportional to the n^{th} of the applied electric field stress E. The variable t in the equation represents time, whereas k is a constant with a unit of time that changes with test circumstances such as the number of layers and electric field stress. E_0 is also a constant with the unit of the electric field, equal to 1 $\frac{kV}{mm}$; E_0 is set in this manner to ensure that the dimensions are identical on both sides. The [78] author concluded that the slope of the lifetime curve rises with frequency, implying that the lifetime is shorter for OIP samples exposed to higher frequencies.

5.2. Preparation of the OIP samples

The impregnation of OIP samples is a much simpler procedure. The process is described in full by the author of [78]. The samples are prepared using the same method. Nynas Nytro Taurus oil and Tervakovski cable paper with a thickness of $0.15mm$ was used. The vacuum oven used was BINDER VD 53, shown in the figure 5.1b. The steps listed below were followed.

1. A large paper roll was cut into a circular form slightly larger in diameter than the electrodes as shown in the figure 5.1a.
2. The paper samples were vacuum dried for 24 hours at a temperature of $120°C$.
3. After 24 hours, the oven temperature is slowly decreased to $60°C$. Enough oil was poured into a beaker and placed inside the oven. To eliminate ambient air within the oven, the oven should be filled with dry nitrogen before placing the oil beaker inside. The paper samples and the oil were dried at $5mbar$ for 24 hours at $60°C$.
4. After drying the paper and oil separately for 24 hours, the oven was refilled with dry nitrogen before being opened. After that, the paper samples were submerged in the oil beaker. It is essential to guarantee that all samples have been immersed. The paper samples were impregnated for 24 hours at $5mbar$ and at $60°C$
5. The oil-impregnated paper samples were vacuum-cooled inside the oven. To prevent moisture infiltration, the samples must be covered. A few samples were taken out with the oil before testing, while the remaining samples were stored within the vacuum oven.

5.3. Test setup

The test setup is shown in the figure 5.2.

- **Power stage:** Two power supplies are required for the pulse generator. The gate drivers will first receive the control voltage, which is 5V. The second source of power

(a) Paper samples cut in circular shape

(b) BINDER VD3 vacuum oven

Figure 5.1: OIP samples preparation pictures.

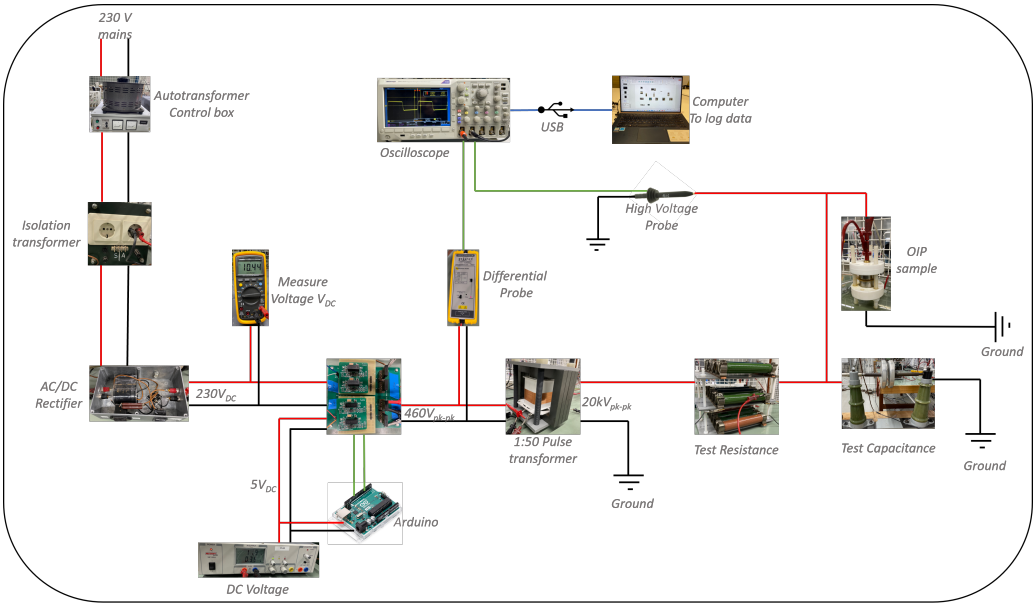


Figure 5.2: Block diagram of the test setup

is DC link voltage. A 230V primary source is obtained from the mains and linked to a single-phase variac. The variac output is connected to an isolation transformer, which aids in giving independent reference to the test setup after this isolation transformer. The isolation transformer output is then rectified to produce DC, which is connected to the H-bridge DC link input. A capacitance of $4500\mu\ F$ is connected to lower the ripples.

- **Pulse generator:** The pulse generator, also known as the H-bridge, generates pulses that are fed into the pulse transformer. The rectified DC voltage is applied to the H-bridge, and the SiC MOSFET switches are controlled by gate drivers, the logic for which is provided by the Arduino. The output of the H-bridge is measured using a *pico technology TA057* differential probe, which is connected to a *Tektronix DPO 3034* oscilloscope to display the waveforms.
- **Pulse Transformer:** The pulse generator's output is fed into the pulse transformer, which steps up 50 times due to the transformation ratio. The secondary cold terminal is grounded, while the hot terminal is connected to the test resistance.
- **Test elements:** As illustrated in the figure 5.2, the test elements—variable resistance and capacitance—were connected. These will allow one to tune the output pulse to the desired waveform shape. The testing electrodes were connected between the HV and ground to test OIP samples.
- **Measurements:** *ELDITEST GE 3830 30kV* high voltage probe was used to measure the voltage across the test sample. The voltage across the DC connection to the H-bridge was measured using a *Tenma 72-7780* multimeter.

5.3.1. Electrode setup

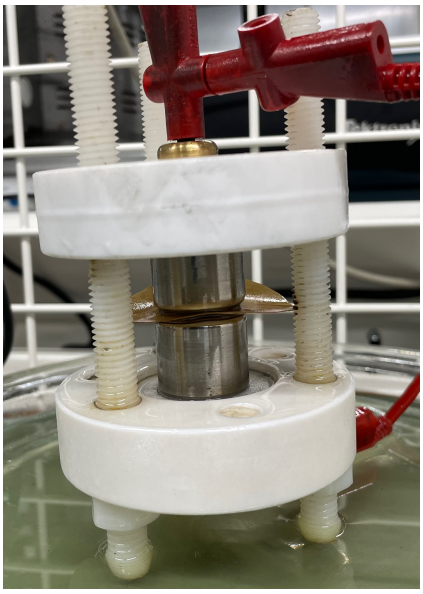
The electrodes used for this test were cylindrical with a diameter of $d = 2.5cm$, which provides a uniform electric field on the OIP sample. The support to hold these electrodes was made of Teflon. A connection provision was provided to connect the terminals. The electrodes were polished to avoid protrusions; the presence of protrusions enhances the electric field and makes the test results inaccurate. The electrodes and their setup is shown in the figure 5.3.

5.4. Ageing experiments

The pulse input to the oil impregnated paper samples at a frequency of $50kHz$ is displayed in the figure below: 5.4.

The rise time of the pulse wave is $T_r = \frac{2.68}{2}\mu\ s$. This was accomplished by adjusting the variable resistance; the value for this particular setup was $15.5k\Omega$. There is a negligible overshoot in the output, which may be minimized by raising the test resistance. There

(a) Electrodes used for testing



(b) Electrodes setup

Figure 5.3: Electrodes and electrodes setup for testing

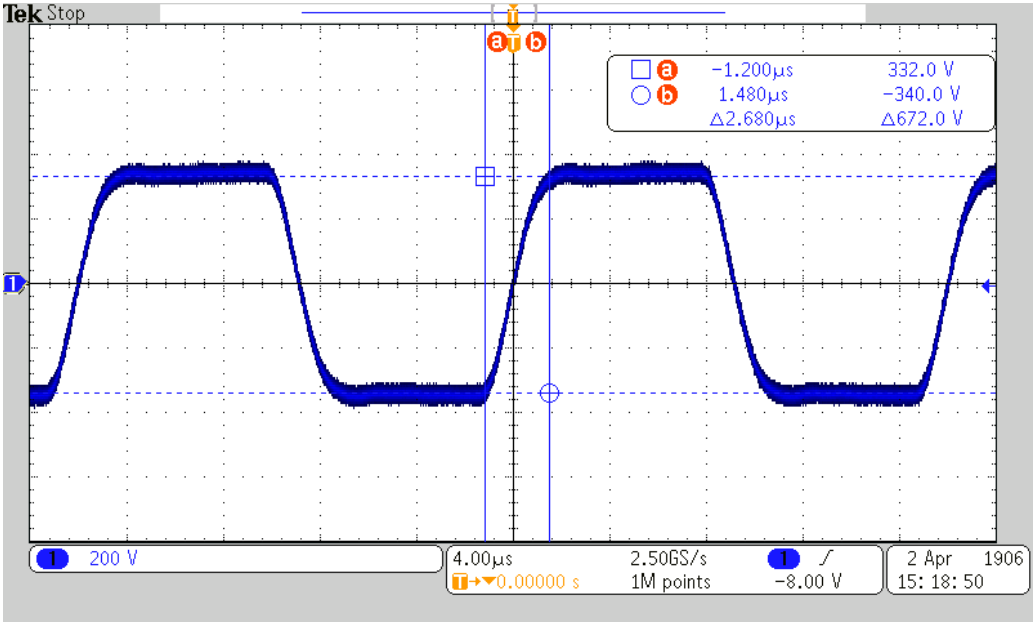


Figure 5.4: Output and rise time at frequency 50 kHz= $\frac{2.68}{2} \mu s$

were three types of resistance accessible in the lab: $4.5k\Omega$, $20k\Omega$ and $50k\Omega$. Fine tweaking is not that flexible with this combination. However, according to the desired parameters for the pulse output, a 5% overshoot is permissible. The test capacitance was not required with a single layer OIP sample since it contributes to the OIP sample capacitance, increasing the pulse rise time. When testing two layers of OIP samples, the variable capacitor can be utilized to raise the total capacitance and adjust to the desired output.

For the ageing testing, five different electric fields were used. They are $E = 22, 21, 20.5, 19.5, 18.66$, while the voltage inputs are $V_{p-p} = 6.6, 6.3, 6.1, 5.85, 5.55$. These are determined by the article [79], the author performed ramp experiments to determine the breakdown strength of oil impregnated paper under pulsed stresses. He used *Weibull* plot to analyze the data and discovered $E = 25kV/mm$ as breakdown strength. The field should be less than the breakdown strength to guarantee that the sample takes some time to break down.

The test begins by establishing the required peak-to-peak voltage using a single layer sample. A new sample is then used for testing. The auto-transformer control box is started instantly with the voltage level already set. When the voltage begins, the starting time is recorded, and the ending time is recorded after the sample break. The failure time of a sample is the difference between start and finish timings. A sample might sometimes take much longer than usual. That particular sample was halted and recorded. The figure 5.5 shows an example of how voltage was applied for ageing testing.

For each voltage level, an average of 30 samples were tested. Matlab was used to plot

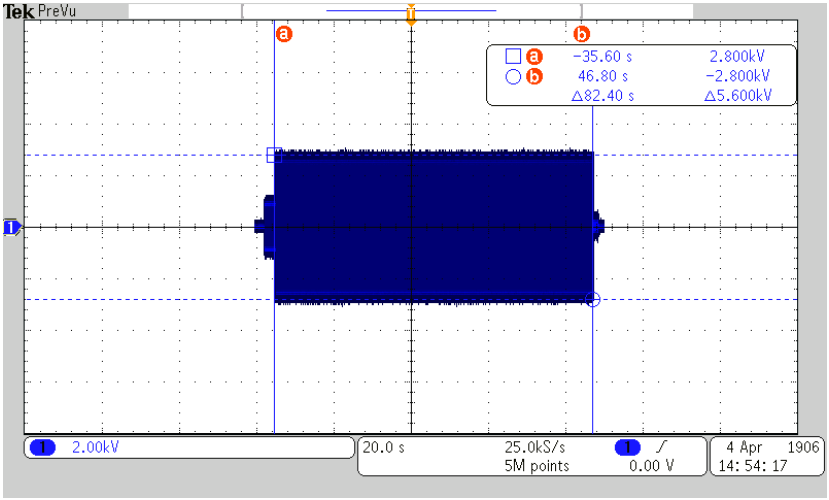


Figure 5.5: Example of voltage application for ageing test

the data on a log-log scale. Figure 5.6 depicts the plotted lifetime curve. The blue circles

Study Case	n	k
above transition	4.57	5.18×10^{6}
below transition	17.76	1.41×10^{24}

Table 5.1: Lifetime curve parameters

represent failure times, while the red dots represent data set medians. The medians were then joined with the best-fitting line. A transition was observed below $E = 21kV/mm$. This indicates a shift in the ageing mechanism in lower fields. The lifetime parameters, above and below the transition point, are given in the table 5.1.

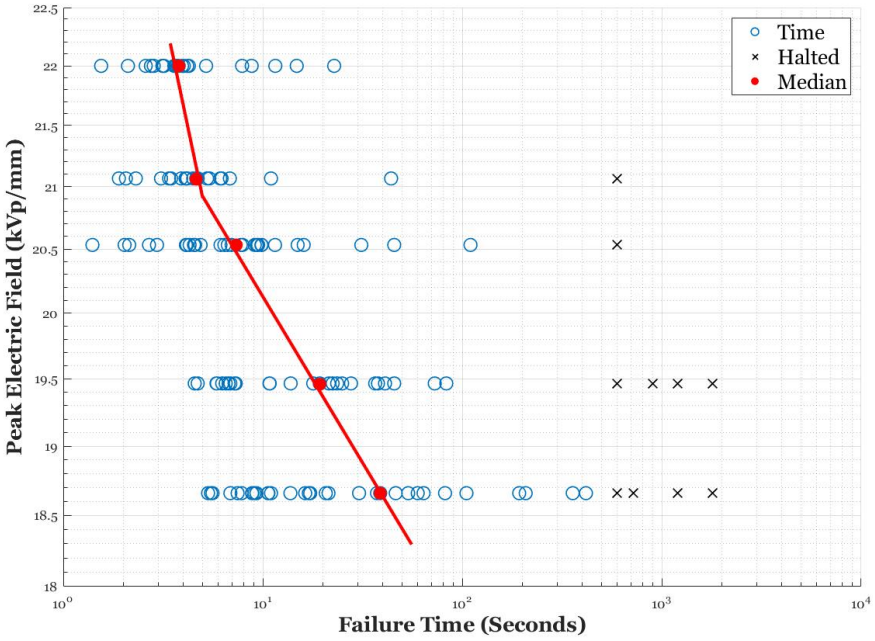


Figure 5.6: Lifetime curve at $50kHz$ under pulsed stress

The figure 5.7 shows a plot with only medians and a transition point. This transition might be caused by oil-filled cavities inside the paper, which initiate field enhancement and increase partial discharge over a specific field. This behaviour would accelerate the ageing of the insulation. This requires more research to conclude the reason, which is outside the scope of this thesis.

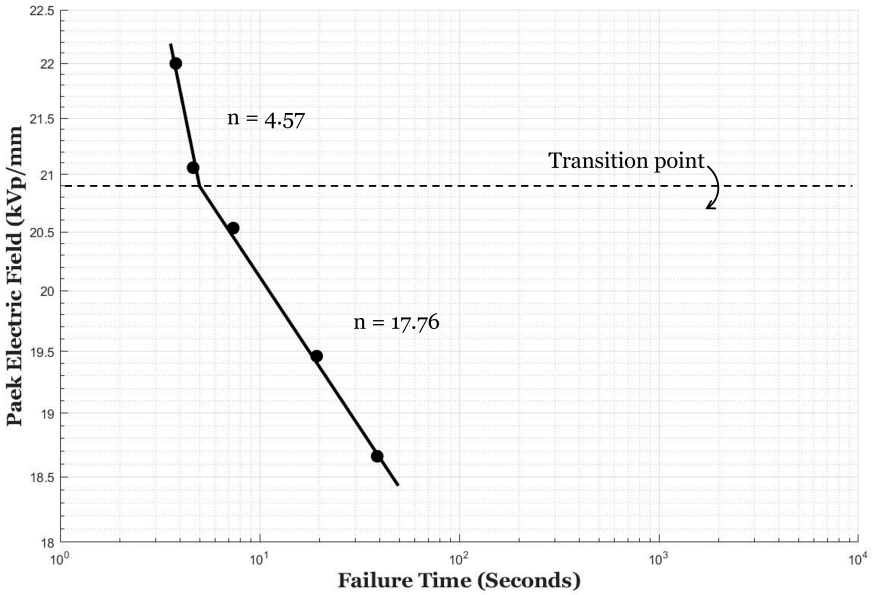


Figure 5.7: Lifetime curve with n and transition point

5.5. Results Summary

It would have been ideal if another test, say at $20kHz$ frequency, had been performed to examine the variation in the lifetime curve with regard to frequency. This result, however, may be compared to the publication [79], since the author worked with $50kHz$ frequency but with a different pulse output's rise time, which was $T_r = \frac{3.68}{2}\ \mu\ s$ in [79] and is $T_r = \frac{2.68}{2}\ \mu\ s$ in this research, and different electrodes. The findings are summarized below.

- Since the output pulse is faster than the pulse given in the study [79], The breakdown happened at much lower times. For example, at $22kV/mm$, the breakdown happened after $12sec$ in [79], whereas in this study, with the same field, the breakdown happened at $2sec$. This occurred as a result of the bigger electrodes employed in this investigation than in the other study, as well as the effect of the fast rise time.
- The author in [79] discovered an intriguing transition point below $20kV/mm$ with a slope that decreases five times. In this study, a transition point is also identified below $20kV/mm$. The slopes of the lifetime curves, however, differ. The slope above the transition point in the previous research was $n = 6.9$, whereas it was $n = 4.57$ in this study. The previous research had $n = 37.5$ below the transition point, but this

study had $n = 17.76$. The slopes were steeper in this study because the pulse input was steeper than in the previous study, and the electrodes utilized in this investigation were larger. Larger electrodes enhance the likelihood of detecting weaker areas of the OIP.

- It can be clearly observed that the insulation fails rapidly at high frequencies with fast rise times. Additionally, the harmonics induced by power electronics can induce steeper pulses than what was applied for this study. Hence, the present form of oil-impregnated paper may not be suitable for medium-frequency applications.

In conclusion, this thesis study has established a solid platform for future scientific research, which will be detailed in the next chapter.

6

Conclusions

This chapter will end the study by summarizing the important research results in connection to the research goals and questions and discussing their worth and contribution. It will also examine the study's limitations and provide recommendations for further research.

6.1. Research answers

This study aimed to investigate oil-impregnated papers under rapid pulses with a high repetition rate. The results show that when the frequency increases, the lifetime decreases rapidly. A transition point was observed indicating a shift in ageing mechanism. The section that follows answers the study's research questions.

- *What are the essential factors to consider when selecting a switch and building a gate driver for an H-Bridge?*

  When choosing a switch, not only should the switch's ratings be based on the application, but the switch's input capacitance should also be considered. If the capacitance is quite large, it will resonate with stray inductances in the layout of the pulse generator setup, causing the output to be badly distorted and the switches to be killed.

  Gate drivers are typically fast, in the tens of nanosecond range. Furthermore, due to the Sic Mosfet's rapid switching speeds, the di/dt and dv/dt rates increase due to stray inductances and parasitic capacitances, resulting in current and voltage overshoots. These overshoots have the potential to kill the gate drivers. Additional components like gate turn-on resistance and gate-to-source capacitance will aid in slowing down gate pulses, lowering di/dt and dv/dt. This also helps to reduce peaks on the H-bridge output since the switching speed is lowered.

- *Can the pulse shape of the pulse transformer be predicted before manufacturing it?*

  Yes, the output pulse of a pulse transformer can be predicted with an acceptable error. The pulse transformer design can be optimized using a circuit simulator (Simulink in this study). This circuit is nothing but the equivalent circuit of a pulse transformer given in the *IEEE Standard for Pulse Transformers*. The parameters of this equivalent circuit can be predicted using COMSOL, and the optimized geometry can be obtained. With this optimized geometry, a physical transformer can be realized.

- *Whether Oil Impregnated Paper can be used as insulation in medium-frequency applications?*

  According to the results, oil-impregnated paper in its current form is less effective for being utilized under medium-frequency conditions. For a deeper understanding, more testing with other frequencies should be conducted. Furthermore, the size of the electrodes influences breakdown times. The influence may be studied in the future by changing the electrodes.

6.2. Limitations

No piece of research is perfect. This study, too, is no exception. The limitations that come with this study are as follows:

- In reality, there will be mixed frequencies, whereas, in this study, only one frequency was used.
- The shape of the pulse, in reality, could be much steeper than the shape of the pulse used here, although fast enough to observe the phenomena.
- The behavior of the OIP under pulses also depends on other factors such as the thickness of the insulation, temperature rise, humidity content, and foreign particles, whereas in this study, other factors were not considered. However, a maximum effort has been made to avoid other parameters playing a role.

Additionally, due to chip shortages, the acquisition of the IC chips used in gate drivers took a long time to arrive, limiting the time that could be utilized to test more samples at different frequencies. A better DC source would have helped provide the transformer with a ripple-free input.

6.3. Future Recommendations

There were no failures during testing in the pulse generator or pulse transformer, which are particularly prone to failure owing to the high voltages and transients that would reflect during sample breakdown. This outcome was accomplished by carefully lowering

the gate driver's output speed with extra components and designing the transformer methodically. However, the design has room for improvement, which is outlined below.

- The design of the gate driver PCB can be improved by putting a copper ground layer instead of just tracks. This implementation would reduce the loop parasitics and lower the dv/dt. The gate drivers and switches were constructed in a modular form so that they could be easily replaced if one failed. This implementation increases loop inductance. This can be avoided by modeling the circuit in a circuit simulator before printing it on a PCB. This will also lower the bill of materials that were added to slow down the gate driver's output.
- The pulse transformer developed for this research was rather large. This is due to the ferrite core's low saturation flux density of $B_{sat} = 400mT$. Due to this, the number of stacked cores was increased to minimize the number of turns on the primary and secondary to obtain lower leakage inductance. High saturation flux density also contributes to lower leakage inductance, resulting in much quicker output pulses. A superior core material, say "nanocrystalline," with a better combination of saturation flux density and high permeability with lower losses, would reduce the size of the transformer.
- The aging trends can be investigated further at various frequencies. The impact of changing the size of the electrodes is also intriguing research. Lower voltage levels, which take a long time to break, can also be examined for improved reliability of the transition observed in OIP aging. Testing samples may also investigate the influence of harmonics with sinusoidal and pulse voltages at the same frequency; the time difference can be attributed to harmonics. The identical pulses may also be used to test two or more layers of the samples, which is how paper is utilized as an insulator in practice.

Finally, this chapter and this thesis ended with a sense of accomplishment from learning.

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