Arsenic-Spike Epilayer Technology Applied to Bipolar Transistors

Wibo D. van Noort, *Student Member, IEEE*, Lis K. Nanver, *Member, IEEE*, and Jan W. Slotboom, *Member, IEEE*

***Abstract*—For the first time, epilayers with an arsenic-doped spike of 50 nm width have been grown and used in silicon bipolar junction transistors (BJTs). The epilayer has been optimized such that the collector–base junction of the BJT is formed within the arsenic spike. The counterdoping of boron out-diffusion by arsenic strongly reduces the basewidth. The portion of the spike that is not counterdoped increases the total amount of n-type doping in the collector without reducing $BV_{\rm ceo}$. The increased collector-doping allows a 60% higher collector current prior to $f_{\rm T}$ fall-off. Arsenic has a low diffusivity so very few constraints are put on the thermal budget of the final process. This high flexibility makes the presented epilayer technology a promising candidate to enhance a bipolar process significantly.**

***Index Terms*—Bipolar transistors, semiconductor device doping, semiconductor epitaxial layers.**

I. Introduction

In A bipolar process, boron will diffuse during the annealing process that is needed to repair implantation damage and to activate dopants. Boron diffuses quite rapidly so the anneal conditions generally determine the basewidth, which is an important parameter for the high-frequency performance of the transistor (BJT).

A new method to reduce the basewidth is demonstrated with fully implanted bipolar transistors [1]. We have grown an n-type spike in the epilayer which counterdopes the out-diffused boron. The spike is fabricated with a novel epitaxial process in which arsenic autodoping is strongly suppressed [2]. With this process 50 nm wide arsenic spikes with a doping concentration varying from 10^{17} to 2×10^{19} cm^{-3} are made and the thickness of the layer grown on top of the spike (top-layer) is controlled very accurately. Contrary to boron, the arsenic in the spike will not diffuse much during the anneal. With the right top-layer thickness, the spike is placed exactly at the collector–base junction. Counterdoping of out-diffused boron by the arsenic spike reduces the basewidth to approximately 60 nm.

A similar approach has been presented by Heinemann *et al.* [3] and Visser *et al.* [4] where (transient-enhanced) boron out-diffusion in SiGe BJTs is counterdoped with a *phosphorus* spike. Phosphorus is very sensitive to (transient-enhanced) diffusion, therefore these spikes can only be used in a low-temperature (700 °C) process.

Our work presents an *arsenic* spike which offers more flexibility because arsenic has a much lower diffusivity than phosphorus. The spike can be used in processes with a conventional 950 °C thermal anneal or a process that suffers from transient-enhanced diffusion of boron.

The n-type doping in the spike is not completely counterdoped by boron which leaves a thin highly doped ($N_d \approx 7 \times 10^{17}$ cm^{-3}) layer in the collector, adjacent to the collector–base junction. Palestri *et al.* [5] have studied such a "launcher-layer" theoretically. They predict an unchanged breakdown voltage ($BV_{\rm ceo}$) and an increased cutoff frequency for devices with such a layer. Two effects explain the improvement.

- The high doping in the spike will not decrease $BV_{\rm ceo}$ due to the nonlocal avalanche effect. The spike is only 50 nm wide and placed exactly at the collector–base junction, which results in a very thin high-field region. The integral amount of doping in the spike is kept sufficiently low ($\approx 5 \times 10^{12}$ cm^{-2}) that electrons and holes crossing the high-field region do not gain enough energy to cause impact ionization [6], [7].
- As the spike introduces more doping in the collector, the Kirk effect will be delayed [8] . Both the basewidth reduction and delay of the Kirk effect will increase the maximum cutoff frequency ($f_{\rm T}$).

Heinemann *et al.* [3] and Schüppen *et al.* [9] have observed these advantages in experimental SiGe devices. Their devices were fabricated by using molecular beam epitaxy (MBE). Our work shows that an arsenic-doped spike that is fabricated with CVD epitaxy can also be used. The arsenic spike also increases $f_{\rm T}$ without a significant reduction in $BV_{\rm ceo}$.

II. Experimental Devices

A. Device Fabrication

Recent developments in CVD epitaxy allow extremely thin arsenic-doped silicon layers to be grown. The major feature is that the well-known autodoping, related to arsenic, has been suppressed. The process is briefly described in Section II-B and a more detailed description is given in [2].

With this new process, several epilayers with a 50 nm wide arsenic spike have been fabricated. The maximum arsenic doping concentration in the spike and the thickness of the top-layer are chosen such that the spike lies at the base–collector junction

Manuscript received September 12, 1999; revised September 1, 2000. The review of this paper was arranged by Editors P. Asbeck and T. Nakamura.

W. D. van Noort and L. K. Nanver are with the Laboratory of Electronic Components, Technology and Materials, Delft University of Technology, 2628 CT Delft, The Netherlands.

J. W. Slotboom is with the Philips Research Laboratories, Eindhoven, The Netherlands.

Publisher Item Identifier S 0018-9383(01)09060-8.

0018–9383/01$10.00 © 2001 IEEE

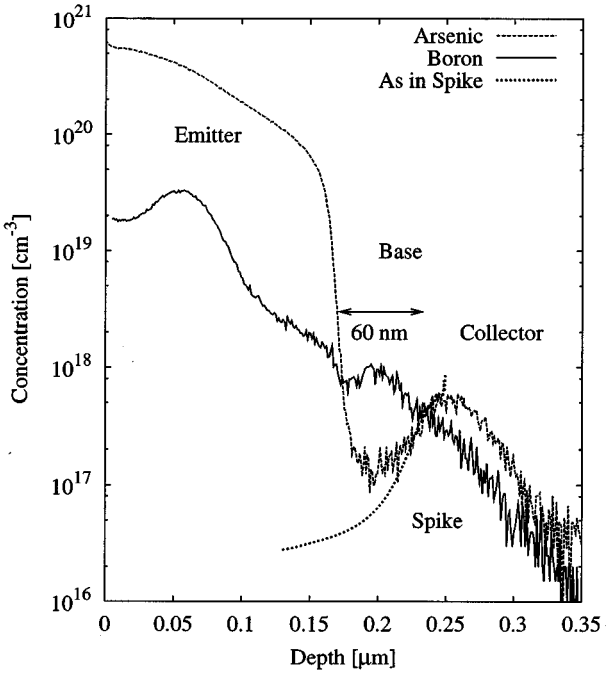


Fig. 1. SIMS doping profiles of a completed device with an arsenic spike and a 225 nm top-layer. The profile of the epilayer is also shown (measured with *C–V*).

which is formed in later processing. Epilayers without a spike have been included in the experiment for comparison.

In all the epilayers, devices are fabricated that are based on the DIMES-03 process [1], which is a fully implanted, low complexity, bipolar process. For these experiments the process is slightly changed; 0.4 μm of silicon has been removed outside the base-regions with a shallow-trench etch. This etch removes the arsenic spike where it is not needed and prevents a premature breakdown of the junction isolation around the device.

A secondary ion mass spectroscopy (SIMS) measurement[1] performed on a device with a spike is shown in Fig. 1. This figure shows that a lot of boron is neutralized by the spike, so the basewidth is strongly reduced. To measure the basewidth, the As SIMS profile has been measured with a low energy to get sufficient depth resolution. The basewidth is estimated to be 60 nm.

At the collector-side adjacent to the collector–base junction, an increased net n-type doping remains. Although this portion of the collector doping is located in a very thin layer the spike contains at least 10^{12} atoms cm^{-2}, a factor two more than a collector without a spike ($\approx 5 \times 10^{11}$ atoms cm^{-2}).

The DIMES-03 process also includes an optional pedestal collector. This is a collector with increased doping ($N_d \approx 10^{17}$ cm^{-3}) which is implanted in the epilayer under the emitter. Devices with a pedestal collector have a better high-frequency performance and a lower breakdown voltage. These devices allow evaluation of the special epilayers at another point on the BV_{ceo} versus f_T curve. Fig. 2 shows a schematic cross-section of the device, the shallow-trench, spike and pedestal collector are indicated.

[1]SIMS is performed by Evans Europa, Uxbridge, UK.

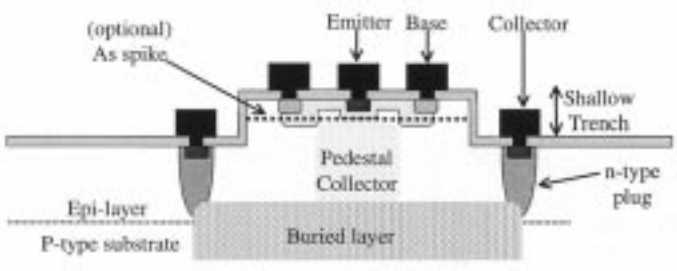


Fig. 2. Schematic cross-section of the fabricated device (not to scale).

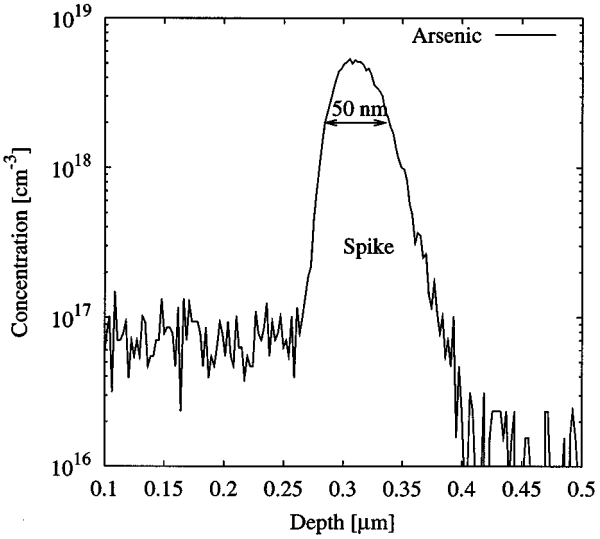


Fig. 3. As-grown SIMS profile of a highly doped As spike (dep. time 4 min).

B. Epilayers With an Arsenic Spike

All the epilayers are grown with a commercially available, lamp-heated, single wafer reactor (ASM Epsilon One). It is suitable for low-temperature AP-CVD epitaxy.

An arsenic-doped spike is grown in the epilayer. The as-grown SIMS profile of such a spike is shown in Fig. 3. The spike itself is grown at 700 °C and atmospheric pressure. This low temperature allows a maximum As concentration up to 2×10^{19} cm^{-3}. After the spike is grown, excess As surface-coverage is removed from the wafer with a hydrogen bake. When this step is omitted, strong autodoping will be present in the top-layer. The top-layer is grown at 950 °C and reduced pressure (60 torr). More details about this process are given in [2].

Both the maximum arsenic concentration in the spike and the thickness of the top-layer have been varied. The maximum arsenic concentration in the spike increases with an increasing deposition time of the spike. Three deposition times are used: 1.5, 2 and 2.5 min, resulting in a maximum As concentration of $\approx 2.5 \times 10^{17}$, 7×10^{17} and 2×10^{18} cm^{-3}, respectively. The top-layer thickness has been varied with three thicknesses of: 225, 275, and 325 nm.

The different epilayers have been characterized with capacitance voltage (*C–V*) measurements. From these measurements a doping profile has been calculated.[2] Fig. 4 shows the calcu-

[2]Good agreement between capacitance–voltage (*C–V*) measurements and SIMS profiles was observed in previous experiments.

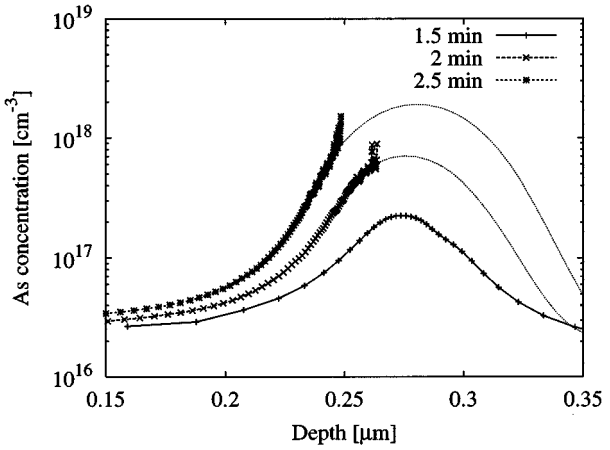


Fig. 4. Doping profiles derived from *C–V* measurements (symbols) and SUPREM simulation (dotted) for three different deposition times of an arsenic spike with a 275 nm top-layer.

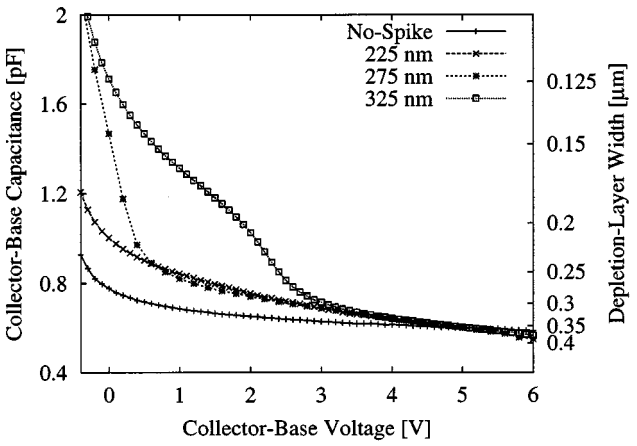


Fig. 6. Collector–base capacitance versus collector–base voltage for 20 × 40 μm^2 emitter area. A 2 min spike is used with a top-layer thickness that is varied from 225 to 325 nm.

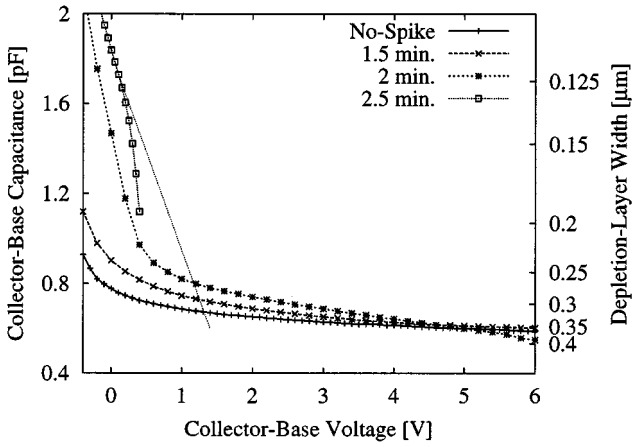


Fig. 5. Collector–base capacitance versus collector–base voltage for 20 × 40 μm^2 emitter area. The spike deposition time is varied from 1.5 min to 2.5 min.

lated doping profiles for three different spike deposition times with a 275 nm top layer resulting in spike-concentrations of 1.7 $\times 10^{12}$, 5×10^{12} and 1.25×10^{13} cm^{-2}. The profiles shown in this figure are not as-grown but have been measured after being subjected to the total thermal budget of the device processing.

III. Results and Discussion

A. Collector–Base Capacitance

The collector–base capacitance ($C_{\rm cb}$) versus voltage ($V_{\rm cb}$) has been measured on devices with a large 40×20 μm^2 emitter area, the larger area allows more accurate measurements. Fig. 5 shows the *C–V* curve of the collector–base capacitance for three devices with different deposition times of the spike. A measurement on a reference device without a spike is also included in the graph. This figure shows that $C_{\rm cb}$ at $V_{\rm cb} = 0$ V (C_0) increases when the deposition time of the spike increases. This increase of C_0 is due to a reduced depletion-layer width. A thinner depletion layer implies a higher doping concentration at the collector side of the metallurgic collector–base junction. So the increasing C_0 shows that the collector–base junction is formed within the arsenic spike.

When $V_{\rm cb}$ is increased, the spike will be fully depleted. Once the spike is depleted, it takes only a small increase of $V_{\rm cb}$ to extend the depletion layer all the way to the buried-layer. With a fully depleted collector, $C_{\rm cb}$ of the reference device and a device with a spike are equal. Fig. 5 shows that the spike is depleted at voltages exceeding 1 V. The slope of the *C–V* curves at higher $V_{\rm cb}$ increases for a longer spike deposition time. Two effects increase the slope: reduction of the net base doping due to increased counterdoping by arsenic and a significant increase of the total amount of doping in the collector. The latter causes the collector–base depletion region to end in a lower doping concentration at the buried layer side. This results in a slightly higher capacitance variation. The reduction of net base-doping can be compensated for by using a higher implanted boron dose for the base.

A device with a 2.5 min spike deposition time breaks down before the spike can be depleted. The integral amount of doping in the spike (1.25×10^{13} cm^{-2}) is too high to benefit from the nonlocal avalanche effect. The high electric field that results from the high doping concentration causes the voltage drop across the depleted spike to exceed a critical value. Electrons and holes crossing the high-field region are accelerated above the impact ionization threshold ($E_{\rm ii} \approx 1.2$ eV). The extrapolation in Fig. 5 shows that the 2.5 min spike is fully depleted when $V_{\rm cb}$ is higher than $E_{\rm ii}/q$.

Fig. 6 shows the *C–V* curve for devices with different top-layer thicknesses on a 2 min spike. Three thicknesses have been used: 225, 275, and 325 nm. For an increasing top-layer thickness, C_0 increases. This indicates that there is more doping at the collector–base junction when the thickness of the top-layer is increased. The curve for the 325 nm top-layer shows a decreasing gradient at 1 V which increases again around 2 V. This shows that as $V_{\rm cb}$ is increased the doping level at the collector-side depletion-boundary increases first and then decreases again. From this we can conclude that for the 325 nm top-layer, the base–collector junction is formed outside the maximum of the spike.

B. DC Measurements

From the *C–V* measurements described in Section III-A, it becomes clear that some boron in the base is neutralized by the ar-

TABLE I
h_{FE} FOR LOW AND HIGH B^+ DOSE, RELATIVE CHANGE IN G_B (CALCULATED FOR THE HIGH DOSE), AND BREAKDOWN VOLTAGE ($BV_{\rm ceo}$) FOR DIFFERENT ARSENIC-SPIKE CONCENTRATIONS (N_d) AND TOP-LAYER THICKNESSES (W_{top})

Layer	W_{top}	N_d	h_{FE}		$\frac{\Delta G_B}{G_B}$	BV_{ce0}
	[nm]	[cm^{-3}]	low	high	-	[V]
T_0	no spike		103*	56	0 %	7
$T_{1.5}$	275	2.5x10^{17}	145	67	-16 %	7
T_2	275	7x10^{17}	233	77	-27 %	4.5
$T_{2.5}$	275	2x10^{18}	8680	125	-55 %	2.5
W_{325}	325	7x10^{17}	162	72	-22 %	3.5
W_{275}	275	7x10^{17}	233	77	-27 %	4.5
W_{225}	225	7x10^{17}	1010	87*	-36 %	6.8

senic spike. To quantify how much boron is neutralized, we have compared the DC current gain (h_{FE}) of the different devices. The DC current gain is determined by the base Gummel-number (G_B) and the emitter Gummel-number ($h_{FE} = G_E/G_B$). The base current at $V_{be} = 0.6$ V is nearly identical for all devices ($\sigma < 6\%$), indicating that they all have the same G_E. Therefore, a change in G_B results in a proportional change in $1/h_{FE}$. The relative difference between G_B of the transistor with a spike and a device without a spike is calculated by comparing their h_{FE}.

Table I shows the average h_{FE} and relative difference in G_B for devices with varying spike doping and top-layer thicknesses. Two boron doses are used, a low and high dose, which result in a $h_{FE} \approx 100$ for devices without spike and with a W_{225} layer, respectively. The relative change in G_B shows that a higher doping in the spike strongly decreases G_B. A thinner top-layer shifts the spike into the base, which also decreases G_B. The decreased G_B can easily be compensated with a higher implanted boron dose in the base. But if there is too much n-type doping left in the collector, the breakdown voltage ($BV_{\rm ceo}$) is decreased. Two devices with a spike have a $BV_{\rm ceo}$ similar to the reference device ($BV_{ce0} \approx 7$ V). A device with layer W_{225} is very attractive. It combines a high arsenic concentration in the spike with a minor change in $BV_{\rm ceo}$. A doping profile of this device is given in Fig. 1

Fig. 7 shows the output curves for devices with a pedestal collector. Devices with and without a spike are compared. Both devices have an emitter area of 20×1 μm^2. The devices have a compensated boron dose resulting in a comparable $h_{FE} \approx 100$ for both devices. For these devices, there is no significant change in Early voltage or $BV_{\rm ceo}$. Devices without a pedestal collector show a significant decrease in Early voltage when a spike is used due to the increased collector-doping resulting from the spike.

C. High-Frequency Measurements

The high-frequency performance of the reference device and the device with a spike (layer W_{225}) is compared (both are marked with $*$ in Table I). The measured $f_{\rm T}$ versus collector current and voltage (I_c and $V_{\rm cb}$) is shown for both devices in Fig. 8. This figure shows that the maximum $f_{\rm T}$ for the device with a spike is reached at a much higher I_c, indicating that $f_{\rm T}$

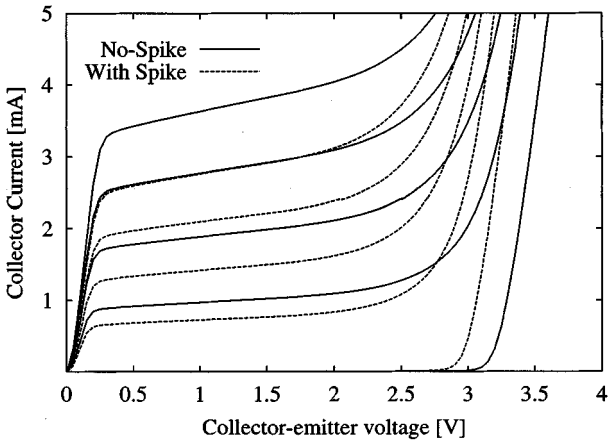


Fig. 7. Output curves for transistors with a pedestal collector without spike and with a 2 min spike (W_{225} in Table I) are shown (20×1 μm^2 emitter area). Between each trace the base current is increased by 10 μA.

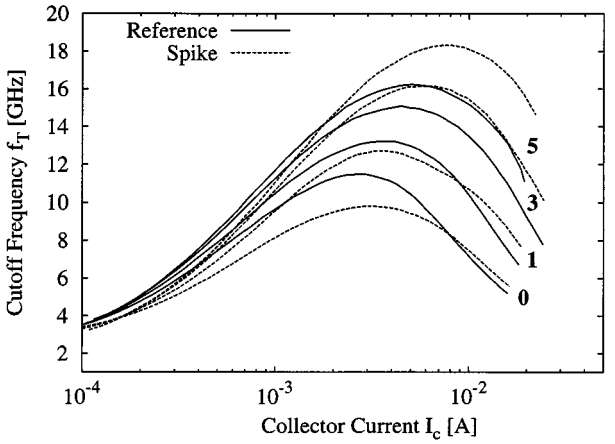


Fig. 8. Cutoff frequency $f_{\rm T}$ for the reference transistor and a device with layer W_{225}. $V_{\rm cb}$ is set to 0, 1, 3, and 5 V (indicated with bold numbers).

fall-off due to the Kirk effect is postponed due to the higher doped spike. With a spike, the current density is increased by about 60%.

To investigate the increase of $f_{\rm T}$, the emitter–collector transit time ($\tau_{ec} = 1/2\pi f_{\rm T}$) is plotted against $1/I_c$ in Fig. 9. In a plot like this, the contribution of depletion capacitance ($C_{be}+C_{\rm cb}$) to τ_{ec} can be separated from that of the neutral storage capacitance.

From comparison of the slope of τ_{ec} of both devices in Fig. 9, we can conclude that ($C_{be} + C_{\rm cb}$) is larger for the device with a spike. From Section III-A, we know that $C_{\rm cb}$ at $V_{\rm cb} = 5$ V is equal for both devices so C_{be} is larger for the transistor with a spike. This is the result of a higher doping concentration in the base due to the compensated implantation dose.

The neutral transit time (τ_n) is found by extrapolating the linear part in Fig. 9. The point where the extrapolation intersects $1/I_c = 0$ gives τ_n. This figure shows that it is reduced by $\approx$1 ps when a spike is used. The reduction is caused by two effects: the smaller basewidth decreases the base transit time (τ_B), and secondly, the acceptor concentration in the base has been increased to compensate counterdoping of the spike. This reduces the level of injection at the emitter–base junction, and consequently, the charge storage associated with it.

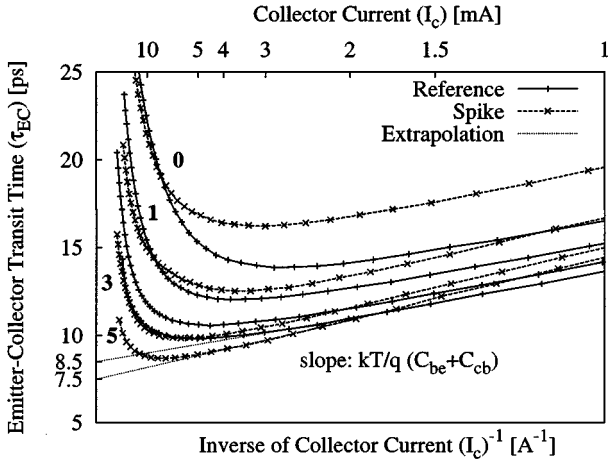


Fig. 9. Emitter–collector transit time τ_{ec} for the reference transistor and a device with layer W_{225}. $V_{\rm cb}$ is set to 0, 1, 3, and 5 V (indicated with bold numbers).

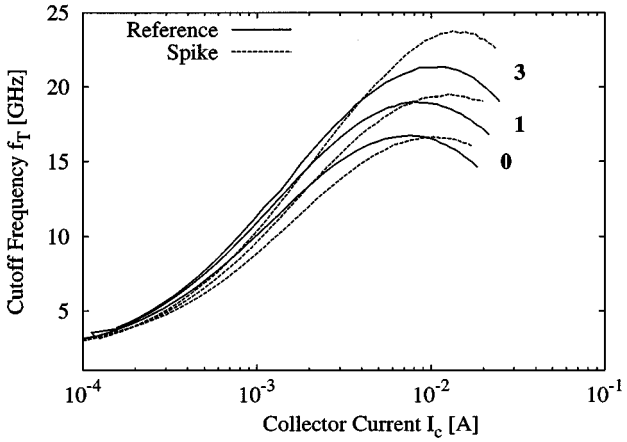


Fig. 10. Cutoff frequency $f_{\rm T}$ for devices with a pedestal collector. A reference transistor and a device with layer W_{225}. $V_{\rm cb}$ is set to 0, 1, and 3 V (indicated with bold numbers).

Equation (1) gives τ_B as a function of basewidth (W_B) and electron diffusion coefficient (D_n). W_B was determined from device simulations of the profile given in Fig. 1, and a modified version without the spike and a lower acceptor concentration in the base. The emitter and base Gummel number are approximately equal for both profiles. From these simulations, it was found that the effective W_B, corrected for depletion induced by $V_{\rm cb}$, is roughly reduced from 60 to 30 nm by the spike. In accordance with (1), this corresponds to 0.4 ps. The remaining transit-time reduction is attributed to the increased acceptor concentration in the base

$$\tau_B = \frac{W_B^2}{2D_n}. \tag{1}$$

The reduction relative to τ_n is small so the higher current density is mainly responsible for the increased $f_{\rm T}$ in the device with a spike.

D. High-Frequency Measurements on Devices With a Pedestal Collector

Devices with a pedestal collector are fabricated in the same epilayers as those presented in the previous section. Phosphorus has been implanted in the epilayer under the emitter, before the deposition of the spike and top-layer. The implanted phosphorus forms the pedestal collector which also neutralizes some boron in the base. The implanted boron dose in the base of both devices has been chosen such that devices with or without a spike have a comparable h_{FE} of 103 and 91, respectively. For both devices $BV_{\rm ceo}$ is reduced to 3 V by the high doping-level in the pedestal collector ($N_d = 10^{17}$ cm^{-3}).

Fig. 10 shows the measured $f_{\rm T}$ for two devices with a pedestal collector. This figure shows that for devices with a pedestal collector, the current density where the maximum $f_{\rm T}$ is reached is slightly higher for the device with a spike.

The devices without a pedestal collector discussed in the previous section show a relatively small decrease of τ_n when a spike is added to the epilayer. In these devices, the collector transit time [$\tau_c = (W_{BC}/2v_{sat}) \approx 2$ ps, where v_{sat} is the saturated drift velocity for electrons in Si] represents a large portion

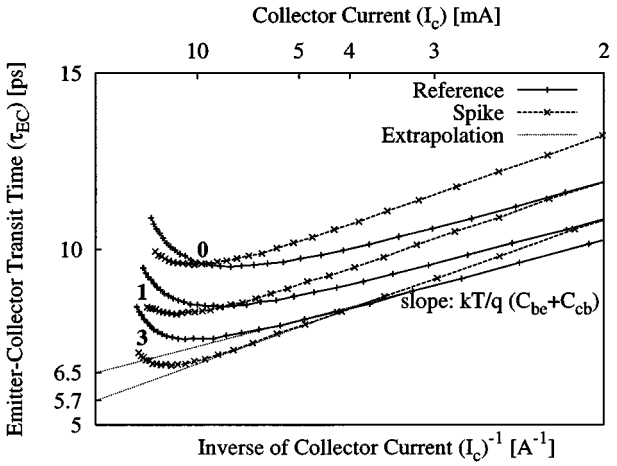


Fig. 11. Emitter–collector transit time τ_{ec} for devices with a pedestal collector. The reference transistor and the device with layer W_{225}. $V_{\rm cb}$ is set to 0, 1, and 3 V (indicated with bold numbers).

of τ_n. The collector τ_c is proportional to the width of the collector depletion-layer W_{BC}, which is reduced in devices with a pedestal collector due to the high collector doping.

Fig. 11 shows τ_{ec} versus $1/I_c$ for the devices with a pedestal collector. The figure shows that when a pedestal collector is used, the spike also reduces τ_n by $\approx$1 ps. With the collector storage practically eliminated, 1 ps reduction of τ_n has more effect. Moreover, pedestal collector devices show an equal or better performance for the full range of collector–base voltages when a spike is used, which shows that the improvement does not diminish at low $V_{\rm cb}$.

IV. Conclusions

This work shows the successful fabrication of silicon bipolar transistors with a very thin arsenic-doped epitaxial layer ("spike") at the collector–base junction. The epitaxial layers are fabricated with a commercially available AP-CVD reactor. The process is compatible with many bipolar processes, because the low diffusivity of arsenic allows very relaxed constraints on the thermal budget during further device fabrication. The

low transient-enhanced diffusion of As makes these layers a promising candidate for compensation of boron out-diffusion in SiGe transistors.

With very few modifications, the epilayers could be implemented in a standard bipolar process. These devices were used to demonstrate experimentally that devices with a spike have an improved high-frequency performance, resulting from a reduced basewidth, a higher acceptor concentration in the base, and a delay of the Kirk effect.

The basewidth is reduced by boron counterdoping in the arsenic spike. For all devices, a 1 ps reduction of the neutral transit time was observed. According to device simulations, the basewidth reduction and the increased doping concentration in the base contribute equally to this. The resulting improvement of high-frequency performance is more pronounced in devices with a relatively large contribution of the emitter–base region to the neutral transit-time: devices that combining a low BV_{ceo} with a high f_T.

The Kirk effect is delayed because a high concentration of n-type doping remains in the spike, which increases the total amount of doping in the collector. This allows a 60% higher current density before high-current effects reduce f_{T}. With a uniformly doped collector such an increase in current density can only be achieved if the breakdown voltage is compromised.

REFERENCES

[1] L. K. Nanver, E. J. Goudena, and H. W. van Zeijl, "Optimization of fully implanted npn's for high frequency operation," *IEEE Trans. Electron Devices*, vol. 43, pp. 1038–1040, June 1996.

[2] W. D. van Noort, L. K. Nanver, and J. W. Slotboom, "Control of arsenic doping during low temperature CVD epitaxy of silicon (100)," *J. Electrochem. Soc.*, vol. 147, pp. 4301–4304, 11 2000.

[3] B. Heinemann, K. E. Ehwald, P. Schley, G. Fischer, F. Herzel, D. Knoll, T. Morgenstern, W. Röpke, and W. Winkler, "Collector profile design of SiGe HBT's for optimized static and high-frequency performance," in *Proc. 25th Eur. Solid-State Device Research Conf.*, 1995, pp. 615–618.

[4] C. C. G. Visser, L. K. Nanver, and A. van den Bogaard, "Epitaxially grown n^+ phosphorus collector peaks in high-frequency HBT's with implanted emitters," in *Mat. Res. Soc. Symp. Proc.*, vol. 533, 1998, pp. 743–746.

[5] P. Palestri, C. Fiegna, G. A. M. Hurk, J. W. Slotboom, and E. Sangiorgi, "Optimization guidelines for epitaxial collectors of advanced BJT's with improved breakdown voltage and speed," in *IEDM Tech. Dig.*, 1998, pp. 741–744.

[6] P. Palestri, L. Selmi, G. A. M. Hurk, J. W. Slotboom, and E. Sangiorgi, "Energy dependent electron and hole impact ionization in Si bipolar transistors," in *IEDM Tech. Dig.*, 1998, pp. 885–888.

[7] J. W. Slotboom, G. Streutker, M. J. v. Dort, P. H. Woerlee, A. Pruijmboom, and D. J. Gravesteijn, "Non-local impact ionization in silicon devices," in *IEDM Tech. Dig.*, 1991, pp. 127–130.

[8] C. T. Kirk, "A theory of transistor cutoff frequency (f_t) falloff at high current densities," *IRE Trans. Electron Devices*, vol. ED-9, pp. 164–174, Mar. 1962.

[9] A. Schüppen, U. Ergen, A. Gruhle, H. Kibbel, H. Schumacher, and U. König, "Enhanced SiGe bipolar transistor with 160 GHz-$f_{\max}$," in *IEDM Tech. Dig.*, 1995, pp. 105–110.



Wibo D. van Noort (S'97) was born in Amsterdam, The Netherlands, on September 20, 1972. He received the M.Sc. degree in electronic engineering from Delft University of Technology (DUT), Delft, The Netherlands, in 1996, where he is currently pursuing the Ph.D. degree.

In 1996, he joined the Laboratory of Electronic Components, Technology, and Materials, DUT. His current research interests are CVD epitaxy, device physics, process technology, and (high-frequency) characterization and measurement.



Lis K. Nanver (S'80–M'83) received the M.S. degree in physics from the University of Aarhus, Aarhus, Denmark, in 1979, the Dr.Ing. degree from the Ecole Nationale Superieure des Télécommunications, Paris, France, where she worked on the simulation of CCD structures, in 1982, and the Ph.D. degree from the Delft University of Technology (DUT), Delft, The Netherlands, where she developed a medium-frequency BIFET process, in 1987.

In 1988, she joined the DIMES IC Process Research Sector as Bipolar Process Research Manager. Since 1994, she has been an Associate Professor with DUT, detached at DIMES Technology Center. Within the Laboratory of Electrical Components, Technology and Materials, she manages research on advanced Si-based devices that is at present mainly directed toward optimization and development of high-frequency Si BJT/SiGe HBT devices, using technologies such as AP/LPCVD epitaxy, dopant activation by excimer laser annealing, and substrate transfer techniques.



Jan W. Slotboom (M'82) was born in Utrecht, The Netherlands, on December 26, 1942. He received the degree in electrical engineering from the Technical University of Delft, Delft, The Netherlands, in 1966, and the Ph.D. degree from the Technical University of Eindhoven, Eindhoven, The Netherlands, in 1977, performing his dissertation on 2-D numerical device simulation of bipolar transistors and pioneering experiments on bandgap-narrowing in heavily-doped silicon.

In 1967, he joined the Philips Research Laboratories, Eindhoven, where he worked on bipolar device modeling, numerical simulation, and experimental silicon device physics. He was involved in the devolvement of CCD memories for video applications and exploratory research of high-density memories. His current research activities are on research of novel silicon devices (e.g., SiGe bipolar transistors), hot-carrier effects, and new memory cells. He has authored and co-authored over 50 papers and 14 patents. Since 1994, he has been a Part-Time Professor with the Micro Electronics Center (DIMES), Technical University of Delft.

Dr. Slotboom was a member of the Solid-State Devices Subcommittee of the IEDM in 1980, 1983, and 1984, respectively. He was Vice Chairman and Chairman of International Arrangements for Europe of the IEDM. He has served as a program subcommittee member of the IEDM in 1991 and 1992 and of the BCTM-'95 Conference. He has been a member of the technical program committee of the ESSDERC for the last six years.