A Transceiver ASIC for a Single-Cable 64-Element Intra-Vascular Ultrasound Probe

by

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Contents

Abstract

This work presents an ASIC designed to be integrated on the tip of an intra-vascular ultrasound catheter, capable of interfacing 64 ultrasonic transducer elements to an imaging system using only one micro-coaxial cable.

Cable count reduction and miniaturization of IVUS probes is important to create a more flexible catheter, simplify the mechanical construction and increase the amount of elements that can be read out. The reduction to one cable is made possible by a novel transmit switch circuit, an integrated low noise amplifier and a communication scheme that modulates data on top of the power supply.

A novel small-area transmit switch is used to pass or block the transmit pulses coming from a system side pulser. An arbitrary selection of transmit channels can be enabled to pass transmit voltages up to 26 V.

A phantom-powered low-noise current amplifier is proposed, that amplifies the echo signals received by piezo elements. The output current of the amplifier can be read out at the other end of the cable using a transimpedance amplifier. With three programmable gain settings a dynamic range of 74 dB is achieved.

By means of a self-clocking communication scheme the ASIC can be configured to select the transmit and receive channels and to set the gain of the amplifier. A redundancy check on the data has been added to monitor the data transmission quality.

An integrated test mode has been implemented to test the piezo elements after fabrication of the array, by measuring their capacitance. The low-noise amplifier is used as a comparator by opening the feedback loop. Combined with a current source at the input, a capacitance to time converter is created. Thus with the help of an FPGA at the system side, the capacitance can be digitized.

A prototype chip has been taped out in TSMCs 0.18 µm BCD Gen2 technology. The prototype has 64 channels that can be used in both transmit and receive mode and consumes 6.1 mW in receive mode. Post-layout simulations show promising results. A test chip is being prepared for experimental verification of the prototype.

This work shows the first ASIC that integrates transmit and receive functionality for a multi-element ultrasound probe using a single coaxial cable. With this contribution IVUS probes can be made more affordable and at the same te make better quality images compared to current devices.

Keywords: Intra-vascular ultrasound, single cable, current LNA, high voltage CMOS, transmit switch.

Acknowledgements

Writing this work could not have been done without the help and support of my colleagues, friends and family.

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Lastly I want to thank my caring parents for supporting me during my study at the Delft University and leaving me the freedom to choose my own direction.

Douwe van Willigen
Delft, June 2017

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Introduction

In the modern world we live a wealthy life, but prosperity comes with a price. Many people consume fatty and sugar-rich food and due to their office jobs don't get enough exercise in their daily routines. Those habits, amongst many other reasons, can cause cardiovascular diseases, nowadays the most common cause of death [1]. To be able to treat these diseases in time, early diagnosis is important. In Figure 1.1 the global mortality rate caused by chronic disease is shown. For high-income countries the improvement of diagnostics has reduced mortality by cardiovascular diseases, but globally it is still by far the main cause of death due to chronic disease. By reducing the complexity and price of the diagnosis tools the low- and middle-income countries can benefit as well from advances in the technology.

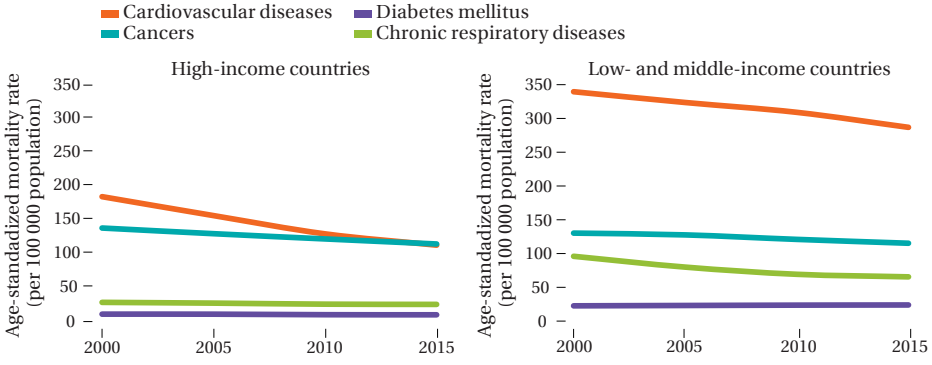

Figure 1.1: Global trend in mortality rate caused by chronic disease [1]

A common way of diagnosing artery diseases is by means of ultrasonic imaging. Using an ultrasonic imaging system doctors can diagnose the symptoms of the disease early on and take actions before more severe symptoms appear.

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1.1. Intra-Vascular Ultrasound

An intra-vascular ultrasound (IVUS) probe is a particularly small probe that is used for the diagnosis of vulnerable plaque inside the blood vessels of the human body. An IVUS probe can help in visualizing the state of an artery and identifying the degree of stenosis (narrowing of the artery).

To guide the probe towards the artery that needs diagnosis (e.g. the coronary artery), the IVUS probe has a more rigid end called the guide-wire. A cross-sectional view of an IVUS probe inside an artery is shown in Figure 1.2, together with an example of a reconstructed ultrasound image.

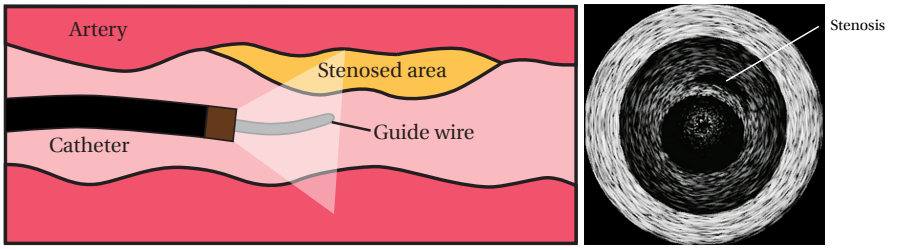


Figure 1.2: Cross-sectional view of an IVUS probe inside an artery and corresponding reconstructed ultrasound image [2].

In ultrasonic imaging, high frequency acoustic waves are used to image tissue in the human body. Figure 1.3 demonstrates the principle of imaging with a single element. An acoustic wave is emitted by applying a pulsing voltage to piezo material ①. The acoustical wave reflects on materials with a different acoustic impedance ②③ (e.g. lipid deposit). The reflection can be measured using piezo material as well, as an electrical signal is generated by the reflected wave. The time between transmitting the wave and receiving the echo is a measure for the distance of the reflecting objects. For transmit high voltage pulses (e.g. 30 V) are used, whilst in receive very small signal levels are generated by the piezo material.

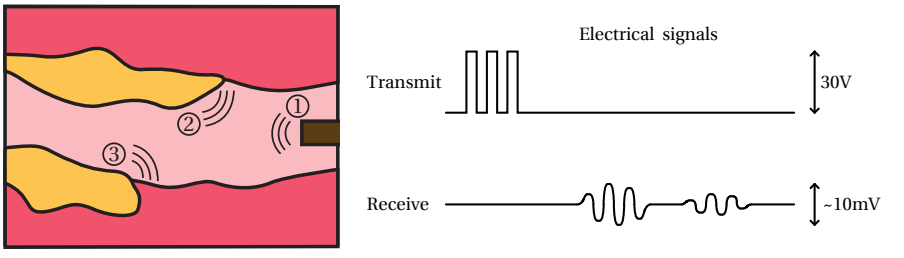


Figure 1.3: Ultrasonic imaging using pulse-echo measurement

To construct an image multiple piezo elements are put together in an array configuration. Using signal processing techniques an image can be constructed from the received echo signals.

Many array shapes for ultrasound probes exist. The most common type is the matrix array, shown in Figure 1.4. A regular matrix array comes with a relatively simple production process as it only requires straight cuts. However, the regular pattern has the drawback that the element pitch is limited to $\lambda/2$. A larger element pitch would result in significant grating lobes causing artefacts in the image. To get good quality images a large enough aperture is needed, resulting in a large number of elements, in particular for two-dimensional arrays.

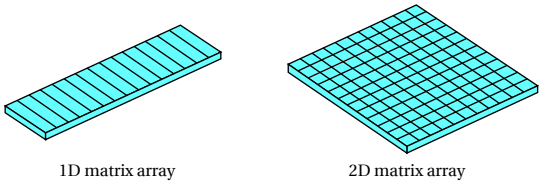


Figure 1.4: Common ultrasound array geometries

In intra-vascular imaging a more appropriate probe layout has a circular geometry, as blood vessels are usually circular in shape. Common types of circular probes use matrix arrays with sectioned annular rings, as shown in Figure 1.5, but due to their regular shape they also suffer from the effects of periodicity.

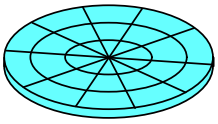
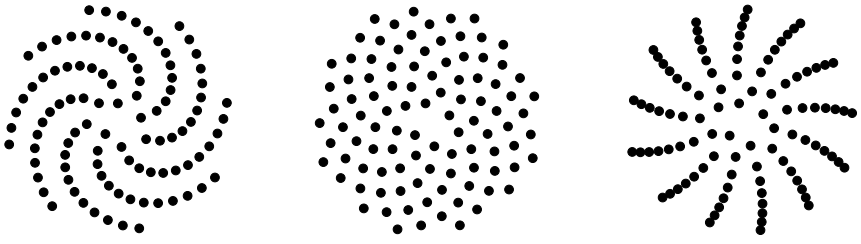


Figure 1.5: Sectioned annular rings

In the effort to reduce the periodicity of the pattern, spiral patterns and in particular the sunflower pattern have been proposed [3]. The sunflower pattern is a spiral constructed using the golden angle (137.51°). It realizes an efficient distribution of elements inside a circular area. Figure 1.6 shows the distribution of elements in spiral patterns for several angles.



(a) $\alpha = 136.0°$ **(b)** $\alpha = 137.5°$ (golden angle) **(c)** $\alpha = 138.3°$

Figure 1.6: Element distributions for several spiral angles

The elements in the sun flower pattern are not placed in a straight line, removing the periodicity of the geometric pattern. The grating lobes are therefore significantly reduced compared to regular patterns, resulting in an image with fewer artefacts.

1.2. Miniaturization

As catheter-based systems are inserted into the patient, big probes cause discomfort. Miniaturization of the probe helps to improve the comfort of the patient. The thickness and stiffness of the catheter are dominated by the coaxial cables connecting the individual piezo elements in the probe to the imaging system. A simple probe readily needs tens of cables. Moreover, the small coaxial cables have a high capacitance, attenuating the signal of the piezo elements with a much smaller capacitance. By integrating a circuit in the tip of the catheter, the amount of cables can be greatly reduced. With active circuitry the signal can be locally amplified and buffered, to improve the signal transfer to the imaging system.

1.3. Fabrication

The integrated circuit inside the probe has to be connected to the piezo elements. A very direct way of connecting the piezo elements is to fabricate them onto the die of the chip.

For prototyping we use the fabrication process described in [4]. Figure 1.7 shows a cross-sectional view of a fabricated piezo array. In the fabrication process, gold balls are bonded on top of the bond pads of the chip and a layer of epoxy is deposited over it. Subsequently the layer is ground until the gold balls are exposed. Then a layer of conductive glue is used to glue down a slab of piezo material (PZT). The piezo material is diced to create the desired pattern. Depending on the pattern complexity a dicing saw or laser is used to cut a kerf until halfway the epoxy layer. The dicing cut splits the piezo material in separate elements. Finally a conductive foil is placed on top to connect one side of the piezo material to a common potential (usually ground).

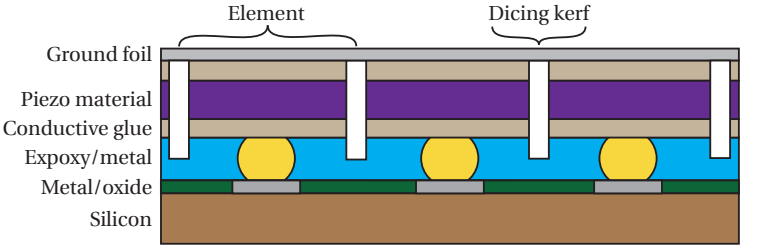


Figure 1.7: Cross sectional view of piezo-on-chip fabrication

1.4. Prior Art

In the effort to reduce the cable count in ultrasound probes, several contributions have already been published. A single cable readout IC for intra-vascular imaging [5] has been proven to be feasible, however it works for a single element and only in receive. For improved image quality multi-element solutions need to be considered. In [6] an IVUS front-end chip with reduced cable count is proposed that only uses 13 cables. A separate power supply for transmit and receive are used, as well as several buffered outputs for the received signals. Recently a digital probe capable of transmitting and receiving has been shown to work with only four cables [7].

An alternative approach has been shown in [8] where the authors propose to power the chip using two wires and have a wireless link to transmit the received data to the imaging system. This design however doesn't prove the possibility to transmit acoustic waves as it is taped-out in a low voltage technology (3.3 V). Moreover, the wireless link has only been proven with bulky antennas connected with an additional coaxial cable.

Table 1.1 gives an overview of the specifications and performance of the discussed prior art.

Table 1.1: Prior art

	[5]	[6]	[8]	[7]
Technology	0.18 µm	0.35 µm	0.35 µm	0.18 µm BCD
# coax. cables	1	13	2 *	4
Power (RX)	13.2 mW	20 mW	53 mW	10 mW
Bandwidth	20 MHz	40 MHz	40 MHz	16 MHz
RX channels	1	56	6	64
TX channels	-	64	6	16
TX voltage	-	25 V	-	26 V

* In [8] bulky antennas are used. Wireless transmit form a catheter has not yet been demonstrated. The mentioned 2 coaxial cables include one cable for the antenna.

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1.5. Motivation

In several ultrasound applications people are interested in performing measurements using small ultrasound probes. The piezo elements used in those probes are very small, causing them to have a high electrical impedance. A big issue with high impedance transducers is the large mismatch with the coaxial cable used to connect the element to an imaging system. The transducer impedance is often in the range of a few picofarads, whereas the cable has an impedance of several hundreds of picofarads. This causes a large attenuation of the signal.

To reduce the size of the catheter and keep it flexible the goal of this thesis is to make an ASIC (Application Specific Integrated Circuit) that only uses a single coaxial cable to connect to an imaging system. Furthermore, we aim at amplifying and buffering the signal so the load of the cable doesn't attenuate the signal.

In transmit, the probe should forward arbitrary high voltage pulses to the piezo element, while in receive it should amplify and buffer the signal. When feasible, a multi-element design should be created so images can be obtained using the probe. By using a single cable the complexity of the interconnection and production is reduced, potentially creating a more affordable probe.

An initial block diagram of the proposed system is shown in Figure 1.8. The block diagram shows the functions of the ASIC inside the tip of the catheter and a system side circuit to interface with an imaging system.

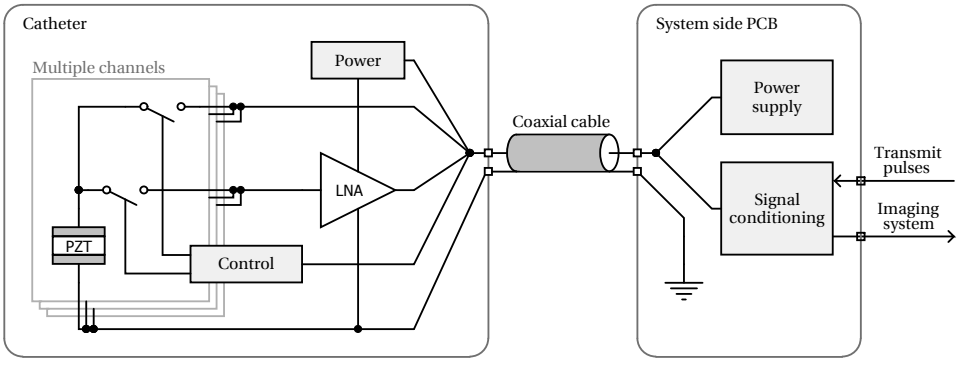

Figure 1.8: Block diagram of the proposed system

1.6. Design Objectives

The coaxial cable defines a lot of the circuit parameters as the power and output signals need to pass through it. For the intended applications a micro coaxial cable with a characteristic impedance of 50 Ω and a capacitance of 100 pF/m is used. The length of the cable is considered to be about 2 m.

The transmit pulse, used to actuate the transducer, has an amplitude of $30\,V_{pp}$ at a frequency of 2 – 20 MHz. The receiver should be able to receive pulses from 2 – 20 MHz. Furthermore the receiver should be optimized for a high impedance piezo element (10 kΩ or higher) with a target dimension of 80 µm by 80 µm. The probe should at least have a dynamic range of 60 dB in receive mode. Harmonic distortion is not a big concern as the ultrasound probe operates at a single frequency. A 3 dB reduction of the fundamental is acceptable and higher order harmonics can be filtered out in the digital domain.

Figure 1.9 shows a timing diagram of the signal on the piezo material. The delay between start of transmit and receive ($t_{tx}+t_d$) should be around 1 µs, when used at 20 MHz.

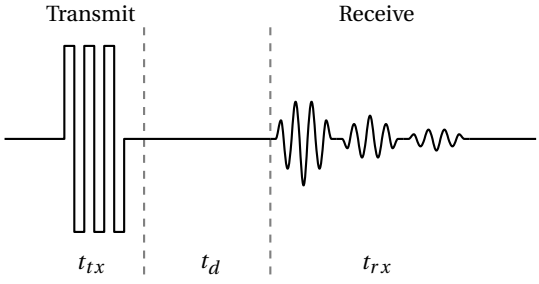

Figure 1.9: Timing diagram of transmit-receive cycle

Power dissipation causes the probe to heat up, therefore it is important that the dissipation is kept to a minimum. The maximum allowable dissipation commonly used for ultrasound probes is 100 mW [9], however a lower power dissipation is preferred.

Table 1.2: Target specifications

# coax. cables	1
Cable length	2 m
Power (RX)	< 100 mW
Dynamic range	60 dB
Transmit voltage	30 V
Bandwidth	2-20 MHz
Piezo dimensions	80 µm × 80 µm

The circuit will be designed for a tape-out in TSMCs 180 nm BCD-Gen2 technology.
A detailed discussion on the best technology choice for miniature ultrasound probes can be found in Appendix A.

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1.7. Thesis Organization

This thesis presents the steps taken to design a single cable ultrasound probe for intravascular ultrasonic imaging. The chapters are organized in a chronological order, starting with the concept ideas and discussions on possible circuit topologies converging towards a good circuit implementation.

Chapter 2 will discuss the parts of the system that define the architecture of the probe.

Chapter 3 discusses the circuit implementations to realize the architecture onto an ASIC.

Chapter 4 reviews the layout of the circuits and the changes needed to reduce the effect of layout parasitics and shows the post-layout performance of the completed ASIC.

Chapter 5 shows an implementation of the system side circuit that is needed to drive and readout the ASIC.

Chapter 6 concludes the thesis by discussing the performance of the final circuit and presents some ideas for future work and improving the design.

The appendices show detailed information that can be used during bonding and the fabrication of the piezo elements.

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Architecture

In this chapter the system architecture will be discussed. First the coaxial cable and its properties will be evaluated to see how it can best be used in the intended application. Next an investigation will be done into ways to supply the chip with power and at the same time send a signal over the cable.

The chip needs to be protected from the high voltage pulses during transmit. Several topologies will be analysed to see how the chip can survive the transmit pulses.

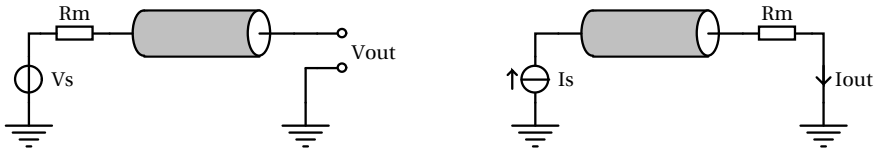
Lastly, the architecture for the low noise amplifier (LNA) will be derived using the specifications of the probe and limitations of the coaxial cable.

2.1. Coaxial Cable

The coaxial cable has a substantial length. It is specified to be 2 m long, which is less than an order of magnitude smaller than the wavelength of 15 m (at 20 MHz). Therefore transmission line effects will have a significant influence on the signal.

Two types of cables were investigated for the use in this application. The first type is a 48 AWG (0.17 mm) coaxial cable [10], that due to its high series resistance of 22 Ω/m attenuates the signal significantly. A thicker cable of 42 AWG (0.3 mm) [11] was also considered.

According to [12] a coaxial cable should be terminated characteristically at least at the receiving end, to prevent reflections. As the signal source is the ASIC, the matching resistor can be placed at the system side, which is the receiving end. This is nice because it means that it can easily be tuned and the power dissipated in the resistor does not heat up the probe. Figure 2.1 shows a transmission line terminated at the driver side and one terminated at the receiver side. In both cases series termination is used.



(a) Driver side termination **(b)** Receiver side termination

Figure 2.1: Series terminated transmission lines

A signal that is generated by a voltage source on the driver side can be terminated on the receiver side by parallel termination (not shown).

To simulate the transmission line the Spectre multi-conductor transmission line model (mtline) is used. The model parameters are the lumped elements of a unit length transmission line, as shown in Figure 2.2, and the length of the transmission line.

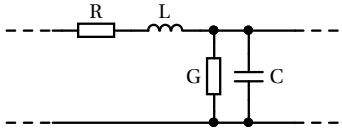


Figure 2.2: Lumped transmission line model

The parameters used for the simulation are shown in Table 2.1. For the 48 AWG cable the values are obtained from measurements performed in [13], those parameters match the values given in the datasheet well. For the 42 AWG cable the parameters from the datasheet [11] are used.

Table 2.1: Micro coaxial cable parameters

	42 AWG	48 AWG
R_{DC} (Ω/m)	7.5	22
C_{gnd} (pF/m)	110	120
L (nH/m)	275	300
G (nS/m)	660	660
Attenuation (dB/m)	0.7	2.0

The characteristic impedance of a lossless transmission line is given by (2.1) [14]

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.1}$$

With the given model parameters, we find a characteristic impedance of 50 Ω for both cables. The characteristic impedance can be used as the reference value for the termination resistor.

Figure 2.3 shows the simulated attenuation in the two types of cables (Blue: 42 AWG, Green: 48 AWG). When no termination resistor is used constructive and destructive interference caused by reflections are clearly visible as peaks in the signal transfer. The plot corresponds to both (equivalent) circuits, shown in Figure 2.1.

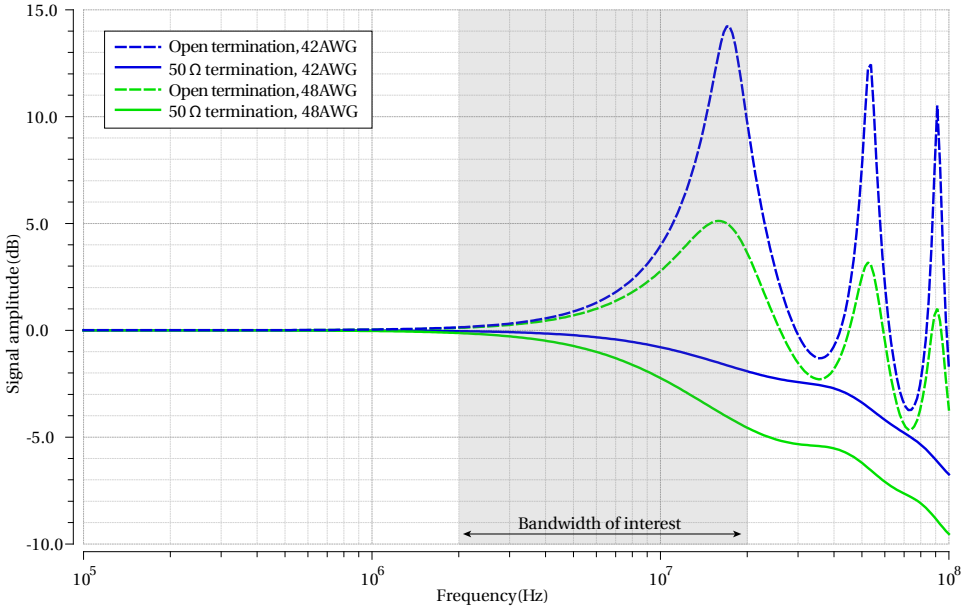


Figure 2.3: Attenuation of a 2 m coaxial cable with and without characteristic series termination

The simulations show that the attenuation of the 42 AWG cable is less than 3 dB inside the bandwidth of interest, making it a good candidate for this system. Also visible is

that for frequencies below 1 MHz the signal is indeed not affected by transmission line effects.

All simulations performed in the thesis include the 2 m coaxial cable, unless otherwise stated.

2.2. Signal and Power Over One Cable

To be able to create an ASIC that only needs a single cable to operate, it is necessary to have the power provided over the same cable as the output signal. In both audio electronics [15] and RF electronics [16] this is commonly done to power and readout a system with the same cable. Such a power supply is called a phantom power supply.

An RF phantom power supply is shown in Figure 2.4. The supply can be considered low frequency and can thus pass through the inductors, but is blocked by the capacitors. For the signal which is modulated at a high frequency, the capacitors are a low impedance but the inductors in turn are high impedance and block the signal.

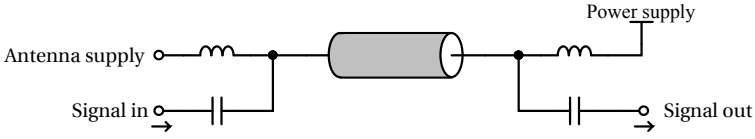


Figure 2.4: Schematic diagram of antenna phantom power supply

The principle relies on the fact that the power supply and the receive signal are separated in the frequency domain. The power supply is provided as a low frequency signal (or DC) and the signal is transmitted at a high frequency.

For ultrasound systems a similar approach can be taken, because the signals usually have a frequency above 2 MHz. Although implementing inductors is not possible in the selected CMOS technology, as it does not include large enough inductors, it is possible to separate the signal and power supply in other ways. When for example a DC voltage is supplied to the amplifier, the current flowing through the amplifier can be measured at the other end of the cable. The current needed to bias the amplifier can be seen as a low frequency or DC signal, while the amplifier can be designed to draw a current proportional to the input signal. Alternatively the reciprocal case can be implemented, where a constant current is supplied and a generated voltage can be measured at the current source.

2.3. Transmit-Receive Switching

When the ultrasound pulses are being transmitted, the ASIC has to pass the signal provided on the cable to the selected piezo element. In receive mode however this is not desired, as the same piezo material is used as a sensor. If the cable would then be connected to

the piezo material, the receive signal would not be measurable. Therefore the transmit switch should turn off as soon as the receive mode is activated.

Two operating modes should thus be defined: transmit and receive. To switch between the two modes a means of controlling the mode is needed. A simple way to do this would be to change the mode of the chip using communication. However it would be safer if the chip detects by itself, given the signal on the cable, in which mode it should operate. This would make the chip more robust against wrong configuration and the high voltage transmit pulses.

Looking at the voltages on the coaxial cable in transmit and receive mode, shown in Figure 2.5, a clear distinction can be made. We know that when the voltage rises above 5.5 V it must be a transmit pulse, as the low voltage transistors of the receive mode are not rated for voltages above this level. In receive a bias voltage is needed for the transistors to operate, therefore the voltage on the cable will be between (e.g.) 1.1 V and 5.5 V.

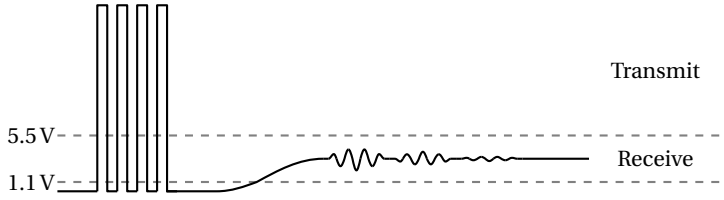
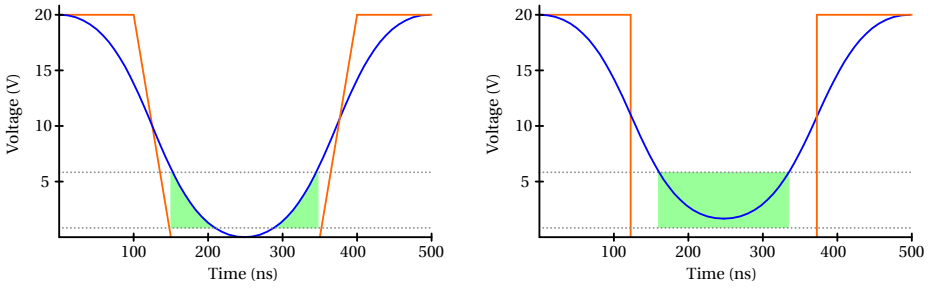


Figure 2.5: Voltage present on the cable in transmit and receive mode

Indicating the correct mode by using only the voltage limits the voltage range for the transmit pulse, as it should not drop below 5.5 V. Otherwise the ASIC will activate the receive mode and turn off the transmit switch.

To make sure the transmit switch doesn't switch off during a transmit cycle that contains voltages below 5.5 V, it would be better to add a delay before the receive mode is enabled. We know from the specifications that the lowest transmit frequency is 2 MHz. The signal of a sine transmit pulse will not be in the receive-voltage range for longer than about 50 ns, as shaded green in Figure 2.6a. For a square wave the time within the specified receive-voltage range is even shorter. However, when the transmit pulses have a limited



(a) Full swing transmit pulse

(b) Limited swing transmit pulse

Figure 2.6: Longest specified low-time (1.1 V < V < 5.5 V) of a transmit pulse

swing, due to for example voltage drop over the cable, the voltage doesn't go below 1.1 V

and the maximum time in the receive-voltage range is extended to 200 ns, as shown in Figure 2.6b. For an ideal square wave of 2 MHz this time is even 250 ns.

Using this knowledge, a delay can be added before the receive mode is enabled and thus the transmit switch will be turned off. The operating boundaries for the transmit and receive mode are shown in Figure 2.7. Assuming the low frequency transmit pulses cross the 1.1 V boundary, a delay of 150 ns is sufficient. This delay allows higher frequency pulses (> 3.3 Mhz) that don't swing below 1.1 V to be used as well.

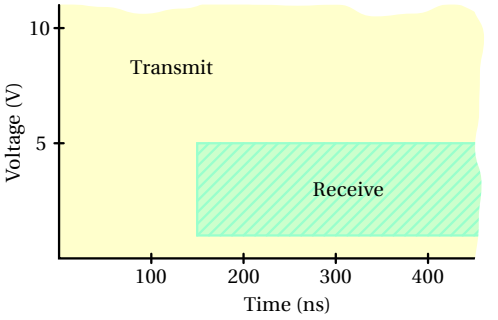


Figure 2.7: Receive mode enabling conditions

2.4. Protecting the Receive Circuitry

Only the high voltage devices can handle voltages higher than 5.5 V, the other devices need some kind of protection to not get damaged by the transmit pulses.

Conventional ultrasound probes use a diode limiter to protect the LNA in combination with an expander to transmit using the same cable [17]. Although simple to implement, the topology dissipates a significant amount of power during transmit and the output voltage of the LNA can not exceed a diode drop, set by the diode limiter. For an application that needs to be powered via the same cable this method is not feasible.

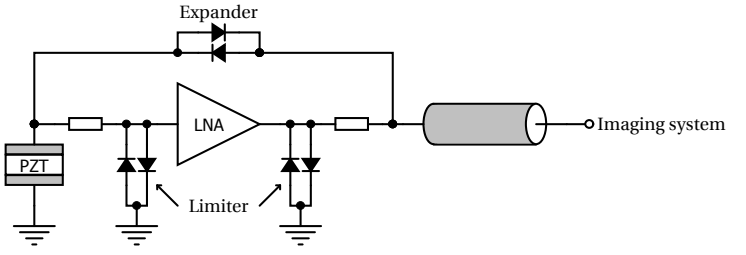


Figure 2.8: Conventional diode limiter and expander

Variations replace the resistors by capacitors or depletion mosfets [18][19] to reduce power consumption and noise or increase the bandwidth [20]. In both improved circuits, excess energy is still shunted to ground causing unnecessary power dissipation.

Alternatively a common way to protect the LNA input (for usually a system side LNA) is by using a bridge structure which is even more power hungry as it needs a relatively high DC current to make the diodes small signal impedance low enough [18].

An interesting protection scheme is proposed in [21], where shunt switches are used on both sides of the piezo material (depicted in Figure 2.9). This can potentially cause a large reduction in area as it only needs one high voltage switch per element (the switch that is enabled during receive, RX). However, due to the fabrication method (as discussed in Chapter 1.3) one side of the piezo material is always connected to ground. Therefore another protection scheme must be used.

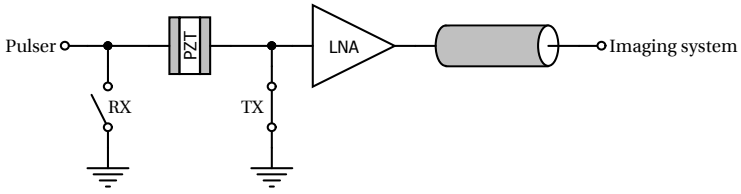


Figure 2.9: Protection scheme proposed in [21]

Clamping the input voltage can also be done by an NMOS transistor with a fixed gate voltage and the source connected to the circuit that needs protection, as shown in Figure 2.10. In normal operation the gate voltage of the clamping transistor will cause it to conduct. However, when the voltage at the source exceeds $V_G - V_{Th}$ the transistor turns off, protecting the circuit connected to its source. This method requires careful design as the parasitic (drain-source) capacitance of the clamp can still cause the source to rise above the maximum allowable voltage. The improvement compared to the other protection circuits is that the circuit is completely switched off when a high voltage is present, no power is shunted to ground. A drawback for this topology is that a reference voltage (V_{clamp}) is required that sets the clamping voltage.

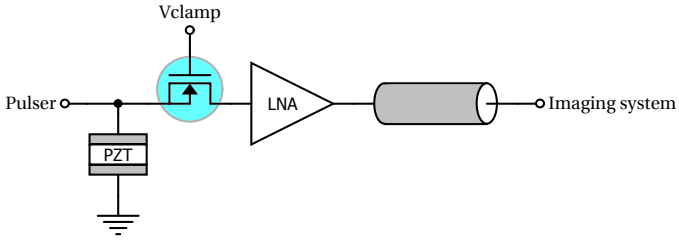


Figure 2.10: NMOS voltage limiter

The protection circuit shown in Figure 2.10 is chosen to protect the ASIC of this work. It is not only energy efficient by switching off instead of shunting the energy to ground, it is also able to pass DC signals with a low on-resistance, making it suitable to protect the output of the LNA as well.

2.5. Low Noise Amplifier

An amplifier is required to amplify the signal well above the noise level of the cable and termination resistor. Moreover, the signal needs to be buffered so the cable capacitance doesn't load the piezo element.
In this section nullors are used to find the right topology for the amplifier. A nullor is an ideal active circuit element with infinite gain and an input voltage and input current of zero [22].

2.5.1. Reading Out the Piezo Material

The best way to read out the piezo material depends on its impedance and the interface with the amplifier. A sensor can be read out in two (ideal) ways. By using an amplifier with a low impedance input, the signal current of the sensor can be read out. Alternatively the sensor can be read out by using a high impedance amplifier, sensing the voltage.

Piezo material has a significant capacitance. By creating an amplifier with a low impedance input (current input) the parallel capacitance will have a smaller influence on the signal. Furthermore, for a voltage input, the input impedance of the amplifier will load the piezo impedance causing attenuation. Therefore the input impedance should be significantly higher than the piezo impedance (e.g. 10x).

For bulk piezoelectric transducer elements, the Butterworth Van Dyke (lumped element) model is often used [23], shown in Figure 2.11. It is the simplest circuit that models the resonant behaviour of piezo material, and is valid close to the resonant frequency.

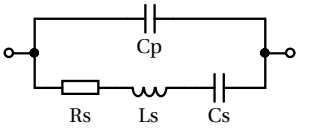


Figure 2.11: Piezo transducer lumped element model

To get an impression of the size of the piezo impedance, the model parameters of some measured piezo elements were analysed. Table 2.2 shows the model parameters for two sizes of PZT piezo elements.

Table 2.2: PZT model parameters

Element dimensions	R_s	L_s	C_s	C_p	F_{res}
70 µm × 70 µm	23.6 kΩ	811 µH	227 fF	311 fF	14 MHz
150 µm × 150 µm	2.18 kΩ*	992 µH	1.03 pF	938 fF	5 MHz

*In measurement this value was 2-3 times higher

Given the model parameters, for a piezo element of 80 μm × 80 μm, as targeted in this work, an impedance of 15 kΩ to 20 kΩ can be expected.

A quantitative analysis to find the preferred sensor readout topology is described in [24]. The work shows that a current readout is always preferred over a voltage readout for high impedance transducers, because it has a better noise efficiency than a voltage readout circuit.

Using some assumptions for the amplifier input capacitance, a qualitative analysis can be performed.

For the given size piezo material the noise requirements of the amplifier, create an input capacitance (C_{in}) in the order of 100 fF. This results in the amplifier input impedance to be in the order of 80 kΩ, as given in by:

$$Z_{\text{in}} = \frac{1}{2\pi f C_{\text{in}}} \tag{2.2}$$

For a current amplifier the feedback causes the input impedance to be lowered by the gain of the amplifier [25], as given by:

$$\begin{aligned} Z_{\text{in}} &= \frac{Z_{\text{f}}}{A-1} \\ Z_{\text{in}} &= \frac{1}{(A-1)\left(2\pi f C_{\text{f}}\right)} \end{aligned} \tag{2.3}$$

When a gain of 100× is used in combination with a feedback capacitor (C_{f}) of 100 fF, an input impedance of about 800 Ω is found.

From those quick calculations, we find that input parasitic capacitance makes it hard to create a voltage input that has an impedance significantly higher than the piezo material. In the example an input impedance of only 4 × higher is found. For the current input, the feedback network helps to reduce the input impedance, resulting in a value almost 20 × smaller than the impedance of the piezo element. This confirms that current read-out is a good choice for high impedance transducer elements.

2.5.2. Amplifying the Signal

Two types of current input amplifier topologies exist. One of them converts the current to a voltage, called a Transimpedance Amplifier (TIA), shown in Figure 2.12. In order to be able to pass the output voltage to the system via the single cable, this topology would need a DC current as the power supply. Such an amplifier has already been proposed in [5], where an integrated version of a single cable amplifier has been demonstrated to read out piezo material.

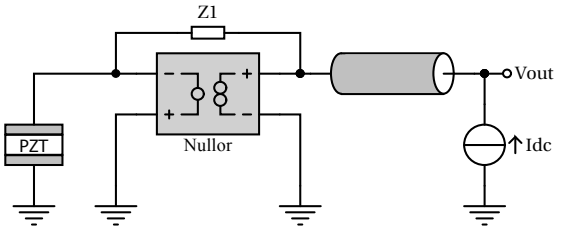


Figure 2.12: Nullor implementation of a single cable transimpedance amplifier

The other topology is a current amplifier, shown in Figure 2.13. The signal output is a current, so the power supply has to come from a constant voltage source, when used with a single cable.

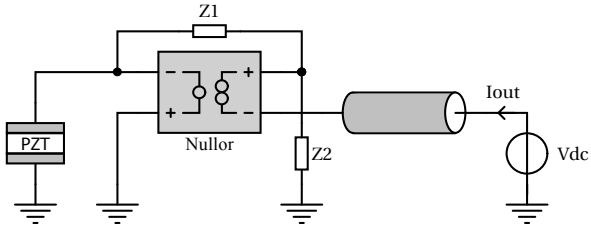


Figure 2.13: Nullor implementation of a single cable current amplifier

To find the best topology both the start-up time and power consumption have been considered.

Looking at the chip from the system side, the chip and cable appear as a mostly capacitive load. When a capacitance C is charged using a constant current, it will take a well defined time before the capacitor reaches the intended voltage, as defined by:

$$\Delta t = C\frac{\Delta V}{I} \tag{2.4}$$

Assuming a supply voltage of 1.8 V to 3 V and a power dissipation of 6 mW (3.3 mA and 2 mA respectively), the rise time would be 120 ns to 330 ns. Clearly the rise time is dependent on the power consumption and operating voltage of the amplifier. Moreover, when the amplifier is optimized for a low power consumption, the rise time would increase.

On the other hand, when a constant voltage is used to supply the amplifier, ideally the capacitance can be charged instantaneously. Due to the resistance of the cable and matching resistor the time will be longer, as given by the 90% rise time:

$$\begin{aligned} \Delta t &= 2.2\tau \\ \Delta t &= 2.2 \cdot RC \end{aligned} \tag{2.5}$$

For the given cable (220 pF, 14 Ω) and matching resistor (50 Ω), the charging time would be 31 ns. Note that in this case the rise time is independent on the amplifier supply voltage and current.

As specified in the introduction of this thesis, the chip needs to switch from transmit to receive in a very short time, a long start-up time can therefore not be tolerated. From these two quick calculations we find that, with the specified cable, the operating voltage of the ASIC will be reached much quicker using a voltage source to power it.

Furthermore, as the cable potentially has a bigger capacitance than the chip, it is more efficient if it is charged from the system side. In the case where the chip output is a voltage, the chip needs to drive the cable capacitance, whilst with a current output, the system side will charge and discharge the cable capacitance.

Given the power benefit and the shorter rise time, the best amplifier topology for the single cable amplifier is the current amplifier.

2.5.3. Feedback Network

For the implementation of the nullor topology shown in the previous section, the best feedback network needs to be chosen. The feedback network ideally uses only capacitors as they don't generate noise. In practice a high valued resistor is added to the feedback network to ensure a correct DC operating point [26].

The resulting nullor including feedback network is shown in Figure 2.14.

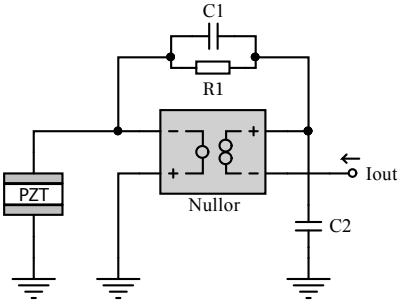


Figure 2.14: Current amplifier

Analysis of the feedback network shows that the closed-loop gain (assuming the capacitor dominates the feedback network) can be defined by:

$$A_{CL} = 1 + \frac{C_2}{C_1} \tag{2.6}$$

The capacitance of the piezo material is not part of the equation as it is at virtual ground of the amplifier and therefore doesn't influence the gain. Another benefit is that the input capacitance doesn't influence the stability of the amplifier.

An amplifier that implements the circuit shown in Figure 2.14 was published in [27]. Although used in a TIA topology, by adding a resistor in series with the current output, it proves that a low noise amplifier can be constructed using this topology with a bandwidth of 622 MHz. Several others have used this topology for amplifiers with a high transimpedance gain, optimized for MEMS [28] and IVUS applications [26].

Although the input capacitance doesn't influence the gain of the amplifier, it does influence the overall noise performance of the amplifier because the noise gain of the nullor implementation will increase for higher input capacitance.

2.5.4. Powering and Reading Out the LNA

Most conventional amplifier and buffer designs output a signal voltage. When a cable capacitance is involved it needs to be charged and discharged by the amplifier or buffer. This means that the power needs to be sent to the ASIC and then back into the cable via the buffer. By using a current output, the cable capacitance can be charged from the system side, which reduces the power dissipated in the ASIC.

This does however create the need for a cable driver at the system side that is fast enough to supply any change in current flowing to the ASIC. At the same time it needs to generate an output voltage proportional to the current flowing through the cable. A transimpedance amplifier can be used at the system side to convert the signal current into an output voltage. Thanks to the feedback loop of the transimpedance amplifier the input voltage (and thus the voltage provided to the cable) will nicely follow the voltage supplied at the non-inverting input.

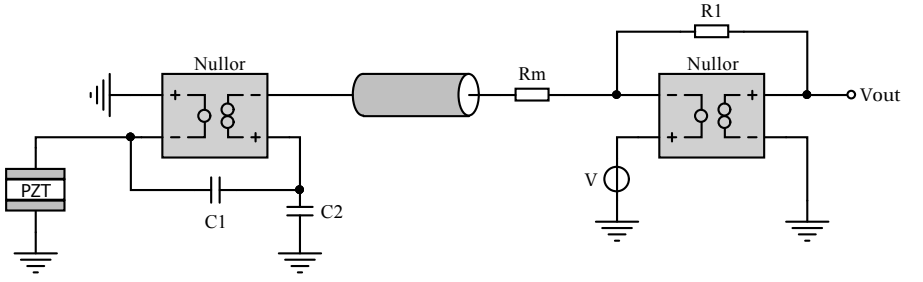


Figure 2.15: Receive mode system topology

As the system side doesn't need miniaturization an off-the-shelf operational amplifier (opamp) can be used for this purpose. An opamp should be chosen that does not limit the bandwidth and noise of the system. For the power consumption no constraint is specified, as the circuit is located outside the patient.

In the ideal case the input impedance of the transimpedance amplifier is zero. However, as any nullor implementation has a gain that is not infinitely large, the input impedance will be larger than zero. This causes the need for the matching resistor (R_m in Figure 2.15) to be smaller than 50 Ω.

Looking at the feedback network, we can write the equation of the TIA input impedance as (2.7).

$$Z_{\text{in}} = \frac{-R_1}{A} \tag{2.7}$$

The equation shows that a high gain is needed if we want to keep the mismatch with the cable impedance small. Additionally, the cable and matching resistor introduce a resistance in the path from the the power supply to the ASIC, causing a voltage drop. When a current of 2 mA is supplied this voltage drop will be 128 mV (assuming series resistance of 64 Ω for the cable and matching resistor). This is a manageable voltage drop, but it should be kept in mind during the design process.

2.6. Communicating with the ASIC

Using the architecture described in the previous sections, the probe is not yet able to work with multiple elements. To switch between different channels a multiplexer is needed that can select a single channel for read-out. A channel can be selected by rotating through all elements in a pre-defined way, but a more versatile operation can be created by making the ASIC programmable. A way to communicate with the ASIC is therefore desirable.

In the previous section it was discussed that the ASIC should use a constant voltage as the power supply, so the output signal can be generated as a small-signal current. This means that the only way to send data over the cable to the ASIC, is by modulating the supply voltage. Figure 2.16 illustrates how a binary signal with a small amplitude is added to the power supply voltage.

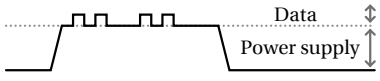


Figure 2.16: Data modulated on the power supply voltage

By AC-coupling and amplifying the data signal inside the ASIC it can be recovered and used to configure the channels and possibly other settings of the ASIC, as shown in Figure 2.17. The data can just like the DC voltage be supplied at the non-inverting input of the transimpedance amplifier.

The matching resistor, initially placed to characteristically terminate the signal current from the ASIC, is now exactly in the right location for series termination of the voltage coming from the system side. Although not placed at the receiving end, it can still help preventing reflections of the configuration data.

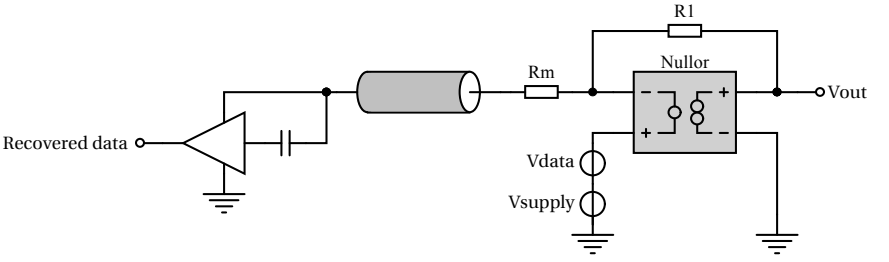


Figure 2.17: Schematic of the data transmission and recovery topology

As discussed in the previous section, the voltage drop over the cable and matching resistor will cause a small output signal dependent voltage swing at the chip side of the cable. It is important that this voltage swing isn't read as configuration data. To ensure this doesn't happen, the data recovery should not be sensitive for small signal levels. The maximum swing to be expected using a 2 mA peak-to-peak output signal is below 150 mV. When the minimal amplitude before the data recovery circuit starts working is chosen higher than this (e.g. 200 mV), the receive signal will not wrongly activate the data recovery circuit.

3

Circuit Design

This chapter will discuss the circuit implementations of the functional blocks needed for the ASIC. First the transmit switch will be designed and the LNA described in the previous chapter will be implemented. Next the logic required to operate multiple channels is discussed and the bias and voltage sources for the LNA will be designed. Finally the circuits will be combined into a complete circuit to be implemented on the ASIC.

All simulation results shown in this chapter are for the complete ASIC circuit including the cable, unless otherwise stated.

3.1. Transmit Switch

The transmit pulses are passed to the piezo element by a mosfet switch. Because of the single cable, the switch needs to be enabled before the transmit pulse is active. The switch needs to be disabled when the chip switches back to the receive mode as discussed in section 2.3. Many channels have to be implemented so the size of the transmit switch is one of the most important parameters for the implementation.

3.1.1. Area of High-Voltage Transistors

In CMOS design it is common to use N-MOS switches when a low on-resistance is needed, because they have a significantly smaller area than a P-MOS transistor with the same on-resistance. In high voltage CMOS however, the difference in size for transistors with the same on-resistance is much smaller, as a large part of the transistor size is occupied by the isolation rings. Figure 3.1 shows a comparison of the three types of 36 V rated high voltage transistors available in the TSMC 0.18 µm BCD technology. To use an N-MOS transistor at the high side (with the source not connected to the substrate), an extra isolation ring is required to disconnect the bulk from the substrate. The extra isolation ring causes the transistor to have very bulky dimensions (GB, Figure 3.1 left).

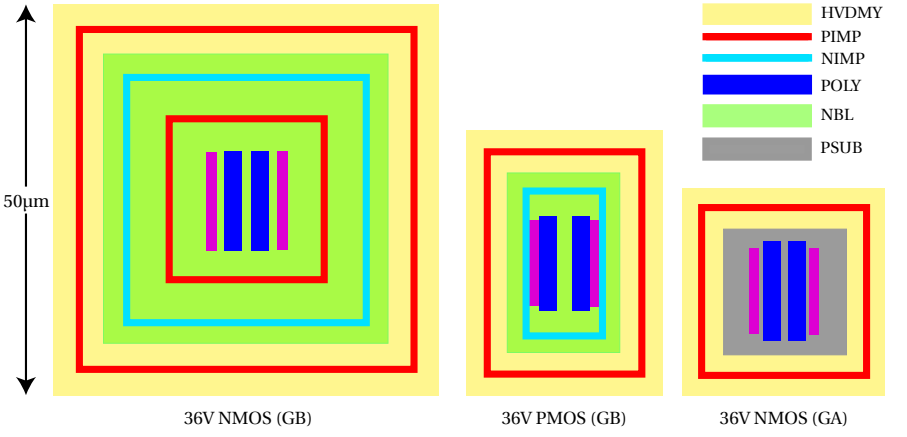


Figure 3.1: Comparison of high voltage transistors with equal gate size (2 fingers of 10 μm)

As is clear from the diagram, for a high side switch the best choice is to take the P-MOS device. When using an N-MOS device, whenever possible a GA device should be used. The bulk and source of a GA device are connected to the substrate and can not be used at higher potentials. Any floating transistor must therefore be a GB-type device.

3.1.2. Transmit Switch Circuit

In ultrasonic imaging applications, the transmit phase is usually implemented by directly connecting each element with a cable to a pulser. To reduce the amount of cables needed for transmit, designs have been proposed to move the pulser closer to the piezo element. Those pulsers tend to only be able to transmit square wave pulses, by switching the element to a high voltage line or to ground. Two common implementations [29] [30] are shown in Figure 3.2. The benefit of a pulser is the relatively small size, but due to the arbitrary waveform specification set in the introduction, it is not sufficient in this work to implement a pulser on the ASIC.

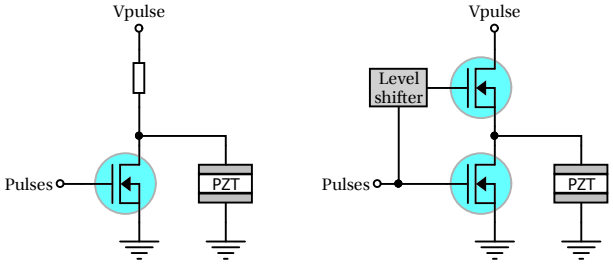


Figure 3.2: High voltage pulser topologies

To transmit arbitrary waveforms a switch has to be designed that can be enabled or disabled and will remember its state. A latching transmit switch, as proposed in [31] would be a good implementation of such a switch. The circuit is shown in Figure 3.3. A pulse on the enable (EN) pin causes the bootstrap capacitor (C_1) to be charged, turning on the high voltage switch. A pulse on the disable ($\overline{\text{EN}}$) pin shorts the bootstrap capacitor and disables the switch. Capacitor C_2 is used to remember the state of the other branch in the latch.

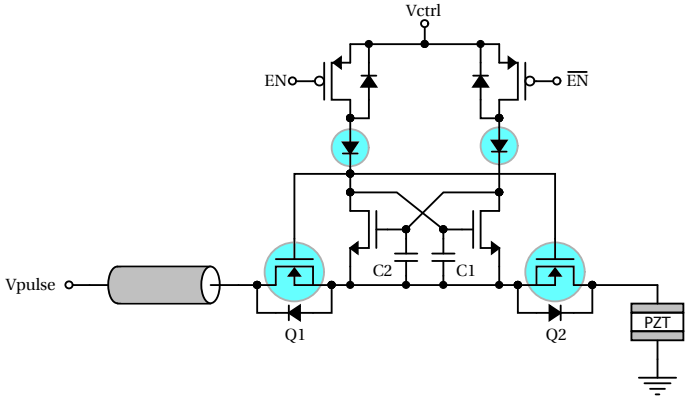


Figure 3.3: Latching high voltage switch

As apparent in the circuit shown in Figure 3.3, the switch contains four high voltage

devices (shaded in blue) and floating low voltage transistors that need an isolation ring as well, resulting in a large occupied area.

A configurable latching switch with a reduced area is proposed in [32] as shown in Figure 3.4. The switch can be enabled by putting a logic high (5 V) on V_2 and pulsing V_1 to 5 V. To turn off the switch, the voltage at V_2 is reset to 0 V.

When bidirectional isolation is not needed, one of the high voltage transistors can be left out (Q_2 in Figure 3.4) as proven effective in [7]. This reduces the amount of high voltage transistors as well as the size of the switch transistor, because the single transistor can have the same on-resistance as the previously used two transistors combined. Still the size is significant because one of the devices is a floating NMOS transistor.

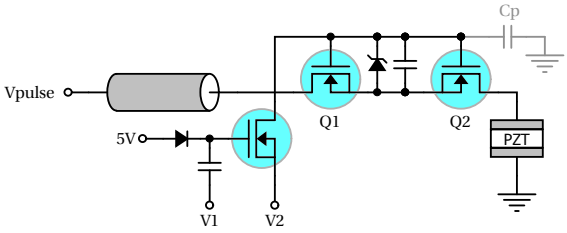


Figure 3.4: Reduced size latching high voltage switch

The bootstrap capacitor in Figure 3.4 is also very big. The large size is mainly needed due to charge sharing with the parasitic capacitor C_p. For the back-to-back version in [32] the capacitor is 7.2 pF. The simplified version has fewer parasitics and can thus use a significantly smaller capacitor of 2.8 pF, however such a capacitor is still very large (5300 μm^2 in [7]).

Implementing a switch with a smaller area is clearly not straightforward. At first glance a simple technique could be to use the circuit shown in Figure 3.5 on the left. The circuit uses a P-MOS transistor as the switch, which has a relatively small area. The N-MOS switch is tied to ground and can thus also be relatively small. However, the circuit as it is shown does not work. The P-MOS transistor can not be turned off: Due to the parasitic drain-source capacitance ($C_{ds} \approx 50$ fF) the transistor will also turn on with a transmit pulse when the enable signal is low.

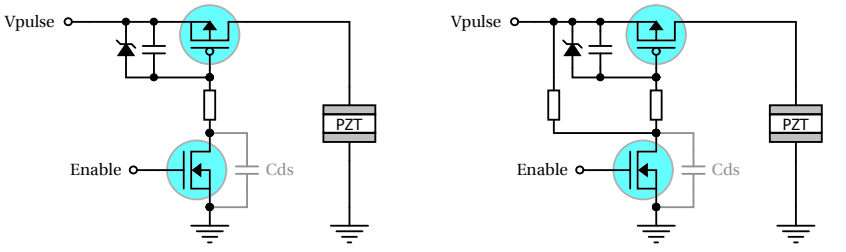


Figure 3.5: High voltage switch, not working (left) and working (right)

A countermeasure to remove the effect of the parasitic capacitor is to add a resistor or

current source between V_{pulse} and C_{ds} to charge the parasitic capacitance when the enable signal is low. This creates a switch that is functional and has a relatively small size, but the resistors take up a large area as they need isolation rings to make them compatible with the high voltage pulses.

The size can be reduced even further by replacing the resistor by a capacitor, as shown in Figure 3.6. Now C_1 and C_2 form a capacitive divider when the transmit switch is enabled. When the switch is disabled the series equivalent of C_2 and C_{ds} forms a divider with C_1. By correctly choosing the values of the capacitors a compact transmit switch can be realised. A current source (Q_{i}) is used so the switch can also be turned off when the voltage on V_{pulse} is non-zero. In that case the current source pulls the drain-source voltage of the N-MOS transistor up to V_{pulse}.

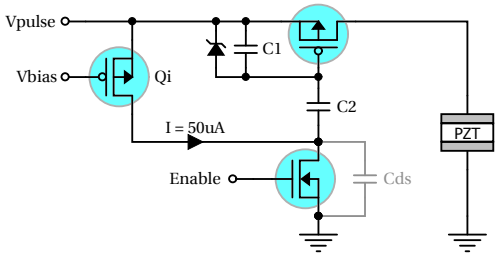


Figure 3.6: Complete transmit switch circuit

The gate voltages for the transmit switch are defined by the equations following equations:

$$V_{\text{gs,on}} = \frac{C_2 \cdot V_{\text{pulse}}}{C_1 + C_2} \tag{3.1}$$

$$V_{\text{gs,off}} = \frac{(C_2 C_{\text{ds}}) \cdot V_{\text{pulse}}}{C_1 (C_2 + C_{\text{ds}}) + C_2 C_{\text{ds}}} \tag{3.2}$$

Assuming $C_1 \gg C_{\text{ds}}$ and $C_2 \gg C_{\text{ds}}$ equation (3.2) reduces to

$$V_{\text{gs,off}} = \frac{C_{\text{ds}} \cdot V_{\text{pulse}}}{C_1} \tag{3.3}$$

We see from (3.3) that C_1 can be used to independently set the maximum allowable voltage on the gate when the transistor is off and C_2 can independently set the gate voltage to turn on the transistor.

3.1.3. Shape of Transmit Waveform

Simulation of the switch shows it functions correctly. The switch is able to pass or block an arbitrary waveform of different frequencies. Figures 3.7 and 3.8 show a square transmit pulse of four periods, with a frequency of 2 MHz and 20 MHz respectively.

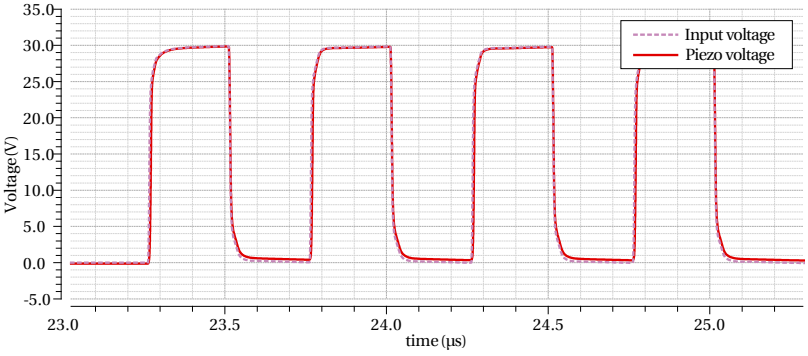


Figure 3.7: Transmit waveform for 2 MHz square wave pulses

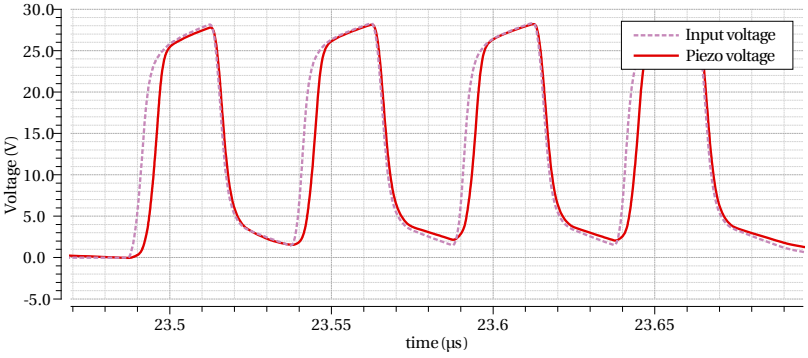


Figure 3.8: Transmit waveform for 20 MHz square wave pulses

In the simulation results a small distortion is visible at the start of the waveforms. This deformation is caused by the transmit switch that only turns on above about 8 V.

When an accurate waveform is required, the transmit waveform can be given a DC offset and a lower maximum amplitude. The DC offset ensures that the transmit switch will not turn off. An example of a 20 MHz sine wave with DC offset is shown in Figure 3.9. The plot shows that the voltage at the piezo material follows the input voltage very well. Moreover, the transmission line delay caused by the coaxial cable can be clearly seen as a phase shift between the system voltage and ASIC input voltage.

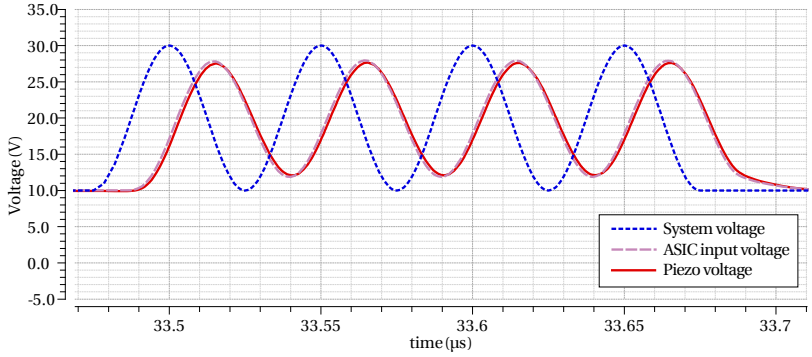


Figure 3.9: Transmit waveform for 20 MHz (offset) sine wave pulses

3.1.4. Transmit Mode Power Consumption

In transmit mode the power consumption is significantly larger than during the receive mode, due to the higher voltage. To reduce the power dissipation most of the receive circuitry is off during transmit. The result of this is that the chip is able to be subject to a 30 V DC voltage without overheating. This is not only a safety feature to prevent the chip from dying when a wrong transmit sequence is applied, but also to reduce heating of the chip in normal operation.

The current consumption for long transmit pulses (and DC voltage) is 180 μA, limiting the power dissipation to at most 5.4 mW. The remaining current is needed for the voltage clamp, start-up circuit and bias sources, all discussed in the upcoming sections.

Figure 3.10 shows a 20 MHz transmit waveform and the corresponding dynamic current at the system side.

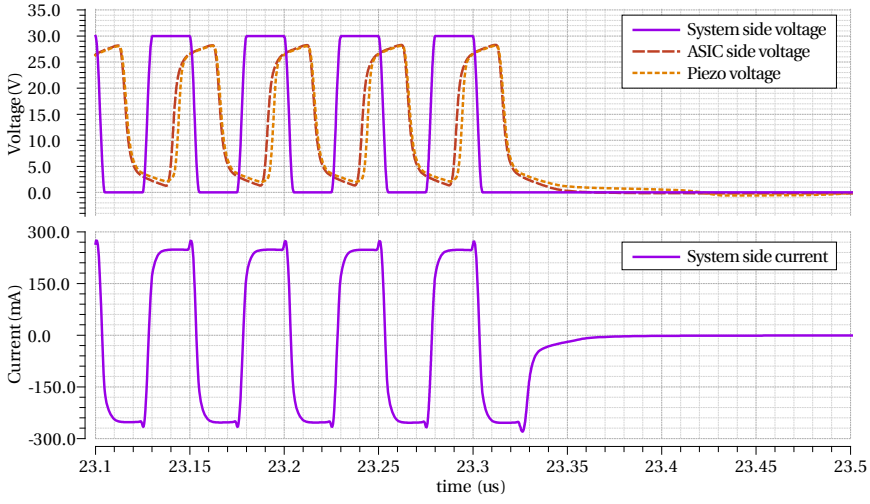


Figure 3.10: System side voltage and current driving the ASIC and one enabled piezo element

The dynamic current seems high at first glance. One might wonder what is causing such a high current. A closer inspection of the cable capacitance and the transmit pulse frequency shows that the current is to be expected. The current needed to charge a capacitor in a given time is defined by:

$$I = C\frac{dV}{dt} \tag{3.4}$$

Writing down the cable capacitance of 220 pF, a very similar value of 264 mA is calculated for only the cable capacitance:

$$I = 220\,\text{pF}\left(\frac{30\,\text{V}}{25\,\text{ns}}\right)$$
$$I = 264\,\text{mA}$$

In reality the circuit capacitance will add to the cable capacitance making the dynamic current even higher. As most of the dynamic power is dissipated at the system side, the ASIC will not heat up significantly.

3.1.5. Remembering the Switch State

A capacitor at the gate of the NMOS transistor is used as a memory element to keep the transmit switch enabled or disabled. A low-V_T transistor (Q_1) is used to latch the value of the enable signal onto the memory element. The low threshold device ensures that the gate voltage of Q_n is high enough to enable the transistor. A normal (thick oxide) transistor would barely enable the high voltage transistor due to its high threshold voltage.

As the high voltage transistors have significant parasitics, the memory capacitor needs to be sized large enough so capacitive coupling will not cause the switch to turn on. Figure 3.11 shows the memory capacitor and the parasitic gate-drain capacitance (C_{gd}) that causes the memory capacitor to be pulled up during transmit when Q_n is off.

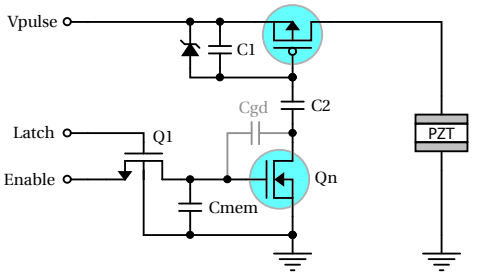


Figure 3.11: Transmit switch with memory element

A simulation of the effect of parasitic coupling to the memory capacitor is shown in Figure 3.12. Even with the simulated capacitance of 300 fF, significant peaks can be noticed.

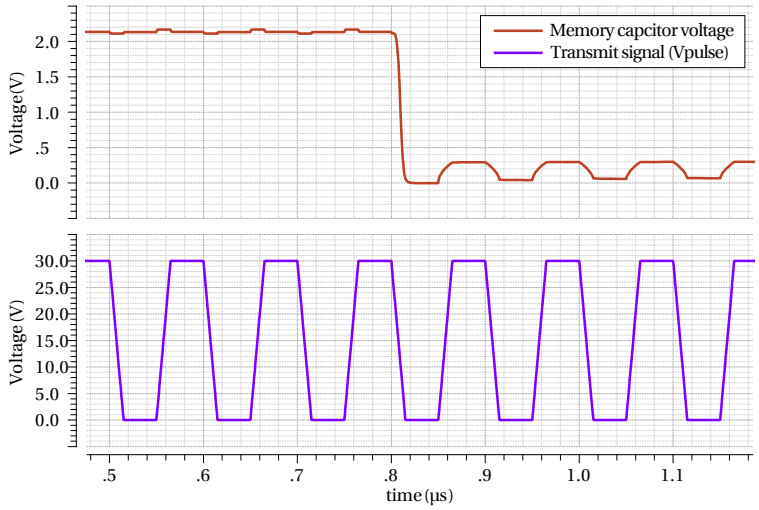


Figure 3.12: Voltage spikes caused by parasitic coupling to the memory capacitor

The amplitude of the peaks is about 300 mV, which is low enough to not turn on the transistor. This i confirmed in Figure 3.13 where the drain current of the mosfet is shown. Below 500 mV the mosfet is off and only shows a leakage current.

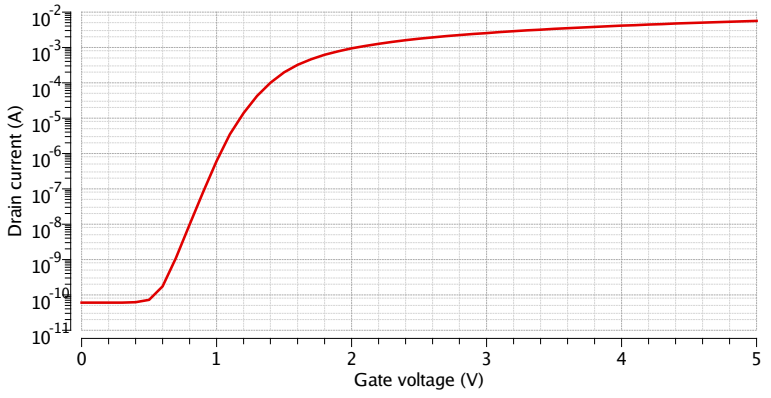
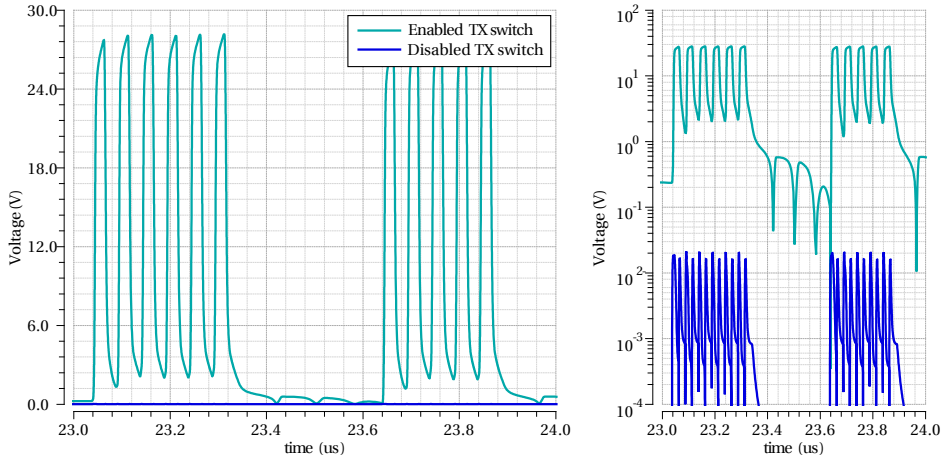


Figure 3.13: Drain current for a minimum size high voltage NMOS (GA) device

3.1.6. Performance

The switch behaves as expected when simulated for the completed ASIC, as shown in Figure 3.14a. The parasitic capacitance of the transmit switch causes a small peak to be coupled onto the disabled piezo element. The peak voltage of a disabled element is 22 mV, when a transmit pulse of 30 V is applied to the ASIC. This amplitude is about 60 dB below the voltage on the enabled piezo elements, as visible in the logarithmic plot of Figure 3.14b.



(a) Linear **(b)** Logarithmic

Figure 3.14: Piezo voltage for enabled and disabled transmit switch

Each switch has its own memory element, making it possible to turn on multiple switches at once. A chip-level simulation of multiple switches operating at the same time was performed to see the degradation in performance. The results in Figure 3.15 show that not only multiple switches can operate at the same time, even with 48 channels enabled a reasonable quality waveform can be generated.

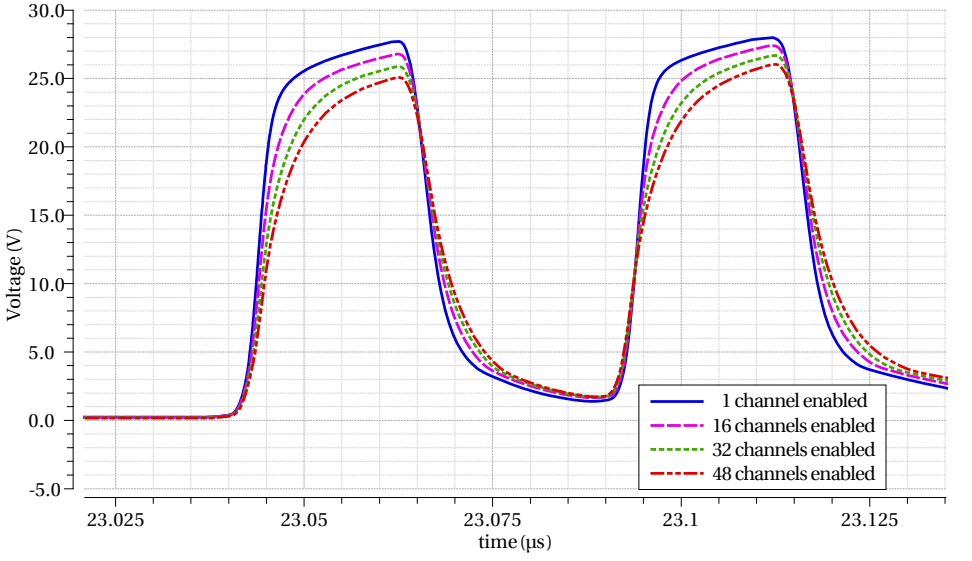


Figure 3.15: Piezo voltage for multiple transmit switches enabled simultaneously

As visible in Figure 3.15, the rise time degrades when many switches are enabled. This is caused by the higher capacitive load of the combined enabled channels, while the same

cable resistance is present. The load in the simulation is 2.5 pF per channel (1.2 pF for the piezo material and 1.3 pF for the combined parasitics of the receive protection, ESD diode and transmit switch).

3.2. Low Noise Amplifier

As discussed in Chapter 2, the LNA needs to amplify a current. Moreover a feedback network has been chosen to set an accurate gain for the amplifier. However, the gain has not yet been defined. To determine the gain of the amplifier we look at the implementation of the system side and the noise associated with it. The TIA used at the system side will have an input referred noise that should not dominate the output signal of the system. A comparison of low noise amplifiers (Appendix B) with a bandwidth well higher than 20 MHz shows that commercial opamps have an input referred noise as low as 1 nV/$\sqrt{\text{Hz}}$, but opamps with higher operating voltages are usually around 1.6 nV/$\sqrt{\text{Hz}}$. To have several options to choose from a safe value of 2.0 nV/$\sqrt{\text{Hz}}$ input referred noise is included for the system side TIA, in the simulations in this section.

To refer the TIA input noise voltage (V_{n}) back to the signal current ($I_{\text{n,eq}}$), the noise voltage source is shifted through the input node into the feedback network and in series with R_{m}. Then it is transformed into a current source parallel to R_{m}, and one parallel to R_1. With this method a total input noise current of 47 pA/$\sqrt{\text{Hz}}$, including the noise contribution of the feedback and matching resistor, can be derived.

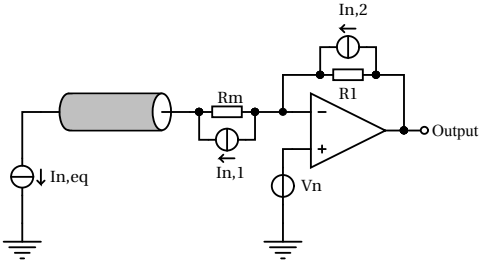


Figure 3.16: Noise sources at the system side

To have a noise level below the noise floor of the current LNA (< 0.8 pA/$\sqrt{\text{Hz}}$), a gain of more than 50× is needed. The design goal for the current gain of the LNA is set to 200×, to have a good noise figure for the system side amplifier.

3.2.1. Transistor-Level Design

The low noise amplifier is implemented as a three-stage amplifier, of which the circuit is shown in Figure 3.17.

For the input stage an NMOS transistor is used. By using the NMOS transistor, the input bias voltage can be at a lower voltage, reducing the amplitude of the step on the piezo material caused by the feedback network of the LNA when it switches on.

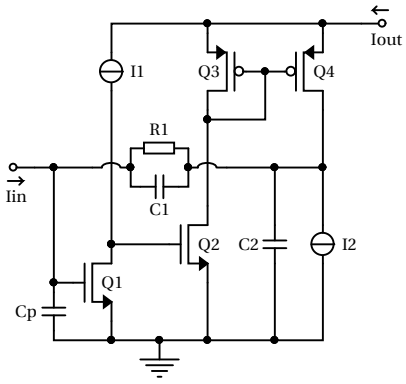


Figure 3.17: Transistor implementation of the current amplifier

Capacitor C_2 of the feedback network is preferably connected to ground with one plate (for layout purpose), defining that the output stage should be a PMOS transistor. The second stage is needed to invert the signal.

To understand how the output current is embedded in the supply current, we take a look at the small signal current in the system. Figure 3.18 shows the amplifier, power supply and the coaxial cable. The small signal current will flow trough the output stage and via the capacitor through the cable to the system side, thus it can indeed be measured at the system side.

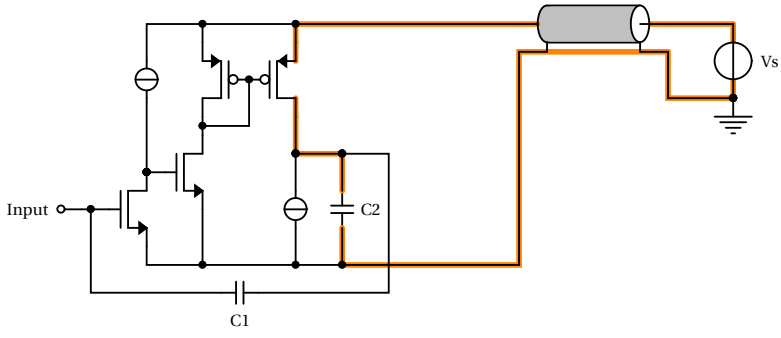


Figure 3.18: Small signal current loop through the output stage

Now imagine that an N-MOS output stage would be used. It would sit in parallel with capacitor C_2, and the current source would supply a DC current to it. The amplifier would still work, and an output voltage swing on the capacitor would be created, however, the small signal current would flow through the N-MOS transistor directly back into the capacitor. No signal current would be embedded in the supply current, making the output signal invisible at the system side.

3.2.2. Gain and Output Swing

In ultrasound imaging a large dynamic range is needed. A common method to increase the dynamic range is to add time gain compensation (TGC) [33]. For this amplifier three programmable gain settings are created, in steps of 6 dB.

The voltage swing at the output of the amplifier is dependent on the size of the output capacitor (C_2). Making the capacitor bigger results in a smaller voltage amplitude in the feedback network and a higher dynamic range. However, as the feedback capacitor loads the amplifier, it can not be made extremely large. Moreover when making the gain programmable it is important that not the output capacitor (C_2) should be programmable. Although it would change the amplifier gain, it would also change the maximum amplitude before clipping distortion occurs. In that case the gain switching doesn't create any benefit. The correct way to change the gain is to change the value of the feedback capacitor (C_1). A bigger C_1 will lower the gain of the amplifier and reduce the swing at the output capacitor, thus increasing the dynamic range.

The implementation of the gain switches is shown in Figure 3.19. Due to the switch

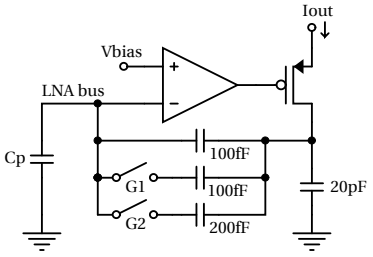


Figure 3.19: LNA with gain switches

choice, four gain settings are available: The three intended settings (200×, 100× and 50×) and one extra settings (68×) for the switch combination that creates a 300 fF feedback capacitor.

The signal transfer of the three intended gain settings is shown in Figure 3.20. It shows a flat spectrum (less than −3 dB variation) for the bandwidth of interest.

A maximum gain of 200 × (46 dB) has been defined, however the AC-simulations shown in figure 3.20 show a higher gain of 47.5 dB. The higher gain is caused by the signal current in the second stage. As the load of the second stage is not a current source but a diode connected transistor, the signal current of the second stage will also be visible in the supply current and hence in the output current of the LNA.

3.2.3. Stability

The stability of the amplifier is dependent on the gain settings. A decrease in gain, causes the phase margin to decrease as well. Normally amplifiers are designed to have a minimum phase margin of 45° [34]. To ensure a high-enough phase margin for the lowest gain setting, two transistors have been added, shown in Figure 3.21. When transistor Q_6 is on, the amplifier is exactly as discussed in the previous sections. Turning off Q_6

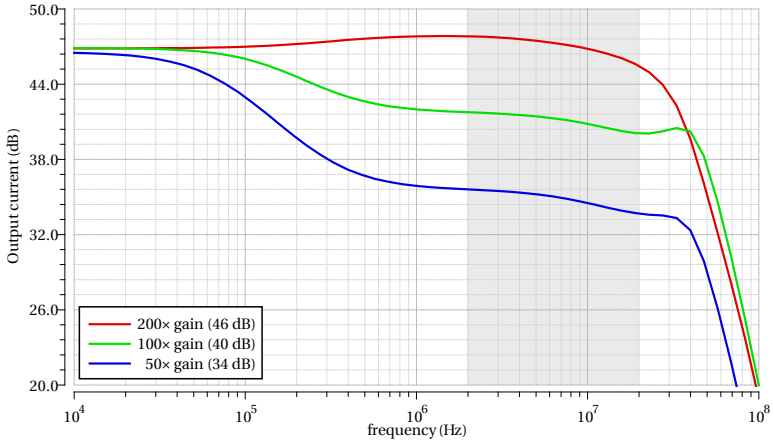


Figure 3.20: Amplifier transfer function for the 3 gain settings

reduces the gain of the second stage, increasing the phase margin. By switching Q_6 together with the feedback capacitor for the lowest gain setting, the amplifier operates with a phase margin larger than 45° for all gain settings.

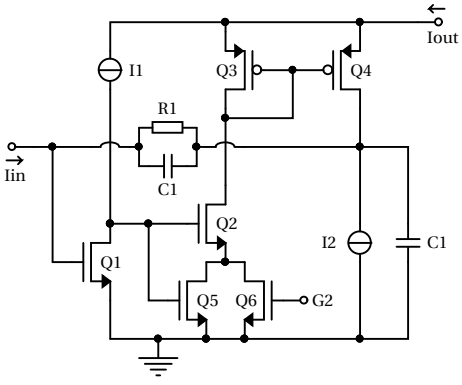


Figure 3.21: Gain reduction switch to make the amplifier stable in low gain settings

As discussed in Chapter 2 the stability is not negatively influenced by the input parasitic capacitor. To show the effect of the piezo capacitance on the phase margin, a simulation is performed as shown in Figure 3.22. Indeed the input capacitance doesn't reduce the phase margin.

The same holds for increasing cable capacitance, as it is not loading the amplifier the stability is not negatively influenced by this capacitance.

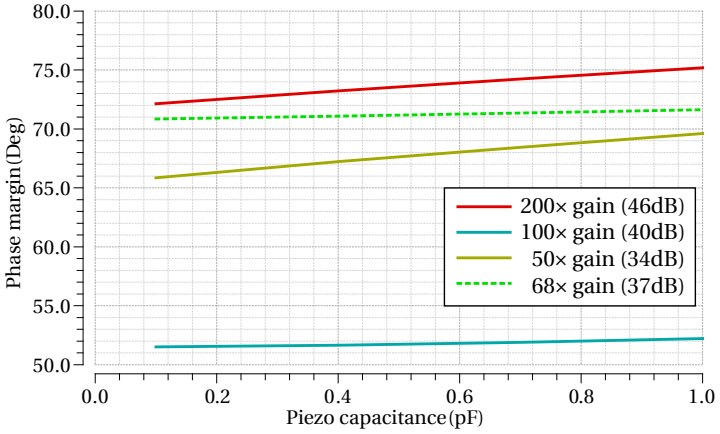


Figure 3.22: Phase margin for the different gain settings and varying piezo capacitance

3.2.4. Parasitic Feedback

The parasitic capacitance between the output node and input of the amplifier plays a significant role in the stability, because it forms a feedback loop. The feedback capacitance is shown in Figure 3.23 as C_p. When designing the layout of the ASIC it is important to keep this capacitance low to ensure correct operation of the amplifier.

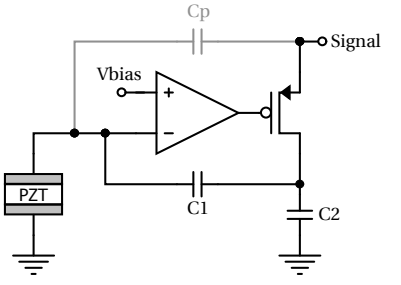


Figure 3.23: Parasitic feedback capacitor, deteriorating the phase margin

A parasitic extraction for a 10 µm trace located directly under the centre of a piezo element pad is done, showing a capacitance of 16 fF. Figure 3.24 shows that the maximum tolerable capacitance is 47.5 fF (for 45 degree stability). The 16 fF can be considered a safe distance from the critical point. Especially because only one channel can be active at a time and the traces of the LNA bus are only 280 nm wide, much smaller than the extracted 10 µm.

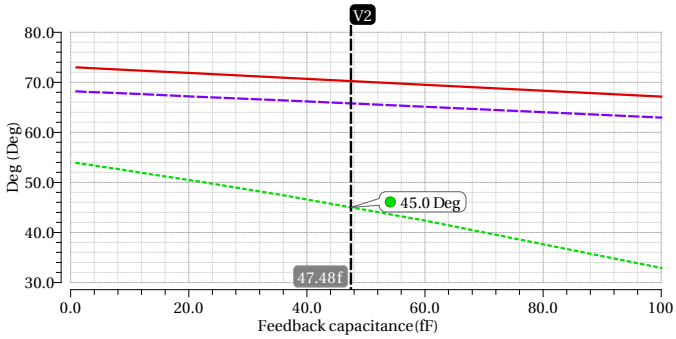


Figure 3.24: Phase margin for increasing parasitic feedback capacitor

3.2.5. Bandwidth

The bandwidth of the amplifier should be more than 20 MHz. Figure 3.25 shows that the amplifier fulfils this requirement. Although the amplifier itself has a bandwidth of about 30 MHz the 2 m cable limits the −3 dB frequency to just over 20 MHz, due to the attenuation losses.

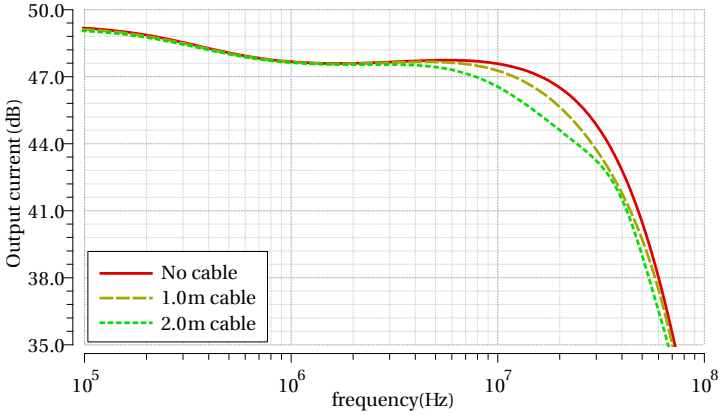


Figure 3.25: Amplifier transfer function for various cable lengths

This also holds for the other gain settings, because the attenuation losses don't change with the gain setting.

3.2.6. Reset Phase

When starting up the ASIC, the LNA needs to be at the right biasing conditions. One way to do this is by having a DC signal from the output to the input, by adding a resistive feedback. The resistor would however add a considerable amount of noise. When increasing the resistor value the noise decreases but the settling time increases well above the specified start-up time.

To get the best of both, a low value resistor is chosen for which the amplifier is still stable. This resistor is connected using a switch for a short time after reset and is then disconnected. In operation the amplifier only has capacitive feedback and a very high valued resistor (5 MΩ) to compensate for drift due to leakage at the input node.

The biasing source generates a 10 µA reference current that is amplified in a current mirror to get the input branch current of around 500 µA. Because of the amplification, the noise in the current mirror is also amplified and visible in the output signal of the amplifier. To remove the noise contribution of the reference current the bias voltage in the mirror is sampled on a capacitor during the reset phase. After the reset phase the reference current is disconnected and the amplifier is biased by the capacitor voltage.

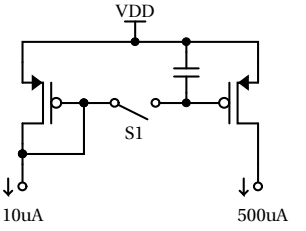


Figure 3.26: Sampling to reduce amplifier noise

In the lower half of the bandwidth of interest, the output stage also shows a considerable noise contribution. However, due to parasitics this can not be solved in the same way. The parasitic drain-gate capacitance of the output current source (C_p) would create a local (unstable) feedback loop, as shown in Figure 3.27. Switch S_2 is therefore not implemented.

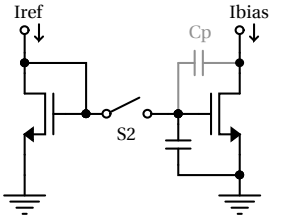


Figure 3.27: Unwanted feedback loop in output stage biasing

Because the noise contribution is not very significant, the reference current was increased and the sampling capacitor was placed at the high side current mirror. For frequencies above 5 MHz the output stage does not contribute a significant amount of noise, for lower frequencies it is visible. However, the higher contribution is not a problem as the total noise is still lower than the noise of piezo elements. Moreover, for a probe with the given dimensions one would rarely use frequencies that low.

3.2.7. Noise

In a good amplifier design the first stage should dominate the total noise of the amplifier [22]. However, several parts of the circuit will also generate a considerable amount of noise, caused by the fact that the power supply and signal are combined.

For the input clamping transistor we find a trade-off between the noise generated by the on-resistance and the increased noise gain caused by the capacitance of this transistor. One could make the transistor very large, to have a small on-resistance, but that readily creates a large capacitance. An optimum clamp size exists that minimizes the total input referred noise, shown in Figure 3.28.

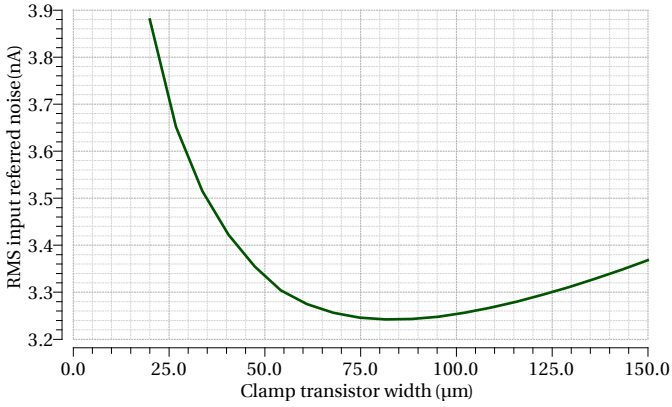


Figure 3.28: Input referred noise (at 20 MHz) for increasing input protection clamp size

The dominating noise source of the final design is the input stage. For low frequencies however, as discussed in Section 3.2.6, the current source noise can not be completely removed without spending significantly more power. Figure 3.29 shows the main noise contributors in the design (referred to the output of the system side TIA).

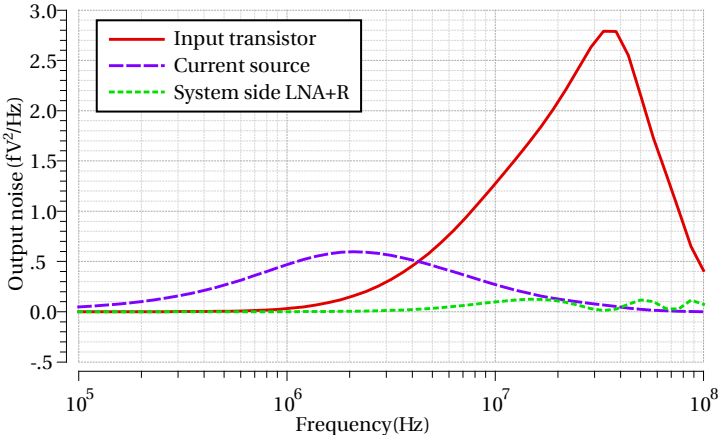


Figure 3.29: Noise contribution of input stage, output stage and system side

Referring the total system noise (ASIC and system side) back to the input of the amplifier, the plot of Figure 3.30 is obtained. The noise floor of the system is low enough to make a 70×70 µm element noise dominant.

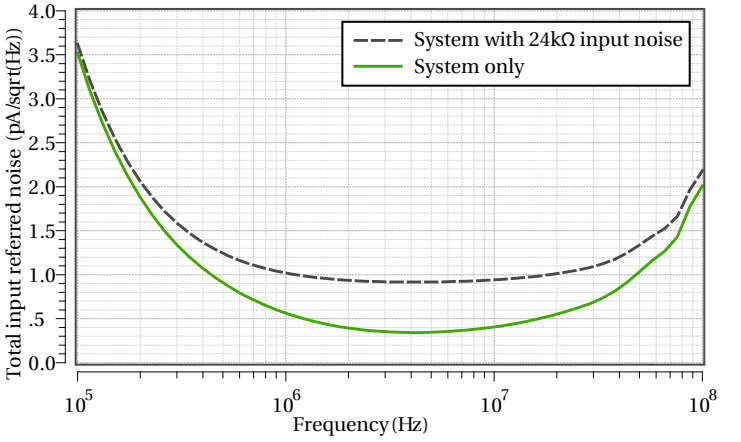


Figure 3.30: Input referred noise of the amplifier

3.2.8. Input Parasitic Capacitance

Input parasitics play an important role in the noise specification of the LNA. To reduce the input capacitance the biggest contributors have been analysed. For reference the components connected to the input of the LNA in receive mode are shown in Figure 3.31.

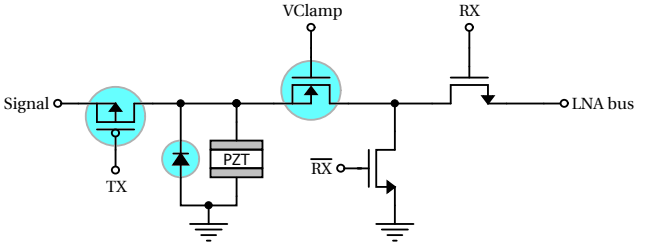
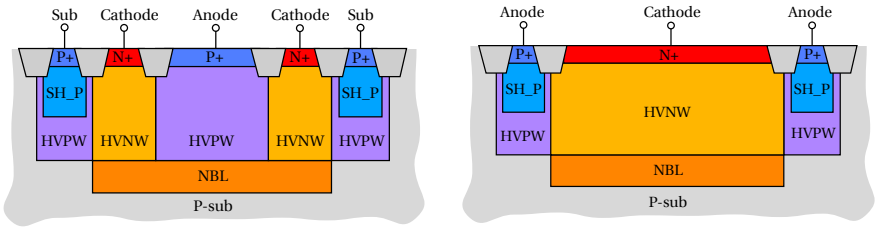


Figure 3.31: Devices connected to the input of the LNA

One important contributor to the parasitic capacitance is the ESD protection diode. Previous designs of the group have used a junction isolated diode (Figure 3.32a left). Simulation shows that this diode has capacitance of 1.27 pF at the amplifier biasing point. A look at the other high voltage diodes in the technology shows that the capacitance can be reduced a lot. As in this design the anode of the diode can be at the same potential as the substrate a much simpler diode layout can be used, because no junction isolation is needed between the anode and substrate (shown in Figure 3.32b). The new diode has a simulated capacitance of 0.048 pF, lowering the capacitance by 25 times.



(a) Isolated diode **(b)** Non-isolated diode

Figure 3.32: Vertical structure of isolated and non-isolated high voltage diode

3

3.2.9. Distortion and Dynamic Range

Harmonic distortion is not an important specification in this particular application, as the probe is intended to be used at a single frequency. This means that all harmonics can be filtered out. It is however interesting to look at clipping distortion to get an impression of the dynamic range of the amplifier.

Transient simulations (including transient noise) were done to find the dynamic range of the amplifier. Figure 3.33 shows the RMS output voltage of the system side TIA for different gain settings. The noise floor of the LNA is visible for low input currents. For high input currents the output stage of the LNA starts to clip.

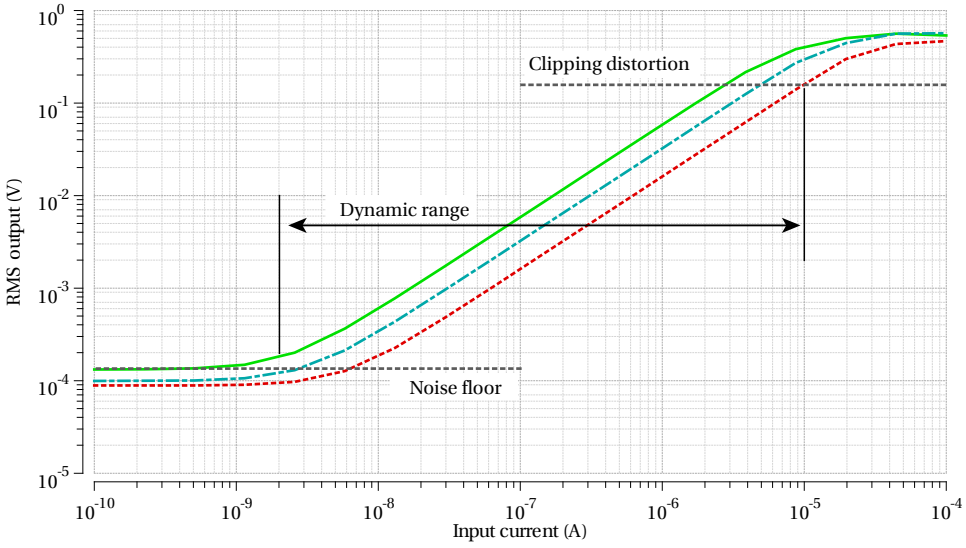


Figure 3.33: Dynamic range plot obtained from transient noise simulations

The plot in Figure 3.33 shows that the amplifier has a dynamic range of 74 dB (including TGC gain). The upper limit is shown for a signal compression of 1 dB caused by clipping distortion.

3.2.10. Entire LNA Circuit

The entire circuit of the amplifier discussed in this section is shown in Figure 3.34.

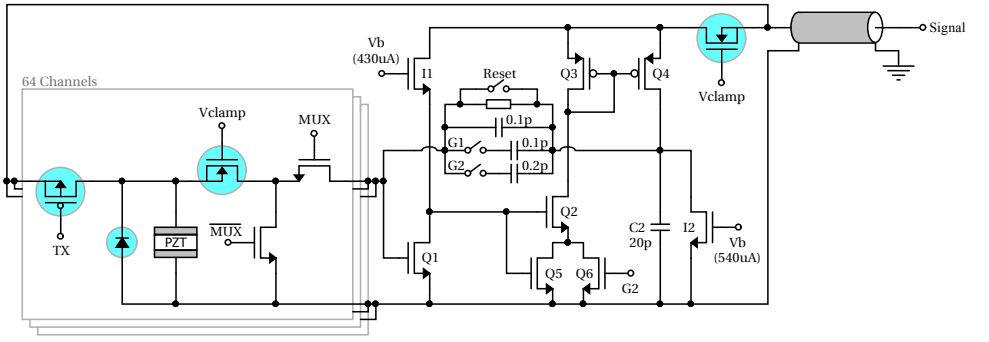


Figure 3.34: Transistor implementation of the LNA

The amplifier input stage consumes 430 µA to reach the noise specification. The second stage consumes 90 µA, mainly needed to be able to drive the large output transistor Q_4. The output stage consumes 540 µA, to reach the bandwidth of over 20 MHz for the output capacitor of 20 pF.

Two gain switches (G_1 and G_2) have been added to increase the dynamic range of the amplifier. Lastly a configuration bit has been added (not shown) to reduce the current consumed in the last stage. When enabled this bit reduces the bandwidth to 19 MHz, but also cuts down the dissipated power to 75 %.

3.3. Fabrication Test Mode

During the integration process to fabricate the piezo material onto the chip, several things can go wrong. To be able to know whether the piezo elements are properly connected to the bond pads, a test mode is considered.

The test mode should involve an easy test step that doesn't compromise the functionality of the chip and preferably also doesn't make the chip more complex. By measuring the capacitance of the piezo material, most failure modes can be detected. The failure modes are illustrated in figure 3.35 and can be characterized as:

- *Bad connection*
  The piezo material is not or badly connected to the input of the amplifier. This can for example be caused by a gold ball that is not in contact with the conductive glue or because the ground foil is not properly connected to the piezo material.

- *Shorted elements*
  A short circuit can exist between two piezo elements, for example caused by the dicing kerf not being deep enough.

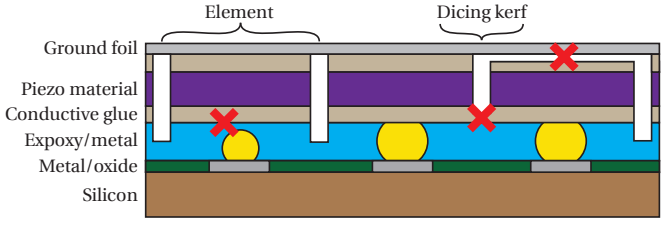


Figure 3.35: Possible failures during piezo-on-chip fabrication

In case of a bad connection the channel capacitance should be significantly lower than expected, when two elements are shorted the channel would have a much higher capacitance.

For the circuit implementation several options were considered, amongst which injecting an external signal. However, ideally the ASIC should be able to self-diagnose without the use of an external signal, as the bond wires are hard (or even impossible) to reach when the piezo elements are placed.

To create a test mode with as few extra components as possible, the LNA is used without the feedback loop, essentially turning it into a comparator. Using the transmit switch a voltage can be sampled on the piezo capacitance. Sequentially a current sink slowly empties the capacitor until the comparator toggles. The time from start-up until the comparator toggles is a measure of the capacitor size.

Figure 3.36 shows the circuit used for the test mode. Q_1 is the transmit switch that is used to sample the voltage onto the piezo element. The NMOS voltage limiter Q_2 is present for the receive mode LNA circuit. A pair of reference capacitors is added at the

input. These capacitors can be used to calculate the absolute value of the piezo material capacitance.

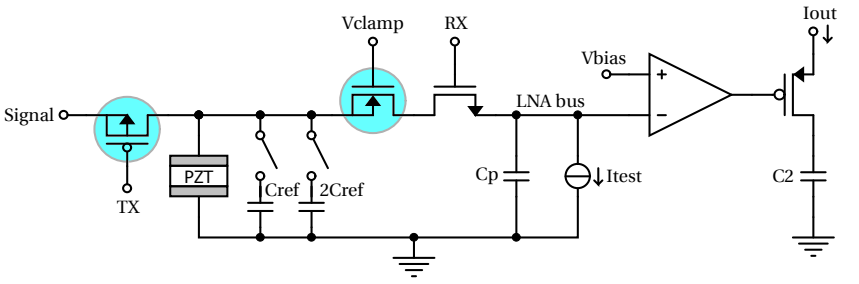


Figure 3.36: Input circuit used for the test mode

The size of the current sink (I_{test}) is chosen such that the delay is about 2 µs for a 1 pF input capacitance.

The waveforms associated with the test mode circuit are shown in Figure 3.37. The first part of the discharge curve shows a clear dependence on the capacitor size. However, as soon as the piezo voltage is below the LNA bus voltage ($V_{clamp} - V_T$), it seems almost independent to the piezo capacitor size. This is caused by the fact that the parasitic capacitors at the LNA bus are much larger than one single element capacitance.

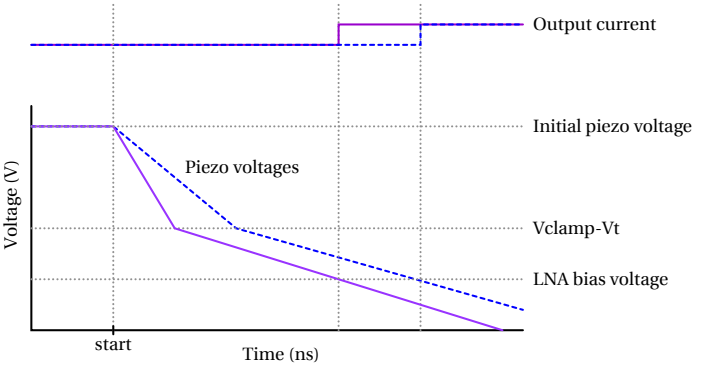


Figure 3.37: Ideal waveform of the test mode for different piezo capacitances

To generate the initial voltage on the piezo material the circuit is set the transmit at the test channel. A short transmit pulse of for example 10 V is used to charge the piezo and without pulling down to zero the signal is changed to the test voltage of 2 V-5 V. After the startup delay the chip automatically switches to receive mode and turns of the transmit switch, keeping the piezo material charged.

When the chip switches, the receive multiplexer connects to the input of the LNA, causing the charge on the piezo capacitance to be shared with the LNA bus capacitance. In Figure 3.38 this is visible in the piezo voltage as a step down, because the bias voltage of the LNA input bus is lower than the voltage on the piezo capacitance.

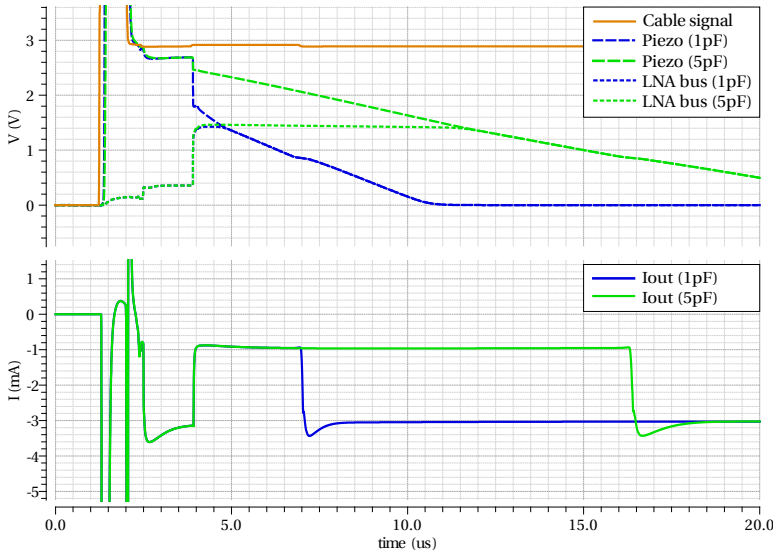


Figure 3.38: Transient simulation of test mode for different input capacitances

A simulation of the time until the comparator toggles for varying element capacitances was performed, plotted in Figure 3.39. The simulation clearly shows that the method has a good linear behaviour. The offset found for zero input capacitance is 0.8 µs after the reset phase, caused by the parasitic capacitance of the protection diode and LNA bus.

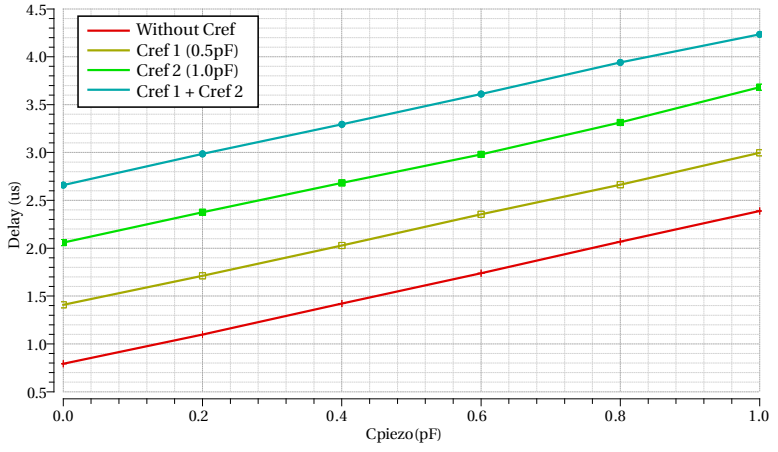


Figure 3.39: Comparator toggle delay for various piezo capacitances

The post-layout simulation shows a sensitivity of 629 fF/µs. A simple counter can be implemented on the system side FPGA to function as a TDC to digitise the delay. When a 100 MHz clock is used, an LSB of about 6 fF can be accomplished.

3.4. Communication

Any data that has to be transferred to the chip should be transferred by adding a signal on top of the supply voltage, as discussed in Chapter 2. A self clocking type of data should be used, because no extra cable is available to provide the clock signal. Two common ways of encoding data to make it self clocking are Manchester encoding [35] and pulse width encoding, both shown in Figure 3.40.

In Manchester encoding the signal is encoded in such a way that every bit has a transition halfway the period. The value of the bit is defined by starting the period with a high or a low signal. A Manchester encoded bit-stream is shown in Figure 3.40. For pulse width encoding a bit always starts with a rising edge, but the value of the bit is defined by the pulse width of the signal. A short pulse corresponds to a zero, a long pulse corresponds to a one.

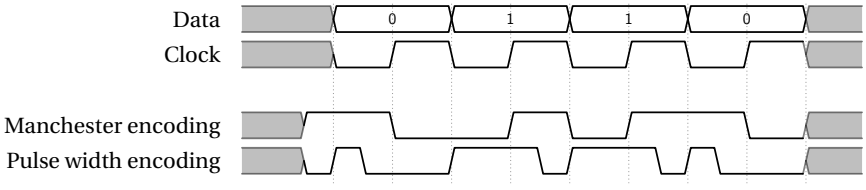


Figure 3.40: Encoding schemes for self clocking data

Manchester encoding has no DC component, which can be very useful when the signal needs to be amplified. In the pulse length encoding scheme the average signal level depends on the data that is being transmitted. This means that the bias voltage of an amplifier would (potentially) shift when many of the same binary values are transmitted. On the other hand, the clock can be very easily recovered from the pulse width modulation scheme. Moreover in the case of Manchester encoding the circuit needs to know the start of the code as there are two possible moments in the period where the signal can change: halfway the period and on the change of data at the start of the period.

The scheme chosen for communication with the chip is pulse width encoding. Because of the non-ambiguous bit transitions a reliable transmission can be made with a relatively simple circuit.

3.4.1. Data Recovery

The data is sent as a small signal on top of the power supply. To recover the data, the AC signal is amplified and then converted to a binary signal using a schmitt-trigger, as shown in Figure 3.41.

The chosen implementation uses a reference voltage of half the supply voltage for the amplifier. As the schmitt-trigger is designed to be symmetric around the supply as well, it can readily be used to recover the data. To make the circuit insensitive to the DC level, a short time constant between the feedback and coupling capacitor is chosen, in order to create a pseudo differentiator. A rising edge will cause a positive peak (relative to

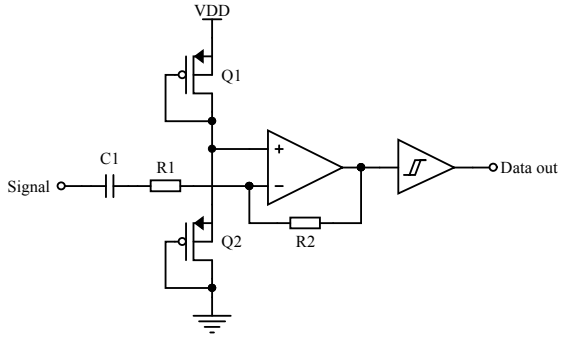


Figure 3.41: Schematic of the data recovery circuit

the bias point) toggling the schmitt-trigger to a low output, as the amplifier inverts the signal. A falling edge will cause a negative peak, toggling the schmitt-trigger to a high output. The input signal, differentiated signal and the output of the schmitt-trigger are shown in Figure 3.42.

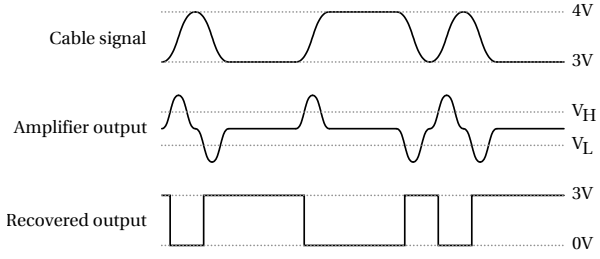


Figure 3.42: Waveforms associated with data recovery

From the recovered bit-stream a clock should be generated. The rising edge of the clock signal should take place half a period after any rising edge in the bit-stream. To detect the rising edge, the clock input of a flip-flop is used. The half-period delay is implemented in hardware by slowly emptying a capacitor using a current source. A rising edge in the bit-stream causes the capacitor to be quickly recharged. The circuit is shown in Figure 3.43.

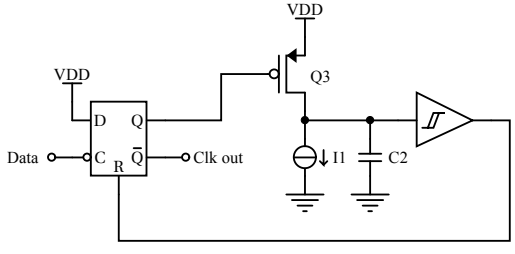


Figure 3.43: Schematic of the clock recovery circuit

3.4.2. Schmitt-trigger

A simple CMOS schmitt-trigger [36] was designed, because it didn't exist in the library of TSMC. The schmitt-trigger is used in the data recovery circuit to convert the possibly noisy analog signal to a binary signal. It is also used at several places on the ASIC in combination with a capacitor and current source, where a long time-delay is needed. The schematic of the implemented schmitt-trigger is shown in figure 3.44.

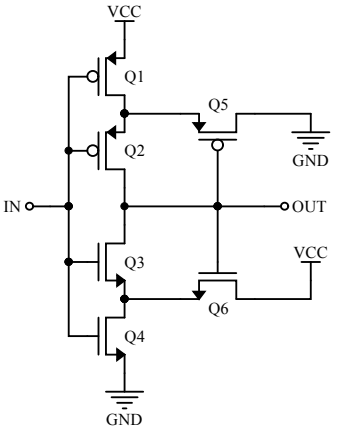


Figure 3.44: Schematic of the CMOS schmitt-trigger

The trip points are set to be symmetric around half the supply voltage for the typical process corner. Simulations show that the trip points can shift slightly for the extreme corners, as visible in Figure 3.45.

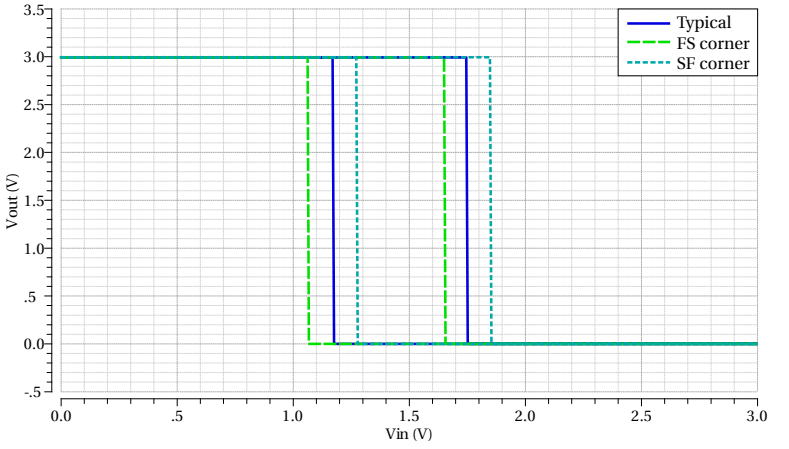


Figure 3.45: Input-output relation of the designed schmitt trigger

3.4.3. Receive Multiplexer

For the receive chain, a 6 to 64 bit demultiplexer is used, distributed as shown in Figure 3.46. Each input code from the shift register sets one output of the demultiplexer high and keeps the other outputs at a low level (1-hot encoding). The selected high output enables one of the 64 channels as the receive channel.

The shift register of 6 bits is split in half. The first 3 bits are demultiplexed into 8 bits driving four quadrants on the chip. The other 3 bits are driving the enabled local demultiplexer. This reduces the global wiring to only 5 wires per quadrant instead of 16.

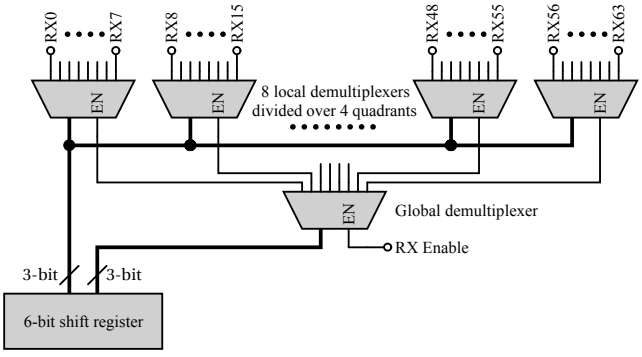


Figure 3.46: Receive channel selection 1-hot encoder distribution

Every piezo element has a switch that can connect the element to the input of the LNA, driven by the 1-hot encoder. The complete input circuit of one channel is shown in Figure 3.47. When the transmit switch is enabled, the NOR-gate makes sure that the pull-down transistor Q_4 is not turned on. In receive mode the 1-hot encoder selects a single input channel by making the node labelled RX high. This turns on transistor Q_5 to pass the signal from the piezo element to the LNA bus (the input node of the LNA, shared by all 64 channels). Only when the piezo element is not used for transmit or receive, the piezo element will be shorted to ground by Q_4.

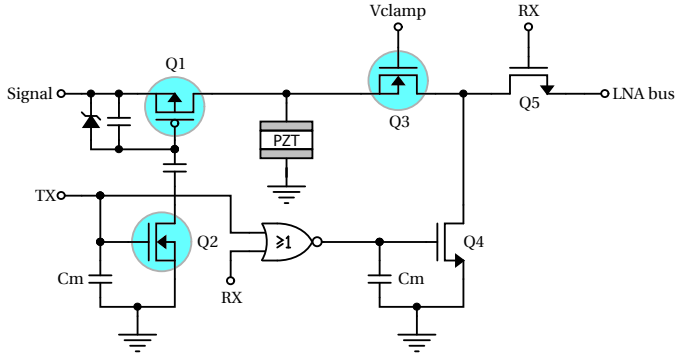


Figure 3.47: Transmit and receive channel selection switches

3.4.4. Memory

To remember the selected receive channel and configuration settings a D-RAM (dynamic random access memory) circuit is implemented. A low-V_t pass transistor is used to latch the data into a holding capacitor of 200 fF. The size of this capacitor and the leakage through the pass transistor determine the data retention time. By making the pass transistor small, the off-leakage is minimized. The simulated data retention including the leakage is 37 ms, which is plenty because the pulse repetition rate should be much faster to get a reasonable frame rate.

The circuit used for the memory cell is shown in Figure 3.48.

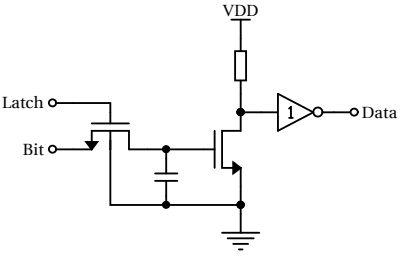


Figure 3.48: Schematic of memory cell

A buffer consisting of an N-MOS transistor and load resistor are used to make the static power consumption of the buffer well defined. A normal buffer would consume a lot more power, because the voltage on the capacitor droops over time, not strictly defining a high or low logic state at the input of the buffer. As a result, both the N-MOS and the P-MOS transistor would be on, causing a high static current.

3.4.5. Latching the Data

While reading in new data, it is preferred to not have logic unnecessary switching: To keep a good signal integrity but also to keep the power consumption low. To achieve this, circuitry has been added that latches the data only when no new data is transferred. To recognize the end of the data transmission, the clock activity is checked. When the clock is not active, the end of transmission is reached and the data can be latched into the memory.

The circuit that enables the latches is shown in Figure 3.49. A 5-bit counter counts the clock edges to detect that at least 16 bits are clocked in. This is done to prevent any spikes on the cable during start-up or switching, from latching incomplete data into the registers. When enough data has been clocked in, and a delay of more than 2 clock periods has passed (set by the current source and capacitor), the circuit will latch the data to the memory.

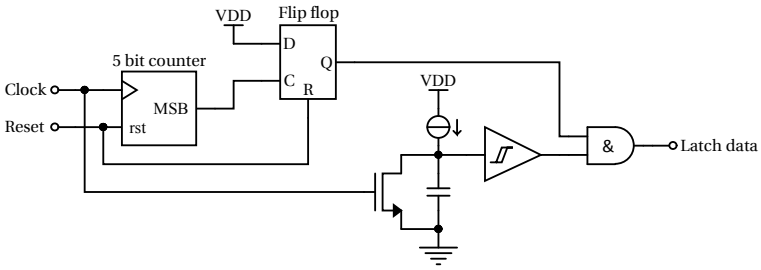


Figure 3.49: End of transmission detection circuit

The recovered data and clock signal drive three 8-bit shift registers and 64 single flip-flops for the transmit switches, as shown in Figure 3.50. The latch signal controls the pass transistor to the capacitors of the memory, at the moment set by the end-of-transmission detection circuit. The block diagram also shows a CRC block, which will be discussed in the following section.

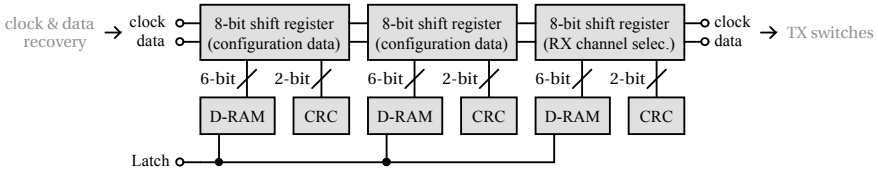


Figure 3.50: Block diagram of the shift registers and memory elements

3.4.6. Bit Error Checking

In the single cable operation it is valuable to know the quality of the data transfer to the chip. To give feedback about the quality of the data transmission an error check is built in that changes the quiescent current of the chip when an incorrect transmission is detected.

Errors in the transmission are detected by implementing a cyclic redundancy check (CRC) for the three 8-bit shift-registers (configuration and RX multiplexer registers). Every byte contains 6 data bits and two bits with a value calculated based on the 6-bits, using a polynomial function. The CRC-circuit, shown in Figure 3.51, performs the same calculation and checks whether the value matches the received CRC bits (bit 6 and bit 7).

Calculation of the CRC using logic is usually done serially, with a linear feedback shift register [37]. In this case a parallel circuit is implemented, for convenience during simulation.

To make sure that no data (all zeroes) would also be seen as an incorrect transmission, the CRC bits are inverted, implemented by the two inverters for bit 6 and bit 7. This results in a correct transmission for the sequence “00000011”.

If the output of the CRC circuit matches the 2 received CRC bits, the circuit will have a normal supply current. When an error (discrepancy) is detected, the supply current is

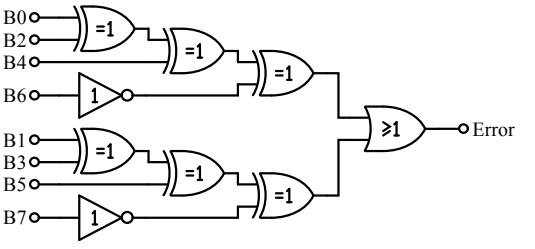


Figure 3.51: Logic implementation of 2-bit cyclic redundancy check

increased by switching on a pull-down resistor. The increase in current can be measured at the output of the system side TIA.

Figure 3.52 shows the increased supply current for a faulty data transmission (simulated by sending an incorrect CRC bit).

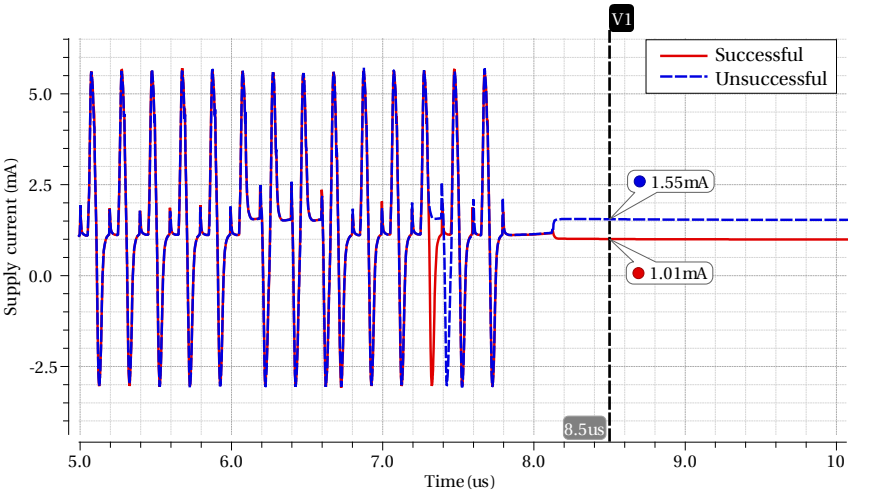


Figure 3.52: Supply current for successful and unsuccessful data transmission

3.5. Programmability

To facilitate testing, several configuration bits are added to the register. The first register contains the bits that enable the fabrication test mode and adjust the gain of the LNA. The second register includes the test mode reference capacitors, adjustment bits for the reset phase and a bit to enable the CRC feedback current.

Table 3.1: Configuration bits

Register	Bit	Function
Reg 1	0	-
Reg 1	1	-
Reg 1	2	Disable feedback (for use in test-mode)
Reg 1	3	Enable test-mode current source
Reg 1	4	Gain A (200 fF)
Reg 1	5	Gain B (100 fF)
Reg 2	0	Enable CRC
Reg 2	1	Low power enable (×0.75)
Reg 2	2	Shorten biasing reset time (× 0.5)
Reg 2	3	Shorten startup delay (× 0.5)
Reg 2	4	Enable test capacitor A (0.50 pF)
Reg 2	5	Enable test capacitor B (1.00 pF)

An overview of all registers in the chip is shown in Figure 3.53. The first shift register connected to the recovered clock and data signal, contains the values of byte 1. Thus, in a data transmission, the first bytes that are sent configure the transmit switches. If wanted, only the last three shift registers can be loaded (byte 1 to byte 3). This puts the chip in receive-only mode but lowers the data transmission time significantly.

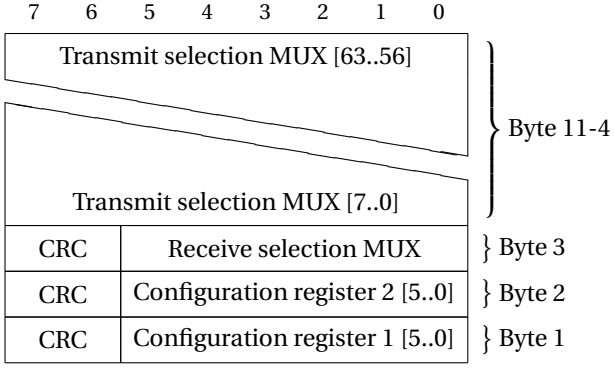


Figure 3.53: Chip registers, first transmitted is byte 11 bit 7

3.6. Additional Circuits

3.6.1. Clamping Voltage Source

As discussed in Chapter 2.4 a floating N-MOS transistor is used with a fixed voltage on the gate to protect the low voltage part of the ASIC. The gate-voltage that is needed for the clamp to properly protect the circuit is at least the sum of the LNA supply voltage and the gate-threshold of the transistor (3.5 V). The maximum allowable voltage at the source is 5 V. Therefore a stable voltage needs te be generated between 3.5 V and 5.5 V, preferably near to 5.5 V to allow for a lower on-resistance of the N-MOS transistor. However, no higher voltage than the operating voltage of the LNA is available during receive mode, so a way needs to be found to create a higher voltage than the receive voltage and to hold it long enough for a full receive cycle.

The implemented circuit uses a capacitor to store the voltage of the transmit pulses. Also here a floating N-MOS transistor is used to limit the maximum voltage sampled on the capacitor. A diode connected bipolar junction transistor (BJT) prevents the capacitor from draining. The complete circuit is shown in Figure 3.54.

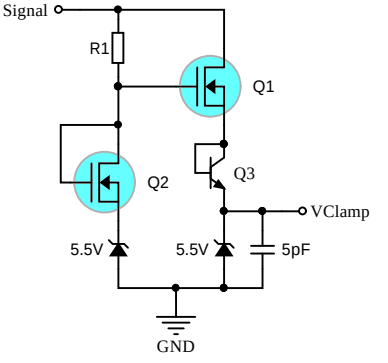


Figure 3.54: Schematic of the clamping voltage source

Some extra precautions were required to prevent over-voltage in the clamping circuit itself. The base-emitter voltage of the BJT can be too high, due to parasitic capacitances (mainly the drain-source capacitor of the NMOS transistor) on fast rise and fall times. An extra capacitor is added between the BJT collector and ground.

This circuit creates the need for an initial transmit pulse before the receive mode of the ASIC can work. After the initial pulse the capacitor only empties very slowly, as only the leakage of the zener diode draws current. Furthermore the capacitor is recharged every transmit cycle.

3.6.2. Biasing Source

A constant-g_m biasing circuit [38] was designed to provide the amplifier with a well defined biasing current. The circuit diagram of the biasing circuit is shown in Figure 3.55.

Because this topology is self-biasing, the circuit has two stable operating points, in on of them no reference current is generated. A start-up circuit is required to pull down the gates of the PMOS transistors to force the circuit in the correct operating point.

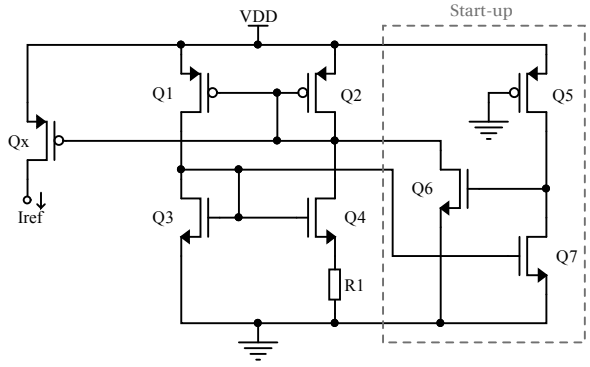


Figure 3.55: Schematic of the biasing circuit

Using the formulas in [38] a biasing source is designed for a reference current of 10 μA.

3.6.3. Receive Mode Start-up

In Chapter 2 the conditions for starting the receive mode were described. To check the conditions and start the receive mode at the correct moment, the circuit shown in Figure 3.56 was added. When a low voltage is supplied, high enough to enable Q_3, capacitor C_1 will charge with a constant rate, set by I_{ref}. As soon as the voltage rises above the zener-voltage, the gate voltage of Q_4 starts to rise and the transistor turns on, shorting C_1 to ground. The schmitt-trigger after C_1 will only output a high signal when the capacitor is sufficiently charged, setting the delay time for the receive mode enable signal. The zener diodes and short circuit switch Q_4 set the voltage limits for the receive mode.

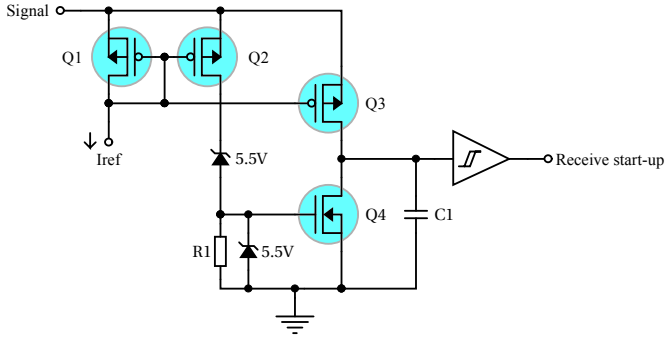


Figure 3.56: Schematic of the receive mode start-up delay circuit

A safe delay that is sufficient for all specified transmit waveforms, chosen in Chapter 2.3,

is 150 ns. A configuration bit to shorten the receive mode start-up delay is added for higher frequency waveforms (10-20 MHz). Figure 3.57 shows simulations of the voltage limits and delays set by the circuit.

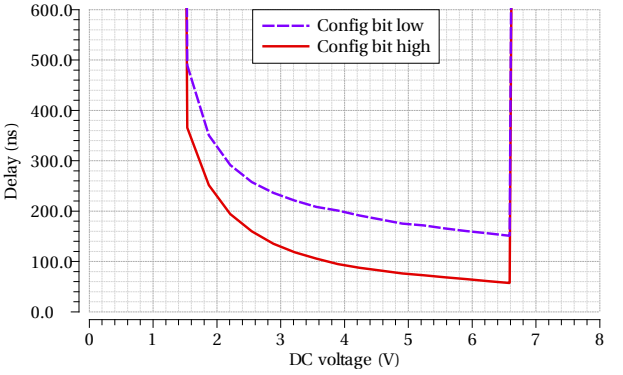


Figure 3.57: Start-up delay for various operating voltages

In receive mode also the communication phase takes place. Additional logic is implemented to time what happens after the data transmission. Figure 3.58 shows the sequence of the enable signals for different parts of the ASIC.
At the start of the receive mode, the start-up signal and receive enable signal go high, enabling the amplifier. When the ultrasound echos are received the configuration data can be transmit at an arbitrary moment. After the transmission, first the receive enable signal goes low, to disable the receive multiplexer. Sequentially the transmit multiplexer can be enabled, which results in the elements that are not going to be used during transmit, to be shorted to ground. At the same time configuration data is latched from the shift registers to the memory.

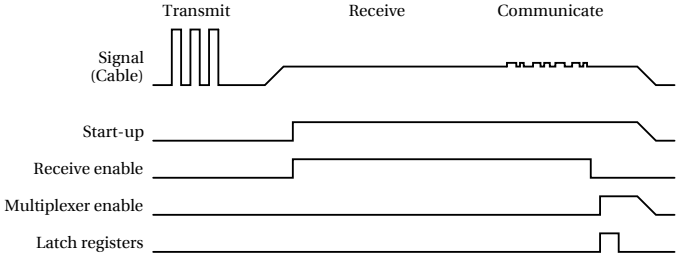


Figure 3.58: Signal sequence during a transmit-receive cycle

In the next receive phase the receive enable signal will enable the receive multiplexer and disable the transmit switches, according to the configuration stored in the memory.

3.6.4. ESD Protection

Electrostatic discharge (ESD) can be a dangerous phenomenon for an ASIC and can already be triggered by just touching the cable. To protect the circuit for ESD a clamp is added that shunts the energy when the voltage on the input is higher than 26 V+V_{th}.

Figure 3.59 shows the implemented ESD protection circuit. A fast rising edge will also trigger the ESD clamp as the capacitance of the ESD diode will pull down the gate of Q_1, enabling the shunt clamp [39]. Capacitor C_1 is added to create a constant voltage for the ESD protection clamp, so it is immune for the fast edges of the transmit pulses. To protect the piezo element pads, a reverse diode to ground is added for negative ESD spikes. The body diode of the transmit switch and D_1 protect the circuit to positive spikes on the element pads.

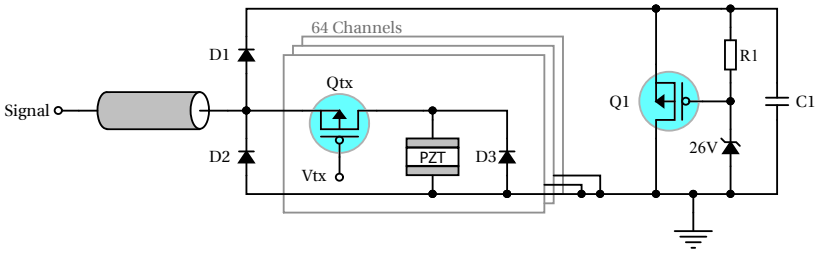


Figure 3.59: Schematic of ESD protection circuit

The transistors used in the circuit can handle a higher voltage than the 26 V limit defined by the ESD protection. A higher limit would help to increase the transmit pressure. A second version of the chip has been taped out with a 5.5 V zener diode stacked on top of the 26 V zener diode, as commonly done in literature to increase the breakdown voltage and reduce the parasitic capacitance [39]. The ESD clamp can not be simulated because no simulation models for the 26 V ESD clamp are available.

3.7. Entire ASIC

To give an overview of how the circuit blocks discussed in this chapter are tied together to make the prototype ASIC, a simplified block diagram is depicted in Figure 3.60.

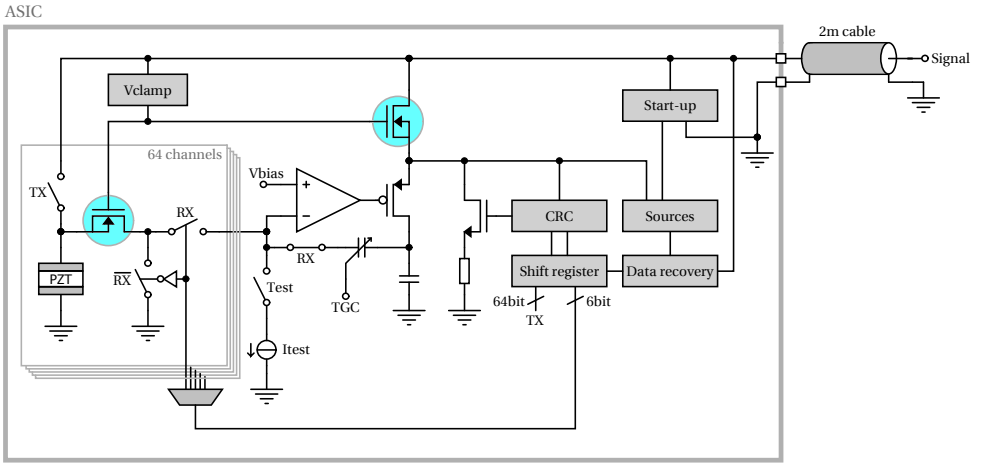


Figure 3.60: Simplified block diagram of the prototype ASIC

Several test features have been added that are not mentioned in this Chapter:

- A test input that connects to the input of the amplifier can be used to characterise low-noise amplifier in the entire system.
- A current can be injected to adjust the biasing block when needed.
- All internal control signals (start-up, load-registers, etc.) are connected to a digital output, for probing if required.
- Several analogue signals are buffered to test pads, to be able to probe internal nodes of the circuit.
- The data and clock signals can be input via a digital pad, skipping the data recovery circuit.
- The internal supply voltage (powering the data recovery block) and the clamping voltage V_{clamp} can be injected via a test pad. This enables testing without having to send transmit pulses to recharge the clamping voltage block.

With those additional test bond pads the prototype ASIC can be properly tested and characterized.

4

Layout

A chip layout has been designed for the circuit discussed in the previous chapters. This chapter will discuss a selection of relevant issues faced in the layout process.

The circuit blocks have been put together in a doughnut-shaped form factor with an outer diameter of 1.5 mm, shown in Figure 4.1. The circular shape is used to fit the form factor of the tip of a catheter. The hole in the centre is left empty to accommodate a guide wire in the final probe design.

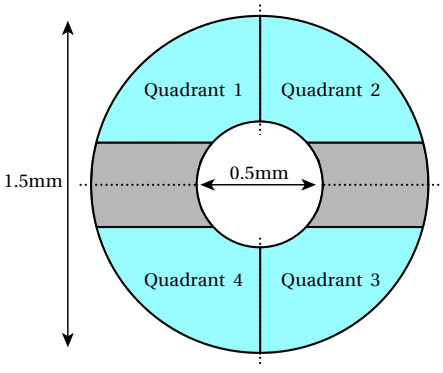


Figure 4.1: ASIC form factor and dimensions

The largest area of the layout is occupied by the transmit and receive channels. To make the layout-work efficient, the ASIC has been split into four equal quadrants, mirrored in the horizontal and vertical axes. The hatched grey part in the middle of Figure 4.1 is used for the remaining circuit blocks.

4.1. Channel Layout

The transmit switch and receive switch together form a channel. The channels are an important part of the layout, because combined they contribute to the largest part of the active area on the ASIC. The total area of each channel is 12 000 μm^2, of which 7300 μm^2 is occupied by the transmit switch. An overview of the layout and dimensions is shown in Figure 4.2. The area of the receive switch is mainly dominated by the N-MOS protection clamp. The transmit switch area is dominated by the two MOM-capacitors and the P-MOS transistor.

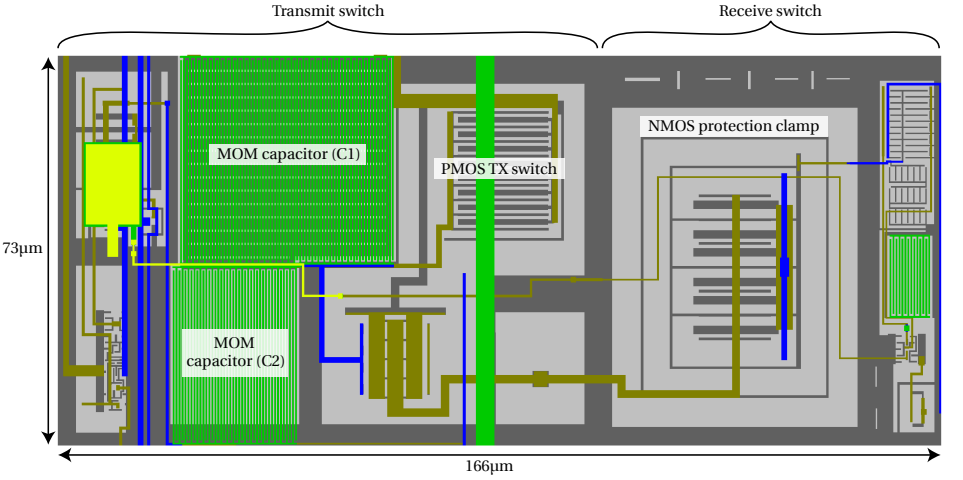


Figure 4.2: Channel layout and dimensions

The layout of the transmit and receive switches took a careful design. All channels are connected individually to the receive multiplexer, but at the same time connected in series for the clock and data signals to the transmit switch shift registers. The wide metal trace in the middle of the channel (green in Figure 4.2) is used to distribute the signal from the coaxial cable over the chip.

4.2. Post-Layout Improvements

The layout involved some important considerations, as especially the transmit switch is quite sensitive to parasitic capacitances. After the initial parasitics extraction the simulation showed that the switches turned on without being enabled. Close inspection of the transmit switch showed that MOM capacitor C_1 had a significant parasitic capacitance to ground, shown as C_p in Figure 4.3. The parasitic caused the gate of the transmit switch to be pulled down in a transmit pulse, causing the switch to turn on. As shown in Figure 4.3 this is resolved by adding a metal shield connected to the transmit signal node (V_{pulse}) in between the substrate and the MOM capacitor. By doing so, the original parasitic capacitance is replaced by a parasitic between the transmit signal and ground,

that doesn't harm the transmit switch performance.

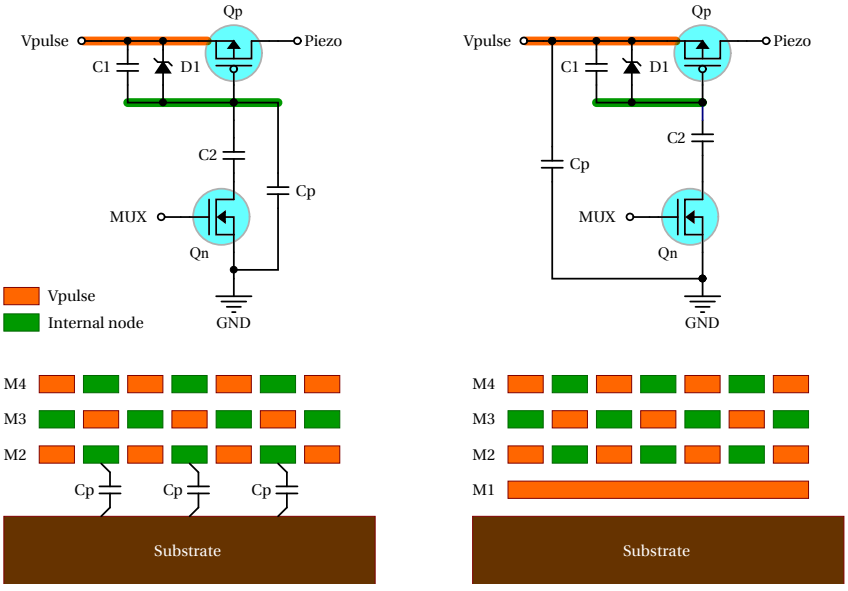


Figure 4.3: Parasitic capacitance (left) and added shield metal (right)

Another important part of the circuit is the memory cell. In the initial post-layout simulation, the circuit was not capable of remembering the configured state. It turned out that the signal controlling the latches spiked at start-up of the chip, causing the memory cells to be reset. Spikes were created in the level shifter controlling the latch signal, due to the parasitic capacitance (C_p) shown in Figure 4.4. The spikes are caused by the internal node at the drain of Q_1 rising slower than the power supply. By adding a MOS capacitor (Q_c) it was ensured that the signal rises together with the power supply on start-up.

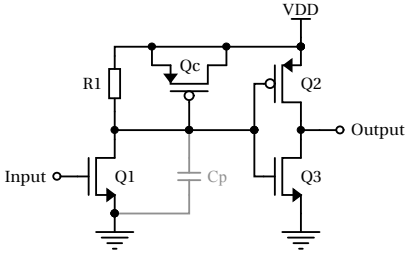


Figure 4.4: Added MOS capacitor (Q_c) to compensate for the parasitic capacitor (C_p)

After those changes the circuit simulation shows the intended operation and the registers retain the data for at least several milliseconds.

4.3. High-Current Paths

In high-voltage and high-current circuits, when creating the layout one must pay attention to the current paths and possible voltage drops associated with them. In the layout of the LNA and transmit switches, the transistor arrays are laid-out in such a way that the current through each transistor is equal. Figure 4.5 illustrates the layout of a high current transistor. From the input current to the output current the path trough each transistor sees the same resistance, causing the current to be distributed equally over the transistors.

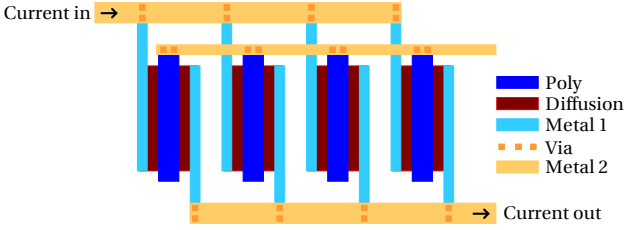


Figure 4.5: Layout of high current transistor

For comparison, if the metal connection in the bottom of the figure was drawn to the left, more current would flow through the leftmost transistor than through the transistors to the right, because of voltage drop over the metal traces.

4.4. Sealrings

For later stage of production, the circular shape is surrounded by a seal rings. Using a laser the chip can be cut out to create the final probe design. Initial tests can be carried out using test bond pads placed around the circle. The routing towards the test-bond pads had to cross the outer circular sealring. To ensure correct operation after cutting the sealring, some precautions were needed.

Cutting around the sealring would leave the inputs floating. As shown in Figure 4.6, the test-inputs have a pull-down resistor to give the inputs a defined state when cut. The output buffers are located inside the circular seal ring but powered by the test-padring. When fabricated the internal circuit will only see the gate capacitance of the output buffers. Even in case the output would be shorted to ground, the circuit can operate as intended.

The power supply test lines are protected using a diode-connected bipolar transistor. When the cutting procedure causes a short, the diode prevents the supply to be shunted to ground.

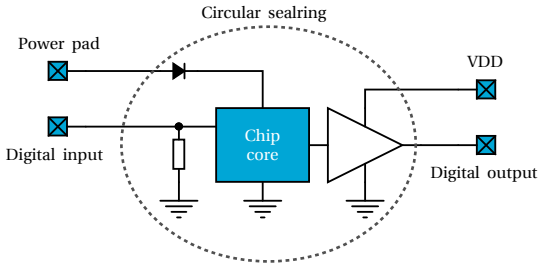
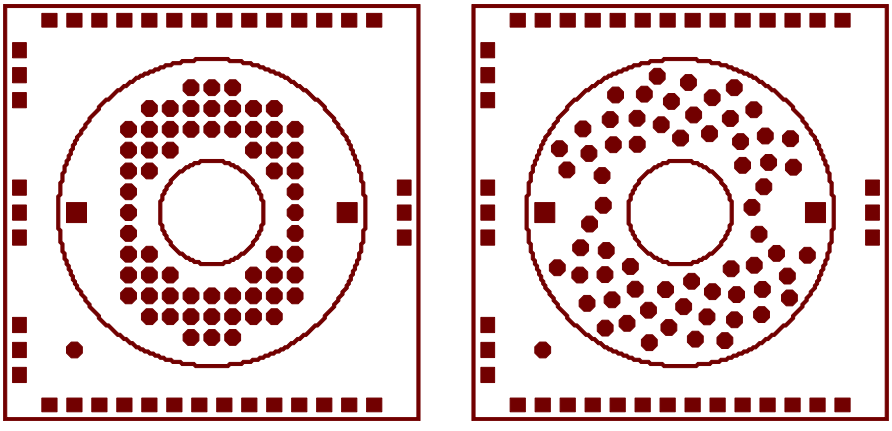


Figure 4.6: Circuit protection for sealring cutting procedure

4.5. Piezo Element Patterns

For testing with the piezo elements two different patterns were taped out. A regular pattern that is easy to machine, shown in Figure 4.7a and the sunflower pattern shown in Figure 4.7b. With the sunflower pattern, eventually better images can be constructed. More advanced techniques (laser cutting) are needed to produce the sunflower pattern on chip, so for initial prototype evaluation the regular pattern can be used, which can be fabricated using a diamond dicing saw.



(a) Regular pattern **(b)** Sunflower pattern

Figure 4.7: Bond pad layout for both element patterns

4.6. Test-Padring Layout

Internal signals that could be useful while testing the prototype ASIC are routed to the test padring. The test padring can be left unconnected in the final application, but helps characterizing the functionality of the chip. An output multiplexer is used to reduce the amount of bondpads needed.

After the piezo elements are fabricated, a ground foil will be placed over the elements. This ground foil is connected to a ground pad on the PCB. To simplify placing the ground foil, one side of the padring only contains ground connections. Those ground connections can either be used to connect the ground foil or be left unconnected. Figure 4.8 visualizes the placement of the ground foil and shows why the absence of bond wires is preferred.

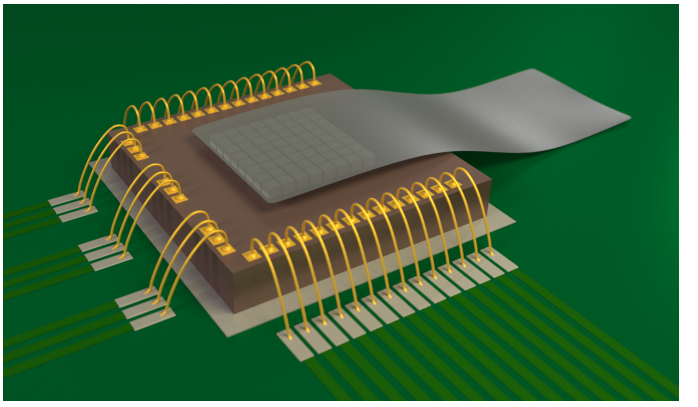


Figure 4.8: The bondpad layout leaves one side empty for the ground foil

4.7. Final ASIC Layout

The final layout of the ASIC with sunflower pattern is shown in Figure 4.9. The two square pads inside the circle (labelled SIG and GND) connect to the coaxial cable. Details on the reference markers can be found in Appendix C.1.

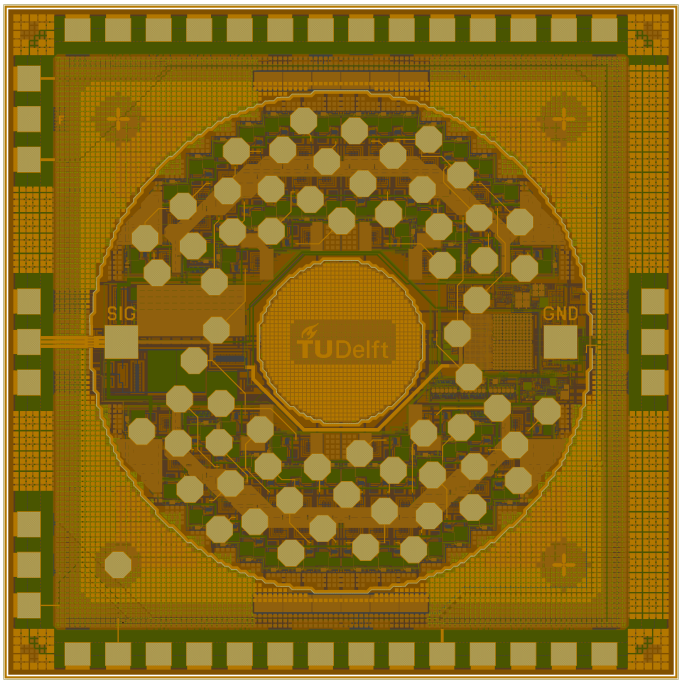


Figure 4.9: Layout of the completed ASIC with element pads in sunflower pattern

An overview of the circuit block placement in the layout is shown in Figure 4.10. The 64 channels are shown in orange, and take-up the top and bottom part of the die. On the left the high voltage and protection circuits are located and on the right the LNA and logic are placed.

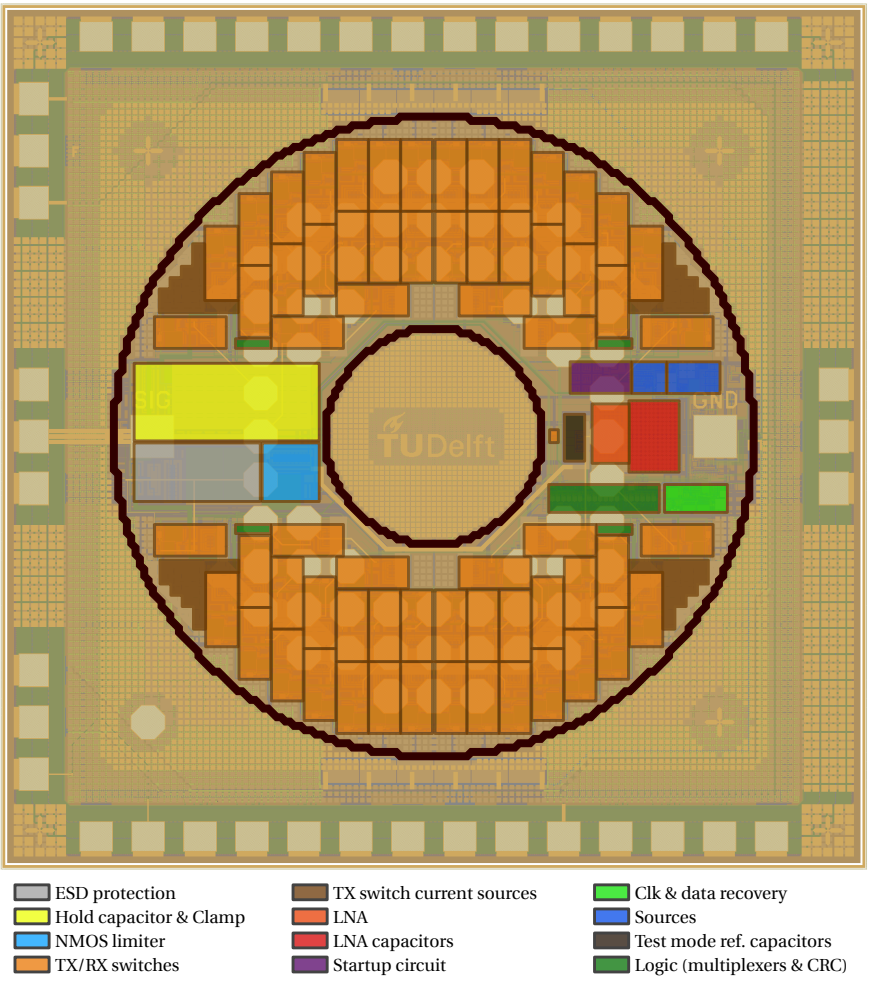


Figure 4.10: Chip layout showing the functional blocks

4.8. Post-Layout Simulations

After layout, simulations of the completed circuit including extracted parasitics have been performed, to verify correct operation. This section will discuss these simulation results and show how all circuits are properly working together in the final prototype.

In normal operation, the sequence shown in Figure 4.11 is used. Initially the capacitor used to generate the clamping voltage needs to be charged by sending a transmit pulse. After this initial pulse, the ASIC can operate normally. Data is sent to configure the ASIC and select the transmit and receive channels. When configured the supply current can be inspected to check whether the data transmission was error-free. Next an arbitrary high voltage pulse can be transmitted after which a low voltage DC signal is supplied to enter the receive mode. The receive mode can be used for several hundreds of microseconds, but usually takes not more than 13 µs as the imaging depth is typically not higher than 10 mm in IVUS. Operating with this scheme a pulse repetition rate of 30 kHz can be reached.

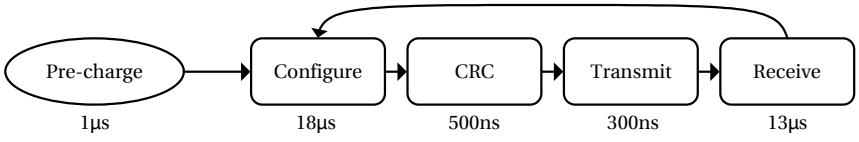


Figure 4.11: Image acquisition state diagram

To receive the signal of all channels, a time of $64 \times 35\,\mu$s is required. Depending on the transmit scheme a high frame-rate lower quality image or low frame rate high quality image can be obtained. If for example transmit is done in groups of 4 elements, a medium frame-rate of 28 fps is possible.

The post-layout simulation results showing the various states of the acquisition are shown in Figure 4.12. The data transmission is shown in the top right corner, for a 300 mV data amplitude. The piezo voltages in transmit for an enabled and a disabled channel are shown at the bottom. The output signal (current at the system side) of the piezo material on the selected channel is visible in the top right.

The power consumption of the full ASIC in receive mode can be calculated using the plot that show the supply current (Figure 4.12, top right). The average current in receive is 1.45 mA when supplied with 3 V, making the total power consumption in receive 4.4 mW (reduced power) and 6.1 mW (normal mode).

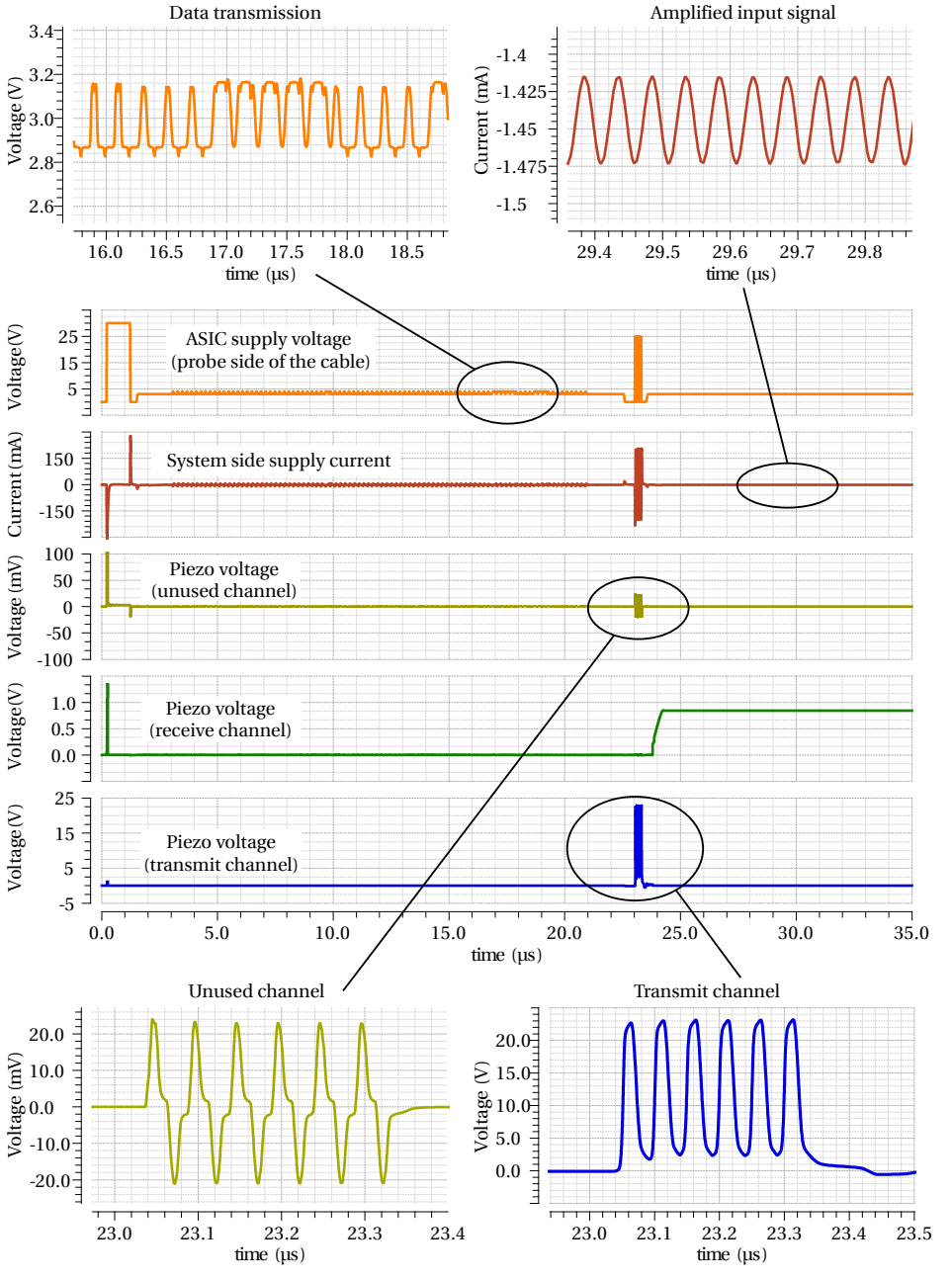


Figure 4.12: Completed chip, post layout simulation including the padring

The gain of the receive mode is simulated for both the normal power mode and the reduced power mode, as shown in Figure 4.13. For the reduced power mode a small reduction of bandwidth in the highest gain setting is apparent.

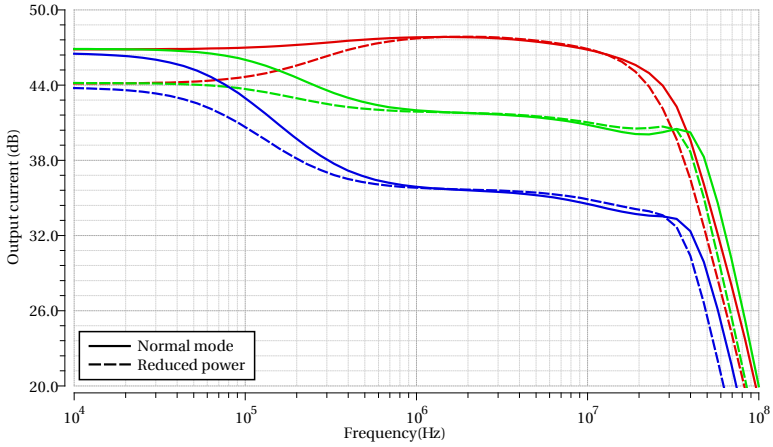


Figure 4.13: Gain of completed ASIC, post layout simulation including the padring

5

Experimental Set-Up

This chapter describes the external circuit that can be used to operate the ASIC. The main subject of the external circuit is the transimpedance amplifier that converts the current flowing through the chip to an output voltage, and powers the ASIC in receive mode. Moreover a protection circuit needs to be implemented to protect the input from the transimpedance amplifier to the high voltage transmit pulses.

5.1. Driving the Chip

The input of the transimpedance amplifier doesn't tolerate the high voltage pulses. In Chapter 2 several protection circuits have been discussed. Diode bridge clamps were not used on the chip because they are power hungry, but for off-chip usage they have good properties. The small signal impedance and noise can be made low by increasing the current. The schematic of a diode bridge clamp is shown in Figure 5.1. For small signal levels, the diodes are forward biased and the signal can pass through the bridge to the input of the LNA. When the signal amplitude is large, the diodes will reverse bias and block the signal.

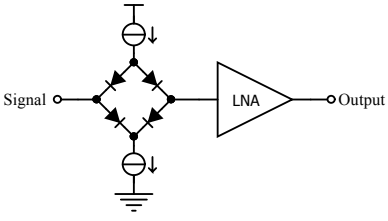


Figure 5.1: Diode bridge limiter circuit

The small signal resistance of a diode is defined by:

$$r_\mathrm{d} = \frac{kT}{qI_\mathrm{d}} \tag{5.1}$$

When the diodes are biased at 10 mA they have a small signal resistance of about 2.5 Ω.

With the limiter in place, the transmit pulses can be coupled-in capacitively and the limiter will automatically block the high voltage pulses from reaching the transimpedance amplifier.

Figure 5.2 shows the circuit with the transimpedance amplifier in place. The current sources in the diode bridge are simply implemented by placing a resistor. The termination resistor for the cable should now be tunable, so it can be set lower to combine with the diode bridge to 50 Ω.

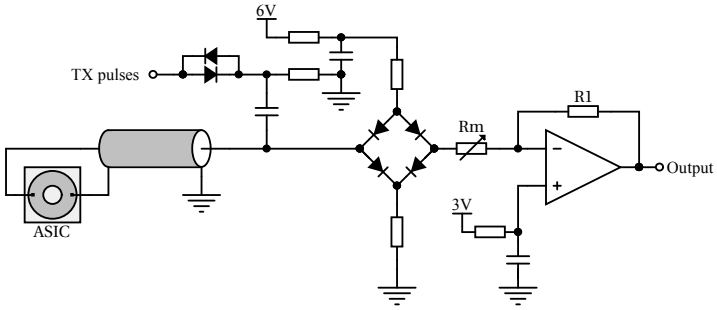


Figure 5.2: System side driver circuit for the ASIC

The transmit pulses are connected to the circuit via an expander. The function of the expander is to block any noise coming from the pulser when its output is low. The 3 V and 6 V supply lines are connected via an RC-filter, to reduce the in-band noise on the supply lines.

The transimpedance amplifier's input-referred noise should not contribute significantly to the noise of the complete system, as discussed in Section 3.2. To achieve this, an opamp with an input referred noise of less than 2 nV/$\sqrt{\mathrm{Hz}}$ has to be used. From the comparison (Appendix B), the high speed opamp THS3001 [40] has been chosen. This opamp has an input referred noise voltage of 1.6 nV/$\sqrt{\mathrm{Hz}}$ and a bandwidth of 420 MHz, which meets the specifications easily.

5.2. Printed Circuit Board

A printed circuit board (PCB) has been designed to implement the system-side circuit and to facilitate testing the prototype chips. Figure 5.3 shows a render of the PCB. An FPGA board is integrated to generate the self-clocking data stream and to do the time-to-digital conversion for the fabrication test mode. Moreover, the FPGA can check for

errors in the transmission by evaluation of the supply current (see Section 3.4.6) and if necessary resend the configuration data.

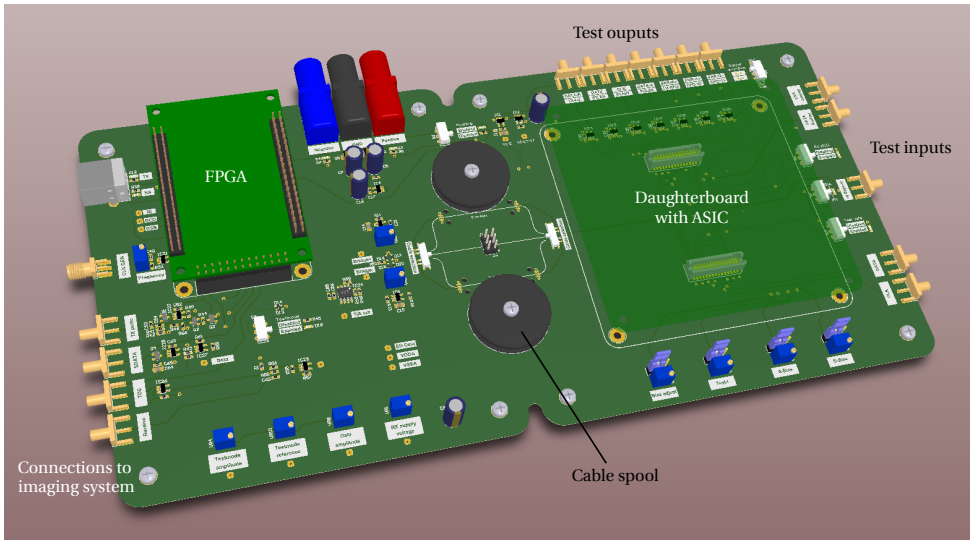


Figure 5.3: Render of the test PCB

A daughterboard with the prototype-ASIC is mounted on top of the right half of the PCB.

The signals used in the final circuit are all located on the left side of the PCB. The pulser and imaging (or acquisition) system can be connected using the SMB connectors.

The test outputs of the ASIC are at the top right of the PCB. A selection switch is used to select a sub-group of test outputs, using the multiplexer on the chip.

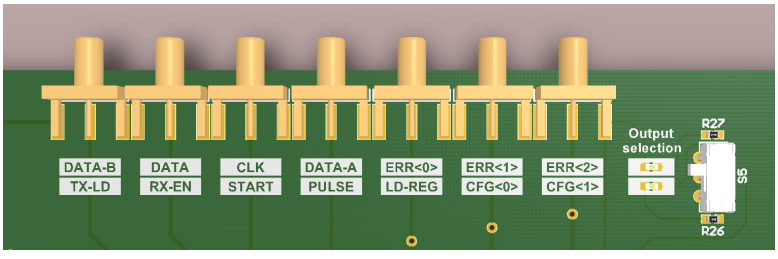


Figure 5.4: Detail of the test output multiplexer selection switch

Two cable spools are integrated on the PCB, to hold a 1 meter and a 2 meter coaxial cable. Switches are used to select one of the cables for characterization. Additionally a cable can be connected to the PCB to do acoustical measurements with the daughterboard disconnected from the motherboard.

6

Conclusions and Future Work

The goal of this thesis was to create an ASIC for intra-vascular ultrasonic imaging, that can be integrated on the tip of a catheter and connects to an imaging system using a single cable. A chip has been taped-out which implements 64 channels that can be used to transmit and receive ultrasonic waves using piezoelectric transducers.

To realize a transmit mode, receive mode and test mode using a single coaxial cable, several techniques have been implemented:

- A novel transmit-switch circuit with a small area has been implemented, making it possible to fit 64 elements in the form factor of a 1.5 mm diameter circle. The transmit switches can be individually enabled to pass an arbitrary waveform, with frequencies ranging from 2 MHz to 20 MHz and voltage levels up to 26 V.
- A communication scheme with transmission error detection has been implemented that can be used to configure the ASIC. An incorrect data transmission is flagged by increasing the supply current. A reliable configuration of the ASIC can thus be ensured. Communication with the chip enables the possibility to multiplex and thus the possibility to create a multi-element probe design.
- Automatic switching, based on the signal-level and timing, has been introduced to start the receive mode. In receive mode an integrated low-noise current amplifier reads out a selected piezo element and conditions the signal to drive the coaxial cable using its output current. The amplifier has three gain settings, covering a dynamic range of 74 dB, which is well above the target specification of 60 dB.
- A test mode that measures the capacitance of the fabricated piezoelectric elements has been added: By only making minor changes to the LNA it is turned into a capacitance to time converter. The output signals can be digitized for analysis and verification of the transducer-fabrication process.

Post-layout simulations predict that the circuit will perform according to the specifications. A prototype chip has been taped-out and is currently being fabricated for experimental verification. To operate the chip, a system side circuit is designed that conditions the signals to be compatible with standard ultrasound imaging systems.

The ASIC proposed in this work is the first front-end ASIC that implements transmit and receive functionality using a single cable. Compared to the demonstrated designs capable of transmit and receive, the cable count is improved by 4 times. Table 6.1 shows a comparison with the recent contributions on IVUS front-end ASICs.

Table 6.1: Performance summary and comparison with prior art

	[5]	[6]	[8]	[7]	**This work**
Technology	0.18 µm	0.35 µm	0.35 µm	0.18 µm BCD	0.18 µm BCD
# coax. cables	1	13	2	4	1
Power (RX mode)	13.2 mW	20 mW	53 mW	10 mW	6.4 mW
Bandwidth	20 MHz	40 MHz	40 MHz	16 MHz	24 MHz
Receive channels	1	56	6	64	64
Transmit channels	-	64	6	16	64
Transmit amplitude	-	25 V	-	26 V	26 V

The table shows that the performance of the circuit does not deteriorate compared to prior art when using fewer cables to connect to the imaging system. Even with a single cable very similar specifications can be reached.

6.1. Improvements and Future Work

The main focus of this work was to combine all functions in an ASIC that connects to the imaging system with a single cable. Individual blocks of the circuit can most likely be improved to increase the overall performance.

Further circuit improvements can be made in reducing the area of the channels and simplifying the circuit where possible. Some suggestions are provided below:

- After transmit it takes 955 ns before the amplifier is operational. This is longer than the specified 1 µs from start of transmit to receive operation. The settling time of the amplifier can be shortened, to reduce the start-up time.
- In the transmit switch transistors can be used that tolerate higher voltages. 45 V transistors of the same technology for example have a marginally larger area.
  The pull-up current sources (of Figure 3.6) can be simplified by using a resistor. This was the initial plan, but because of uncertainty about the voltage tolerance of the poly resistors and the lack of good documentation, the safer option of using high voltage P-MOS transistor was implemented. The poly resistors are much smaller, creating the possibility to integrate them into the channel, removing the routing of all connections to the current sources.
- The channels can be significantly reduced in size by replacing the transmit switch capacitor by a MIM capacitor. As the voltage on the capacitor is limited by a zener diode, the voltage should stay within the safe operating voltage. The current MOM capacitor takes up an area of 42 µm × 42 µm. A MIM capacitor can be placed over the transmit switch reducing the area occupied by a channel by 15%.

- The input clamp of the amplifier can be made smaller, because of the higher parasitic capacitance seen at the input of the amplifier after post-layout extraction changes the trade-off for the optimum size.
- Finally an interesting alternative for the N-MOS voltage limiters might be to use depletion mode mosfets in a similar way as the N-MOS limiters were used in this work. Using depletion mode mosfets eliminates the need for a voltage higher than the supply voltage, while keeping the protection effect. Potentially this means that the storage capacitor and initial charging pulse can be left out, simplifying the transmit scheme.

Before the ASIC can be used inside an IVUS catheter, several steps still have to be taken. One of the first steps will be to find a good way to connect the cable through the back of the chip to the circuit, and next to that several other mechanical issues need to be addressed.

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A

Technology

As the transmit signal has an amplitude of several tens of volts, the chip design needs to be made in a technology compatible with high voltages. Two different technologies were considered for the high voltage chip design. The XFAB foundary provides fully isolated devices by using silicon-on-insulator (SOI) technology combined with deep trench isolation (DTI). Due to the isolation properties a relatively small area is occupied by the high voltage switches. A simplified drawing of the vertical structure is shown in Figure A.1. Clearly visible in the figure is the isolation around all sides of the device (in grey).

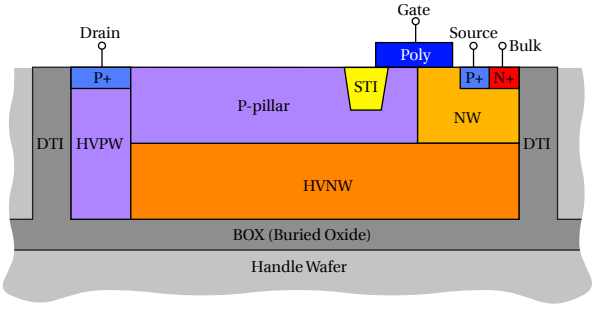

Figure A.1: Simplified vertical structure of XFAB HV transistor

Another way to isolate a high voltage device from the substrate is by creating a reverse biased junction that can withstand the high voltage. The TSMC foundary offers such a technology (0.18 μm BCDg2). The downside of using junction isolation is a bigger area occupied by the transistor. A simplified drawing of a TSMC high voltage transistor is shown in Figure A.2. The source and bulk of the PMOS transistor are always connected to the highest potential in the device. This ensures that the P-N junction with the substrate is always reverse biased.

A

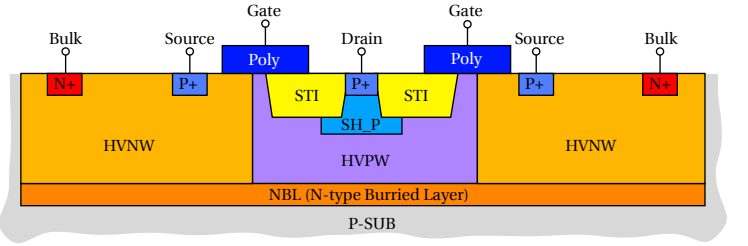

Figure A.2: Simplified vertical structure of TSMC HV transistor

The area consumed by an XFAB PMOS trasistor is 520 μm^2. Compared to the TSMC transistor with the same gate area that consumes 850 μm^2, it is significantly smaller. For isolated NMOS transistors the difference is even more substantial, as the TSMC isolated NMOS transistor occupies 2450 μm^2.

Although the area benefits of the XFAB technology are convincing, for practical reasons the TSMC technology has been chosen for this work.

B

Commercial Low-Noise Opamp Comparison

Type	Manufacturer	V_n	V_{max}	GBW	I_{supply}	Slew-rate
LTC6409	LT	1.10 nV/$\sqrt{\text{Hz}}$	5.5 V	10 000 MHz	52 mA	3300 V/µs
LT6200	LT	0.95 nV/$\sqrt{\text{Hz}}$	12 V	1600 MHz	17 mA	310 V/µs
AD8009	AD	1.90 nV/$\sqrt{\text{Hz}}$	12 V	1000 MHz	14 mA	5500 V/µs
AD8017	AD	1.90 nV/$\sqrt{\text{Hz}}$	12 V	160 MHz	7 mA	1600 V/µs
OPA695	TI	1.70 nV/$\sqrt{\text{Hz}}$	12 V	1700 MHz	13 mA	4300 V/µs
OPA847	TI	0.85 nV/$\sqrt{\text{Hz}}$	12 V	3900 MHz	18 mA	950 V/µs
LMH6628	TI	2.00 nV/$\sqrt{\text{Hz}}$	12 V	200 MHz	9 mA	550 V/µs
THS3001	TI	1.60 nV/$\sqrt{\text{Hz}}$	32 V	420 MHz	6.6 mA	6400 V/µs
THS4031	TI	1.60 nV/$\sqrt{\text{Hz}}$	32 V	100 MHz	8.5 mA	100 V/µs

C

Production reference

C.1. Reference markers

Several reference markers are added to ease the bonding and piezo fabrication steps. Figures C.1 shows the locations of the reference marks (in μm). Lines with a pitch of 100 μm are added at the top and bottom of the chip to aid the alignment of the dicing saw (the lines should be collinear with the dicing saw cut).

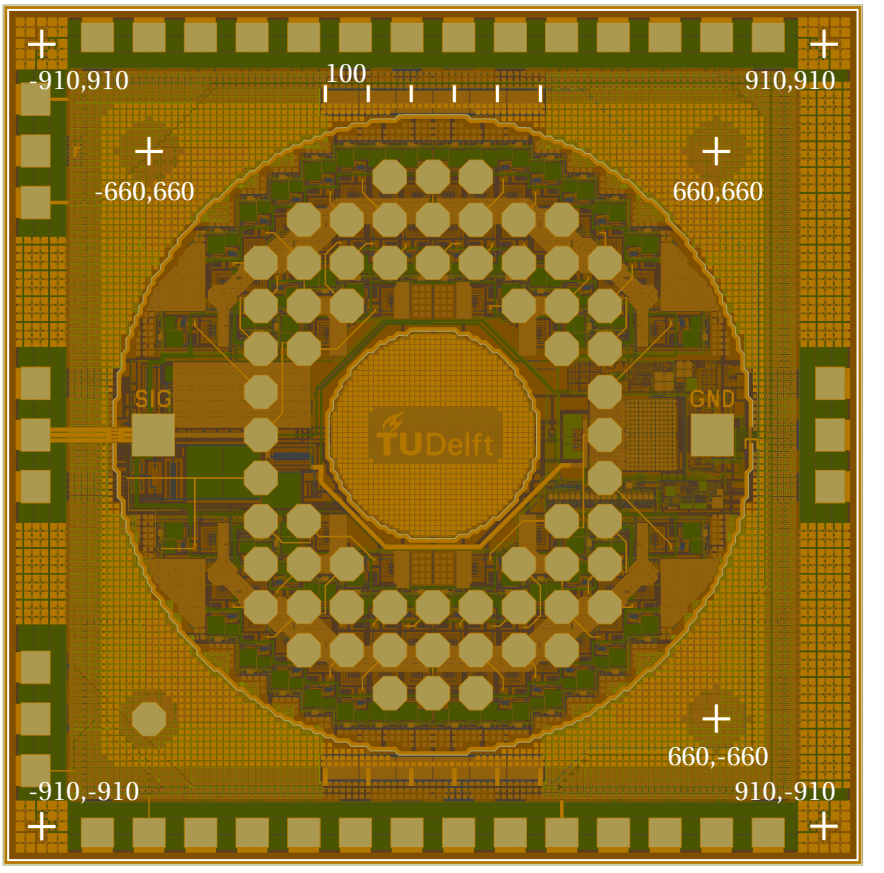

Figure C.1: Reference mark locations relative to the center of the chip

C.2. Chip bonding

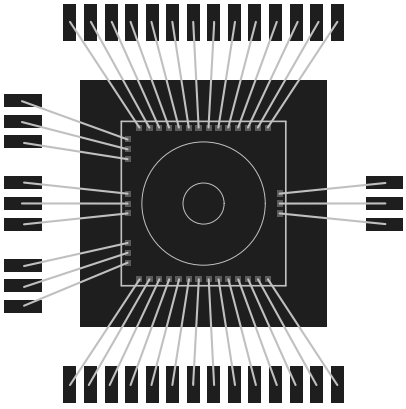

Figure C.2: Chip bonding diagram for PCB footprint

C.3. Bond connections

The output bond pad connections, used to test the ASIC are shown in Table C.1.

Table C.1: Pin mapping of test output multiplexer

Pin	Function	Pin	Function
SEL	0	SEL	1
A0	TXMuxEN	B0	Data out B
A1	RX EN	B1	Data
A2	Startup	B2	Clk
A3	Pulse	B3	Data out A
A4	load reg	B4	ERR<0>
A5	config<0>	B5	ERR<1>
A6	config<1>	B6	ERR<2>

An overview of all bond pads in the test-padring is printed in Figure C.3

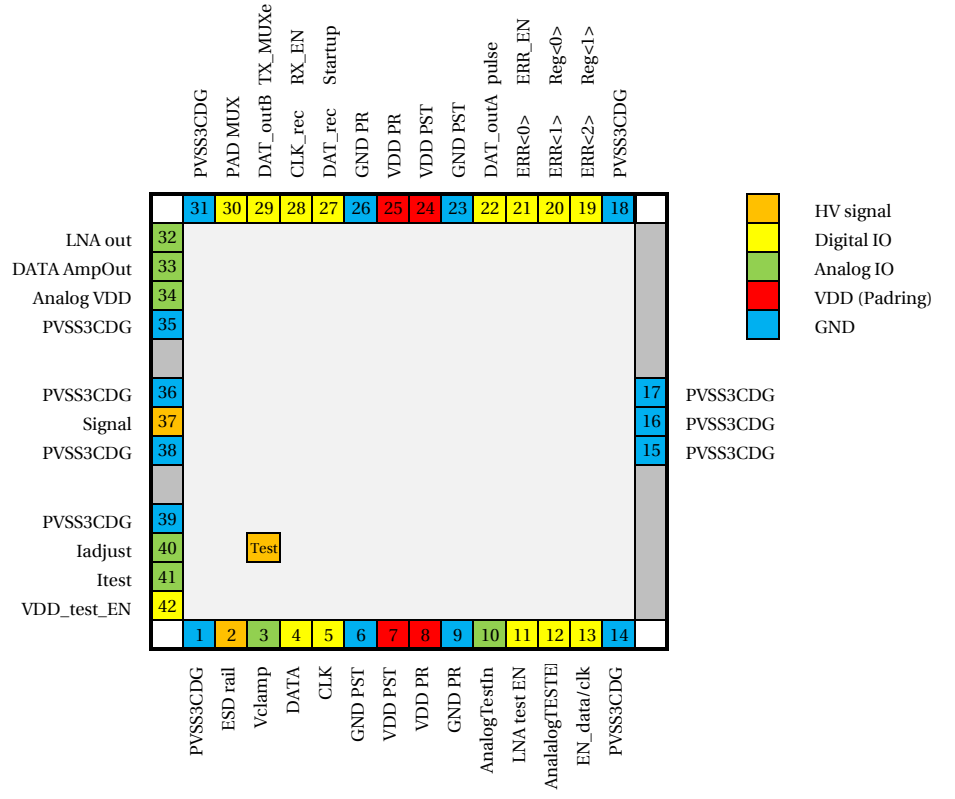

Figure C.3: ASIC test-padring connections