Fundamental Characteristics of a Pinned Photodiode CMOS Pixel

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To my beloved parents and Jianhua

致我亲爱的父母和叶剑华

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Chapter 1

Introduction

Over the past four decades, the information revolution has changed the lives of most people forever. One of the technologies, which has rapidly evolved in this period is the digital imaging technology. Image and video, two important carriers of information, fulfill a unique and irreplaceable function for a wide variety of applications.

In this chapter, a brief introduction to image sensor development will be given in Section 1.1. CMOS image sensor technology will be introduced considering device, circuit, and system aspects in Section 1.2. In Section 1.3, the challenges and motivation of this thesis will be presented. Finally, the structure of the thesis will be given in Section 1.4.

1.1 Introduction to Image Sensor

In 1922, the Nobel Prize in Physics 1921 was awarded to Albert Einstein for “his services to theoretical physics and especially for his discovery of the

law of the photoelectric effect". Almost a century later in 2009, the Nobel Prize for Physics was awarded to Willard S. Boyle and George E. Smith for their invention in 1969 of the first successful imaging technology using a digital sensor: the Charge-Coupled Device (CCD) in 1969 [1.1]. These two prizes mark two important milestones in the development of digital imaging which have left an indelible mark on the field. For instance, the photoelectric effect proposed by Einstein is still the basis for all digital imaging technologies used today. What is more, CCD technology, with the improvement on the fabrication, was becoming the dominant digital imaging technology in 1980s and 1990s. Until today, the CCD technology still plays an important role in different digital imaging applications.

Before the first reported CCD device, there were also several attempts to invent a new device to replace the film-based camera with an electronic image sensor. Morrison [1.2] invented the first MOS image sensor in 1963; Horton et al. [1.3] in 1964 and Schuster et al. in 1966 [1.4] also reported progress with these preliminary imaging devices. In addition to the photon sensing elements, the researchers also considered the electron storage and readout mechanism. In 1967, the integrated pn-junction photo-detector was first introduced by Weckler [1.5], which is called passive pixel since it does not include any active component; in 1968, the in-pixel source follower was used in a pixel array for readout and a buried photodiode structure to reduce dark current and to improve the packing density of pixels was presented by Noble et al. [1.6], which is the first active pixel sensor (APS). These inventions, which have had a significant influence on the working mode of CMOS image sensors, are even still used nowadays.

Since the invention of the CCD in 1969, the focus of digital imaging development has changed from the MOS imagers to CCD technology, because the CCD devices achieve a lower fixed–pattern noise than MOS imagers did, due to technological circumstances at that time. However, it still took 15 years from the invention of CCD imagers to their vast commercialization, to attain the necessary improvements in the technology. After solving the fabrication and reliability problems, the commercialization potential of CCD technology was realized and it quickly dominated almost all digital imaging applications.

Nowadays, most CCDs use the dedicated optimized photodiode as the photon sensitive element, as it can achieve good quantum efficiency, dark current, uniformity, and noise performance. The reason why CCD technology dominated and was massively manufactured since 1980 was mainly due to its superior image quality. An array of closely spaced MOS capacitors can be used to shift data along in a serial bit stream in the form of packets of electrons. The electrons finally shift to the chip level output amplifier for charge conversion to the voltage signal and then to the output. Due to this multiple stage shift out mechanism for charge readout in a CCD, transfer efficiency is a tradeoff with the frame rate.

With the improvement of CMOS fabrication technology, and the demand for system integration and power consumption, several groups attempted to reignite CMOS image sensor development in 1980s [1.7, 1.8]. The revolutionary break happened in the early 1990s. The new development of the passive pixel sensor [1.9, 1.10], and active pixel sensor [1.11, 1.12] established the remarkable foundation for the subsequent flourishing of the CMOS image sensor. In 1997, the implementation of a pinned photodiode demonstrated a new pixel structure that was able to provide an advanced noise cancellation technique in CMOS technology [1.13]. Consequently, this proposed technique made it possible for CMOS image sensors to compete with the CCD with respect to image quality. Due to the natural advantages of the CMOS image sensor with cost and system integration, more research effort has been invested in the development of the CMOS image sensor to achieve a low cost and high performance for multiple applications. Comparing to the performance of CCDs, the CMOS image sensor has nearly the opposite pros and cons. The advantages of CMOS imagers are:

1. High integration and low cost: as already mentioned, the CMOS image sensor can integrate the photon sensitive component with standard CMOS technology, which means the readout circuit, ADC, and even the digital signal processing module can be integrated in one chip. This system-on-chip architecture advantage is becoming one of the most important driving factors for CMOS image sensor development. CMOS technology has a smaller process dimension than CCD technology. System integration in one chip can further

decrease the product area, which is very important for manufacturing costs. Integrated intelligence leads to a smaller, low-cost product.

2. Low power: since the CCDs require multiple relative high power supplies compared with CMOS image sensor, the power consumption of the CMOS image sensor can achieve much less power consumption than CCDs.
3. High speed: CMOS image sensor design can achieve a more flexible readout mechanism, which results in a much higher speed than that of CCDs.

Due to these advantages, CMOS imagers began their “golden age” in 2000 due to the huge demand for mobile phones. With the natural advantages like low power consumption, small size, low cost, and high speed, CMOS image sensors are perfect to meet the requirements of mobile electronic device application. With technology development and performance improvement, CMOS imagers have replaced CCDs in many fields. Many ideas and inventions for CCDs have been fused to CMOS image sensor technology.

1.2 CMOS Image Sensor: Device, Circuit, System

Due to the development which CMOS image sensors have undergone over many years, today they are considered mainstream in the market. However, since the system itself is complicated, the research and development of CMOS image sensors involved the improvement in process, device, circuit, and system aspects. From the signal flow aspect, Figure 1-1 shows an example of a simple CMOS image sensor system diagram. The input of the system is the light signal (photon). The pinned photodiode (PPD) is normally used in CMOS image sensors as the light sensitive element device. The floating diffusion together with the source follower and other transistors in the pixel are called pixel readout. In CMOS image sensors, pixel study is based more on the device level.

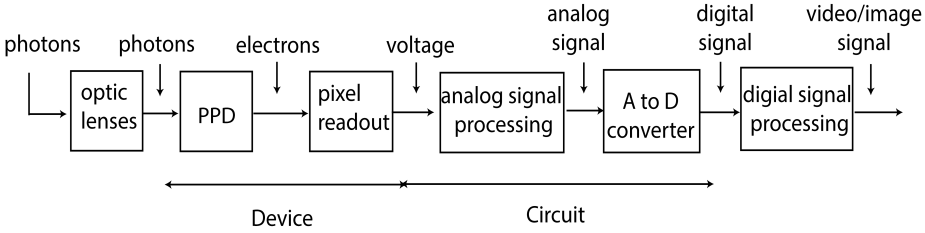

Figure 1-1: Image sensor system signal flow diagram.

With the scaling down of the semiconductor process, image sensors have benefited from high resolution, low power consumption and lower cost. The pixel pitch has shrunk from 20μm to 1μm and the resolution has increased from 10 thousands to 100 megapixels level. It was inevitable that competitors also have to join the megapixel race if they want to survive in the digital camera sector. Pixel size reduction has already become the most powerful driving force for new technologies and innovations in pixel development. At the process and device level, a great deal of effort has been made to achieve good sensitivity with a shrinking pixel pitch. The technologies such as backside illumination (BSI), pixel binning, and electron multiplication have been proposed. BSI is one of the technologies which enhances image quality by improving sensitivity. BSI technology was first developed in CMOS image sensor by Omni Vison [1.14] and Sony [1.15] commercially in 2008. As its name implies, this technology reversed the conventional front illumination method by illuminating the backside of the silicon substrate. Using the backside of the silicon as the photon sensitive area and front-side as the readout circuit decreases the chip area and thus miniaturizes the pixel pitch.

With the photon converted into a voltage signal in the pixel, the signal processing circuit function in the image sensor is similar to that of other sensors. In the current digital camera market, imaging systems require to have high performance but low energy consumption, at high speeds but with a small size. All of these requirements are strongly linked to the circuit level design of CMOS image sensor. Here, the circuit level design is mainly referred to as the analog signal processing circuit and analog-to-digital converter (ADC) design. Analog signal processing is employed between sensor data acquisition and analog-to-digital conversion. Normally, to achieve a good noise performance and SNR, based on different specifications and

design architectures a few different sampling methods and amplifier designs are implemented in this analog signal processing chain. Normally, this processing chain is implemented as column circuitry. In CMOS image sensors, correlated double sampling (CDS) [1.16] is a widely used noise reduction technology which can reduce the reset noise and offset effectively. Furthermore, based on CDS technology, some different sampling technologies [1.17-1.24] have been proposed for noise reduction.

The analog to digital conversion of the pixel output is an important process for readout that affects the image quality, frame rate and so on. ADC designers are usually concerned with resolution, speed and power consumption [1.25]. For ADCs in image sensors, the optimization goal is to save area and power while maximizing the conversion speed. According to the location of the ADC on the image sensor chip, ADCs can be sorted into three categories: the chip level ADC, column level ADC, and pixel level ADC. The chip level ADC is globally connected at the output of the analog signal of the whole sensor. All pixel outputs are time-multiplexed to the input of the global ADC. The drawback of the global ADC image sensor is a low frame rate limited by this global working principle. The advantage is that there are nearly no area constraints for the layout. To fulfill the requirements for sensors with a high resolution and high frame rate, the column level ADC [1.26-1.31] has been used for a few years. The input of the column level ADC is connected to one group (one or a few) of the column circuit outputs. By increasing the number of ADCs working in parallel, the frame readout time will be reduced. The main challenge of column level ADC design is the area limitation. By placing one ADC in every column, the column ADC layout width should be smaller than the corresponding pixel pitch. If an ADC is included at the pixel level [1.32-1.34], the SNR can be increased compared with a column level ADC or chip level ADC [1.32, 1.35]. A pixel level ADC helps to reduce the system noise by combining an analog circuit and signal in the pixel and only transmitting digital data. In addition to the noise benefit, the advantages of a pixel level ADC also include low power and convenience pixel signal accessibility. Since every pixel includes an ADC, the fill factor of the pixel will decrease. The limitation of the pixel level ADC design is the area, which poses a big challenge for the designer.

Thanks to the optical lenses, analog devices, circuit blocks and digital signal processing blocks, the image sensor system has become a complete system which can transform light signals into an image. With the development of process technology and design innovation, the image sensor system is now used in many fields. The image sensor system can be used not only for photo cameras and mobile products, but also for the industry machine vision, surveillance, medical imaging and scientific research.

1.3 Motivation and Objectives of the Thesis

As mentioned above, CMOS image sensors continue to become an increasingly more complex system, as a variety of new processes and circuits have been integrated in image sensors' technology. In this complex system, the pinned photodiode CMOS pixel is still the key component, which is related to many important performance features of image sensors. To further improve the related performance and processes of pixels, a thoroughly investigated and characterized PPD pixel structure is needed.

The high performance demanded by CMOS image sensors normally includes one or more specifications such as high resolution, high dynamic range, high speed, low noise, low dark current, no image lag, etc. Some of the specifications are related while some need to be a trade-off. There are many important topics worth investigating for pixel performance improvement. In this thesis, the research focus can be summarized by the following three aspects:

- With the high-resolution trend of image sensors the pixel dimension is shrinking which means a smaller photon sensitive area and small full well capacity in normal cases. A high dynamic range pixel means low noise and high full well capacity. Thus achieving a high dynamic range and high resolution together requires accurate control and estimation of the full well capacity, pinning voltage, and transfer gate potential barrier.

- For high speed and low light level imaging application, the number of photon-generated electrons in a PPD is limited by the short exposure time and low light level input. In these cases, complete transfer of all electrons in the PPD is becoming an important issue for pixel designers. For very large photodiode pixel designs, the charge transfer time is longer than for a small photodiode, but a decreasing charge transfer time is necessary for high speed applications. For ultra-low noise and photon counting application, the floating diffusion has been reduced into a minimum [1.36-1.38]. The conversion gain has already even reached 300μV/e^-. In this situation, even one electron missing during the transfer process will become an issue.

- Dark current is another important performance parameter for CMOS pixels, as it is closely related to noise performance, it is particularly important for long exposure times and elevated temperatures. With the technology shrinking, the hot carrier in the MOSFET is also a possible dark current source in pixel design. Learning more about the hot carrier mechanism can be helpful to avoid hot carrier effect in pixel.

1.4 Thesis Outline

The outline of the thesis is shown in Figure 1-2.

In addition to this first chapter, there are five more chapters in this thesis. Chapter 2 gives an introduction of 4T CMOS active pixels. Upon reviewing the PPD device physics and 4T pixel design, a few basic characterization parameters are briefly introduced.

In Chapter 3, two test chips are introduced. Based on the designed testchips, the potential based analysis of the PPD-TG-FD structure is presented. A simple physics model of pinning voltage is proposed, and the pinning voltage is measured for these two test chips. Next, using the same characterization method of the pinning voltage, the transfer gate “ON” and “OFF” channel potential can be characterized. Based on the classic MOS model, the related transfer gate process parameter can be estimated. Using the feed forward

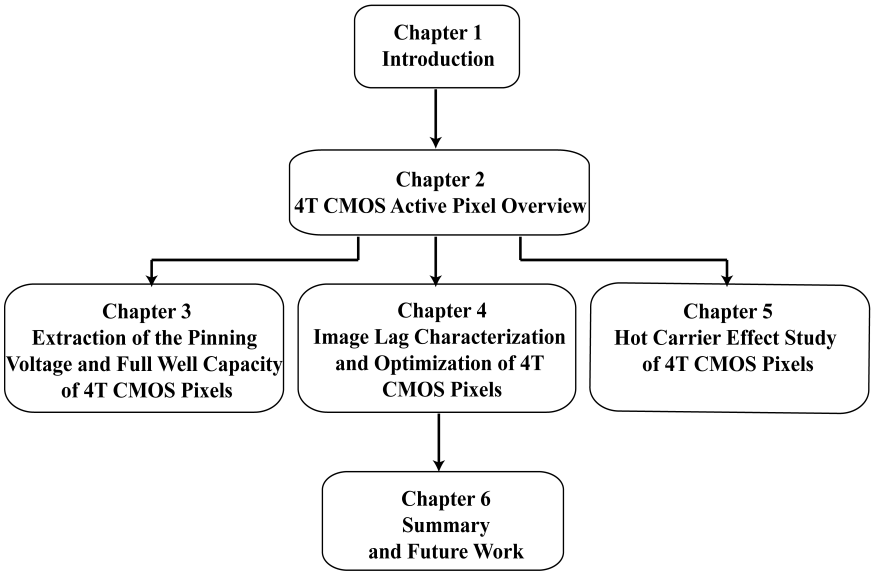

Figure 1-2: Outline of the thesis.

effect measurement, a few secondary order effects which might influence the TG "OFF" potential barrier, are discussed based on the measurement result.

In Chapter 4, the focus shifts to the charge transfer process of the pixel. The image lag related characterization and optimization are discussed. The origins of image lag are analyzed. The influences of the photodiode shape, transfer gate dimension, and transfer gate voltage on image lag performance is discussed. Based on the photodiode shape and transfer gate shape, a few different variations are implemented for image lag performance optimization.

In Chapter 5, the focus is on the hot carriers effect of the source follower of the 4T pixel. In the review of the hot carrier mechanism in the MOSFET, the hot carrier effect in 3T and 4T CMOS active pixels is theoretically analyzed. Furthermore, the measurement results based on the 4T pixel test chips are provided to support the analysis. The hot carrier effect dependency on the voltage, current, and temperature is verified using the measurement result.

Finally, Chapter 6 gives a summary of this thesis. The thesis ends with identifying potential directions for the future research.

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Chapter 2

4T CMOS Active Pixel Overview

This chapter gives a brief introduction of the 4T CMOS active pixel from different aspects. The chapter begins with the introduction of the pinned photodiode in Section 2.1. In Section 2.1, some different pixel structures are also introduced, including the 4T active pixel structure. Section 2.2 takes a look at some important image sensor evaluation parameters, some of which will be focused on in the following chapters of this thesis.

2.1 Device Physics of Pinned Photodiode

The pinned photodiode is the basic sensing element of a 4T active pixel. In this section, the photodiode and pinned photodiode will be introduced with respect to the device physics aspect. In addition, 4T pixel design is also introduced.

2.1.1 Photodiode

A photodiode is a specially fabricated pn-junction diode which has a large window to allow light to reach the sensitive part of the device. The basic function of a photodiode is to convert the incoming light signal into a current or a voltage signal. When a photon of sufficient energy (normally larger than the bandgap of silicon Eg) strikes the diode, the photon is absorbed and an electron-hole pair is generated. This is the well-known internal photoelectric effect. The photon energy is $E=h\upsilon=hc/\lambda$, where h is Plank's constant; υ is the frequency; c is the speed of light; and λ is the wavelength. Because incoming photons can only excite an electron if photon energy E is larger than E_g, the

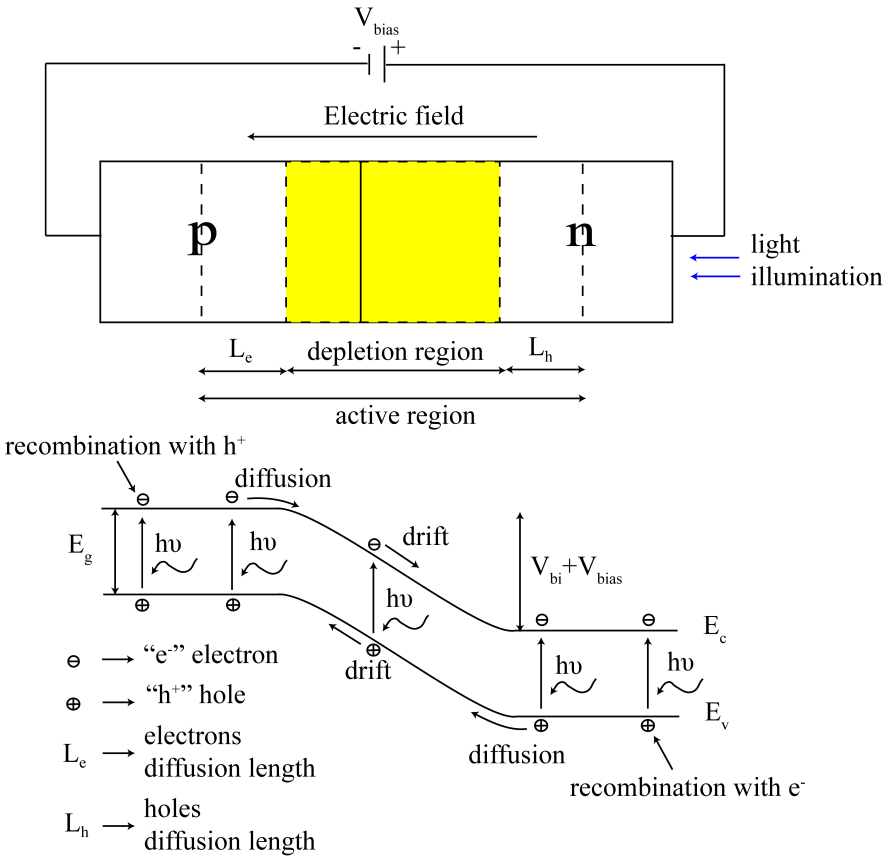

Figure 2-1: Photodiode energy band diagram for photon excitation.

maximum detectable wavelength can be calculated based on E_g as follows:

$$\lambda_{\max} = \frac{hc}{E_g} \tag{2-1}$$

The transport of the free electrons and holes is decided by the electric field. Photodiodes are used as photon detectors in image sensors when the pn-junction is reverse biased. The photoelectric current formed by transportation of the electrons is used to characterize the injection light intensity. This whole photon excitation process is illustrated in the energy band diagram of the photodiode in Figure 2-1 [2.1]. In a photodiode, generation of electron hole pairs by optical absorption can take place in different regions of the junction. In the pn- junction depletion region, the internal electric field sweeps the photon-generated electrons to the n-region, and the holes to p-region. This process results in a drift current that flows in the reverse direction from the n to the p region. Outside the depletion region, but within the length of the electrons/holes diffusion, the minority carriers of the region (electrons in the p-side, and holes in the n-side) will arrive in the depletion region by diffusion and then be swept by the electric field. This process results in a diffusion current that also flows from n to p region. For an electron-hole pair generated in the homogeneous region, the produced minority carrier cannot diffuse to the depletion region before recombining with a majority carrier. Thus, the active area is defined by:

$$W_{dep} + L_e + L_h = W_{active} \tag{2-2}$$

$$\begin{aligned} L_e &= \sqrt{D_e \tau_e} \\ L_h &= \sqrt{D_h \tau_h} \end{aligned} \tag{2-3}$$

where W_{dep} is the depletion region width; L_e is the electron diffusion length; L_h is the hole diffusion length; W_{active} is the active area width; D_e is the diffusion coefficient for the electrons; τ_e is the lifetime of the excess electrons; D_h is the diffusion coefficient for the holes; and τ_h is the lifetime of the excess holes. The total junction photocurrent density from n to p has been derived as (based on Equation 2.9 in [2.2]):

$$J_{ph} = qI_0[1 - \frac{\exp(-\alpha W_{dep})}{1+\alpha L_e}] + qn_{p0}\frac{D_e}{L_e} \quad (2\text{-}4)$$

where J_{ph} is the photon current of the pn-junction, and α is the optical absorption coefficient, which indicates the fraction of photons absorbed in an incremental slice of photon detecting material at a given wavelength. I_0 is the incident photon flux per unit area. Equation (2-4) is based on the assumptions that the surface n-layer is so thin that negligible photon absorption occurs there; and that all the photon carriers generated in the active region always contribute to the photon current (without recombination in that region).

The total current in a reversed photodiode also needs the addition of dark current, which is the reverse current of the pn-junction. The photocurrent of a normal photodiode is not strong, thus a charge integration based operation is used in many active pixel designs.

2.1.2 Pinned Photodiode

In 1980, to solve the interline transfer lag and kTC noise problem, a low lag structure was invented by Teranishi et al. [2.3]. This structure added a p^+ layer on top of the n-layer of a normal photodiode, and was first called a "pinned photodiode" by Burkey et al. [2.4]. Today, the pinned photodiode

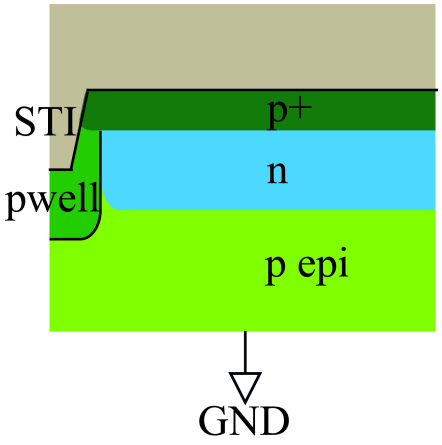

Figure 2-2: Cross-section of a pinned photodiode.

(PPD) is used as a photodetector structure in almost all CCD and CMOS image sensors. In 2014, a comprehensive review of pinned photodiodes was done by Fossum [2.5]. The cross-section of a pinned photodiode is shown in Figure 2-2. The pinned photodiode is composed of at least two implantations: a p-epi with n-doping covered with a shallow p^+ doping in the surface. Two pn-junctions form this sandwich structure. Both the p^+ layer and p-epi layer are grounded.

Compared with the photodiode, the pinned photodiode structure suppresses the surface generated dark current due the heavily doped p^+ layer partly pinned the Si-SiO2 interface. Thus, both PPD top and STI side wall interface traps can be filled, the total dark current of PPD can be decreased.

The other advantage of the PPD is the existence of the pinning voltage (V_{pin}) [2.6]. The pinning voltage is the voltage generated in the n-region when the two depletion regions of a p^+n junction and n-p-epi junction are situated back-to-back. When the whole n-region has been depleted, the PPD is emptied of charge. No image lag is left in the PPD when the charge is completely readout from the pixel. A band diagram of a PPD with a V_{bias} equal to the pinning voltage is shown in Figure 2-3.

In Chapter 3, more detail about pinning voltage estimation and extraction will be discussed.

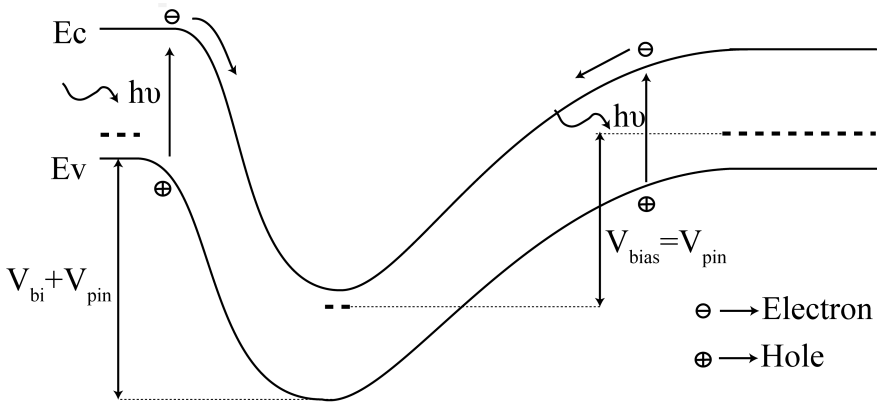

Figure 2-3: Band diagram of depleted pinned photodiode.

2.1.3 4T CMOS Active Pixel

In the previous sections the photodiode and pinned photodiode were introduced. In this section, the 4T pixel structure will be described. Depending on whether an amplifier is implemented in the pixel, the various pixel structures can consist of either a passive pixel sensor (PPS) structure or an active pixel sensor (APS) structure [2.7]. With the developments in CMOS technology, accommodating an amplifier transistor in the pixel is becoming possible, where APSs are the main choice for the CMOS image sensors.

The pinned photodiode was originally invented for interline transfer CCDs due to its low dark current and good blue response. With PPDs used in CMOS APS pixel, a 4T pixel is introduced based on the variation of the 3T pixel. The schematic of a 3T and 4T pixel are shown in Figure 2-4.

A normal 4T pixel timing diagram and the corresponding potential diagram of the PPD-TG-FD structure are shown in Figure 2-5. The transfer gate is “OFF” during the integration time. The photon generated electrons are accumulated in the PPD. Before the charge transfer, the FD node is reset. When the integration time has ended, the transfer gate is turned “ON” for charge transfer.

Based on the 3T APS pixel structure, except the PD is replaced by a PPD, a transfer gate and FD node are added. The transfer gate and FD node are used to decouple the reset and charge integration and transfer process, which is necessary for correlated double sampling (CDS) to remove the reset or kTC noise. Another advantage of the 4T pixel compared with the 3T is the electron-to-voltage conversion gain. The conversion gain of the 3T pixel is decided by the photodiode capacitance. Therefore, a tradeoff between the conversion gain and the size of photodiode needs to be considered. With the transfer gate decoupling, the conversion gain in the 4T pixel is only decided by the FD node capacitance, which could be optimized for specific applications. Since the TG decouples the photon sensing element from the readout node, the 4T pixel not only supports the rolling shutter operation like a normal 3T pixel, but it could also be used for the global shutter operation mode as well, which is important for high speed imaging application.

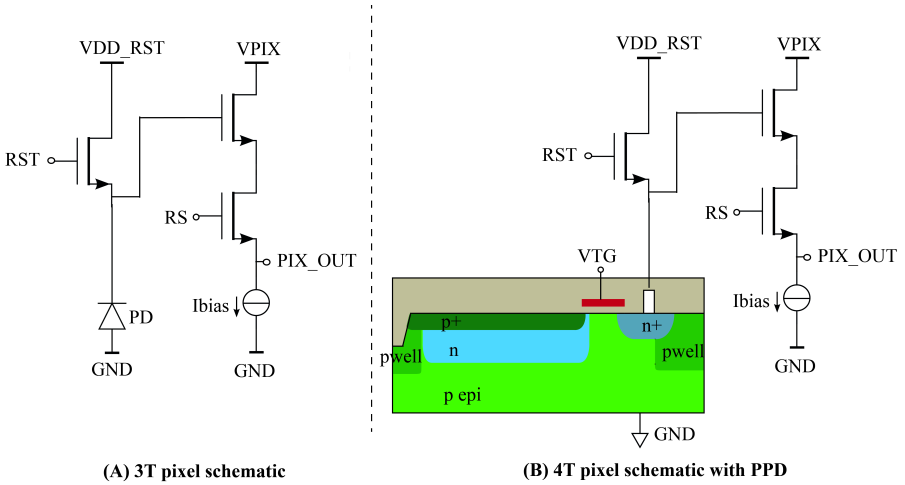

Figure 2-4: 3T and 4T pixel schematic.

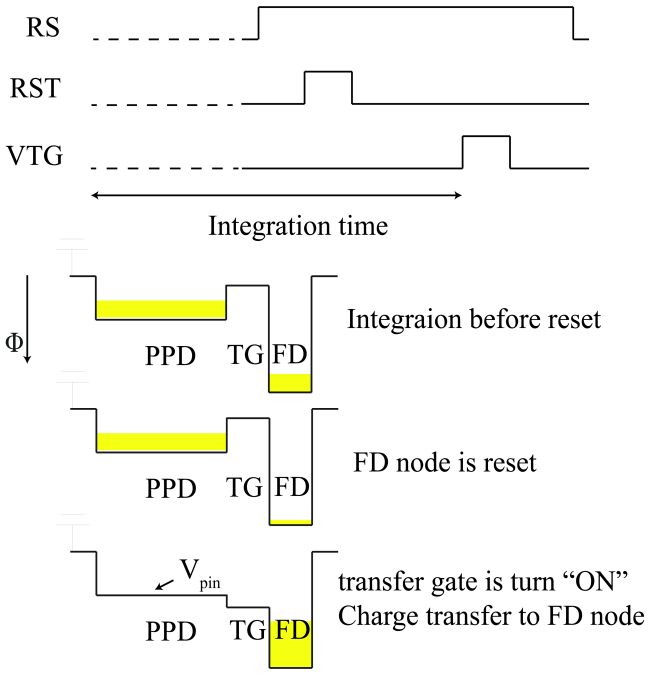

Figure 2-5: Timing diagram of 4T pixel operation and corresponding potential diagram of PPD-TG-FD structure.

Based on 3T and 4T pixel design, many pixel variations have been implemented for different applications. For example, the readout transistors (reset transistor, source follower, and row select transistor) can be shared by multiple pixels [2.8, 2.9] to increase the fill factor; adding more transistors or capacitors in pixel (5T,6T,8T…) for global shutter operation [2.10-2.12], as well as high speed [2.13, 2.14] and high dynamic range applications [2.15, 2.16]. Even though, there are many pixel design variations, the PPD-TG-FD structure is still used in most pixel architectures, therefore it is important for image sensor performance.

2.2 Characterization of the CMOS Image Sensor Pixel

To characterize a CMOS image sensor, a few different parameters are used. Many of the parameters are determined and/or limited by the pixel design. In this section, a few thesis related characterization parameters are introduced.

2.2.1 Dynamic Range and Signal-to-Noise Ratio

Dynamic range is defined as the ratio between the maximum signal of a pixel and its dark noise level. A dynamic range is typically expressed in decibel units as:

$$DR = 20\log(\frac{V_{sat}}{V_{dark}}) = 20\log\frac{N_{sat}}{n_{dark}}[dB] \tag{2-5}$$

where V_{sat} is the saturation signal level in volts, which is related to the well capacity or the total charge each pixel can hold during integration time. V_{dark} is the dark noise or noise floor in volts at the output. N_{sat} is the signal charge at saturation in electrons. n_{dark} is the pixel noise floor in electrons without illumination. An input referred noise in the charge domain is calculated by dividing the dark noise (in volts) by the image sensor's conversion gain. The noise floor level indicates the smallest detectable input signal of the sensor.

Dynamic range quantifies the ability of an image sensor to adequately image both high lights and dark shadows in a scene. Increasing the dynamic

range of image sensor is achieved either by increasing the largest input signal or decreasing the smallest detectable input signal.

The signal-to-noise ratio (SNR) is one of the most important parameters used to characterize the quality of the signal detection of the measuring image sensor system. In contrast to the dynamic range, the SNR of an image sensor is defined as the ratio between the signal and the corresponding noise at a given input level. The noise also includes the signal level related noise like photon shot noise. The SNR can be given by:

$$SNR = 20\log(\frac{N_{sig}}{n_{sig}})[dB] \tag{2-6}$$

where N_{sig} is the signal level in electrons; and n_{sig} is the total noise at the given signal level. At a low signal level, the readout noise is dominant [2.17]. The SNR for the readout noise limited range is proportional to the signal and produces a slope of 20dB/decade. With an increasing signal, the photon shot noise, which is equal to the square root of the signal, becomes the dominant noise source. In this situation, the SNR increases with the square root of the signal, for which the slope is 10dB/decade.

2.2.2 Full Well Capacity

The maximum output voltage swing of an image sensor can be limited either by the saturation of the readout circuit or by the full well capacity (FWC) of the PPD [2.18]. Therefore, the FWC of the PPD is one of the parameters that can determine the dynamic range of the image sensor. The FWC in the 4T pixel structure is defined as the maximum charge that can be stored on the PPD-TG structure. A few previous studies [2.18, 2.19] have proved that the FWC depends on the photon flux and low voltage of the TG for both the TG-depleted and TG-accumulated situation. Based on these works, Figure 2-6 illustrates a possible potential diagram of the PPD_TG structure under TG depleted and accumulated. If the low voltage of the transfer gate (VTG_L) is lower than the flat band voltage of the TG (V_{FB}), the transfer gate is biased in accumulation. When the PPD is empty, the accumulated electrons in the PPD will increase proportionally to the photocurrent and integration time until the potential difference of the

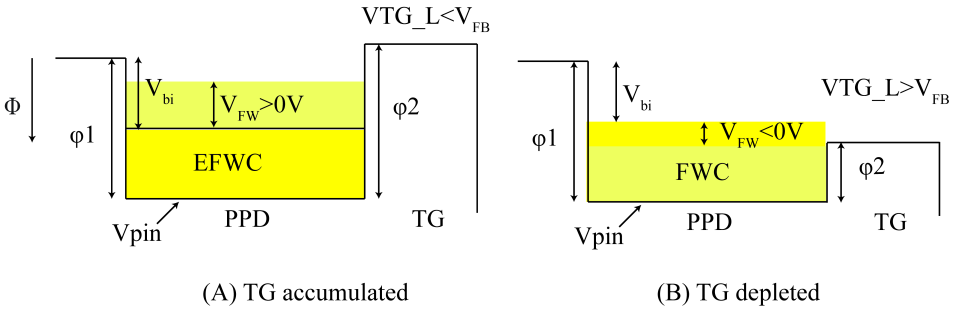

Figure 2-6: Potential diagram of a FWC in a PPD-TG structure: (A) TG- accumulated and (B)TG-depleted.

photodiode pn-junction is equal to the built-in potential V_{bi} of the pn-junction. With more electrons accumulated, the pn-junction becomes forward biased, and the forward current will compensate the input photocurrent. If the TG voltage is higher than the flat band voltage of the TG, the TG is depleted. The V_{FW} (the PPD voltage at the full well) could be higher than 0V or lower than 0V. Figure 2-6 (A) shows the situation of TG accumulated and the pn junction is forward biased, which means V_{FW}>0V. In this situation, the maximum full well capacity will be limited not only input photocurrent, but also the potential barrier of pwell (φ1). Figure 2-6 (B) shows TG depleted and V_{FW} below 0V situation. In this situation, the maximum FWC will limited by potential barrier of transfer gate (φ2). For both of these situations, the feed forward electron current will compensate the input photocurrent. All in all, in a certain range the FWC will increase with photon flux, but the minimum potential barrier surrounding the PPD will influence the maximum FWC value. Details of the FWC analysis will be given in Chapter 3.

2.2.3 Image Lag and Transfer Efficiency

For both CCD image sensors and 4T pixel CMOS image sensors, the charge transfer process is an important process for signal readout. In an ideal situation, all the accumulated electrons in the photon-sensitive element should be transferred and converted into a voltage signal for the image sensor readout. However, this is not the real situation. PPDs were originally invented to deal with the lag problem of photodiodes [2.3] in CCD image sensors. For 4T pixel CMOS image sensors, the charge transfer process is the process of photon-

generated electrons in the PPD being transferred to the FD node by the TG "ON". The electrons left in the PPD after the TG transfer process comes to an end, is called image lag. Transferring all the photon-generated electrons with a limited TG pulse is very difficult especially for low light and high speed applications. Since different input signals and/or PPD sizes could achieve very different image lag, comparing the absolute image lag in electrons is not an objective parameters for different pixel charge transfer performances characterization. Charge transfer efficiency (CTE) is defined as the ratio of successfully transferred electrons in one pixel during one transfer cycle to the total electrons need to be transferred. Charge transfer inefficiency (CTI) is the fraction of charge left behind after the TG transfer.

$$CTE=1-CTI \tag{2-7}$$

CTI is defined as the percentage of charge remaining in the photodiode after the transfer period in relation to the total charge needed to be transferred from the photodiode to the FD node, as shown in formula (2-8).

$$CTI=\frac{\text{number of electrons left in PPD}}{\text{number of electrons in PPD before transfer}} \tag{2-8}$$

The incomplete transfer of charge can lead to noise and image lag, which will deteriorate the image quality. Many scientific, medical and industrial CMOS image sensor applications require a large photon-sensitive area and/or short transfer time for high speed and/or low light level application image sensors. However, image lag is becoming a challenge for these applications [2.20-2.23]. Chapter 4 of this thesis will focus on the image lag problem in 4T pixels and pixel optimization. Detail analyses and measurement results about image lag will be given in Chapter 4.

2.2.4 Dark Current

For image sensors, the signal response should be the reflection of the incident light. However, in reality there is still a small amount of signal generated even without light input, which is called dark current. Dark current is an important parameter which characterizes the performance of an image sensor. Furthermore, many different mechanisms cause dark current

generation. At the location of the 4T pixel, the dark current in the 4T pixel mainly comes from the PPD and TG.

Sources of dark current generations are typically classified into three different categories in CMOS technology: dark carriers generated and diffused in the neutral bulk; dark carriers generated in the depletion region, and carriers generated due to presence of the surface states at the Si-SiO_2 boundary [2.24, 2.25].

Normally, a photodiode interface with a surrounding shallow trench isolation (STI) will result in surface leakage current. Thus, part of the dark current in a photodiode is proportional to the perimeter of the PD. To decrease the dark current in a PPD, a heavily doped p^+ layer and p-well are added at the interface with SiO_2 to decrease the dark current generated at the Si-SiO2 interface on the surface of the PPD and the surrounding STI interface (shown in Figure 2-4). Hole carriers in the p-doped region can be used to fill these traps and energy states at Si-SiO_2 interface [2.26]. Interface states that are filled with charge carriers no longer generate any dark current [2.27]. Except for the surface generated dark current, the thermal generated electrons in the depletion region of a PPD and the dark current generated in the neutral region will also contribute to the total dark current in a PPD. Both the dark current in the depletion region and in the neutral region are related to the area and perimeter of the PPD. Not only do the area and perimeter of the PPD influence dark current, but, as research [2.28] shows, the external angle of the shape of the PPD also influences the generation of dark current, since a higher concentration of defects typically occurs in the high stress photodiode area. With the angle increased, the dark current is decreased. A rounded corner may introduce less dark current while maintaining the higher fill factor. Besides, the electric field at the rounded corners will also be deceased.

The transfer gate is another major location for dark current generation in 4T pixels. The Si-SiO_2 interface state generated electrons under the gate is one of the origins of dark current in the TG. To suppress the dark current generated in the silicon interface under the TG, a small negative gate bias voltage on the TG is widely used to suppress the under gate Shockley-Read-Hall (SRH) surface electron generation [2.19, 2.29, 2.30]. The mechanism of dark current reduction with negative voltage applied is due to the accumulation of holes

under the gate with a negative biasing. However, if the negative biasing voltage is too large, the dark current will increase due to the trap-assisted tunneling leakage current induced by gate biasing [2.30]. Besides the interface state induced dark current, there is still another dark current possibly generated under the TG. There is a high electric field at the overlap region of PPD-TG, a high electric field could form due to the heavily doped of p^+ layer when the TG is switched on. This electric field could induce a hot carrier effect and impact ionization effect to generate dark carriers [2.31].

All in all, the dark current performance is an important parameter which could influence the pixel noise performance and the dynamic range of the pixel. The dark current performance of the pixel is substantially determined by the pixel process, design and operation.

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Chapter 3

Extraction of the Pinning Voltage and Full Well Capacity of 4T CMOS Pixels

The pinning voltage (V_{pin}) is one of the critical parameters, which define the pinned photodiode (PPD) structure. On one hand, it directly affects the charge transfer from the pinned photodiode to the readout node. On the other hand, in some extent it also can determine the full well capacity (FWC) of the PPD. This chapter gives an analysis and extraction method of the pinning voltage and full well capacity of 4T CMOS pixels, and also investigates more related parameters based on the designed test chip measurement results.

In this chapter, the physical model of the pinning voltage in pinned photodiode is described in Section 3.1. In Section 3.2, the measurement of the pinning voltage is presented and the designed test chip will be introduced (Section 3.2.1). The measurement details will be presented in Section 3.2.2 and the measurement results will be discussed in Section 3.2.3. In Section 3.3, a MOS model is applied on transfer gate analysis, based on the measurement result analysis, some TG related process parameters are extracted. In Section 3.4, the potential barrier dependencies are considered and proved. A few related secondary order effects are also explored. Both the technology and design optimization methods for the potential barrier of the transfer gate are considered. In Section 3.5, the concepts related to full well capacities are investigated.

3.1 Basic Physical Model of the Pinning Voltage

The performance of the image sensor strongly depends on the way in which the characteristics of the photon detectors are exploited and mastered. Nowadays, pinned photodiode (PPD) are used as photon detector in almost all CCD and CMOS image sensors. The advantages of a PPD include low noise, high quantum efficiency and low dark current [3.1]. After many years of developments, the technology and design of the image sensors are becoming mature. Still, defining, measuring and modeling its physical parameters are not straightforward [3.2], which is an important consideration in the pixel design and process optimization. In this section, a basic physical model is found, which can characterize the pinning voltage of the pinned photodiode. It is worth mentioning that the pinned photodiode structure is analyzed here independently, without considering the effect of the transfer gate and floating diffusion node.

As mentioned in Chapter 2, a normal pinned photodiode is composed of at least two implantations: a p-epi with an n-doping covered with a shallow p^+ doping in the surface. These two implantations form a sandwich structure with two pn-junctions. Both the p^+ layer and p_epi layer are connected to ground. When there is no reverse voltage applied across the PPD, these two pn-junctions are in thermal equilibrium state, which means the Fermi energy level is constant throughout the system. If a voltage is applied between the p and n-regions, it will no longer stay in an equilibrium state. The Fermi energy level will not be constant throughout the system. The reverse voltage applied to the PPD causes the quasi-Fermi level of the electron and hole to separate. The pinning voltage is the maximum potential differences which can be achieved between the p-epi and n-doping in pinned photodiode structure [3.1, 3.3]. There are a few references, which have also analyzed the pinning voltage of the PPD [3.3-3.6]. In the ideal case, considering a pnp structure, the pinning voltage as the name implies, is the voltage which makes the neutral region of the n-type to disappear. The cross section of this p^+-n-p_epi structure is shown in Figure 3-1. The doping profile and corresponding potential diagram, which are simulated based on a Gaussian distribution, are shown in Figure 3-2. The following definitions will be used: L_{p1} stands for the width of the depletion region in p-region (p^+n junction), and the L_{n1} is the

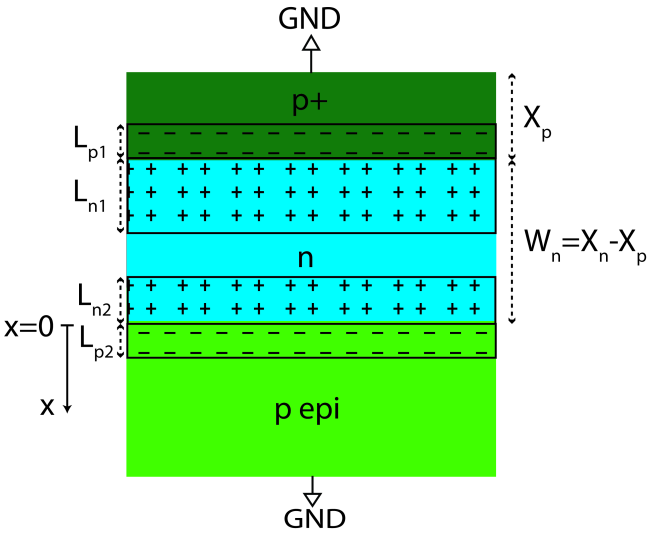


Figure 3-1: Schematic diagram of the pinned photodiode cross section structure.

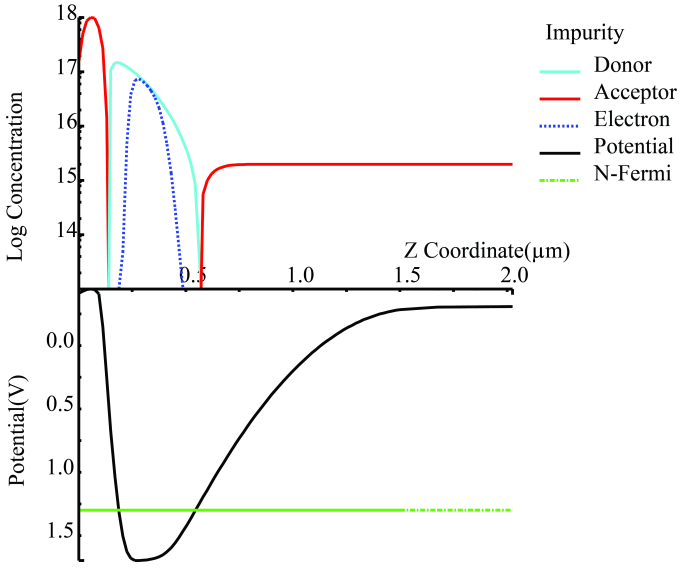


Figure 3-2: Doping profile and corresponding potential diagram of pinned photodiode – Gaussian distribution.

depletion region width in n region. L_{n2} and L_{p2} are the depletion region widths of the n-p_epi junction in the n- and p- region respectively. X_p is the implantation depth of the p^+ pinned layer. Lastly, W_n is the width of the n-doping region, which is equal to X_n-X_p. Here X_n is the depth of the n-implantation. With an increasing voltage connected to the n-doping region, both the reverse voltage for two pn-junctions in the PPD and the space region widths (L_{p1}, L_{p2}, L_{n1}, L_{n2}) will also increase. When L_{n1}+ L_{n1}=W_n, the reversed voltage is equal to the pinning voltage (V_{pin}), and the space region in the two pn-junctions touch each other. Then the entire n-doping region is depleted and no neutral region exists at all in the n-region.

The doping concentration in p^+ pinned layer (N_{p+}) is much larger than the doping concentration in n-doping region (N_n). Therefore, a one-sided junction is used here as an approximation for the p^+ ion implantation. V_{bi1} (the built-in potential of the p^+n junction) and L_{n1} (the depletion region width of the p^+n junction extending into n-doping area) can be expressed as the following [3.7]:

$$L_{n1} = \sqrt{\frac{2\varepsilon_s (V_{inj} + V_{bi1})}{qN_n}}$$
$$V_{bi1} = \frac{kT}{q} \ln\left(\frac{N_{p+} N_n}{n_i^2}\right) \tag{3-1}$$

which ε_s is the semiconductor dielectric constant; T is the absolute temperature; k is Boltzmann constant; n_i is the intrinsic carrier concentration. The other junction n-p_epi also extends its space charge region into the n-region, and the space charge region width is L_{n2}. Here the linearly graded junction hypothesis is utilized [3.7]. The linearly graded junction means that the impurity concentration in the p_epi layer is constant, but the net n-type doping concentration near the metallurgical junction is approximated as a linear function of the depth. In addition, α is defined as gradient of the impurity concentration. Here the metallurgical junction X_n is defined as the reference of x axis. And the direction of x axis in the silicon depth direction. The space charge density $\rho(x)$ is given by:

$$\begin{aligned} \rho(x) &\approx q(\alpha x + N_{p\_epi}) \qquad -L_{n2} < x < 0 \\ \rho(x) &\approx -qN_{p\_epi} \qquad\qquad 0 < x < L_{p2} \end{aligned} \tag{3-2}$$

where N_{p_epi} is the doping concentration of the p_epi. The Poisson equation can be written as Eq. (3-3). Considering the boundary conditions in the n-region, the electric field is given by Eq. (3-4). Equation (3-5) gives the electric field in the p-region.

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{dE(x)}{dx} \tag{3-3}$$

$$\begin{aligned} E_n &= \int \frac{q(\alpha x + N_{p\_epi})}{\varepsilon_s} dx \qquad -L_{n2} < x < 0 \\ &= \frac{q}{\varepsilon_s}(\alpha x^2 + N_{p\_epi} x + N_{p\_epi} L_{n2} - \alpha L^2_{n2}) \end{aligned} \tag{3-4}$$

$$E_p = \frac{-qN_{p\_epi}}{\varepsilon_s}(x - L_{p2}) \qquad 0 < x < L_{p2} \tag{3-5}$$

Where E_n is the electric field in n region of this junction; E_p is the electric field in p region of this junction. Moreover, when x=0, at the metallurgical junction the electric field will be same for the n-and p-region. The relation between L_{p2} and L_{n2} is given as:

$$L_{p2} = (L_{n2} - \frac{\alpha L^2_{n2}}{N_{p\_epi}}) \tag{3-6}$$

Furthermore, using Eq. (3-3), the potential in the n-and p-region can be found. Equation (3-7) for the p-region will be derived. Since the p-epi layer is connected to ground, the potential in L_{p2} is zero.

$$\begin{aligned}\phi(x) &= -\int E_p(x)dx = \int \frac{qN_{p\_epi}}{\varepsilon_s}(x - L_{p2}) \qquad 0 < x < L_{p2} \\ &= \frac{qN_{p\_epi}}{\varepsilon_s}(\frac{x^2}{2} - L_{p2}x) + \frac{qN_{p\_epi}}{2\varepsilon_s}L^2{}_{p2}\end{aligned} \tag{3-7}$$

$$\begin{aligned}\phi(x) &= -\int E_n(x)dx \qquad -L_{n2} < x < 0 \\ &= \int \frac{q}{\varepsilon_s}(\alpha x^2 + N_{p\_epi}x + N_{p\_epi}L_{n2} - \alpha L^2{}_{n2})dx \\ &= \frac{q}{\varepsilon_s}(\frac{1}{3}\alpha x^3 + \frac{1}{2}N_{p\_epi}x^2 + (N_{p\_epi}L_{n2} - \alpha L^2{}_{n2})x) + \frac{qN_{p\_epi}}{2\varepsilon_s}L^2{}_{p2}\end{aligned} \tag{3-8}$$

Using Eqs. (3-4) and (3-7), the potential in the n-region can be calculated as Eq. (3-8). If x=0, the potential in the p-and n-region will be same. Due to the p-epi layer connected to ground, the built-in potential of this junction will be the potential in the n-region ($x=-L_{n2}$) (Eq. (3-9))

$$\begin{aligned}V_{bi2} &= \left|\phi(x = -L_{n2})\right| = \frac{q}{\varepsilon_s}(\frac{2}{3}\alpha L^3{}_{n2} - \frac{1}{2}N_{p\_epi}L^2{}_{n2}) + \frac{q}{\varepsilon_s}N_{p\_epi}L^2{}_{p2} \\ V_{bi2} + V_{inj} &= \frac{q}{\varepsilon_s}(\frac{\alpha^2 L^4{}_{n2}}{N_{p\_epi}} - \frac{4}{3}\alpha L^3{}_{n2} + \frac{1}{2}N_{p\_epi}L^2{}_{n2})\end{aligned} \tag{3-9}$$

When $V_{inj}=V_{pin,}$ then $L_{n1}+L_{n2}=W_n$. Based on the equations derived above, such as Eqs. (3-1) and (3-9), the pinning voltage is only depending on the technology parameters. These parameters are all defined by the implantation dose (Q_n, Q_p) and implantation energy (E_n, E_p).

It is worth mentioning that in this section, the pinned photodiode is treated as a simple p-n-p structure and not the actual three-dimensional device is analyzed in this section. On one hand, in a real devices, the pinning voltages are not only determined by processing parameters, but also modulated by both the PPD width and PPD length [3.8]. On the other hand, this structure will connect with the transfer gate and floating diffusion in the pixel. All these factors should be considered for a more realistic model.

3.2 Measurement of the Pinning Voltage

As mentioned in the beginning of this chapter, the pinning voltage is an important physical parameter for the pixel performance, and described by a basic physical model, it is related to the processing parameters. From the perspective of the user or pixel designer, it is difficult to know all the processing parameters details. Even when using these details, because of the various doping profile approximations, physical models will differ. These models therefore have to be verified and improved. Consequently, the method to measure the pinning voltage measurement should be considered and/or developed. Without a proper measurement, further related research can only be limited to theoretical modelling. The pinning voltage is the parameter related to the PPD structure, which is difficult to access from outside of the pixel. The solution proposed in [3.9] is an effective measurement technique that can be used to characterise a PPD-TG-FD structure. This method is also approved by other pinning voltage related research [3.2, 3.10]. In this thesis, the same measurement principle [3.9] are introduced, implemented, and further analysed.

In this section, first the test chip design is introduced, which is used to measure and characterize the 4T pixels. Next the pinning voltage measurement will be presented.

3.2.1 Test Sensor Design

The pixel is the most important component of an image sensor. To better understand the pinned photodiode 4T pixel and to analyse its different parameters, a test image sensor chip with 80 different pixels was designed. A similar sensor design was implemented in two distinct technologies to understand the impact of the technology on the pixel characteristics. Both technologies are commercial 0.18μm pinned photodiode CMOS image sensor foundry processes. Process A and process B represent these two processes. The example pixel and its parameter variations (PPL, PPW, TGL, TGW) in this test chip are presented in Figure 3-3. The pinned photodiode and transfer gate design are varied by means of length, width variations. All these parameter permutations and combinations form nearly 80 different pixel

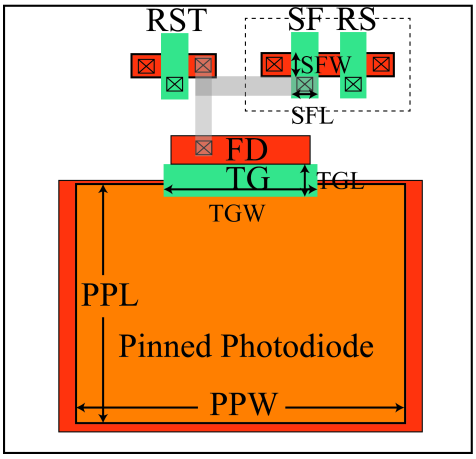


Figure 3-3: Pixel layout and parameter variations.

designs. The pixel array is divided into 80 different regions with different pixel parameter combinations. Each pixel type design contains 10×8 pixels. In order to satisfy all parameter options, the pixel pitch is 15µm. Except for these parameter variations, a few special pixel designs are changed based on the special shape of the pinned photodiode and transfer gate. The details will be introduced in the corresponding section of the thesis. Figure 3-4 shows a simplified schematic diagram of a 4T nMOS pixel and its column readout chain, including a column gain amplifier, a sample and hold circuit and a column buffer. The column gain amplifier can adjust the DC level of the output signal and one can increase the gain to suppress the input referred

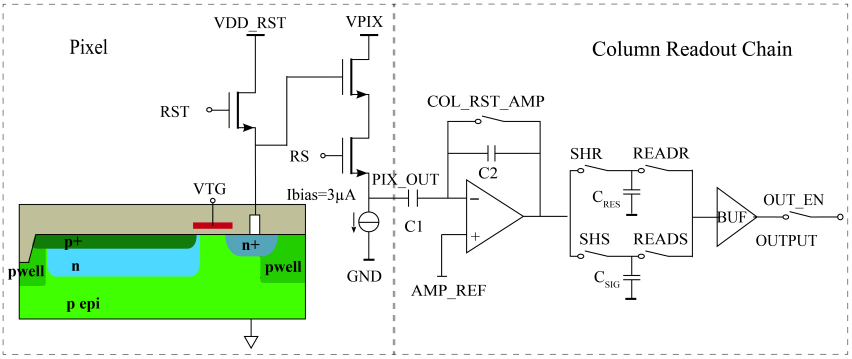


Figure 3-4: Schematic diagram of the pixel and the column readout chain.

noise. The closed loop gain is determined by C1/C2, where C1 is the input capacitor and C2 is the feedback capacitor of the column gain amplifier, respectively. In order to maximize the input swing of the column readout chain, and measure the pixel full well capacity, in this test chip the column amplifier closed loop gain is fixed to 1 (C1=C2). The sample and hold circuit is used as a correlated double sampler to remove the reset or kTC noise. Due to the large dynamic range and high open loop gain requirements, a folded cascade amplifier is chosen as the column amplifier. The COL_RST_AMP is the reset switch of the amplifier. After the FD node is reset, the reset level is available in PIX_OUT and the COL_RESET_AMP is also "ON" to reset the amplifier. The reference voltage VREF and both the reset noise and offset noise of every stage are then stored in a subsequent capacitor (C_{RES}) (SHR is "ON") and later cancelled by the CDS operation. After the reset sampling, the transfer gate in the pixel is opened and the charge packet is transferred from the PPD to the FD node, where it is converted into a voltage and buffered by the source follower. The signal is available on AMP_IN. Thus the difference between the pixel signal and pixel reset level (ΔV) will be available on the output of the amplifier. The switch SHS will sample this AMP_REF+ΔV onto capacitor C_{SIG}. The signals stored on these two capacitors (C_{SIG}, C_{RES}) will be output column by column, which is controlled by the READR and READS switches. The column buffer increases the driving capability of the output signal to avoid a considerable attenuation and fluctuation of the signal. The OUT_EN switch is designed to isolate the sample and hold capacitor from the multiplexing bus.

Figure 3-5 and 3-6 shows two microphotos of the two 4T pixel test chips implemented in process A and process B respectively. These two chips are based on the same architecture.

Chip A (process A) has a larger pixel array of 80(rows)×160 (columns), which contains both n-type and p-type pixels. The difference between both options: the source follower and row selection change from nMOS to pMOS. The same sized pixel array (80×80) is produced by both the n- and p-type pixel. In total, there are two sub-pixel arrays, each of which contains 80 different pixel designs. Because pMOS and nMOS have opposite "row select" pulses, an inverter is needed between the pMOS pixel and nMOS array. Then

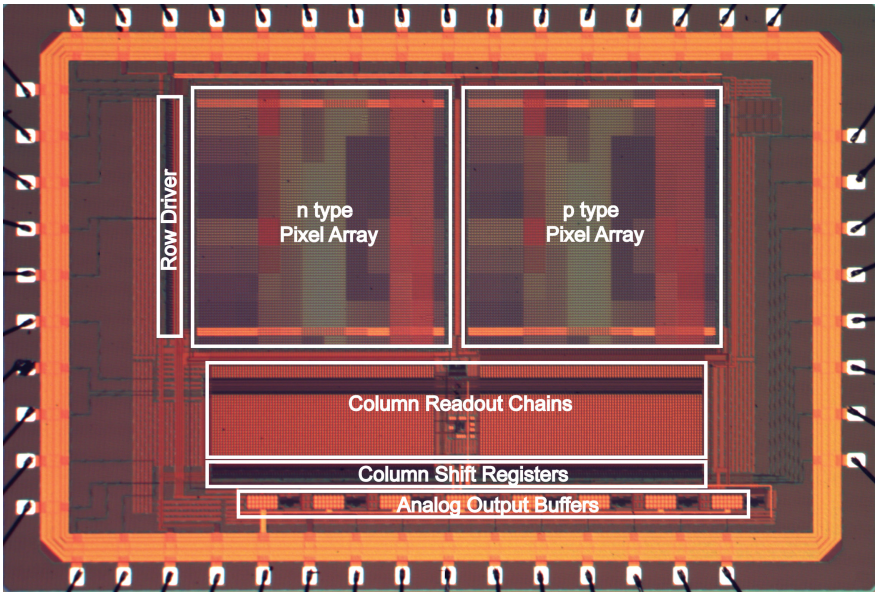


Figure 3-5: Micrograph of the test sensors in process A.

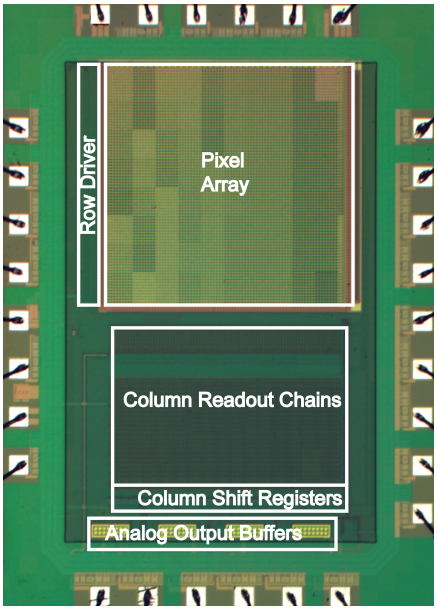


Figure 3-6: Micrograph of the test sensors in process B.

a column digital block connects these two sub-pixel arrays, the design is made such hat both nMOS and pMOS pixels can readout with the same on-chip electronics. The chip B (process B) only has an n-type pixel. The pixel array is 80(row)×80(column). The size of the chip A is 4.62mm×3.15mm; the size of chip B is 2.3mm×3.15mm.

The operation principle of both sensors is a rolling shutter. The row and column addressing circuitry is realized by a shift register structure. The imager operation timing is controlled by an external FPGA.

3.2.2 Pinning Voltage Measurement Method

This measurement works in a completely dark environment. There is no light input, no photon-generated electrons are produced in photodiode. The signal consists of the electrons injected from the drain of the reset transistor. The reason, we use injected electrons instead of photon-generated electrons is because the injected electron number can be directly controlled by a voltage input. In this way, the relationship between the PPD potential and the number of collected/injected electrons can be revealed.

The timing diagram for the PPD parameter extraction based on the pixel schematic shown in Figure 3-4, is illustrated in Figure 3-7. Compared to the normal pixel readout timing, the node VDD_RST is changed from a DC power connection to a pulse. Both the high voltage (VDD_RST_H) and low voltage level (V_{inj}) can be adjusted externally. The whole pinning voltage measurement can be divided into two phases: the injection and readout phase. In the injection phase, the node VDD_RST is biased to a relatively low voltage (V_{inj}). This voltage defines the injection potential for the PPD and the FD node. To inject electrons into the FD node and PPD, both the RST and TG are switched to the “ON” state. After the injection, the transfer gate is closed to keep the injected electrons stored in the PPD. The readout phase takes place like a normal imaging readout where the VDD_RST is changed to a high voltage level. The reset transistor RST is switched “ON” again to reset / empty the FD node. After the reset level is sampled on the capacitance C_{RES}, the transfer gate is opened. The electrons stored on the PPD are now transferred, converted into a voltage and this signal is stored on the capacitance C_{SIG}.

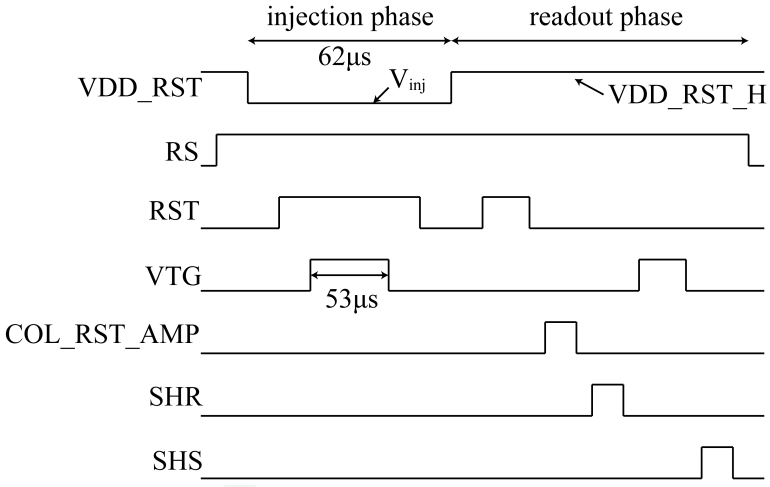


Figure 3-7: Main control timing for the PPD pinning voltage measurement.

To make sure the electron potential in the PPD is the same as this injection voltage [3.2], some details need to be taken into account for a proper measurement operation. First, as Figure 3-7 shows the transfer gate pulse (VTG) should be enclosed by the VDD_RST and RST pulse. Additionally, the VTG pulse duration should be long enough for a proper charge injection. Secondly, a bidirectional digital switch should be added for the VDD_RST signal. If the FPGA produced digital control signal is "0", the low voltage reference will be connected to VDD_RST to all of the pixels. Otherwise, when the control signal is "1", the high voltage reference will be connected to VDD_RST. This bidirectional digital switch design, which connected with VDD_RST, should consider the load capacitance from the VDD_RST metal line in all columns. The measurement will take place multiple times while varying V_{inj}, which is changed from 0V to 2.5V or even higher.

3.2.3 Physical Description of the Pinning Voltage Measurement

In this measurement, the V_{inj} will gradually increase to characterize a few potential steps in the PPD-TG-FD structure. According to the changing trend of the readout number of electrons, the curve can be divided into four different regions, and a few important parameters can be extracted from it. Figure 3-8 plots two similar pixel pinning voltage measurement results for the

two different fabrication processes. The four region divisions are shown in Fig. 3-8 based on the measurement result of process A.

For the curve of process A, the signal readout from PPD is constant when V_{inj} is small. Increasing the injection voltage until $V_{inj}=V_{b\_processA}$ (the first keen point of the curve), the output begin to decrease with the V_{inj} increasing further. This means when $V_{inj}< V_{b\_processA}$, the output signal is saturated by readout out chain, FD node, or TG "OFF" potential barrier. In our case, since the same FD node and readout chain can achieve larger readout signal level for larger PPD, the limitation is the TG "OFF" potential barrier. This flat part is the "TG "OFF" Barrier Leakage region. When the injection phase is changed to the readout phase, the number of electrons held in the PPD will be readout. If the transfer gate cannot "produce" a sufficiently high barrier (when TG is "OFF") to prevent an overflow of charge, part of the electrons held in the PPD will be lost during the FD node reset. The voltage of the TG potential barrier can be characterized as $V_{b\_processA}$, which can be extracted from the first knee-point of the measurement curve. V_b is defined as the

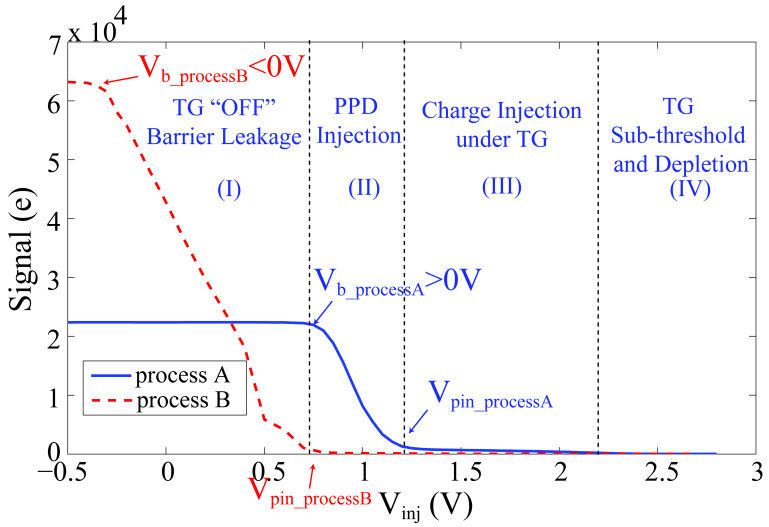


Figure 3-8: Pinning voltage measurements (for processes A and B) can be divided into four regions: (I) TG "OFF" Barrier Leakage; (II) PPD Injection; (III) Charge Injection under TG; and (IV) TG Sub-threshold and Depletion.

potential difference between the lowest potential of the barrier beneath the transfer gate (when TG is "OFF") and the PPD electron potential in equilibrium state (V_{inj}=0V). In this region ($V_{inj} < V_{b\_processA}$) with the increasing injection voltage from 0V to V_b, fewer electrons are injected into the PPD. Even with fewer injected electrons, the readout electrons are constant. The potential barrier limits the number of electrons, which can be held. When the transfer gate "OFF" barrier is equal to V_{inj}, no more electrons are lost during the FD node reset. Figure 3-9 (A) and (B) present a potential diagram of this "TG "OFF" Barrier Leakage" region for process A.

In our process B measurement, due to the different technology and structure, V_b is negative, which means the transfer gate "OFF" barrier is sufficiently high for the equilibrium state. A larger V_b means a lower TG "OFF" barrier potential, more leakage of electrons to the FD node and a lower FWC in the PPD. Except for the positions of the different parameter (e.g. V_b, V_{pin}), the curve shapes are the same for both process A and B. The following analysis in this chapter will be given based on process A.

With a further increase in the injection voltage, when $V_b < V_{inj} < V_{pin}$, the measurement characterizes the "PPD Injection" region. In this region, all the injected electrons in the PPD can be recollected by signal readout. No overflown electrons are lost during the FD node reset operation. The number of injected electrons in the PPD is reduced with an increase in the injection voltage (V_{inj}).

When $V_{inj}=V_{pin}$, the entire PPD structure is depleted. The potential difference between the p-well and n-doping in the PPD structure cannot be enlarged. No electrons can be directly injected into the PPD structure. However, if the transfer gate voltage is high enough, in the "Charge Injection under TG" region the charge will be injected underneath the transfer gate and then kicked back into the PPD during the transfer gate "ON-OFF" transition period [3.11, 3.12]. The number of kicked-back charges is very limited compared with the "PPD Injection" region.

Before the transfer gate is completely depleted, there is also a sub-threshold part, resulting in fewer electrons being injected under the TG. The injection voltage is increased until the transfer gate is fully depleted, at which point no

electrons can be injected anymore under the transfer gate. This region is defined as the “TG Sub-threshold and Depletion” region. These two regions “Charge Injection on TG” and “TG Sub Threshold and Depletion” potential diagrams are also described in Figure 3-9 (C) and (D). These two regions will be presented in more detail in Section 3.3.

All in all, the “TG OFF Barrier Leakage” region is determined by how many electrons can be held in the PPD, i.e, by the TG “OFF” potential barrier. Thus, from this region, the TG “OFF” potential barrier can be extracted and investigated. The other three regions are determined by how many electrons can be injected from the FD node into the PPD and under the TG, which happens during the injection phase of the measurement. From the “Charge Injection under TG” and “TG Sub-threshold and Depletion” regions, the TG “ON” state can be characterized.

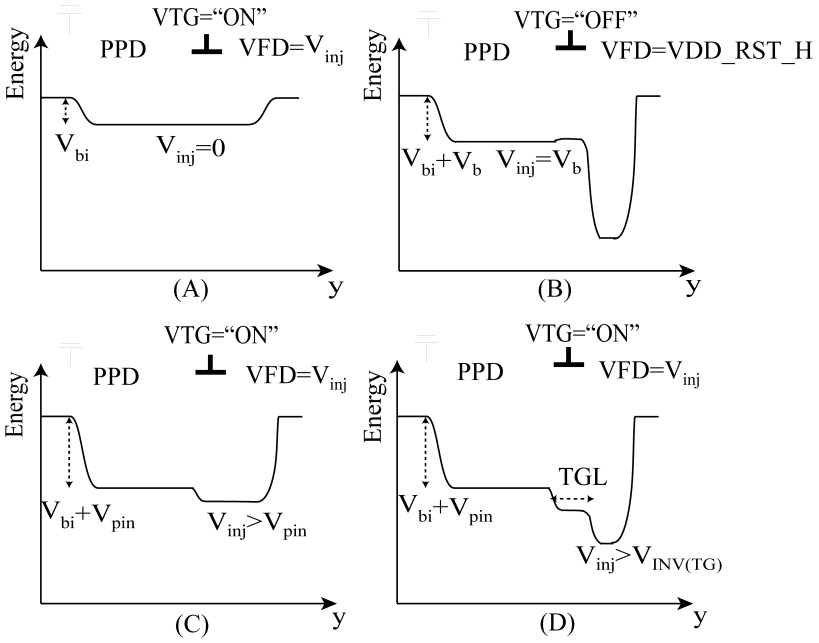


Figure 3-9: Different potential diagram states during the pinning voltage measurement of process A.

3.3 Transfer Gate Related Parameters Extraction

As mentioned above, the pinning voltage measurement is a powerful tool for pinning voltage characterization. Not only the pinning voltage but also other related device parameters can be extracted from this. All in all, this method can characterise the PPD-TG-FD structure. In this section, the surface potential-based transfer gate analysis will be given.

3.3.1 MOS Model in PPD-TG-FD Structure

The PPD-TG-FD structure can be seen as a special MOS transistor. In the injection phase, the electrons are injected into the PPD and the TG channel. From the direction of the electron movement, in the injection phase, the FD node can be treated as the source of the MOS transistor, and the transfer gate can be treated as the gate of transistor. According to the law of conservation of potential and charge, for an MOS transistor, the following basic formulas can be written:

$$V_G = V_{ox} + \phi_s + \phi_{ms} \tag{3-10}$$

$$Q_G' + Q_{SS}' + Q_{SD}' = 0 \tag{3-11}$$

where V_G is the applied gate voltage; V_{ox} is the voltage across the oxide; ϕ_s is the surface potential of the silicon under the transfer gate; and ϕ_{ms} is the work difference of the gate material-semiconductor. In this situation, the n^+ poly is used as the gate material, and

$$\phi_{ms} = -\frac{E_g}{2} - \phi_{fp} \tag{3-12}$$

where E_g is the silicon band gap equal to 1.12eV; and ϕ_{fp} is the difference (in Volts) between the intrinsic Fermi level (E_{Fi}) and Fermi level (E_F) of the silicon under the TG gate. Q_G' is the charge density on the poly gate; Q_{SS}' is the charge introduced by the traps in the oxide per unit area; and Q_{SD}' is the space charge density per unit area of the depletion region under the gate. Here

the inversion layer charge is neglected (before the strong inversion) because it is quite small compared to the charge in the depletion region. Then we have:

$$V_{ox} = \frac{Q_G{}'}{C_{ox}} = \frac{\left(\left|Q_{SD}{}'\right| - Q_{SS}{}'\right)}{C_{ox}} \tag{3-13}$$

$$V_{FB} = \phi_{ms} - \frac{Q_{SS}{}'}{C_{ox}} \tag{3-14}$$

Equation (3-10) can be expressed as (3-15) [3.13] using (3-13) and (3-14):

$$V_G = \frac{(2q\varepsilon_s N_a)^{\frac{1}{2}}}{C_{ox}} \phi_s^{\frac{1}{2}} + V_{FB} + \phi_s \tag{3-15}$$

where C_{ox} is the gate oxide capacitance, V_{FB} is the flat band voltage of TG; This relationship is valid before the structure reaches inversion. Thus the inversion condition will be the boundary condition in this situation. The injection voltage (V_{inj}) is applied to the "source" (FD), and considering the substrate bias effect, the inversion condition is:

$$\phi_s = 2\phi_{fp} + V_{inj} \tag{3-16}$$

furthermore, in the strong inversion situation, the surface potential will stay pinned to $2\phi_{fp} + V_{inj}$, varying only logarithmically [3.14]. According to Eq. (3-15) and the inversion condition, a diagram of the relationship between ϕ_s and V_G is plotted in Figure 3-10 (supposing $N_a=10^{17}$ cm^{-3}, the oxide thickness is 80Å, and $Q_{SS}{}'$ is neglected). The linear part of the surface potential curve (dashed blue line) is based on Eq. (3-15), which is the depletion and weak inversion region. The flat part of the surface potential curve (black line) is the strong inversion part. The surface potential of the inversion point depends on the FD node injection voltage (V_{inj}). Different injection voltages result in different curves. For a given injection voltage, the inversion point surface potential is defined by Eq. (3-16); from the cross point of V_{inj} and the blue dash line the corresponding TG threshold voltage and V_{inv} can be found. In

the pinning voltage measurement, for a given high transfer gate voltage, the injection voltage is increased step by step from 0V. When V_{inj} is small, the corresponding working region is the strong inversion. Since electrons from the FD node can be injected into the channel, the channel potential will be equal to V_{inj}. With a further increase in V_{inj}, the surface potential will increase further to maintain the inversion state until it reaches the threshold inversion point. At this point we define the injection voltage as V_{inv}. If there is a further increase in V_{inj}, the transfer gate will turn into the weak inversion state. At the weak inversion to depletion state turning point, the given V_{TG} cannot support enough balanced charges Q_G for the inversion layer electrons, and nearly no electrons can be injected under the transfer gate. Bringing the inversion condition Eq. (3-16) into the Eq. (3-15) allows Eq. (3-17) to be derived as:

$$V_{th} = \frac{(2q\varepsilon_{si}N_a)^{\frac{1}{2}}}{C_{ox}}(V_{inv} + 2\phi_{fp})^{\frac{1}{2}} + V_{FB} + V_{inv} + 2\phi_{fp} \qquad (3\text{-}17)$$

In Figures 3-10 and 3-11, there are two situations given for the transfer gate high voltage. When the transfer gate voltage is equal to V_{t1}, the corresponding injection voltage, which makes TG turn into the inversion point, will be V_{inv1}. If $V_{inv1}<V_{pin}$, with the increase in V_{inj}, the number of output electrons will be

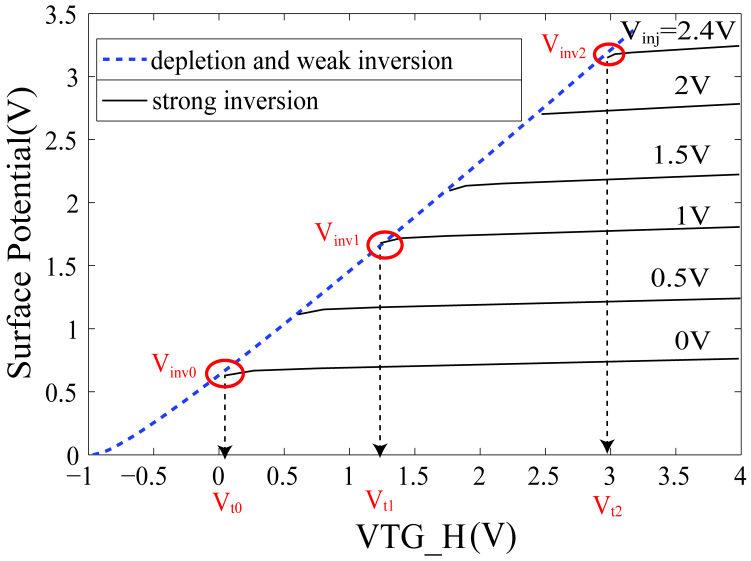


Figure 3-10: Surface potential vs. transfer gate high voltage for different FD injection voltage.

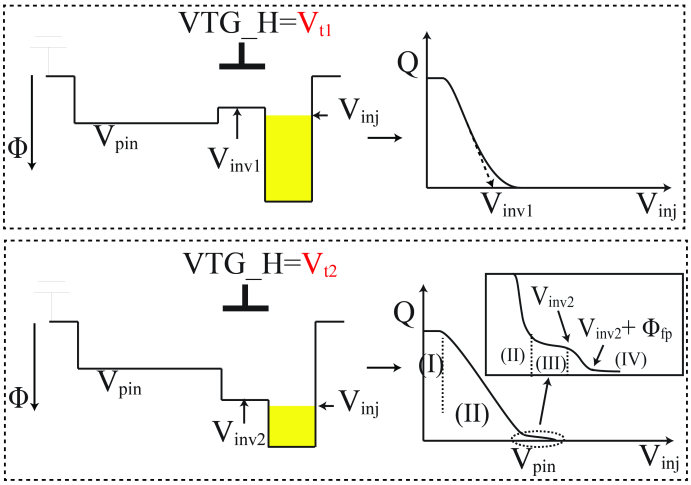


Figure 3-11: Under different transfer gate high voltage situations.

decreased until V_{inj} reaches the V_{inv1}. The "Charge Injection on TG" region will disappear and V_{pin} cannot be extracted from the measurement. With the increase in V_{inj}, the number of output electrons will be decreased until V_{inj} reaches the V_{inv1}. If the TG voltage is high enough, V_{inv} and V_{pin} will differ slightly and V_{inv} will be extracted more easily. In the case that the transfer gate voltage is equal to V_{t2}, the corresponding injection voltage, which turns TG into the inversion point, will be V_{inv2}. If $V_{inv2}>V_{pin}$, we can extract both the V_{pin} and V_{inv2}. With an increase in V_{inj}, fewer electrons will be injected into the PPD through the transfer gate. The knee point will therefore be V_{pin}. When the injection voltage is larger than the pinning voltage, the electrons will be injected under the transfer gate only. When V_{inj} is increased further, the output will decrease slowly, until it is close to V_{inv2}. Because the injection current is saturated in the strong inversion region, the surface potential of channel is also nearly constant. A further increase in the injection voltage will cause the transfer gate state to change into the weak inversion. With a further increase of V_{inj} from $V_{inv2} + \phi_{fp}$, the TG region will be depleted, and no electrons can be injected under the transfer gate.

3.3.2 Measurement and Verification

Figure 3-12 shows the process A measurement results for different transfer gate high voltages, ranging from 2.1V to 3.5V. The different TG high voltages

correspond to different inversion voltages V_{inv}. These different V_{inv} can be extracted from Figure 3-12. For the largest transfer gate voltages (here VTG_H>2.9V), V_{inv} is easier to identify because a large transfer gate voltage makes a larger difference between V_{inv} and V_{pin}. The result is that V_{pin} has a smaller effect on V_{inv}. When 2.5V<VTG_H<2.9V, V_{pin} is very close to V_{inv}. In this situation, it is difficult to identify an accurate inversion point from one single measurement. At the inversion point and for the same pixel, the number of electrons injected under the transfer gate will be the same for different transfer gate voltages. Thus also the inversion point for lower transfer gate voltages can be found. With a further decrease in the transfer gate voltage such as VTG_H=2.3V, the threshold inversion point of the TG will not be influenced anymore by the pinning voltage. This is the case shown in Figure 3-11 (top plot VTG=V_{t1}). In this situation, the slope of the linear part of "PPD injection region" can also be used to find the inversion point as Figure 3-11 shows. It is worth mentioning that in process A the barrier height is considerably low (large V_b). If the transfer gate voltage further decreases, V_{inv} will approach V_b, preventing an accurate V_{inv} being found with this method. The voltage difference ϕ_{fp} can be calculated from both the inversion point (V_{inv}) and sub-threshold point $V_{inv}+\phi_{fp}$ in the plot. Here ϕ_{fp} is around 0.45V. Therefore the doping concentration N_a equals to 5.5×10^{17} cm^{-3}, as can be calculated from Eq. (3-18).

$$\phi_{fp} = \frac{kT}{q}\ln\frac{N_a}{n_i} \tag{3-18}$$

The extracted ϕ_{fp} value has been approved by different pixel design measurement. This value is not influenced by design but only decided by process. However, existence of region (III) is one condition to accurate extract ϕ_{fp}. To further verify proposed extraction method, the VTG_H and channel surface potential relationship, which is similar with extraction method mentioned in [3.2] can be used for verification. Using the inversion conditions Eq. (3-16), the surface potentials (ϕ_s) for different transfer gate voltages can be calculated and is plotted in Figure 3-13. The relationship between ϕ_s and V_G should also fit Eq. (3-15). By using the calculated value for N_a, the

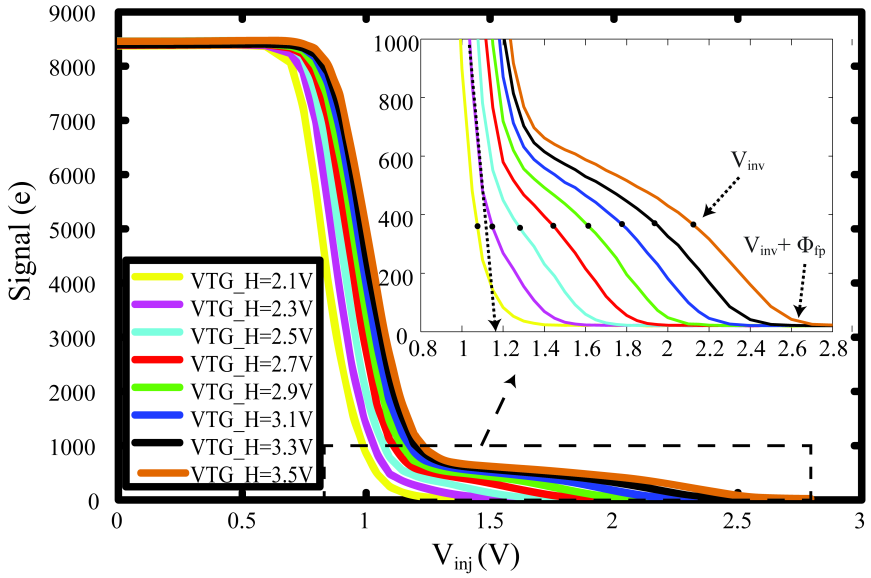


Figure 3-12: Different transfer gate high voltages measurement results, all obtained from the same pixel.

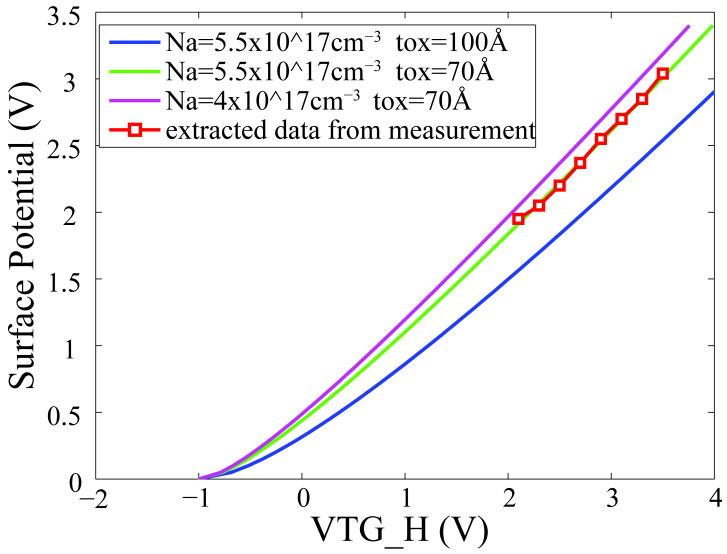


Figure 3-13: Measured transfer gate voltage vs. surface potential for fitting of the processing parameters.

corresponding oxide thickness $t_{ox} = \varepsilon_{ox} / C_{ox}$ can be derived (ε_{ox} is the dielectric constant of oxide layer). Using all these extracted process parameters, and according to Eq. (3-17), the threshold voltage $V_{to} \approx 0.85V$ ($V_{inj}=0V$) can be derived. Figure 3-13 shows that all the measured data points for different transfer gate voltages fit to the green line very well, being the result of Eq. (3-15) using $N_a=5.5\times10^{17}\,cm^{-3}$, $t_{ox}=70Å$. The extracted parameter t_{ox} is also consistent with the information provided by the foundry, which proves the validation of the TG model and the proposed parameter extraction method.

3.4 Potential Barrier of the Transfer Gate (TG)

3.4.1 Potential Barrier Characterization

As mentioned in Section 3.2, the two different processes implemented have different potential barrier heights, which are shown in Fig. 3-8. From this comparison, it can be found that the curve shapes will be different in the low injection voltage part. In the ideal situation, when the injection voltage is increased ($V_{inj}<V_{pin}$), which means that the injection potential is decreased and that the corresponding number of injected electrons should be decreasing as well. However, the number of readout electrons for process A is constant until $V_{inj}=V_b$. While for process B, the number of electrons is already decreasing from $V_{inj}=0V$. From this comparison it can be derived that $V_{b\_processA} >0V$ and $V_{b\_processB} <=0V$. Figure 3-14 also illustrates this situation. When the transfer gate is "OFF" and the PPD has been filled with electrons, the FD node will be reset to a high voltage level. The potential of the PPD should equal to V_{inj}. Yet for process A, due to the barrier height of the transfer gate, the electrons will be overflowing into the FD node when $V_{inj}<V_{b\_processA}$, until the V_{inj} is increased to $V_{b\_processA}$. The measurement result of process B looks similar with result shown in [3.2]. $V_{b\_processB}\approx-0.4V$. When $V_{inj}<0V$, the PPD is forward biased. The forward current of PPD [3.15] could influence the full well capacity of PPD. FWC can be limited by the forward current. But in this pinning measurement, due to the very large injection current and enough injection duration, the maximum measured electrons are still limited by TG potential barrier or pwell isolation barrier. Then the knee point of curve

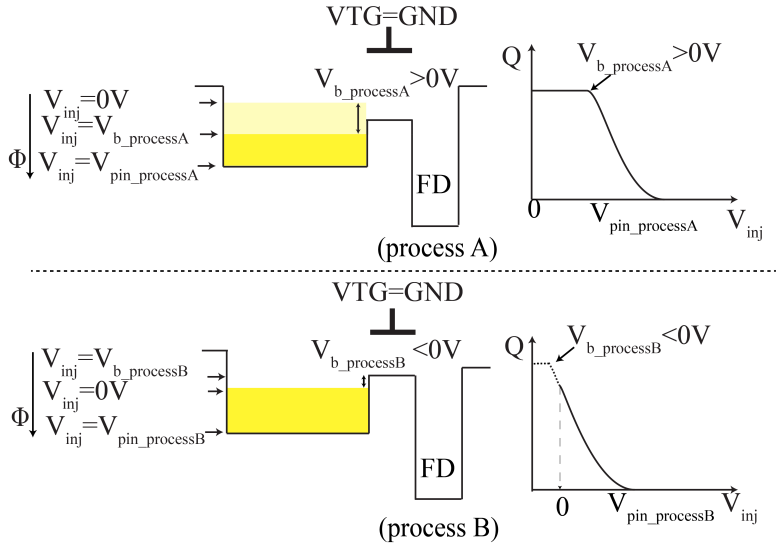


Figure 3-14: The potential diagram analysis for both process A and process B.

($V_{b\_processB}$) can characterized the lower one of two barriers. The bottom plot in Fig. 3-14 (process B) also illustrates the situation (supposing TG potential barrier is lower than isolation barrier of pwell). For process B, from V_{inj} =0V, increasing the injection voltage will directly cause the number of collected electrons to decrease. This means that the potential barrier is high enough to hold all electrons in PPD when V_{inj}=0V. Decreasing the injection voltage further below 0V allows the first knee point to be found in the negative direction ($V_{b\_processB} \leq 0V$). All in all, the V_b is the potential difference between the surface potential of the barrier beneath the transfer gate (when TG is "OFF"; VTG=VTG_L) and the PPD potential of the equilibrium state (V_{inj}=0V). The two different technologies could have different process parameters such as under-gate doping concentration and/or the oxide thickness, resulting in two measurements exhibiting the different V_b. A larger V_b means a lower TG "OFF" barrier potential, more leakage electrons and less FWC in the PPD.

To measure the value of V_b, the method mentioned above is quite limited. The flat part of the curve shown in Figure 3-14 (process A) could also be due

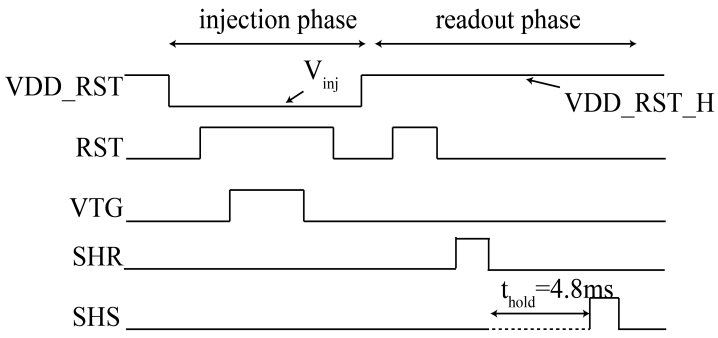


Figure 3-15: Timing diagram of the feed-forward measurement.

to the limitation of the FD node or of the readout circuit voltage swings. If the FWC of the pixel is not limited by the PPD but limited by the FD node, the first knee point will not be defined by the potential barrier V_b, but will be decided by the FD node. To overcome the limitation of the FD node, another solution is proposed to measuring V_b for different pixel designs. Compared with the pinning voltage measurement, the new solution of V_b measuring does not measure the electrons injected into the PPD, but measures the leakage electrons collected in the FD node. This method is known as the feed-forward measurement, which is also proposed in [3.16].

The timing diagram based on the pinning voltage measurement is adjusted. The new timing diagram for the feed-forward measurement is illustrated in Figure 3-15. The transfer gate is only open for the charge injection from the FD node to the PPD, but not open for readout. The time delay between the reset sample and signal sample will be increased from μs to ms, and it is called holding time. Here our measurement used 4.8ms as the holding time (t_{hold}). The final output signal measured will consist of the electrons jumping from the PPD to the FD node during the holding time. The variable in this measurement also will be the VDD_RST pulse low voltage level. The measurement result is shown in Figure 3-16. The potential diagram, which explains this measurement, is plotted in Figure 3-17.

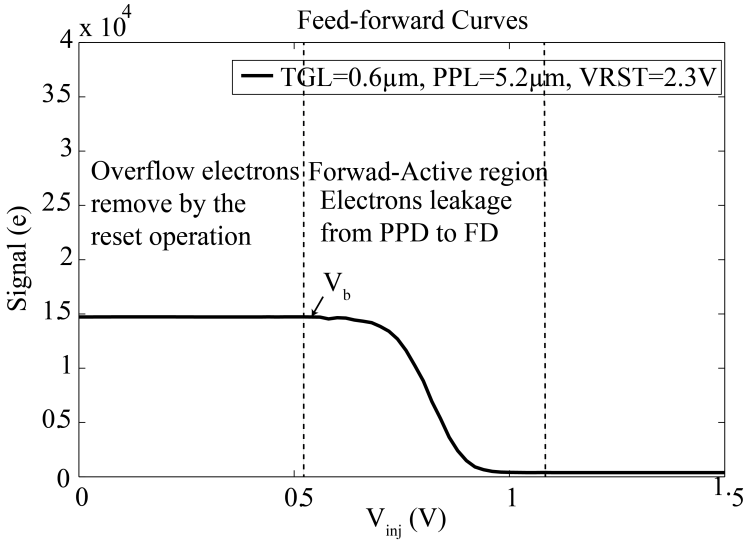


Figure 3-16: Feed-forward voltage measurement curve example.

Figure 3-17 (A) describes the potential diagram state, which has a flat band voltage (V_{FB}) applied to the transfer gate (process A). In this state, the surface potential ϕ_s is 0V, and the built-in potential between the PPD and TG is set when V_{inj}=0V. When a voltage larger than V_{FB} is applied on TG, the energy band of the MOS structure will be bent. For p substrate, V_{FB} <0V, V_{FB} means positive voltage applied, then ϕ_s (Fermi potential difference between substrate and the under gate surface silicon) will be increased. In our process A, when the TG voltage is grounded, the potential under the transfer gate is lower than the potential of the PPD part when V_{inj}=0V. The injected electrons cannot be held in PPD since a reset pulse will remove the overflow of electrons. Until the injection voltage is increased to V_b, the potential of the PPD will be nearly the same with the transfer gate barrier potential. Figure 3-17 (B) describes this situation. Because of the V_{inj}<V_b part, the actual electrons injected into the PPD is constant for different injection voltages, hence the measured number of electrons that escape to the FD node without charge transfer is also the same. V_b can also be found in the feed-forward measurement shown in Figure 3-16.

With a further increase of the injection voltage (V_{inj}>V_b), the potential of

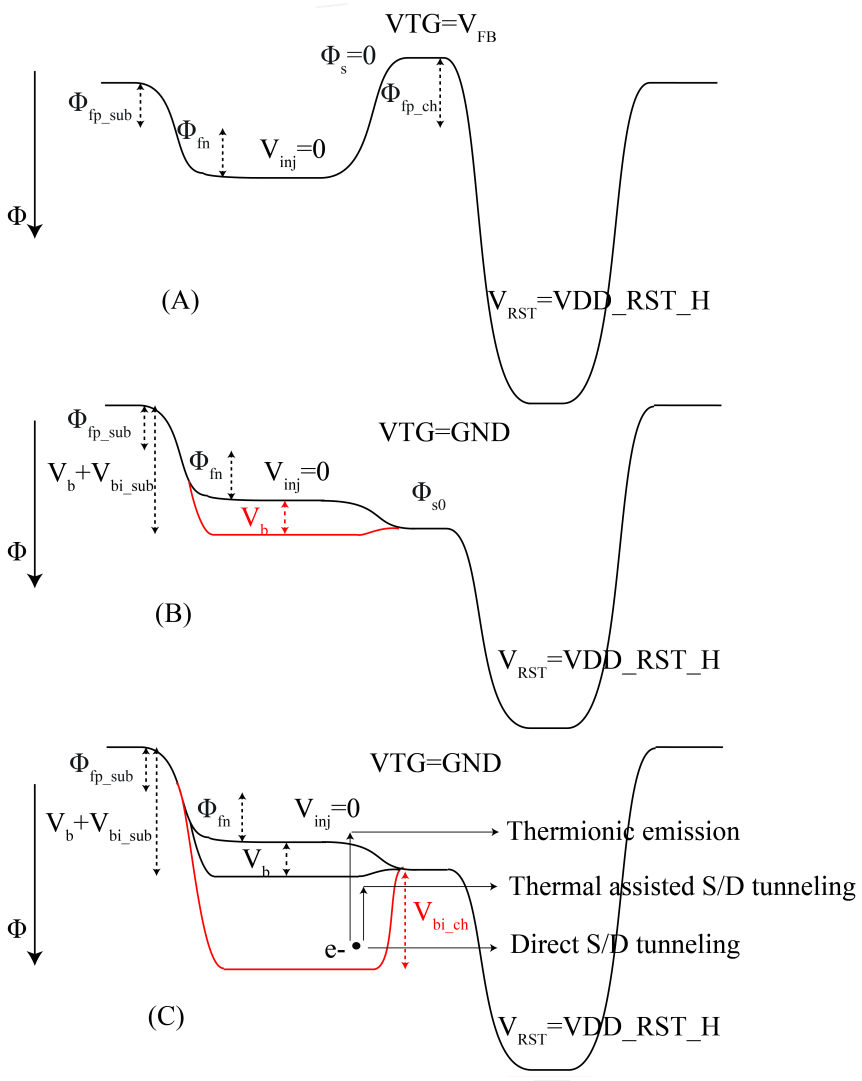


Figure 3-17: Potential diagram to explain feed-forward measurement of process A.

the PPD after injection will be lower than the surface potential of the transfer gate. Since the potential difference is still not big enough, there are also electrons that are feed-forwarded into the FD node. The number of feed-forward electrons will decrease with the injection voltage increase. In this

situation, as shown in Figure 3-17 (C), there are three distinct mechanisms [3.17] to be considered here for the feed-forward effect.

The first mechanism is the thermionic emission. Carriers are thermally excited in the PPD, and then jump over the TG potential barrier. This effect will depend on the total number of electrons being held, temperature, and the electron potential. On one hand, both increasing the potential barrier distance (V_{inj}-V_b) and decreasing temperature will decrease the possibility of electron emission. On the other hand, because the photodiode well depth (V_{pin}) is limited, with an injection voltage increase, the total number of electrons being held also decreases. Therefore with the injection voltage increasing, the thermionic emission of electrons will disappear.

Secondly, with thermally assisted S/D tunnelling, carriers are thermally excited and then tunnelling slightly beneath the top of the potential barrier. Both thermionic emission and thermally assisted S/D tunnelling as their names implied, have a strong temperature dependence.

The third one is direct S/D tunnelling. In this situation, the PPD-TG-FD structure can be seen as an npn-bipolar transistor. The PPD is the emitter of the transistor, and the entire transistor is working in forward active operating mode. The electrons from the PPD are injected across the junction into the "base"(silicon beneath the gate). Some of the electrons will diffuse across the base region into the "collector" (the FD node), where the electric field of the TG-FD junction will sweep the electrons into the FD node. Of course, some of the diffusion current from the PPD will recombine with the majority hole under the gate region; therefore, the rate of the recombination depends on the length of the transfer gate. The injection voltage is increased until the potential differences between the PPD and transfer gate surface potential is again equal to the built-in potential (V_{bi_ch}). An equilibrium state is then achieved in this PPD-TG junction. "V_{BE}" will be the V_{bi_ch}-(V_{inj} -V_b). The forward bias current of this junction before equilibrium can be simply written as:

$$I = I_s \exp\left(\frac{q(V_{bi\_ch} - (V_{inj} - V_b))}{nkT} - 1\right) \tag{3-19}$$

in which n is the ideality factor, V_{bi_ch} is the built-in potential of the n-doping channel junction. If V_{bi_ch} -(V_{inj}-V_b) is large, then n≈1; if V_{bi_ch} -(V_{inj}-V_b) is small, then n≈2. I_s is the reverse saturation current of this pn- junction. From the Eq. (3-19), it can be found that the leakage current decreases with a decrease in V_{inj}.

Except for the diffusion current, the sub-threshold current is also the most important component of the leakage current in this situation. The result is [3.18]:

$$I_{d,sub} = I_0 \frac{TGW}{TGL} \exp(\kappa VTG\_L - V_b) \frac{q}{kT} \tag{3-20}$$

in which $I_{d,sub}$ is the sub-threshold current; I_o is a proportional constant of the sub-threshold current, κ is the gate coupling coefficient of about 0.7, and VTG_L is the transfer gate "OFF" voltage, V_b is TG potential barrier height. T is the temperature; k is Boltzmann constant. All these feed forward current components result the feed-forward electrons. The electrons will feed forward to FD node until the potential differences between electrons in PPD and TG "OFF" potential barrier is achieved V_{bi_ch}.

3.4.2 Potential Barrier Dependency

Based on the theoretical analysis above, if the TG "OFF" potential barrier height is only determined by the technology, then $V_b = V_{so} - V_{bi\_ch}$. However, in our measurement, V_b is much larger than expected, which means the TG "OFF" potential barrier is lower than expected. Thus there are a few practical design parameters and secondary effects influencing the potential barrier.

The DIBL (Drain-Induced Barrier Lowering) effect: regardless of the normal 4T pixel operation, the pinning voltage or the feed-forward voltage measurement operation, electrons will be generated in or injected into the PPD. In order to readout out the electrons, the FD node has to be reset to a high voltage (VDD_RST_H), which means a low potential to empty non-signal electrons before the charge transfer. In addition, the direction of electrons movement in the readout phase will be from the PPD to the FD node. Therefore, in this phase, the FD node can function as the drain of the MOSFET. In a MOSFET, the drain potential can also influence the gate barrier potential, which is called the DIBL effect. Similarly, VDD_RST_H

applied on FD node will partly control the TG “OFF” potential barrier.

DIBL is a mechanism to describe a drain bias causing by lowering of the source channel junction barrier [3.19]. This effect occurs in short channel devices. With the transfer gate length reducing and VDD_RST_H increasing, the depletion region of the FD node moves closer to the depletion region of the PPD. The two electric fields will interact with each other, and the charge in the channel cannot be totally regulated by the gate voltage. For a short transfer gate length, reducing the potential barrier that electrons in PPD must surmount in the transfer gate “OFF” state, leads to higher leakage currents. Due to the effect of DIBL, the threshold voltage will decrease while the high reset voltage increases. The most extreme situation of DIBL is when the two depletion regions touch each other, creating a conduction path without the influence of the gate bias. Figure 3-18 shows the DIBL effect potential diagram, increasing the high reset voltage (VDD_RST_H) will increase the space charge region of the TG-FD junction, which will decrease the potential barrier for a short transfer gate pixel. Finally, the full well capacity will be decreased owing to the DIBL effect. It is worth mentioning that normally, without considering the DIBL effect, increasing the reset voltage can increase the FWC by increasing the voltage swing of the FD node. However, if the FD node capacity is large enough for the PPD size, and the transfer gate length not long enough, then the FWC is determined by the PPD size, pinning voltage and potential barrier. Consequently increasing the reset voltage will decrease the FWC due to the DIBL effect. The measurement result also proves this. Figure 3-19 shows the pinning voltage measurement for a relatively small PPD size (PPL=3.2μm) and short transfer gate length

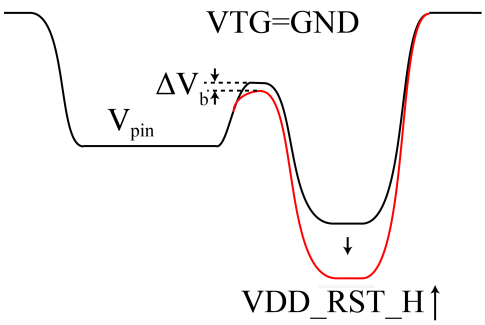


Figure 3-18: DIBL effect potential diagram.

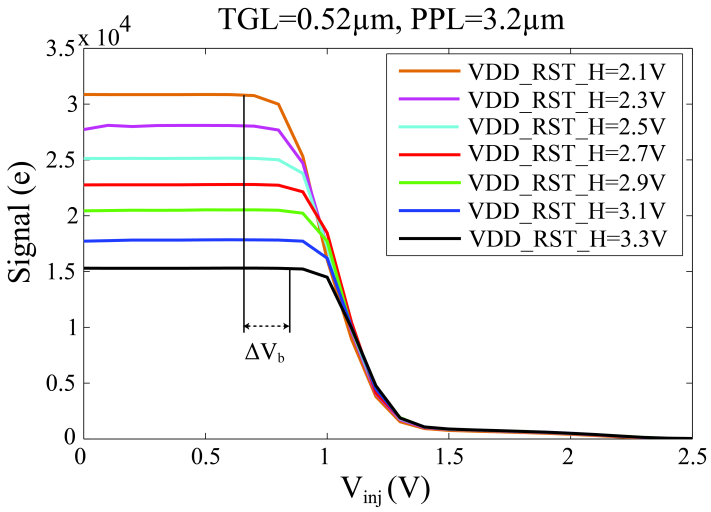


Figure 3-19: Different reset voltage pinning voltage measurements for DIBL effect.

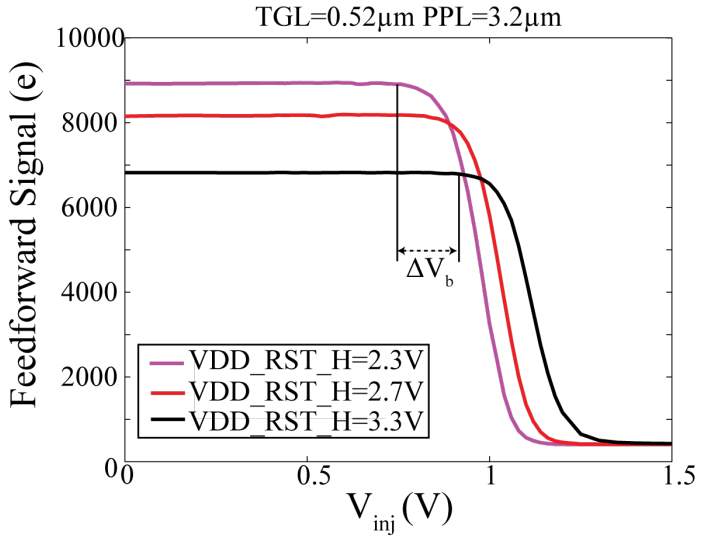


Figure 3-20: Feed-forward voltage measurements for the DIBL effect under different reset voltages.

(TGL=0.52μm) pixel, for the different high reset voltage levels. The result shows that when reset voltage is decreased from 3.3V to 2.1V, the potential barrier V_b is increased about 0.2V, and the FWC value in electrons is nearly doubled. For a relative larger PPD, the FD node capacity limits the measured FWC. Especially if the reset voltage is lowered further, the FD node will is quickly become saturated. The result is that the real V_b cannot be measured. As mentioned above, in this situation for the feed-forward voltage measurement, only leakage electrons are measured. Figure 3-20 is the feed-forward measurement for a PPL=3.2μm with the same transfer gate size and PPD width. The measurement result shows that, the V_b position is the same for corresponding reset voltage, compared to Figure 3-19. Therefore, a larger reset voltage will lower the potential barrier, and lead to an increased V_b.

Short transfer gate effect: as aforesaid in the section on the DIBL effect, the short transfer gate can cause the DIBL effect. Thus it is clear that, like the MOS transistor, in the PPD-TG-FD structure, the transfer gate length also can have an effect on the performance. In this section, the influence of the transfer gate length on the potential barrier will be discussed.

In Section 3.3, in the ideal situation it is assumed that only the inversion surface electrons in the channel under the gate are considered for gate voltage controlling. However, in reality the space charge area of the PPD-TG and FD-TG junctions will extend into the channel region, and then the actual channel length will be smaller than the designed one. Both $Q'_{SD(\max)}$ and the transfer gate threshold voltage will be decreased. For a long transfer gate length situation, the junction extension effect does not have much influence. However, for the short channel design, this extension could make the effective channel length to disappear in the extreme situation, which results in a punch-through of the transfer gate. On one hand, different high reset voltages will change the valid channel length, threshold voltage, and potential barrier of the transfer gate. On the other hand, for the same high reset voltage, decreasing the transfer gate length can also reduce the potential barrier height. Figure 3-21 plots the potential diagram of the PPD-TG-FD structure for the short transfer gate (TGL') and long transfer gate (TGL), which show the different potential barrier heights. Figure 3-22 is the feed-forward voltage measurement result for the same PPD size, high reset voltage, high and low transfer gate voltages, but different transfer gate lengths. From this result, it can be shown

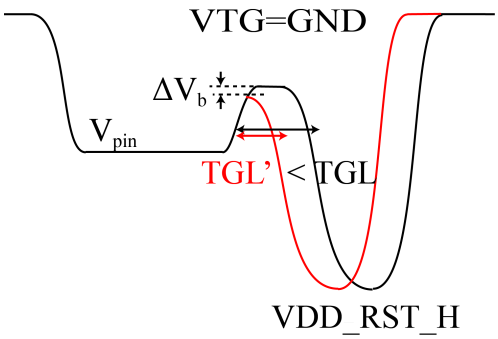


Figure 3-21: Potential barrier influenced by the transfer gate length.

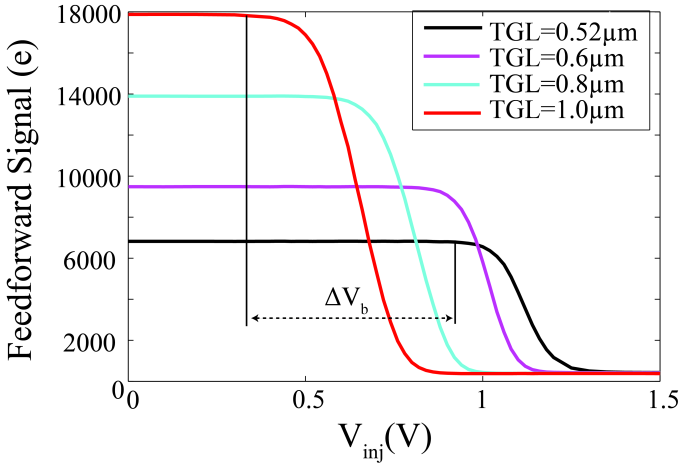


Figure 3-22: Potential barrier height improved by an increased transfer gate length.

that when the transfer gate length increases from 0.52µm to 1µm, the potential barrier height is increased (V_b is decreased from around 1V to 0.4V).

Narrow transfer gate effect: Figure 3-23 shows the cross section of the transfer gate structure in the direction of its width. If a transfer gate voltage is applied, a depletion region will be generated. In the ideal situation, the charge in the depletion region is. $Q_{SD} = qN_a x_{dt} WL$ (x_{dt} is the width of the depletion region, W and L are the gate width and length). Nevertheless, the actual depletion region in the channel is always larger than what is usually assumed

for a one-dimensional analysis; this is due to the existence of fringing fields [3.20]. The extra charge introduced in the depletion region is ΔQ_{SD}, which can be calculated as Eq. (3-21):

$$\begin{aligned} \Delta Q_{SD} &= qN_a L x_{dt}(\xi x_{dt}) \\ Q_{SD} &= qN_a x_{dt} WL + \Delta Q_{SD} = qN_a x_{dt} WL(1+\frac{\xi x_{dt}}{W}) \end{aligned} \tag{3-21}$$

where ξ is the parameter for the extension region. Suppose the total shape of the extension parts is the half round, then $\xi = \frac{2}{\pi}$. The extensions of the two extra depletion regions under the field oxide also contribute to the charge required for the compensation of the transfer gate voltage. If the transfer gate width (TGW) is big enough, the extra depletion regions can be neglected compared with the depletion region under the gate. However, with a decrease of the TGW, these depletion region extensions cannot be neglected anymore. Here, the extra depletion region charges introduced by overlap between TG and p^+ layer of PPD are neglected. Since this charge component is also proportional to W, the conclusion will not be changed.

Calculating the potential barriers introduced by different transfer gate widths should result in finding the surface potential for the zero gate voltage $\Delta\phi_{s0}$. Here the VTG is constantly grounded. For TGW1 >TGW2, based on (3-15), the following formulas are valid:

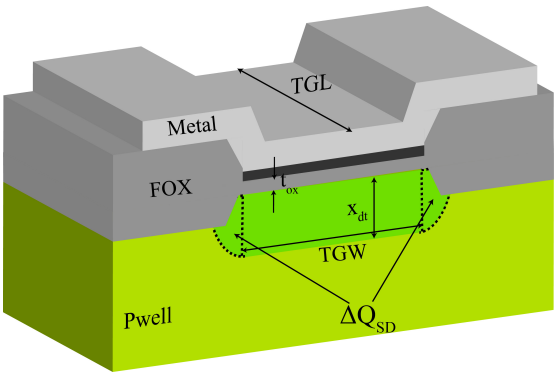


Figure 3-23: Cross section of the transfer gate in the width direction.

$$TGW1:\phi_{S0\_TGW1}+V_{FB}+\frac{qN_a x_{dt1}}{C_{ox}}(1+\frac{\xi x_{dt1}}{TGW1})=0 \tag{3-22}$$

$$TGW2:\phi_{S0\_TGW2}+V_{FB}+\frac{qN_a x_{dt2}}{C_{ox}}(1+\frac{\xi x_{dt2}}{TGW2})=0 \tag{3-23}$$

$$\begin{aligned} x_{dt1}&=\left(\frac{2\varepsilon_s\phi_{S0\_TGW1}}{qN_a}\right)^{\frac{1}{2}} \\ x_{dt2}&=\left(\frac{2\varepsilon_s\phi_{S0\_TGW2}}{qN_a}\right)^{\frac{1}{2}} \end{aligned} \tag{3-24}$$

Substitute Eq. (3-24) into the Eqs. (3-22) and (3-23), and comparing between these two equations, it can be derived that:

$$\begin{aligned} &(1+\frac{2\varepsilon_s\xi}{C_{ox}TGW1})\phi_{S0\_TGW1}+\frac{\left(2qN_a\varepsilon_s\right)^{\frac{1}{2}}}{C_{ox}}{\phi_{S0\_TGW1}}^{\frac{1}{2}} \\ &=(1+\frac{2\varepsilon_s\xi}{C_{ox}TGW2})\phi_{S0\_TGW2}+\frac{\left(2qN_a\varepsilon_s\right)^{\frac{1}{2}}}{C_{ox}}{\phi_{S0\_TGW2}}^{\frac{1}{2}} \end{aligned} \tag{3-25}$$

For TGW1>TGW2, we can derive:

$$\phi_{S0\_TGW1}>\phi_{S0\_TGW2} \tag{3-26}$$

What this means is that if the transfer gate width (TGW) is decreased, then the transfer gate "OFF" surface potential ϕ_{s0} will be decreased as well. A smaller ϕ_{s0} means an almost flat band state, and a higher potential barrier. The feed-forward voltage measurement can also prove this. Figure 3-24 is the feed-forward measurement for a few different pixels. These pixels have the same photodiode size (PPL=5.2μm and PPW=12μm), the same transfer gate length (TGL=0.6μm), and the same operating voltage for the transfer gate and reset voltage. However, they have a different transfer gate width and floating

diffusion size. A narrow transfer gate corresponds to a smaller floating diffusion area. Based on the measurement result shown in Figure 3-24, V_b is increased from about 0.6V to 1V with the TGW increasing from 4µm to 10µm. This reveals that the potential barrier height is decreased by 0.4V, which is consistent with the analysis above. It is worth mentioning that normally if the barrier height is increased, the PPD can hold more electrons. This allows more electrons feed-forward into the FD node after a certain time, which is shown in the comparison of different transfer gate lengths and different high reset voltages. However, here from the measurement results we found a lower potential barrier (higher V_b) and an accumulation of more feed-forward electrons in the FD node after 4.8ms. The decreased potential barriers shown in Figure 3-24 are caused by an increase the TG width. The larger TGW means that the interface from the PPD to the FD node is wider, allowing more electrons to pass through the TG potential barrier by the mechanisms indicated in Figure 3-17. Therefore when $V_{inj}<V_b$, the number of feed-forward electrons for TGW=10µm are at the maximum in these different TGW measurements.

In general, but depending on design and technology, the FD node reset voltage (VDD_RST_H), transfer gate length (TGL) and gate width (TGW)

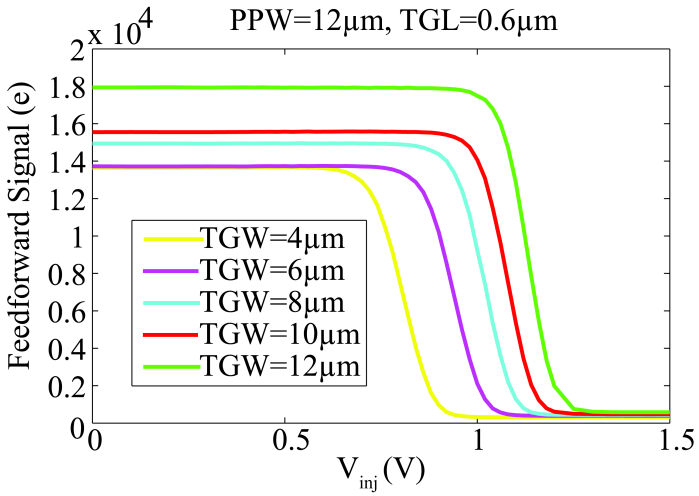


Figure 3-24: Potential barrier height differences for the different transfer gate widths.

will also limit or regulate the potential barrier height of the transfer gate "OFF" state. With the fully understanding of these mechanisms and effects, the designer can easily detect whether the FWC is limited by the short gate effect. The process and pixel design can be optimized further to achieve better performances. It is worth mentioning that the DIBL and short gate effects are not universal for all the processes. The testchip B, which we also characterized, did not show these effects.

3.4.3 Potential Barrier Optimization

Based on the analysis of the potential barrier dependencies in the last section, and with a pixel shrinkage in mind, the method of enhancing the potential barrier height and improving the FWC of the pixel should be considered.

Improving the transfer gate "OFF" potential barrier also means increasing the threshold voltage (V_{th}) of the transfer gate. Increasing the V_{th} could mean that the transfer gate is more difficult to turn "ON". In other words, the gate "OFF" potential barrier is increased, and the zero applied gate voltage surface potential ϕ_{s0} is decreased. Without considering any secondary-order effects, the threshold voltage based on an n-poly gate electrode can be expressed as:

$$\begin{aligned} V_{th} &= (\left|Q'_{SD(\max)}\right| - Q'_{ss})\frac{t_{ox}}{\varepsilon_{ox}} + \phi_{ms} + 2\phi_{fp} \\ &= ((4\mathrm{N_a}\varepsilon_s kT\ln\left(\frac{N_a}{n_i}\right))^{\frac{1}{2}} - Q'_{ss})\frac{t_{ox}}{\varepsilon_{ox}} - \frac{E_g}{2} + \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \end{aligned} \tag{3-27}$$

To increase the threshold voltage and the TG "OFF" potential barrier, the n-poly transfer gate can be replaced by a p-ploy material. The poly silicon working function differences of n and p are listed in Eq. (3-28).

$$\begin{aligned} \phi_{ms\_npoly} &= -\frac{E_g}{2} - \phi_{fp} \\ \phi_{ms\_ppoly} &= \frac{E_g}{2} - \phi_{fp} \end{aligned} \tag{3-28}$$

To minimize the impact of the DIBL effect, decreasing the n-doping concentration of the FD node can be a solution from the technology point of view. However, this will also decrease the FD node capacitance.

From the operational point of view, based on the definition of the DIBL effect, decreasing the high reset voltage can improve the potential barrier but will limit the voltage swing on the FD node. From the design point of view, to increase the transfer gate "OFF" potential barrier, the secondary order effects that result in potential barrier dependency have to be considered. If both the DIBL effect and short transfer gate effect are considered, the best solution is to increase the transfer gate length. To deal with the narrow transfer gate effect and to enhance the potential barrier, the corresponding solution is to decrease the transfer gate width. Combining both of these aspects, a long, narrow transfer gate should be preferred for potential barrier improvement. In other words, decreasing the W/L ratio can improve the potential barrier height, and improve the full well capacitance. Moreover, the transfer gate design can also influence the charge transfer efficiency of the pixel. Details about the transfer efficiency analysis will be introduced in Chapter 4. In our test chip, a few special transfer gate shapes have been implemented which try to analyse the consequence of the different transfer gate shapes on the potential barrier. Figure 3-25 shows a few of them.

In Figure 3-25 **(**A), the traditional rectangular transfer gate shape is shown, which is used as a reference. Figure (B) illustrates a special shape, which is called a reversed T-shape. Based on the rectangular transfer gate shape, this shape has an extra length extension in the center part of the TG, which is embedded into the FD node. The shape shown in part (C) is called a reversed Pi shape. Its gate length extension is located in both width direction of the TG. Like the reversed T-shape, this one also extends in the FD node direction. Illustration (D) corresponds to the reversed T-shape. The only difference with this shape is its gate length extension direction. Shapes (B), (C) and (D) are the extensions of the part of the gate based on (A). The gate length of A (TGL) is equal to 0.6μm. All the extended parts in the other three transfer gate shapes are 0.4μm, and the maximum length parts in these three special shapes are 1.0μm (TGL'). Moreover, the basic transfer gate width (TGW) is 6μm and the extended part width (TGW') is 2μm.

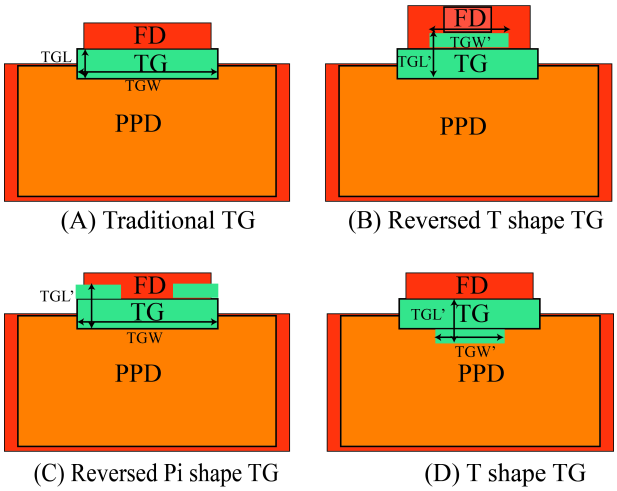


Figure 3-25: Different transfer gate shape implementations.

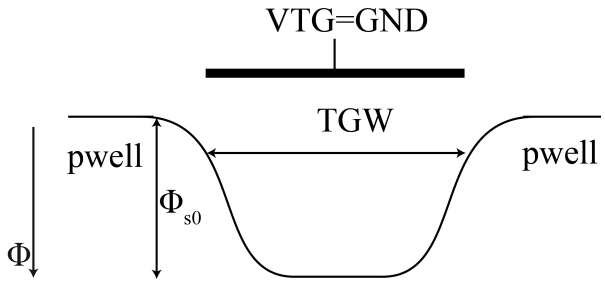


Figure 3-26: Potential diagram of the transfer gate in width direction.

When analyzing the TG gate potential in the width direction, which is shown in Figure 3-26, the potential of the left and right edges of the transfer gate is bent, which is produced by the gate channel and p-well interface. The center part of TGW has a lower potential than the edge. This means there could be first a leakage path in the center of the gate. To improve the potential barrier, one solution could be giving the central part of the gate a longer transfer gate. The T shape TG and reversed T shape TG implement the length extension in two different directions, so that the center part of both TG length can achieve 1μm. The reversed Pi shape adds the extra length in the two edges of the transfer gate, which could be used to determine for proving the leakage path location.

Figure 3-27 is the feed-forward voltage measurement result for these different transfer gate shape pixels. For the traditional rectangular shaped TG, increasing the TG length (TGL) from 0.6μm to 1.0μm, the first knee point V_b of feed-forward electrons is decreased from 0.8V to 0.45V. Consequently the potential barrier height is enhanced 0.35V. The reversed Pi TG-shape pixel potential barrier improved slightly compared with the normal transfer gate with a length of 0.6μm. However, both of the T-shape TG directions improved the potential barrier from 0.8V to 0.65V. The reversed T-shape has a slight advantage compared to the T shape. From these results, it can be found that extending the center of the transfer gate can yield more improvement than the side extension, which means the analysis of the leakage path in the center of the TG is correct. However, we still cannot achieve a similar or better performance compared with the long transfer gate (TGL=1.0μm). If we can further optimize the reversed T-shape pixel design of illustration (B), the FD node design can be changed. If the FD node width is reduced until it is smaller than the width of the extended part (TGW'), this design could also offer the advantage of a narrow channel effect. It should have a higher TG "OFF" potential. However, because of the real pixel implementation, the extended TG part is surrounded by the FD area, this

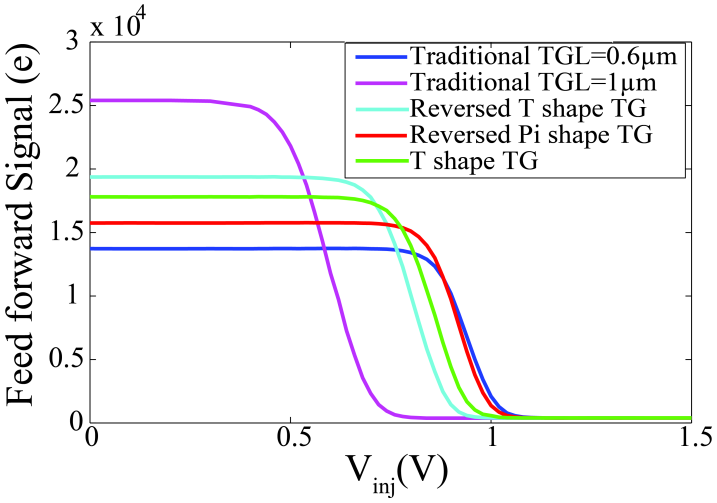


Figure 3-27: Different transfer gate shape feed-forward measurement results.

narrow channel effect advantage cannot be gained.

The T-shape TG pixel design in figure (D) has not only the improved potential barrier but also has the benefit of transfer efficiency. The center gate extension in length makes the DIBL effect smaller on one side. On the other side, it extends into the PPD. When the transfer gate is switched on, the electrical field of the extended TG will be closer to the center of the PPD, improving the transfer efficiency. This statement will be analysed and proved in the next chapter.

From the operational aspect of the pixel, a direct way to enhance the TG "OFF" potential barrier is decreasing the transfer gate low voltage until V_{FB}. According to the definition of the flat band voltage, if VTG_L=V_{FB}, then ϕ_{s0} =0V, meaning that the potential barrier is already the same as the grounded p-well potential. This improvement directly increases the full well capacity of the PPD. The related measurement result will be shown in next section, which is the full well capacity of the pixel.

3.5 Full Well Capacity Measurement and Optimization

As mentioned in Chapter 2, the full well capacity of the chip is one of the two parameters that determine the dynamic range of the chip. With the pixel size shrinking, achieving sufficient full well capacity is becoming a challenge.

The full well capacity of the image sensor can have a few different definitions. The most common definition is the maximum signal obtained from the sensor. Consequently, tracking along the signal path there are a few limitations that will determine the final output signal swing. The maximum signal swing will be limited either by the maximum value of the ADC on the chip, by the analog circuit voltage swing range, by the FD node voltage swing and the FD node capacity, or by charge content of the pinned photodiode. Therefore the smallest range, which is listed above, will limit the maximum signal one gets from the sensor. In this section, further the research is based on the assumption that the pinned photodiode is the bottleneck. Without other limitations, the output directly reflects the capacity ability of the PPD-TG

structure. Here the largest amount of charge that can be stored on the PPD-TG structure will be investigated.

The previous studies [3.10, 3.15, 3.21] have found that the full well capacity (FWC) highly depends on the illumination value and TG low voltage (VTG_L). The full well capacity will be increased with the photon flux increasing. For Figure 3-28 (process B), the TG potential barrier is higher than the potential of the PPD when V_{inj}=0V. The pinning voltage measurement result shows $V_{b\_processB}$ <0V. In this situation, without illumination and with an injection voltage V_{inj}=0V, the PPD is in equilibrium. The total charge stored in the PPD in this state is called the equilibrium full well capacity [3.2] (EFWC). With light, the input signal breaks the equilibrium state. The potential differences between p-well n-doping junctions in photodiode will be smaller than the built-in potential. The total number of electrons that can be accumulated in the PPD (FWC) will be higher than the EFWC. The electron losing in PPD due to sub-threshold current of the transfer gate and forward current of the pn-junction can be compensated by the input photon current. In this balanced state, the full well state is achieved. The electrons cannot increase anymore under the same illumination value. For the pinning voltage measurement, the electrons are injected from VDD_RST pulse to PPD. The injection current is quite large like a very large photon flux injected on the PPD. The injection current could be much large than the forward bias current and/or the sub-threshold current. With the enough injection time and injection current, the measured maximum signal in the PPD will be limited by the TG potential barrier or pwell insolation barrier. V_b is used to characterize the lowest potential barrier between TG and pwell. In our measurement, because $V_{b\_processB}\approx$-0.4V, supposing the TG "OFF" barrier is lower than the pwell potential due to the built in potential of the pwell-n doping junction normally larger than 0.4V. But in reality, both of the situations are possible.

As shown in Figure 3-28, for the process B situation and using the pinning voltage measurement, when V_{inj}=0V, the amount of charge output is the EFWC. With a decrease of the V_{inj} to a negative value, until $V_{inj}=V_{b\_processB}$ the output charge will be saturated, the maximum FWC under certain VTG_L voltage of this PPD-TG structure is achieved. FWC_{max}>EFWC, which can be calculated as follows:

$$FWC_{\max} = C_{ppd}(V_{pin\_processB} - V_{b\_processB})$$
$$EFWC = C_{ppd}(V_{pin\_processB} - 0V) \quad (3\text{-}29)$$

The maximum FWC value will be influenced by the TG "OFF" potential barrier height.

If the situation is the one in process A, shown in Figure 3-28: the TG "OFF" potential barrier is lower than equilibrium photodiode potential (V_{inj}=0V). From the pinning voltage measurement result, it can found that $V_{b\_processA}$>0V. When V_{inj}<$V_{b\_processA}$, the potential barrier already limits both EFWC and FWC. Thus the maximum full well capacity for V_b>0V can be derived as:

$$FWC = EFWC = C_{ppd}(V_{pin\_processA} - V_{b\_processA}) \quad (3\text{-}30)$$

However, this EFWC will be decreased by increasing the time delay between the injection phase and readout phase. Feed-forward electrons are lost, which is mainly due to the diffusion current and the sub-threshold current. Therefore, based on the analysis above, for these two different process situations there are a few techniques, which can improve the FWC. For instance, different solutions result in an increase of the potential of the transfer gate "OFF" potential barrier [3.21] (decreasing the value of V_b), the capacitance of the photodiode (C_{ppd}), and the pinning voltage of the photodiode (V_{pin}). If V_b<=0V, the EFWC will not be changed with the transfer gate "OFF" potential barrier (V_b). If V_b>0V, the EFWC is same as the FWC and can be increased by decreasing V_b.

Using the pinning voltage measurement method mentioned in this chapter and Eq. (3-29) and (3-30), the maximum FWC can be estimated. However, there is a limitation and could have some deviations with maximum value can be measured in real image sensor situation. In this pinning voltage measurement situation, there is some time slot between charge injection and FD reset pulse. Some electrons in PPD will be feed-forward into FD node without any compensation. In the real sensor-imaging situation, the photon flux always injects on PPD, which will compensate the feed-forward electrons all the time compared with the charge injection of pinning voltage measurement. Further, the light input during the transfer time (TG is "ON")

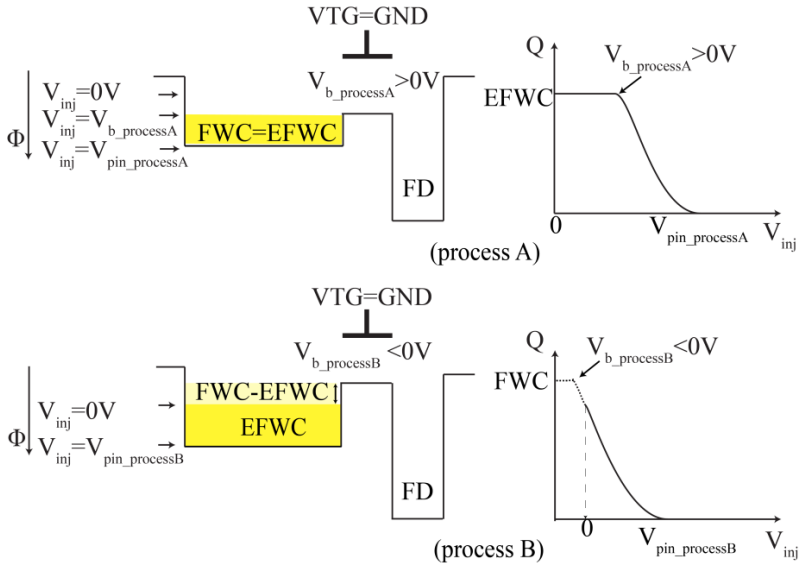


Figure 3-28: Full well capacity diagrams for both process A and process B.

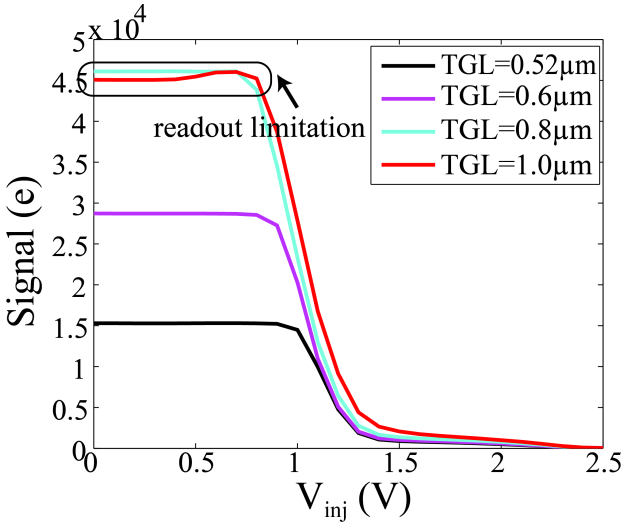
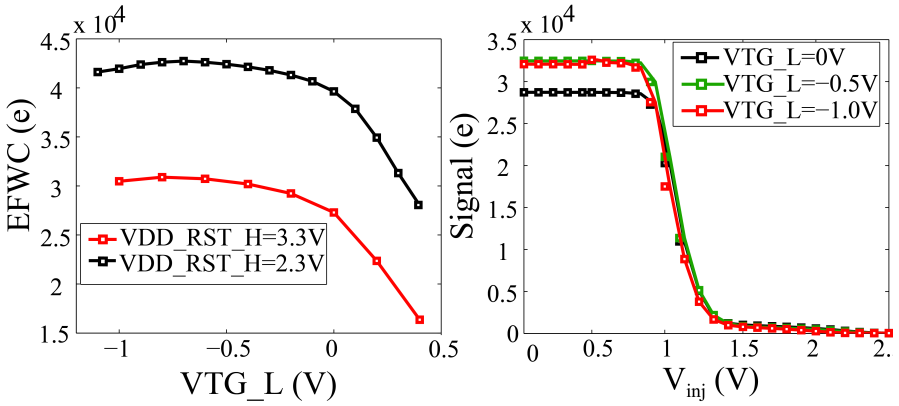


Figure 3-29: V_b >0V, increasing TGL can improve the FWC.

will also contribute to the final full well capacity. The differences between pinning voltage measurement and light illumination situation depend on the timing diagram and specific photon flux in the real situation. Thus, this

method gives a simple estimation of the full well capacity of the PPD-TG structure. The full well capacitance influencing parameters, except the operation environment like illumination level and temperature [3.22], can also be investigated by this method. However, the measured value mentioned in this section still has some deviations with maximum value in the imaging situation.

In Section 3.4, many optimizing solutions for improving the TG "OFF" potential barrier height are proposed and approved. Here the pinning voltage measurement result for process A will be given to prove the improvement of these solutions on the EFWC. Figure 3-19 shows the potential barrier height improved with the high reset voltage (VDD_RST_H) decreasing. The EFWC/FWC is also increased with a reset voltage decrease. The pinning measurement results in Figure 3-29 are valid for the same photodiode size with different transfer gate lengths. When the TGLs are equal to 0.8μm and 1.0μm, the PPD stored electrons already saturate the limited FD node here. Thus electrons under TGL=0.8μm and 1.0μm cannot be completely readout, so the exact number is hard to measure. However, still it can be found that the maximum number of electrons stored in the PPD increases with an increase in the TGL. Another direct way to enhance the TG "OFF" potential barrier is by decreasing the transfer gate "OFF" voltage (VTG_L) [3.21]. For easy comparison, all the pinning voltage or the feed-forward voltage measurement results used before is for VTG_L=0V. Tuning the VTG_L voltage, while keeping V_{inj}=0V results in an EFWC change as shown in Figure 3-30 (A). The measurement result shows that there are three regions according to the relationship between EFWC and VTG_L. When VTG_L>0V, the injected electrons decreased rapidly with the VTG_L increasing. If -0.7V < VTG_L< 0V, the injected electrons increased slowly with VTG_L decreasing further below zero. This means the potential barrier increases with a VTG_L decrease until VTG_L=-0.7V. Further decreasing the VTG_L cannot make the EFWC increase further, which could be caused by the following: One reason could be that the peripheral circuit of VTG_L cannot deal with a more negative voltage. The second reason could be that the measured pixel TG length is 0.6μm, limiting the effective gate area for VTG_L to control. The two curves in Figure 3-30 (A) compare the two situations for VDD_RST_H=2.3V and 3.3V, which prove the influence of the DIBL effect due to the short TG length. The



(A) (B)

Figure 3-30: EFWC vs. VTG_L

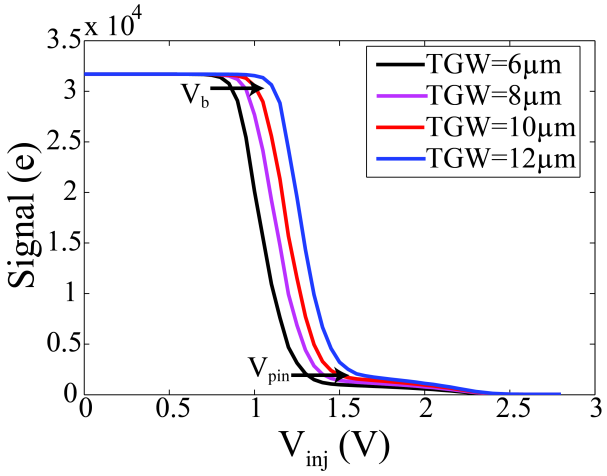


Figure 3-31: EFWC, V_b, and V_{pin} parameter vs. TGW.

final reason for no further increase in EFWC could also be that the transfer gate potential barrier is already higher than the p-well isolation between the pixels. Then blooming happens. The three reasons can work simultaneously. The specific reason for a stable EFWC should be identified in a case-by-case basis. Figure 3-30 (B) is the pinning voltage measurement for different VTG_L voltages. The result also shows that before the TG reaches the accumulation state, lowering VTG_L can improve the EFWC if V_b>0V.

Except for the potential barrier height, the EFWC is also determined by photodiode capacitance C_{ppd} and the pinning voltage (V_{pin}). One thing worth mentioning is that decreasing the transfer gate width (TGW), as proved in the last section, can increase the potential barrier height (V_b), but will not increase the EFWC of the pixel. Decreasing the TGW at the same time is can also decrease the measured V_{pin}, which is nearly the same difference as it for V_b. When both V_b and V_{pin} change together, EFWC or FWC do not have that many differences for different TGWs.

Figure 3-31 shows for the same voltage biasing condition, the same photodiode width and length, how the extracted EFWC, V_b and V_{pin} can be influenced by different transfer gate widths ranging from 6μm to 12μm. This TGW increase can increase both V_b and V_{pin} together. Thus decreasing TGW could not improve the EFWC. Because the EFWC value is decided by these parameters together, only improving the potential barrier cannot improve the EFWC here.

For C_{ppd} extraction, the pinned photodiode structure can be considered as composed of two pn-junctions. When V_{inj} increases, the depletion region width will increase, and then the junction capacitance will decrease. When the voltage in the pinned photodiode reaches its pinning voltage then the capacitance will be the minimum. Using a simple one side step junction as an example, we have:

$$C_{ppd} = A_{ppd}\left(\frac{\varepsilon_s}{L_{n1}} + \frac{\varepsilon_s}{L_{n2}}\right) = A_{ppd}\left(\sqrt{\frac{q\varepsilon_s N_n}{2(V_{inj}+V_{bi1})}} + \sqrt{\frac{q\varepsilon_s N_{p\_epi}}{2(V_{inj}+V_{bi2})}}\right) \quad (3\text{-}31)$$

in which A_{ppd} is the area of the photodiode, and $N_{n,}$ and N_{p_epi} are the doping concentrations of the n-photodiode and p-epi respectively. V_{bi1} and V_{bi2} are the equilibrium built-in potentials of the p+ -n junction and n-p-epi junction. When the pixel pitch shrinks, the photodiode area also becomes smaller and the lateral electric field will have a greater influence on the pixel performance. The research in [3.8] mentions the short PD effect on the pinning voltage. Except the influence on the pinning voltage, our measurement results show that the small size photodiode will influence the unit capacitance of the PPD also. The reason also could be the existence of the PPD lateral depletion

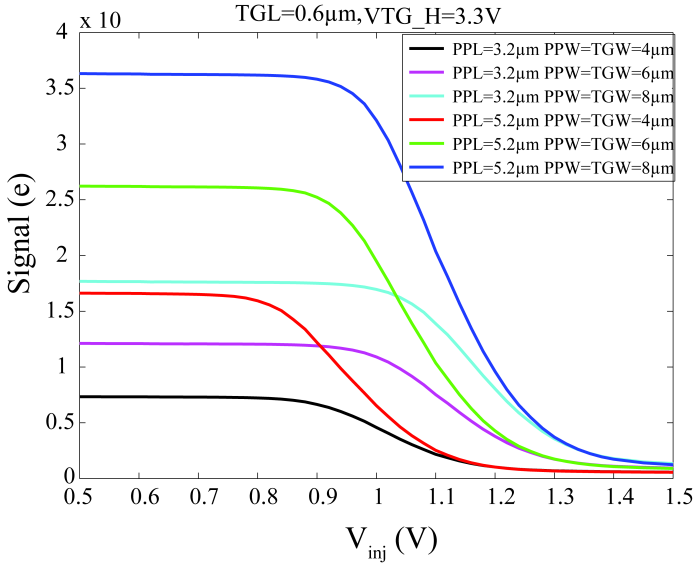


Figure 3-32: Different photodiode area pinning voltage measurement.

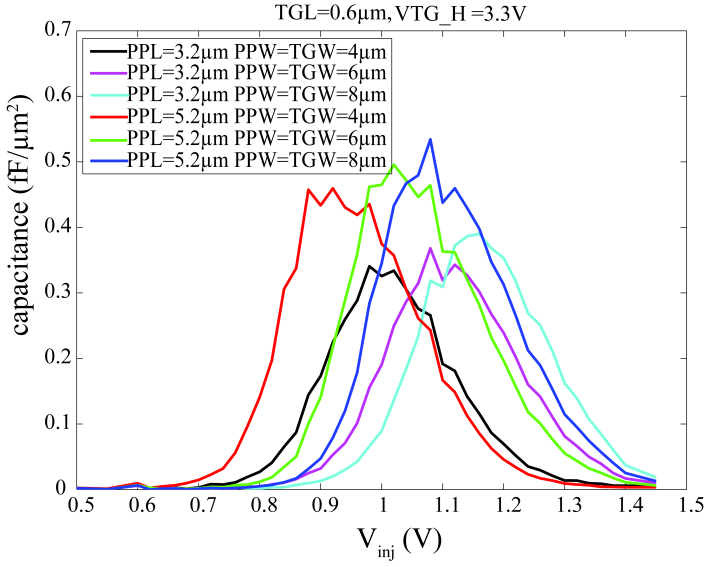


Figure 3-33: capacitance per unit area (C'_{ppd}) extraction from different photodiode areas.

region. Figure 3-32 illustrates a few pinning voltage measurements for different photodiode areas. As expected, the photodiode area influences the EFWC, which is due to the different C_{ppd} for different areas. The C_{ppd} is extracted by taking derivatives of the changing number of electrons as a function of injection voltage, allowing the relationship between C_{ppd} and V_{inj} be determined. After dividing by the corresponding photodiode area, the capacitances per unit area (C'_{ppd}) for different pixel designs are compared, as shown in Figure 3-33. The plot shows that even C'_{ppd} changes rapidly with different V_{inj}, but the maximum values are closed to each other. The measurement result also shows that for smaller PPD length (PPL) values the effective capacitance per the unit area would be smaller than for the bigger PPD length. This is due to the depletion region of the PPD edge causing the effective area to be smaller than expected. For the small photodiode, this rate ((the expected area-effective area) / expected area) accelerates compared with larger PPD area. Therefore, the full well capacity of the photodiode can be optimized in three aspects. First, the potential barrier height (decreasing V_b) of the transfer gate can be increased. The optimization could be done from the technology point of view, pixel design aspect, or operational point of view. Secondly, the pinning voltage (V_{pin}) can be increased, which is mainly determined by the technology. A final solution is to increase the photodiode capacitance (C_{ppd}) by enlarging the photon sensing area or increasing the PPD doping concentration. But it is worth mentioning that, when the length or width of the photodiode is small, the scaling down of the capacitance value is not proportional to the area decreasing.

3.6 Conclusion

In this chapter, a basic physical analysis of the pinned photodiode pinning voltage is made. To better understand and model the PPD-TG-FD structure, and to extract the pinning voltage and other parameters, two 4T pixel test chips are implemented. Two different measurements called pinning voltage and feed-forward measurement methods are used to characterize the devices. Using these methods, the transfer gate of the pixel is analyzed, and the related parameters are extracted. Also based on these methods, the potential barrier

height of the transfer gate is characterized and analyzed. Optimization methods are proposed as well. Finally, the relationship between the full well capacity (FWC) and equilibrium full well capacity (EFWC) is investigated, and the extraction and optimization of the EFWC are discussed. All the discussions presented in the previous sections have led to the a few important conclusions:

- From the pinning voltage measurement for a few different high transfer gate voltages, doping and oxide parameters can be derived.
- When the transfer gate high voltage is not high enough, V_{pin} cannot be measured.
- A shorter transfer gate length and a larger FD reset voltage lower the TG potential barrier.
- A wider TG can lower both the TG potential barrier and pinning potential.
- A special shaped transfer gate can improve the potential barrier without sacrificing the charge transfer efficiency.
- Decreasing the transfer gate low voltage can improve to a certain extend the full well capacity by enhancing the potential barrier.
- The capacitance of the PPD does not proportionally scale with the size of the PPD area. A small PPD has a smaller unit capacitance.
- The PPD capacitance extraction using the pinning voltage measurements is very dependent on the technology, pixel design, and biasing conditions. Moreover, due to the large variation in the injection voltage, its absolute value is difficult to extract. If the PPL and PPW size are not very small, the maximum value of PPD capacitance extraction can be used for comparison.

Certainly, the above analyses, measurements, and modeling works cannot cover all the aspects of the PPD-TG-FD structure modeling. However, these analyses provide more understanding of the physical structure, especially from the electrostatic potential point of view. The dependency of the potential barrier, the full well capacitance, the abstract pinning voltage concept, etc., are clearer and easier to measure and to analyze based, on the model and analysis method of this work.

The research in this chapter generally discusses how to hold the charge in the pinned photodiode during exposure time. When the exposure time is finished, another important process takes place, being the charge transfer. The next chapter, the topic of 4T pixels will mainly focus on charge transfer and image lag characterization and optimization.

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Chapter 4

Image Lag Characterization and Optimization of 4T CMOS Pixels

Image lag is one of the non-ideal effects of solid state image sensors. Image lag occurs because of an incomplete charge transfer in the pixel. The charge residues from the previous frame will cause the present information to deteriorate. The worst case situation occurs in the bright-to-dark transition situation. To better understand and to deal with this problem, this chapter will give an analysis of the image lag mechanism; the characterization and optimization of image lag will also be discussed.

In this chapter, the origins of image lag are analysed in Section 4.1. In Section 4.2, the effect of the photodiode shape is discussed. A pixel design based on the various photodiode shapes is proposed for image lag optimization. In Section 4.3, the analysis of the TG parameter influencing image lag is presented. In Section 4.4, the proposed pixel based on the TG optimization for image lag is introduced. The related measurement result will also be presented. Finally, the conclusions are outlined in Section 4.5.

4.1 The Origin of Image Lag in CMOS Image Sensors

In recent years, with the fast development of CMOS image sensor technology and increasingly number of applications, pixel size scaling is evolving in two opposite directions: very small and very big. Both pose significant challenges to pixel designers. For high-speed applications and low light imaging, a larger photodiode is needed. On one hand, light sensitivity can be increased because more photons are projected onto a larger pixel. On the other hand, transferring all the photon-generated electrons from the photodiode to the floating diffusion can become an issue in a larger pixel. This insufficient transfer results in image lag. Moreover, many applications of CMOS image sensors need a small chip size and high resolution simultaneously. The pixel pitch and photodiode area shrink rapidly as IC technology progresses. With a small photon sensitive area, the image lag will decrease the readout signal level further. In this situation, the noise performance becomes even more important. The incomplete charge transfer will also introduce charge transfer noise that often limits the performance of the image sensor when read noise is below 2e- rms [4.1]. Therefore, eliminating image lag is always one of the important concerns in image sensor design.

In the early CCD time, the interline-transfer CCDs pixel was designed using a pn-junction as the photodetector that was connected to a charge transfer device. Because of the physical nature of this device, it suffers from image lag. A pinned photodiode (PPD) was proposed [4.2, 4.3] to deal with the image lag problem of an interline transfer CCD device. Nowadays, the PPD-TG-FD structure, similar to the PPD in CCDs, is commonly used in CMOS image sensor pixels. The origin of the image lag of a pn junction image sensor has changed from sub-threshold conduction to the a few other sources in the PPD-TG-FD structure.

To eliminate image lag, its origin will be investigated in this section. First, the limited transfer speed is one of the root causes of image lag. For a large area PPD, due to the long transfer path, the electrons need time to transfer across the PPD from its edge to the transfer gate. At the edge of the PPD, there is a reversed pn junction formed by the n-doping of the photodiode and

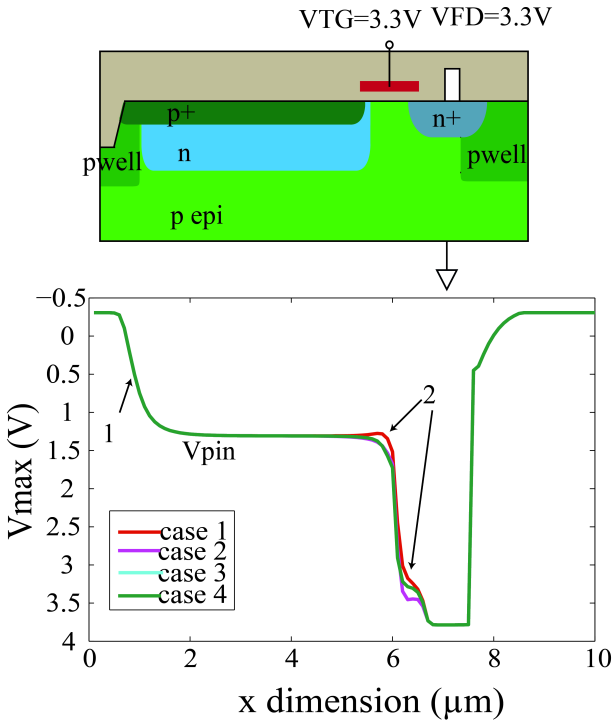

Figure 4-1: Cross-section of PPD-TG-FD structure and corresponding simulation potential diagram.

the surrounding p-well. The electric field across this junction will speed up the photon-generated electrons to pass the TG [4.4-4.10]. The intensity of this electric field decreases with the distance to the n-doping edge. If the photodiode is too long, the electric field drift cannot provide enough speed and energy to the electrons to pass through the PPD and TG within the transfer time, thus the image lag pops up.

The second origin of the image lag is the potential barrier and/or potential pocket [4.5, 4.9-4.11] produced around the PPD-TG intersection area when the TG is "ON". The position relationship of the p^+ layer, n-photodiode diffusion layer and TG poly layer can determine the barrier height and pocket depth. This barrier and pocket will hamper the electrons to be completely transferred. If there is a potential barrier, the electrons need extra energy to jump over the barrier to the transfer gate; some of the electrons even will stay

in the PPD. Figure 4-1 shows the device potential diagram simulation result. In the simulation, transfer gate and FD node are biased at 3.3V. This figure also plots a few situations of different layer offset and the two origins of image lag mentioned. From the simulation result, it can be seen that the designer can tune the design to optimize the potential diagram for a smooth charge transfer. Since the layer offset in this area can also influence the TG "OFF" potential barrier, which has a big influence on the full well capacity of the PPD, this layer optimization should also consider the TG "OFF" potential diagram.

The discussion above only considered free electrons in the conduction band. In reality, silicon devices often suffer from the interface traps as well. Lag can also arise from carrier trapping by defects either in the PPD or under the transfer gate [4.12]. After the transport of charges across the oxide interface of the transfer gate, there is a possibility of some carriers being trapped in the interface states under the transfer gate [4.13]. If the interface states have an emission time constantly equal to or larger than the transfer time, only a fraction of the trapped carriers will emit.

To optimize the image lag there are a few different methods available. On the technology side, to enhance the carrier drift process, the n-doping concentration and p^+ doping concentration should be accurately controlled to optimize for image lag [4.14]. There is also a method which uses a non-uniform lateral doping profile to generate an electrostatic potential gradient [4.9]. Using technology optimizations, the lateral drift field in the photon sensitive pixel area enables high charge transfer speeds and low image lag. To optimize the electrical potential distribution around the TG, the doping concentration around the TG also should be well controlled to diminish the potential barrier and potential pockets [4.15, 4.16]. Except for the technology influence, the PPD shape can also have a big influence on the electric field of the PPD, which has influence on the image lag. In the next section, the related effects will be investigated.

4.2 The Effect of Photodiode Shape

4.2.1 The Effect of Photodiode Shape on Image Lag

For high speed applications and low light level applications, pixels always requires a high sensitivity, which means a large photodiode area. However, with the photodiode length increase, the image lag will also increase. In other words, to completely transfer the charges, the long photodiode requires a long transfer time. Different PPD shapes will form different electric fields in the photodiode. Thus by optimizing the photodiode active area geometrical shape and size the charge transfer inefficiency (CTI) can be optimized by changing the electric field of the photodiode.

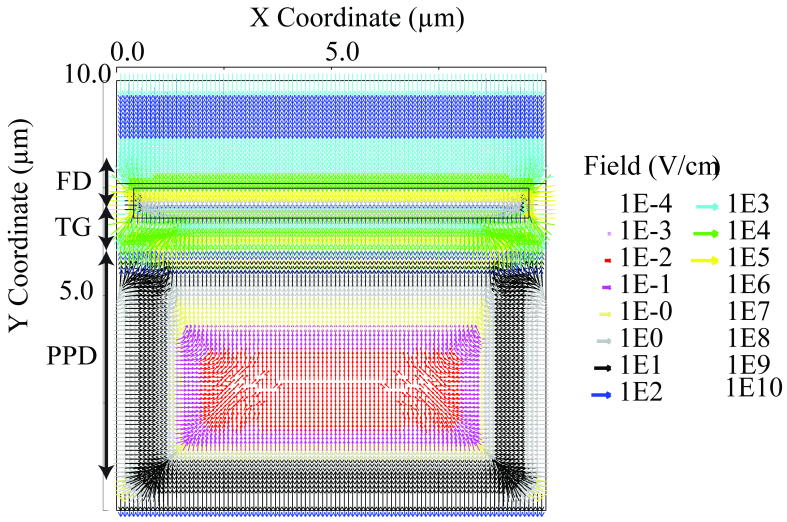

Figure 4-2: The electric field in rectangular shape of PPD (TG “ON”).

At the edge of the PPD, the direction of the electric field, which is formed by the pn junction, is always perpendicular to the edge of the photodiode. Furthermore, the intensity of the electric field in the PPD is inversely proportional to the distance of the n-doping edge. To better understand the pixel, a PPD-TG-FD structure was built in the device simulation tool “SPECTRA”. In Figure 4-2, the electric field distribution simulation of the normal rectangular shape PPD is shown. From Figure 4-2 it can be found that

the minimum value of the electric field is the center of the PPD. Thus, for a large length PPD, the electrons generated in the corners of the PPD might not have enough energy to be transferred to the FD node due to the long transfer path. In this weak electric field situation of the center of the PPD, the electrons slow down and just can move by thermal diffusion movement. Therefore, to speed up the charge transfer process for an image lag decrease, decreasing the electron transfer path or creating extra electrical fields in the charge transfer direction are two possible solutions.

Test chip B was used to verify the simulation of the image lag for different pixel designs. This image lag measurement used a flashing LED to simulate the bright-to-dark transition situation. The timing of the image lag measurement is shown in Figure 4-3.

To measure the image lag, 20 frames of raw data are recorded. The LED is "OFF" in the first n-1 frames. During the time between frame n-1 and frame n, the LED is flashed "ON", and the entire pixel array is exposed. Then frame n will contain the illuminated image data. The light flash time can be controlled externally. The signal readout from frame n+1 will contain the electrons left in the PPD after the charge transfer of frame n. The value of n should be set so that it is large enough to ensure all the electrons left in the last illumination are completely emptied by multiple readouts. The image lag here is expressed in the digital numbers (DN) directly obtained from the ADC readout. As already mentioned in Chapter 2, the charge transfer inefficiency (CTI) is defined as ratio of the charge remaining in the photodiode after the transfer

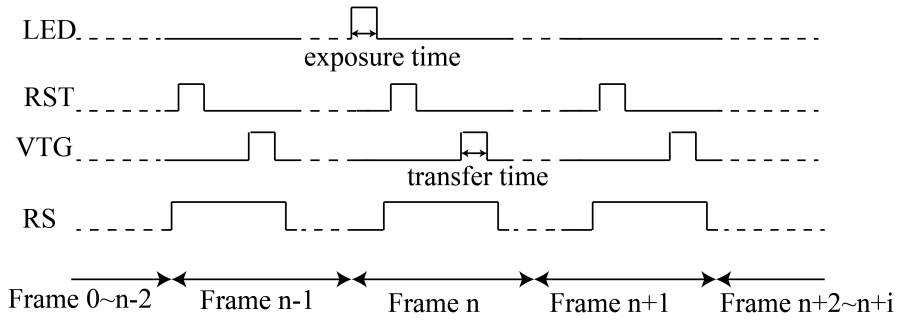

Figure 4-3: Timing diagram of image lag measurement

period, to the total charge accumulated in PPD before transfer. A perfect charge transfer process is transferring all of the charge without any left, then CTI would be 0%. Normally, the charge readout in the next frame is used to calculate the charge remaining in the photodiode. Different measurement conditions for the image lag characterization will achieve very different results. Therefore, it is very hard to compare the image lag performance without mentioning the other conditions, such as the illumination condition (exposure time, and light intensity), TG transfer time, TG high voltage and so on.

If the transfer time is long enough, complete charge transfer will be achieved. However, the application requirements always aim to minimize this transfer time. Thus, evaluating the image lag performance of different pixels could compare the CTI obtained under the same transfer time, or can compare the required transfer time to obtain a particular CTI.

The Figure 4-4 shows the measured image lag change with exposure time for different PPD lengths (transfer time=2μs, VTG_H=3.3V). This result

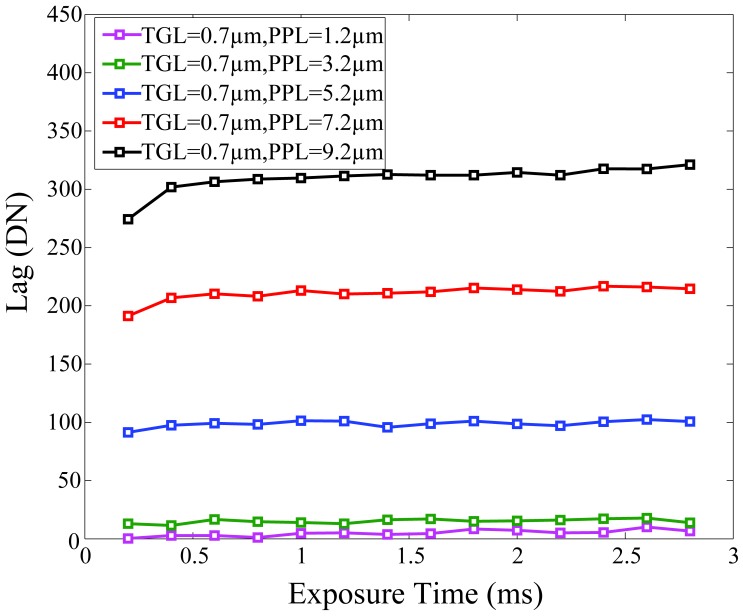

Figure 4-4: The image lag of different photodiode length pixel measured for different exposure times.

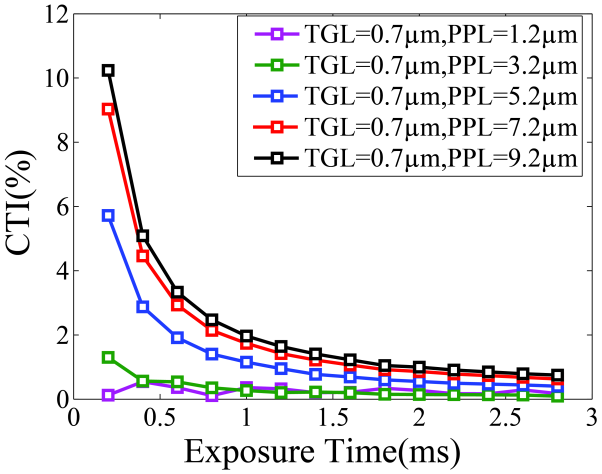

Figure 4-5: CTI of the different photodiode length pixels measured for different exposure times.

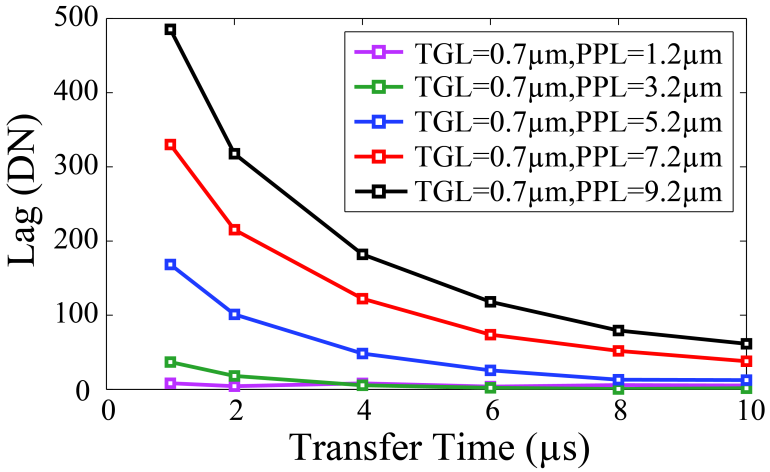

Figure 4-6: Image lag of the different photodiode length pixels measured for different transfer times.

proves that the image lag is increased with PPD length (PPL) (from 1.2μm to 9.2μm) due to the increased charge transfer path and PPD area. However, the image lag remains nearly constant with longer exposure time. It means the electrons left in PPD is TG barrier and/or pocket limited, it will not be increased with signal level under same transfer time and PPD area. From

another aspect, it is also means CTI is highly depends on the signal level, and it will get worse at low signal level as shown in Figure 4-5.

With the same exposure time, changing the transfer time can also prove the transfer time relationship with image lag performance. Figure 4-6 shows that the transfer time has a larger influence on the large PPL pixel than on the small PPL pixel. The voltage of TG is 3.3V. For example, for PPL=5.2μm, to achieve lag=100DN (Digital Number), the pixel operation needs a 2μs transfer time; for PPL=9.2μm, to achieve the same image lag, the pixel operation needs extend the transfer time to 8μs. However, simply decrease the PPL value for a normal rectangular PPD will also decrease the full well capacity and the light sensitivity, which is not acceptable for applications such as high dynamic and high speed applications. Therefore, speeding up the electrons in a large PPL pixel is critical for these applications.

4.2.2 Proposed Non-Traditional Photodiode Shapes for Image Lag Optimization

A. Proposed "W" Shaped PPD

In order to optimize the image lag performance of the pixel, some non-traditional photodiode shapes can be used. The main principle of the PPD shape optimization is to enhance the electric field in the center of the PPD and also minimally sacrifice the light sensitivity and the full well capacity.

Based on the rectangular shaped PPD, a rectangular opening of the PPD (shown as grey area in Figure 4-7) can be made to intensify the electric field in the center of the PPD. Then the center of the original rectangular PPD becomes much closer to the pn-junction formed in this new "bridge" shaped photodiode. The electric field in the PPD center will be increased. Based on the electric field direction analysis a further optimization of the image lag performance is based on the trapezoidal photodiode design [4.4], the four corners will be modified from a right angle to an obtuse angle (β). Consequently, the whole shape becomes a "W" shape. The proposed "W" shaped PPD layout design is shown in Figure 4-8.

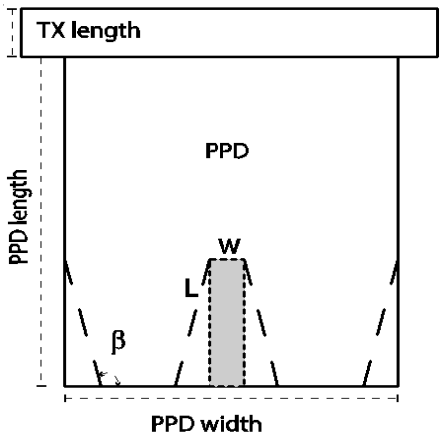

Figure 4-7: Photodiode shaped optimization to intensify the electric field in the center of the PPD.

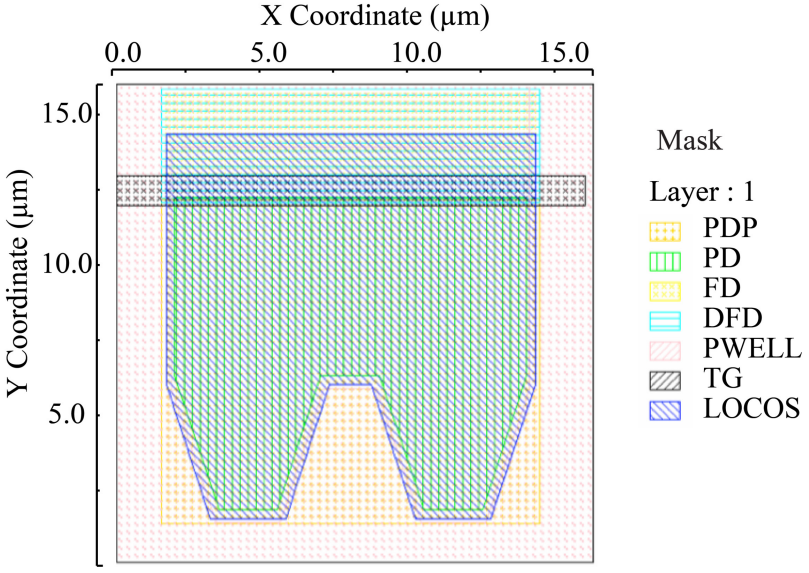

Figure 4-8: Proposed "W" shaped photodiode layout.

From the simulation result in Figure 4-9, it can be found that the electric field intensity in the "W" shaped PPD center is much larger than the rectangular shape. Figure 4-9 presents the 2D plot of the electric field. Figure 4-10 shows the 3D plot of potential diagram of the proposed "W" shaped PPD

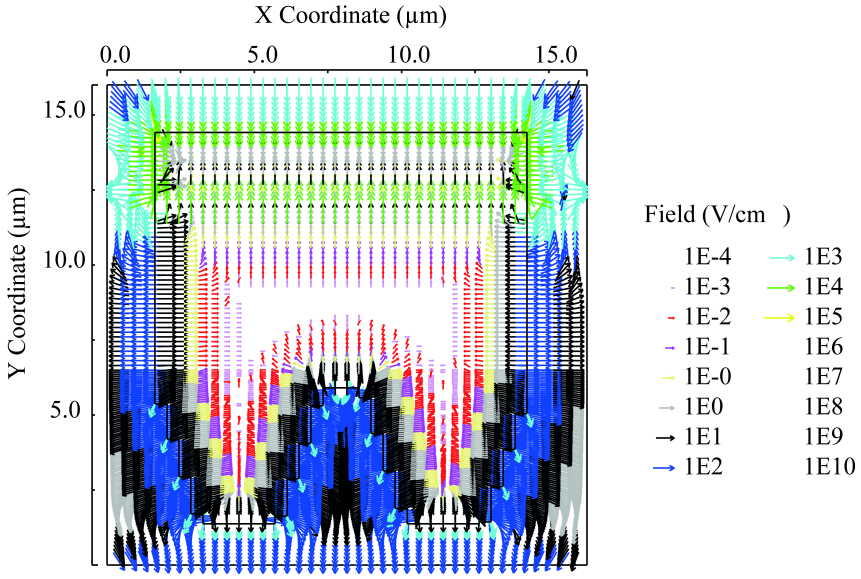

Figure 4-9: XY plot of the electric field of the “W” shaped PPD.

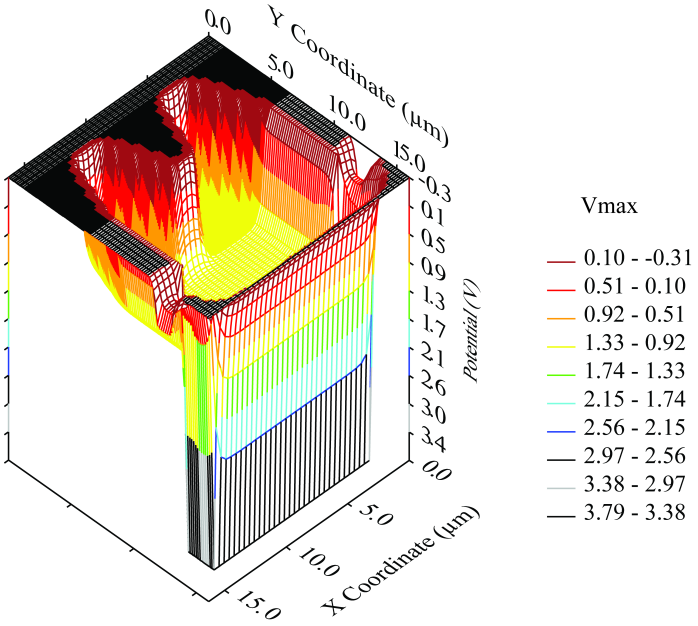

Figure 4-10: 3D plot of the potential for the “W” shaped PPD.

pixel. The similar design principle also has implemented in works of [4.17, 4.18] recently. To prove the image lag performance optimized by the proposed "W" shaped designs, three other pixel designs are used here as references: in Figure 4-11, these pixel designs are plotted. The purple line belongs to the optimized proposed "W" shaped PPD (Here W=2μm, L=4.5μm, β=110˚). The green line belongs to the inverted trapezoid shape with β=100˚

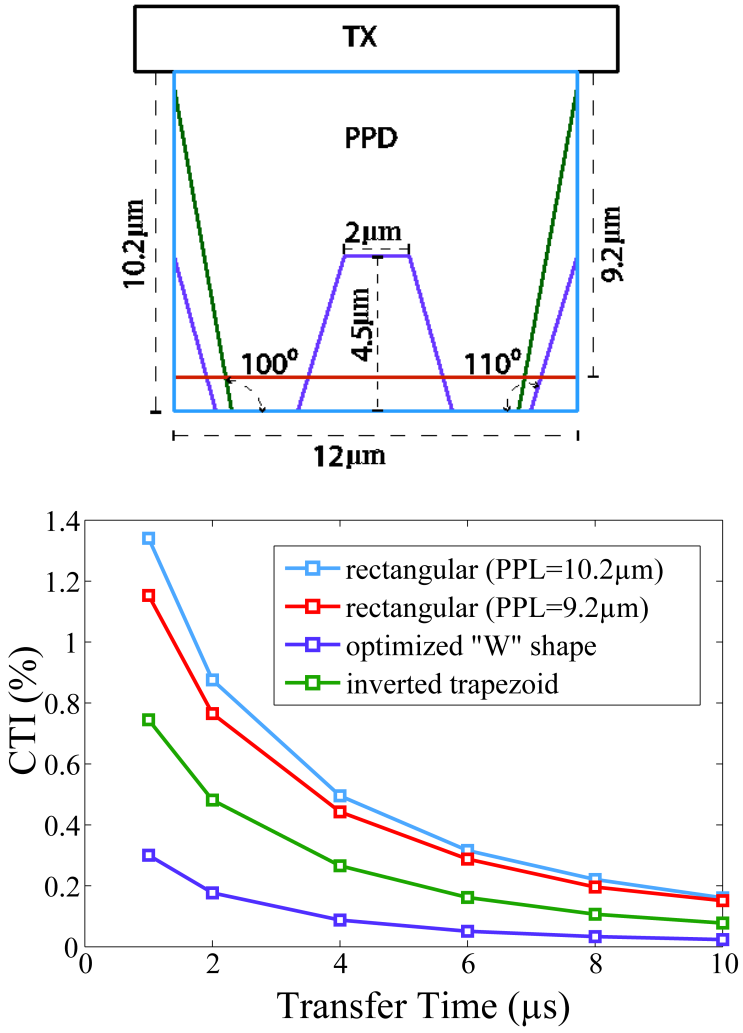

Figure 4-11: CTIs for different transfer times and differently shaped PPD structures.

and without the extra opening. The blue line presents the traditional rectangular photodiode pixel (PPD length=10.2μm), which has the same PPD length as the "W" shaped and inverted trapezoid shape. The red line indicates the 9.2μm photodiode length. The corresponding charge transfer inefficiency (CTI) measurement result shows that for the same illumination condition, to achieve a 0.2% transfer inefficiency, the proposed "W" shaped PPD needs a TG transfer time about 1.8μs; the inverted trapezoid needs 5μs; and the two rectangular shaped PPD pixels need about 9μs. Hence for the same transfer time, the proposed "W" shaped can achieve a much lower image lag than a normal rectangular shaped PPD.

Due to the extra opening of the "W" shaped PPD, and the modified corner, the remaining area of this "W" shape is about 81% of the rectangular shaped photodiode (same PPD length). However, the number of integrated photocarriers is not only determined by the photon sensitivity area but also by the other parameters [4.19]. The carriers are also created within the photodiode surrounding regions and can successfully diffuse and being collected by the photodiode. This process is not only decided by the PPD area, but also decided by the PPD perimeter, the area surrounding the PPD, the characteristic diffusion length of the electrons, and the junction depth. This proposed "W" shaped PPD has a large perimeter and a large surrounding area. Thus, the light sensitivity will not decrease at the same rate as the area (81%). The light sensitivity measurement result also proves this conclusion (Figure 4-12). With the exposure time increase, the output signal of the optimized "W" shaped PPD is only slightly smaller than the rectangular shaped PPD (PPL=10.2μm), the difference (3%) is much smaller than the area differences (19%).

B. "L" Shaped PPD and Transfer Gate

Except for the proposed "W" shaped PPD, there are other possible designs, which can also increase the electrical field intensity of the PPD center. The "L" shaped PPD and TG design is also optimized for image lag by changing the electrical field of the PPD. This optimization method has been reported in many studies [4.20, 4.21]. For our testchip B, this "L" shaped design pixel is also implemented. The layout is shown in Figure 4-13. In this special design, the corner of the TG is located very near the center of the PPD. To achieve the

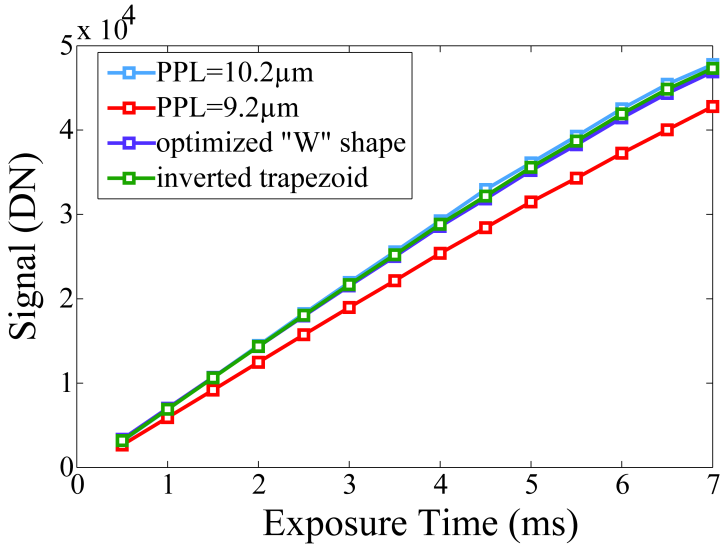

Figure 4-12: Light sensitivity comparison of the various PPDs.

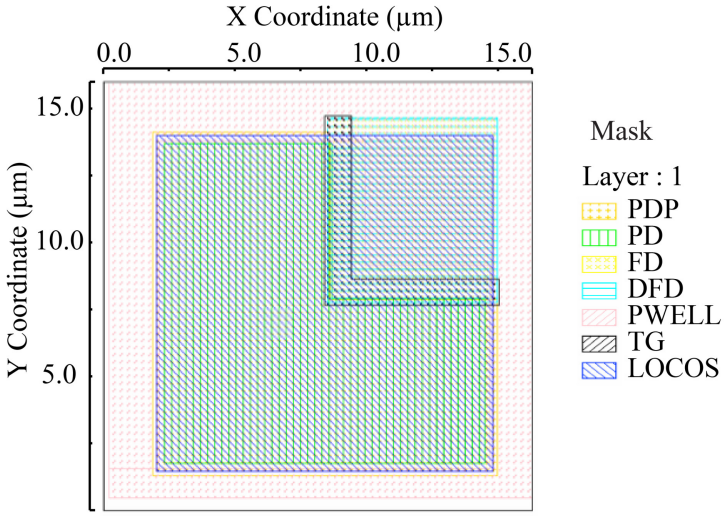

Figure 4-13: “L” shaped PPD and TG pixel layout.

same area as normal rectangular PPD, the L shape TG can decrease the distance between the far edge of the PPD and the TG. Thus, the electric field of the PPD center is intensified. Figure 4-14 shows the electric field simulation result of the “L” shaped pixel design. Except for the PPD electric

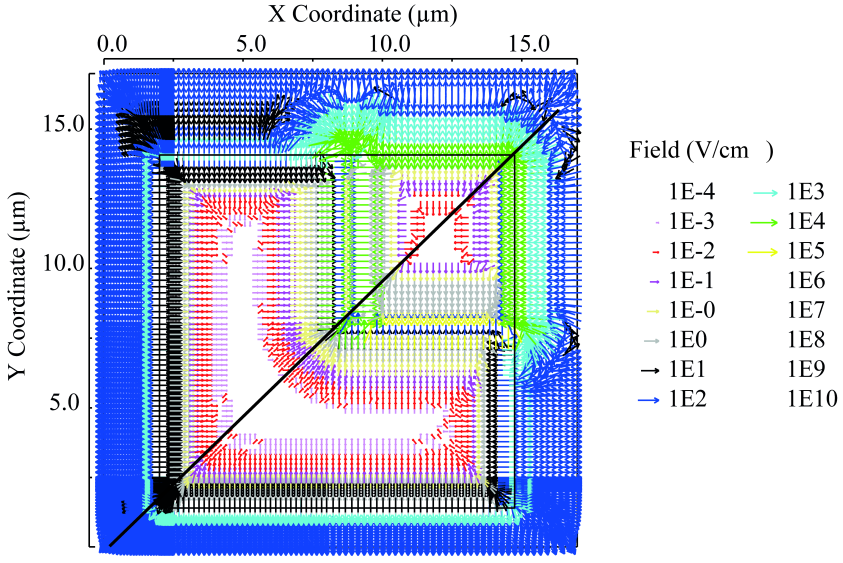

Figure 4-14: XY plot of “L” shaped PPD and TG pixel electric field simulation result.

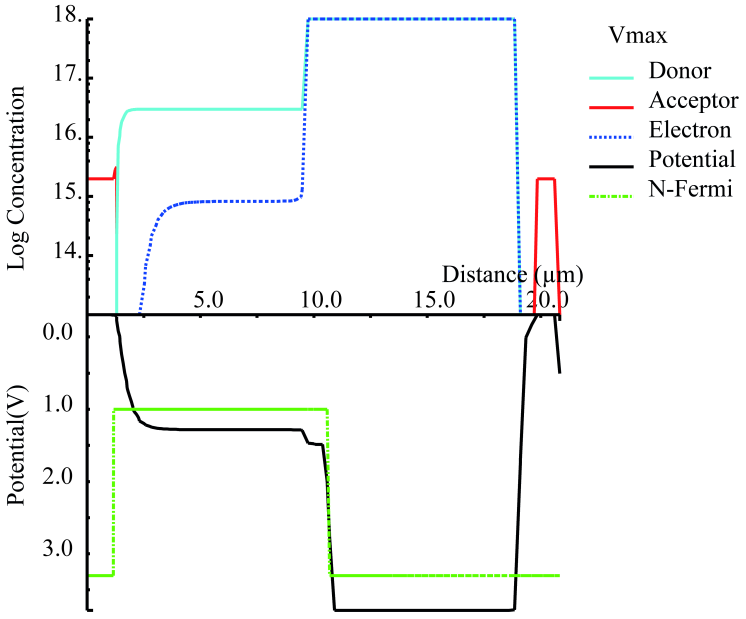

Figure 4-15: 1D potential diagram along the diagonal of the pixel.

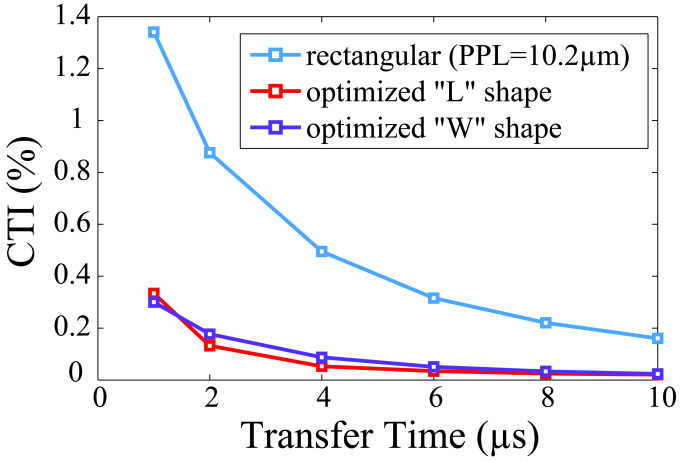

Figure 4-16: Transfer inefficiency comparison between the “L” shape and other shapes with same pixel pitch.

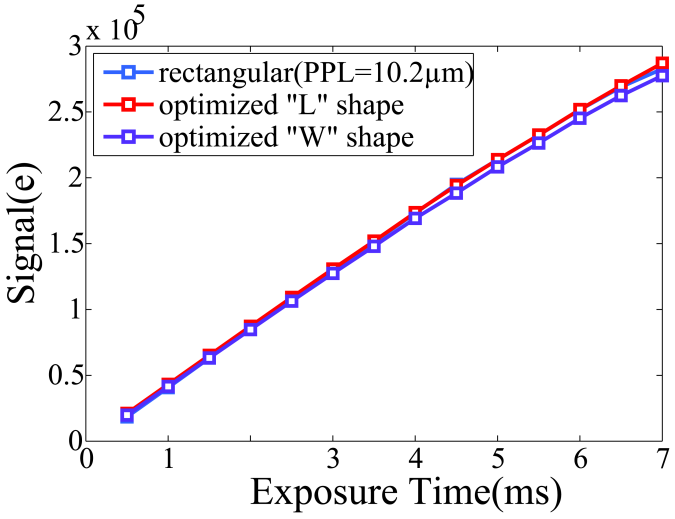

Figure 4-17: Light sensitivity comparison between the “L” shape and other shapes.

field optimization, this structure also removes the TG potential barrier [4.20] by positioning the edge of the readout gate near the center of PPD. Figure 4-15 plots the 1D potential diagram along a transfer path, which is the diagonal

of the pixel as shown in Figure 4-14. This potential diagram shows that there is nearly no potential barrier along the transfer path. From these simulation results, it can be predicted that this structure will have the advantage of both a higher transfer speed and a smaller potential barrier for the electron transfer. The pixel measurement results are shown in Figure 4-16.

This measurement compares the transfer inefficiency between the rectangular shape and optimized “L” shape and “W” shape mentioned in this section. The result shows that the proposed “L” shape can achieve a much smaller image lag compared with the normal rectangular shape, and even slightly smaller than the “W” shape pixel design. The “L” shape PPD pixel implementation does not need extra area sacrifice, therefore it can achieve the equivalent fill factor for same pixel pitch. Figure 4-17 present the light sensitivity comparison in electrons of “L” shape PPD with rectangular shape PPD and “W” shape PPD. Since in this test chip, “L” shape pixel do not implement a completely same conversion gain with other two pixels, the measurement results here are converted into electrons for comparison. The “L” shape achieved a little larger light sensitivity compared with rectangular PPD.

In summary, the measurement results prove that both proposed “W” and “L” shaped PPD 4T pixels can indeed improve the transfer efficiency, and drastically decreases the image lag for a large PPD pixel. Moreover these new PPD shapes can provide the equivalent light sensitivity for the same pitch pixel that is of crucial importance for using large PPDs in CMOS pixels. There are other parameters could be influenced by PPD shape changing. In the next section, other parameters influence will be discussed.

4.2.3 Other Parameters Influenced by the Photodiode Shape

As discussed in Section 4.2.1 and 4.2.2, the photodiode shape has an important influence on the electric field in the PPD. Except for the electric field, the photodiode shape also influences the photon-response and dark current.

As analyzed for the “W” shape, the photon response is not only determined be the active area, but it is also influenced by the perimeter, and surrounding area of the PPD, etc. The total photon generated electrons have a few different components, as shown in Figure 4-18 [4.22, 4.23]. There are three main

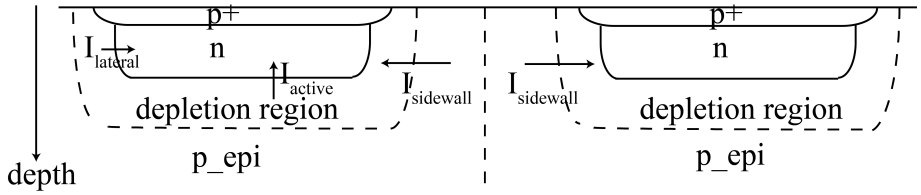

Figure 4-18: Cross-section of two neighboring PPDs where the different current components are indicated.

current components indicated in Figure 4-18. First, the dominant current I_{active} which is the current related in the active area and represents the contribution of the photo carriers created within the photodiode. Secondly, $I_{lateral}$ represents the electron current generated in the lateral depletion region where carriers mainly move by drift. This current is related to the perimeter of the PPD and the junction depth. Thirdly, $I_{sidewall}$ is the lateral current, which is generated in the peripheral sidewall around the PPD by minority carriers that reach the junction by diffusion. This phenomenon is known as the edge effect [4.24-4.26]. Some of the carriers created within the substrates are recombined in the substrate bulk. Some of them contribute to the final readout signal. Some of them have the possibility to diffuse into the neighboring pixel, which results in lateral crosstalk. All in all, the I_{active} is mainly related to the area of the PPD. $I_{lateral}$ and $I_{sidewall}$ are not only decided by the area but also influenced by the PPD perimeter, PPD shape, pixel pitch, diffusion depth, etc. Thus, special shape PPD design takes advantage of a shorter transfer path and a large perimeter to achieve less image lag at same signal response.

Considering the dark current performance of the different photodiode shapes, the dark current also not only relates to the area, but also to perimeter of the PPD. Various conclusions have been derived from different studies about that. Study [4.27] reports that “rounder” PD shapes with fewer acute angles result in a reduction of dark current due to the prevalence of defects in the stressed sharp corners. However, a recent study [4.28] states that the 90-degree corner and square shape exhibit the lowest dark current.

In our measurement, for a large PPD (12μm ×10.2μm), with a small modified corner (135˚), the dark current of the pixel is lowered from 19e^-/s/pix to 18e^-/s/pix at room temperature. Nevertheless, due to the noise

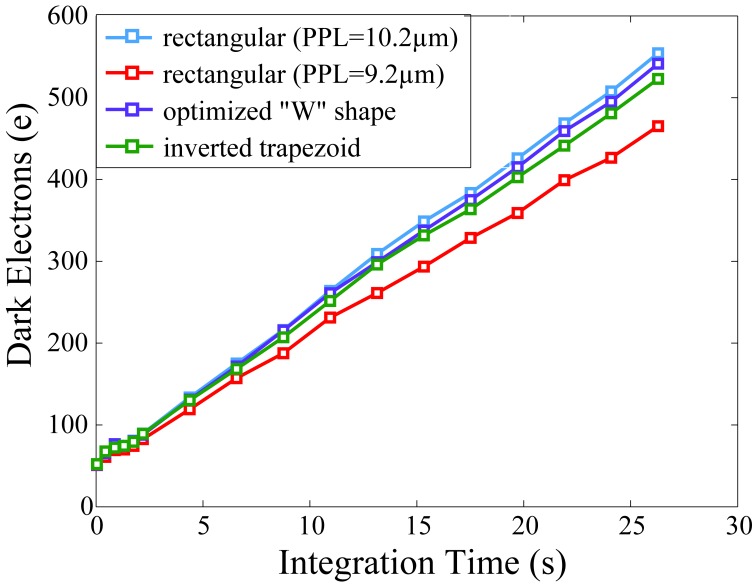

Figure 4-19: The dark current comparison for “W” shape pixel with others design.

limitation, it is difficult for such a small difference to ensure that the “rounder” corner can decrease the dark current.

The proposed “W” shaped pixel has a smaller area than the corresponding rectangular PPD. However, due to the larger perimeter the “W” shaped PPD generates the same level of dark current as the normal rectangular PPD. Figure 4-19 shows this dark current measurement result. From the slope of the curve, it can be derived that, for the rectangular shape (PPL=10.2μm), the dark current is 19e^-/s/pix; the dark current of the optimized “W” shaped pixel is 18e^-/s/pix. It can be concluded that the proposed “W” shaped pixel can improve the image lag performance and without sacrificing light sensitivity (as shown in Figure 4-12) or the dark current of the pixel.

Since the PPD shape changing will not influence on the TG and FD node, the related parameter like conversion gain will not be changed by PPD shape changing. The full will capacity of PPD has the possible to be changed by PPD shape variation. In our optimized “W” shape pixel, it achieved even a little larger equilibrium full well capacity (356903e^-) compared with

rectangular PPD (PPL=10.2μm) which achieved 346130e⁻. The dynamic range also could be influenced by FWC change, but it will depend on the specific design.

4.3 Effect of the Transfer Gate Shape and Voltage on Image Lag

In a 4T pixel design, the transfer gate is one of the most important components. The functions of the TG are to hold the photon-generated electrons in the PPD during the exposure phase, and transfer the accumulated electrons to the FD node in the readout phase. This transfer process determines the output signal and the image lag performance. On one hand, the PPD fringing fields "push" the electrons from the PPD towards the TG direction; on the other hand, the TG channel also forms an electric field to "pull" the electrons when the TG is "ON". The different TG dimension designs and operation voltages also will change this electric field, which in its turn will change the image lag performance.

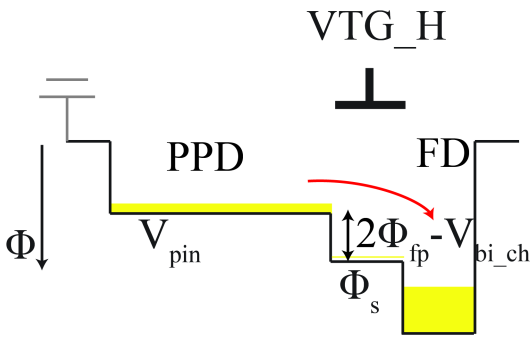

Figure 4-20: Potential diagram of the PPD-TG-FD structure during charge transfer.

In Chapter 3, the relationship between the TG channel surface potential ϕ_s and the gate voltage VTG is already derived as Equation (3-15). $\phi_s \geq \phi_{ppd} + 2\phi_{fp}$ is the TG inversion condition, where ϕ_{ppd} is the potential of

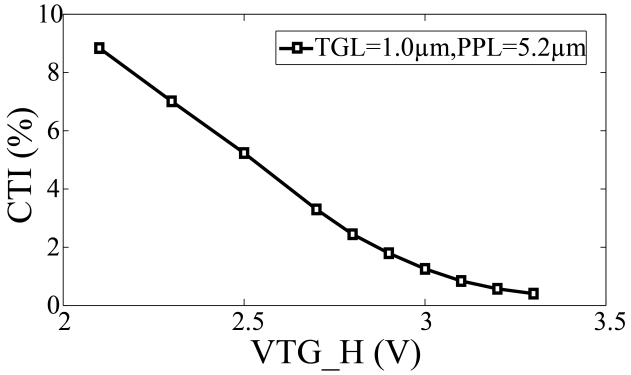

Figure 4-21: Transfer inefficiency performance change as a function of the TG high voltage.

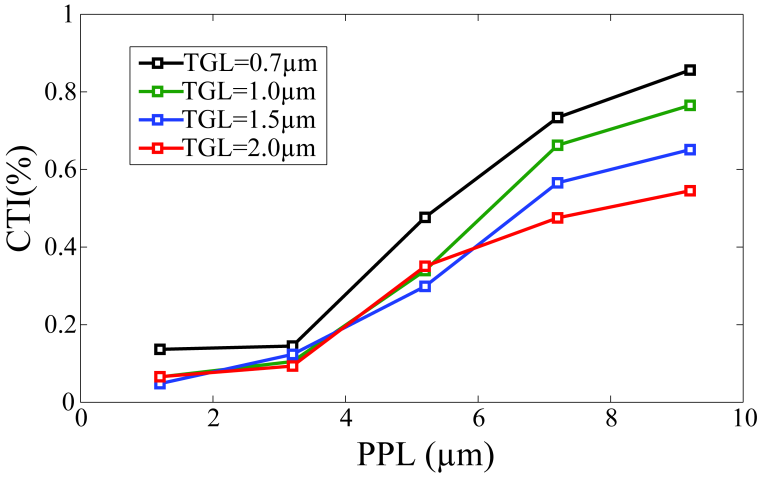

Figure 4-22: Transfer inefficiency performance comparison for different TGLs.

the electrons in the PPD, ϕ_s is the surface potential of silicon under the transfer gate, ϕ_{fp} is the difference (in volts) between the intrinsic Fermi level and the Fermi level of the silicon under the TG. As shown in Figure 4-20, during the transfer period, with an increasing numbers of electrons transferred to the FD node, the electron potential in the PPD will decrease, and value will increase until it reaches V_{pin}. Due to the existence of the pinning voltage of the

PPD, completely emptying the electrons from the photodiode becomes possible. Therefore, to completely empty the photodiode, the surface potential of the TG ϕ_s should at least larger than $V_{pin} + \phi_{fp}$, and better larger than $V_{pin} + 2\phi_{fp}$. Figure 4-21 shows a pixel measurement result as an example, which proves that the CTI decreases with the increase in TG high voltage.

Except for the TG voltage, the TG size also will influence the image lag performance. In common sense, a longer TG will achieve a lower image lag performance, considering the longer TG needs a longer time to transfer. However, from the measurement results of the designed test chip, it can be found that this is not true in every case. Figure 4-22 plots the CTI for pixels with different PPD length and TG length pixels. The PPD width, TG width, and FD node area are constant for measured pixel; PPD length and TG length are two parameters in this measurement. The transfer time for this measurement is 2μs and VTG_H is 3.3V. From Figure 4-22, it can be found that, as already proved, increasing the PPD length will increase the charge transfer inefficiency. Moreover, for large PPD lengths, a longer transfer gate length will achieve a better image lag performance. For example, when PPL=9.2μm and TGL=0.7μm, the charge transfer inefficiency is about 0.9%; when PPL=9.2μm and TGL=2μm, under the same illumination condition and transfer condition, the corresponding charge transfer inefficiency decreases to about 0.5%. A possible explanation could be that the potential on the TG is changed by accumulated electrons on the TG and FD nodes. In this charge transfer process, the PPD and FD nodes are two finite capacitances. When most of the electrons from the PPD flow to the FD nodes, the transferred electrons will decrease the voltage of the FD node. If the number of accumulated electrons are large enough, the transferred electrons will also be located in the channel under the TG to decrease the potential under TG.

Figure 4-23 plots this situation for two different TG lengths. When most of the electrons have been transferred, the remaining electron potential in the PPD is close to V_{pin}. The transferred electrons will make the potential difference ($\Delta\phi$) smaller between V_{pin} and the channel under the TG. Because a longer transfer gate provides a larger channel area, for TGL=2μm, $\Delta\phi_1$ is larger than the potential difference $\Delta\phi_2$ for TGL=1μm. This effect is similar to

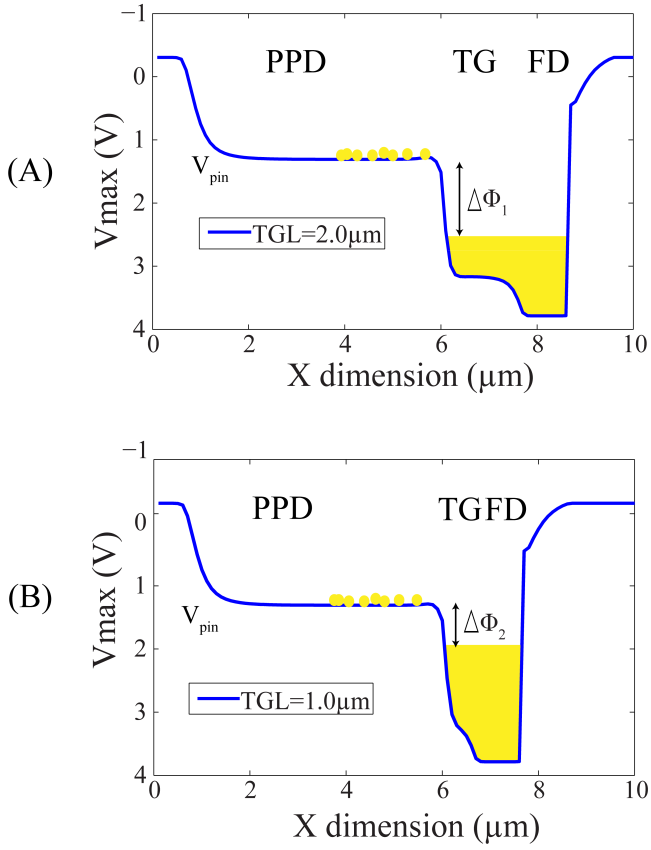

Figure 4-23: Potential diagram to illustrate the TGL influence on the charge transfer process.

lowering the transfer gate voltage, the surface potential of channel under the gate will be more closer to the electron potential in PPD. If this potential difference $\Delta\phi$ is small enough, the electrons already transferred can even jump back to the PPD. Thus, to completely transfer the remaining electrons of the PPD, a longer transfer gate provides a larger potential difference,which turns into a larger electric field. Consequently, a lower image lag can be achieved with a longer transfer gate for this reason.

Not only the transfer gate length, but also the transfer gate area will have an influence on the image lag performance due to the potential difference $\Delta\phi$. The influence of $\Delta\phi$ on the image lag performance can also be proved by

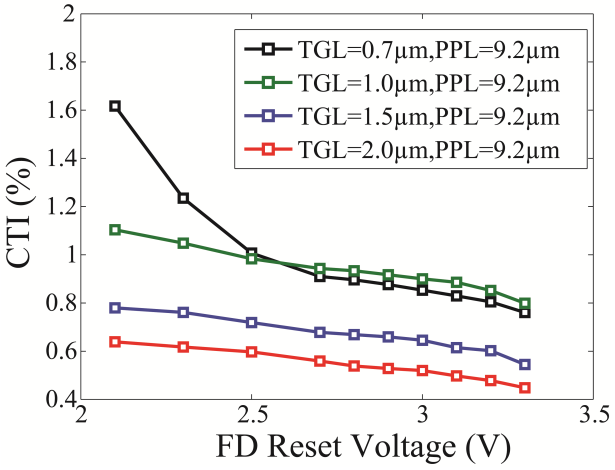

Figure 4-24: CTI decrease with an increased FD node reset voltage.

changing the FD node reset voltage or the FD node capacitance. The total number of charges, which is stored on the FD node and in the channel (when TG is "ON"), is determined by the transfer gate high voltage, capacitance of the TG (TG is "ON"), the capacitance of FD, and the FD node reset voltage. Except for the technology limitation, the TG and FD node capacitance are defined by their respective area. With the FD node reset voltage increasing, more electrons can be stored on the FD node. In other words, if the same electrons are transferred to the FD node, the readout voltage is increased with FD node reset voltage increases. Figure 4-24 shows the influence of the FD node reset voltage on the charge transfer inefficiency. The FD node reset voltage is increased from 2.1V to 3.3V. All the measured pixels with four different transfer gate lengths show a lower charge transfer inefficiency with the FD node reset voltage increase.

4.4 Proposed Non-Traditional Transfer Gate Shape for Image Lag Optimization

In order to optimize the TG "OFF" potential barrier, there is one special TG design, which can improve the FWC of PPD, mentioned in Section 3.4.3. The proposed "T" shape TG design can also optimize the image lag performance.

In this section, two non-traditional TG designs based on this “T” shape [4.29] are introduced.

4.4.1 Pixel Design and Implementation

Based on the normal rectangular TG, the proposed “T” shape transfer gate design adds an extra extension in the center of the TG in the direction of the PPD. The pixel layout is shown in Figure 4-25. This extension not only can increase the TG “OFF” potential barrier, but also can increase the electric field in the center of the PPD. From the device simulation result in Figure 4-26 it can be proved that the electric field of the PPD center is enhanced by the extension of the “T” shaped TG. When the electrons in the corner drift to the center of the PPD, the electrons will gain energy from the strengthened electric field to realize a faster transfer to the FD node. Consequently, the electron transfer time will be decreased. Or, for an equal transfer time, more electrons will be transferred to the FD node. With this “T” shape design, adding an extra extension could further decrease the image lag, however, the added extension would occupy more light sensitive area. The two-extensions TG shape is shown in Figure 4-27 is referred to as “Pi” shape in this thesis.

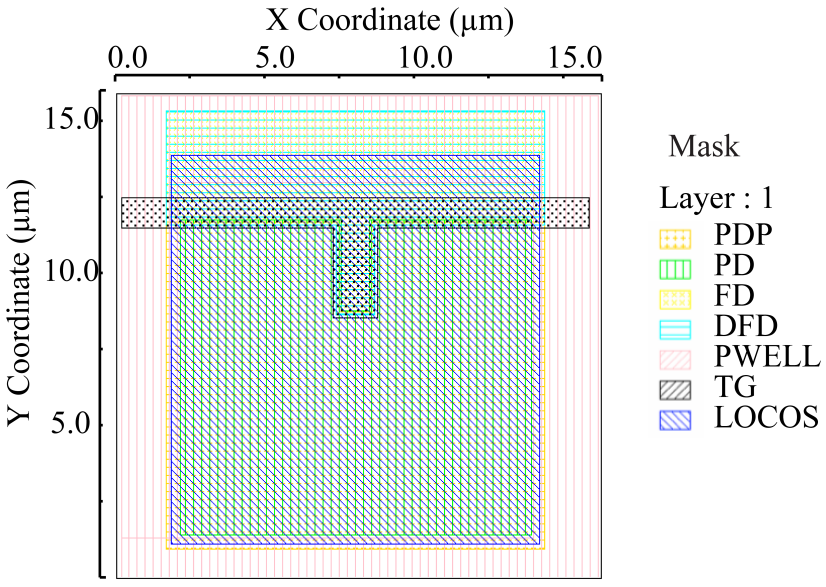

Figure 4-25: Proposed “T” shape TG pixel layout.

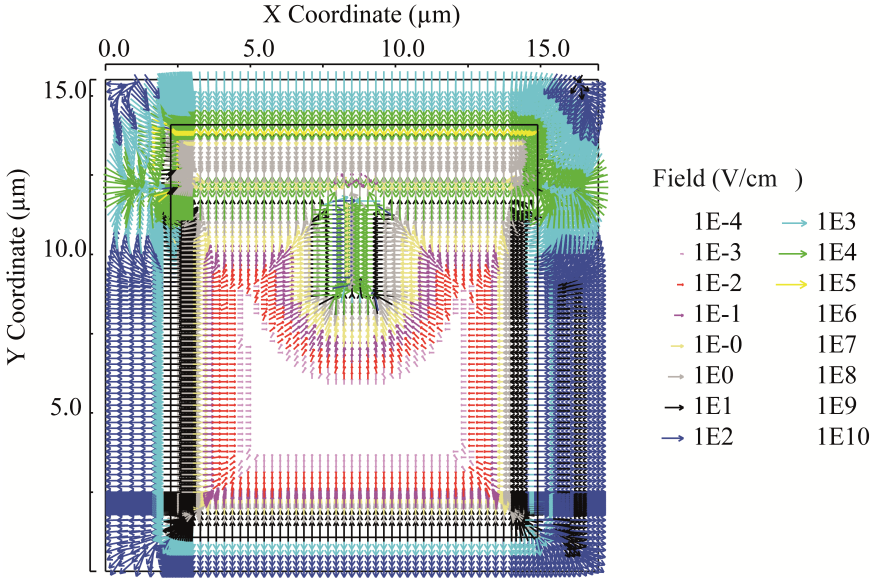

Figure 4-26: Proposed “T” shape TG pixel electric field simulation result.

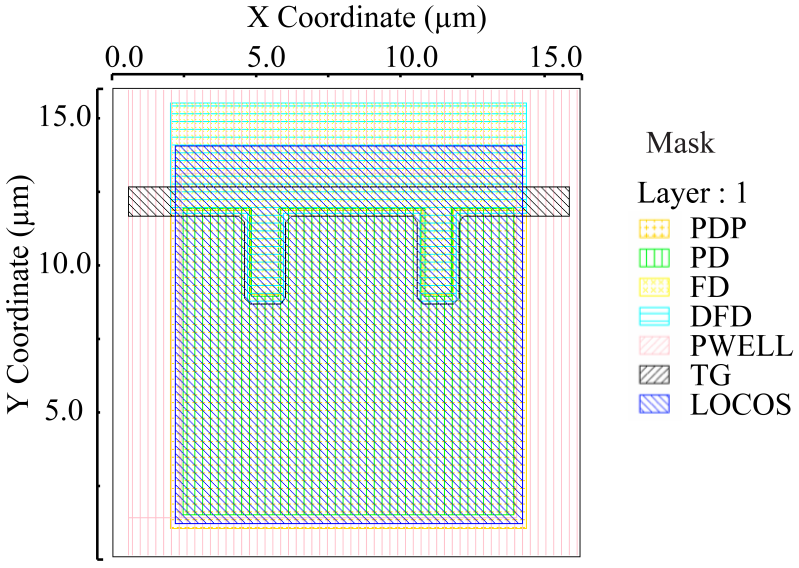

Figure 4-27: Proposed “Pi” shaped TG pixel layout.

4.4.2 Performance Evaluation

To prove the advantage in image lag performance advantage of the two proposed non-traditional TG shaped pixels, a pixel with the traditional rectangular TG is implemented as well together with the new ones. All the designed and measured pixel types have the same PPD, FD node, TG length and width. Only the TG shapes of these pixels are different. The measurement results are shown in Figure 4-28. Figure 4-28 compares the charge transfer inefficiency of the proposed "T" shaped TG, "Pi" shaped TG, and normal rectangular shaped TG pixel under VTG_H=3.3V. When the transfer time is 1μs, the normal rectangular shaped TG pixel can achieve a charge transfer inefficiency of about 1.3%. To optimize this image lag performance, the proposed "T" shaped TG pixel reduces the charge transfer inefficiency from 1.3% to 0.5%. Furthermore, under the same transfer time conditions, the proposed "Pi" shaped TG achieved 0.3% CTI. Although the proposed non-traditional pixel can decrease the image lag, the extra extension of TG still occupy some photosensitive area. Figure 4-29 compares the light sensitivity performance of these pixels. The measurement result shows that the proposed "T" shape and "Pi" shape have a smaller light sensitivity compared to the light sensitivity of the rectangular shape TG. For the same light level, the rectangular shaped TG pixel achieved 17400DN/ms; the "T" shape TG pixel achieved 17100DN/ms; and the "Pi" shape TG pixel achieved about 16920DN/ms. Compared with the image lag performance differences, the sensitivity difference is acceptable, and the "T" shaped TG pixel gives a good tradeoff between the image lag and light sensitivity performance.

4.5 Conclusions

In this chapter, the image lag origins are analyzed. In order to optimize the image lag performance and enhance the transfer speed in large photodiodes, different optimized pixels are proposed. Without changing the manufacturing process, some optimizations are done based on the layout. By understanding the effect of the photodiode shape, some non-rectangular PPD shapes are

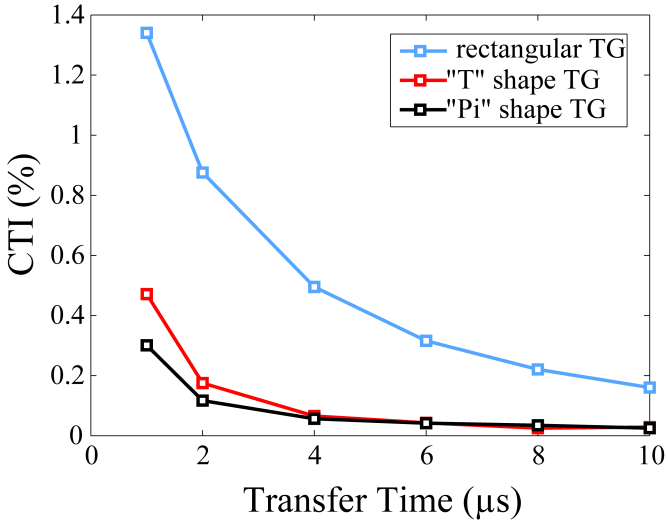

Figure 4-28: CTI comparison of the proposed non-traditional TG-shaped pixels with the classical configuration.

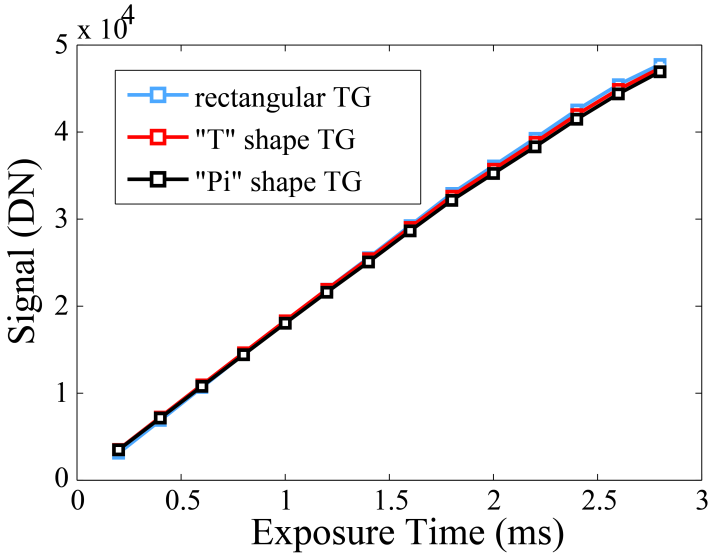

Figure 4-29: Light sensitivity measurement comparison of different TG shapes.

proposed and implemented. The measurement result shows that the optimization of the photodiode shape is effective for image lag reduction. Except for the photodiode optimization, the influence of the transfer gate and the FD node on the image lag is also investigated. Two special TG shaped designs are implemented in a test chip. These special TG shaped pixel designs can also be used to decrease the electron transfer time and image lag, which is quite critical for high speed and low light imaging applications.

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Chapter 5

Hot Carrier Effect

Study of 4T CMOS Pixels

The hot carrier (HC) effect is a phenomenon that occurs in solid-state electronic devices. Hot-electron induced device degradation can impose a limit on device scaling. Extensive work has been done on the hot carrier effect of silicon MOSFETs. However, only limited hot carrier research has focused on CMOS image sensor pixels. In this chapter, a study of the HC effect on 4T CMOS pixels is presented. The mechanism of the HC effect will be introduced, and the performance degradation on CMOS image sensor pixels will be investigated.

The chapter starts with an introduction of hot carrier induced degradation of MOSFETs in Section 5.1. In Section 5.2, the HC effect in a 3T pixel is briefly described. 4T CMOS image sensor pixel performance degradation due to the hot carrier effect is presented in Section 5.3. In Section 5.4, the dependency of the HC effect in 4T CMOS pixels is analysed from different aspects. Some measurement results are then presented. Finally, conclusions are drawn in Section 5.5.

5.1 The Hot Carrier Induced Degradation of MOSFET

A metal-oxide-semiconductor-field-effect-transistor (MOSFET) is the basic component in IC design. Since its birth in the mid-1960s, thanks to impressive advances in lithography technology, the channel length of MOSFETs used in state-of-the-art technology has been reduced by a factor of 0.7 every 2-3 years. This scaling allows increasingly more complex functions to be integrated on-chip. Because the power supply of the circuit is not scaled as much as the channel length, the channel reduction has resulted in an increase in the electric field, which leads to a gain in high kinetic energy of the holes and electrons [5.1]. Within a certain range, this high electric field will increase the carrier velocity and hence allow higher speed for device operation. However, with the electric field increasing, the carrier velocity becomes saturated, and the performance of the device is degraded. High kinetic energy helps carriers to be injected into the gate oxide and form interface states, which in its turn causes degradation of the circuit performance. This effect is called the hot carrier effect (HC effect). The particles attain a very high kinetic energy, which is higher than the equilibrium thermal energy in the semiconductor lattice. These high energy carriers are called hot carriers [5.2, 5.3]. Hot carrier generation, injection and the resulting device degradation are complex processes in general. Although a great deal of understanding has been gained, there remains some controversy and debate about the nature of the degradation [5.4].

Hot carrier injection mechanisms in MOSFETs have been demonstrated in a variety of ways including the Drain Avalanche Hot Carrier (DAHC), Channel Hot Electron (CHE), and Substrate Hot Electron (SHE) [5.5].

Drain Avalanche Hot Carrier Injection mainly happens when the drain voltage (V_D) is higher than gate voltage (V_G). The large voltage drop across the channel pinch-off region results in a high lateral electric field close to the drain of the transistor. The cross-section of a MOSFET is shown in Figure 5-1. The accelerated channel carriers with energy above the impact ionization threshold ($\approx$1.6eV) cause an impact ionization effect, which generates electron hole pairs [5.4]. Some of these generated carriers with an energy high enough to overcome the potential barrier between Si and SiO_2 will be injected into the gate oxide. The energy barrier for the injection of electrons is considerably smaller than that

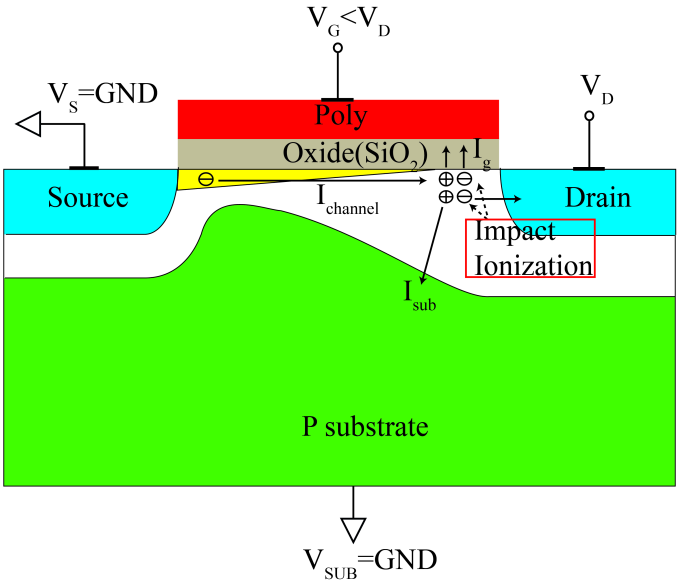

Figure 5-1: Cross-section of MOSFET to show the drain avalanche hot carrier (DAHC) injection.

for holes. Thus, the possibility of hole injection into the gate oxide is much lower than electron injection. Some of the injected carriers can also be trapped at certain defects present in the gate oxide. However, as the hole mobility in SiO_2 is considerably lower than that of electrons, holes have a higher probability of becoming trapped [5.3, 5.6]. Thus, a large proportion of the injected electrons that reach the gate terminal will contribute to the gate current. Except for injection into the gate oxide, considering the electron potential difference, the hot electrons will also drift to the drain, and hot holes will drift to the bulk [5.2]. For the injected electrons in the oxide, except for the ones becoming trapped in the gate oxide, the injected carrier can also result in an increase in the density of interface traps present at the silicon/silicon oxide interface [5.7-5.9].

Channel Hot-Electron (CHE) is another hot carrier mechanism. When both the gate voltage V_G and the drain voltage V_D are high and equal, the high gate voltage will attract some of the channel electrons. The electrons will gain enough energy to surmount the Si/SiO_2 barrier at the drain end of the MOSFET. The injected electrons also will be the part of the gate current.

Substrate Hot Electrons (SHE) happen when the substrate back bias is very large (positive or negative) [5.5]. The injection is due to the homogeneous emission of leakage electrons from the Si substrate into the SiO_2. This injection mechanism could be important in bootstrap circuits.

Among these injection mechanisms, during normal operation, DAHC injection is the most dominate injection effect. The above analysis is based on a default nMOSFET. Compared to the nMOSFET, pMOSFET hot carrier degradation is typically perceived to be less of a problem. Due to the shorter mean free path and higher oxide barrier for holes in pMOSFETs, fewer hot carriers are generated. It is believed that electron trapping in the gate oxide is responsible for most pMOSFET hot carrier degradation [5.10]. Electron trapping results in a shortening of the effective channel length, which leads to an increase in drain current.

All in all, no matter which hot carrier mechanism, regardless of hot electrons, holes injection or interface state generations, all of these phenomena can significantly change the characteristics of the MOSFET, and can significantly reduce the operating lifetime of these devices.

5.2 3T Photodiode APS Performance Degradation due to the HC Effect

With CMOS process scaling, and an increasing imager resolution requirement, the pixel designer is working on creating much smaller pixels. Because of pixel pitch shrinking and fill factor considerations, the geometries of the MOSFET in the pixel are close to the minimum size. Ideally, the transistors in the pixels should process the voltage and current signal without influencing the photon sensitive element behaviour. However, with the high electric field produced in the pixel transistor, if the hot carrier effect occurs, then the injected electrons can be absorbed by the nearby photodiode. The readout signal will therefore be distorted. These effects of HC generation that occur in 3T pixels have been reported in a few studies [5.11-5.15].

As introduced in Section 2.2.1, in a 3T photodiode APS, as shown in Figure 5-2, the photon sensitive region and the charge integration node are implemented with the same photodiode junction. The dual role of the photodiode causes the photodiode to be directly connected with the gate of the source follower. The source follower is operated in the saturation region, and the pinch-off region near the drain of the source follower can generate a high electric field. The accelerated electrons in this region can induce an impact ionization, which produces many hot electron and hole pairs. This is the first step shown in Figure 5-2. As explained in Section 5.1, this is the drain avalanche hot carrier (DAHC) injection. Some of the generated electrons can gain energy to break the gate oxide interface. The electrons without being trapped will arrive at the gate terminal, which is connected to the PD capacitor (step 2 in Figure 5-2). With the accumulated gate injected electron in the photodiode, the voltage of the gate will be decreased and the source follower gate drain voltage differences will be increased further. The enhanced electric field in the drain of the source follower can introduce a more severe hot carrier generation effect (step 3 in Figure 5-2). These three steps form a positive feedback loop. The hot carrier mechanism in the 3T pixel is strengthened and more excess carriers are generated.

The definitive mechanism causing electrons to flow to the PD region is hard to confirm. In previous studies [5.11-5.13], the explanation focused on the substrate current. As shown in the cross-section of the PD and source follower (Figure 5-2), some of the generated electrons flow to the PD through the substrate as minority carriers.

Both of these transfer mechanisms are possible. If transferred by gate injection, the electrons need enough energy to overcome the potential barrier between the Si and SiO_2 interface. Even some of the electrons already injected into the oxide, still have the possibility to being trapped by the interface state at the Si-SiO_2 interface. If the generated hot electrons do not drift to the drain of the source follower and do not have enough energy to be injected into the gate, then some of them also have the possibility to being absorbed by the PD through the substrate. During this transfer, many will be recombined with the hot generated holes. Thus, if there is a short path from the source follower under the gate substrate to the PD, the possibility that the hot carrier will flow to the PD from the substrate will be greater. With the HC effect, even under the complete

darkness, the generated hot electrons can cause the readout signal to become very large. The generated hot electrons can also flow to the neighboring pixel through substrate.

For 3T pixels, if the hot carrier effect emerges in the source follower in certain circumstances, the hot carriers injected into the PD will increase very quickly due to the existence of the hot carrier feedback loop regardless of the transfer mechanism. This effect will deteriorate the signal response of the pixel completely. To avoid the hot carrier effect, the transistor designed in the pixel should avoid operation in the deep saturation region. If the pixel circuit is too complex, special attention should be paid for isolating the photo-sense area from the possible transistor for the HC effect [5.13].

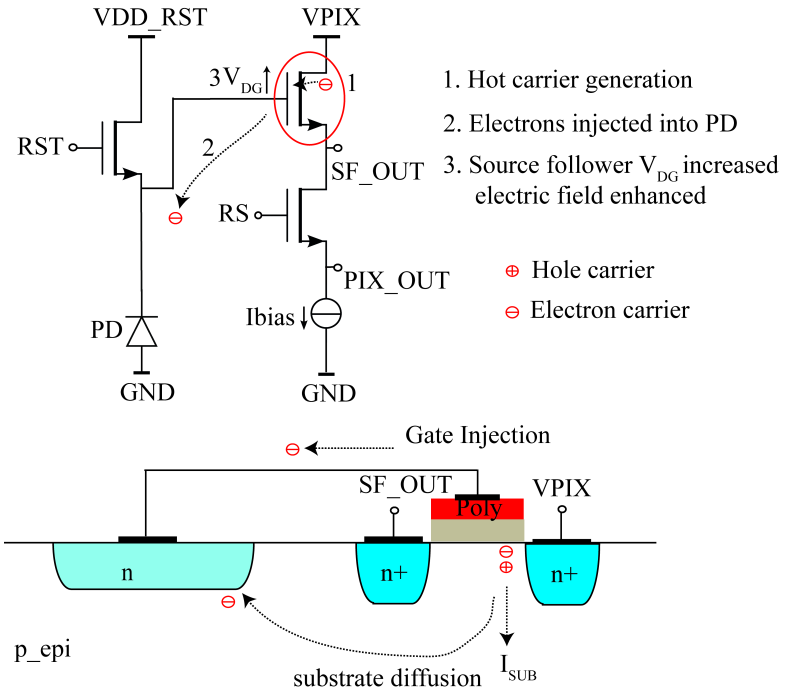

Figure 5-2: Schematic and cross-section of 3T pixel to show the hot carrier effect in a 3T pixel.

5.3 4T PPD APS Performance Degradation due to the HC Effect

Compared to the 3T pixel, the 4T pixel separates the charge integration capacitor with the photon sensitive element by adding a transfer gate.

In the ideal situation, the transfer gate can stop the hot carrier electrons from flowing to the photodiode. During the integration time, the PPD collects the photon-generated electrons; some of the hot carriers produced in the channel of the source follower can flow to the floating diffusion. Before the readout, the hot electrons in the FD node are emptied by a reset pulse. No extra hot electrons can be transferred to the PPD from the FD node. Then the light-generated signal

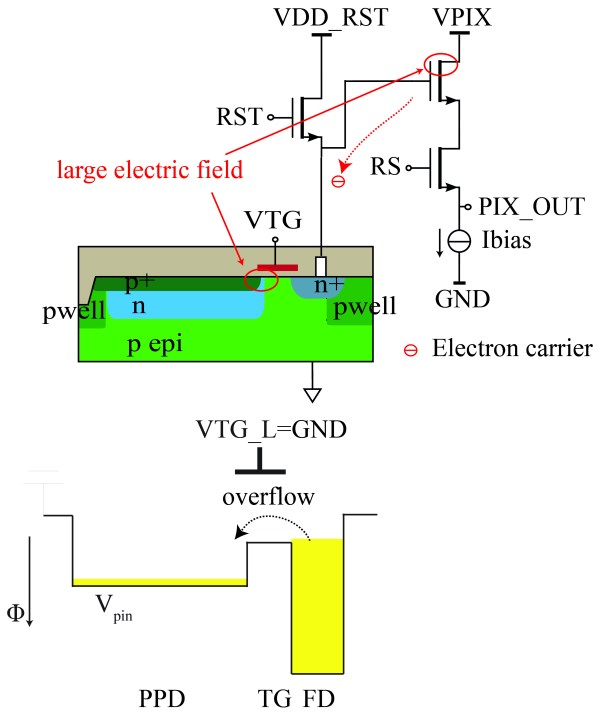

Figure 5-3: Schematic and potential diagram of a 4T pixel to show the hot carrier transfer path in a 4T pixel.

will not be contaminated. To completely blocking the hot electron leakage from the FD to the PPD when photodiode is integrating, the TG "OFF" potential barrier will need a high enough potential barrier. However, in reality as explained and characterized in Chapter 3, the TG "OFF" potential barrier is not always as high as the p-well potential barrier. Figure 5-3 illustrates the 4T pixel hot carrier situation. Just as the 3T pixel situation, under the influence of a high electric field, the hot carrier could be generated near the drain of the source follower. If the hot carrier effect occurs, the generated electrons will flow to the FD node. The hot carrier electrons can fully fill the FD node. When the filled electron potential is higher than the TG "OFF" barrier, the electrons will overflow into the PPD node, which will contaminate the image signal. Besides the leakage from the FD node to the PPD, there is also the possibility that the hot carrier is transferred from the substrate of the source follower directly to the PPD. With an increasing integration time, the accumulated HC electrons will be more dramatic. In a 4T pixel, during the charge transfer process, the positive VTG also creates a strong inversion layer along the interface of the silicon oxide underneath the TG [5.16]. A large electric field is generated in the PPD-TG overlap region. Some of the photon-generated carriers from the PD will gain enough kinetic energy to produce hot carriers during the charge transfer as well.

In our testchip A, the hot carrier effect was found during the dark current measurement. The pure dark electrons produced in the PPD cannot be measured due to the overwhelming influence of the HC electrons.

To better understand the hot carrier effect in the 4T pixel, the dark signal measured from both the FD node and the PPD are compared. The FD node signal is the dark signal accumulated in FD node without a TG charge transfer. The signal measured from the PPD is the signal transferred from the PPD to the FD node after the FD node is emptied by reset. The measurement results are shown in Figure 5-4. The dark signal in the FD increases quite linearly with integration times shorter than about 17s. When the integration time increases further, the readout dark signal from the FD becomes saturated. For the dark signal transferred from the PPD, the measured dark signal is increasing quite slowly when the integration time is shorter than about 17s. When the integration time increases further, the dark signal slope becomes steeper. Both slopes of these curves are changed around 17s. A possible explanation is that when FD node is already filled in 17s the electrons began to leak to PPD.

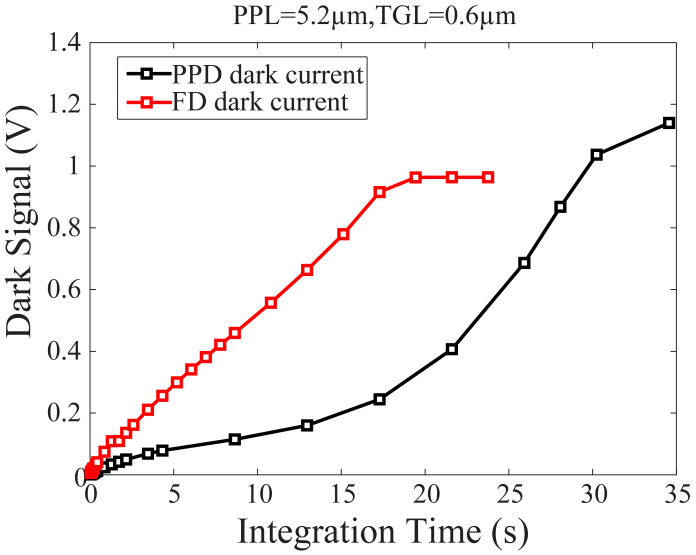

Figure 5-4: Comparing the FD node dark and PPD dark signal introduced by the HC effect.

In this testchip measurement, the measured HC effect does not increase with the transfer time which means the TG introduced HC in our measured testchip can be overlooked. Just as in the 3T pixel, the origin of the HC generation is still the source follower. The floating diffusion capacitance and TG "OFF" potential barrier also influence this process when the HC carriers are injected from the FD node to the PPD. The pn junction leakage in FD node also will contribute to the dark signal. However, this large signal value is not the normal range of the pn junction dark current. The large hot carrier injection will overwhelming the pn junction dark current which cannot be identified from the total dark signal.

To improve the HC effect, with the same technology and same source follower size, replacing an nMOS source follower with a pMOS source follower could decrease the HC effect. A schematic of a pMOS source follower pixel is shown in Figure 5-5. In a pMOS source follower, a large V_{DS} and V_{DG} is avoided, thus the hot carrier induced degradation should be much better than in an nMOS. From the layout perspective, the nwell isolates the source follower from the FD node and the PPD. Therefore the hot carrier diffusion from the substrate to the FD node and/or PPD will be hampered. From the measurement result comparison shown in Figure 5-6, it can be found that the pMOS pixel

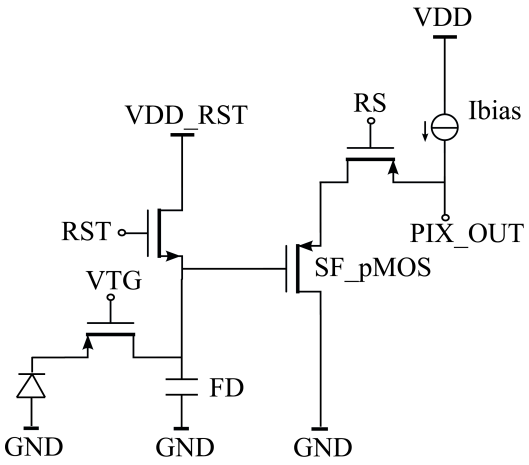

Figure 5-5: Schematic of pMOS source follower 4T pixel.

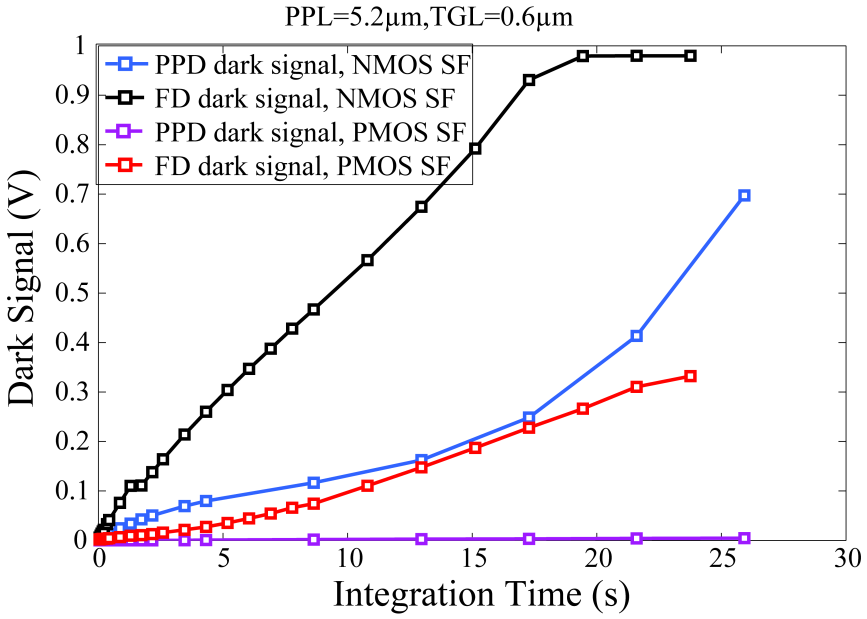

Figure 5-6: Comparison of nMOS and pMOS source follower pixel HC effect.

achieves a smaller FD node dark signal compared with the nMOS pixel FD node. Moreover, there is nearly no hot carrier diffusion into the PPD from the FD node or SF substrate. Since measured dark signal from PPD of pMOS pixel are

very small compared with nMOS pixel, which has the same FD node, the injected hot electrons are the main component of the measured dark signal from PPD.

5.4 The Dependency of the HC Effect in 4T CMOS Pixels

In this section, the HC generation dependency will be analyzed using our 4T test chip, which suffers from the HC effect. The HC generation dependency will be analyzed. The result and analysis can also be used for 3T pixels.

5.4.1 Voltage Dependency

Based on the generation mechanism of hot carriers, a high electric field is a fundamental prerequisite for the hot carrier effect. For drain avalanche hot carrier injection, the V_{DG} voltage will determine the electric field at the drain gate region; in turn the drain voltage has a huge influence on the hot carrier injection. In a standard pixel design, a hot carrier injected in a PPD is dependent on the drain voltage of the source follower (VPIX shown in Figure 5-3). In Figure 5-7, the dark signal of the PPD is measured. Two VPIX values, 2.8V and 3.3V, were applied individually. With the integration time increase, the dark signal measured from PPD increases for both cases. When the integration time is shorter than 15s, the two voltage-supplied situations exhibit the same dark signal performance; when the dark signal achieves about 0.15V (integration time about 15s), the dark signal for VPIX=3.3V increases exponentially, which is much more severe than the VPIX=2.8V situation. The increasing speed (V/s) of the dark signal measured for the VPIX=3.3V biasing situation was about 10 times that of the VPIX=2.8V situation (integration time>15s). From this measurement result, a strong correlation between the dark signal and the source follower power supply value is presented. Decreasing the drain voltage of the source follower helps to reduce the electric field, which in turn will decrease the dark signal measured from the PPD. When the integration time is short, the dark signal is small, which means the FD node voltage is close to the reset voltage (3.3V). At this time, the source follower drain gate voltage (V_{DG}) is not high for both VPIX=3.3V and VPIX=2.8V biasing conditions. Thus, the injected hot carrier for VPIX=3.3V and 2.8V are equal at a short integration time. With an

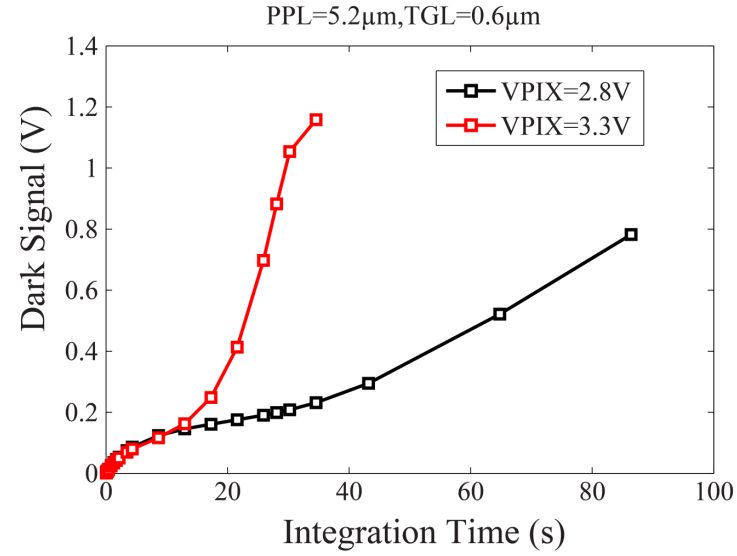

Figure 5-7: HC injection comparison for different source follower drain voltages.

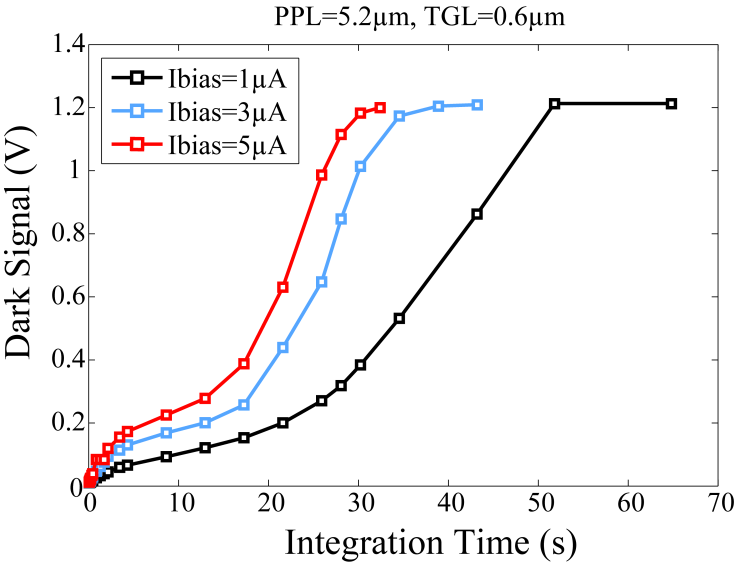

Figure 5-8: HC injection comparison for different source follower biasing currents.

integration time increase, the FD node voltage decreases, then the source follower V_{DG} differences for VPIX=3.3V and VPIX=2.8V will become important for the hot carrier effect. The VPIX=3.3V provides a larger V_{DG} for an high electric field, which induces a much larger hot carrier injection in for longer integration times than for the situation VPIX=2.8V.

5.4.2 Current Dependency

Not only the drain voltage of the source follower, but also the source follower biasing current (I_{bias}) influences the HC effect of 4T pixels [5.11, 5.13]. The amount of I_{bias} determines the number of electrons flowing through the high electric field region. An increased bias current induces higher minority carrier's generation along with the substrate current. Therefore, the collected hot carriers in the PPD are also dependent on the current of the source follower.

Figure 5-8 compares dark signal performance for three different Ibias biasing conditions (1μA, 3μA, 5μA). From the measurement results, it is clear that with the same integration time, a larger I_{bias} value will result in much more dark signal. For I_{bias}=5μA, the dark signal is saturated at an integration time of about 32s; for I_{bias}=3μA, the dark signal is saturated at 38s; for I_{bias}=1μA, the dark signal is saturated at 50s. The higher I_{bias} value not only contributes to the number of electrons that flow directly to drain region of source follower for HC injection, but also increases the V_{GS} of the source follower. Therefore, the V_{DS} of the source follower is enlarged with a large bias current, which also results in a more severe hot carrier injection mechanism.

5.4.3 Temperature Dependency

Low temperature operation of MOS devices, which offers many advantages over room temperature operation, is being used for both space and commercial applications. The advantages offered at low temperatures include lower carrier velocities, lower junction leakage, better sub-threshold turn-off, etc. [5.17, 5.18]. As a thermally activated process, generation of leakage current in photodiodes should have the following temperature dependency [5.19, 5.20]:

$$D = AT^m \exp(-E_a / nkT) \tag{5-1}$$

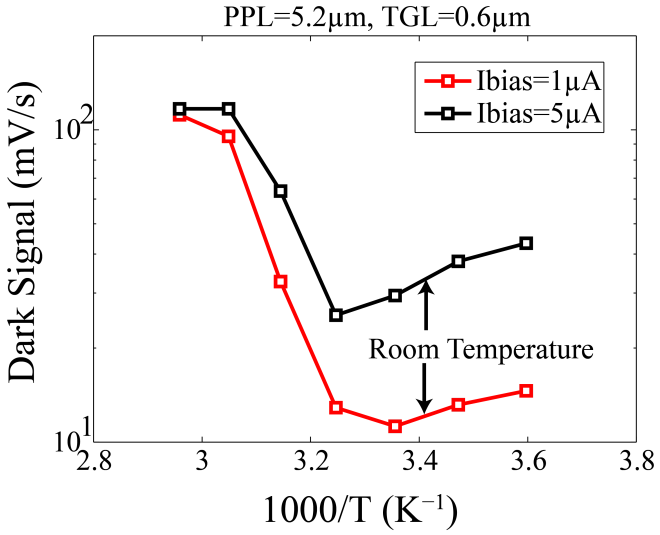

Figure 5-9: Arrhenius plot for HC injection under different current biasing.

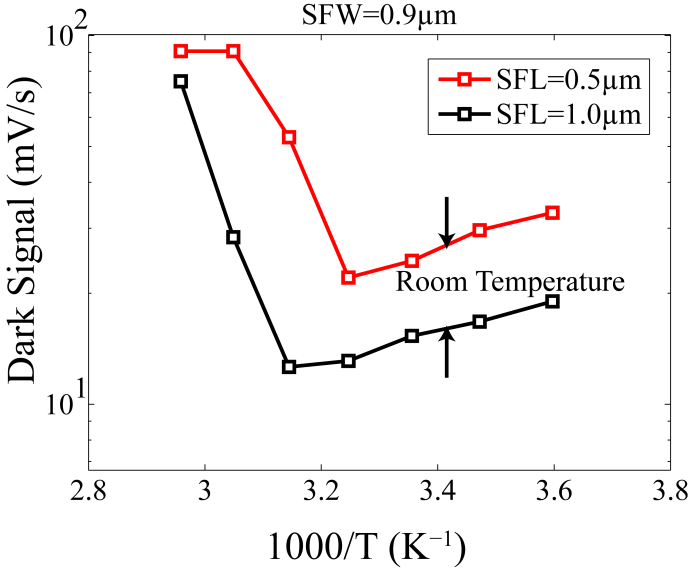

Figure 5-10: HC injection comparison for different source follower lengths.

where D is the leakage dark current in (e/s); A is a constant; T is the absolute temperature; E_a is the leakage generation activation energy which is positive;

and m is a constant that underlines the degree up to which D is temperature dependent and which is larger than 1 for dark current generation. Therefore, there is an Arrhenius equation as follows:

$$\ln(D) = \ln A + m \ln T - \frac{E_a}{nkT} \tag{5-2}$$

which means the dark current will increase with an increase in temperature. However, considering the hot carrier effect, the degradation of the device becomes significantly worse at low temperatures [5.21, 5.22]. Temperature measurement is an effective tool for verifying the HC effect existence in a pixel. The Arrhenius plot results are shown in Figure 5-9. The temperature was changed from 5°C to 65°C in 10°C increments. At high temperatures, the dark signal increases as temperature increases. The thermal activated leakage signal is dominant for both I_{bias}=1μA and I_{bias}=5μA at high temperatures. At low temperatures, the HC injection carrier is dominant since the measured dark signal does not decrease with decreasing temperature. For I_{bias}=5μA, the dark signal even increases with decreasing temperature. In the last section, the HC effect dependency on current biasing is already proved. In this temperature measurement, the I_{bias}=5μA pixel biasing also performed higher HC injection than I_{bias}=1μA. The temperature performance of the pixel is a strong evidence of the hot carrier mechanism since the mean-free path of hot carriers is longer at lower temperatures [5.13]. The other temperature measurements shown in Figure 5-10 are for the different source follower length designs. As expected, decreasing the length of the SF will increase the electric field of the SF drain end. The HC injection will be increased with length reduction.

5.5 Summary

A study of the hot carrier effect is presented in this chapter. The hot carrier introduced dark signal significantly degrades the CMOS image sensor performance. In this chapter, possible generation mechanisms of the hot carrier effect are analyzed based on MOSFETs in 3T and 4T pixel devices. Using the measurement results, its voltage, its current, and its temperature dependency the hot carrier effect in 4T pixels are further verified. In future work, as pixel size

shrinks, the design and process aspects of the optimization method will need to be investigated to completely eliminate the hot carrier effect. Since lowering the power supply will decrease the output swing of the pixel, a new solution needs to be proposed to solve the influence of the hot carriers.

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Chapter 6

Summary and Future Work

In this thesis, a few fundamental characteristics of pinned photodiode CMOS pixels are presented. In Chapter 3, the pinning voltage, transfer gate "OFF" potential barrier is characterized based on the PPD electron injection method. In Chapter 4, the image lag related pixel characterization and optimization are implemented. In Chapter 5, a preliminary in-pixel hot carrier effect study is presented based on test chip measurement results. In this final chapter, the main findings and contributions of this thesis will be summarized.

6.1 Summary

Regarding the potential based PPD-TG-FD structure characterization

- Both the pinning voltage measurement method [6.1] and feedforward measurement method [6.2] are potential-based characterization methods. Potential-based characterization methods can be used to characterize a few potential steps of the PPD-TG-FD structure. With the increase of the

injection voltage, the potential steps can be extracted from low to high voltages.

- The pinning voltage of the PPD can be characterized by the potential based characterization method when the transfer gate high voltage (VTG_H) is large enough (as shown in Figure 3-11). If the VTG_H is not large enough, the TG "ON" potential barrier will hamper the PPD to be completely depleted to measure V_{pin}.

- Both the PPD pinning voltage and the TG "OFF" potential barrier influence the maximum full well capacity of the pixel. The TG "OFF" potential barrier height can be characterized by potential-based characterization methods with a parameter V_b extraction. V_b is defined as the potential difference between zero PPD injection voltage and the TG "OFF" potential barrier. With the TG "OFF" potential barrier characterization for certain biasing conditions and without limitation of the readout circuitry, the maximum full well capacity of the PPD-TG also can be extracted with the pinning voltage measurement.

- In addition to the transfer gate low voltage (VTG_L) and fabrication process options, the pixel design and operation conditions can also influence the TG "OFF" potential barrier. In our testchip, due to the short gate effect and the DIBL effect, the TG length and FD reset voltage can modulate the TG "OFF" potential barrier. Both decreasing the TG length and increasing the FD reset voltage can decrease the TG "OFF" potential barrier. From another aspect, using the TG "OFF" potential barrier characterization method, determining whether the test pixel is suffering from the DIBL effect is easy to justify. Furthermore, considering the narrow gate effect, decreasing the TG width can also increase the TG "OFF" potential barrier.

- Using the potential-based pinning voltage measurement, with the injection voltage increasing, based on the classic MOSFET model, the TG "ON" operation mode will change from a strong inversion to weak inversion and even enter the depletion mode. Using the injection voltage differences between the TG inversion point and the weak inversion point, ϕ_{fp} of the

TG channel can be extracted, which means the channel doping concentration N_a and gate oxide thickness t_{ox} can be derived based on the measurements.

Regarding the image lag characterization of the 4T pixel

- To reduce the image lag, the potential barrier and/or pocket around the PPD-TG intersection part should be minimized by process and layout.

- For the same process barrier and TG design situation, the transfer time limited image lag is another main source of image lag especially for large PPDs. For high speed applications, a large photosensitive area and a short transfer time are required at the same time, which poses a high image lag performance demand on the pixel design.

- Generating extra electric fields in the charge transfer direction and decreasing the charge transfer distance of the PPD, can decrease the charge transfer time in the PPD. The PPD shape can influence both the electric field and transfer path. In our test chip, two non-traditional photodiode shapes are implemented. From the measurement result it can proved that both the “W” shaped and “L” shape PPD can decrease the charge transfer time. For the same transfer time, the image lag in these two pixels is decreased drastically.

- The special shaped PPD, like the “W” or “L” shape, could decrease the image lag for large PPD pixels. However, the detailed angle and size of these special shapes need to be well optimized to achieve an equivalent performance such as light sensitivity, dark current, and full well capacity.

- The transfer gate is one of the most important in-pixel components, especially for the charge transfer process. The TG voltage influences the CTI by modulating the surface potential of the channel. In addition to the TG voltage, the transfer gate shape can also influence the image lag performance by changing the fringing field underneath the transfer gate. The “T” shape and “Pi” shape TG designs can not only influence the full well capacity of the PPD, as mentioned in Chapter 3, but can also improve

the charge transfer efficiency by adding the gate extension towards the PPD.

- To design an "ideal" pixel with a relatively large pitch, the PPD design should be a tradeoff between light sensitivity and image lag performance. The proposed "W" shape could combine these two aspects. The transfer gate design should be optimized for charge transfer and full well capacitance. A short length of the transfer gate cannot comply with a high potential barrier when transfer gate is "OFF", but does neither result in a better CTE. A proper length of the transfer gate should be found, depending on certain process parameters to avoid the DIBL effect. To further increase the electric field in the center of PPD, the "T" and "Pi" shape transfer gate can be used to improve the CTE with a little sacrifice in light sensitivity performance.

Regarding the hot carrier degradation of the 4T pixel

- The hot carrier effect will degrade the dark signal performance of the pixel drastically. In CMOS image sensors, the reported hot carrier sources are the transfer gate [6.3] and source follower [6.4]. In this thesis, the pinned photodiode 4T pixel hot carrier is investigated based on our test chip measurement result.

- In our test chip, the hot carriers are not be measured from the PPD of pMOS transistor pixel, only from the nMOS transistor pixel. This result shows that the source follower is the dominant source of the measured hot carrier effect in this test chip. Although the detailed mechanism of hot carrier in the source follower cannot be confirmed completely, it can be deduced that the hot carrier either gains enough energy to surmount the Si/SiO_2 achieved by the FD node, or the hot carrier will diffuse into the substrate. The hot electrons diffused into the substrate have the possibility to be absorbed into either the PPD or FD node.

- Since the hot carriers are generated by the source follower in the measured pixel, the measured hot carriers exhibit a strong dependency on the supply voltage of the source follower, the biasing current of the source follower, and temperature. Firstly, lowering the drain supply voltage of

the source follower can decrease the measured hot carriers of the PPD, even though this will also decrease the output swing of the source follower. Secondly, lowering the biasing current of the source follower can also decrease the measured hot carriers in the PPD, since this decreases the number of electrons flowing through the high electric field region of the source follower. Last but not the least, as the hot carrier effect occurs in all devices, hot carriers have a different temperature dependency with normal leakage dark current. The hot carrier effect becomes more dramatic at low temperatures. Therefore, the measured dark signal in our device can find the minimum temperature value, which is a tradeoff between leakage current and the hot carriers. Increasing the temperature beyond this point (around 30°C in our measurement) shows that the leakage current increases with temperature and becomes the dominant source of dark signal, hence overall dark signal increases with temperature. Decreasing the temperature from this minimum point also results in an overall increase in dark signal since the hot carrier effect becomes the dominant dark signal source.

6.2 Future Work

This thesis has focused on the pinned photodiode CMOS pixel from three different aspects. Nearly all the important performances parameters of image sensors are related to the pixel design. There are still many related topics worth to further investigating in future work.

Study of the transfer gate and hot carrier effect by statistical analysis

In this work, two test chips with 80 different pixel variations have been investigated. However, one pixel type only contains 80 pixels, which is not enough for statistical research. In future work, implementing a larger pixel array per pixel design would allow for statistical analysis of pixel characterization. The pixel variation of the TG “OFF” and “ON” potential barriers could be investigated using statistical histogram analysis to see the process variation of the transfer gate. In addition to the transfer gate potential, the hot carrier effect mechanism in the source follower cannot be completely

confirmed. In our testchip, the hot carriers in the small pixel array already exhibit a spatial non-uniform distribution, thus it is worth to further investigate the physical mechanism of the hot carrier with a large number of pixels.

Optimization of the transfer gate parameter extraction method for different process implementations

In Chapter 3, using the proposed extraction method for the doping concentration of the transfer gate channel and oxide thickness, the MOS model can fit the measurement result very well. Since the method proposed by [6.5] is based on a different process than is used in this thesis, the extraction method in this thesis could be further optimized by studying more technology cases. Therefore, a more universal transfer gate related extraction method should be found.

Study of the pixel characterization and optimization for other pixel structures

The study of the pixels in this thesis is mainly based on the 4T pixel PPD-TG-FD structure. However, current pixel designs reflect process improvements such as backside illumination (BSI) technology and design variation such as the global shutter pixel, or even EMCMOS. The global shutter pixel normally adds an extra transfer for exposure control and anti-blooming. The EMCMOS, on the other hand, uses more transfer gates for electron multiplication in the charge domain. All these pixel variations pose new challenges for pixel level characterization and modeling work.

For example, in terms of dark current performance, the FD node suffers from a much larger current than the PPD. For a normal rolling shutter image sensor, the dark current in the FD node is not a serious issue since the FD is reset before the charge transfer. However, for the global shutter pixel, some of them such as the 5T global shutter pixel [6.6, 6.7] use the floating diffusion as analog memory, which suffers from a high dark current due to the heavily doped junction. Even using an extra capacitor [6.8] or pinned storage diode [6.9, 6.10] as the storage node, the measured dark current is still higher than the rolling shutter image sensor. In future work, an optimized solution for dark current reduction in the FD node or other storage nodes should be

considered from both the process and design aspects.

As mentioned in Chapter 5, in our test chip, the pMOS source follower pixel does not show the hot carrier effect, which can lower the dark signal. The in-pixel pMOS transistor not only can avoid the hot carrier effect, but also has the advantage of noise performance [6.11, 6.12]. In future work, the pixels with a pMOS source follower or even a hole based photodiode can be investigated and optimized further especially regarding noise, speed, output swing and fill factor aspects.

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Summary

This thesis gives an insightful analysis of the pinned photodiode 4T CMOS pixel from three different aspects. Firstly, from the charge accumulated aspect, the PPD full well capacity and related parameters of influence are investigated such as the pinning voltage, and transfer gate potential barrier. Secondly, from the charge transfer aspect, the image lag performance of 4T CMOS pixels is characterized and optimized. Thirdly, from the dark signal aspect, the hot carrier effect in the 4T CMOS pixel source follower is characterized and analysed.

In Chapter 1, a brief overview of the image sensor development is given. Two types of image sensors are compared: the charge coupled device (CCD) and the complementary metal-oxide-semiconductor (CMOS) image sensor. Since system integration is one of important advantages of CMOS image sensors, the CMOS image sensor is considered from the device, circuit and system level. In this thesis, the research is focused on pixel design at the device level. To further understand and improve the performance of the pixel, two test chips are implemented and a few pixel level parameters are characterized and analysed in this thesis.

Chapter 2 introduces the 4T CMOS active pixel. First, the photodiode is presented on the basis of theory and optimization. Next, as an improvement of the photodiode, the pinned photodiode (PPD) is then presented for CMOS image sensor pixel design. The main advantages of the PPD are better noise characteristics, and dark current performance compared with the photodiode. A few important performance specification parameters, e.g. dynamic range, full well capacity, and image lag, are introduced and some of them are discussed further in the following chapters.

In Chapter 3, two potential based characterization methods named the pinning voltage measurement and feedforward effect measurement are used to characterize a few potential steps in the PPD-TG-FD structure. To investigate the influence of different pixel design variations in more depth, two test chips with different fabrication processes are implemented which each contain 80 different pixel designs. As an important parameter of the PPD, the pinning voltage of the PPD does not only influence the charge transfer process but also influences the full well capacity. In addition to the pinning voltage, the TG “ON” and “OFF” potential can also influence the charge transfer process and full well capacity. Using the pinning voltage measurement, methods of estimation and extraction the TG “ON” potential and the transfer gate related process parameters such as channel doping concentration and oxide thickness are proposed based on the classic MOS model. The TG “OFF” potential barrier can also be extracted from the feedforward effect measurement without any FD node capacity limitation. From our testchip measurement results it can be found that the TG “OFF” potential barrier is not only determined by the transfer gate low voltage, but can also be influenced by the transfer gate length, width, and FD node reset voltage in certain design and process cases. With both the pinning voltage and transfer gate potential barrier characterization, the full well capacity of the PPD is discussed further in this chapter.

Chapter 4 is focused on image lag performance. To optimize the image lag performance of the large photodiode, in addition to the transfer gate potential barrier optimization, changing the photodiode shape can also help to speed up the charge transfer process without changing the manufacturing process. A few different photodiode shapes are implemented for image lag optimization. Along with the photodiode optimization, the influence of the transfer gate

dimension, voltage and FD node on the image lag are also discussed in this chapter. A “T” shape transfer gate pixel design of the test chip is verified, which can increase the charge transfer efficiency of the pixel. From the measurement result it can be found that a longer transfer gate does not necessarily achieve a lower image lag. The transfer gate length can also influence the floating diffusion capacity. The potential of transferred electrons in the FD node will influence the lag after the charge transfer process.

In Chapter 5, the hot carrier mechanism induced dark signal is investigated based on the 4T pixel. As with the hot carrier mechanism in the MOSFET, the source follower and transfer gate in the 4T pixel have the possibility of inducing hot carrier injection in certain process, design and application cases. In our test chip, the hot carrier injection can be found in the nMOS source follower. In the same testchip, replacing the nMOS source follower with a pMOS can prevent the hot carrier effect. Based on further measurement results, the 4T pixel hot carrier effect dependency on the voltage, current and temperature are presented, which can also confirm the hot carrier injection occurrence in the test structure.

Chapter 6 summarizes the main work in this thesis based on three different aspects. Furthermore, some proposals are given for the possible research considerations for future work in this field.

Samenvatting

Deze thesis geeft een inzichtelijke analyse van de pinned photodiode 4T CMOS pixel vanuit drie verschillende aspecten. Als eerste, vanuit het aspect van lading ophoping, wordt de full well capaciteit van de PPD (Pinned Photodiode) en gerelateerde parameters die van invloed zijn onderzocht, zoals de pinning voltage, en transfer gate potential barrier. Als tweede, vanuit het aspect van lading transport, wordt de image lag van 4T CMOS pixels gekarakteriseerd en geoptimaliseerd. Als derde, vanuit het aspect van donker signaal, wordt het hot carrier effect in de source follower van de 4T CMOS pixel gekarakteriseerd en geanalyseerd.

In Hoofdstuk 1, wordt een kort overzicht van de ontwikkeling van beeldsensoren gegeven. Twee type beeldsensoren worden vergeleken: het charge coupled device (CCD) en de complementary metal-oxide-semiconductor (CMOS) beeldsensor. Omdat systeem integratie één van de belangrijke voordelen van CMOS beeldsensoren is, is de CMOS beeldsensor benaderd op component, circuit en systeem niveau. In deze thesis is het onderzoek gericht op pixel ontwerp op component niveau. Om de werking van de pixel verder te begrijpen en te verbeteren, zijn er twee testchips

geïmplementeerd en zijn er enkele parameters op pixel niveau gekarakteriseerd en geanalyseerd in deze thesis.

Hoofdstuk 2 introduceert de 4T CMOS actieve pixel. Eerst wordt de fotodiode geïntroduceerd op basis van theorie en optimalisatie. Vervolgens, als verbetering op de fotodiode, wordt de pinned photodiode (PPD) geïntroduceerd als pixel ontwerp voor CMOS beeldsensoren. De grote voordelen van de PPD zijn betere ruisgedrag, en lekstroom prestaties in vergelijking met de fotodiode. Enkele belangrijke prestatie specifieke parameters, zoals dynamisch bereik, full well capaciteit, en image lag, worden geïntroduceerd en sommige van deze worden verder besproken in de volgende hoofdstukken.

In Hoofdstuk 3, worden twee methodes gebaseerd op potentiaal karakteristieken, namelijk de pinning voltage en de mate van het feedforward effect, gebruikt om een paar potentiaal stappen in de PPD-TG-FD structuur te karakteriseren. Om de invloed van verschillende pixel ontwerp variaties verder te onderzoeken in de diepte, zijn er twee testchips met verschillende processen geïmplementeerd, welke elk 80 verschillende ontwerpen bevatten. Als belangrijke parameter van de PPD, wordt de pinning voltage van de PPD niet alleen beïnvloed door het proces van lading overbrenging maar ook door \ de full well capaciteit. Naast de pinning voltage, kan de TG “AAN” of “UIT” potentiaal ook het proces van lading overbrenging en de full well capaciteit beïnvloeden. Op basis van metingen van de pinning voltage, worden methodes voor het schatten en het uitlezen van de TG “ON” potentiaal en transfer gate gerelateerde proces parameters, zoals de dopingconcentratie in het kanaal en de oxide dikte, voorgesteld op basis van het klassieke MOS model.

In Hoofdstuk 4 wordt gefocust op image lag prestaties. Om image lag van een grote fotodiode te optimaliseren, naast het optimaliseren van de transfer gate potentiaal barrière, kan het veranderen van de vorm van de fotodiode helpen bij het proces van lading overbrenging zonder het productieproces aan te passen. Verschillende vormen fotodiodes zijn geïmplementeerd ten behoeve van image lag optimalisatie. Naast optimalisatie van de fotodiode, worden ook de invloed van de transfer gate dimensies, - spanning en - FD node op de image lag in dit hoofdstuk besproken. Een “T” vormig transfer

gate pixel ontwerp op de testchip, welke de efficiëntie van ladingsoverdracht van de pixel kan verhogen, wordt geverifieerd. Uit metingen kan worden verondersteld dat met een langere transfer gate niet per se een lagere image lag kan worden bereikt. De lengte van de transfer gate kan ook de capaciteit van de floating diffusion beïnvloeden. De potentiaal van overgebrachte elektronen in de FD node zal het proces van ladingsoverdracht beïnvloeden.

In Hoofdstuk 5, wordt de lekstroom, geïnduceerd door het hot carrier mechanisme, onderzocht op basis van de 4T pixel. Zoals bij het hot carrier mechanisme in de MOSFET, hebben de source follower en de transfer gate in de 4T pixel ook de mogelijkheid, om in bepaalde proces -, ontwerp - en applicatie gevallen, hot carrier injectie te induceren. In onze testchip kan er hot carrier injectie gevonden worden in de nMOS source follower. In dezelfde testchip kan het vervangen van de nMOS source follower door een pMOS source follower, het hot carrier effect voorkomen. Op basis van verdere meetresultaten, wordt de afhankelijkheid van het hot carrier effect van de 4T pixel van spanning, stroom en temperatuur gepresenteerd, welke tevens de aanwezigheid van hot carrier injectie kunnen bevestigen in de teststructuur.

Hoofdstuk 6 vat het gehele werk in deze thesis op basis van de drie verschillende aspecten samen. Daarnaast worden verschillende voorstellen gedaan voor verdere onderzoeksmogelijkheden voor toekomstig werk in dit veld.

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List of Publications

Journal Papers

Y. Xu, X. Ge, and A. J. P. Theuwissen, "Hot Carrier injection analysis and optimization of the source follower in 4T CMOS pixels," submitted to *IEEE Transactions on Electron Devices*.

Y. Xu, X. Ge, and A. J. P. Theuwissen, "A potential based characterization of the transfer gate in CMOS image sensors," accepted to *IEEE Transactions on Electron Devices* (will be published in Jan. 2016).

Y. Chen, **Y. Xu**, A. J. Mierop, *et al.*, "Column-parallel digital correlated multiple sampling for low-noise CMOS image sensors," *IEEE Sensors Journal*, vol. 12, pp. 793-799, 2012.

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Y. Xu, X. Ge, and A. J. P. Theuwissen, "Investigating transfer gate potential barrier by feed-forward effect measurement," presented at *International Image Sensor Workshop*, Vaals, the Netherlands, 2015, pp. 116-120.

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Y. Xu, A. J. Mierop, and A. J. P. Theuwissen, "A CMOS image sensor with charge domain interlace scan," presented at *IEEE Sensors Conference*, Hawaii, USA, 2010, pp. 123-127. **(Best Student Paper Award)**

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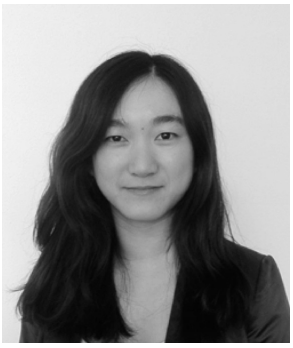

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