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Position-controlled epitaxial III–V nanowires on silicon

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Abstract
We show the epitaxial integration of III–V semiconductor nanowires with silicon technology. The wires are grown by the VLS mechanism with laser ablation as well as metal–organic vapour phase epitaxy. The hetero-epitaxial growth of the III–V nanowires on silicon was confirmed with x-ray diffraction pole figures and cross-sectional transmission electron microscopy. We show preliminary results of two-terminal electrical measurements of III–V nanowires grown on silicon. E-beam lithography was used to predefine the position of the nanowires.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Higher operation speeds in silicon devices have been achieved by reducing the device dimensions [1]. To make substantial progress, however, effort has been put into the investigation of semiconductor materials that intrinsically have higher mobilities, such as GaAs, InP, and InAs [2]. An additional advantage is that most of the III–V compound semiconductors have a direct bandgap, enabling optoelectronic devices, such as LEDs and lasers [3]. We must note, however, that light emission has also been observed from quantized silicon structures [4]. Nowadays, silicon is the standard for the electronics industry. For mainstream applications, silicon cannot be replaced by III–V compound technology because of the inherent cost and availability of these materials. A better approach would be to combine the best parts of these different technologies; i.e. the monolithic integration of the (superior) III–V semiconductors into the mature silicon technology. There are some clear advantages for both worlds. However, fundamental issues such as lattice and thermal expansion mismatch and the formation of antiphase domains have prevented the industrial epitaxial integration of III–V with group IV semiconductors [5, 6]. These problems could be avoided by reducing the contact area of the III–V crystals and by making vertical devices. In this sense, the crystal lattice of the III–V material will be elastically deformed near the interface, and due to the small dimension the strain could be accommodated at the nanowire surface. In addition, since per crystallite there will only be one nucleation site, we will not suffer from antiphase or twin boundaries.

Recently, III–V semiconductor nanowires have been grown on Si [7] and Ge [8] substrates. The crystallographic relation between InP wires and the Ge(111) substrate has been examined in detail with (high-resolution) x-ray pole figures and transmission electron microscopy (TEM) [8]. Such detailed studies have so far not been presented for III–V wires grown on silicon. Moreover, for any application the ability to control the position of the wires and the electrical properties of the III–V/Si interface is a prerequisite.

In this paper, we show the epitaxial growth of a wide range of III–V materials on silicon by pulsed laser deposition (PLD) and metal–organic vapour phase epitaxy (MOVPE). It is shown that GaP, GaAs, InP and InAs can be grown on silicon with a lattice mismatch ranging between 0.4% (GaP) and 11.6% (InAs). The epitaxial relation between the wires and substrate was confirmed with x-ray diffraction pole figures and the quality of the interface was studied by using cross sectional transmission electron microscopy. Importantly, the electrical properties of the III–V/silicon interface are inherently affected by the structural quality of the junction, but also by fundamental issues, such as polarity and the band-offset between the III–V semiconductor and silicon.

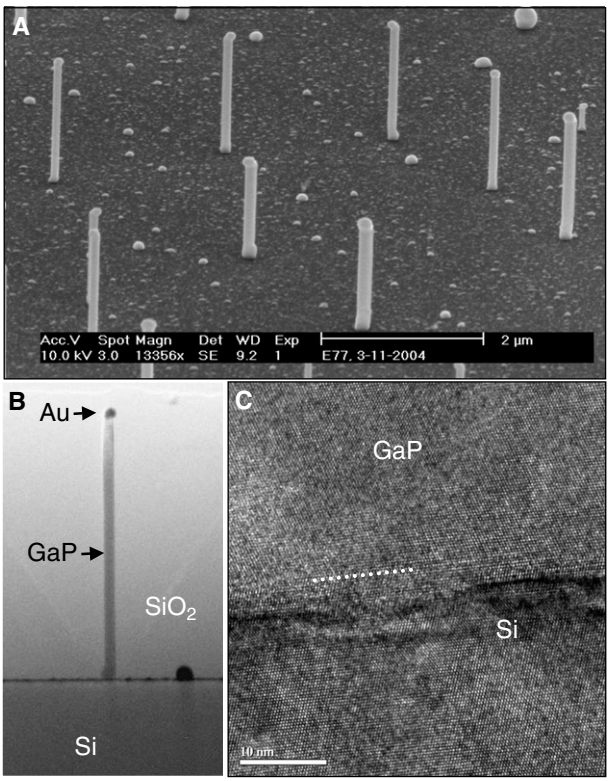

Figure 1. (a) GaP nanowires grown epitaxially on Si(111) by laser ablation. (b) Cross-sectional TEM image of a single GaP wire on Si and (c) a high resolution TEM image of the GaP–Si interface. A rotational twin dislocation is indicated with the dotted line.

We show preliminary two-terminal measurements on InP nanowires grown epitaxially on silicon. Finally, we used e-beam lithography to predefine the position of the catalyst particles from which the nanowires grow.

2. Experimental details

Nanowires were grown by the vapour–liquid–solid (VLS) growth mechanism [9], and Au was used as the catalyst. Prior to the deposition of a thin Au film the oxide on the silicon wafers was removed with a buffered hydrofluoric acid (BHF) etch. It is known that Au catalyses the oxidation of Si [10], and tens of nanometres of SiO_2 are formed on top of the gold at room temperature within a period of days. Just before growth the silicon oxide on top of the gold was removed with BHF. Alternatively, Au colloids with a mean diameter of 20 nm were spin-coated on the cleaned and etched Si substrates. The laser-ablation set-up used to grow the nanowires is similar to that reported in previous work [11]. The beam of an ArF laser ($\lambda = 193$ nm, 70 mJ/pulse, 2 Hz) is focused on a pressed III–V target (density 65%). The silicon substrate was placed on an Al_2O_3 block at the downstream end of a tube oven. The substrate temperature was in the range of 500–550 °C depending on the choice of material and an Ar background pressure was used of 140 mbar. The composition of the wires is in principle determined by the composition of the target.

Alternatively, MOVPE was used to grow nanowires. These wires were synthesized in an Aixtron 200 MOVPE reactor from $(CH_3)_3Ga$ (trimethylgallium, TMG), $(CH_3)_3In$ (trimethylindium, TMI), PH_3, and AsH_3 precursors in H_2 at a total pressure of 50 mbar in a total flow of 6.0 l min^{-1} (slm). The TMG and TMI molar fractions were in the range of 1.5×10^{-5} to 1.5×10^{-4}, and the PH_3 and AsH_3 molar fractions were varied in the range of 7.5×10^{-4} to 5.0×10^{-2}. During heating of the substrate a group V pressure was applied, and when the desired growth temperature was reached growth was initiated by opening the group III source.

For the characterization of the nanowires on silicon substrates, scanning electron microscopy (SEM), transmission microscopy (TEM) and x-ray diffraction were used. The samples for the cross sectional TEM were prepared by embedding the wires in 500 nm of SiO_2 by plasma-enhanced chemical vapour deposition. A focused ion beam (FIB) was used to cut and lift out the sample slice. Additionally, the samples were treated with low-angle, argon ion-milling thinning steps to obtain samples that were thin enough for the high-resolution TEM studies.

For two-terminal electrical measurements, InP nanowires, grown epitaxially on Si(111), were embedded in a 500 nm thick poly(methylmethacrylate) (PMMA) layer. After the PMMA was spun on, the sample was etched by reactive ion etching (RIE, with O_2) such that the tops of the wires were exposed. For n-InP wires a Ti/Al contact and for p-InP a Ti/Zn/Au top contact was evaporated through a shadow mask. The contact pad sizes were 150×150 μm^2, 100×100 μm^2, and 50×50 μm^2.

3. Results

In figure 1(A) a SEM image of GaP wires grown by PLD on a Si(111) substrate is shown. The wires have grown perpendicular to the substrate surface, indicating that the growth direction of the wires corresponds to the ⟨111⟩ direction. The typical dimensions are 180 nm for the diameter and 2 μm for the length, which appears to be uniform. The diameter is also constant through the wire, except for a short thickening at the base. All wires are terminated by a metal particle. Some gold islands are also found on the silicon surface. In order to study the crystallinity of the interface between the wires and the substrate, cross sectional TEM studies were performed. In total over ten GaP wire/Si substrate interfaces were studied. In figure 1(B) a TEM cross-section is shown for a single GaP wire on silicon. From energy-dispersive x-ray analysis (EDX) we found that the particle at the top of the wire and the particle on the silicon surface contain Au as well as Ga. In figure 1(C) the GaP–silicon interface can be seen in more detail in a high-resolution TEM image. The crystal planes continue from the Si substrate into the GaP wire, confirming the epitaxial growth. It is clear however that the interface between the GaP and the silicon is not flat. The wire/substrate interfaces show a typical roughness of 5–10 nm. We believe that this roughness is induced by the formation of a Au/Si eutectic prior to the nanowire growth. Due to intimate contact between the evaporated gold layer and the silicon, these two materials are alloyed during the heating of the substrate. This alloying was studied in more detail by heating an identical sample under identical conditions, i.e. 525 °C for approximately 1 h under an argon flow, but without

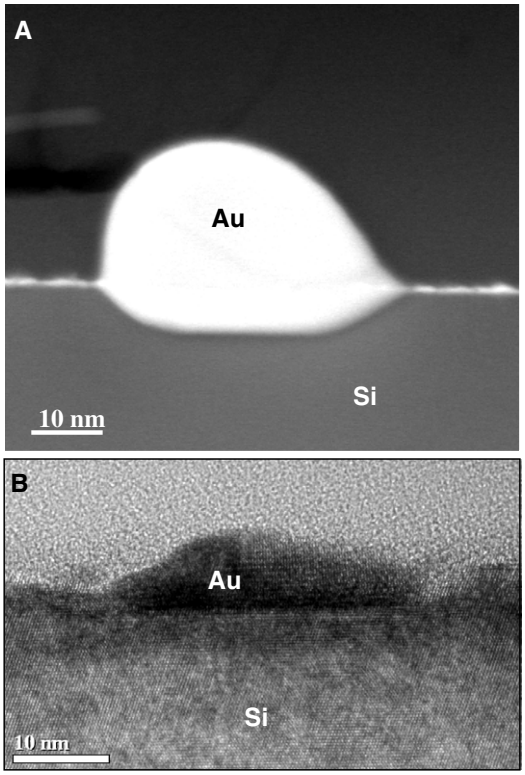

Figure 2. (a) High angle annular dark field (HAADF) TEM image of a Au particle on a Si(111) surface after annealing at 525 °C. (b) High resolution TEM image of another Au particle on the Si substrate.

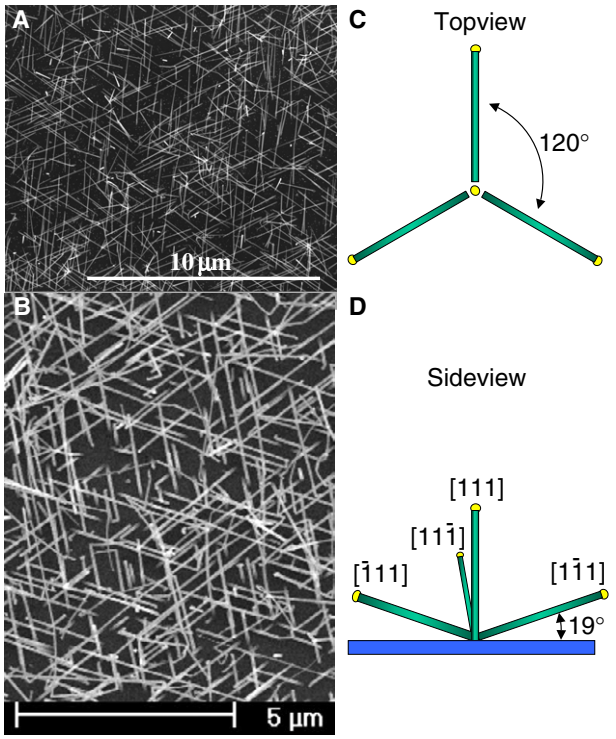

Figure 3. Top-view SEM images of (a) InAs, and (b) InP nanowires grown by MOVPE. The threefold symmetry of wires grown in the ⟨111⟩ direction on a (111) surface can be clearly seen. Wires grown perpendicular to the (111) surface can be seen as dots. (c) A schematic top view and (d) a side view to illustrate the four ⟨111⟩ directions in which the wires grow.

ablating from the target. In figure 2(a) a dark field and in 2(b) a high resolution cross sectional TEM image of a Au particle on a Si(111) is shown. The particles have sunk into the silicon substrate, thereby creating {111} facets with a different orientation than the initial (111) surface plane. When we then offer the group III and V materials to the gas phase, these atoms will dissolve in the Au/Si particle. When nanowire growth is initiated the Si will be excreted, giving rise to the rough interface as well as the formation of a thickened base.

In figure 3 top view SEM images are shown for (a) InAs, and (b) InP nanowires grown by MOVPE on Si(111). The three equivalent ⟨111⟩ growth directions of the wires can be distinguished. These orientations correspond to the four ⟨111⟩ directions typical for a (111) oriented crystal; one orientation perpendicular to the surface and three orientations having a 19° angle with the surface and having in-plane components at an angle of 120° from each other. A fraction of the wires is oriented perpendicular to the surface, and will appear as small bright spots in this top-view image. The fact that we have a large fraction of the wires growing in the three other ⟨111⟩ directions with in-plane components is, most probably, related to the formation of the other {111} facets during the alloying of the Au particle with Si. The nanowire growth can now be initiated on one of the side facets, resulting in an orientation which is not perpendicular to the surface. A similar mechanism was proposed for the growth of non-vertical InP nanowires on InP(100) [12]. For this system, the wires could be grown perpendicularly when the growth temperature was kept below the Au/In eutectic temperature. In analogy, the rough III–V/Si interface could possibly be avoided by using an alternative metal as catalyst that has a higher eutectic temperature than the Au/Si system (363 °C), such as Co (1170 °C) or Ni (966 °C). Another reason to replace Au is that it has a high diffusion coefficient in Si and it forms deep defect levels in Si [11].

To predetermine the position of the Au particles prior to the nanowire growth e-beam lithography and lift-off was used. The size of the metal particles was varied between 25 and 200 nm and the pitch was varied in the range 100–2000 nm. For these experiments a Au layer with a thickness of 1 nm was evaporated. In figure 4 SEM images of GaAs wires grown by MOVPE from an e-beam structured catalyst array are shown. The dot size and the pitch in these images are (a) 100 nm, 2 μm, (b) 50 nm, 750 nm, and (c) 25 nm, 2 μm. For the wires grown from the 50 and 25 nm particles the epitaxial growth is clear from the threefold in-plane symmetry. Typically, for the larger diameters (a) the Au islands tend to break up into more particles resulting in a growth of multiple wires per dot. From the smallest dot size (c) the wire growth is not always observed. This might be due to small variations in the processing; for these small dimensions some holes in the resist might not have been completely opened. For the 50 nm dots (b) we observe a growth of a single wire from almost every dot. By using the e-beam defined dots the fraction of the vertically grown wires is not very high.

The crystallographic relation between the silicon substrate and a large number of the III–V nanowires was studied by XRD pole figure measurements. This technique is explained in more

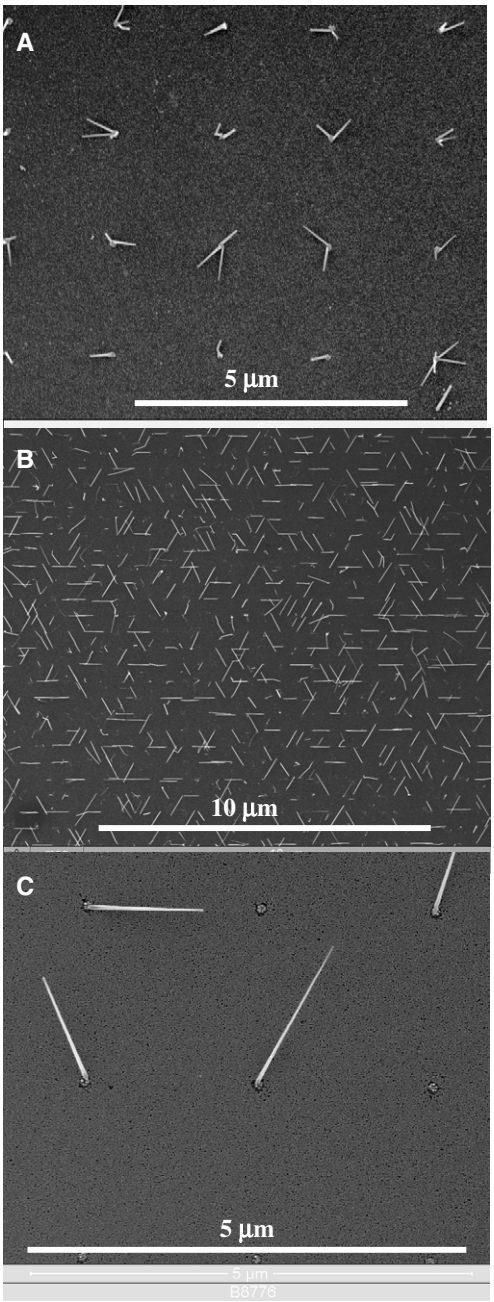

Figure 4. Top-view SEM images of GaAs nanowires grown by MOVPE from e-beam defined Au dots. The dot size and the pitch in these images is (a) 100 nm, 2 μm, (b) 50 nm, 750 nm, and (c) 25 nm, 2 μm.

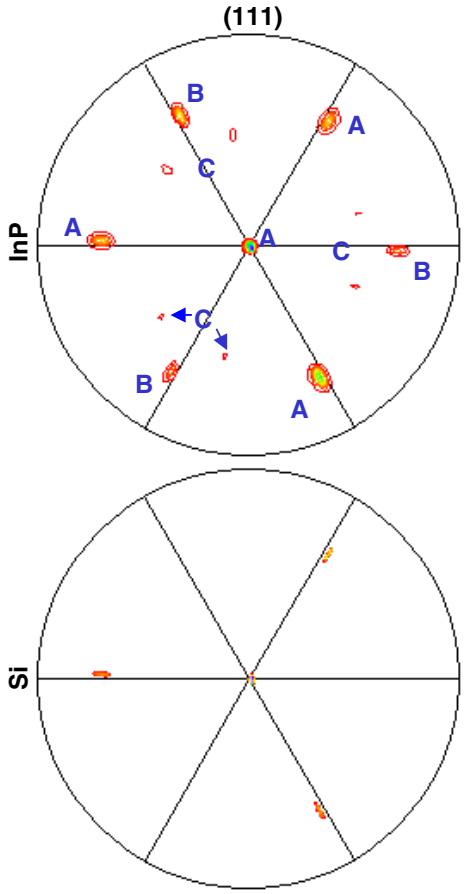

Figure 5. X-ray diffraction pole figures for the (111) reflections from the InP wires and the Si(111) substrate. The four peaks in the figure for InP(111) with identical orientation to the Si(111) pole figure correspond to reflection from epitaxially grown nanowires.

detail in previous work [8]. As an example, the pole figure for InP wires grown by MOVPE on Si(111) is shown in figure 5; the lattice mismatch for the InP/Si system is 8.1%. Pole figures were measured for the (111) and (200) reflections of the Si substrate and the III–V nanowires. For the InP(111) pole figure we observe four peaks, labelled with an A, corresponding to the same orientation as those in the Si(111) figure. These peaks indicate that the wires have grown epitaxially on the substrate. The three other peaks, that have a 180° in-plane rotation with respect to the peaks from the epitaxial wires, labelled with a B, arise from wires that have a rotational twin dislocation around the substrate surface normal vector. An example of such a twinning boundary is indicated in the TEM cross section (figure 1(C)) with a white dotted line. The small signals appearing closer to the centre of the figure (labelled C) originate from wires which have grown in one of the alternative ⟨111⟩ directions, having an angle of 19° to the surface, and that have a twin dislocation orthogonal to their longitudinal axis. The fact that the mirrored orientations give a smaller signal than the orientation identical to the substrate reveals that the density of twinning defects is low. With these pole figures the epitaxial relation between a range of III–V nanowires, such as GaAs, InP, and InAs, and the Si(111) substrate was confirmed.

As a final result, we want to discuss the electrical properties of the nanowire–silicon interface. To investigate this we provided an as-grown sample of InP wires (grown by MOVPE) on silicon with a spin-on PMMA layer acting as an insulator. Then a top metal contact was evaporated in order to measure the I–V characteristics of the Si/InP-nanowire/top-contact system (figure 6(a)). The density of the nanowires was approximately 80 wires per 10×10 μm^2. In figures 6(b) and (c) the I–V curves of the integrated InP nanowires on Si substrates are shown on a semi-logarithmic scale for 50 × 50 μm^2 top contacts measured at room temperature. Importantly, the measured currents scale linearly with the area of the top

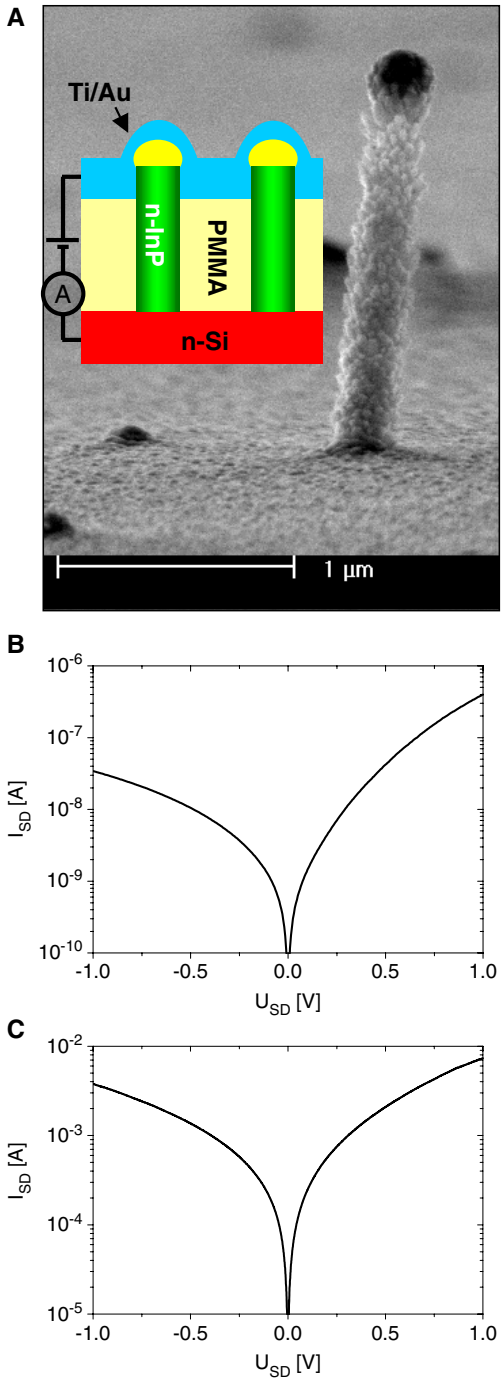

Figure 6. (a) SEM image of an n-InP wire protruding from the PMMA layer that has been electrically contacted with a Ti/Al metal stack. (b) *I*–*V* characteristic of p-InP nanowires grown on a highly p-doped Si substrate and (c) n-InP nanowires on a highly n-doped Si substrate.

contact. The *I*–*V* curve in figure 6(b) corresponds to p-doped InP nanowires grown on a highly doped p-Si substrate, and figure 6(c) to n-doped InP nanowires integrated on highly n-doped Si substrates. That means that in figure 6(b) only holes are involved in the current transport across the interface and thus the valence band offset between Si and InP is important. This holds for figure 6(c) for the electrons and the conduction band offset. From the measured *I*–*V* curves it can be seen that the *I*–*V* curve for the hole transport shows a stronger rectifying behaviour and generally lower currents while the one for the electrons does not exhibit a rectification and gives much higher (factor 10^5) currents. The different *I*–*V* behaviour of the n-doped and p-doped heterojunctions could be due to several factors. In the first place, neither the electron and hole concentrations are known nor the band alignment in this system. The quality of the III–V/Si interface should also be improved in order to quantitatively characterize the electrical transport at the heterointerface. Still, these preliminary results qualitatively suggest a higher valence band offset compared to the conduction band offset. This is in agreement with results in the literature [13] but care has to be taken in the interpretation because of different interface orientations and also defects in the overlayer growth due to lattice constant mismatch. To minimize the defect density, the nanowire heteroepitaxy is very promising, since it allows growing heavily mismatched semiconductors epitaxially on Si, which is not possible in 2D layer geometry.

To conclude, we have demonstrated that laser assisted VLS as well as MOVPE can be used to grow III–V semiconductor nanowires on silicon. The epitaxial growth of these wires was confirmed with x-ray diffraction pole-figures. With high-resolution TEM cross-sections we have shown that the interface can be rough. Electronic measurements reveal a good electrical contact and show different behaviour for n-doped and p-doped heterojunctions. The next challenge would be to have the wires growing in the ⟨100⟩ direction on Si(100) substrates to be compatible with present day silicon technology.

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