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A Switch-Bank Approach for High-Power, High-Resolution, Fully-Digital Transmitters

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***Abstract* — An implementation strategy for high-power, high-resolution, fully digital transmitters (DTX) is proposed. It is based on a high-speed CMOS controller featuring a high-density flip-chip interconnect to an LDMOS power MMIC containing large arrays of custom low-V_T LDMOS gate segments configured in RF-power switch banks. Using a two-level thermometer approach and a novel symmetric control scheme for the activation of the gate segments, a high-resolution 11-bit DTX switch bank is realized. It can provide peak RF powers > 10 W at 45 %/40 % peak drain/system efficiency at 3.525 GHz.**

***Keywords* — Transmitter, DTX, switch bank, flip-chip, CMOS, RFIC, LDMOS, RF, RF power, resolution, thermometer coding.**

I. Introduction

Digital transmitters (DTXs) hold many promises over traditional analog transmitters since they can offer higher system integration, (close to) frequency-agile operation, absence of quiescent currents, reduced memory effects, improved control of Doherty branches, and higher drain/system efficiencies. DTX has made enormous progress over the last decade, e.g., [1]–[7]. However, so far, DTX falls short in covering the needs of sub-7 GHz massive multiple-input and multiple-output (mMIMO) wireless network applications. These systems demand over 10 Watts of peak RF output power per antenna element and high resolution to handle wideband (> 200 MHz) modulated signals with sufficiently low quantization noise levels (< -55 dBc). In [8] RF output powers beyond 10 W were demonstrated, using a (two-chip) DTX approach featuring a digital CMOS controller that is bond wire connected with a RF-power-MMIC containing low-V_T, gate-segmented LDMOS output stages (Fig. 1(a)). However, its bond wire approach yielded several drawbacks:

- Only a limited number of LDMOS gate segments on the power-MMIC can be controlled.
- Mutual coupling between the bond wires causes deviations of individual LDMOS segment currents, yielding bit mismatch and bit-to-bit interactions.
- The bond wire interconnect limits the DTX control speed, thus putting bounds on the DTX operating frequency (f_c) and rise and fall times.

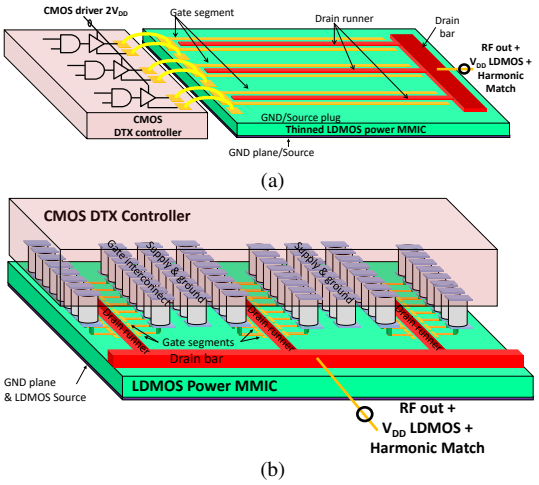

Fig. 1. Illustration of high-power DTX concepts: (a) Bond-wire-based prior-art [8]; (b) Proposed high-density flip-chip solution.

- It causes RF current redistribution in the switch bank due to the very coarse nature of gate segments and their activation.

The imperfections of the above severely degrade the smoothness of the ACW-to-RF-output voltage transfer in [8], reducing its resolution to only 5.7 effective bits and thus its ability to handle wideband modulated signals with high spectral purity.

To overcome these drawbacks, this paper introduces a revolutionary power-DTX implementation strategy. It utilizes a high-speed CMOS DTX controller placed directly on top of a customized power MMIC die, using a high-density flip-chip interconnect to control large arrays of high-breakdown ($V_B \approx 72$ V), low-threshold voltage ($V_T = 0.7$ V) LDMOS gate segments organized in switch banks (Fig. 1(b)). This approach allows for higher DTX operating frequencies and very fine gate-segmentation. All (other) connections to the DTX CMOS die (e.g., supplies, reference clock, and control) are routed over the LDMOS MMIC, which also offers improved grounding and decoupling of the CMOS controller by its through-wafer source plugs and back-side metallization (Fig. 1(b)). The proposed approach also allows the use of new activation schemes for the gate segments, avoiding RF current redistribution when changing the amplitude code word (ACW). This facilitates very smooth ACW-to-RF

* equal contribution

transfers and the creation of wideband RF output signals with high spectral purity. Although the realized CMOS-LDMOS DTX configuration in this work features 8 switch banks that can be configured into a more complex digital transmitter (e.g., an N-way Doherty), this paper focuses on the implementation and operation of the high-power, high-resolution DTX switch bank itself and its optimized segment activation.

II. A High-power, High-resolution DTX Switch Bank

To reach high spectral purity, sampling replicas must be placed far away from the in-band signal. By choosing the sampling frequency equal to the transmit (TX) frequency ($f_s = f_0 = 3.5\,\text{GHz}$), the sampling replicas fall into the baseband and the 2nd harmonic band which can be suppressed by the bias and digital class-C harmonic terminations [6].

The required switch bank resolution in terms of the number of bits can be estimated using the dynamic range equation, $\text{DR}\,(\text{dBc}) = 6.02N_B + 1.76 + 10\log\left(\frac{f_s}{2BW}\right) - \text{PAPR}$, when targeting quantization noise levels below −55 dBc in combination with modulation bandwidths of up to 200 MHz for TX signals having more than > 10 dB PAPR, at least 9 effective amplitude bits (N_B) are required. To have some leeway, this work targets an 11-bit switch-bank implementation.

A. Switch Bank Topology, Dimensioning, and Control

A single level of thermometer coding would yield 2047 gate segments, which is very challenging to implement in a (single) switch bank, even when using a high-density flip-chip approach. Hence, in this work, a multi-level thermometer coding is adopted, which uses 8 bits in the most significant bit (MSB) layer and 3 bits in the least significant bit (LSB) layer.

To enable the energy-efficient generation of wideband complex modulated signals, an 8-phase multi-phase operation is used [7], [9]. To improve the switch bank power utilization, each MSB unit cell can be activated with either the A or B clocks, having a relative phase offset of 45°. A global switch bank phase-mapper controls the phase selection (Fig. 3).

In the least significant bit (LSB) layer, the 3 bits are separately implemented for the A and B activations as a second thermometer-coded layer, giving a total of $(2^8-1)+2(2^3-1) = 269$ LDMOS gate segments in the switch bank that need to be controlled by CMOS drivers. Complementing every driver–gate-segment with alternating $2V_{\text{DD}}$ and V_{SS} connections provides a close-by driver return path (Fig. 2(b)), yielding in this switch-bank to 448 flip-chip interconnections.

Using a 40 µm flip-chip pitch, the high-resolution switch bank can be directly implemented as an LDMOS power transistor with gate segments on both sides along each drain finger/runner (Fig. 2(b)). In the lateral direction, we include 20 µm additional gate-drain separation on top of the 40 µm flip-chip pitch to avoid substantially increasing C_{GD}. With the above, the complete switch bank becomes 640 µm × 1300 µm.

B. Low-V_T, High-Voltage LDMOS for Power-DTX Operation

RF-power LDMOS devices are generally optimized for linear analog RF operation. As such, they demand V_{GS} swings as high

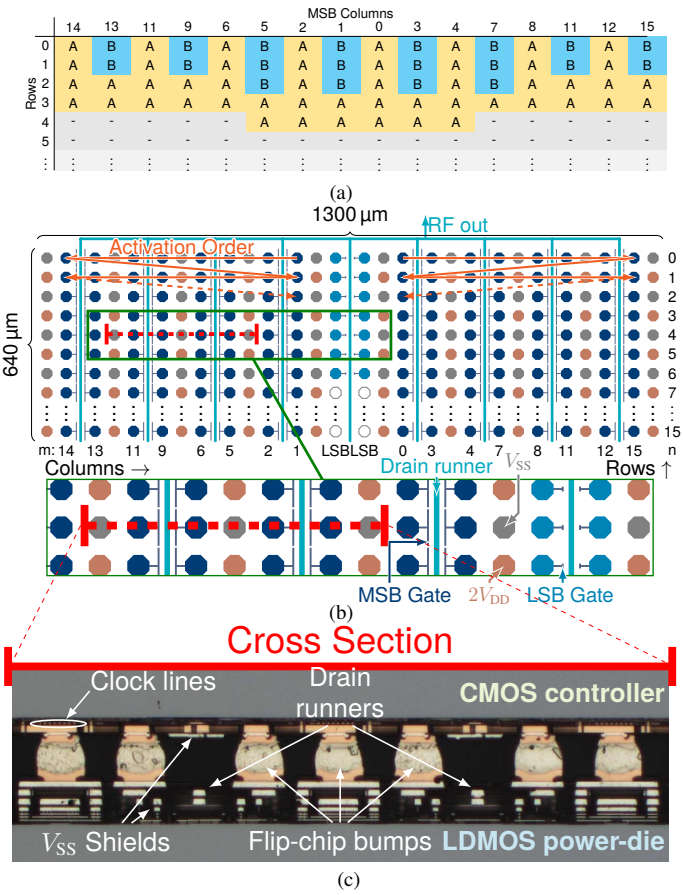

Fig. 2. (a) Example of an activation pattern; (b) Artist illustration of the high-resolution switch-bank layout with activation order; (c) Cross-section micro-photograph of the realized switch bank. The location of this cross-section is indicated as a red dashed line in the switch-bank layout.

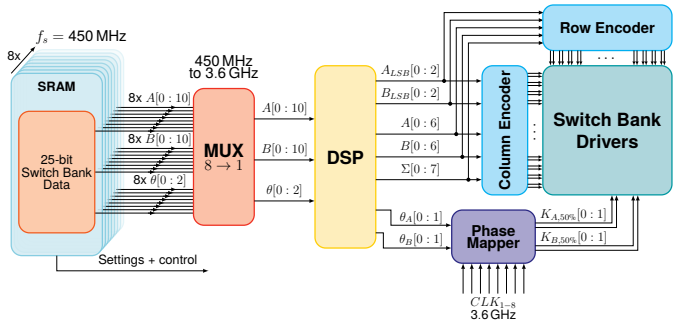

Fig. 3. Block diagram of the CMOS switch bank controller.

as 5 V to reach their I_{MAX}. DTXs using current scaling [7] require LDMOS gate segments that fully "switch-on/off" with a voltage swing that is compatible with high-speed digital drivers while still offering an excellent on/off-current ratio (in this work $> 10^7$). To achieve this, the LDMOS threshold voltage has been lowered to $V_T = 0.7$ V by reducing the LDMOS gate-oxide thickness and adjusting the channel doping. Fig. 4 shows that the modified g_m curve rises and falls steeply over a limited V_{GS} span (2× the V_{DD} of the high-speed CMOS 40 nm core devices), lowering the sensitivity of the switch-bank RF-current to the (actual) voltage provided by the CMOS drivers, thus lowering the impact of supply-voltage variation of the drivers.

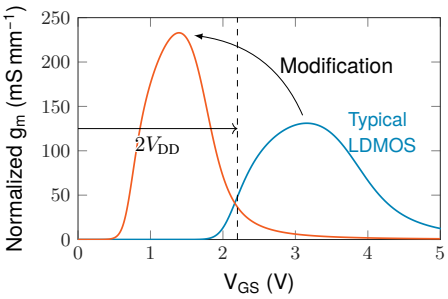

Fig. 4. The g_m of the modified (digital) low-V_T LDMOS used in this work compared to a typical (analog) RF-power LDMOS technology.

C. The CMOS–LDMOS Flip-Chip Interconnect

The flip-chip processing flow is based on a modified version of [10] and has been extended here for the digital-RF-power application. Fig. 2(c) gives a cross-section of the realized CMOS–LDMOS stack. It shows the copper under bump metallization on both dies and SnAg micro-bumps used in this flow. Since the entire die with its 8 switch banks measures 7 mm × 5.3 mm, special care has been taken to prevent bow and warpage of the thinned LDMOS die during the assembly, which is achieved by attaching it onto a copper-tungsten flange prior to the actual flip-chip bonding.

The flip-chip interconnect parasitics can be estimated by performing 2.5D EM simulations, illustrated in Fig. 5(b). Using close-by ground connections as a return path, the series inductive parasitic is limited to 44 pH for each LDMOS gate segment, with negligible mutual coupling. The total effective capacitive driver's load of an MSB segment is $C_L = 107$ fF, consisting out of $C_{GG} = 72$ fF and $C_{int} = 16.5$ fF (including the Miller multiplication of C_{GD}), and $C_{ESD} = 18.2$ fF. This is a huge improvement compared to the approach of [8], where a single driver is loaded by 2.41 pF. Namely, in [8], large LDMOS segment sizes are needed to account for the limited number of bond wire interconnects. Moreover, the series inductance in [8] was 620 pH, yielding an interconnect resonant frequency of 5 GHz. The proposed flip-chip approach has improved this parasitic resonance to 73 GHz.

D. High-Speed CMOS Driver Design

To minimize rise and fall times and enable full switching of the low-V_T LDMOS device segments, a 2.2 V swing is provided by CMOS using 40 nm core oxide devices in a house-of-cards topology without sacrificing reliability [11]. The preceding tapered buffer chains for the top and bottom devices and voltage-level shifter are DC-coupled and operate between V_{SS} to V_{DD} and V_{DD} to $2V_{DD}$. Special care was taken to match the upper and lower signal path delays to preserve the desired duty cycle. The resulting (for design-safety reasons over-dimensioned) driver chain can drive up to 150 fF while providing 10 %–90 % rise and fall times of 29 ps and 69 ps, respectively.

E. Smart Activation of the Switch Bank Gate Segments

In an analog (class-B) PA, the output stage transistor is driven by the time-continuous varying V_{GS}. In our DTX, each segment

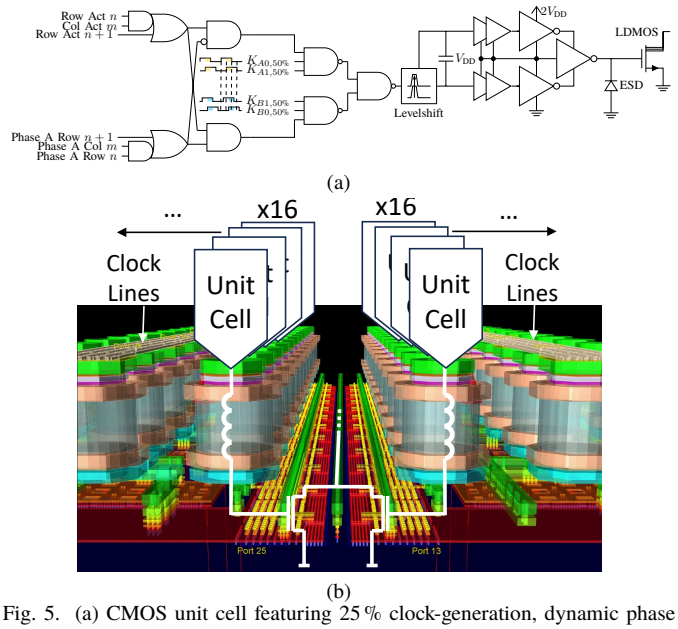

Fig. 5. (a) CMOS unit cell featuring 25 % clock-generation, dynamic phase allocation, and a stacked house-of-cards driver for the LDMOS gate-segments; (b) Unit cells connected through flip-chip bumps to LDMOS segments.

is individually controlled by its (digital) rectangular waveform. As such, a DTX modulates the number of activated segments instead of the driving V_{GS} amplitude [7]. Since the switch bank for a given operating frequency can be electrically large, the physical position of an activated gate segment matters. To realize a monotonic ACW-to-RF output transfer, the segments should be activated using a pattern that minimizes the redistribution of the RF output current. In this work, the activation with increasing ACW starts from the center segments and extends symmetrically to the outer ones, on a row-by-row basis (Fig. 2(b)). As such, it prevents irregularities, yielding a smooth and monotonic ACW-to-RF output signal transfer. The remaining linearity error due to, e.g., output stage compression can be compensated using DPD, which can be significantly relaxed due to the much smoother (and monotonic) behavior.

F. Dynamic Phase Allocation of the MSB Unit Cells

The MSB unit cell logic (Fig. 5(a)) is improved from [3], which now allows dynamic phase-selection of the A or B clocks in support of 8-phase DTX operation [7], [9]. It adds to the previously described symmetric activation of the gate segments, to also perform the phase allocation of the MSB cells in a strictly symmetrical manner, as is illustrated in Fig. 2(a) for $ACW_A = 400$ and $ACW_B = 160$. In addition, the included MSB logic also provides the aimed 25 % duty-cycle activation of an LDMOS output segment from the globally distributed 50 % duty-cycle input clocks provided by the switch bank's phase-mapper.

G. Expected Switch Bank Performance

The full DTX switch bank contains 11.5 mm of total LDMOS gate width ($W_{G,tot}$). The LDMOS can provide 0.22 A mm^{-1} when switched at $V_{GS} = 2.2$ V (see Fig. 4). When biased at 28 V, operating with 25 % RF duty-cycle (digital

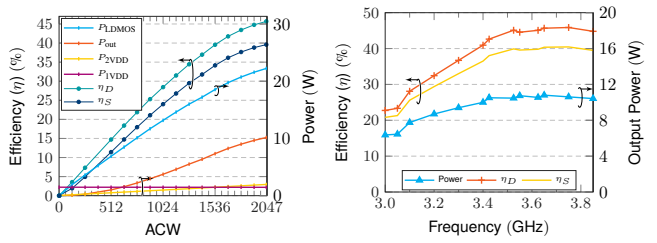

Fig. 6. Pulsed continuous wave measurements with 12.5 % time duty-cycle pulses, showing RF output power, drain and system efficiencies (η_D resp. η_S) for (a) powers and efficiencies vs. ACW at 3.525 GHz; (b) peak output power (triangle) and efficiencies vs. frequency.

class-C [6]), and using the 8-phase operation, a power density of 1.27 W mm^{-1} can ideally be expected, and a phase-averaged theoretical upper limit for the drain efficiency of 85.4 % [7], considering an ideal device with lossless output matching. The input capacitance to be driven is 2.38 pF mm^{-1}, of which 0.77 pF mm^{-1} can be attributed to interconnect parasitics and ESD diodes. When activated at 3.5 GHz, the expected drive power is then 0.142 W mm^{-1}, of which 0.027 W mm^{-1} is intrinsic to the LDMOS C_{GG} and 0.013 W mm^{-1} due to interconnect parasitics and ESD protection; the rest is due to capacitive overhead added by the driver and its tapered buffer chains.

III. Measurements

The DTX measurements are performed by uploading IQ-test data in the on-chip memory and providing the external f_s (data sampling) and f_0 (RF up-conversion) clocks to the DTX.

First, pulsed continuous wave (CW) test signals with a 12.5 % time duty-cycle are uploaded to the SRAMs to avoid excessive self-heating of the DTX at high RF-output power conditions while mimicking a PAPR of 9 dB. The related measured RF-output power, drain, and system efficiencies are given in Fig. 6 for $V_{\mathrm{LDMOS}} = 28$ V. At 3.525 GHz, this DTX sample reaches 45 %/40 % peak-drain/system efficiency, with an output power of 10.5 W, providing close to 1 W mm^{-1}. Fig. 6(a) gives the measured DTX switch-bank efficiencies and (output) powers at 3.525 GHz vs. amplitude code word (ACW), while Fig. 6(b) gives the measured peak-efficiency and peak-RF-output power vs. frequency, showing an −1 dB power RF bandwidth of over 650 MHz, only limited by the output matching network.

Second, to characterize the realized (effective) DTX resolution, a spectrum analyzer in vector signal analyzer (VSA) mode is used, and the DTX is programmed with a slow linear up and down ACW ramp. Due to the limited SRAMs' depth available, first a coarse up-and-down sweep is performed using only the MSB cells. The measured ACW–AM is shown in Fig. 7, where no digital pre-distortion (DPD) has been applied. Next, both MSBs and LSBs are swept over the 0–128 ACW range (see the zoomed graph of Fig. 7), showing the very fine ACW–AM control of the high-resolution DTX.

IV. Conclusion

A high-resolution, high-power switch-bank concept for digital transmitters is presented. It features a digital CMOS controller

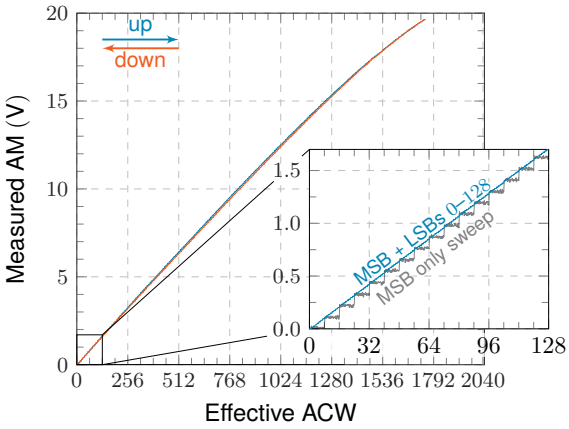

Fig. 7. Measured ACW–AM curve of the high-resolution DTX. In the main graph only the MSB segments are used, while in the zoomed graph both the MSBs and the second layer of 7 thermometer coded LSBs are used.

that is high-density flip-chip mounted on an LDMOS power die. The proposed configuration allows the high-speed control of hundreds of tiny gate segments directly embedded in the drain fingers/runners of an LDMOS power device. The resulting DTX switch-bank configuration combines high resolution with low layout parasitics, enabling RF output powers above 10 W peak with drain/system efficiencies of 45 %/40 %, respectively. In addition, the high-density flip-chip assembly offers improved grounding and supply decoupling for the CMOS gate drivers, facilitating reduced memory effects. The proposed DTX configuration offers an excellent starting point for developing highly integrated, energy-efficient, wideband DTX massive multiple-input and multiple-output (mMIMO) solutions.

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References

[1] S.-W. Yoo *et al.*, "A multimode multi-efficiency-peak digital power amplifier," *IEEE JSSC*, 2020.
[2] H. M. Nguyen *et al.*, "A mm-wave switched-capacitor RFDAC," *IEEE JSSC*, 2022.
[3] M. Beikmirza *et al.*, "A wideband four-way Doherty bits-in RF-out CMOS transmitter," *IEEE JSSC*, 2021.
[4] J. Zanen *et al.*, "A predistortion-less digital transmitter with −50-dB ACLR exploiting output conductance linearization," *IEEE SSC-L*, 2021.
[5] V. Diddi *et al.*, "Broadband digitally-controlled power amplifier based on CMOS / GaN combination," in *IEEE RFIC*, 2016.
[6] D. P. N. Mul *et al.*, "Efficiency and linearity of digital "class-C like" transmitters," in *2020 50th EuMC*, 2021.
[7] D. P. N. Mul *et al.*, "The efficiency and power utilization of current-scaling digital transmitters," *IEEE TMTT*, 2023.
[8] R. J. Bootsman *et al.*, "High-power digital transmitters for wireless infrastructure applications (a feasibility study)," *IEEE TMTT*, 2022.
[9] M. Beikmirza *et al.*, "A wideband energy-efficient multi-mode CMOS digital transmitter," *IEEE JSSC*, 2023.
[10] P. Svihra *et al.*, "Development of novel single-die hybridisation processes for small-pitch pixel detectors," *JINST*, 2023.
[11] L. G. Salem *et al.*, "A recursive switched-capacitor house-of-cards power amplifier," *IEEE JSSC*, 2017.