Device-Aware Test: A Means to Attack Unmodelled Defects (Invited)

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***Abstract*—Structural testing has been very successful in the VLSI manufacturing process to screen out faulty devices and provide high outgoing product quality. However, recent reported data show that existing solutions are not good enough for advanced technology nodes and emerging device technologies. This paper discusses a new manufacturing test approach called Device-Aware Test (DAT), applies it to different flavors of emerging devices, and its potential to be used beyond just manufacturing test.**

***Index Terms*—Device-Aware test, defect modeling, fault modeling, test generation.**

I. INTRODUCTION

Advancements in smaller technology nodes and new devices continuously push researchers to develop improved fault models for better defect coverage in structural testing — a challenge that remains ongoing. E.g., recent data from Google and Meta [1] reveal that faulty chips are bypassing test programs, leading to Silent Data Corruptions (SDC) in the field. At the International Test Conference 2024, Meta reported that approximately 78% of in-field interruptions stem from confirmed hardware failures, such as faulty GPUs and memory. This underscores the urgent need to enhance fault models and test generation for manufacturing test.

Recent studies have highlighted the limitations of commercial testing solutions and explored new approaches for improvement. Real measurement data [2] show a significant decline in defects exhibiting stuck-at fault behavior, yet reliance on this model persists. Additionally, increasing random process variations in advanced low-nanometer nodes introduce timing marginalities that can cause unpredictable failures under adverse conditions [3], yet these are not accounted for in structural test generation. Moreover, the data reported in [4] reveals that the traditional fault modeling approach fails to deal with emerging devices such as STT-MRAMs. In the absence of new fault models and test solutions, chip companies increasingly rely on additional functional and system-level tests to catch escaped faulty chips [5].

This paper discusses a novel test approach, refereed to as *Device-Aware Test (DAT)*, and shows how it can be applied to emerging memories such as STT-MRAMs and FeFETs. It also highlights further directions of the application of DAT for other technologies and its potential to be used beyond just manufacturing test.

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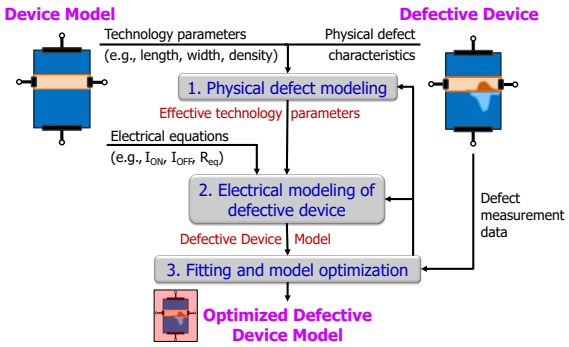

Fig. 1. Device-Aware defect modeling flow.

II. DEVICE-AWARE TEST (DAT)

DAT [6] is a novel test approach comprising three steps: defect modeling, fault modeling, and test generation. A key differentiator of DAT is Device-Aware (DA) fault modeling, which extends beyond Cell-Aware testing [7]. Unlike conventional methods that model defects as linear resistors, DAT incorporates the defect's impact on technology parameters and, consequently, on the electrical parameters. Figure 1 shows the defect modeling process; it takes the electrical model of the good device and the defective device (under investigation) as inputs, to generate an optimized, parameterized defective device model; the process consists of the three steps:

1) Physical defect modeling: The identified physical defect is analyzed to determine the impact on the device's technology parameters. One or more parameters will deviate from their defect-free values, resulting in *effective technology parameters*.
2) Electrical modeling of the defective device: The impact of these updated technology parameters on electrical characteristics is derived, reflecting how the defect alters device electrical behavior. This involves updating defect-free electrical parameters with parameterized effective values, producing a *parameterized defective device model*.
3) Fitting and model optimization: If real measurement data is available, the defective device model is calibrated to generate an optimized, defect-parameterized compact model. Otherwise, the model can still be used in subsequent steps with different parameter values.

Once the defective electrical model is defined, a systematic fault analysis is performed to derive appropriate fault models and subsequently test solutions [8].

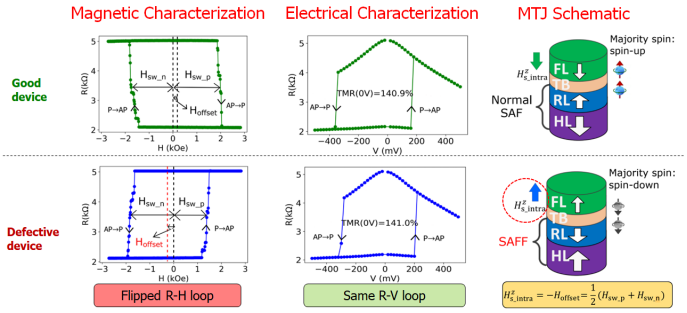

Fig. 2. Normal Device vs Device with SAFF defect.

III. DAT for STT-MRAMs

In this section, we will apply DAT to a unique STT-MRAM defect called *Synthetic Anti-Ferromagnet Flip* (SAFF).

A. Basic STT-MRAM Principles

The *Magnetic Tunnel Junction* (MTJ) forms the basis of STT-MRAMs and can be used to store a single bit into the relative magnetization directions of ferromagnetic layers. Its stack organization fundamentally comprises four layers: Free Layer (FL), tunnel barrier, Reference Layer (RL) and Hard Layer (HL) [9]. The reference and hard layer together form a *Synthetic Anti-Ferromagnet* (SAF) structure [9], which sometimes is also referred to as *pinned Layer (PL)*. Due to a magnetic field created by the PL, a net *intra-cell stray field* $\boldsymbol{H_{\text{s\_intra}}}$ may exist at the FL. Its magnitude depends on the stack design, device size, etc. [10].

Together with an access transistor, an MTJ device can be used as a memory cell. To guarantee successful switching, the magnitude of the write current has to be larger than the MTJ's *critical switching current*. Due to the bias dependence of STT efficiency and stray fields [11], the critical write current can significantly differ for a write 0 and a write 1. Write operations change the magnetization direction of the FL; in case it is parallel (P) to the reference layer the MTJ has a low resistance and in case anti-parallel (AP) the device is in high resistance.

B. Defect Characterization and Modeling

Figure 2 shows the measurement results of a good device and a device that suffers from SAFF. Although their electrical characterization using R-V (resistance-voltage) loops shows similar behavior (minor differences are caused by process variation and intrinsic STT stochatisity), the R-H (resistance-magnetic field strength) hysteresis loops is horizontally flipped for the defective device. This can be attributed to the flip of magnetization in both HL and RL, hence the name *Synthetic Anti-Ferromagnet Flip (SAFF)* defect. As a result of inhomogeneities that occur during the device fabrication process, HL with significantly reduced coercivity may exist in certain outlier devices [12].

Due to the existence of $H^z_{\text{s\_intra}}$ at the FL, the *positive* switching field $H_{\text{sw\_p}}$ and the *negative* switching field $H_{\text{sw\_n}}$ are asymmetric [12]. The defect-free R-H loop has a positive offset. In contrast, the defective device shows a horizontally flipped R-H loop with a negative offset. This indicates that the *polarity* of $H^z_{\text{s\_intra}}$ *reverses* for the defective device while its *coercivity* H_{c} is *not influenced*. In addition, the switching direction also changes. For example, a positive field $H_{\text{sw\_p}}$ induces a P→AP transition for the defective device while it leads to an AP→P transition for the defect-free device.

Although the SAFF defect has no impact on the switching current direction, the polarity of $H^z_{\text{s\_intra}}$ is reversed by the defect. This affects the way the SAFF-defective MTJ manifests itself at the functional level in an STT-MRAM array.

C. Testing SAFF Using the Conventional Approach

Before applying Device-Aware fault modeling, we apply the conventional approach in order to highlight its shortcomings. We model each defect as a linear resistance and we inject them in a victim-cell being in the center of 3x3 cell array netlist. Here we sweep resistive defects in series and parallel to the MTJ of the cell.

Using the conventional approach, we observed two types of faults: incorrect read faults (i.e., applying a read operation results in a wrong value while the cell did not flip) and transition write faults (i.e., applying transition write operation fails); these can be easily detected using the test: {⇕(w0); ⇑(w1, r1); ⇓(w0, r0)} (for march notation see for example [13]). However, applying this test to a device with a SAFF defect will clearly not detect the fault as the R-V loops of the good and the bad devices are almost the same; hence, the defect will escape the test.

In conclusion, applying the traditional approach for testing such a unique fault results in wrong fault models and unnecessary waste of test time.

D. Device-Aware (DA) defect modeling

Using DA defect modeling requires modeling of the impact of SAFF defect on the overall stray field H^z_{stray} (including both intra- and inter-cell stray fields) in the FL of the defective cell within a memory array. Hence, the magnetic coupling of eight neighboring cells have to be taken into consideration. The details of the model are reported in [12].

E. Device-Aware Fault Modeling

We reused the simulation platform for conventional fault modeling to perform DA fault modeling. However, instead of injecting linear resistances, we replaced the defect-free MTJ model in the victim cell with our SAFF model. As the SAFF defect does not affect the magnitude of the magnetizations of the RL and HL (only their directions are flipped), the SAFF defect size or strength plays no role.

The simulation results reveal interesting observations. First, no single-cell faults and no two-cell coupling faults were observed. However, a transition write 0 operation (i.e., 1w0) to the victim-cell was failing in 1150 cycles out of the simulated 10k cycles, when all neighborhood cells were in state '1'. This corresponds to an occurrence rate of 11.5%. Note that the fault is *intermittent* in nature, and is called Passive Neighborhood Pattern Sensitive Fault (PNPSF$_i$). The intermittent behavior

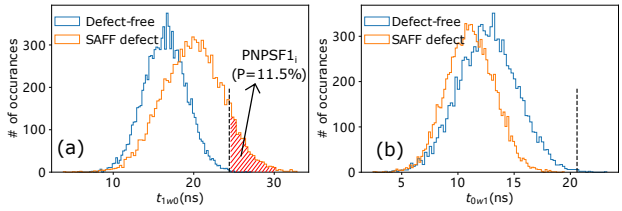

Fig. 3. Impact of SAFF on transition write operations

is shown in Figure 3(a) where the presence of a SAFF defect shifts the write time distribution to the right potentially causing 1w0 failures with a 11.5% probability, assuming a switching time of $25ns$. Figure 3(b) shows the results for 0w1 operations; note that the presence of SAFF in this case accelerates the switching. Compared to conventional fault modeling, DAT sensitizes the right fault primitives, optimizes the test and reduces test escapes.

F. Test Generation

A straightforward test for the (PNPSF$_i$) fault, would be $\{\Updownarrow(\mathrm{w1}); \Updownarrow(\mathrm{w0,r0,w1})^n\}$; n denotes the number of times that the second march element is repeated. The algorithm sensitizes a 1w0 transition while ensuring that all neighbors have a value equal to 1. As there is a write failure probability of 11.5%, this test cannot guarantee a 100% fault coverage. For example, if n=19 the detection probability equals $(1-11.5\%)^n$=70%; we assume that each write operation is independent from the previous one. Clearly, getting high confidence in the detection comes at a large test time.

The second test solution aims at guaranteeing the detection by incorporating *magnetic* write operations in the March test:

$$\{\Updownarrow(\mathrm{w0_H}); \Updownarrow(\mathrm{r0})\}, \text{ or } \{\Updownarrow(\mathrm{w1_H}); \Updownarrow(\mathrm{r1})\}.$$

Here, the element $\mathrm{w0_H}$ ($\mathrm{w1_H}$) indicates a magnetic write '0' ('1') operation; i.e., an *external* field H_{ext} is applied to switch the MTJ state. H_{ext} should be strong enough to flip the FL, but not the PL. This enforces that the defective and defect-free devices have opposite magnetization directions in the PL and same directions in the FL; resulting in different resistances. As an entire STT-MRAM chip or even multiple chips can be reset to a certain state by an external field in one shot, the additional cost to perform this step could be minimized.

IV. DAT for FeFET

FeFETs resemble MOSFETs but replace the high-κ dielectric with a ferroelectric (FE) layer. They typically use a metal-FE–metal-insulator-semiconductor (MFMIS) structure [14]; FE materials exhibit polarization–voltage hysteresis, enabling binary storage: downward polarization lowers the threshold voltage (LVT, '1'), while upward polarization increases it (HVT, '0'). The *Memory Window (MW)*, defined as MW=HVT-LVT, represents the voltage difference at a current level of $10^{-9}A$ [15]. The typical FeFET memory cell configuration used is 1T (FeFET)-1R (Resistor) structure, where the word line (WL) controls the gate of the FeFET, the bitline (BL) and the select line (SL) are set to voltages suitable for write and read operations. The 1T-1R NOR memory architecture

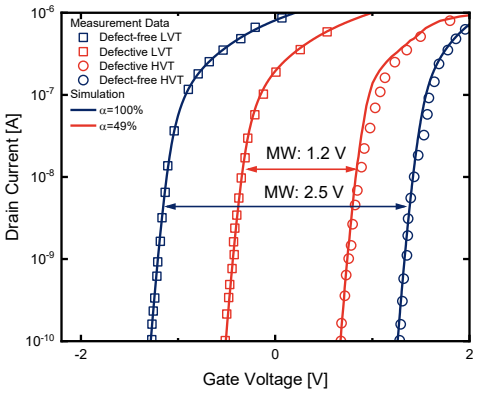

Fig. 4. Defective and device-free devices fitting in the logarithmic y-axis.

is commonly used; cells within the same row share common WL and SL connections, while those within the same column share the same BL connections. In the rest of this section, we will illustrate the application of DAT on Stuck-at-Polarization (SAP) defects in FeFETs.

A. Defect Characterization and Modeling

Figure 4 shows the measurement results, in the form of $I_D - V_G$ (dain current- Gate voltage) curves, of a good device and a bad device. These devices were manufactured at at EMECA [16] using Metal/-Insulator-Semiconductor structure; the effective channel width is $4\mu m$ and the length $15\mu m$. The figure clearly shows a significant decrease in the MW, signaling a defect referred to as *Stuck-At-Polarization (SAP)* .

The SAP defect can be integrated into the defect-free model by calculating the key parameter *FE polarization* P_{FE} [17], while the relationship between I_d and V_g follows the conventional MOSFET model [18].

$$\begin{aligned} P_{\mathrm{FE}} &= P_S \cdot \tanh\big(V_{\mathrm{FE}} - \mathrm{dir} \cdot E_C \cdot t_{\mathrm{FE}}\big) \\ V_g &= V_{FE} + V_{MOS} \end{aligned} \tag{1}$$

P_{FE}	FE polarization	P_S	FE layer maximum polarization
V_{FE}	Voltage across the FE layer	dir	Polarization direction
E_C	Coercive field	t_{FE}	FE layer thickness
V_g	Gate voltage	V_{MOS}	Voltage across MOS structure

To generate a model for a defective device suffering from SAP, we assume that the FE consists of different domains; each domain may or may not switch. SAP has two versions: a) SAP^+ where some domains are trapped in a fixed downward polarization, and b) SAP^-, where some domains are trapped in a fixed upward polarization. The polarization of e.g., SAP^+ can be given by:

$$\begin{aligned} P_{\mathrm{FE}}(\mathrm{SAP}^+) = P_S \cdot \Big(&\tanh\Big(V_{\mathrm{FE}} - \mathrm{dir} \cdot \alpha \cdot E_C \cdot t_{\mathrm{FE}}\Big) \\ &\pm \tanh\Big((1-\alpha) E_C \cdot t_{\mathrm{FE}}\Big)\Big) \end{aligned} \tag{2}$$

Here, α refers to the defect strength, representing the percentage of domains capable of free conversion; α=100% indicates defect-free devices. As α decreases, fixed domains begin to appear and gradually increase in number. The impacted physical parameter (P_{FE}) is integrated into the compact Preisach model described in Verilog-A and integrated into the

FeFET compact model [17]. We calibrated the model using measurement data [16]. Figure 4 shows how our $I_D{-}V_G$ simulated curves fit perfectly with measured data; the model allows for seamless integration into SPICE simulators.

B. Fault modeling

The simulation platform consists of 3x3 FeFET NOR memory. Cadence Spectre is employed for circuit-level simulations, where SAP defects injection is carried out by replacing the defect-free Preisach models with the generated defective device model. We define the cell state 0 as the state where $I_D{=}I_{on}{>}10^{-7}A$, and the cell state 1 as the state where $I_D{=}I_{off}\ {<}10^{-9}A$, meaning that $I_{on}/I_{off}{>}100$ (see Figure 4). If the current value lies between the two, then the cell is in an incorrect, undefined state U which may lead to functional errors during reading. Moreover, 1V is chosen as the read voltage, which is a reasonable and conservative value.

Table I shows the results of defect injection and circuit simulation for different defect strengths presented by α. The impact on the MW is also included. The senistized faults are described using the fault primitive notation: $<S/F/R>$. S describes the sensitizing sequence $\in \{0w0, 0w1, 1w1, 1w0, 0r0, 1r1\}$; e.g., 0w1 describes a write 1 operation to a cell containing an initial value 0. F describes the fault effect $F \in \{0, 1, U\}$; e.g., U means that the cell will switch to an undefined state after S. R describes the readout value $r \in \{0, 1, -\}$; '-' is used for R when S is a write operation.

The sensitized faults are classified as *Easy-to-detect (EtD)* or *Hard-to-detect (HtD)* faults. A fault is considered EtD when its detection is guaranteed by regular read/write operations; otherwise, it is a HtD fault.

TABLE I
FAULT MODELING RESULTS FOR SAP

α %	MW [V]	Sensitized faults	Type
[70, 100]	1.76-2.53	fault free	
[59, 70]	1.43-1.76	$\langle$0r0/U/0$\rangle$, $\langle$0w0/U/$-\rangle$, $\langle$1w0/U/$-\rangle$	HtD
[44, 59]	0.98-1.43	$\langle$0r0/U/1$\rangle$	EtD
		$\langle$0w0/U/$-\rangle$, $\langle$1w0/U/$-\rangle$	HtD
[0,44]	0-0.98	$\langle$0w0/1/$-\rangle$, $\langle$1w0/1/$-\rangle$, $\langle$0r0/1/1$\rangle$	EtD

C. Test development

Detecting EtD faults can be guaranteed with a simple March test such as: $\{\Updownarrow(\mathrm{w1}); \Updownarrow(\mathrm{w0, r0})\}$. Although such march test may detect some HtD faults, it can never guarantees their detections as these may result in random read values due to the U state of the faulty cell. Guaranteeing the detection of such faults requires a dedicated Design-for-Testability (DfT) scheme. One option for DfT is to change the design of the sense-amplifier such that it can differentiate the three states 1, U and 0 instead of solely distinguishing the regular 0 and 1. This can be done by providing different reference currents to the sense amplifier by for example using a trimming circuit [19].

V. CONCLUSION AND FUTURE DIRECTIONS

DAT can clearly contribute to close the gap between the fault models (abstraction) and the real manufacturing defects; hence, improving the test generation process while optimizing the test time and improving the outgoing product quality. In addition, DAT can significantly fasten yield learning. As defects have their own compact models and unique signatures, it becomes easier to distinguish between defects and improve diagnosis.

Although DAT is currently demonstrated only on some emerging devices such as STT-MRAM, RRAM and FeFET, it can address any device technology including advanced technology nodes and new emerging devices. For example, manufacturing defects in CMOS based logic designs, including defects in transistors (such a pinholes in the gate) can be analyzed using the DAT approach in order to understand and minimize the deviations between used fault models/approaches (stuck-at-fault, cell-aware test, delay test) and actual defect behavior; this is crucial for enhancing test quality in the context of advanced technology nodes.

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