Prognostics and thermal management of power electronic packages

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PROGNOSTICS AND THERMAL MANAGEMENT OF POWER ELECTRONIC PACKAGES

PROGNOSTICS AND THERMAL MANAGEMENT OF POWER ELECTRONIC PACKAGES

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen Maandag 24 maart 2025 om 12.30 uur.

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In
Memory
of my
baby girl
Simone Martin

CONTENTS

Nothing in life is to be feared; it is only to be understood.
Now is the time to understand more so that we may fear less.

- Marie Curie

PREFACE

BACKGROUND AND MOTIVATION

The evolution of energy conversion from complex mechanical machines like synchronous and rotary converters in the early 1900s to the invention of solid-state semiconductor devices in the 1950s has led to the modern era of power electronics. Power semiconductor devices that are responsible for efficient energy conversion or rectification play a vital role in renewable energy technology, automotive electric vehicles, smart grids, telecommunications, and high-power industrial applications. As the global demand for green energy and sustainability increases, the importance of power electronic components remains paramount.

In recent years, the drive towards miniaturization and higher power density intensified, causing electrical overstress, especially due to the adoption of Wide-Band Gap semiconductors, such as Silicon Carbide (SiC) and Gallium Nitride (GaN). In addition, the packaging materials for power devices undergo challenging conditions through harsh environments and extreme temperature swings. Compounding electrical, thermal, and mechanical stresses raises concerns over power devices' meeting reliability requirements, particularly for applications where failures can have severe consequences.

Advanced materials and innovative technologies have emerged to address the reliability concerns. For instance, the regulations on lead (Pb) solders and the need for high-temperature die-attach material created an opportunity for silver sintering to be adopted in power electronics packaging. However, their usage is still limited due to the process-dependent properties of silver sinter materials. Likewise, conventional methods of addressing reliability challenges depended on destructive testing and post-mortem analysis. Despite their effectiveness in identifying the failure mechanism, the need to detect early signs of failure created a demand for prognostic monitoring approaches. Besides, power electronic devices predominantly suffer from thermal breakdowns. Hence, advanced thermal management strategies are required for next-generation applications.

Considering longevity and efficient heat dissipation as ongoing challenges, this dissertation is motivated to develop novel methodologies for Prognostics and Thermal Management of Power Electronic Packages. The findings presented herein are relevant for industries as they strive to extend the boundaries of power density and miniaturization.

RESEARCH OBJECTIVES AND CHALLENGES

The reliability of power electronic packages is often compromised by degradation mechanisms such as thermal fatigue and delamination, leading to economic consequences due to premature failures. Conventional approaches for reliability testing are inadequate for

early fault detection. On the other hand, the emergence of complex materials, such as silver sintering, and the increasing demand for power density exacerbate the thermal and thermo-mechanical challenges. This research aims to address these challenges based on the following approaches:

- Develop a prognostic framework based on condition monitoring methods, focusing on early detection of performance degradation indicators.
- Establish a thermal characterization methodology for thin-bond line interfaces with complex materials like silver sintering to better understand their thermal behavior and associated degradation mechanisms under operating conditions.
- Investigate integrated thermal management approaches to mitigate thermal stresses and enhance power electronic packages' overall reliability and performance.

To realize the goals mentioned above, several scientific challenges need to be addressed, which are summarised as follows:

- Developing a methodology to detect early signs of failure must also remain non-intrusive during the operation of power electronic devices.
- Characterizing the thermal properties of interfaces with complex die-attach materials must also consider the correct form factor representing the die attachment in packaging applications.
- Integrating advanced thermal management strategies into existing packaging technologies must also maintain compatibility with industry standards and production processes.

NOVELTY AND CONTRIBUTIONS

This research aims to offer the following key novelties and contributions in reliability engineering, material science, and heat transfer.

- For non-intrusive early detection of faults and performance degradation, a novel condition monitoring methodology based on a transient pulse is developed to determine the time-transient temperature-dependent thermal impedance '$Z_{th}(t,T_{amb})$' of the package. Monitoring this parameter contributes to understanding the reliability of the package's thermal performance.
- The effective interface thermal conductivity of complex silver sintering material is evaluated in the right form factor as die-attachment through a novel thermal characterization methodology that determines '$\Delta Z_{th}(t,\Delta x)$'. Monitoring this parameter contributes to understanding the interface material's thermal properties.
- A novel co-packaging approach of integrating electronics with microfluidics is developed through classical back-end package assembly processes. The methodology contributes to improved device power rating and reduced package thermal resistance.

DISSERTATION OUTLINE

This dissertation encompasses seven chapters that are structured as follows:

- Chapter 1 provides an outlook on power electronics reliability and reliability monitoring methods. It discusses the dominant chip-related and package-related degradation mechanisms, with a detailed review of measurement methods for aiding reliability monitoring.
- Chapter 2 introduces a novel online condition monitoring methodology using a thermal test chip to detect package thermal performance degradation. The chapter details the package assembly processes, measurement parameters, experimental findings, and failure analysis to support the findings.
- Chapter 3 focuses on prognostic monitoring of PQFN packages with distinct silver sintered materials that vary in material compositions and sintering processes. A functional power MOSFET was utilized in this study to understand the performance degradation of the silver sintering materials on an industry-representative Power QFN package.
- Chapter 4 evaluates the lifetime reliability of hybrid silver sinter materials with stress-absorbing additives designed for high-reliability applications in power electronics.
- Chapter 5 introduces a novel thermal characterization methodology suitable for thin bond-line interfaces with high-conductive materials. In this chapter, three different materials (silver sintering, SAC305, and non-conductive epoxy) were tested to demonstrate the methodology's effectiveness. The results are evaluated against the literature, and the methodology is compared against conventional methods.
- Chapter 6 explores a heterogeneous method of integrating diamond heat spreaders onto thin semiconductor substrates to reduce concentrated thermal hot spots and maintain a uniform temperature gradient.
- Chapter 7 introduces a novel co-packaging approach by integrating electronics with microfluidics. The effectiveness of the package was demonstrated in this chapter, and significant improvements were made to the device power rating.

1

AN OUTLOOK ON POWER ELECTRONICS RELIABILITY AND RELIABILITY MONITORING

Increasing awareness of environmental concerns and sustainability underlines the importance of energy-efficient systems, renewable energy technologies, electric vehicles, and smart grids. Hence, stringent constraints and safety regulations have been prompted to meet reliability standards in power electronics. This chapter provides an outlook on the current state of power semiconductor devices, field-critical applications, dominant degradation mechanism (chip-related and package-related), and the emerging measurement techniques for condition monitoring. This chapter delves into the underlying physics behind each reliability measurement method reviewed. A comparative summary of cost, complexity, online monitoring capability, accuracy, and intrusiveness is provided to enable readers to make informed decisions about the measurement methods. This chapter emphasizes the significance of early fault detection through online monitoring, as it can effectively reduce system downtime for seamless, non-interruptive operation.

This chapter has been published in Recent Advances in Microelectronics Reliability. Springer, Cham. (2024).

1

1.1. INTRODUCTION

RELIABILITY is an essential performance metric in power electronics for developing high-efficiency and high-power-density devices. In today's rapidly evolving technological landscape, meeting reliability requirements presents several challenges. These include catering to field critical applications, enduring harsh environmental conditions, adhering to rigorous testing and safety regulations, accommodating the need for higher power density, complex integration, uncertainties related to new materials, and resource constraints [1]. Besides, reliability qualification has undergone a transformative shift. The evolution of reliability qualification is distinct into four stages, as illustrated in Figure 1.1 [2–5].

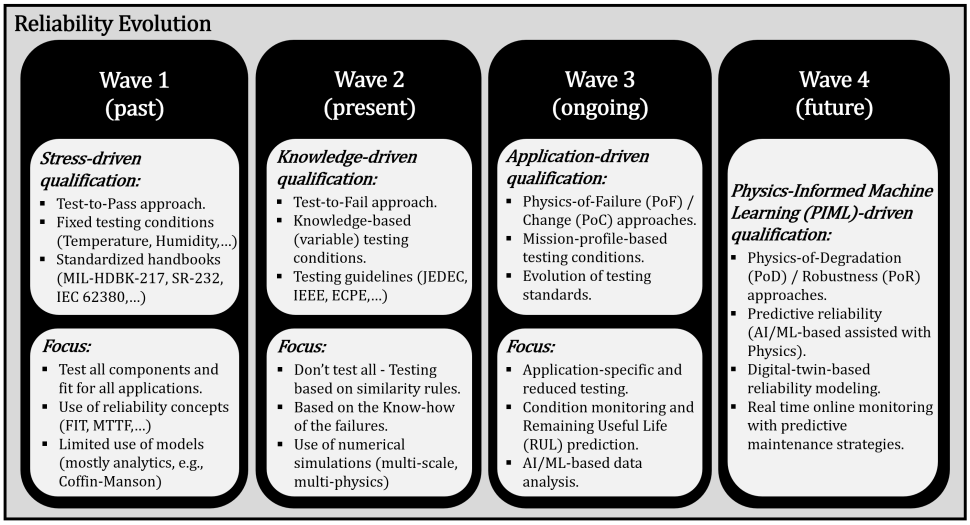


Figure 1.1: The evolution of reliability summarized as Wave 1 (Past), Wave 2 (Present), Wave 3 (Ongoing), and Wave 4 (Future). Each stage highlights the driving aspect of reliability research and its vital focus elements. [*Adapted from iREL4.0 newsletter (with permission)*]

In the past, micro and power electronic devices underwent various stress tests (temperature cycling, thermal shock, humidity testing, electrical overstress, and vibration testing), irrespective of their application. The component failure rates were further documented in empirical military handbooks MIL-HDBK-217, technical handbook SR-232 from Telcordia, technical report IEC 62380, and Siemens SN29500 standards. This approach was primarily reactive, focusing on identifying and resolving issues after they occurred. A proactive knowledge-driven approach later emerged, emphasizing reliability physics and understanding failure mechanisms. Esteemed bodies like JEDEC, IEEE, and ECPE have instituted predefined testing standards and guidelines for electronic components. These span across integrated circuits, discrete semiconductors, electronic modules, and passive components, categorized based on their designated applications.

A noticeable trend has recently emerged, focusing attention on application-driven qualifications. This approach emphasizes mission-profile-based testing, active condition

monitoring, and an intricate grasp of two complementary approaches in reliability engineering: the Physics of Failure (PoF) and the Physics of Change (PoC). The PoF approach analyzes root-cause failure mechanisms, considering materials, defects, and stresses, while the PoC approach seeks to understand physical alterations resulting from failure. In the evolving landscape of reliability qualification, traditional metrics like Failure in Time (FIT) and Mean Time To Failure (MTTF) are being superseded by Remaining Useful Life (RUL) prediction with a shift in focus from understanding failure mechanisms to degradation mechanisms and device robustness [6, 7]. Physics-informed computational techniques, including Machine Learning (ML) and Artificial Intelligence (AI), are expected to play a crucial role in early fault prediction and performance decline. Reliability modeling based on digital twins is anticipated to be pivotal for high-value applications. These coordinated approaches are essential in developing reliable power semiconductor devices, ensuring seamless operation, and promoting a sustainable environment.

To support the ongoing reliability evolution, several measurement strategies have been devised to streamline the process of reliability monitoring. Monitoring reliability requires assessing the device's condition continuously throughout its lifetime. Three fundamental conceptions of implementing condition monitoring are elucidated below: [8, 9].

1. Measuring the device's intrinsic parameters as an indication of the device performance degradation.
2. Add-on (or) embedded sensors to measure the device's robustness against performance degradation.
3. Reliability modeling approach to compare the device's performance against a computational model.

Reliability modeling at the component level, system level, and software reliability has the highest percentage of research publications [10]. Therefore, reliability modeling is excluded from the scope of this chapter. Recent publications on lifetime modeling are presented in [11, 12]. The primary objective of this chapter is to present a comprehensive overview of various relevant measurement techniques, particularly thermal measurements, commonly used in industry and academia that can support reliability monitoring (both online and offline). An ideal strategy for device performance monitoring would avoid additional sensors to measure temperature, humidity, and mechanical stresses. An increment in those stressors might not directly relate to the device's electrical performance characteristics. Besides, additional sensors might introduce additional failure modes. Hence, measuring the device's intrinsic electrical performance parameters is preferable. However, the limitation in understanding the relationship between various stressors and device performance degradation necessitates embedded sensors for reliability monitoring.

This chapter discusses the current state of power electronics reliability and several noteworthy reliability measurement methodologies. The following section explores the power electronics market and survey reports from the literature on power device failure rates. Subsequent section focuses on selected chip-level and package-level degradation

mechanisms. A detailed review of various reliability measurement methodologies are further provided. A summary of the discussed methods are finally discussed with highlights on their advantages and disadvantages. The chapter concludes with an emphasis on the need for online reliability monitoring for a sustainable future.

1.2. Power Electronics Market and Failure Statistics

Concerns about device efficiency and reliability surfaced due to the increasing demand for high power. The recent transition towards Wide-Band Gap (WBG) semiconductors further amplified reliability concerns. While silicon has traditionally been the preferred material for semiconductors, its energy gap decreases from ~1.12eV at room temperature (25^oC) to around ~1eV at 300^oC, resulting in reduced power transistor efficiency at high operating temperatures [13, 14]. Consequently, semiconductor materials with band-gap energy exceeding 2eV at 25^oC have gained significant interest, enabling the development of power transistors with higher breakdown voltage and higher operating temperature, thereby generating market demand. The increasing demand is reflected in the current market projections. As of 2021, the global power electronics industry was valued at around ~$17B, with a Compound Annual Growth Rate (CAGR) of 6.9% by 2026 [15]. This growth is primarily driven by three segments: **(1.)** Consumer electronics, **(2.)** Automotive Electric Vehicle (EV) systems, and **(3.)** Industrial applications.

1. Silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have traditionally dominated consumer applications. However, Gallium Nitride (GaN) technology has recently replaced Silicon in fast-charging consumer electronics.
2. The automotive inverter technology market has conventionally relied on Integrated Gate Bipolar Transistor (IGBT) modules based on Silicon. The adoption of SiC technology in automotive inverters has experienced significant growth since Tesla implemented Silicon Carbide (SiC) MOSFETs. In 2020, BYD Semiconductors and LUCID Motors adopted SiC MOSFETs in their automotive inverters [16].
3. Silicon IGBT modules dominate high-power industrial applications, including PhotoVoltaic (PV), Wind energy, and Battery Energy Storage Systems (BESS). SiC IGBTs demonstrate higher efficiency than Si IGBTS for controllers used in Aircraft Ground Power Units (AGPU) [17].

A survey conducted on the reliability of power converters across various applications revealed that power semiconductor devices are particularly susceptible to failures [18]. Figure 1.2 illustrates the failure rates of power semiconductor devices in four highly demanding industrial applications. In wind energy systems, a survey conducted over a span of 15 years on 1500 wind turbines indicated that approximately 23% of the reported malfunctions (34,582) were attributed to electrical system failures, with wind energy power converters exhibiting the highest failure rate distribution [19] (Figure 1.2a). Similarly, in utility-scale-grid-connected PhotoVoltaic (PV) systems, a survey revealed that 37% of unscheduled maintenance events between 2001 and 2006 accounted for 59% of the overall maintenance cost. Among these events (Figure 1.2b), power inverters were responsible for the majority of repairs [20, 21]. Power semiconductor devices are vital in Electric Railway Traction Chain (ERTC) systems. A survey conducted from 2009 to 2013 reported

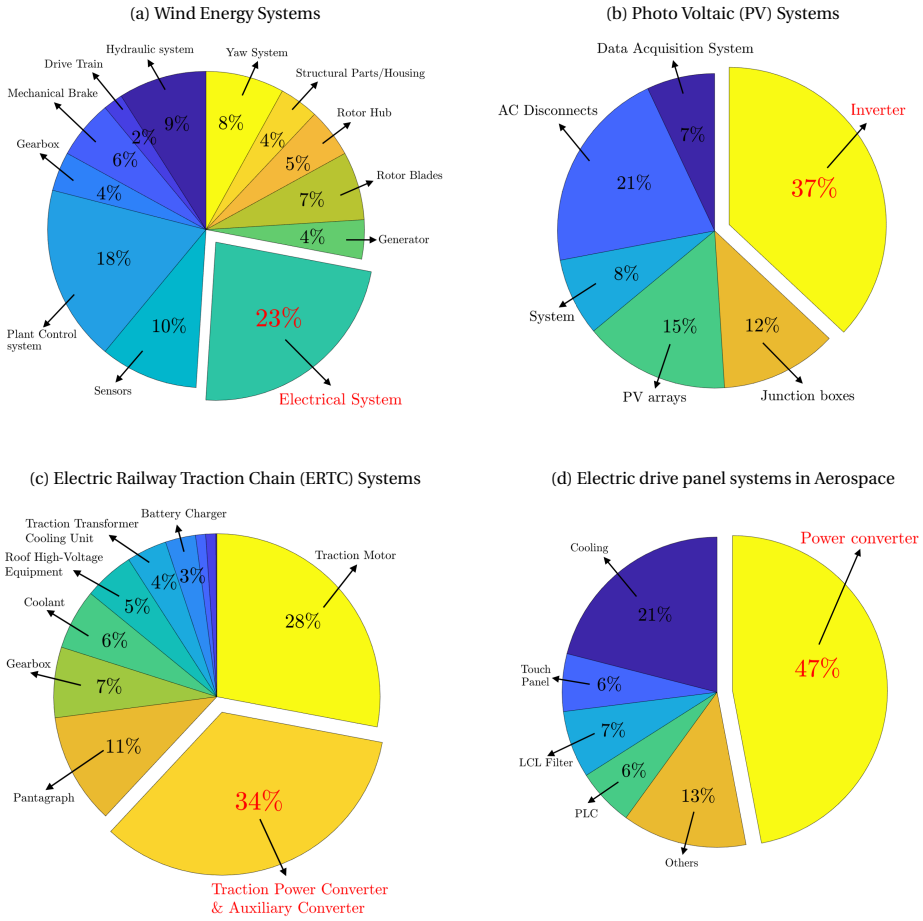


Figure 1.2: The percentage failure rate of power devices against other components was compiled based on the survey reports in high-power demanding industrial applications. **(a)** In wind energy systems, power converters have the highest distribution of the failure rate [19]. **(b)** The power inverter malfunction in PV systems accounted for 37% unscheduled maintenance [20, 21]. **(c)** 34% of the total failures in electric train traction systems were due to the traction power converter [22]. **(d)** The power converter failure rate in aircraft electric-drive systems was reported to be 47% of the total system failure [23]. [*Adapted from the literatures that are cited.*]

that the traction power converter contributed to 34% of the total failures in the traction drive systems [22] (Figure 1.2c). Furthermore, as the aerospace industry moves towards electrified aircraft, the demand for high-power converters in hybrid electric propulsion systems is increasing. A survey on the failure rate of electric-drive panel systems revealed that power converters accounted for 47% of the total system failures [23] (Figure 1.2d).

The survey findings reported in the literature provide compelling evidence that despite the extensive history of power electronics, its reliability remains a significant concern, particularly due to its impact on real-life applications resulting in increased downtime and costs. While power electronics play a crucial role in automotive applications, comprehen-

sive statistical data on the failure rate of power devices in Electric Vehicles (EVs) is rarely available to the public. However, it is worth noting that power MOSFETs used for battery connect/disconnect switches in automobiles exhibit a failure rate of a few per million. [24]. The failure statistics depicted in Figure 1.2 have significant implications attributed to factors such as electrical overstress and environmental conditions like temperature and humidity. Consequently, exploring and understanding the key chip-related and package-related degradation mechanisms that contribute to these failures is imperative.

1.3. Power Electronics Degradation Mechanisms

Material degradation is an inevitable natural phenomenon that significantly affects power electronics device reliability, performance, and lifespan. Power devices experience degradation caused by multiple factors, including operating temperature, power input, switching stresses (electrical transients), humidity, mechanical stresses, and aging. Figure 1.3 illustrates a schematic of a typical power module and provides a classification of chip-related and package-related degradation, which will be discussed further in detail.

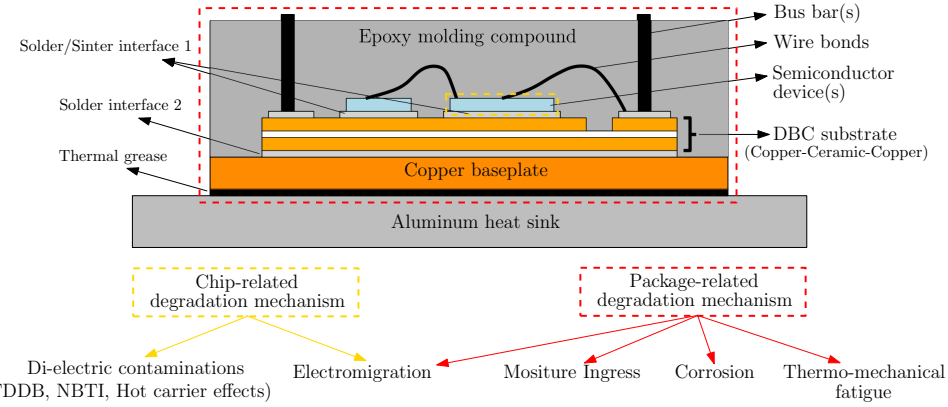


Figure 1.3: A schematic of a typical power module is shown with layer stacks of different materials enclosed in a plastic housing. Some dominant degradation mechanisms in power electronics are classified into chip-related and package-related. The Time Dependent Dielectric Breakdown (TDDB), Negative Bias Temperature Instability (NBTI), and Hot carrier injections are categorized as Di-electric contamination. Though the mechanisms are differentiated as chip and package-related, they overlap in reality.

1.3.1. Chip-Related Degradation Mechanisms

Chip-related degradations primarily involve intrinsic mechanisms, where the device's internal operation deteriorates, primarily as a result of electrical overstress and temperature. Among these mechanisms, two dominant wear-out mechanisms at the chip level are electromigration and dielectric contamination. Electromigration on the chip level refers to the movement of ions in the circuit interconnects, leading to their degradation over time. On the other hand, dielectric contamination involves the entrapment of ions in the dielectric material. Both of these mechanisms contribute to degraded performance and eventual failure of the chip. The impact of temperature on the electromigration process and gate-oxide contamination accelerates the rate of deterioration. Higher temperatures

exacerbate these wear-out mechanisms, intensifying the degradation of the chip and shortening its overall lifespan.

ELECTROMIGRATION

Metal interconnects on semiconductors are susceptible to electromigration at high current densities (10^5 A/cm^2) [25]. Electromigration is a material transport phenomenon that occurs when electrons flowing through the conductors transfer their momentum. This leads to either the depletion or accumulation of material, resulting in open-circuit or short-circuit conditions, respectively [26, 27]. The process of ions electro-migrating is thermally activated, which is shown in Black's equation for electromigration (Eq.1.1). The MTTF_{EM} is inversely proportional to the current density j, the effective length L_{eff} over which the current density is applied, and an Arrhenius behavior of thermal activation. Here E_a represents the activation energy for migration, T is the temperature in Kelvin and k is the Boltzmann constant. The constant n in the equation is specific to the material and influences the overall behavior of the electromigration process [27–29]

$$\text{MTTF}_{\text{EM}} \propto \frac{1}{j^n \times L_{eff}} \exp\left(\frac{E_a}{k\boldsymbol{T}}\right) \tag{1.1}$$

The degradation caused by electromigration experiences exponential growth with increasing temperature. It is also possible for electromigration to occur at the package level, affecting components such as wire bonds and interconnects. Apart from temperature, the presence of intermetallic compounds significantly influences the rate of electromigration. Intermetallics such as Copper-tin (Cu-Sn), Silver-copper (Ag-Cu), Nickel-tin (Ni-Sn), or Gold-aluminum (Au-Al) at interface joints or wire bonds can accelerate the migration rate.

DIELECTRIC CONTAMINATION

In Metal Oxide Semiconductor (MOS) devices, the dielectric serves as an insulating oxide layer between the gate and the conductive channel. Contamination of the dielectric, i.e., ions getting entrapped, can lead to transistor performance degradation. Applying a sufficiently high electric field across the dielectric layer can cause Dielectric Breakdown, which is a Time-Dependent (TDDB) failure. This failure occurs due to processes such as electron tunneling or ion entrapment in the oxide layer over time [27, 29–32]. The lifetime of the dielectric is influenced by several factors, including the quality and thickness of the oxide layer, the applied electric field, and the operating temperature of the device. However, conflicting experimental observations have been reported, particularly for ultra-thin dielectrics, leading to controversies in the equations that define TDDB [31–33]. Based on experiments conducted in reference [33], an empirical model for Mean Time To Failure (MTTF) due to TDDB has been derived from [27, 29]. In Eq.1.2, t_{ox} represents the gate oxide thickness, A_{ox} denotes the oxide area over which a voltage V is applied, and T is the temperature in Kelvin. The parameters a, b, X, Y, and Z are fitting parameters used in the model.

$$\text{MTTF}_{\text{TDDB}} \propto 10^{t_{ox}} \times \frac{A_{ox}}{V^{(a-b\boldsymbol{T})}} \times \exp\left(\frac{X + Y\boldsymbol{T}^{-1} + Z\boldsymbol{T}}{k\boldsymbol{T}}\right) \tag{1.2}$$

Contamination of the dielectric can also occur through other means. At extremely high operating temperatures (beyond the lattice temperature), some ionic charge carriers flowing through the conductive channel are entrapped (diffused) in the gate oxide layer. This phenomenon is referred to as ionic contamination or hot carrier injection [8, 30]. Like TDDB, another effect of dielectric contamination is the Negative Bias Temperature Instability (NBTI), a commonly observed phenomenon in PMOS devices. It arises due to the presence of gate-oxide interface traps (positive charges) that neutralize the negative gate voltages [30]. NBTI happens also in NMOS devices operated under negative bias.

The chip-level degradation mechanisms mentioned above primarily result in reduced efficiency and electrical performance, which can be observed by a shift in the device threshold voltage and higher leakage currents. These mechanisms do not immediately impact transistor operation but instead, cause cumulative damage over time. However, the degradation process can be accelerated under extremely harsh environmental conditions. For instance, the power semiconductor devices used in avionics and space applications have reported single-event burnout failure. This occurs due to the transfer of kinetic energy from charged particles in the Earth's magnetic field and exposure to cosmic radiations like high-energy neutrons. [8, 34, 35].

1.3.2. Package-Related Degradation Mechanisms

Chip-related degradation mechanisms are primarily driven by intrinsic stresses, whereas electronic packages are susceptible to both intrinsic and extrinsic environmental conditions. At the package level, dominant wear-out mechanisms include moisture ingress, corrosion, and thermo-mechanical fatigue. Similar to chip-related degradation, the operating temperature has a significant influence on the rate of deterioration in package-related mechanisms.

Moisture Ingress

Epoxy-based Molding Compound (EMC) is a commonly used encapsulant for electronic devices, providing protection against temperature, humidity, and dust. However, being hygroscopic, EMC is susceptible to oxidation when exposed to high temperatures and highly humid conditions. In [36], the moisture diffusion characteristics of an epoxy-based molding compound (90.6wt% silica filler and 2.04g/cm^3 density) were analyzed using a dynamic sorption analyzer at temperatures 20^{o}C – 85^{o}C with 0 – 85% relative humidity. Moisture ingress, in turn, leads to device degradation through electrochemical migration and corrosion. A review on moisture ingress in photovoltaic modules has reported that the moisture content in the thermoplastic polymer encapsulant led to corrosion on the metal grids [37]. The aging process of the epoxy compound due to moisture ingress is accelerated at higher temperatures due to increased moisture absorption and diffusion within the EMC material. An experimental study [38, 39] demonstrated that pristine EMC undergoes rapid oxidation within 24 hours when exposed to elevated temperatures. The oxidation significantly alters the mechanical properties of the molding compound, including changes in the elastic modulus, thermal expansion coefficient, and glass transition temperature. The Mean Time To Failure (MTTF) due to moisture ingress follows an inverse relationship with Relative Humidity (RH) and exhibits an Arrhenius behavior

characterized by an exponential decay (Eq.1.3). The constant n in the equation depends on the specific epoxy compound being used.

$$\text{MTTF}_{\text{MI}} \propto \frac{1}{RH^n} \exp\left(\frac{E_a}{k\boldsymbol{T}}\right) \tag{1.3}$$

The oxidation of the molding compound further impacts the reliability of the package solder joints. The correlation between the oxidation of the molding compound and solder-joint thermal fatigue was investigated in [40]. It provides insights into the effects of oxidation on the lifetime and durability of solder joints.

CORROSION

Corrosion is a well-studied phenomenon, but its significance in electronics packaging requires further attention. An overview of failure mechanisms associated with corrosion in Control Electronics (ECU), Sensor Electronics, and Power Electronics is provided in [41]. Water treeing is a corrosion mechanism that degrades the packaging molding compound in high-power electronic devices operating in the kV range. High voltages generate electric fields that ionize the moisture content in the molding compound, resulting in the formation of microchannels. Based on an electrochemical corrosion process called Anodic Migration, dendrite structures start growing within the microchannels. An experimental study was conducted in [41] to analyze the dendrite structures due to Anodic Migration Phenomenon (AMP) in polymer compounds, and temperature plays a significant role. The mobility of metal ions increases with temperature, thereby accelerating the rate of dendrite growth through the polymer to form conductive paths.

In recent times, considerable research efforts have been focused on investigating inorganic encapsulation materials with high thermal conductivity as potential replacements for epoxy molding compounds in high-power devices [42]. In power electronics, cement-based encapsulants were proposed in [43] for their potential usage. However, corrosion remains a primary concern when utilizing cement-based materials. The Mean Time To Failure (MTTF) due to corrosion can be described by an inverse relationship with relative humidity and applied electric field ($E = V/d$) and an exponential relationship with temperature, as expressed in Eq.1.4. It is worth noting that other forms of material migration, including anodic corrosion, cathodic corrosion, and purple plagues, may also occur in packaging materials.

$$\text{MTTF}_{\text{AMP}} \propto \left(\frac{1}{RH^n} + \frac{d^m}{V}\right) \exp\left(\frac{E_a}{k\boldsymbol{T}}\right) \tag{1.4}$$

THERMOMECHANICAL FATIGUE

Thermo-mechanical fatigue (TMF) occurs due to repeated cyclic loading caused by temperature fluctuations, temperature gradients within the device, and mechanical stressors like vibrations or shocks. A power module consists of layer stacks of materials with distinct properties housed within a plastic enclosure. The thermal expansion coefficient (CTE) of pure copper (~16.5 ppm/^{o}C) is roughly four to five times higher than that of Silicon (~3 ppm/^{o}C) or SiC (~4 ppm/^{o}C). This discrepancy induces thermo-mechanical stresses

at the interface, as depicted in Figure 1.4. Therefore, selecting the interconnect material between the semiconductor die and the copper substrate plays a crucial role.

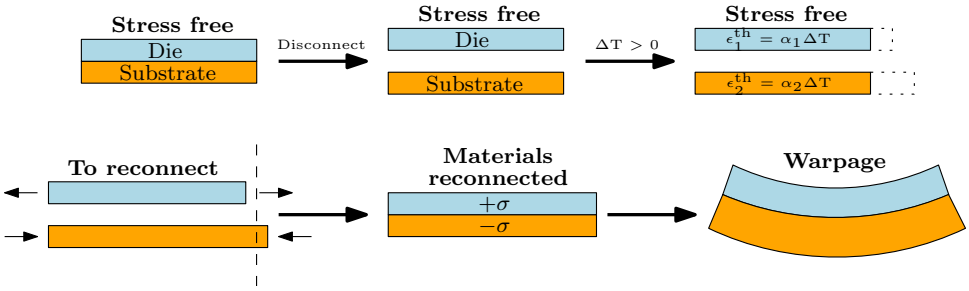


Figure 1.4: A schematic illustration of thermo-mechanical stresses induced due to thermal expansion coefficient α mismatch. In a stress-free situation, the strain ϵ will result in independent expansion when $\Delta T > 0$. However, if the dissimilar materials remain connected, the thermo-mechanical stresses σ will lead to material warpage.

Thermo-mechanical fatigue occurring at the interface material is a cumulative damage process. The impact of thermo-mechanical fatigue conditions on automotive power modules has been extensively investigated in [44]. One resulting behavior of repeated thermo-mechanical loading conditions is stress migration. Stress migration refers to material migration due to thermo-mechanical stresses. Interestingly, the phenomenon of stress migration in silver is also utilized as a die-attachment bonding process [45, 46]. An empirical relationship is provided in Eq.1.5 correlating the number of cycles to failure, the temperature swing (ΔT), and the maximum temperature (T_{max}) [47, 48].

$$\mathrm{MTTF_{TMF}} \propto \Delta \boldsymbol{T}^{n} \exp\left(\frac{E_a}{k\boldsymbol{T}_{max}}\right) \tag{1.5}$$

The T_{max} is an arbitrary temperature established from the empirical model, suggesting that the material lifetime will be longer if stayed below the maximum temperature. The equation expresses a power law dependence of MTTF on the temperature swing and exhibits an Arrhenius behavior of thermal activation between MTTF and T_{max}.

To summarize,

1. The Mean Time to Failure (MTTF) metric serves as a measure to estimate the expected time until a material fails due to degradation. Many prevalent chip-related and package-related degradation mechanisms demonstrate an Arrhenius relationship with temperature. However, it is important to note that these empirical models may not be universally accurate and necessitate thorough experimental validation. It is also essential to consider complex relationships with material properties, testing conditions, and microstructures, which require comprehensive experimental validation.

2. This suggests that traditional reliability concepts such as Failure In Time (FIT) and Mean Time To Failure (MTTF) are undergoing a transition. The failure rate

documented by empirical handbooks is no longer sufficient to address the uncertainties associated with field-critical applications. As a result, the future calls for the adoption of real-time online reliability monitoring supported by advanced computational techniques for seamless, non-interruptive system operation. This transition aims to embrace predictive reliability qualification and effectively address the evolving challenges in ensuring reliable performance.

1.4. POWER ELECTRONICS RELIABILITY MONITORING

Reliability, as the highest level of robustness assurance, is essential in ensuring the system's resilience and performance [49]. *Reliability monitoring* can be defined as continuously assessing the device's performance throughout its lifetime to detect early signs of anomalies and implement predictive maintenance strategies to reduce system downtime. Power semiconductor devices are particularly vulnerable to failures due to factors such as high electric fields, high currents, and high temperatures [18]. Field experiences, as illustrated in Figure 1.2, indicated the impact of power component failure and its aftermath, leading to unforeseen system downtime and additional repair costs. Such unexpected maintenance could have been mitigated through early fault detection based on real-time online monitoring. Hence, this section delves into various measurement methods that can support online or offline reliability monitoring.

Monitoring the power device's reliability involves measuring its key performance metric. Particularly in automotive and high-power industrial applications operating in harsh environments, device failure caused by thermal breakdowns outweighs the impact of vibrations and humidity [50, 51]. To address the importance of reliability monitoring, this section summarizes various measurement methodologies, mostly tailored towards thermal methods, as depicted in Figure 1.5. These tailored measurement methods effectively monitors the device condition without interrupting the system during operation. In Figure 1.5, several reliability measurement methods are classified into contact and contactless approaches. In the past, measuring the device junction temperature involved directly probing thermocouples on the device's active surface. However, this method presented various limitations, such as low resolution, contact inaccuracies, and the invasive nature of physical probing [47, 49]. To overcome these challenges, contactless techniques were introduced, which are further subdivided into thermal and non-thermal methods. Among the non-thermal methods, two notable approaches are measuring the device's electrical parameters and using acoustic microscopy. These methods are widespread and commonly used measurement techniques in various industries.

The on-state resistance $R_{DS(on)}$ is a critical electrical parameter that characterizes the resistance to the flow of current through the channel of a device when it is in its conducting state. In most packages, the drain terminal of the device is electrically connected to the package substrate. As a result, the on-state resistance includes the resistance contributions from the die, the die-attach material, and the package substrate. Having a lower $R_{DS(on)}$ is crucial for ensuring optimal device performance with minimal power losses and maximum efficiency. Changes in the on-state resistance directly correspond to performance degradation in the package, particularly in the electrical and thermal

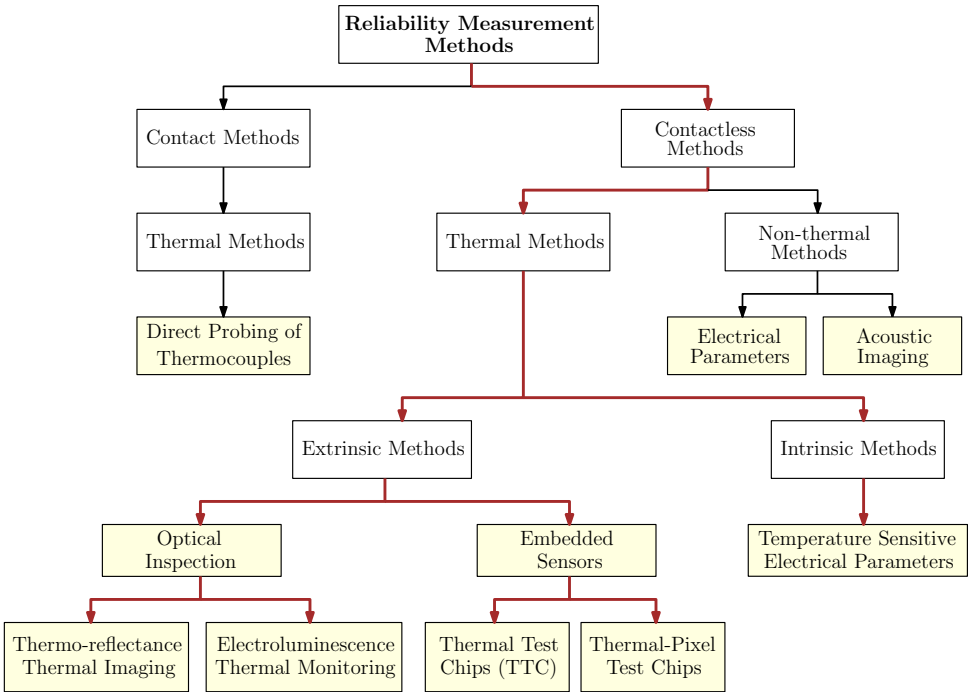


Figure 1.5: Measurement methodologies mostly tailored towards thermal measurements were identified from the literature and shown. Probing a thermocouple was used to identify the junction temperature in early times, which was replaced sooner by contactless techniques, further subdivided into thermal and non-thermal methods. Measuring the device's electrical parameters and acoustic imaging are the most commonly used methods to monitor the device's reliability performance. Thermal methods are further divided into extrinsic and intrinsic methods. Extrinsic methods include optical inspection and embedded sensors. Though several optical techniques exist for thermal measurements, thermo-reflectance-based thermal imaging and electroluminescence-based temperature estimation are studied in depth in this section. Likewise, the intrinsic methods section discusses temperature-sensitive electrical parameters (TSEP). The listed methods are commonly used measurement/characterization techniques employed in academia and industries. The relevance of the above-mentioned methods for online monitoring requires careful consideration and implementation, which are further explained in Section V.

interconnects that are more susceptible to failures. Therefore, monitoring the device's on-state resistance over its lifetime allows for identifying potential issues with the device's electrical performance. However, localized failures or thermal hotspots may not directly reflect in the device's electrical resistance $R_{DS(on)}$.

On the other hand, scanning acoustic microscopy (SAM) is a powerful, non-destructive method for identifying packaging defects. SAM consists of a piezoelectric transducer that generates ultrasonic pulses transmitted to the sample through a water medium. SAM uses water as a coupling medium due to its excellent ultrasonic conductivity and relatively low acoustic impedance. As the ultrasonic waves interact with material interfaces, they undergo reflection and scattering, producing an echo signal that is converted into an electrical output. An image processor then digitizes this signal. The raster scanning

motion of the acoustic transducer generates ultrasonic pulses at high frequencies that are reflected from the sample, thereby capturing the depth information [52]. It is important to acknowledge that SAM, like any imaging technique, has its limitations. The penetration depth of acoustic waves typically ranges from approximately 1 to 2 mm for most materials, and image quality is highly dependent on the properties of the sample being imaged. Encapsulation of semiconductor devices with epoxy molding compounds attenuates acoustic signals, while laminates and PCBs introduce significant reflection and scattering of ultrasonic pulses due to their complex layered structures with different materials. Consequently, an effective strategy for scanning encapsulated packages is to perform through-acoustic scan, before mounting on PCBs. During lifetime testing, power electronic packages are micrographed at intermittent life cycles to identify physical damages resulting from fatigue [53, 54].

The severity of thermal breakdowns has led to the development of various thermal measurement/characterization methods, categorized as extrinsic methods in Figure 1.5. Likewise, semiconductor devices controlling the flow of electrons exhibit temperature sensitive electrical properties. These Temperature-Sensitive Electrical Parameters (TSEP) represent an intrinsic approach that enables direct translation of electrical measurements into device temperature readouts. In the following subsections, each of these contactless thermal measurement methods will be thoroughly reviewed by explaining its underlying physics.

1.4.1. OPTICAL THERMAL INSPECTION

Emissivity, a fundamental material property, plays a crucial role in optical thermal inspection. It refers to a material's ability to emit electromagnetic and infrared (IR) radiation. In an ideal scenario, a perfect emitter would absorb all incident radiation and emit thermal radiation across all wavelengths, and a perfect reflector would reflect all incoming radiation. However, in reality, no material is a perfect emitter or reflector. IR thermography, one of the earliest techniques used in electronics, utilizes IR radiation to detect thermal hot spots and gradients. As all materials above absolute zero emit IR radiation to some extent, IR-sensitive photodiode arrays and microbolometers can measure the emitted infrared energy as a function of temperature. A comprehensive review of IR thermography for non-destructive testing can be found in [55]. Steady-state IR thermography has also been employed to determine in-plane thermal conductance properties of materials [56].

Fiber optic thermal sensors have gained significant interest in recent years due to their advantages, including high sensitivity, wide operating temperature range, rapid response time, immunity to electromagnetic interference, and suitability for use in hazardous environments. These fiber-optic high-temperature sensing systems utilize optical fiber transducers based on various principles such as black body radiation, fluorescence-based techniques, interferometry, or Fiber Bragg Grating (FBG) [57]. For instance, Khatir et al. [58] integrated fluorescence-based optic fibers into a multichip power electronic module to measure the junction temperature and characterize thermal impedance. Other thermal characterization techniques, such as Raman thermometry and liquid crystal thermography, have also been utilized in [59, 60]. While these optical thermal inspection

methods have been extensively reviewed in the past, this section specifically focuses on reflectance-based thermal imaging and electroluminescence-based thermal monitoring methods, providing detailed discussions of their principles and applications.

Thermoreflectance-based Thermal Imaging

The reflective properties are specific to each material and can be influenced by the interaction with electromagnetic radiation. The energy associated with the reflected or scattered light beam exhibits a strong dependence on temperature. Thermoreflectance-based thermal imaging relies on the temperature-dependent surface reflectivity of materials, where thermoreflectance is inversely proportional to the material's thermal conductivity. Consequently, thermoreflectance-based measurements are commonly used to characterize the thermal conductivity of materials in both steady-state and transient-state techniques [61]. In optical thermal imaging systems, thermoreflectance and transient techniques are employed, incorporating detectors with raster scanning capabilities. These detectors comprise photodiode sensor arrays that detect the reflected signals' amplitude and phase shift, as illustrated schematically in Figure 1.6. The rate of change in surface reflectivity with respect to surface temperature change is governed by the thermoreflectance coefficient β, as shown in Eq.1.6. A higher value of β corresponds to a lower noise level in the measurement signal. For example, the thermoreflectance coefficient of aluminum is approximately $2.55\times10^{-5}, \mathrm{K}^{-1}$, while for silicon, it is approximately $1.5\times10^{-4}, \mathrm{K}^{-1}$ [62–64].

$$\frac{\Delta R(T(t))}{R} = \left(\frac{1}{R}\frac{\partial R}{\partial T}\right)\Delta T(t) = \beta \Delta T \tag{1.6}$$

The thermoreflectance coefficient is influenced by the wavelength of the probing medium and the surface roughness. By tuning the illumination wavelength, certain encapsulant materials can become transparent, allowing for noninvasive identification of the device junction temperature. For instance, a thermoreflectance-based thermal mapping of an IGBT power module encapsulated with silicone gel demonstrated that the

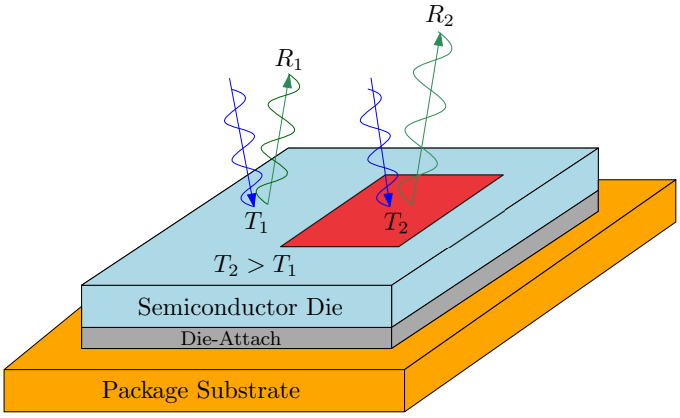


Figure 1.6: The temperature-dependent surface reflectivity resulting in a change in amplitude and phase shift are schematically shown.

silicone gel becomes transparent to visible white light, with green light exhibiting the highest thermoreflectance coefficient [65]. Similar thermal mapping using thermoreflectance thermography has been conducted on the surface of power devices, as documented in [64]. A thermoreflectance thermography setup with a 488nm Ar-Ion laser system at 50MHz frequency was used to capture thermal transients in [66]. This method enables submicron spatial resolution, making it highly effective for detecting hot spots and obtaining precise thermal readings. Thermoreflectance-based thermal imaging is currently the only known method that can capture submicron thermal information.

ELECTROLUMINESCENCE-BASED THERMAL MONITORING

Electroluminescence is a well-established concept, referring to the emission of electromagnetic radiation when a material absorbs energy, typically through an electric current or electric field. It is driven by radiative recombination, where a free electron combines with a positively charged ion (exciton), resulting in the emission of a photon. This phenomenon occurs in direct bandgap semiconductors, such as amorphous silicon and Silicon Carbide (SiC), where there is no change in momentum when an electron transit from valence to conduction band. Consequently, SiC exhibits strong electroluminescence due to radiative recombination. The intensity of electroluminescence in semiconductor devices is influenced by the material's bandgap and doping concentration. Higher impurity concentrations lead to increased electron-hole recombination events and, consequently, higher luminescence intensity.

Compound semiconductors like Gallium Nitride (GaN) and Indium Gallium Nitride (InGaN) are renowned for their high electroluminescence efficiency and find applications

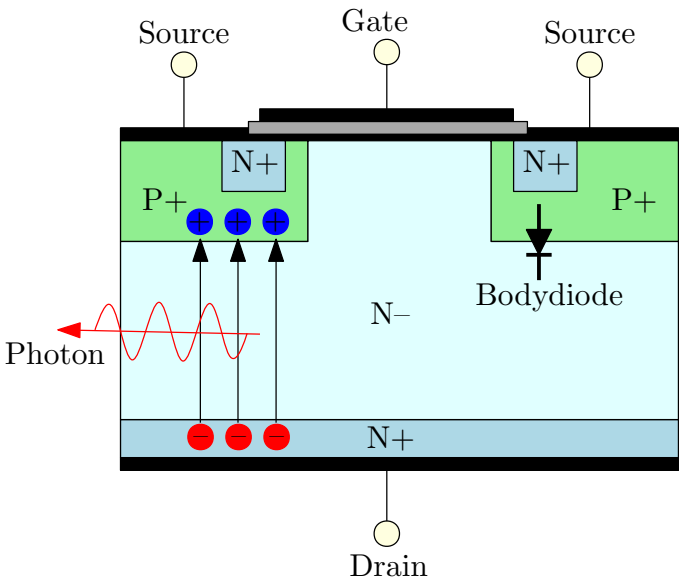


Figure 1.7: Radiative recombination mechanism emitting photons on a SiC vertical MOSFET operating under reverse conduction is schematically shown as a symmetric structure.

in Light Emitting Diodes (LEDs) and Laser diodes. The intensity of electroluminescence is also temperature-dependent, as well as wavelength-dependent. By calibrating the spectral density of the emitted light at a specific wavelength, it is possible to determine the junction temperature. The relationship between the electroluminescence spectrum and the junction temperature of LEDs has been studied in previous research [67, 68].

Electroluminescence-based junction temperature estimation is being successfully implemented in wide-direct bandgap devices, such as SiC MOSFETs. The MOSFET devices have an inherent structure that allows for the formation of a PN Junction between the source and drain terminals, known as the Body diode. Figure 1.7 illustrates the schematic representation of the body diode in a vertical MOSFET construction, accompanied by photon emission resulting from the radiation recombination mechanism. By operating the SiC MOSFET in reverse bias through the body diode, the junction temperature can be determined. The intrinsic body diode of SiC MOSFETs emits visible blue light, which is dependent on the device's current and junction temperature [69, 70]. In a study by [71], a simultaneous extraction method for junction temperature and drain current was demonstrated for SiC MOSFETs based on the device's electroluminescence effect. Two spectral peaks were observed: at a wavelength of 390nm, the luminescence intensity increases with temperature, while an inverse relationship was observed at a wavelength of 510nm. Another study [72] measured SiC light emission by retrofitting a Silicon PiN photodiode into a SiC module. Numerous researchers have successfully estimated the junction temperature of SiC MOSFETs using the electroluminescence effect, making it a promising and non-invasive method for temperature monitoring [73, 74]. Likewise, porous SiC has been reported to yield temperature-dependent photoluminescence properties [75].

1.4.2. Thermal Test Chips

Thermal Test Chips (TTCs) are specialized devices fabricated using the same process technology as semiconductor devices. These chips are equipped with built-in heating and temperature sensing elements, enabling engineers to characterize the thermal behavior of interconnect materials, optimize package thermal performance, and evaluate the effectiveness of Thermal Interface Materials (TIM). Test chips from Thermal Engineering Associates (TEA) [76] contain two metal film resistors, covering approximately 86% of the active surface area, and strategically placed diodes for temperature sensing. Another example is the TTC designed and fabricated by Sattari et al. [77], which contains three Resistance-based Temperature Detectors (RTDs) and six heaters distributed across a 4mm x 4mm area. Metal RTDs offer several advantages over diodes due to their higher sensitivity to temperature. However, the resistance sensitivity of an RTD relies on Temperature Coefficient of Resistance (TCR) of the base material. In a study conducted by [78], TTCs were utilized to characterize nano metallic silver and copper sinter joints.

Fabricating Thermal Test Chips (TTCs) is relatively straightforward and can be performed on various semiconductor substrates. The process begins with depositing an oxide (or) a nitride passivation layer using either Chemical Vapor Deposition (CVD) or Plasma Enhanced CVD (PECVD). Subsequently, the active areas, which include the heating and sensing elements, are defined through lithography. Another passivation layer is

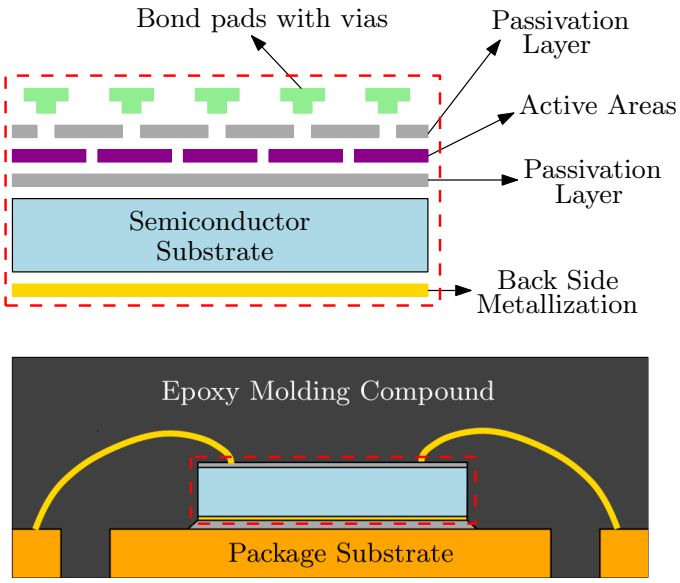


Figure 1.8: A schematic illustration of fabricating a relatively simple thermal test chip with active areas (heating and sensing) is shown. The realized TTCs are assembled into packages to optimize the package's thermal performance.

applied over the active areas, with vertical vias spacing provided for electrical interconnects. Additionally, a bond pad is created for wire bonding or solder bumps. To enhance adhesion with the die-attach material, the backside of the semiconductor substrate is metalized. Finally, the wafer is cut into individual dies and assembled into packages for characterization. Figure 1.8 depicts the steps involved in this process. The fabrication of TTCs follows similar processes as semiconductor devices, and their design can be customized to meet specific requirements. Consequently, TTCs offer an appealing solution for package thermal optimization.

The integration of Thermal Test Chips (TTCs) into functional Power Quad Flat No-Lead (PQFN) surface mount packages for package reliability analysis has been demonstrated in [79]. Furthermore, TTCs have been utilized for characterizing Diamond heat spreaders in advanced packaging solutions [80]. Diamond is renowned for its exceptional thermal conductivity but relatively low thermal capacity, making it an ideal material for heat-spreading applications. To validate the heat-spreading effects across an active device surface, TTCs are particularly well-suited due to their multiple temperature-sensing elements. Numerous researchers have explored the integration of on-chip temperature sensors in electronic modules to analyze the device's thermal performance [81, 82].

1.4.3. THERMAL-PIXEL TEST CHIPS

Thermal-Pixel Test Chips, similar to TTCs, have been developed as a non-destructive method for detecting interface delaminations. These test chips, as demonstrated in [83–87], incorporate thermo-electrical transducers known as "thixels" that operate based on

the 3-Omega (3ω) principle. The 3ω method is widely recognized for its precise measurement of the thermal conductivity of thin films. By applying an electrical current (I) at an angular frequency of 1ω, joule heating ($Q = I^2R$) occurs at a higher frequency of 2ω. The amplitude and phase of temperature fluctuations depend on the material's thermal properties. This perturbation in the heating element's electrical resistance at 2ω is amplified by the driving current at 1ω, resulting in a small voltage signal across the heating element at a frequency of 3ω [88].

Wunderle et al. [83–85] employed the same process technology used for semiconductor devices to fabricate thermal-pixel test chips, which featured an array of 3ω structures patterned on a glass wafer. Each 3ω transceiver on the test chip emitted a thermal wave into the surrounding materials, and the wave was reflected upon interaction with an interface. The thermal wavelength depended on the material and the frequency of the AC signal. When a crack or delamination was present near a 3ω transceiver, the reflected signal caused an increase in the 3ω voltage. By analyzing the reflected signals, packaging defects in the vicinity of the transceiver could be identified. Recent advancements have focused on fabricating thermal pixels on a silicon substrate using flip-chip technology, allowing for higher thixel density and enabling the detection of on-chip interface delaminations and thermal inhomogeneities [86, 87].

1.4.4. TEMPERATURE SENSITIVE ELECTRICAL PARAMETERS

Monitoring the device junction temperature by measuring the Temperature Sensitive Electrical Parameters (TSEP) of semiconductor devices is an effective method for reliability monitoring. Temperature has a profound influence on the material properties on atomic and molecular levels. Atoms vibrate more vigorously with increasing temperature, affecting the kinetic energy and leading to changes in materials' electrical, magnetic, and mechanical properties. In metals, elevated temperatures intensify atomic collisions, impeding the flow of electrons and causing an increase in electrical resistance. Similarly, temperature variations impact the conductivity and carrier mobility of semiconductors. Various temperature-dependent factors, such as charge carrier mobility, doping concentration, and bandgap energy, determine the performance of semiconductor devices [49]. Consequently, electrical measurements can be correlated to device temperature. For a comprehensive understanding of the temperature dependence of semiconductor bandgaps and the underlying principles of power semiconductor devices, refer to [89, 90].

All previously mentioned thermal measurement methods require physical or visual access to the semiconductor device. In contrast, measuring the device TSEP enables estimating the device junction temperature without the need for direct chip access. However, the TSEP assumes a uniform temperature over the complete device, which may not hold true in reality due to surface thermal gradients. Additionally, the TSEP method may not be applicable when the device's electrical parameters exhibit high non-linearity with temperature. A study on various temperature-sensitive electrical parameters of Si, SiC, and GaN power transistors is provided in [91, 92]. In this subsection, we present the temperature dependence of two such parameters of a Through-Hole (TO) packaged N-Channel Silicon Power MOSFET device; the forward bias on-state resistance $R_{DS(on)}$ and

the reverse conduction source-drain voltage V_{SD}. It is essential to realize that the TSEP may vary depending on the type of device (e.g., bipolar junction transistor, field-effect transistor, diode) and the semiconductor material.

ON-STATE RESISTANCE ($R_{DS(ON)}$)

Among the various electrical parameters, the on-state resistance $R_{DS(on)}$ is a critical parameter. It represents the resistance measured across the drain-source terminals of a MOSFET device under forward bias conditions. In a vertical MOSFET configuration, the drain terminal is located at the bottom of the die and is electrically connected to the die pad of the package. Therefore, the measured $R_{DS(on)}$ includes the resistance contributions from multiple components. It is the sum of the semiconductor device resistance under on-state conditions (R_{Die}), the die-attach resistance (R_{DA}), and the package substrate (leadframe) resistance (R_{LF}). The semiconductor device resistance under on-state conditions (R_{Die}) depends on the device structures (trench or lateral). The R_{Die} comprises of the channel resistance (R_{CH}), drift region resistance (R_{drift}), and substrate resistance (R_{sub}). The wire bond resistances R_{wire} can be neglected assuming 4-point Kelvin contacts. All other contact resistances are denoted as R_C. Therefore, the expression for the drain-source on-state resistance $R_{DS(on)}$ of a packaged device can be defined as shown in equation 1.7.

$$R_{DS(on)} \approx R_{CH} + R_{drift} + R_{sub} + R_{DA} + R_{LF} + R_C \tag{1.7}$$

The $R_{DS(on)}$ parameter varies for different devices depending on the semiconductor material and the package assembly processes. Furthermore, the $R_{DS(on)}$ is temperature

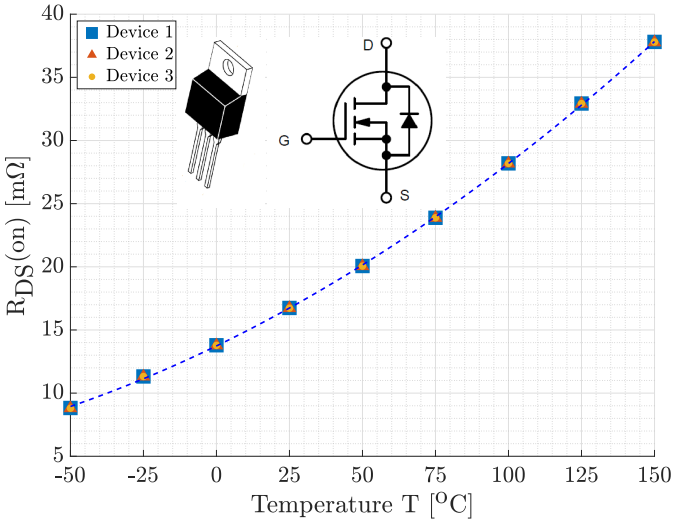


Figure 1.9: R_{DS}(on) of multiple N-Channel Silicon Power MOSFETs assembled in Through-Hole (TO) packages were measured inside a climate-controlled oven at nine different temperatures between −50°C to +150°C. A Gate-Source voltage V_{GS} of 10V is applied with a drain current I_D of 1A.

dependent, and the temperature coefficient(s) of $R_{DS(on)}$ is dependent on its operating characteristics. For instance, when a MOSFET device is turned on, two effects determine the device's behavior with temperature. With increasing temperature, the device threshold voltage reduces, which allows more current to flow through the device than at lower temperatures. In contrast, with increasing temperature, the thermal resistance property of silicon also increases, thereby reducing the flow of current. The resultant effect leads to a critical current limit (at Zero Temperature Coefficient (ZTC)), below which the temperature coefficient experiences a change in sign (negative to positive), and the device experiences a risk of thermal runaway. Therefore, it is essential to understand the device characteristics and it is crucial to calibrate every device to establish the relationship between the electrical on-state resistance $R_{DS(on)}$ parameter and the device temperature.

To exemplify, multiple commercially available N-Channel silicon power MOSFETs in Through-Hole (TO) packages were measured in a climate-controlled oven at temperatures from -50^{o}C to $+150^{o}$C (see Figure 1.9). The device was forward biased with a gate-source voltage V_{GS} of 10V and a drain current I_D of 1A. The resulting voltage difference across the drain-source terminal V_{DS} was measured at different temperatures. Thereby, a relationship between the device's on-state resistance and temperature was established. Consequently, the device's junction temperature during operation can be extracted by measuring its on-state resistance. Similar temperature-dependent $R_{DS(on)}$ measurements on SiC devices have been demonstrated in [93]. Moreover, other parameters such as turn-on saturation current and threshold voltage also have strong temperature dependence (when the device is fully open $R_{CH} << R_{DS(on)}$) that is used to estimate the junction temperature of SiC power MOSFETs in [94].

SOURCE-DRAIN VOLTAGE (V_{SD})

As previously mentioned, Silicon and SiC MOSFETs possess a PN Junction between their source and drain terminals, known as the body diode. This body diode enables conduction in the reverse direction when the gate is off. In power electronics applications, the body diode plays a crucial role in dissipating inductive energy and protecting the MOSFET and circuits from voltage spikes. [95] demonstrated that the body diode of SiC FETs can safely dissipate inductive energy. Furthermore, a comprehensive analysis of the switching performance and robustness of Power MOSFETs' body diodes is provided in [96]. During reverse conduction, the resistance across the various layers in a packaged device remains relatively the same. However, the current direction is reversed, flowing through the body diode, resulting in a voltage drop across the source-drain terminals denoted as V_{SD}. The N-Channel Silicon Power MOSFETs in TO packages were measured by applying a gate-source voltage V_{GS} of 0V, and a negative potential difference was applied between the drain-source terminal ($-V_{DS} = +V_{SD}$) with a source current I_S of 1A.

The voltage difference between the source-drain terminals (V_{SD}) was measured inside a climate-controlled oven at nine different temperatures from -50^{o}C to $+150^{o}$C. The relationship between the source-drain voltage (V_{SD}) and temperature is illustrated in Figure 1.10. A similar experimental investigation of the source-drain voltage (V_{SD}) for temperature estimation during power cycling tests was conducted in [97]. With the increasing demand for SiC MOSFETs in automotive inverter technology, recent research

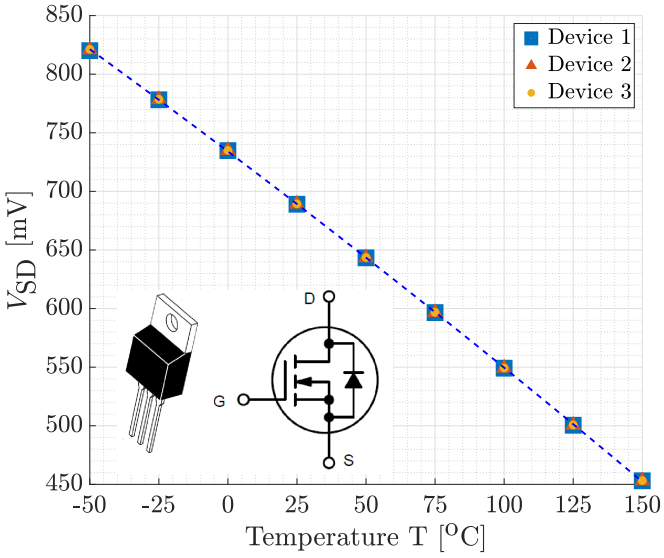


Figure 1.10: The V_{SD} of multiple N-Channel Silicon Power MOSFETs assembled in TO packages were measured inside a climate-controlled oven at nine different temperatures between −50°C to +150°C. A Gate-to-Source continuous voltage V_{GS} of 0V is applied with a source current I_S of 1A.

publications indicate the usage of the intrinsic body diode of SiC devices for junction temperature estimation. The body diode of SiC MOSFETs experiences interface traps when the gate-source terminal is set to zero volts ($V_{GS} = 0$). To mitigate this issue, an alternative approach is to set the gate-source terminal to negative voltages ($V_{GS} < 0V$) on SiC devices [98]. The body diode, also called a parasitic diode, proves to be a valuable component for accurately estimating the device junction temperature without needing external sensing elements. In [99, 100], the junction temperature measurements obtained using the TSEP method were compared with measurements from an IR camera to assess its accuracy.

1.5. COMPARATIVE SUMMARY OF MEASUREMENT METHODS

A summary of the measurement methods discussed in the previous section is presented in Table 1.1, providing an overview of their merits and limitations. Directly probing a thermocouple on the active device surface is a cost-effective approach. Still, it necessitates physical access and relies on the accuracy of surface contact, making it less desirable despite its affordability. Optical inspection offers a contactless and non-invasive means of temperature determination. Infrared (IR) thermography is widely employed for temperature distribution analysis, but the working environment can influence its effectiveness. Fiber optic thermal sensors, on the other hand, offer immunity to electromagnetic radiation, making them suitable for harsh and hazardous conditions. However, both IR and fiber optic sensors are limited to surface measurements. Thermoreflectance-based thermography stands out as the method capable of detecting surface temperatures at

Table 1.1: A comparative summary of the various measurement methodologies are listed with each of its working principle, measurement parameters, advantages, and limitations. To visually aid in representing the strengths and weaknesses of each measurement method, we have ranked them into five categories: Cost, Complexity, Online Monitoring Capability, Accuracy, and Intrusiveness with ranking ranges from 1 to 5, i.e., the most positive (Green shaded area) to the most negative (Red shaded area) outcome.

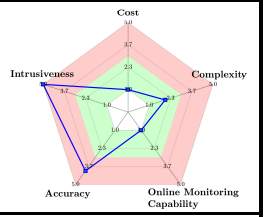
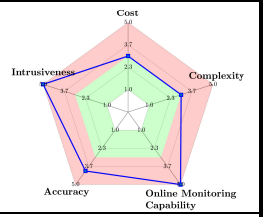
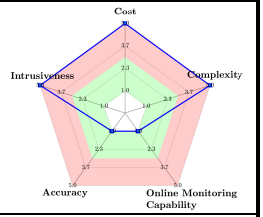
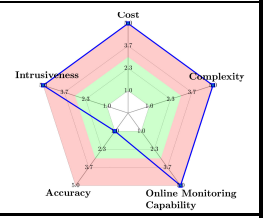
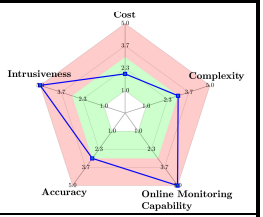
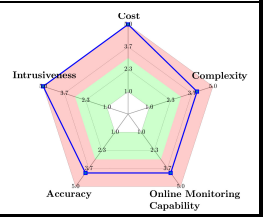
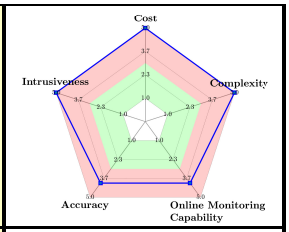
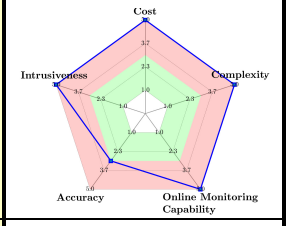
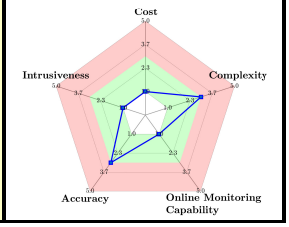
Measurement Method	Working Principle	Measurement Parameter	Advantages	Disadvantages	Graphical Representation
Direct Contact (Thermocouples)	Physical Probing (Seebeck effect)	Voltage / Temperature	1. Low cost. 2. Easy to Implement 3. Suitable for online monitoring.	1. Low Resolution. 2. Contact inaccuracies. 3. Needs physical access to the chip.	
IR Thermography (Optical)	IR Radiation Detection	IR radiation / Temperature	1. Contactless and non-destructive method. 2. Wide temperature range (up to 2000^{o}C). 3. High Resolution. 4. Rapid detection technique.	1. Surface measurement only. 2. Sensitive to emissivity. 3. Accuracy can be biased by its working ambient. 4. Low to High Cost. 5. Requires visual access to the chip.	
Fiber Optic Thermal Sensors (Optical)	Radiation / Fluorescence / Interferometric / Fiber Bragg Grating	Temperature	1. Small size, contactless, and non-destructive. 2. Highly temperature sensitive 3. Immune to EM radiation. 4. Wide temperature range (-200^{o}C to 1000^{o}C). 5. Fast response time.	1. Surface measurement only. 2. Difficult to calibrate. 3. Complex installation and needs visual access. 4. High cost and Fragile components.	
Thermo-reflectance (Optical)	Temperature-dependent Surface Reflectivity	Reflectivity / Temperature	1. Sub-micron spatial resolution. 2. Contactless and non-destructive method. 3. Transparency. 4. Wide temperature range 5. Highly temperature sensitive. 6. Fast response time.	1. Requires reflective surface (material dependent). 3. Difficult to calibrate. 4. Complex installation and need visual access. 5. High cost and requires dedicated setup.	
Electro-luminescence (Optical)	Radiative Recombination	Spectral Intensity / Temperature	1. Contactless and non-destructive method. 2. Low cost - Suitable to measure with optical cameras. 3. Sensitivity and response time depends on the detectors.	1. Surface measurement only. 2. Radiative recombination works only on SiC and amorphous Silicon 3. Difficult to calibrate. 4. Need visual access to the chip.	
Thermal Test Chips (TTC)	Electrical	Resistance / Voltage / Temperature	1. Package optimization, and interface characterization. 2. Same process technology as semiconductor devices. 3. Design to requirements. 4. Small and compact.	1. High Cost. 2. Limited spatial resolution. 3. Limited flexibility. 4. Requires specific electrical layout and direct access.	

Table 2.1: Continued

Thermal-Pixel Test Chips	3ω	Voltage	1. Ideal alternative for acoustic imaging to detect delaminations. 2. Same process technology as semiconductor devices. 3. Small and compact. 4. Suitable to integrate on real functional power devices.	1. Expensive and under development. 2. High computational power (Depending on thixel density). 3. Resolution is proportional to thixel density. 4. Complex integration. 5. Requires specific electrical layout and direct access.	
Acoustic Imaging	Reflection of Ultrasound	Acoustic Impedance	1. Contactless (Non-invasive). 2. Non-destructive method. 3. High resolution and accurate. 4. Various scanning methods (Lateral and through scan with single and sequential steps).	1. High Cost and complex. 2. Ultrasound attenuation depending on materials. 3. Misinterpretation. 4. Direct access and water as a medium.	
Temperature-Sensitive Electrical Parameters (TSEP)	Electrical	Resistance / Voltage / Temperature	1. Non-invasive, non-destructive. 2. Real-time monitoring. 3. High-temperature sensitivity 4. No external sensors 5. Wide temperature range. 6. No visual access is needed. 7. fast time-transients.	1. Assumes uniform temperature distribution. 2. Complex semiconductor device phenomenon can lead to a high non-linearity. 3. High signal-to-noise ratio.	

sub-micron resolution, enabling the identification of micro-thermal hot spots. The transparency of certain materials can be achieved by tuning the illumination wavelength, although this requires complex processes and meticulous calibrations. With the increasing use of SiC MOSFETs, the electroluminescent property of wide-direct bandgap materials emitting visible blue light during reverse conduction has gained attention. Extracting device temperature by calibrating the spectral intensity at a specific wavelength poses a significant challenge. Despite optical methods' non-intrusive and non-invasive nature, visual access to the device is typically required.

Thermal Test Chips (TTC) can be designed for application requirements, allowing engineers to optimize the package's thermal performance. The TTCs consist of embedded temperature-sensitive heating and sensing elements, offering a non-invasive alternate solution to probing a thermocouple onto the device's surface. Recent developments focus on incorporating mechanical strain sensors into the TTCs. However, test chips require additional input/output readout in real-life applications. A recent advancement is the Thermal-Pixel (Thixel) test chip, which utilizes transceivers to emit and receive thermal signals for detecting packaging defects. This approach presents an appealing alternative to acoustic imaging. However, it is important to note that acoustic microscopy offers a unique advantage over other monitoring methods. It enables non-destructive imaging of samples with buried interfaces, providing spatial and depth information. Nonetheless, acoustic imaging requires a dedicated setup and water as a coupling medium.

The Temperature Sensitive Electrical Parameter (TSEP) is a promising methodology for real-time online condition monitoring, as it eliminates the need for external temperature sensing devices. Unlike other methodologies that require direct chip access, the TSEP allows for the extraction of device junction temperature based on its inherent property. The device's on-state resistance $R_{DS(on)}$, which exhibits a strong temperature dependence, serves as a key performance indicator for MOSFETs. Monitoring the on-state resistance over the device's lifetime provides valuable insights into its electrical and thermal performance. However, it is essential to acknowledge that this method assumes a uniform temperature distribution across the device, which may not reflect the actual temperature gradients. This could lead to an underestimation of the device's temperature. Furthermore, the signal-to-noise ratio is influenced by the transient measurement time. Therefore, each method has advantages and limitations, making it necessary to choose the measurement method carefully based on the application.

1.6. CONCLUSION

As global concerns over environmental sustainability and energy conservation intensify, there is an increasing demand for renewable energy generation, energy-efficient systems, industrial carbon-neutral commitments, and electric vehicle transportation. At the core of such transitional technologies lies power electronic devices, which are pivotal in elevating these systems to higher levels of efficiency and performance. However, ensuring the reliability of power semiconductor devices is paramount to ensure the long-term viability and widespread adoption of energy-efficient technologies. This chapter has presented a comprehensive outlook on the current state of power electronics, emphasizing its reliability concerns in field-critical applications, elucidating dominant degradation mechanisms encompassing both chip-related and package-related aspects, and exploring advanced measurement methodologies for reliability monitoring.

Diverse sectors, including low-power consumer electronics, high-value automotive electric vehicles, and high-power industrial applications, drive the global demand for power electronic devices. However, such field-critical applications have been surveyed to suffer from more than 20% of unscheduled maintenance and repairs. The growing concerns about power device reliability and increasing environmental awareness have prompted the establishment of stringent reliability requirements and safety regulations for semiconductor device manufacturers. For e.g., Automotive AEC-Q100/101 – 2000 thermal cycles -55^{o}C/$+150^{o}$C for highest Grade 0 and replacements of lead (Pb) solders and poly-fluoroalkyl (PFA) free substance. The pursuit of higher efficiency and higher reliability has also led to a transition in reliability metrics. The empirical-model-based Failure in Time (FIT) and Mean Time to Failure (MTTF) approaches are being superseded by Remaining Useful Life (RUL) prediction. The semiconductor industry and academia have invested considerable efforts in developing new measurement methods for reliability/condition monitoring to facilitate reliability prediction. A comprehensive overview of various measurement methods, including their underlying physical principles, is provided in this chapter. Based on a thorough review of these techniques, a summary that highlights their respective advantages and limitations was further presented. A multivari-

ate radar chart has been included to interpret the comparison visually. This chart plots the measurement techniques based on five key categories: cost, complexity, online monitoring capability, accuracy, and intrusiveness. The radar chart depicts the strengths and weaknesses of each measurement method, enabling readers to make informed decisions.

Investigating failure and degradation mechanisms is crucial for developing high-efficiency and highly reliable power devices. However, reliability monitoring methods are required for seamless, non-interruptive system operation. Monitoring the device condition makes early detection of faults possible, leading to efficient maintenance strategies and minimizing costly downtime. The integration of reliability monitoring methods, coupled with a deeper understanding of degradation mechanisms, provides a comprehensive and proactive approach to enhancing the reliability of power electronics. Such efforts are crucial in building a sustainable future where energy-efficient and reliable power systems are pivotal in advancing technology, industry, and society.

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2

An Online Condition Monitoring Strategy for Package Reliability Investigation

This chapter introduces an online condition monitoring strategy that utilizes a transient heat pulse to detect package thermal performance degradation. The metric employed is the temperature-dependent transient thermal impedance "$Z_{th}(t,T_{amb})$." The proposed methodology offers quantitative insights into the package thermal performance degradation and effectively pinpoints the presence of multiple failure mechanisms. A Thermal Test Chip assembled in a Power Quad Flat No-Lead package was used in this study to demonstrate the methodology. The packaged devices were first characterized to determine the transient pulse duration, a critical parameter to monitor a specific region of interest. Subsequently, the package thermal performance degradation was continuously monitored online during Thermo-Mechanical Cycling Lifetime experiments. The validity of the measurement results was later confirmed through acoustic imaging and cross-sectional analysis. The changes observed in $Z_{th}(t,T_{amb})$ over thermal cycling corresponds to the delamination of the active metal layers on the die and cohesive failure on the die-attach. This chapter further includes a comparative summary, highlighting the distinctions between the proposed and industry-standard test methods. In conclusion, the importance of online condition monitoring to detect early signs of failure was emphasized, and the proposed methodology's practical applicability in real-life scenarios was briefly discussed.

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2.1. INTRODUCTION

ENSURING the reliability of power electronic packages is crucial in today's rapidly evolving technological landscape, as the scaling of More than Moore and mission-profile-based applications are becoming significantly important [1]. Recent advancements in power electronics reliability research are provided in [2]. Surveys conducted across various highly demanding industrial applications indicate power semiconductor devices to be particularly susceptible to failures [3–8]. Power devices in field-critical applications undergo various stresses, including electrical overstress, mechanical vibrations, environmental humidity, and temperature fluctuations. While electrical, mechanical, and chemical-related issues are essential considerations for package reliability, thermal breakdowns pose a particularly severe challenge [9, 10]. Thermal bottlenecks and thermo-mechanical challenges primarily arise from the packaging materials' inhomogeneities. The mismatch in thermal expansion coefficients between the semiconductor die and the package substrate creates residual stresses, ultimately leading to thermal performance degradation.

Power packages are commonly subjected to rigorous stress tests such as active power cycling [11] and temperature cycling [12] to ensure reliability and meet qualification standards [13, 14]. However, the "test-to-fail" approach mostly involves offline monitoring and necessitates destructive techniques to identify failures. Hence, there is a clear need for online condition monitoring strategies to detect early signs of failure and gain quantitative insights. Further references to condition monitoring methods, online measurements, and lifetime reliability models are provided in [15–23].

In this research, we present a novel methodology for identifying the temperature-dependent transient thermal impedance, denoted as "$Z_{th}(t,T_{amb})$," by utilizing a transient-pulse. Our methodology demonstrates the following in this paper:

1. Online monitoring of package thermal performance degradation during accelerated lifetime testing.
2. Quantitative insights into the package degradation behavior and the ability to detect the presence of multiple failure mechanisms.
3. Applicability of the proposed methodology on functional power devices (MOSFETs, IBGTs) to facilitate application-driven qualification in real-life scenarios.

The following section covers the semiconductor device selection, packaging materials, and the experimental methodology. The experimental results and analysis are presented subsequently with a brief discussion on practical challenges. Lastly, a comparison to the industry standard thermal characterization methods is summarized.

2.2. EXPERIMENTAL METHODS

2.2.1. SAMPLE PREPARATION

Silicon-based Thermal Test Chips (TTCs) are specialized devices fabricated using the same process technology as semiconductor devices. These test chips feature lithographically

defined heating and temperature sensing elements designed to optimize and evaluate package thermal performance. Several research efforts have been devoted to developing TTCs for interconnect material characterization and package reliability assessment [24–27]. Since thermal test chips realistically represent thermal challenges that actual power components experience in operation, we chose them as a test vehicle in this study to demonstrate the online monitoring methodology. However, it is worth noting that the methodology can also be applied to functional power devices like MOSFETs and IGBTs by utilizing their Temperature-Sensitive Electrical Parameters (TSEP) for both heating and temperature sensing purposes.

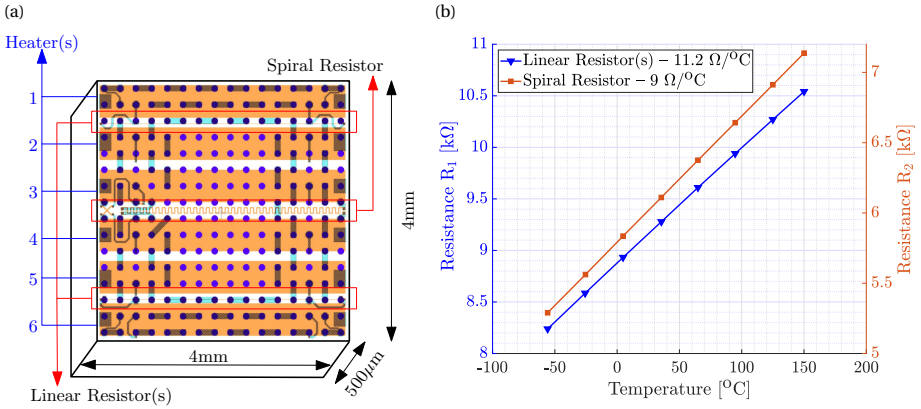

Figure 2.1: (a) Layout of the Thermal Test Chip, depicting its geometry, in-built heaters, and resistors; (b) Resistance sensitivity of linear and spiral resistors evaluated at eight temperature points ranging from -55^{o}C to 150^{o}C, demonstrating a linear temperature dependence.

The TTC chosen for this study contains six heaters and three Resistance-based Temperature Detectors (RTDs) (Figure. 2.1a). The temperature dependence of the linear and spiral RTDs was measured at eight different temperatures ranging from -55^{o}C to 150^{o}C, revealing a linear relationship (Figure. 2.1b). The differences in resistance sensitivity between the linear and spiral RTDs arise from their geometrical variations. Normalizing the resistance sensitivity with the base resistance yields the resistor material's Temperature Coefficient Resistance (TCR). In the remainder of this paper, Heater-3 was used for heating, and the Spiral resistor was used for temperature sensing. Further details about the TTC are provided in [25, 28].

The choice of interconnect material is a critical factor in package assembly. High-temperature Pb-rich solders have been favored in power electronics for their high melting point ($\geq 300^{o}$C) and low stiffness ($\sim 45-60$ GPa). However, their usage has been progressively reduced due to concerns about lead toxicity. An alternative technology for die attachment has emerged in the form of sintering metal particles (lead-free compositions). Metal precursors (Ag/Cu) in paste form are fused under heat and pressure. A review of die-attach materials for high-temperature applications, recent advancements in sintering materials, and lifetime modeling are provided in [29–33].

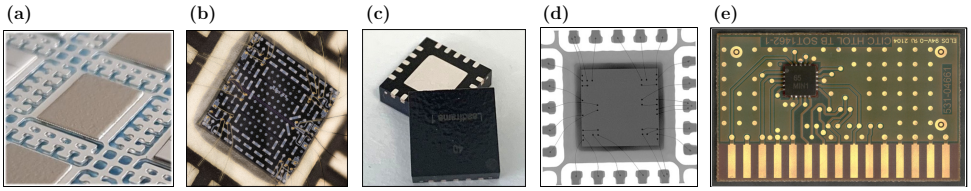

Figure 2.2: Illustration of the steps involved in the package assembly process. (a) Micro-Ag sinter material screen printed on a leadframe, (b) Sintering of a test chip onto the leadframe with wire bonding, (c) Molded, singulated, and laser marked PQFN packages, (d) X-ray inspection of a molded package, and (e) PQFN soldered to a test board for online measurements.

The package assembly process involved in this study is further enumerated below:

- A pressureless micro-Ag sinter material in the form of wet paste was screen printed onto a silver-metalized copper lead frame (Figure. 2.2a).
- The Thermal Test Chip (TTC) was then wet mounted over the sintering paste and sintered in a nitrogen-filled oven at 150^{o}C for sixty minutes, followed by an additional sixty minutes at 200^{o}C. After sintering, electrical connections were established using 99.99% pure gold wire bonds with a bond wire diameter of 25μm and a bond bump of 50μm (Figure. 2.2b).
- Subsequently, the entire stack was transfer molded using an epoxy molding compound, and individual packages were then singulated (Figure. 2.2c).
- The integrity of the package was further assessed through X-ray inspection, which offers high contrast with low-density materials like silicon and polymers compared to heavy metals such as gold and silver. This enables the detection of inhomogeneities in wire bonds and die attachments. An X-ray image of an over-molded package is presented in Figure. 2.2d, illustrating the absence of voids or wire bond failures.
- The packages were soldered onto a specially designed test board with 4-point Kelvin connections extending up to the device, as depicted in Figure. 2.2e. The solder joint interface was assumed to remain stable during the lifetime test.

2.2.2. EXPERIMENTAL SETUP

A dedicated setup was developed for online monitoring of the package condition during Thermo-Mechanical Cycling Lifetime (TMCL) testing, as illustrated schematically in Figure. 2.3. The test boards, soldered with PQFN packages (Figure. 2.2e), were securely placed on a test socket inside a temperature cycling oven. The electrical connections from the test socket were extended to the sourcing and measuring equipment using a multiplexer (switch matrix), allowing for sequential measurements. The source unit has 40V compliance at 1A in continuous mode and 20V at 10A in pulsed mode. A trigger synchronization and communication protocol (TSP) was established between the instruments to ensure proper synchronization and communication. A dedicated control program exchanges data between the master computer and the TMCL oven. A user-defined Matlab program manages all instrument communications.

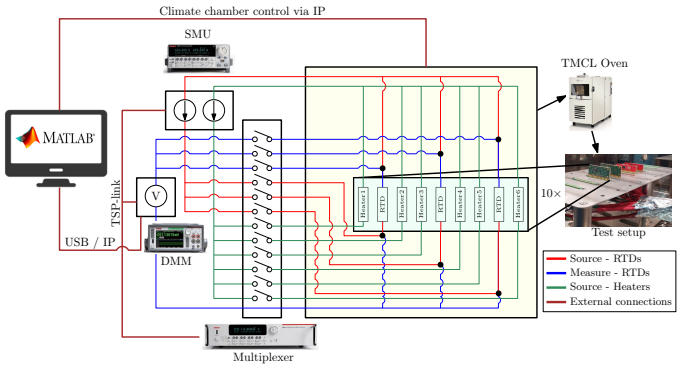

Figure 2.3: Schematic of the experimental setup for online condition monitoring during accelerated lifetime testing. Packaged devices, soldered to the test boards, are placed in dedicated slots inside a temperature-cycling oven. Test boards are connected to an SMU and a DMM through a multiplexer for sequential measurements.

The measurement conditions were fine-tuned to optimize the sensitivity of Resistance-Based Temperature Detectors (RTDs). Various input currents were applied to the test chips to determine the optimal measurement currents (≤0.3mA) with minimal self-heating. The measuring equipment has a resolution of 1μV for measurements in the 10V range, and the accuracy was determined to be within ± 0.1mV. Further information regarding measurement variation, repeatability, and reproducibility can be found in [28]. While the electrical layout depicted in Figure. 2.3 pertains to the test chip configuration, the test setup also features dedicated slots designed to measure up to 15 MOSFETs and/or IGBTs sequentially.

2.2.3. EXPERIMENTAL CHARACTERIZATION

The thermal characterization methodology employed in this study is an adaptation of the JESD51-14 transient dual interface test method [34]. To analyze the package thermal performance, it is necessary to measure the transient thermal impedance $Z_{th}(t)$. This parameter represents the packaging materials' ability to dissipate heat, and it is a sum of individual layer resistances R_{th}. In this study, Heater-3 was used for heating, and the spiral resistor (RTD-2) was used to measure the change in electrical resistance due to heating, which further translates to device temperature. To ensure efficient heat dissipation, the test boards were clamped onto a water-cooled heat sink, and the thermal characterization was conducted with and without a Thermal Interface Material.

A continuous current of 100mA (equivalent to approximately 0.7W or 32W/cm^2 @25^{o}C ambient) was supplied to heater-3 for a duration of 100 seconds. This current value was selected in consideration for online monitoring experiments during thermal cycling. The intention was to apply a brief localized heat pulse that would generate sufficient heat for package thermal performance analysis without deviating beyond the limits set for thermal cycling. The resulting changes in the resistance of RTD-2 were measured to determine the device temperature. During the 100-second heating period, the device and packaging materials reached a one-dimensional steady state, allowing the extraction of the resistance-capacitance network. This was achieved by computing the structure-

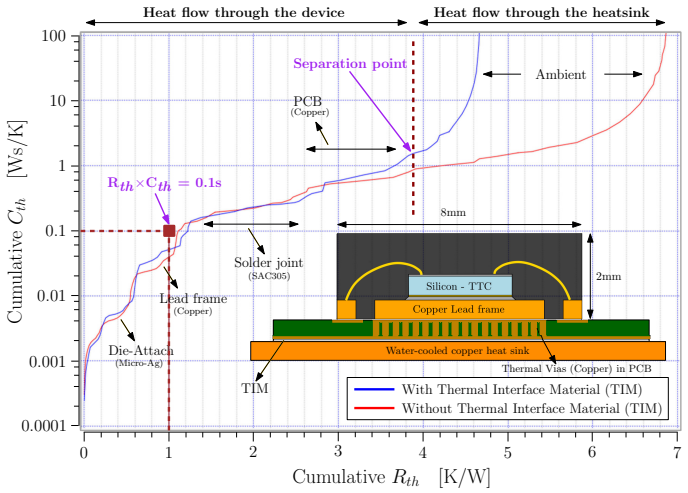

Figure 2.4: Cumulative resistance (R_{th}) – capacitance (C_{th}) network graph from the measured data. The PQFN on a test board, mounted on a water-cooled heat sink, allows heat to flow from the device toward the heat sink. Analysis with and without a Thermal Interface Material (TIM) identifies the key heat dissipation information, notably at the die-attach interface, within a 0.1-second transit time window.

function, as described in [35–37]. The TDIM-Master software provided by JEDEC [34] was used for time-constant spectrum deconvolution and foster-cauer transformation. The computed results of the structure-function are depicted in Figure. 2.4, along with a schematic representation of the PQFN package on a PCB mounted to a heat sink.

Based on the thermal characterization measurements depicted in Figure. 2.4, the following conclusions and assumptions were drawn to support the online condition monitoring experiments:

1. Figure. 2.4 illustrates the separation point distinguishing the heat flow paths between the device (PQFN + PCB) and the heat sink. Regarding heat flow through the device, the primary sources of resistance are the package solder joint interface and the PCB.

2. Given that the die-attach interface is the region of interest, a transient pulse duration of 0.1 seconds was chosen for localized heating and online condition monitoring, as highlighted in Figure. 2.4. The transient pulse duration of 0.1 seconds was chosen to limit the influence of the solder joint and the PCB materials.

3. The 0.1-second heating window defines a thermal resistance boundary of 1K/W (Figure. 2.4). Due to thermal aging, the packaging material's thermal resistance might shift, subsequently altering the boundary conditions for a 0.1-second heating interval. Since the region of interest is to monitor the die-attach interface, we assumed that the thermal resistance shift of the die-attach layer over the lifetime testing would not exceed the thermal resistance boundary.

2.2.4. ONLINE CONDITION MONITORING METHODOLOGY

Packaging materials undergo degradation over time, influenced by operational and environmental conditions. Package degradation may cause an increase in thermal resistance and impede heat dissipation, resulting in elevated device temperatures. Traditional thermal characterization methods, such as MIL-STD-883E, involve invasive means to measure the device junction and its case temperatures to determine the "steady-state" thermal impedance [38]. This method has been surpassed by transient thermal impedance measurements proposed by Szekely [35], which has been adopted as the JEDEC standard JESD51-14 [34]. These approaches are suitable for offline monitoring and thermal characterization.

In this study, we introduce a novel "temperature-dependent transient-pulse test method" to obtain the temperature-dependent transient thermal impedance, denoted as $Z_{th}(t,T_{amb})$. The transient time is the transient pulse duration illustrated in Fig. 2.4, and the temperature dependence is established by measuring $Z_{th}(t)$ at different temperature ambients during TMCL testing. This approach allows for the package's thermal behavior to be characterized under dynamic conditions.

The TMCL tests were in accordance with the guidelines outlined in the JESD22-A104 standard [12], and automotive norms AEC-Q101 [14]. The PQFNs with TTC soldered to the PCB underwent thermal cycling from -55^oC (compression state) to 150^oC (expansion state), as illustrated in Fig. 2.5. The temperature cycling rate was maintained at approximately 1-2 cycles per hour, with a rise time (t_{rise}) and fall time (t_{fall}) of around ten minutes. The dwell time (t_{dwell}) was dependent on the time required for the oven to reach a stable

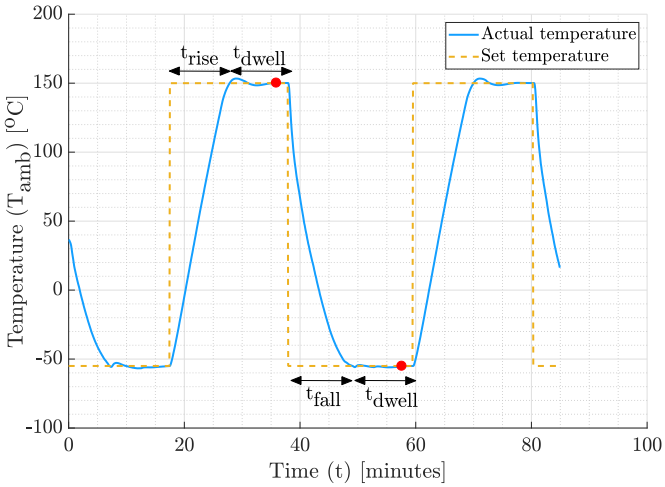

Figure 2.5: The graph illustrates the temperature cycling profile adapted according to JEDEC standards for automotive-grade discrete semiconductor devices. The devices are cycled at 1-2 cycles per hour. The Z_{th}(t = 0.1s) was measured during every cycle once the oven reached a stable temperature, as indicated by a red dot in the graph.

temperature. Although thermal cycling is a relatively slow process for power device aging, the transient pulse measurements for online monitoring take only a few seconds per device. Once the oven's temperature stabilized, a short transient heat pulse of 0.1 seconds was applied using Heater-3, and the device temperature was measured using RTD-2. It is important to be aware that the measurements were conducted without a water-cooled heat sink due to thermal cycling.

The transient pulse response of RTD-2 measured at −55°C and 150°C is shown in Fig. 2.6, along with the applied input power for the heater. The initial fluctuations observed within the first 0.2 seconds are a measurement artifact resulting from the trigger range settings of the sourcing equipment. The differences in power input at −55°C and 150°C are due to the temperature sensitivity of the heater material. Hence, the temperature change ΔT was normalized with the applied input power to obtain the transient thermal impedance $Z_{th}(t)$. The $Z_{th}(t)$ parameter was determined during the heating phase since the heating time chosen was not long enough for the device to reach a steady state. Besides, the test chip has separate structures for heating and sensing, with heating power remaining relatively constant during the heating pulse time and no electrical cross-talk occurring to the sensing element. Hence, in accordance with JESD51-14 standards, it is acceptable to extract $Z_{th}(t)$ during the heating phase.

The $Z_{th}(t)$ obtained from Fig. 2.6 exhibit strong temperature dependence, which can be attributed to the temperature-dependent thermal properties of the packaging materials. The micro-Ag sinter die-attach and the copper lead frame exhibit minimal temperature dependence within the thermal cycling temperature range [39, 40]. However, the thermal properties of the semiconductor substrate (Silicon) undergo significant changes with temperature [41]. Therefore, the observed change in temperature ΔT between −55°C

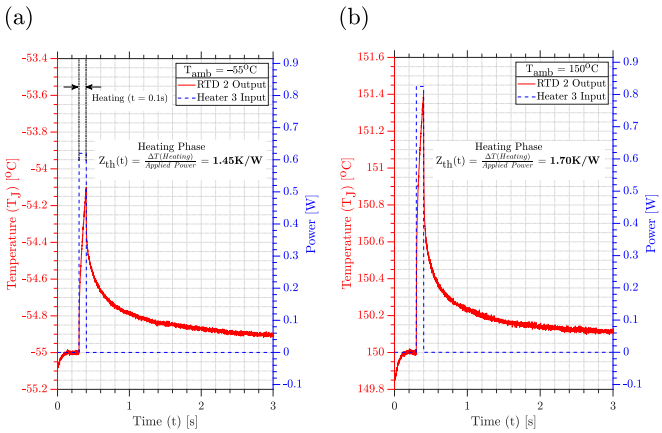

Figure 2.6: (a) Measurements at −55°C, and (b) Measurements at 150°C. A 0.1s, 100mA heat pulse applied to Heater-3, with junction temperature (T_j) measured using RTD-2 at different ambient temperatures (T_{amb} = −55°C and 150°C). The applied power input varied with T_{amb} due to the temperature sensitivity of the heater material. Differences observed in $Z_{th}(t)$ at different T_{amb} result from the temperature-dependent thermal properties of packaging materials, where silicon plays a significant role.

and 150°C (Fig. 2.6) is influenced by the temperature-dependent properties of the silicon substrate. A theoretical explanation of the temperature-dependent properties of the packaging materials and their impact on the relative change in temperature ΔT is provided in [28]. The change in temperature-dependent transient thermal impedance "$Z_{th}(t,T_{amb})$" parameter over "N" thermal cycles indicating the package's health is demonstrated in the subsequent section. It is important to be aware that an increment in $Z_{th}(t)$ would suggest degradation and the dissimilarities at different temperatures $Z_{th}(t,T_{amb})$ would signify the degradation behavior.

2.3. EXPERIMENTAL RESULTS

2.3.1. ONLINE CONDITION MONITORING RESULTS

The transient thermal impedance $Z_{th}(t)$ obtained from the transient pulse measurements (Fig. 2.6) was continuously monitored during thermal cycling until a sufficient amount of data on package degradation was obtained to demonstrate the online monitoring methodology. Ideally, the $Z_{th}(t)$ should remain constant (within the measurement variability) over time. However, due to continuous cyclic loading, the packaging materials tend to degrade, resulting in an increase in the $Z_{th}(t)$ value. Since the transient time is kept short (t = 0.1 seconds), the obtained time-transient Z_{th} information reflects the behavior of the materials near the die, such as the die-attachment, as observed in the experimental characterization (Fig. 2.4). The measurement results of 436 thermal cycles at −55°C and 150°C are presented in Fig. 2.7.

To facilitate visual interpretation of the measurement data and identify the degradation trend, Simple Moving Averages (SMA) were calculated for the variable vector $Z^i_{th}(t)$ over N observations. The 5-cycle moving average highlights short-term fluctuations in the measurements, while the 50-cycle moving average smooths out variations and reveals long-term trends. The 50-cycle SMA data at −55°C (Fig. 2.7a) indicates a gradual increase in thermal impedance, signifying degradation of the packaging materials due to repeated thermal cycling-induced expansion and contraction. Similarly, the 50-cycle SMA data at 150°C (Fig. 2.7b) also suggests comparable indications of package degradation. However, comparing the measurement data at −55°C and 150°C indicates dissimilarities in the

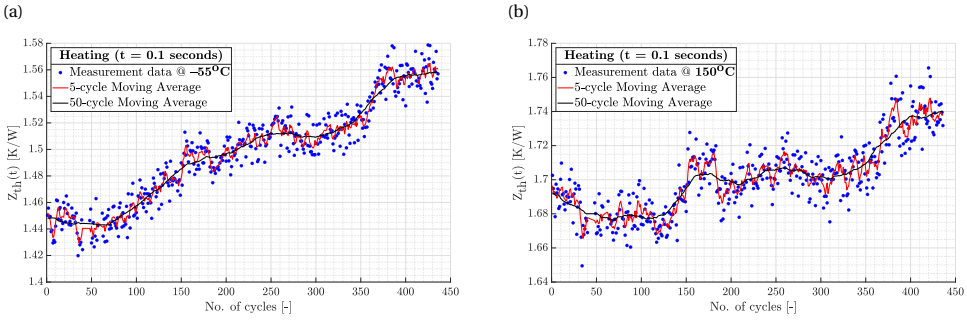

Figure 2.7: (a) Measurement data at −55°C , and (b) Measurement data at 150°C. The measurements were halted at 436 cycles, as the acquired data was deemed sufficient to demonstrate the methodology.

$Z_{th}(t)$ trend. Consequently, the 50-cycle SMA data from -55^oC and 150^oC were plotted together for further analysis, as depicted in Fig. 2.8.

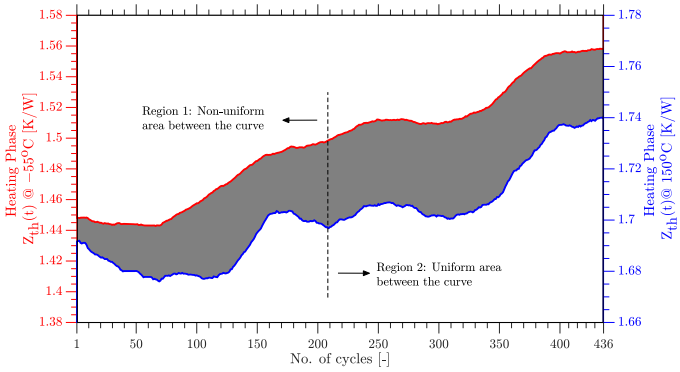

Figure 2.8: The differences in the measurements at -55^oC and 150^oC are visualized by highlighting the area between the curves. Two distinct regions (Region-1 and Region-2) can be identified within the highlighted area. Region-1 indicates a non-uniform increase between the curves, and Region-2 indicates a relatively uniform increase.

Two distinct regions, namely Region-1 and Region-2, can be observed by comparing the area between the curves. In Region-1, the area between the curves shows a non-uniform increasing trend, while in Region-2, the area remains relatively uniform with marginal variations. One possible explanation for such distinct regions can be due to the interplay of multiple failure mechanisms influencing the measurements of $Z_{th}(t)$. Under compression, defects such as delamination and/or in-plane fractures may grow, leading to larger thermal resistances. Conversely, the defects might close during expansion, resulting in lower thermal resistance. Such behavior can induce different thermal responses at -55^oC and 150^oC as observed in Fig. 2.8. This reasoning aligns well with the non-uniform increasing trend observed in Region-1. However, beyond ~210 cycles (Region-2), the thermal resistances increase uniformly at -55^oC and 150^oC. This suggests that the dominant failure mechanism in Region-1 may differ from that in Region-2. It is important to note that the interpretation provided here based on the experimental results represents one of several possible explanations. The device was subjected to acoustic imaging (CSAM) to investigate further and provide quantitative evidence, followed by cross-sectioning to gather comprehensive insights.

2.3.2. FAILURE ANALYSIS

Confocal Scanning Acoustic Microscopy (CSAM) is a highly effective imaging technique for the non-destructive identification of delaminations occurring at buried interfaces within electronic packages [42, 43]. Fig. 2.9a illustrates CSAM imaging obtained from a reference 0-hour sample, where no indications of delaminations were detected. However, a notable contrast emerges when examining the device under test after 436 thermal cycles, as displayed in Fig.2.9b. Delaminations near the overmold-die interface are visible in the image. Although the exact cause of these delaminations remains unknown, we consider them a significant contributing factor to the observed increase in thermal impedance

during online monitoring. To conduct further analysis, the sample was cross-sectioned, and the location of the cross-section is indicated in Fig. 2.9b.

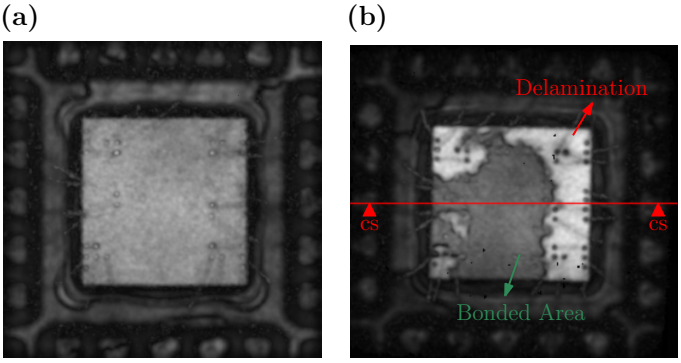

Figure 2.9: (a) Reference PQFN sample at 0-cycle, and (b) Device Under Test after 436 thermal cycles. A sequential lateral scan (C-scan) analysis reveals signs of delamination near the overmold-die interface, clearly distinguishable from bonded areas in the thermally cycled sample. Further cross-sectioning of the delaminated sample is highlighted in (b).

The tested PQFN package was potted in an epoxy resin and meticulously cross-sectioned by polishing at a step of 25 microns with 150 RPM and 5N force. After the completion of the polishing procedure, a comprehensive analysis of the sample was conducted. The cross-sectioned sample was examined using an optical microscope and an electron microscope near the overmold-die interface. This analysis aimed to identify the root cause of the delamination observed during CSAM imaging. Upon close inspection of the cross-sectional images taken in proximity to the overmold-die interface (Fig. 2.10a), it became evident that the active-metal layers consisting of a 100nm titanium film on the silicon substrate had experienced delamination from the silicon dioxide passivation layer. This delamination is most likely attributed to residual stresses originating from the manufacturing process or thermo-mechanical stresses encountered during testing.

Further analysis was conducted on the cross-sectional sample, focusing on the region near the die-attach interface. Fractures within the micro-Ag sinter die-attach material were observed (Fig. 2.10b). These fractures exhibited a distinct pattern. The fractures aligned parallel to the die interface at the center, while towards the edges, the fractures were inclined into the bulk of the silver sinter material. Repeated thermo-mechanical loading conditions caused the die-attach interface to endure cumulative stress damage from continuous expansion and contraction. The fracture behavior exhibited by the micro-Ag pressureless sinter material raises concerns regarding its reliability. Therefore, further research on sintering materials is crucial to identify an optimal replacement for high-Pb solders.

Based on the findings from CSAM and cross-sectional analysis, the following conclusions can be drawn, which align in line with the online monitoring measurement results shown in Fig 2.8.

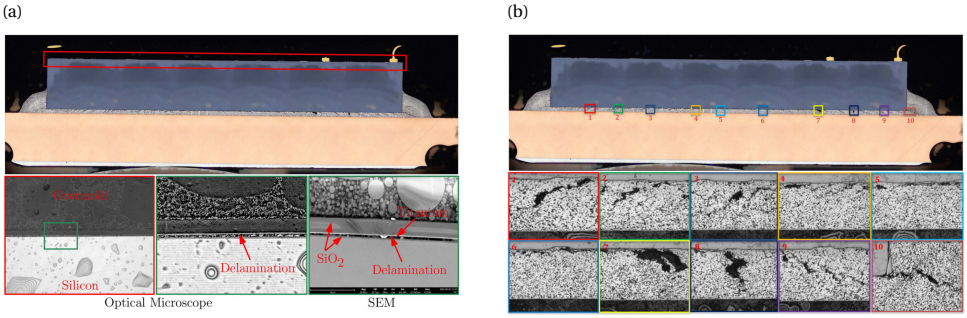

Figure 2.10: (a) Cross-sectional micrographs focused near the overmold-die interface indicate delamination of titanium metal layers from the silicon dioxide passivation layer on the test chip. (b) Cross-sectional micrographs focused near the die-attach interface indicate a cohesive failure within the bulk of the micro-Ag sintered die-attach material. Notably, fractures align parallel to the die in the center and are inclined towards the bulk along the edges.

1. Two distinct failure mechanisms were identified: (i.) Delamination of active metal layers from the passivation layer, confirmed by CSAM and cross-sectional analysis, and (ii.) Die-attach failure. The micro-Ag pressureless sinter material experienced significant long-term fractures under repeated cyclic loading conditions.

2. The analysis quantifies the experimental results and confirms the presence of multiple failure mechanisms.

2.3.3. DISCUSSION

The online condition monitoring methodology proposed in this study has demonstrated its capability for real-time assessment of the package's health and performance, particularly during accelerated lifetime tests (thermal cycling). Nevertheless, it is essential to acknowledge the practical challenges that accompany this methodology and its applicability in real-life situations.

- The proposed method has demonstrated its effectiveness in monitoring package thermal performance degradation. However, with a complex interplay of multiple failure mechanisms (Fig. 2.8), decoupling the influence solely from the experimental results remains challenging. Hence, the methodology requires further testing and validation.

- The thermal resistance of the various packaging layers might shift over time due to aging. Based on the experimental results (Fig. 2.7), the relative change in thermal resistance $\Delta Z_{th}(t,T_{amb})$ over 436 thermal cycles was ~0.1K/W, which remains within the thermal resistance boundary highlighted in Fig. 2.4. Hence, in this particular testing condition, the assumption to consider a 0.1-second heating interval was appropriate. However, this needs to be verified for different package geometries.

- Temperature significantly affects the semiconductor material's conductivity and carrier mobility. By utilizing the temperature-sensitive parameters, the transient thermal impedance based on a transient pulse can be determined in functional

power devices (MOSFETs, IGBTs). Hence, the methodology is not bound to thermal test chips but can be applied to other temperature-sensitive devices.

- Additional refinements are required for monitoring the devices online in real-life scenarios. The transient thermal impedance must be measured in real-time at a predefined interval without disrupting the system operation. It is also necessary to capture the ambient conditions (temperature, humidity, etc.) while measuring the transient thermal impedance. The objective is to create a continuous, longitudinal dataset spanning the device's lifespan, analyzing its real-time thermal performance in correlation to environmental factors.

- In this study, moving averages were used to reduce measurement variation and identify the degradation trend. Recent advances in Machine Learning techniques involving Artificial Neural Networks and Convolutional Neural Networks enhance prognostic monitoring and enable failure mode classification [44, 45].

2.4. PROPOSED METHODOLOGY COMPARED TO INDUSTRY STANDARD METHODS

Despite the aforementioned practical challenges, the proposed methodology provides compelling reasons for its adaptation as an online condition monitoring tool for package reliability assessment. For decades, measuring the package thermal impedance has been a standard practice in the industry, serving as a pivotal metric for evaluating package thermal performance. Established standards such as MIL-STD-883E [38] and JESD51-14 [34] have provided guidelines for determining the steady-state and transient-state thermal impedance.

This research takes a step further in determining the temperature-dependent transient thermal impedance. This innovative approach leverages transient heat pulses to identify the changes in thermal resistance within a specific region of interest. Notably, the transient time is instrumental in delineating the boundary conditions for continuous monitoring. A comprehensive summary is presented herein, comparing the proposed methodology with established industry-standard test methods outlined in MIL-STD-883E and JESD51-14. This comparison spans various facets: purpose, suitability, measurement methodology, metric employed, advantages, and limitations (Table 2.1).

Besides, several research efforts have been devoted to establishing online condition monitoring based on diverse prognostic device health management measurement methodologies. These measurement methods can be broadly classified as follows: contact (probing) [15, 16] and contactless techniques, thermal and non-thermal (electrical, acoustic [43, 46], etc.) methods, extrinsic methods involving sensors [47–50], and intrinsic methods (Temperature Sensitive Parameters [51]), and reliability modeling methods [22, 23]. Notably, most of these measurement techniques necessitate physical or visual access to the device and are intrusive to device operation, limiting their practical applicability in real-life scenarios. In contrast, the methodology proposed in this study monitors the package's thermal performance without requiring physical or visual access. This char-

Table 2.1: The online monitoring methodology proposed in this paper against the industry standards MIL-STD-883E and JESD51-14.

	MIL-STD-883E Thermal Characteristics Testing Method	**JESD51-14 Transient Dual Interface Test Method**	**Proposed Methodology Temperature Dependent Transient-Pulse Test Method**
Purpose	To determine the Junction-to-Case thermal impedance of a package.	To determine the packaging materials individual layer contribution towards Junction-to-Case thermal impedance.	To determine the package's thermal performance degradation based on temperature-dependent (ambient) transient thermal impedance.
Application / Suitability	1. Thermal Characterization. 2. Offline monitoring during accelerated lifetime testing.	1. Thermal Characterization. 2. Offline monitoring during accelerated lifetime testing.	1. Thermal Characterization. 2. Online monitoring during accelerated lifetime testing.
Methodology	1. Measure the device junction and case (package substrate) temperature at steady-state by external sensors (extrinsic) and/or temperature sensitive device parameters (intrinsic).	1. Measure the change in the device junction temperature (extrinsic or intrinsic) to compute the resistance – capacitance network. 2. Requires a water-cooled heat sink to achieve a one-dimensional conductive heat flow path.	1. Pre-characterization is required based on the JESD51-14 test method to identify the transient pulse duration. 2. Ambient conditions to be recorded. 3. Measure the change in the device junction temperature (intrinsic) by applying a transient heat pulse.
Measurement parameters	"Steady-state" thermal impedance - $\mathbf{Z_{th\text{-}JC}(t = \infty)}$	"Transient-state" thermal impedance - $\mathbf{Z_{th\text{-}JC}(t)}$	"Temperature-dependent transient-state" thermal impedance - $\mathbf{Z_{th}(t,T_{amb})}$
Advantages	1. Easy to implement. 2. Less computational effort. 3. Precise estimation of Junction-to-case package thermal impedance.	1. Accurate thermal characterization. 2. Enables estimating the individual layer thermal resistance-capacitance network. 3. Non-destructive method.	1. Fast and accurate measurements. 2. Online monitoring. 3. The presence of multiple failure mechanisms can be identified. 4. Advanced data analytics can improve identifying degradation trends. 5. Includes the advantages of JESD51-14 test method.
Limitations	1. Invasive method. 2. Offline monitoring.	1. Assumes one-dimensional heat flow. 2. High signal-to-noise ratio. 3. High computational effort. 4. Offline monitoring.	1. Requires further tests and validation. 2. Additional refinements are needed for real-life applications. 3. Lifetime reliability models are needed to understand the aging mechanisms. 4. Includes the limitations of JESD51-14 test method.

acteristic underscores its potential as a viable solution for online monitoring in real-life applications.

2.5. CONCLUSION

In response to the growing demand for reliable power semiconductor devices in field-critical applications, particularly in environments prone to thermal breakdown, an online condition monitoring methodology has been introduced in this study. The methodology facilitates real-time detection of thermal degradation within packaged devices. An accelerated lifetime test (thermal cycling) was conducted in this study to validate the methodology. Based on the changes monitored in the temperature-dependent transient thermal impedance $Z_{th}(t,T_{amb})$, we were able to understand the package degradation behavior and identify the presence of multiple failure mechanisms.

The proposed methodology was demonstrated using a Thermal Test Chip (TTC) integrated into a Power Quad Flat No-Lead (PQFN) package as a test platform. The transient dual-interface test method from JESD51-14 was adapted to determine the optimal transient pulse duration, a critical parameter for acquiring thermal performance data within the region of interest. During TMCL testing, an increase in $Z_{th}(t)$ was observed at different ambient temperatures (T_{amb}), indicating thermal degradation due to cyclic loading.

Disparities in measurements at different ambient temperatures hinted at multiple failure mechanisms, later confirmed through confocal scanning acoustic microscopic (CSAM) analysis and cross-sectional inspection.

The proposed methodology has proven effective for online monitoring and offers quantitative insights into the degradation behavior. In this paper, we further discussed the practical challenges associated with the methodology and highlighted distinctions between the proposed and industry-standard methods. The applicability of the online monitoring methodology in real-life applications requires additional refinements, which were briefly discussed. The experiments were demonstrated with Thermal Test Chips in a PQFN package subjected to thermal cycling. However, the methodology can also be applied to functional power semiconductor devices and other accelerated aging processes. The proposed method's significance lies in the early detection of signs of failure or degradation, thereby preventing unexpected system downtime and additional costs.

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3

PROGNOSTICS OF POWER QFN PACKAGES WITH SILVER SINTERED MATERIALS

This chapter delves into the prognostics of Power QFN packages with four distinct silver sinter pastes, each varying in material composition (pure-Ag and resin-reinforced hybrid-Ag) and sintering processes (pressure-assisted and pressureless). The PQFN packages with silver sintered die-attach materials were subjected to thermal cycling tests (−55 to 150^{o}C), and the performance degradation was evaluated based on the following metrics: (i.) Electrical on-state resistance R_{DSon} monitored periodically at specific thermal cycling intervals, and (ii.) Transient thermal impedance $Z_{th}(t = 0.1s)$ monitored online during thermal cycling. These measurements were further validated using acoustic microscopy imaging and cross-sectional inspection. The pressureless Ag-sintering material demonstrated comparable performance to pressure-assisted Ag-sintering, with a dense microstructure and consistent electrical and stable thermal performance. Whereas the pressureless resin-reinforced hybrid-Ag material exhibited degradation with a relative increase of ∼33% in R_{DSon}, ∼38% in $Z_{th}(t = 0.1s)$, and ∼67% delamination of the die-attach interface over 1000 cycles. These findings suggest that pressureless Ag-sintering may offer a viable alternative to pressure-assisted methods for Pb-free die-attachments, while resin-reinforced hybrid-Ag requires further development for improved thermo-mechanical reliability.

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3.1. INTRODUCTION

RELIABILITY stands as a critical performance metric for sustainable packaging in electronics. However, meeting reliability requirements presents several challenges. These include catering to field-critical applications, enduring harsh environmental conditions, complying with rigorous testing and safety regulations, accommodating the demand for higher power density, managing complex integration processes, and navigating uncertainties due to new materials [1–4].

The dominant degradation mechanism on electronic packages arises from temperature fluctuations and mismatched material properties, particularly die-attach layers subjected to thermo-mechanical loading conditions [5, 6]. Growing emphasis on the robustness of die-attach materials is challenged in meeting application-specific requisites. Restrictions on lead (Pb) solders and concerns over the environmental and health impacts of 1-methyl-2-pyrrolidone (NMP) and Per-and-Poly-FluoroAlkyl Substances (PFAS) regulate material suppliers to review the chemicals used in their die-attach adhesive manufacturing processes. [7, 8].

Silver sintering technology offers a promising solution for Pb-free die-attachments in electronic packaging due to its low electrical resistivity (<2$\mu\Omega$-cm) and heightened thermal conductivity (~100–200W/mK) [9–14]. Additionally, silver sintering allows processing at relatively low temperatures (~200–300^{o}C) while achieving a high melting point (~900–1000^{o}C) after processing, reducing the risk of oxidation compared to copper sintering materials [15]. However, the formation of reliable sintered interconnects for both silver and copper pastes is influenced by several factors, including paste rheology (solvents and binders), particle composition (shape and size distribution), sintering process parameters

Table 4.1: Storage and process conditions of silver sinter pastes used in this study. The process conditions were chosen based on prior experimental analysis.

	Material-A	**Material-B**	**Material-C**	**Material-D**
Type	Pressure Ag-Sintering	Pressure Ag-Sintering	Pressureless Ag-Sintering	Pressureless Resin-Reinforced Hybrid-Ag
Storage Conditions	~ 10^{o}C	−40^{o}C	Room Temperature	−40^{o}C
Pre-Conditioning	Thawing	Thawing	Thawing	Thawing
Pre-Drying Temperature	130^{o}C	80^{o}C	N/A	N/A
Pre-Drying Time	5 minutes	30 minutes	N/A	N/A
Sintering Pressure	20MPa	10MPa	N/A	N/A
Sintering Temperature	250^{o}C	250^{o}C	90^{o}C & 250^{o}C	200^{o}C
Sintering Time	5 minutes	5 minutes	10 minutes & 45 minutes	90 minutes
Sintering Atmosphere	N_2 (or) Forming gas	N_2 (or) Forming gas	N_2 (or) Forming gas	N_2 (or) Forming gas

(time, temperature, and pressure), process conditions (staging time, sintering method - convective or conductive, and ambient environment), and paste shelf life [16–21].

Recently, hybrid silver materials gained increasing attention for their ability to sinter at even lower temperatures (≤200°C) and their relatively lower modulus [22–25]. Several studies characterized silver sintering materials' viscoplastic behavior and creep response [26–29]. However, there is a notable gap in understanding the impact of different silver sintering materials and their processing conditions on the long-term reliability of functional electronic packages. This study addresses this gap by systematically evaluating packages with four distinct silver sintering materials (see Table 4.1), varying in material composition (pure-Ag and resin-reinforced hybrid-Ag) and sintering process (pressure-assisted and pressureless). Accordingly, the package performance was evaluated based on the following methods:

1. Changes in electrical on-state resistance R_{DSon} and transient thermal impedance $Z_{th}(t = 0.1s)$ monitored during thermal cycling. R_{DSon} was measured intermittently using 4-point Kelvin contacts between the MOSFET source and drain (leadframe), while $Z_{th}(t = 0.1s)$ was measured online by applying a brief localized transient heat pulse.

2. Degradation of packages imaged intermittently during thermal cycling using Acoustic Microscopy.

3. Cross-sectional inspection of the die-attach interface after 1000 thermal cycles.

Understanding the package performance degradation necessitates monitoring strategies to create better awareness of the component's health [30–32]. Monitoring the device R_{DSon} and $Z_{th}(t)$ facilitates informed decisions regarding de-rating and preemptive maintenance. The subsequent section covers the package assembly processes, with a concise overview of the experimental setup and monitoring parameters. The results are further presented with a brief discussion.

3.2. EXPERIMENTAL METHODS

3.2.1. SAMPLE PREPARATION

Silicon-based N-channel enhancement mode Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) of 4.5mm × 5.5mm were used as a test vehicle. These MOSFETs are 170μm thick and are commercially utilized in high-performance automotive systems. Silver sintering pastes specifically formulated for assemblies of large die on silver finish substrates were chosen in this study. The pastes' material type, storage, and processing conditions are provided in Table 4.1. The fundamental differences between all four material types are as follows:

- **Material-A** contains >80% Ag particles dispersed in a solvent, with an average particle size of ~100nm. During sintering at 250°C and 20MPa, the organics evaporate, resulting in a dense Ag-sintered interface (<10% porous) with a modulus expected to be closer to bulk Ag. [33] correlates elastic modulus with sintered-Ag density.

- **Material-B** contains ~ 75 – 90% of Ag content with organic solvents. Upon sintering at 250°C and 10MPa pressure, the sintered interface is relatively dense with modulus expected to be lower than Material-A.
- **Material-C** contains a high Ag concentration of ~ 90 – 95%. Despite the pressure-less sintering process at 250°C, this material is expected to form a dense sintered interconnect with a relatively high elastic modulus due to rich Ag content.
- **Material-D** is a hybrid-Ag sintering technology with ~ 80 – 90% of Ag, ~ 1 – 10% of resin to reinforce the porous interface, < 5% additives, and ~ 5 – 10% of high-boiling solvent. This hybrid-Ag material has a relatively lower modulus (~17GPa).

It is important to be aware that the material composition mentioned above is in weight percentages. Also, the compounds and the expected modulus mentioned are based on the material datasheet.

In this study, the MOSFETs were assembled into a Power Quad Flat No-Lead (PQFN) surface mount, non-hermetically sealed package. The substrate is made of copper with Ag-metallization. The backside of the silicon MOSFETs was metalized with Ag to promote adhesion and reduce intermetallics. The silver pastes were pre-conditioned (thawed)

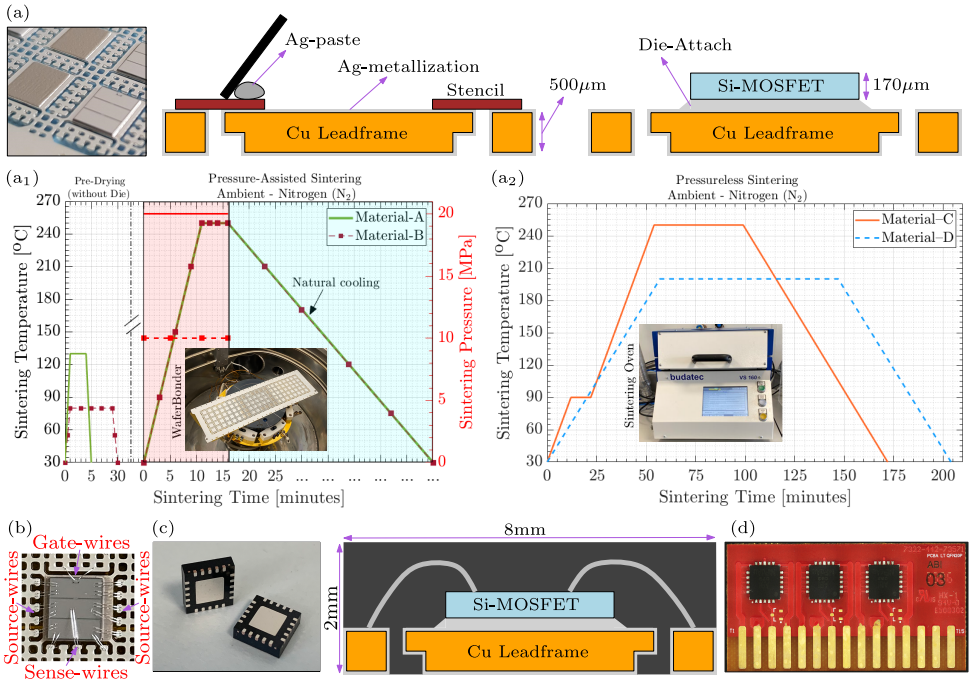


Figure 3.1: (a) Stencil printing and sintering of the die to the leadframe; (a_1) Pressure-assisted sintering process; (a_2) Pressureless sintering process; (b) Electrical connections through wire bonds; (c) Encapsulated, singulated, and laser marked PQFN packages; (d) Packages soldered to test boards.

to achieve consistency upon printing. Figure 3.1 provides an overview of the package assembly processes.

- The silver pastes were stencil-printed over the die-pad of the leadframe. The MOSFETs were subsequently placed using a force-controlled die-bonder and sintered according to the prescribed process conditions in Table 4.1. A schematic representation of the printed Ag-paste and sintered die is shown in figure 3.1a.
  - The pressure-assisted sintering process was carried out using a wafer bonder with minor adjustments for pressure-sintering. The printed wet-paste first underwent a pre-drying stage (without die) according to the process parameters specified in Table 4.1. Uniform pressure is applied over the leadframe under Nitrogen (N_2) ambient (see Figure 3.1a$_1$).
  - The pressureless process was carried out using an industrial hot plate sintering oven under Nitrogen (N_2) ambient (see Figure 3.1a$_2$).
  - The prescribed process conditions for both pressure-assisted and pressureless sintering were chosen from prior experimental analysis. It is important to be aware that the pressure sintering process adapted using a wafer bonder may not adequately represent the commercial pressure sintering tools, which are preheated to the sintering temperature.
- Upon sintering, the assembled devices were wire-bonded with 25μm thick Aluminum wires. All electrical connections are made of 4-point kelvin contacts between the MOSFET source and the drain (die-pad) terminals (see Figure 3.1b). The gate terminal is connected separately. Four-point probe configuration enables precise monitoring of the device's on-state resistance (R_{DSon}).
- The samples are further encapsulated using a commercial epoxy molding compound at 175^{o}C. The molded samples are then singulated into separate PQFN packages and laser-marked for unique identification. A schematic of the packaged device is shown in Figure 3.1c.
- Individual PQFN packages are further soldered using SAC305 onto a specially designed test board, which accommodates three packages with separate source and sense wires for four-point connections (see Figure 3.1d).

3.2.2. MEASUREMENT SETUP

A dedicated measurement setup was developed for monitoring the package performance during thermal cycling tests, as shown in figure 3.2. The test setup contains sockets for mounting test boards inside a Thermo-Mechanical Cycling Lifetime (TMCL) oven with electrical connections extending from the test socket to the sourcing and measuring equipment via a multiplexer (switch matrix). The multiplexer enables sequential measurements of multiple devices during testing conditions with a maximum switching current of 1A (hot switching). A dual-channel Source Measurement Unit (SMU) was used for sourcing drain current (I_D) and applying gate-source voltage (V_{GS}). A Digital MultiMeter (DMM) was used for measuring the voltage across the drain-source terminals (V_{DS}). The polarity was reversed while measuring the body diode of the device.

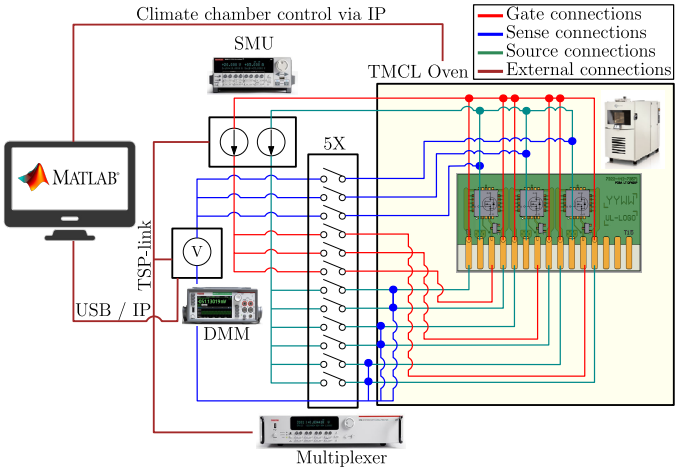


Figure 3.2: Schematic illustration of the experimental setup with different connections color-coded.

3.2.3. MEASUREMENT CONDITIONS AND MONITORING PARAMETERS

The lifetime reliability of Power QFN packages with diverse sintering materials was evaluated under thermal cycling conditions. The cycling temperature ranged from −55 to 150°C according to the stress test qualification for automotive discrete devices outlined in AECQ101 testing guidelines. The JESD22-A104 thermal cycling standards were adapted with an additional measurement step at 25°C during every cycle for online monitoring. The experimental temperature cycling profile used in this study is depicted in Figure 3.3a.

Two monitoring parameters were chosen to evaluate the package performance over cycling;

1. Electrical on-state resistance R_{DSon} under forward bias, and
2. Transient thermal impedance $Z_{th}(t)$ under reverse bias.

Similar studies on reliability investigation based on electrical and thermal measurements were previously assessed under power cycling conditions [34, 35]. The MOSFET typically exhibits on-state resistance (R_{DSon}) in the range of a few milli-ohms at room temperature (~ 25°C), and the measuring equipment has a resolution of 0.1μV for voltages up to 1V. The R_{DSon} was measured using 4-point kelvin contacts, applying 10V over the gate terminal and 1A drain current over the drain-source terminals. No visible self-heating effects were observed over five seconds, and an average on-state resistance (R_{DSon}-Avg) was determined (see Figure 3.3b). The R_{DSon}-Avg parameter denotes the resistance across the die (R_{Die}), the die-attach (R_{DA}), the leadframe (R_{LF}), the solder joint interface (R_S), and other contact resistances (R_C). The wire bond resistances (R_{Wire}) can be ignored due to four-point kelvin contacts between source and drain terminals.

$$R_{DSon}\text{-Avg} \approx R_{Die} + R_{DA} + R_{LF} + R_S + R_C \tag{3.1}$$

Since the four-point measurements eliminate the influence of resistances from wire bonds and other PCB materials, the changes in the measured R_{DSon} must reflect alterations within the packaging components.

Measuring the transient thermal impedance $Z_{th}(t)$ of a package involves localized heating and measuring the device temperature. The Si-MOSFET's intrinsic body diode exhibits a linear temperature sensitivity of ~2.26mV/^{o}C across the thermal cycling range (see figure 3.3c) With 0V applied over the gate terminal, the transistor channel remains closed, allowing source current ($I_S = -I_D$) to flow through the body diode. No changes in V_{SD} were observed upon applying negative gate-source voltages ($-V_{GS}$). Varying the source current I_S allows localized heating and estimating the junction temperature.

Traditional thermal characterization methods outlined in MIL-STD-883E and JESD51-14 to determine the Junction-to-Case thermal resistance $Z_{th(j\text{-}c)}(t)$ are not suitable for online monitoring during thermal cycling. The MIL-STD-883E method requires steady-state temperature measurement over the junction and the case, while the JESD51-14 relies on relative comparison measurement with and without thermal interface material. Besides, the JESD51-14 assumes a one-dimensional heat flow, thereby requiring a water-cooled heat sink to limit lateral heat spreading, which is not feasible for integration with thermal cycling experiments. Hence, the transient thermal impedance $Z_{th}(t)$ was determined based on a transient pulse (see figure 3.3d). The $Z_{th}(t = 0.1s)$ is not the same as $Z_{th(j\text{-}c)}(t)$. A detailed explanation of extracting $Z_{th}(t)$ from a transient pulse is provided

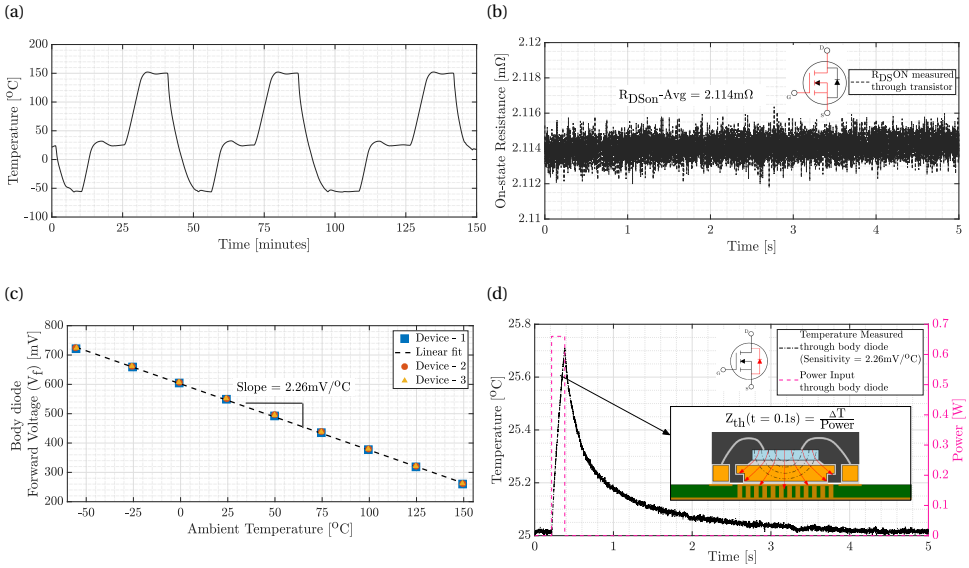


Figure 3.3: (a) Thermal cycling profile. (b) R_{DSon} measured over five seconds with V_{GS} of 10V and I_D of 1A. (c) $Z_{th}(t)$ determined based on localized heating through the body diode (V_{GS} = 0V & $-I_D = I_S$ = 1A). The heat flow path within 0.1 seconds of heating is schematically illustrated.

in [30], and a review of measurement methods for thermal resistance extraction based on TSEP is provided in [36].

A brief localized heat pulse was applied to cause local temperature changes without deviating from the oven's ambient condition. Our previous work [30] determined a heating transit window of 0.1 seconds using a 1D time-domain structure-function. The system's thermal behavior can also be modeled in the frequency domain as explained in [37, 38]. In [39], a multi-dimensional approach was introduced for determining structure-function, considering heat transfer in all directions. In this study, the transient heat pulse of 0.1 seconds was chosen based on our previous work. The 0.1-second heating defines a thermal resistance boundary within the package, excluding the influence of PCB materials on the measured $Z_{th}(t)$ (see figure 3.3d). The solder joint interface was assumed to remain relatively stable during TMCL due to matching CTE between the leadframe and solderable top surface of the test board. Besides, the $Z_{th}(t)$ was determined during the heating phase; Estimating $Z_{th}(t)$ upon cooling down (after 0.1s of heating) might be less sensitive since the device does not reach a steady state within 0.1 seconds of heating. However, the heat generated is spread across the device, and the temperature changes are averaged. Therefore, $Z_{th}(t)$ may not be influenced by localized failures originating within a small regime until sufficiently large failures occur.

Based on the aforementioned methods, the package performance was monitored as follows:

1. The electrical R_{DSon}-Avg parameter was statistically evaluated by measuring multiple samples for each material type at specific thermal cycling intervals; 0, 100, 200, 500, and 1000 cycles, all at room temperature (~ 25°C).

2. The thermal impedance $Z_{th}(t = 0.1s)$ parameter was monitored online by measuring one sample per material type at 25°C during thermal cycling.

Additionally, the online monitored samples were intermittently examined with CSAM imaging at 0, 100, 200, 500, and 1000 cycles to identify degradation evolution and further cross-sectioned after 1000 cycles to validate the die-attach degradation. The experimental findings are discussed in the subsequent section.

3.3. EXPERIMENTAL RESULTS

3.3.1. PROGNOSTIC MONITORING BASED ON ELECTRICAL MEASUREMENTS

The changes in electrical R_{DSon}-Avg over TMCL were statistically analyzed using standard deviation to assess the die-attach material reliability under thermo-mechanical stresses. Standard deviation helps identify the dataset's inherent variability, based on the dispersion of measurements around their mean value and outliers. Outliers signify sudden failures or significant deviations during TMCL. The measurements were also analyzed using Weibull probability distribution. Weibull analysis helps to understand the predictable pattern in R_{DSon}-Avg over TMCL, which is crucial for assessing material reliability. It is important to note that outliers were excluded when determining the Weibull probability distribution to prevent skewing of regression lines. Eleven packages were tested for Materials A,

ten packages for Material- B, and nine packages for Materials C and D. The arithmetic mean and standard deviation of R_{DSon}-Avg was calculated for each material type and plotted along with identified outliers in figure 3.4. A 20% deviation in R_{DSon}-Avg from the reference 0 cycle Mean was considered a failure criterion. Furthermore, the Weibull probability distributions were determined for each thermal cycling interval and plotted with linear regression lines to assess whether the R_{DSon}-Avg changes conformed to the expected Weibull distribution behavior. The following conclusions can be drawn based on the results presented graphically in figure 3.4:

- Packages with **Material-A (pressure-assisted Ag-sintering with 20MPa at 250°C)** exhibited no outliers and a steady increase in mean R_{DSon}-Avg with 6% deviation over 1000 cycles (see figure 3.4a). Although the probability distribution seems to broaden over cycling, most measurements stayed around the expected Weibull behavior, with sufficient margin from the threshold, suggesting good material reliability and a predictable pattern.

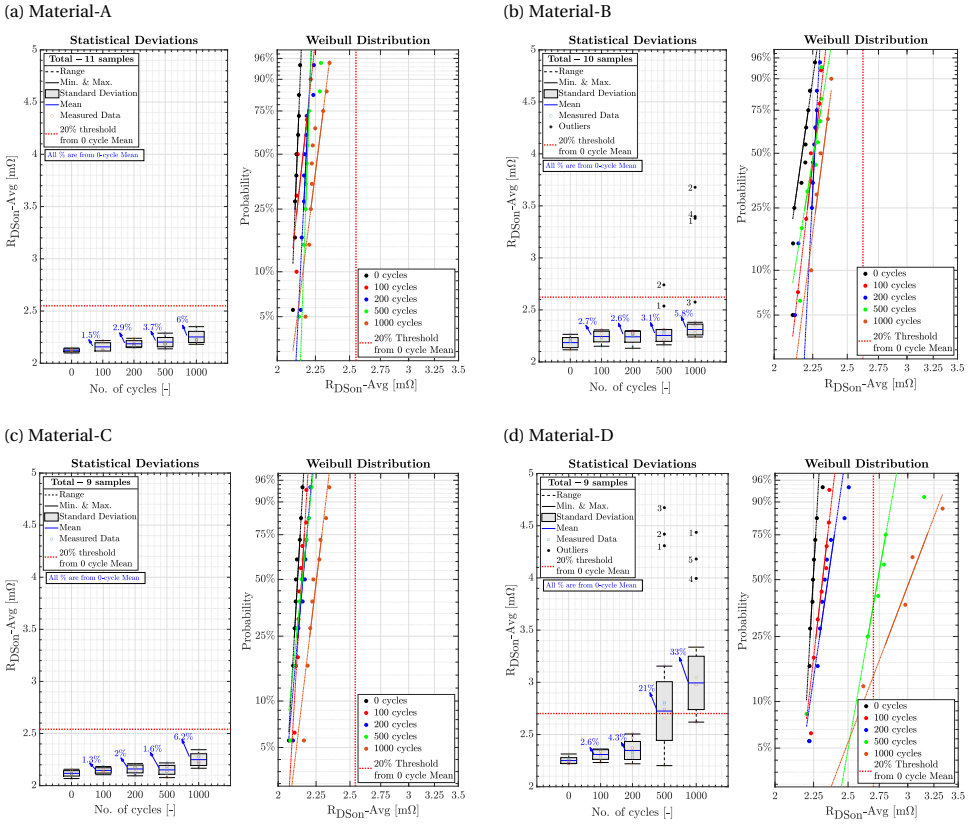


Figure 3.4: Thermo-mechanical reliability of packages with different die-attach materials evaluated based on electrical measurements at room temperature (~ 25°C). A 20% deviation from the 0 cycle mean was considered a failure criterion. Outliers were excluded when determining the Weibull probability distribution.

- Packages with **Material-B (pressure-assisted Ag-sintering with 10MPa at 250°C)** displayed a wider spread in R_{DSon}-Avg and a broader distribution of probabilities compared to Material-A (see figure 3.4b). Additionally, four outliers were observed after 500 cycles. Excluding these outliers, the remaining samples indicate <6% change in mean R_{DSon}-Avg and align closer to the Weibull prediction. However, Material-B might be less reliable than Material-A due to higher variability and outliers.

- Packages with **Material-C (pressureless Ag-sintering at 250°C)** demonstrated consistent performance without any outliers similar to Material-A (see figure 3.4c). The packages demonstrated less than 2% deviation up to 500 cycles, followed by a steep increase (6.2% deviation) after 1000 cycles. The Weibull analysis indicates a similar trend, and the probability distribution centered closer to the prediction. The results suggest that Material-C exhibits good reliability with predictable behavior but may experience degradation after extended thermal cycling.

- Packages with **Material-D (pressureless resin reinforced hybrid-Ag at 200°C)** indicated the highest initial mean R_{DSon}-Avg (at 0 cycles) among all materials. They also drifted 21% in mean R_{DSon}-Avg, surpassing the threshold within 500 cycles, which further escalates to 33% after 1000 cycles. Out of nine tested samples, five samples were identified as outliers, with two samples exceeding 5mΩ resistance (see figure 3.4d). Excluding these outliers, the remaining samples conformed to the linear regression line with a broader distribution range. Material-D indicates poor reliability due to an increase in resistance and increasing outliers.

In summary, Material-A and Material-C demonstrated consistent performance with minimal increase in R_{DSon}, without any outliers, and good alignment with the Weibull distribution. Material-B indicated acceptable performance within limits but had increasing outliers, and its Weibull suggested higher variability compared to Materials A and C. Material-D displayed reliability concerns, exceeding the threshold criterion and a substantial shift in Weibull distribution. These results suggest that packages with Material-A and Material-C perform relatively better under thermal cycling conditions compared to Material-B and Material-D. To further differentiate the degradation behavior observed between all four die-attach materials, the transient thermal impedance based on a transient pulse, $Z_{th}(t = 0.1s)$, was monitored online, and the results are presented subsequently.

3.3.2. PROGNOSTIC MONITORING BASED ON THERMAL MEASUREMENTS

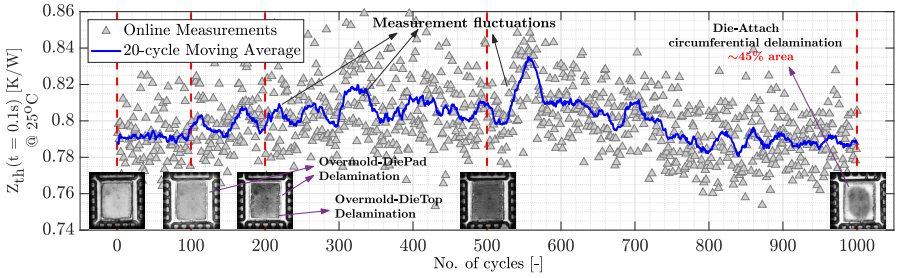
Material degradation is inevitable due to continuous thermal cycling conditions, causing reliability issues like die-attach delamination or fractures that impede heat dissipation and thermal performance. To monitor the die-attach material degradation, the transient thermal impedance $Z_{th}(t = 0.1s)$ was measured online during the thermal cycling test (see figure 3.5). To visually distinguish long-term trends from measurement fluctuations, simple moving averages (SMAs) over a fixed observation window (20 cycles) were determined and superimposed on the real-time measurement data in figure 3.5. The 20-cycle moving averages illustrate the measurement fluctuations and the overall degradation trend.

The thermal measurement results were further correlated with CSAM images from 0, 100, 200, 500, and 1000 thermal cycles. CSAM inspection identified two distinct failure modes (see figure 3.5): (i.) Delamination of epoxy molding compound and (ii.) Delamination at the die-attach interface. Since the dominant heat flow path is through the die and die-attach, overmold delamination might not directly affect thermal measurements. However, it can strain bond wires and impact electrical resistance shown in Figure 3.4, potentially explaining outliers in Material B and D. Overmold delamination poses additional risks due to moisture ingress and package instability, potentially leading to long-term performance degradation.

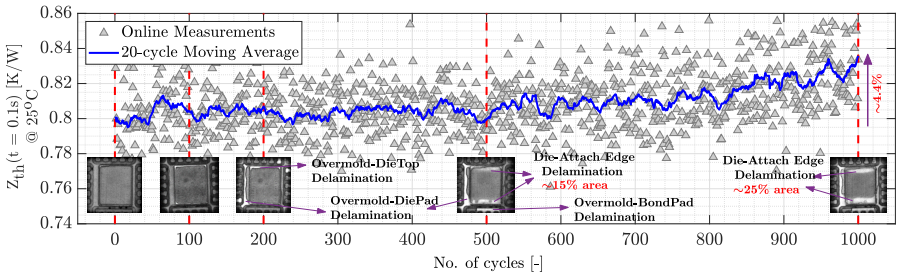
This study focuses on the die-attach interface, which acts as a thermal transfer medium between the die and the package substrate. Delamination or failure of the die-attach layer might significantly affect the package's thermal performance. The die-attach material, sandwiched between the silicon die and the copper substrate endures thermo-mechanical stresses, particularly shearing forces acting from the edges towards the center of the die. An estimate of the die-attach interface delamination from the outer edges is shown in figure 3.5. The following observations can be made by comparing the thermal measurements with CSAM images:

- The package with **Material-A (pressure-assisted Ag-sintering with 20MPa at 250^{o}C)** exhibits a fluctuating $Z_{th}(t = 0.1s)$ (see Figure 3.5a). These fluctuations likely originate from the degradation of packaging material. CSAM analysis reveals ~45% die-attach interface delamination along the circumference, but marginal changes are observed in the measurements. This suggests that die-attach degradation along the outer edges has minimal impact on package thermal performance, possibly due to heat dissipation through the bonded area at the center.
- The package with **Material-B (pressure-assisted Ag-sintering with 10MPa at 250^{o}C)** exhibits stable heat transfer up to ~500 thermal cycles and the $Z_{th}(t)$ increases moderately by ~4.4% over 1000 cycles (see Figure 3.5b). CSAM analysis shows ~15% edge delamination at 500 cycles, escalating to ~25% after 1000 cycles. CSAM images correlated with thermal measurements suggest that the dominant heat transfer path remains through the die-attach center despite edge delaminations.
- The package with **Material-C (pressureless Ag-sintering at 250^{o}C)** exhibits a relatively lower initial $Z_{th}(t)$ at 0 cycles compared to other materials, although the differences are marginal (see Figure 3.5c). Material-C displays stable thermal performance over 1000 cycles with minimal fluctuations, highlighting the material's resilience, and ~20% edge delamination highlights the dominant heat dissipation through the center.
- The package with **Material-D (pressureless resin reinforced hybrid-Ag sintering at 200^{o}C)** exhibits the highest initial $Z_{th}(t)$ at 0 cycles with a fluctuating trend. Furthermore, Material-D shows thermal degradation, with a notable ~38% increase in $Z_{th}(t)$ between 500 and 1000 cycles (see Figure 3.5d). CSAM inspection supports these findings, revealing ~32% delamination along the circumference at 500 cycles, which escalates to ~67% extending towards the center after 1000 cycles. This

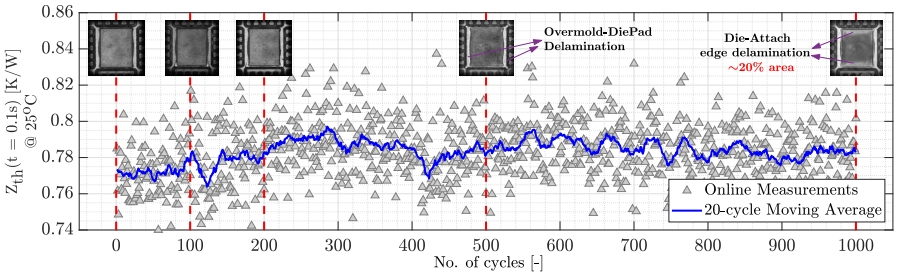
(a) Material-A



(b) Material-B



(c) Material-C



(d) Material-D

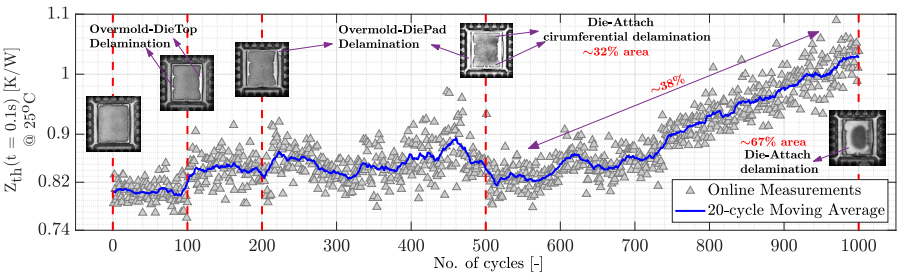


Figure 3.5: Thermo-mechanical reliability of packages with different die-attach materials evaluated based on thermal measurements. The $Z_{th}(t = 0.1s)$ was measured at 25°C during every thermal cycling step. Likewise, the samples were imaged using CSAM at intervals of 0, 100, 200, 500, and 1000 cycles.

extensive delamination explains the increase in thermal impedance observed for Material-D.

All four packages were further cross-sectioned after 1000 thermal cycles and imaged using an Electron Microscope (see Figure 3.6). Packages with pure-Ag sintering paste (Material A, B, and C) exhibit relatively dense sintered layers compared to the resin-filled porous interface (Material-D). Likewise, pressure-assisted sintering (Material A and B) favors dense sintered interconnects, with Material-A exhibiting a visibly denser interface than Material-B due to increased pressure. Notably, the pressureless pure-Ag material sintered at 250^{o}C (Material-C) exhibits a comparatively dense sintered interconnect despite pressureless processes.

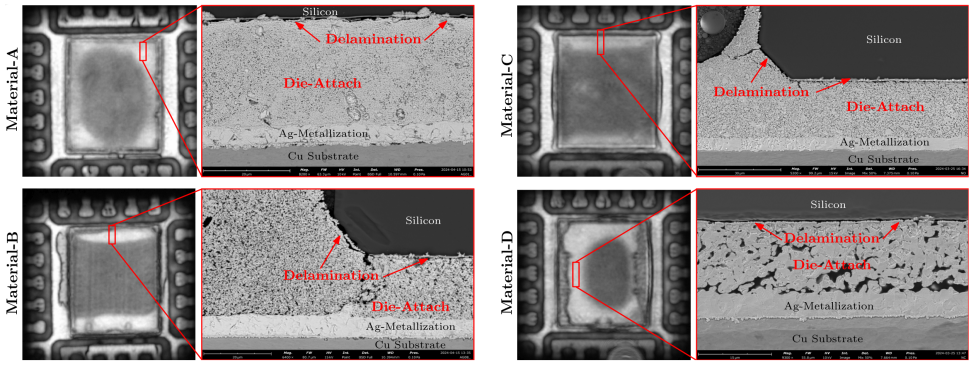


Figure 3.6: Cross-sectional inspection of online monitored samples after 1000 cycles. The samples were polished to a desired depth, and the polished surface was milled using Broad Ion Beam (BIB).

However, all four materials experienced failure closer to the die-backside metallization layer, and the severity varies across materials, with Material-D exhibiting the most deviation. The failure regions observed from the cross-sectional inspection coincide with CSAM images. Though the precise mechanism underlying the accelerated degradation of Material D is not known, it is evident that the resin-reinforced material suffers from thermo-mechanical fatigue despite lower elastic modulus. Further investigations are recommended for all four materials to understand the correlation between the material microstructure and its thermo-mechanical performance.

In summary, the thermal measurement results, CSAM images, and cross-sectional inspection are in agreement with electrical measurement results, despite the potential influence of overmold delamination on the measured electrical R_{DSon}.

3.3.3. DISCUSSION

The impact of die-attach material selection and their processing techniques on the thermo-mechanical reliability of electronic packages was investigated in this study. The experimental findings indicate a correlation between the thermo-mechanical reliability of the die-attach interface and the sintered interface material density. A dense sintered

interconnect seems more resilient to thermo-mechanical stresses shearing from the outer edges to the center. However, further investigations are required to validate the correlation. Besides, the experimental results offer additional valuable insights:

- **Pressureless Silver Sintering:**
  - Pressureless Ag-sintering demonstrated consistent electrical and thermal performance, with a relatively dense interface comparable to pressure-assisted sintering. This contradicts the assumption that pressure is typically required to achieve a dense sintered layer.
  - From a manufacturability standpoint, pressureless Ag-sintering can be advantageous by simplifying the assembly process (eliminating the need for pressure) and potentially reducing costs.
  - Pressureless Ag-sintering is a promising approach for Pb-free die-attach applications. However, not all pressureless Ag-sintering materials might exhibit similar performance. Further investigations are recommended to characterize the relationship between the material microstructure and its thermo-mechanical performance.
- **Resin-Reinforced Hybrid-Silver Sintering Material:**
  - Despite resin-reinforced hybrid-Ag paste having a relatively lower modulus, they displayed degradation in this study with ~33% drift in R_{DSon}, ~38% increase in $Z_{th}(t)$, and ~67% interface delamination over 1000 cycles.
  - However, it is important to acknowledge that the chemical compounds used in this material are proprietary to the material supplier, and they might vary among different suppliers. Hence, further investigations are required to understand and optimize this material.
- **Die-Attach Prognostic Monitoring:**
  - While measuring R_{DSon} and $Z_{th}(t)$ are representative parameters for monitoring the package performance signifying die-attach materials, there are limitations.
  - Despite 4-point Kelvin contacts, the electrical measurements might be influenced by external factors (non-uniform current spreading, gate leakage, and solder-joint degradation). Similarly, $Z_{th}(t)$ can be impacted by temperature gradients within the package.
  - Future studies can explore specialized test structures to isolate the die-attach interface contribution from the R_{DSon} measurements. Likewise, $Z_{th}(t)$ based on variable transit time, analyzing under frequency domain [37, 38], and incorporating multi-dimensional approach [39] can further improve the measurements.

3.4. CONCLUSION

In this study, the thermo-mechanical reliability of Power QFN packages was investigated with four distinct Ag-sintering materials:

- **(A & B)** Pressure-assisted Ag 20MPa and 10MPa at 250^{o}C,
- **(C)** Pressureless Ag at 250^{o}C, and
- **(D)** Pressureless resin-reinforced hybrid-Ag at 200^{o}C.

The lifetime reliability of these die-attach materials was assessed under thermal cycling conditions by monitoring the drift in electrical on-state resistance R_{DSon}, and changes in transient thermal impedance $Z_{th}(t = 0.1s)$. The measurement results were further validated with CSAM imaging and cross-sectional inspection.

The pressureless Ag-sintered (Material-C) demonstrated consistent electrical and thermal performance with sintered interconnect density comparable to pressure-assisted sintering materials. Whereas the pressureless resin-reinforced hybrid-Ag sintered at a lower temperature (Material-D) indicated reliability concerns with ~33% increase in R_{DSon}, ~38% in $Z_{th}(t = 0.1s)$, and ~67% delamination over 1000 thermal cycles. The experimental findings suggest a correlation between the die-attach material density and their thermo-mechanical reliability, which requires further experimental verification.

This comprehensive study underscores the importance of die-attach material selection and recommends careful consideration of thermo-mechanical properties during package design. Furthermore, such efforts in implementing prognostic monitoring strategies are crucial in understanding performance degradation to create better awareness, make informed decisions, and schedule preemptive maintenance.

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4

Reliability Evaluation of Hybrid-Silver Sintered Materials

Emerging trends like 6G Telecom and Electric Vehicles (EVs) are driving advancements in semiconductor packaging, specifically in back-end assembly. These enabling technologies are focused on achieving higher functionality, improved connectivity at higher frequencies, smaller form factors, efficient heat dissipation, and reduced power consumption. Wide-Band Gap semiconductors' instrumental role in enabling high-frequency RF transmissions and efficient power switching necessitates advancements in thermal dissipation and the ability to withstand higher thermo-mechanical stresses in next-generation power devices. Concurrently, the semiconductor industry has been seeking a lead (Pb) solder replacement with improved automotive reliability for over two decades. The lead-free alternatives must be compatible with larger die sizes on metal lead frames and must align with the high productivity demands of semiconductor back-end processing. However, finding a suitable, drop-in lead-free solution to address these challenges has proven to be highly challenging. This chapter describes the ongoing product development and comprehensive testing of a new hybrid silver sintering die-attach development with stress-absorbing additives specifically designed for large die on lead frame based applications. This development work has resulted from the dire need to meet the industry's evolving trends and requirements towards higher power and sustainable products.

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4.1. INTRODUCTION

GIVEN the complex challenges encountered during the package assembly processes and the imperative to fulfill application-specific requirements, it is vital to assess the compatibility of individual components, processes, and materials [1–3]. Therefore, this study specifically emphasizes evaluating the die-attach layer, encompassing the assembly process and its impact on the reliability of the end product.

Choosing an appropriate die-attach material plays a critical role in package assembly. A review of die-attach materials for high-temperature applications can be found in [4–6]. Previously, high-lead (Pb)-based solders were mostly preferred due to their high melting point and relatively low stiffness. However, concerns regarding lead toxicity have led to restrictions on their usage. This has resulted in market demand for lead-free die-attach materials that offer superior thermal properties and improved thermo-mechanical stability. Addressing the challenge of reducing thermo-mechanical stresses between a large die with a coefficient of thermal expansion (CTE) of ~3ppm/^{o}C and copper lead frames (~17ppm/^{o}C) require a multi-disciplinary approach, encompassing thermal, electrical, mechanical, and material science domains. Due to their low melting point, traditional lead-free solders are not viable alternatives for semiconductor die-attach. The reliability of lead-free solders with high-melting temperatures for harsh environmental applications has been the subject of comprehensive studies on its own [7].

Sintering technology presents a promising solution that offers several advantages compared to traditional solders. The sintering process involves the fusion of metal (micro/nano) particle precursors in paste form under heat and, optionally, pressure. One of the main benefits of sintering is its ability to sinter at relatively low temperatures, typically between 200–300^{o}C, and achieving the high-melting-point characteristics of a bulk metal after sintering. Sintered joints exhibit improved thermal stability and enhanced thermal performance, making them highly suitable for high-temperature and high-power applications. However, the success of sintering heavily relies on the sintering paste chemistry and precise processing conditions. In electronic packaging, sintering materials typically contain silver or copper base metals. Copper is favored in terms of process compatibility, but sintering remains challenging due to the reactivity and sensitivity of copper precursors (risk of Cu oxidation/corrosion). As a result, silver sintering has emerged as the most promising and reliable lead-free die-attach solution [8–15].

Pressure-less silver sintering materials provide an excellent basis for improving thermal and electrical performance and thermo-mechanical reliability compared to solders. Furthermore, from a practical point of view, pressure-less silver sintering is expected to enable increased production output as compared to solders and pressure-assisted sintering. However, a significant challenge with pure solvent-based silver sintering (pressure-less) materials is their inherent porosity, which leads to microscopic stress concentrations within the die-attach material and allows moisture ingress. This, in turn, reduces the Moisture Sensitivity Level (MSL) of the finished component and increases its brittleness compared to bulk silver material. To address these concerns, an effective approach has been incorporating an organic resin phase into the sintered joint, called 'hybrid silver

sintering.' This method minimizes porosity through filling and sealing, improving the sintered bulk material's overall flexibility and toughness. As a result, the thermo-mechanical performance of the sintered die-attach joint during stressful Moisture Sensitivity Level (MSL) and Thermo-Mechanical Cycling Lifetime (TMCL) reliability testing is enhanced. However, it should be noted that pressure-less hybrid silver sintering materials often exhibit lower thermal performance as compared to pure silver or pressure-assisted silver, which was previously investigated on similar silver sintering materials with metal-organic and resin-reinforced technology [16–18].

This study investigated a new class of experimental 'stress absorbing' hybrid silver sintering die-attach materials ('EXP3' and 'EXP5') with ~150–200 W/m-K effective bulk thermal conductivity. The fundamental difference between these two new die-attach materials is that EXP5 has a higher bulk sintering density and, consequently, higher modulus than EXP3. These materials were developed to pass severe Automotive Electronics Council (AEC) Q100 and Q101 (respectively for Integrated Circuits and Discretes) reliability test requirements (up to 2000 thermal cycles -55^{o}C/$+150^{o}$C for highest Grade 0). This is achieved by optimizing the silver paste formulation with special filler packages and stress-absorbing additives to increase the bulk sintering network and interfacial sintering to die and lead frame, next to improving MSL and thermal cycling performance. The thermo-mechanical reliability of these stress-absorbing hybrid silver sintering materials was benchmarked against a commercially available hybrid silver sintering material ('8068TI') with ~165 W/m-K bulk conductivity without the stress-absorbing feature [19] (for reference, LOCTITE® ABLESTIK ABP 8068TI is successfully released in automotive power semiconductors with die sizes up to ~3×3mm, but facing thermal cycling limitations on a copper lead frame with larger die sizes).

This work focuses on examining the package assembly process and thermo-mechanical reliability testing. The following section provides a detailed description of the various steps involved in the test package assembly. The subsequent section discusses the hot die-shear strength experiments and the experimental findings from the Thermo-Mechanical Cycling Lifetime (TMCL) testing. This section includes the functional device's electrical measurement (changes in electrical resistance R_{DS}(on)) during thermal cycling for the new class of hybrid silver sintering die-attach materials with stress-absorbing technology versus commercially available reference material. This paper concludes with remarks on the potentially broader use of hybrid silver sintering die-attach adhesives for larger die sizes on copper-based lead frame applications.

4.2. EXPERIMENTAL METHODS

4.2.1. SAMPLE PREPARATION

Silicon-based N-channel enhancement mode Field Effect Transistor (FET) with TrenchMOS technology was chosen as a test vehicle in this study. These devices are commercially used in high-performance automotive systems with a maximum power rating of up to 333W. The MOSFETs were assembled in Power Quad Flat No-Lead (PQFN) surface mount packages as follows:

1. The package assembly process commences with the preparation of the lead frame. As depicted in Figure. 4.1a, the package substrate (lead frame) is made of fully hardened C194 copper with 500μm thickness. To enhance adhesion, the lead frame surface was plated. Two distinct lead frame finishing options were examined: (i) Nickel- Palladium-Gold (NiPdAu, also known as 'PPF') and (ii) Silver. Prior to processing, the lead frames were treated with Argon plasma to remove surface contamination.

2. Next, the commercial and experimental die-attach materials (8068TI, EXP3, EXP5) were dispensed in a snowflake pattern (Figure. 4.1b) using a Musashi Image Master 350PC Smart Dispense Robot equipped with a 25-gauge needle and applying 100–200KPa of pressure.

3. Die placement was performed on a Finetech Sigma Fineplacer equipped with a position-controlled z-axis. The Silicon MOSFETs dies with 4.5×5.5×0.17 mm dimensions and silver backside metallization (Ag BSM) were carefully picked and placed with a placement force of approximately 0.3N (Figure. 4.1c). Once the die was properly positioned, the sintering process was carried out in a Budatec VS160 vacuum oven under Nitrogen. The first step involves staging at 130^{o}C for two hours, followed by pressure-less sintering at 200^{o}C for one hour. After sintering, all samples were inspected with a confocal microscope to measure the die-warpage.

4. Electrical connections were established to the lead frame through wire bonding (Figure. 4.1d). A 4-point probe configuration was used for all terminals: Source, Gate, and Drain.

5. The final step involves transfer molding. This was performed with Sumitomo EME-G700LA epoxy molding compound at 175^{o}C. The molded devices were further laser marked, singulated, and soldered with SAC305 alloy onto a Printed Circuit Board (Figure. 4.1e). These soldered devices were further subjected to Moisture Sensitivity Level (MSL3) and TMCL tests as described in the following subsection.

In this study, six types of functional test packages (3 die-attach materials and 2 lead frame metallizations) were prepared with over 32 packages per leg. The Bond-Line Thickness (BLT) of the sintered die-attach layer was evaluated using confocal optical microscopy. The typical wet BLT after die placement was ~45–50um and the average dry (sintered) bond line thickness was ~28–37um. In addition to the functional test packages,

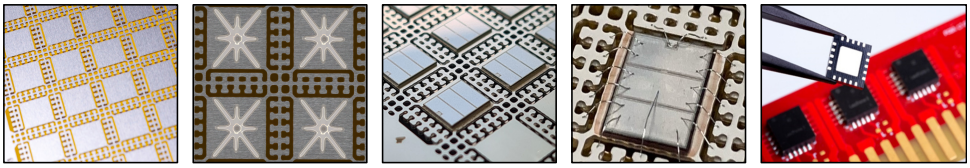

Figure 4.1: A pictorial representation of the package assembly processes is shown. The various stages of the assembly process are explained in steps (a) to (e) in section II. *A.*

a series of test samples were prepared in a similar process to evaluate the Hot Die-Shear Strength (HDSS) at typical solder reflow temperature (260°C) for both commercial and experimental die-attach materials. A dummy silicon die of 4.9×4.6×0.52mm with silver backside metallization was sintered on a 2mm copper flange with both NiPdAu and Silver metallization using the same staging and sintering profile. The die-shear experimental results were evaluated and compared to the die-warpage measurements after sintering.

4.2.2. THERMO-MECHANICAL CYCLING LIFETIME EXPERIMENTS

To assess the reliability of the PQFN test packages prepared with commercial and experimental hybrid silver sintering die-attach adhesives, Thermo-Mechanical Cycling Lifetime (TMCL) experiments were conducted. Before commencing the TMCL testing, all packages underwent the Moisture Sensitivity Level 3 (MSL3) pre-conditioning step. The MSL classification system aids in assessing the moisture sensitivity of an electronic component during storage before assembly, particularly surface mount devices (SMDs). This MSL3 step involved drying the PQFN packages at 125°C for 24 hours, followed by exposure to 60% relative humidity at 60°C for 42 hours. Subsequently, within one week, the PQFN packages were subjected to three consecutive reflow soldering cycles (260°C).

As mentioned earlier, the TMCL experiments were conducted based on the guidelines provided by AEC Q100 and Q101. These stress tests are recommended for qualifying automotive grade discrete semiconductors involving temperature cycling from −55°C (compression state) to 150°C (expansion state), as depicted in Figure. 4.2. The cycling rate was maintained at ~1–2 cycles per hour and the device's electrical performance was monitored intermittently.

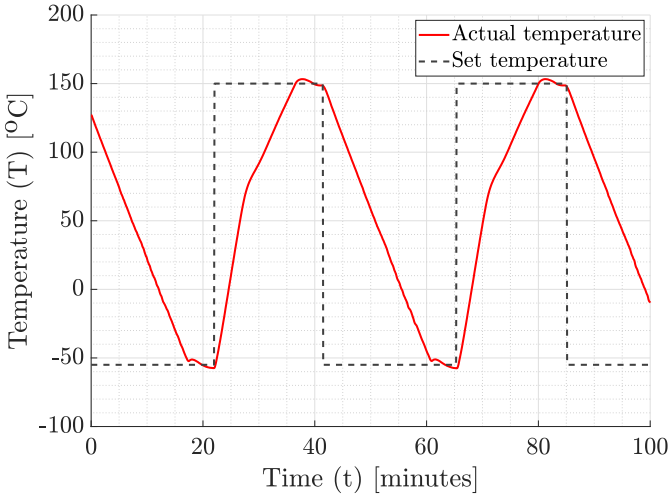

Figure 4.2: The temperature cycling profile −55°C to 150°C shown is based on the automotive AEC norms for ICs & discrete semiconductors and the JEDEC temperature cycling standards.

The on-state electrical resistance (R_{DS}(on)) of the N-channel MOSFET was measured at specific thermal cycle intervals: 0, 100, 500, 1000, 1500, and 2000 cycles. The PQFN device was operated under a forward source-drain bias with a positive gate-source voltage (V_{GS}) of 20V and a drain-current (I_D) of 2A for a duration of 5ms. The reliability of the die-attach joint was monitored effectively during thermal cycling based on intermittent electrical measurements. This was possible since the device's drain terminal is electrically connected to the package substrate through the die-attach interface. The subsequent experiment results section discusses the hot die-shear strength test results compared to the die-warpage measured after sintering and the in-package electrical measurements on the PQFN test vehicle during TMCL testing.

4.3. EXPERIMENTAL RESULTS

4.3.1. HOT DIE-SHEAR STRENGTH EXPERIMENTS

The die-shear strength of both commercial and experimental die-attach materials was evaluated at the typical lead-free reflow soldering temperature of 260°C to investigate and benchmark the adhesive and the sintering performance. The experiments were conducted using a Universal Bond Tester (Royce 650). The evaluation encompassed all three die-attach materials, 8068TI, EXP3, and EXP5, on both copper lead frame metallizations (NiPdAu and Ag). The results of the HDSS experiments are presented in Table 5.1. Both experimental hybrid silver sinter materials exhibited good adhesion/sintering on NiPdAu and Ag finish lead frames, yielding HDSS in the range of approximately 14 MPa (~1.4 kgf/mm^2 which is in line with typical application requirements). Cohesive failure modes within the sintered die-attach bond line were observed in all cases. However, for commercial 8068TI on NiPdAu metallization, a significantly lower HDSS of approximately 5 MPa was observed, with adhesive failure occurring at the NiPdAu interface. On the other hand, when 8068TI was used with the silver finish, failure occurred at the interface of the silver backside of the die with an HDSS of approximately 14 MPa (like EXP3 and EXP5).

The difference in thermal expansion CTE of the copper lead frame (~17 ppm/°C) and the silicon die (~3 ppm/°C) causes measurable warpage at room temperature af-

Table 5.1: Hot Die-Shear Strength (HDSS) of three hybrid silver sintering die-attach adhesives at 260°C on two different lead frame metallizations.

HDSS [MPa]	8068TI			EXP3			EXP5		
NiPdAu	3.2	7.1	5.4	13.8	14.7	15.6	12.8	15.2	11.8
	3.5	2.9	4.8	12.2	13.2	14.6	13.7	16.1	16.2
	Avg. 4.48 MPa			*Avg. 14.02 MPa*			*Avg. 14.3 MPa*		
Silver	15.0	17.2	17.4	11.1	15.7	13.5	15.2	11.5	13.7
	10.9	10.1	12.5	11.2	11.5	13.6	13.5	12.4	14.6
	Avg. 13.85 MPa			*Avg. 12.76 MPa*			*Avg. 13.48 MPa*		

Table 5.2: Die-warpage for all three die-attach materials onto two lead frame finishes measured after the sintering process over the two axes of the die (short and long).

Warpage	Die short side - 4.5mm			Die long side - 5.5mm		
[μm]	8068TI	EXP3	EXP5	8068TI	EXP3	EXP5
NiPdAu	*0.5*	5.8	6.6	*0*	9	9.3
Silver	*2.3*	5.2	5.5	*4.3*	8.6	10.2

ter sintering at ~200°C. This is a direct result of the residual stress within the sintered die-attach bond line after cooling down. It is driven by the stiffness, CTE, and the temperature at which sintering occurs, and the die-attach bond line solidifies (which was found experimentally to be around 150°C). Lower-than-expected warpage values are reminiscent of relaxation within the die-attach bond line layer. The die-warpage was experimentally measured using a Keyence laser confocal surface profiler. The results are tabulated in Table 5.2. In this configuration, Finite Element Method (FEM) simulations confirmed that the material properties (modulus, CTE, and thickness) of the die-attach layer have a neglectable influence on the die-warpage itself. Rather, it is fully defined by the mechanical properties of the lead frame and die.

The experimental 'stress-absorbing' hybrid silver sintering materials (EXP3 and EXP5) demonstrate a curvature of approximately 10µm along the long side of the die and around 6µm along the short side on both NiPdAu and Silver metalized lead frames. These results confirm a favorable bonding/sintering between the die and lead frame, contributing to the observed warpage of the complete stack. The die-warpage with EXP3 and EXP5 aligns within 30% of that obtained from FEM simulations. In contrast, the commercial silver sintering material (8068TI) on NiPdAu exhibits no warpage, indicating poor adhesion and delamination at the die edges. Lower-than-expected warpage was observed for 8068TI material on Silver metalized lead frames. The poor adhesion of 8068TI to NiPdAu is aligned with the Hot Die-Shear Strength (HDSS) results. Contradicting evidence was observed for 8068TI on Silver metalized lead frames. The HDSS on Silver indicates good adhesion. However, the die-warpage measurements suggests some relaxation within the 8068TI material.

In summary,

- The new 'stress-absorbing' hybrid silver sintering materials (EXP3 and EXP5) demonstrate high die-shear strength at 260°C on both NiPdAu and Silver metalized lead frames. These findings are further supported by die-warpage measurements conducted on functional devices after sintering.
- The 8068TI reference material shows lower adhesion to these specific NiPdAu finished PQFN lead frames. This was confirmed through hot die-shear strength and die-warpage measurements. 8068TI adhesion to these specific Silver metalized lead frames indicates higher HDSS values, however die-warpage measurements indicate some form of mechanical relaxation.

4.3.2. ELECTRICAL MEASUREMENTS

The electrical on-state resistance ($R_{DS}(on)$) refers to the resistance measured across the drain-source terminals of the packaged device under forward bias. It is a combination of the electrical resistances of the die (R_{Die}), die-attach (R_{DA}), lead frame (R_{LF}), and the package substrate solder joint interface (R_S). The solder joint interface is assumed to remain relatively stable during the TMCL test. This assumption is based on the matched coefficient of thermal expansion (CTE) between the copper lead frame and the copper metallic pad on the PCB substrate. Hence, changes in the electrical resistance $R_{DS}(on)$ are expected to correspond to degradation, specifically in the die-attach bond line, which is more prone to failure as compared to other materials during cyclic loading. The packaged devices were subjected to thermal cycling from -55^oC to 150^oC, and the electrical resistance ($R_{DS}(on)$) was measured intermittently at room temperature ($\sim 25^oC$). The test results are presented in Figure. 4.3.

The measurement results were analyzed based on Weibull probability distribution. Weibull probability analysis is a statistical method of analyzing and interpreting the failure data based on the Weibull distribution. It involves fitting the observed failure data to the Weibull distribution, thereby estimating the shape and scale parameters of the

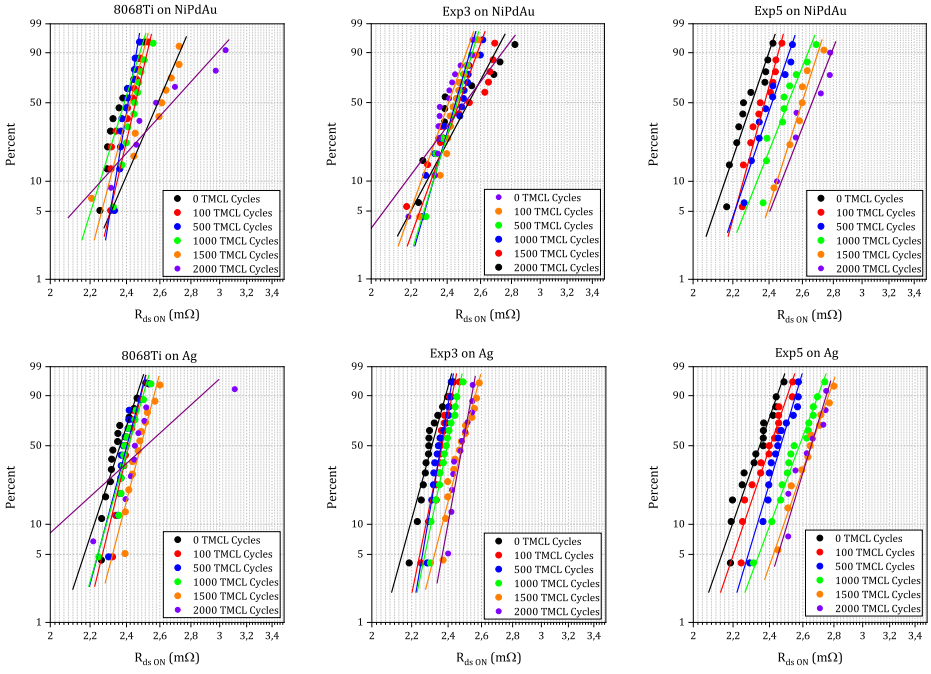

Figure 4.3: Weibull probability plots showing the electrical on-state resistance ($R_{DS}(on)$) measured on all three tested die-attach materials (8068TI, EXP3, and EXP5) on two PQFN lead frame metallizations (NiPdAu and Ag) up to 2000 thermal cycles (-55^oC to 150^oC).

distribution. The shape parameter β represents the slope of the fitted line, and the scale parameter η is related to the intercept (electrical shift or drift). Accordingly, the electrical resistance (R_{DS}(on)) of the packages measured at fixed intervals (0, 100, 500, 1000, 1500, and 2000 thermal cycles) were plotted against the percentage distribution (Figure. 4.3). For each sample variation, the data from every cycle was fitted with a straight line to determine the shape and scale parameters. The evolution of the shape β and scale η parameters over thermal cycling up to 2000 cycles can be visually observed in Figure. 4.3. From a physical context, the scale parameter (η) signifies the shift or drift in electrical performance (typically degradation by higher resistance values), where the shape parameter (β) reflects the distribution of the degraded samples after thermal cycling.

For the PQFN packages with NiPdAu finish, a noticeable drift in R_{DS}(on) is observed with increasing thermal cycles. In particular, 8068TI and EXP5 show more shifts to the right, indicating a higher degree of degradation than EXP3, leading to considerably higher electrical resistance, as depicted in Figure. 4.3. Conversely, the slope of the line decreases with increasing thermal cycling in the case of 8068TI and EXP3. This suggests that the degree of performance diverges among the samples, implying the presence of a possible stochastic degradation mechanism. In the case of the die-attach materials (8068TI, EXP3, and EXP5) on Silver (Ag) finish, a relatively limited drift in R_{DS}(on) is observed as compared to NiPdAu finish, suggesting a more gradual and slower degradation process during thermal cycling. Besides, the measurement data does not exhibit significant variations compared to the NiPdAu test samples. This indicates that the degree of degradation is relatively consistent among all samples with a Silver (Ag) finish, with EXP3 showing

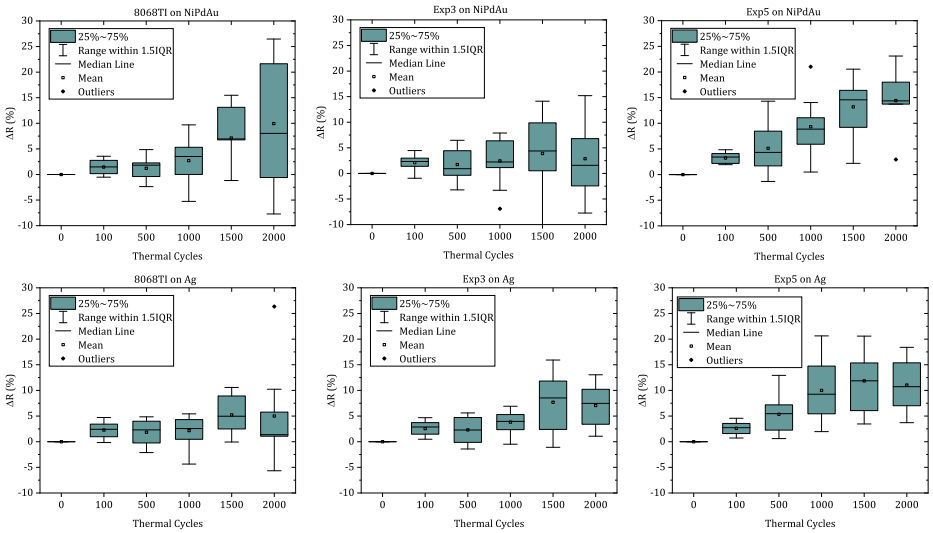

Figure 4.4: Interquartile range (IQR) plots showing the percentage change in the electrical on-state resistance (R_{DS}(on)) measured on all three tested die-attach materials (8068TI, EXP3, and EXP5) on two PQFN lead frame metallizations (NiPdAu and Ag) up to 2000 thermal cycles (-55^{o}C to 150^{o}C).

the most stable electrical performance with the lowest electrical drift after 2000 thermal cycles.

Another statistical aspect of interpreting the experimental measurements is to understand the dispersion present within the datasets. The interquartile range (IQR) is a robust statistical method used to evaluate dispersion. The IQR method summarizes data spread by focusing on the middle 50% of observations between the 25th and 75th percentiles. Based on the experimental measurement results shown in Figure. 4.3, the IQR was determined and visually represented in Figure. 4.4. These box plots illustrate the central 50% data spread, while the whiskers indicate the 1.5IQR range. Additionally, Figure. 4.4 presents the mean, median, and outliers in the measurement data, comprehensively analyzing the thermal cycling datasets' characteristics.

The IQR data as presented in Figure. 4.4 clearly indicates that all three die-attach materials (8068TI, EXP3, and EXP5), when used with both NiPdAu and Ag finish lead frames on this specific PQFN test package, exhibit a shift of less than 20% in the electrical on-state resistance over 2000 thermal cycles. Notably, the EXP3 die-attach with stress-absorbing additive stands out, demonstrating a deviation of less than 10% on both lead frame metallizations. Meeting the stringent long-term reliability requirement of less than 10% variation in electrical resistance ($R_{DS}(on)$) is of utmost importance, especially for automotive grade semiconductor packages. In this regard, EXP3 convincingly meets this criterion with both NiPdAu and Ag finish PQFN copper lead frames on relatively large die size (~4.5×5.5 mm).

In summary,

- A noticeable difference in the electrical performance during thermal cycling is observed between the 8068TI, EXP3, and EXP5 test samples on both lead frame metalization types; NiPdAu and Ag finish lead frames (Figure. 4.3 & 4.4).
- The new experimental hybrid silver sintering material EXP3, with stress-absorbing additives, exhibits the best resilience to thermo-mechanical loading. EXP3 demonstrates less than 10% deviation in $R_{DS}(on)$ over 2000 thermal cycles on both copper lead frame types (with Ag finish giving the best test results versus NiPdAu).
- Comparatively, 8068TI reference material without 'stress-absorber' performs similarly well when used with Ag finish lead frames, but shows large variety in $R_{DS}(on)$ test results on NiPdAu.
- The other new EXP5 material with 'stress-absorber' displays an $R_{DS}(on)$ drift of ~10% when used with Ag lead frames and ~15% when used on NiPdAu finish lead frames.

4.4. DISCUSSIONS AND CONCLUSIONS

This comprehensive test work on PQFN test packages with 4.5×5.5×0.17 mm die size demonstrates that all three hybrid silver sintering die-attach materials exhibit reasonably good to very good thermo-mechanical reliability performance based on electrical

measurements. It became evident that these three die-attach formulations' adhesion, sintering, and reliability performance on Ag finish is better overall than that of NiPdAu finish lead frames. Notably, the experimental hybrid silver sintering die-attach materials (EXP3 and EXP5) with 'stress absorbing technology' demonstrate improvements compared to the commercially available (8068TI) reference material without 'stress-absorber' regarding adhesion and sintering performance. The EXP3 die-attach formulation stands out in this specific PQFN test work with superior performance on both NiPdAu and Ag finish lead frames, as confirmed by hot Die-Shear experiments and automotive thermal cycling (TMCL) testing up to 2000 cycles ($-55/+150^{o}$C) with a maximum of 10% drift in R_{DS}(on). Similarly, the EXP5 die-attach formulation with higher bulk sintering density and consequently higher modulus than EXP3, shows improved adhesion in Die-Shear experiments compared to 8068TI reference material. However, the thermal cycling reliability performance of EXP5 falls somewhere between that of 8068TI and EXP3.

It is essential to mention, realize, and acknowledge that the outcome of all test work described in this study is based on the specific PQFN test package used and that the test results can be different on other test devices, such as different geometries (die size and thickness), die types (Si/SiC/GaN), backside metals (Ag/Au), lead frame finishes, surface roughness, etc. This understanding is crucial when selecting the most suitable die-attach material for specific applications, as the choice can significantly impact the overall performance and reliability of the package. For instance, for applications with a thicker lead frame and thinner die, and vice versa, EXP5 with higher bulk sintering density and higher modulus may perform better than EXP3 with lower modulus.

To summarize, the new experimental hybrid silver sintering materials with stress-absorbing features exhibit commendable die-shear strength at elevated temperatures (260^{o}C), which are further supported by die-warpage measurements. Furthermore, the comprehensive thermo-mechanical cycling test results strongly indicate that the stress-absorbing hybrid silver sintering technology offers suitable die-attach solutions with enhanced thermo-mechanical reliability for larger die sizes on copper lead frame applications. With the introduction of stress-absorbing additives, the application space of this 'next generation' of hybrid silver sintering die-attach adhesives, developed for copper-based lead frames, can be expanded from typical die sizes of ~3×3mm in the past, towards ~5×5mm and above, by qualifying the severe automotive AEC Q100 and Q101 reliability test requirements (2000 thermal cycles $-55/+150^{o}$C for highest Grade 0). Besides, this pressure-less hybrid silver sintering technology offers other benefits such as high thermal conductivity, sustainable lead-free composition, and well-established dispensing application using existing die-attach equipment and processes proven in high-volume IC and Discrete production.

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5

THERMAL CHARACTERIZATION METHODOLOGY FOR THIN BOND-LINE INTERFACES WITH HIGH CONDUCTIVE MATERIALS

Silver sintering offers a promising landscape for Pb-free die attachment in electronics packaging. However, the sintered interface properties are highly process-dependent and deviate from bulk silver properties. Conventional measurement methods do not adequately capture the die-attach application geometry. Hence, this chapter introduces a novel methodology for characterizing thin bond-line interfaces with high-conductive materials. The transient heat flux impedance $\Delta Z_{th}(t,\Delta x)$ was measured between two thermally sensitive devices interconnected using pressureless Ag-sintering material. Based on thermal half-space principles, a correction factor was derived to account for non-uniform heat spreading over the die-attach interface. Experimental findings estimate an effective conductivity of ~115W/mk for the pressureless Ag-sintered interface. The measurement results were validated by measuring a SAC305 soldered interface, which exhibited ~55W/mK, and a non-conductive epoxy interface of ~2.5W/mK. Voids on the die-attach layer, resulting from material processing, were identified to influence the interface thermal behavior. An uncertainty analysis was further discussed, emphasizing equipment tolerances, measurement sensitivity, and geometrical and thermal anisotropies. The chapter concludes with a comparative summary of the proposed methodology against conventional methods, highlighting differences in working principle, thickness range, measurement parameters, and their advantages and limitations.

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5.1. INTRODUCTION

UNDERSTANDING and optimizing the die-attach material properties is crucial for high-temperature, high-power electronic devices [1–4]. The effectiveness of these materials has a significant impact on thermal performance and thermo-mechanical reliability, particularly in applications where efficient energy conversion and thermal management are pivotal [5–7]. Power devices undergo electrical overstress, mechanical vibrations, environmental humidity, and temperature fluctuations. Consequently, the die-attach layer that provides the necessary mechanical, electrical, and thermal bonding of the die to the package substrate endures thermo-mechanical stresses, affecting the device's electrical and thermal performance [8, 9].

High-conductive materials such as silver sintering are emerging as a promising solution for lead-free die-attachments in power device packaging due to their low processing temperature and high melting point after processing [10–13]. Despite their benefits, the thermal properties of silver sintering materials are often extracted based on bulk materials that do not represent thin interconnect layers. On the other hand, characterizing and extracting the thermal conductivity of a thin interface material (<50μm) presents a formidable challenge [14–17]. Streb et al. [18] explain the discrepancies in thermal conductivity extracted with conventional measurement methods such as laser flash, transient plane source measurements, and the ASTM D5470 standard DynTIM tester. Besides, these methods require specific samples that do not adequately represent the application form factor. The widely adopted JESD51-14 transient dual interface test method [19], despite an industry standard to determine Junction-to-Case thermal resistance, requires necessary resolution for extracting die-attach interface thermal resistance, particularly for materials with superior thermal conductivity [20].

Simone et al. [21] proposed a one-dimensional time-temperature transient model to determine the heat transfer coefficient between two flat metallic surfaces. In this study, we have demonstrated a similar methodology, particularly for characterizing die-attach interface thermal properties within the application-specific form factor. Motivated by the evolving landscape of die-attach materials [22–26] and the need to understand the effective interface thermal properties, this study demonstrates the following:

1. A methodology to estimate the effective interface thermal conductivity for complex and highly conductive die-attach materials, such as Ag-sintering, with appropriate form factor for semiconductor packaging applications.

2. A correction factor to account for the influence of non-uniform heat spreading based on thermal half-space principles.

3. A comparative summary to highlight the differences between the proposed methodology and other conventional measurement methods.

In the following section, the material selection and sample preparation are discussed first. Subsequently, the measurement methodology is detailed and the measurement results are presented with a comparative summary of the proposed methodology against other industry standard measurement methods.

5.2. MATERIALS AND METHODS

5.2.1. MATERIAL SELECTION

To demonstrate the experimental methodology, two thermally sensitive active devices were selected: (A) Thermal Test Chip (TTC) and (B) Schottky Diodes.

(A) THERMAL TEST CHIPS

Thermal Test Chips (TTCs) are specialized devices designed with integrated heating and temperature sensing elements to characterize and optimize interconnect materials and package thermal performance. The fabrication of TTCs follows a relatively straightforward and similar process to that of semiconductor devices. The TTCs can be developed on various semiconductor substrates, such as silicon (Si) or silicon carbide (SiC), by first depositing an oxide or nitride passivation layer using (plasma-enhanced) chemical vapor deposition techniques. Subsequently, the active heating and temperature sensing elements are lithographically defined. A second passivation layer is then applied over the active areas with vertical vias. An aluminum bond pad is deposited over the vias, facilitating wire bonding or flip chip bonding application. Further details on the development of TTCs are provided in [27, 28].

The test chip utilized in this study is a commercially available Silicon-based TTC with dimensions of 3.2mm × 3.2mm × 400μm and a 165Ω resistance per heating cell (3.2mm × 0.2mm). Each heating cell can handle a maximum current of ~400mA, resulting in a maximum power rating of ~250W per test chip when properly cooled. Figure 5.1a presents the calibration of a single heating cell at various ambient temperatures alongside a schematic layout of the TTC used in this study. The calibrated heating cell exhibits a linear temperature dependence with a sensitivity of ~0.47Ω/^{o}C over the temperature range of −55 to 150^{o}C. To best demonstrate the methodology, an ideal strategy would have been to connect all heating elements on the test chip in parallel, ensuring a more uniform temperature distribution across the device. However, due to practical constraints,

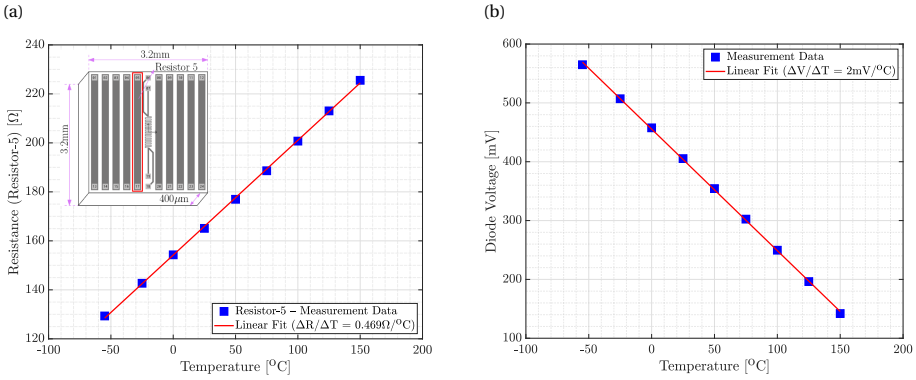


Figure 5.1: The resistance sensitivity of Resistor-5 (a) and Schottky diode (b) was evaluated at nine different temperatures, which exhibits a linear temperature dependence.

a single heating cell on the test chip was utilized in this study. A concentrated heat flux of ~2.6W/mm^2 was applied over Resistor-5 or Heater-5, which is positioned centrally (see figure 5.1a). This configuration resulted in a non-homogeneous thermal flux across the device. The lateral heat spreading over the silicon surface can potentially influence the estimated thermal conductivity at the die-attach interface. To account for this effect, a geometrical correction factor based on a characteristic width was employed. This correction factor is explained further in detail within the experimental results section. The backside of the test chip substrate was metalized with TiPtAu (100/100/100nm) to promote adhesion with the die-attach interface.

(b) Schottky Diode

A 200V 60A Silicon Schottky Rectifier in bare die form was utilized as the second active device in this study. Silicon Schottky Diodes are semiconductor devices with metal-semiconductor junctions, known as the Schottky barrier. They are used for fast switching and low forward voltage drop applications. However, in this study, we utilized these Schottky diodes for the sole purpose of temperature measurement. These diodes contain solderable top and bottom surfaces with TiNiAg (3μm) metal composition. Silicon Schottky diodes are temperature-sensitive devices that allow us to calibrate the Forward Voltage (V_f) with temperature (see figure 5.1b). A perfectly linear relationship can be exerted with a sensitivity of ~2mV/^{o}C.

(c) Die-attach materials

The choice of die-attach material is crucial to demonstrate the methodology. Three different materials with a wide range of thermal conductivities were selected for comparative analysis. The thermal conductivity values mentioned are based on the material datasheet.

1. **Commercial pressureless Ag-sinter material** with a high thermal conductivity of ~300W/mK.
2. **Commercial SAC305 solder paste** with a thermal conductivity of ~58W/mK, and
3. **Non-conductive epoxy material** with a thermal conductivity of <5W/mK.

5.2.2. Sample Preparation

The sample preparation involves semiconductor back-end packaging processes schematically illustrated in figure 5.2. The first step in the assembly process involves gluing the test chip onto the diode due to matching thermal expansion coefficients. The gluing process is different for each die-attach material.

- **Ag-Sintering:** Kapton films of varying thicknesses were used as stencils to apply the wet paste onto the TiNiAg metalized top surface of the Schottky diodes. The thermal test chips were then mounted using a die-bonder and sintered under nitrogen in a commercial hot-plate oven. The Ag paste was initially dried at 90^{o}C for ten minutes and subsequently sintered at 250^{o}C for forty-five minutes (see figure 5.2).
- **SAC305 Soldering:** Similar to the Ag-sintering process, SAC305 solder paste was stencil printed, and the devices were assembled using a die-bonder and soldered

in a hot-plate oven. The sample was first ramped up to 180°C at a ramp rate of 150K/min and held constant under Nitrogen for 120 seconds. Subsequently, the sample was further heated to 260°C at 200K/min and held at this reflow temperature under nitrogen for 12 seconds (see figure 5.2).

- **Non-conductive epoxy:** The non-conductive epoxy material was dispensed on the diode surface, the test chip was placed, and the assembly was cured in a hotplate at 150°C for an hour. Due to the lower curing temperature, the process order was reversed: the Schottky diode was first soldered to a PCB, and then the test chip was attached using epoxy.

Following the gluing step, the die-attach interface thickness, also known as the Bond Line Thickness (BLT), was measured using a confocal laser microscope. For the Ag-sintered samples, the BLT was varied during assembly by using stencils of different thicknesses. The primary goal of varying the BLT was to quantitatively evaluate its impact on thermal performance. The measured BLTs are shown in Figure 5.2.

The entire stack, except for the epoxy samples, was subsequently soldered onto a PCB and wire-bonded (see Figure 5.2). The samples were bonded using 99.99% pure gold wire bonds, with different wire diameters for the test chip (25μm) and the diode (50μm) due to practical constraints in bonding at different heights.

Finally, the samples were encapsulated using a solvent-free, pre-mixed thermoset epoxy-based "Fill" adhesive, along with a "Dam" encapsulant to protect the wire bonds (see figure 5.2). These epoxy-based encapsulants can withstand temperatures up to 160°C.

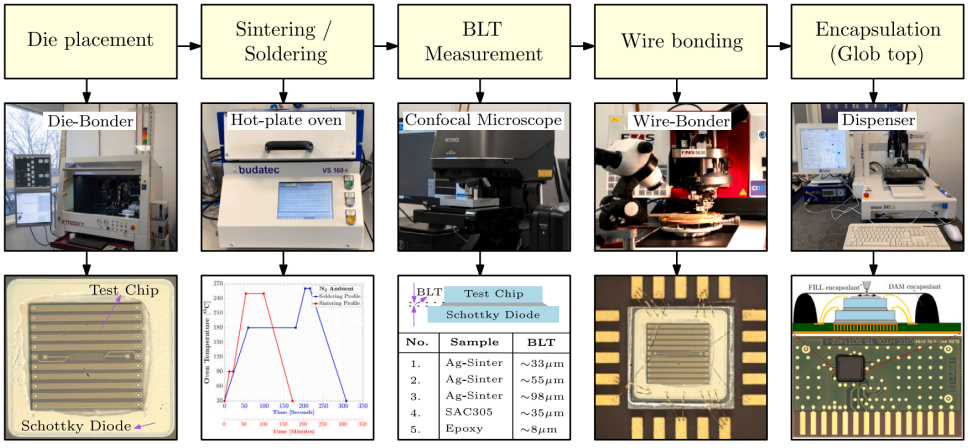


Figure 5.2: Illustration of the various package assembly processes involved in sample preparation. The TTC was placed over the diode using a die-bonder and subsequently cured using an industrial hot-plate oven. The interface bond line thickness (BLT) was measured upon curing using a confocal laser microscope. The samples were further wire-bonded and encapsulated.

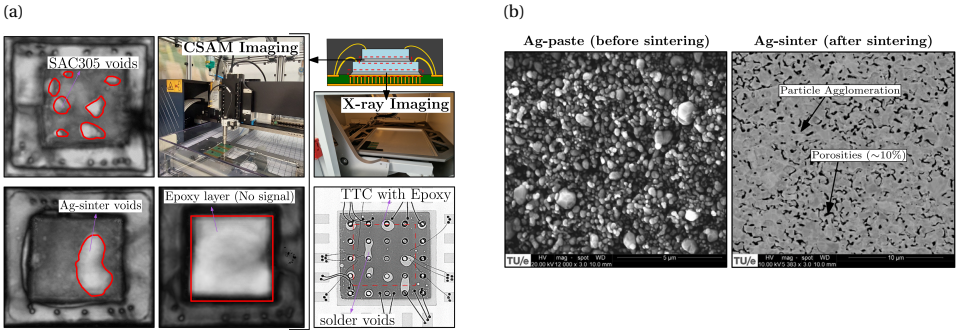


Figure 5.3: (a) Inspection of samples using CSAM imaging and X-rays. Voids on the Ag-sintered layer and SAC305 soldered layer were observed. No signal passes through epoxy material due to higher acoustic impedance. X-ray examination indicates voids on the PCB solder layer (below the diode). (b) SEM images of the Ag-paste before sintering (laterally dispensed in a flat plate) and after sintering (vertically cross-sectioned) are shown. Agglomeration of particles with 10% porosities was observed after sintering.

5

The encapsulated samples were further inspected using Confocal Scanning Acoustic Microscopy (CSAM) imaging. CSAM revealed abnormalities, primarily voids, within the Ag-sinter and SAC305 die-attach materials (see Figure 5.3a). The presence of voids on the die-attach interface can potentially influence the effective thermal conductivity of the interface, which is taken into account and explained in the experimental results section. The epoxy-layered sample exhibited higher acoustic impedance, which hindered the acoustic signal, making it difficult to evaluate the quality of the epoxy bonding. Therefore, no definitive information about the epoxy bonding quality could be obtained. However, epoxy samples facilitated X-ray inspection to detect solder voids beneath the diode (see Figure 5.3a). While the presence of voids is undesirable, the region of interest within this study is the interface between the test chip and the diode.

It is important to be aware that the effective thermal conductivity of an Ag-sintered interface is significantly influenced by the porosity of the sintered layer. Therefore, the Ag-paste was examined using an electron microscope both before and after sintering (see figure 5.3b). Post-sintering, the agglomeration of particles was observed, with the porosity estimated to be approximately ~10%.

5.3. EXPERIMENTAL PROCEDURE

A dedicated setup was developed to demonstrate the thermal characterization methodology, depicted schematically in Figure 5.4. The test boards with assembled samples were secured on a test socket inside a climate chamber oven. The backside of the test boards was clamped with a water-cooled heat sink using a thermal interface material. Electrical connections from the test socket were routed through a multiplexer (switch matrix) to connect the device to sourcing (SMU) and measuring (DMM) equipment. The source unit has a compliance of 40V up to 1A continuous current, and the measuring equipment has a resolution of ±0.16mV, which translates to ±0.005K/W. The SMU, DMM, and Multiplexer are interconnected using a trigger synchronization and communication

(TSP) protocol. All equipment, including the oven, is controlled using a user-defined MATLAB program. The electrical connections to the test chip and the diode are made of 4-point Kelvin contacts to minimize measurement inaccuracies.

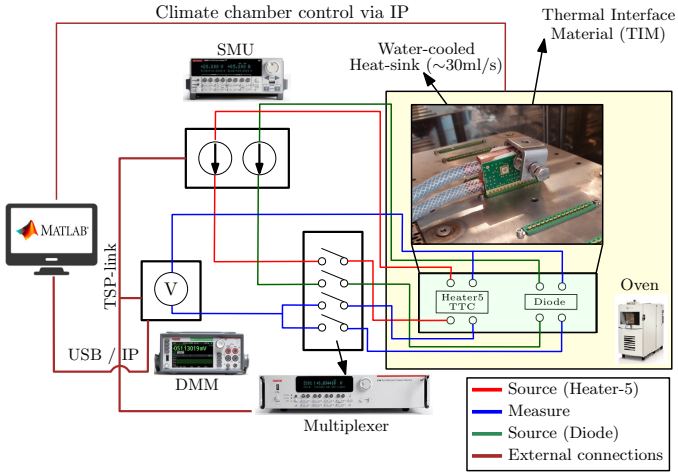


Figure 5.4: Schematic illustration of the experimental setup for measuring TTC on Diode configuration.

The thermal characterization method proposed in this study is an adaptation of the industry standard JESD51-14 transient dual interface test method [19]. The JESD51-14 determines Junction-to-Case thermal resistance $Z_{th(j\text{-}c}(t)$ of a package by comparing measurements with and without Thermal Interface Material (TIM). The JESD51-14 suggests mounting the devices on a water-cooled heat sink for 1-dimensional heat flow from the device to the heat sink. In this study, the samples were mounted using TIM on a water-cooled heat sink with a flow rate of 30ml/s. The water-cooled heat sink ensures the heat generated from the test chip is driven towards the diode. The fundamental difference between both methods is that the JESD51-14 measures only the device junction temperature, whereas the proposed method measures the temperature difference between the device junction and substrate under the transient mode, thereby the effective interface thermal resistance can be extracted.

The workflow of the measurement method and the data processing steps are charted in figure 5.5. The measurements begin with the calibration of Heater-5 and the diode. After recording the ambient conditions, the change in temperature $\Delta T(t,x)$ of both the test chip and the diode was sequentially measured by applying a maximum heat flux of $\sim 2.6 W/mm^2$ for one hundred seconds and further cooled down over another one hundred seconds. Figure 5.6a illustrates the measured $\Delta T(t,x)$ of the test chip and the diode for the Ag-sintered sample with a bond line thickness of approximately 33μm, along with the applied input power. The measurement data of the test chip shows a lower signal-to-noise ratio, indicating higher fluctuation compared to the diode measurement. The fluctuation in temperature measurements of the test chip was approximately $\pm 0.5K$.

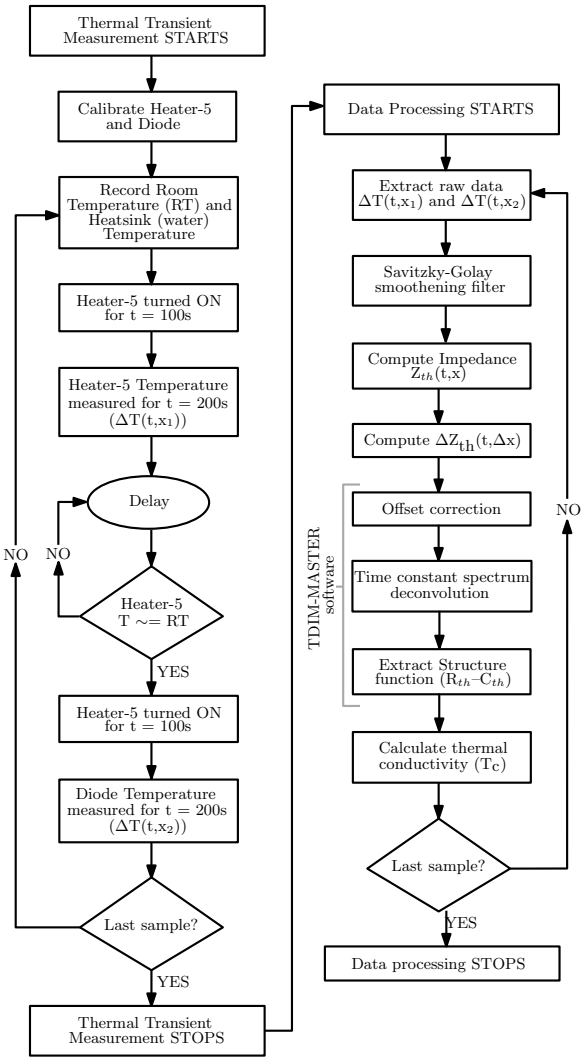


Figure 5.5: Flow chart demonstrating the experimental methodology and data processing. All measurements were performed at room temperature (~25°C). The heat sink temperature was the same as room temperature. The data processing was partly performed using JEDEC TDIM-Master software.

Normalizing the measured temperature $\Delta T(t,x)$ with the applied input power yields transient thermal impedance $Z_{th}(t,x)$ for both the test chip and the diode based on the heating up and cooling down measurements (see figure 5.6b). The data shown are processed after fitting a Savitzky-Golay smoothening filter to mitigate measurement noise. The impedance data provides comprehensive insights into the thermal characteristics spanning from transient to steady-state conditions. An offset in impedance between heating up and cooling down is observed, indicating heat loss during switching currents. This offset is corrected at a later stage. By subtracting the diode impedance $Z_{th}(t,x_2)$

from the test chip impedance $Z_{th}(t,x_1)$, we obtain the heat flux impedance $\Delta Z_{th}(t,\Delta x)$ between the test chip and the diode (see figure 5.6c). The heat flux impedance shows more pronounced thermal dissipation signals during the cooling down phase compared to heating up, which is in agreement with the guidelines stated in JESD51-14 [19].

Consequently, the heat flux impedance $\Delta Z_{th}(t,\Delta x)$ was determined for all samples during the cooling down phase, and the results are shown in figure 5.6d. The heat flux impedance $\Delta Z_{th}(t,\Delta x)$ for the Ag-sintered interfaces increases with increasing bond line thicknesses. Likewise, the thermally non-conductive epoxy material exhibits the highest heat flux impedance compared to Ag-sintered samples and SAC305. The obtained heat flux impedance represents the combined resistance of the test chip silicon and the die-attach interface. Therefore, further processing is required to extract the effective interface thermal resistance and subsequently translate it into effective interface thermal conductivity.

An essential step in extracting the contribution of interface thermal resistance from the heat flux impedance is to determine the time-constant spectrum. The offset in the cooling down curve (figure 5.6b) was corrected first by extrapolating the $\Delta Z_{th}(t,\Delta x)$ to t = 0 as shown in figure 5.6e. Subsequently, the time-constant spectrum was established and discretized into finer steps to construct the thermally equivalent Foster network, which was further transformed into a Cauer network. The resistance-capacitance network in the Cauer domain (structure-function) represents the actual thermal properties of the materials within the system. For a detailed explanation of the steps involved in structure-function computation, please refer to [29–31]. In this study, we utilized the TDIM-Master software provided by JEDEC for offset correction, time-constant spectrum deconvolution, and structure-function computation. The following section discusses the results, including a correction factor for non-uniform heat spreading and an uncertainty analysis.

5.4. EXPERIMENTAL RESULTS AND DISCUSSION

5.4.1. THERMAL CHARACTERIZATION RESULTS

Upon generating the RC Cauer network from the time constant spectrum, the TDIM Master generates the cumulative structure-function. This graphical representation illustrates the thermal resistance-capacitance network of the system, encompassing the bulk silicon of the test chip and the die-attach interface (see figure 5.6f). The cumulative structure function is plotted on a logarithmic scale to highlight the influence of silicon resistance. The theoretical thermal resistance of the test chip silicon was calculated to be ~0.26K/W, corresponding to the transition point identified in the structure-function. This enables determining the effective interface thermal resistance of the die-attach as emphasized in figure 5.6f. Knowing the effective interface thermal resistance, the effective thermal conductivity of the die-attach interface can be calculated as follows:

$$T_c[W/mK] = \frac{1}{R_{th}[K/W]} \frac{L[m]}{A[m^2]} \tag{5.1}$$

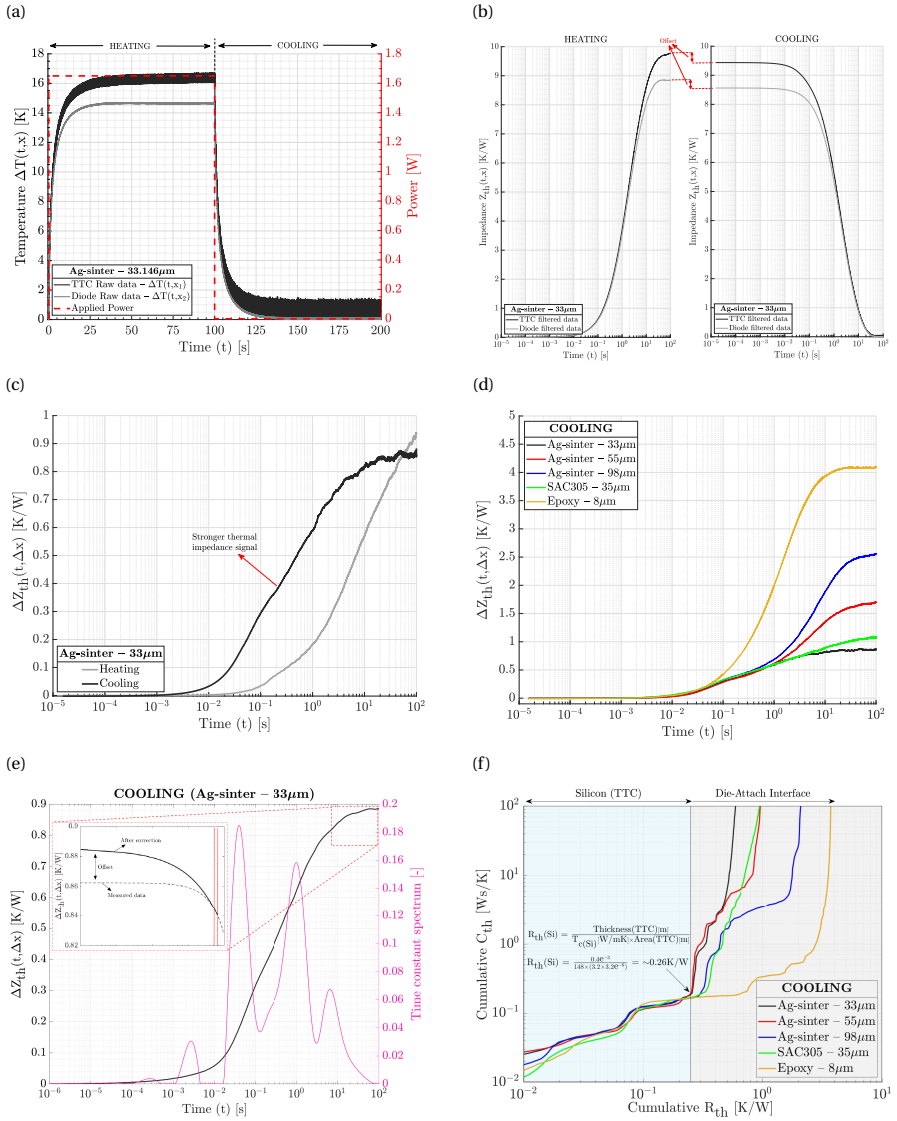
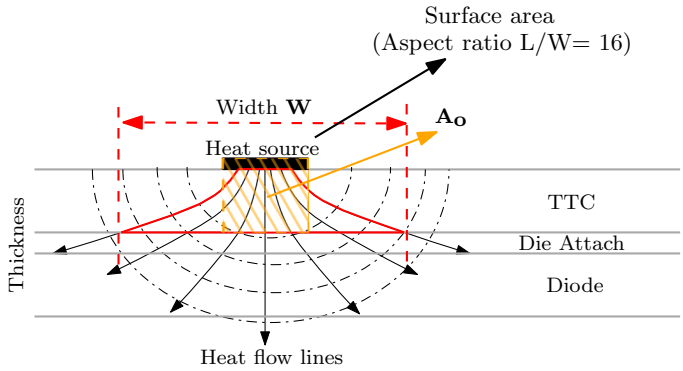


Figure 5.6: (a) Raw measurement data of the test chip and the diode is shown along with the applied power input. The test chip has a lower signal-to-noise ratio compared to the diode. (b) Smoothened impedance data is shown on a logarithmic scale, highlighting the offset between heating up and cooling down. (c) The heat flux impedance obtained from the cooling down curve indicates a stronger heat dissipation signal. (d) The heat flux impedance data of all five samples; Ag-sinter ~33μm, ~55μm, and ~98μm; SAC305 solder paste and non-conductive epoxy glue are shown. (e) The offset on heat flux impedance data $\Delta Z_{th}(t,\Delta x)$ was corrected and the time-constant spectrum was determined. (f) Cumulative structure function of Ag-sinter ~33μm, ~55μm, ~98μm, SAC305 & Epoxy glue is shown. The Silicon test chip has a resistance of ~0.26K/W, and the remainder provides the effective thermal resistance of the die-attach interface.



Non-dimensionalized heat-spread area

Step:1 Out-of-plane heating area A_O
Assumption - Isothermal heating

Step:2 Characteristic width $W = \sqrt{A_O}$

Step:3 Correction factor (CF) $= \frac{\sqrt{A_O}}{\text{Heater Width}}$

Step:4 Active Area 'A' = CF×Heater-5 area

Figure 5.7: Schematic representation of heat spreading on half-space. A characteristic width was determined from the out-of-plane heating area, and a correction factor was established to estimate the heat spread area on the die-attach.

In equation 5.1, 'L' represents the bond line thickness, and 'A' denotes the active heat spreading area on the die-attach interface. However, the actual interaction area (electrical, thermal, and mass transfer) between two contacting bodies varies depending on the contacting surfaces [32]. Two fundamental phenomena can influence heat transfer area; thermal contact resistance due to interface imperfections and thermal spreading resistance. The extracted effective interface thermal resistance from figure 5.6f is a summation of resistances from the metallization layers, die-attach material, and other contact resistances. For more details on the influence of thermal contact resistance in heat transfer, please refer to [33, 34].

Thermal spreading resistance is a widely researched topic in thermal engineering, which needs to be taken into account in scenarios where a concentrated heat source interacts with a broader conducting surface, resulting in spreading resistance. Hence, considering the Heater-5 area as the active heat spreading area on the die-attach interface may provide insufficient representation for computing the effective interface thermal conductivity. Decades of research on both steady-state and transient thermal spreading phenomena over smooth and rough surfaces are extensively documented in [32]. The square root of the heat source area $\sqrt{A_o}$ is commonly used to non-dimensionalize spreading resistance for different shapes on a half-space. [35] has validated $\sqrt{A_o}$ as the

most appropriate parameter to compute non-dimensional spreading resistance. In this study, we employed the characteristic parameter $\sqrt{A_o}$ to derive a correction factor that adequately represents the active heat spreading area on the die-attach (figure 5.7).

Two assumptions were made to compute the active area on the die-attach surface for non-uniform heating surfaces:

- The geometry of Heater-5 has an aspect ratio (L/W) of 16. Hence, the heat spreading along the length of the heater surface was assumed to be uniform.
- The second assumption is that the primary heat transfer area to the die-attach is equivalent to the area of Heater-5; thus, considering an isothermal out-of-plane heating area A_o.

Accordingly, a characteristic width ($\sqrt{A_o}$) was determined, and a correction factor was derived (see Figure 5.7). Notably, this correction factor is derived under the assumption of concentrated heating over an infinitely large plane. Further validation of the correction factor's applicability is essential. Based on the effective interface thermal resistance extracted from Figure 5.6f and the active area 'A' estimated from Figure 5.7, the effective interface thermal conductivity 'T_c' can be determined using Equation 5.1. However, the presence of voids on the die-attach interface (see figure 5.3a) leads to underestimation of 'T_c'. Therefore, based on voids identified from CSAM imaging, a reduced active area '$A_{reduced}$' was determined, establishing the 'T_c' of Ag-sintered interface. A standard deviation was further shown based on Active Area 'A' and Reduced Active Area '$A_{reduced}$'. The results are depicted in Figure 5.8, leading to the following conclusions:

- Ideally, thermal conductivity should be independent of the interface thickness. However, due to processing defects observed on the die-attach layer (see Figure 5.2),

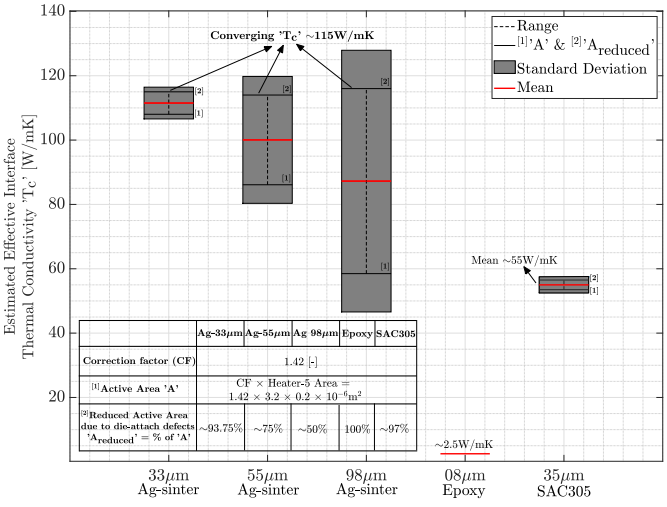


Figure 5.8: Standard deviation of effective interface thermal conductivity 'T_c' estimated based on active area 'A' and reduced active area '$A_{reduced}$' due to interface defects.

the effective interface thermal conductivity varies among samples with different thicknesses.

- A standard deviation of the effective thermal conductivity for Ag-sintering and SAC305 was determined based on the active area 'A' and the reduced active area '$A_{reduced}$'. Ag-sinter samples with bond line thicknesses of 55μm and 98μm exhibit the largest deviation due to the presence of voids. However, based on '$A_{reduced}$', a converged T_c of ~115W/mK was estimated for Ag-sintered interfaces.

- In comparison, the SAC305 interface exhibits ~55W/mK, while epoxy glued interface indicates ~2.5W/mK, which are expected as mentioned in their datasheet.

The estimated effective thermal conductivity for Ag-sintered interface (~115W/mK) compared to the Ag-sintered material conductivity stated in the datasheet (~300W/mK) highlights the limited understanding of interface properties as opposed to bulk materials. Therefore, based on the literature, a comparison of the Ag-sinter properties as a function of porosity is presented in Table 1.

Table. 1. A comparison of Ag-sinter thermal conductivity from literature.

No.	Material Type	Porosity (%)	Thermal Conductivity (W/mK)	Ref.
1.	Heraeus C1075S pressure-assisted Ag-sintering	~38%	~75W/mK	[36]
2.	DuPont LF131 pressure-assisted Ag-sintering	~19%	~175W/mK	[36]
3.	Heraeus LTS016 pressure-assisted Ag-sintering	~7%	~350W/mK	[36]
4.	Heraues LTS043 pressure-assisted Ag-sintering	~4%	~375W/mK	[36]
5.	Nanosilver 250^{o}C &; 10MPa	~0 – 15%	~200 – 158W/mK	[37]
6.	Heraeus Ag-paste 200^{o}C & 5MPa	~22%	~150W/mK	[38]
7.	**Pressureless Ag 250^{o}C (This study)**	**~10%**	**~115W/mK (Eff. Interface conductivity)**	[-]

The thermal conductivity determined based on the proposed method is in a similar range as observed in the literature. However, there are two primary distinctions: The samples analyzed in this study have the appropriate form factor for die-attach interfaces, as compared to sintered coupons or dog-bone structures. The estimated thermal conductivity is an effective interface property that includes metallizations, the die-attach material, and other contact interactions.

5.4.2. DISCUSSION

The methodology proposed in this study has demonstrated its capability to measure the effective interface thermal resistance across varying bond line thicknesses and materials with diverse thermal properties. Based on the measured interface thermal resistance, this study has also demonstrated a means to estimate the effective interface thermal conductivity for surfaces with non-uniform heat-spreading and interfaces with processing defects. Nevertheless, it is essential to acknowledge that several other factors might introduce uncertainty to the measurement results (see Table 2).

Table. 2: Standard Uncertainty Analysis

Source of Uncertainty		Standard Uncertainty				
		Ag ~33μm	**Ag ~55μm**	**Ag ~98μm**	**SAC305 ~35μm**	**Epoxy ~8μm**
BLT Measure--ments	**Equipment tolerance**	$\pm0.1\mu$m				
	Die Tilt (~5% BLT)	$\pm2\mu$m	$\pm3\mu$m	$\pm5\mu$m	$\pm2\mu$m	$\pm0.5\mu$m
Measurement Sensitivity		±0.16mV = ±3.9mΩ = ±0.008K = ±0.005K/W				
TTC Noise-to-Signal ratio		±0.5K = ±0.3K/W				
Offset correction		~0.04K/W	~0.03 K/W	~0.06 K/W	~0.07 K/W	~0.04 K/W
Silicon thermal conductivity		140–156 W/mK = ±8W/mK = ±0.015K/W				

- Measuring the bond line thickness of the die-attach interface is critical for estimating the effective interface thermal conductivity (Equation 5.1). The confocal laser microscope has a tolerance of $\pm0.1\mu$m. Additionally, the samples typically exhibit die-tilt during the curing process, amounting to ~5% of BLT.

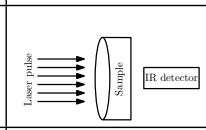
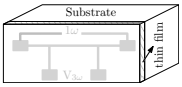
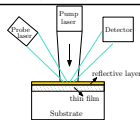
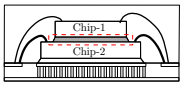
- The measuring equipment (DMM) has a sensitivity of ±0.16mV, translating to an uncertainty of ±0.005K/W. Furthermore, the low signal-to-noise ratio observed in Figure 5.6a results in fluctuations of ±0.5K, which corresponds to ±0.3K/W in $Z_{th}(t,x_1)$.

- The offset observed in Figure 5.6b, results in an uncertainty of ~0.03 to 0.07K/W in $\Delta Z_{th}(t,\Delta x)$.

- Extracting the interface thermal resistance by subtracting the influence of silicon, introduces an uncertainty due to variations in silicon's thermal conductivity at room temperature (typically between 140W/mK to 156W/mK), leading to an uncertainty of ±0.015K/W. Besides, the thermal properties of silicon have a strong temperature dependency.

Managing these uncertainty parameters poses challenges, especially in addressing geometrical and thermal anisotropies. Besides, the correction factor introduced for non-uniform heat spreading requires further validation. Moreover, the presence of intermetallic compounds at the die-attach interface introduces additional challenges in

Table. 3: A comparative summary of the proposed methodology against other thin-film thermal conductivity measurement methods.

	Laser flash method	**3ω method**	**Time-Domain Thermoreflectance (TDTR)**	**Heat flux Impedance (This paper)**
Working principle				
Thin film thickness	~0.1mm to a few mm.	~0.01 to 0.1mm	Depends on the penetration depth of the probe laser (Typ. ~0.01 to a few mm.)	~0.008 (demonstrated in this paper) to a few mm.
Measurement parameter	Temperature	Temperature-dependent Electrical resistance	Temperature	Temperature Sensitive Electrical Parameters
Advantages	1. Fast and non-destructive. 2. High accuracy and precision	1. Non-destructive and contactless. 2. Suitable for very thin samples.	1. High sensitivity and high spatial resolution. 2. Non-destructive and contactless	1. Right form factor. 2. Wide range of thicknesses and materials. 3. Non-destructive and contactless.
Limitations	1. Specific samples and specialized equipments are needed. 2. Not suitable for optically transparent materials.	1. Complexity. 2. Dependence on substrate properties. 3. Limited thickness range.	1. Complexity. 2. Specific samples and specialized equipments. 3. Limited material compatibility.	1. Accuracy needs to be validated. 2. Require specific samples and dependent on the sample quality.

ensuring reliable interconnect formation. Despite several practical challenges addressed, the methodology provides compelling reasons for its adoption as a tool to determine die-attach interface thermal conductivity in semiconductor packaging.

Table 3 summarizes the proposed heat flux impedance methodology alongside three other conventional thin-film thermal conductivity measurement methods, namely laser flash, 3ω, and Thermoreflectance thermography. The comparative summary highlights the differences in their working principle, thin-film thickness range, measurement parameters, and advantages and limitations.

5.5. CONCLUSION

While several drop-in replacements for lead (Pb) solders are emerging, it is important to understand the effective thermal conductivity of the die-attach interface and their influence on the package thermal performance. This study has addressed this critical need by introducing a methodology for characterizing the effective interface conductivity for complex and high conductive die-attach materials, overcoming misrepresentations of bulk material properties for thin film interfaces.

- The methodology demonstrated its efficiency by estimating the thermal conductivity across a range of materials (pressureless Ag-sintering material, SAC305 solder paste, and non-conductive epoxy) with varying bond line thicknesses (~8 – 98μm).
- A correction factor for non-uniform heat spreading based on the thermal half space principles was introduced to estimate the effective heating area on the die-attach interface.

- The influence of die-attach materials processing defects was identified as a significant challenge. Hence, standard deviations in thermal conductivity measurements were determined.
- Besides, parameters such as geometrical and thermal anisotropies, equipment sensitivity, and other external influences, introduce uncertainty to the measurement results. This has been briefly discussed along with a comparative summary of the proposed method against other conventional measurement methods.

In conclusion, this study advances our understanding of die-attach interface thermal conductivity, recognizing that bulk material properties do not adequately represent interface behavior. This is particularly important for complex materials such as Ag-sintering, whose effective interface conductivity depends on its processing conditions.

For future research and practical applications, the methodology can be simplified by connecting two diodes using the desired die-attach material, achieving a PNP or NPN configuration with a die-attach interface. This approach can mitigate the effects of non-uniform heat spreading. An NPN interface configuration, in particular, might further minimize the influence of silicon resistance on the interface measurements, as device heating occurs at the P-junction, which is closer to the die-attach interface. Continued refinement of measurement techniques and deeper exploration into interface thermal behavior will lead to sustainable semiconductor packaging technologies.

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6

HETEROGENEOUS INTEGRATION OF DIAMOND HEAT SPREADERS FOR POWER ELECTRONICS APPLICATION

Integrated Circuits and Electronic Modules experience concentrated thermal hot spots, which require advanced thermal solutions for effective distribution and dissipation of heat. The superior thermal properties of diamonds are long known, and it is an ideal material for heat-spreading applications. However, growing diamond films to the electronic substrate require complex processing at high temperatures. This chapter investigates a heterogeneous method of integrating diamond heat spreaders during the back-end packaging process. The semiconductor substrate and the heat spreader thicknesses were optimized based on simulations to realize a thermally enhanced Power Quad-Flat No-Lead package. The performance of the thermally enhanced PQFN was assessed by monitoring the temperature distribution across the active device surface and compared to a standard PQFN (without a heat spreader). Firstly, the thermally enhanced PQFN indicated a ~9.6% reduction in junction temperature for an input power of 6.6W with a reduced thermal gradient on the active device surface. Furthermore, the diamond heat spreader's efficiency increased with increasing power input. Besides, the reliability of the thermally enhanced PQFN was tested by thermal cycling from -55^oC to 150^oC, which resulted in less than 2% thermal degradation over two-hundred cycles. Such choreographed thermal solutions are proven to enhance the packaged device's performance, and the superior thermal properties of the diamond are beneficial to suffice the increasing demand for high power.

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6.1. INTRODUCTION

ADVANCES in the semiconductor lithography process, heterogeneous integration, and advanced electronic packaging are the driving factors for electrification [1, 2]. For instance, the transportation sector has experienced a paradigm shift due to carbon-neutral commitments. The percentage cost of electronics in automobiles was less than 10% in 1980, which surpassed ~35% in 2010, and it is expected to reach 50% by 2030 [3]. The incremental growth also led to increased power density, i.e., the chip heat flux in today's modern devices is around 300 times higher than the flux density in 1980 (0.5 W/cm^2) [4, 5]. The increasing demand for high power in electronics emphasizes the need for thermal management. Device failure due to thermal breakdown is significantly higher than vibrations, humidity, and dust [5, 6].

Device heating is an undesirable side-effect during operation, thereby limiting its performance. With miniaturization and increasing chip density, the heat generation is concentrated within a small area, leading to thermal hot spots. For instance, the gate-to-gate spacing in Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) is typically less than 50μm, which creates concentrated thermal regions [9]. Heat sinks alone are insufficient to dissipate highly concentrated heat flux. Consequently, thermal barriers in power electronics are becoming inevitable. Figure 6.1 [7, 8] shows an overview of various materials and their thermal conductivity. Thermal conductivity is the ability of a material to conduct heat, and diamonds are known for their excellent thermal conductivity. Diamond also has a relatively low thermal capacity, which makes it an ideal candidate for a heat spreader. Several researchers have focused on incorporating diamonds in power electronics as either active semiconductors or passive heat spreaders [9–12]. Despite

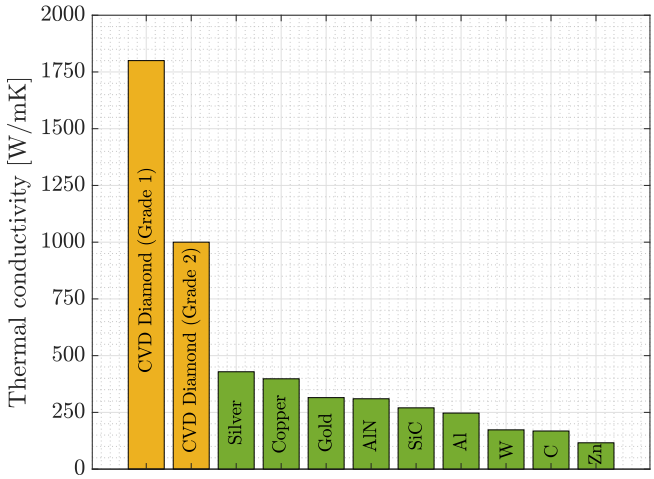

Figure 6.1: The thermal conductivity of CVD diamond outperforms other materials such as silver, copper, and gold [7, 8]. CVD diamonds come in two grades, Grade 1 and 2, with thermal conductivity ranging from 1800 to 1000W/mK

considerable research interests, incorporating diamonds in power electronics suffers from complex processing, high temperatures, and cost. Recent advancements in fabricating diamonds through the Chemical Vapor Deposition (CVD) process have reduced the cost to ~$\$1/mm^2$ [9].

The most common way to create passive heat spreaders on active devices is to grow synthetic diamond films on silicon substrates. However, these processes typically yield micro-crystalline structures, resulting in higher thermal resistance between the Diamond-Silicon interface [12]. Besides, implementing such a complex process on wafer-level fabrication is more risky due to high processing temperatures. This study investigates a heterogeneous integration process of incorporating diamond heat spreaders to the backside of a thin silicon device during package assembly. A double sintering process using pressureless nano-silver sinter material was adapted for integration. Commercial Thermal Test Chips (TTCs) [13] were used as a test vehicle to characterize the heat spreading effect.

The Silicon and Diamond layer thicknesses were optimized based on parametric transient thermal simulations. The heterogeneous integration process of realizing the thermally enhanced packages and the package integrity evaluation is then discussed. Subsequently, the experimental evidence on the heat spreading effect is demonstrated by comparing standard packages (without a heat spreader) with thermally enhanced packages. Finally, the thermo-mechanical reliability of a thermally enhanced package was assessed for two hundred thermal cycles from -55^oC to 150^oC. This paper concludes by summarising the empirical results and emphasizing the need for advanced thermal solutions.

6.2. EXPERIMENTAL METHODS: OPTIMIZATION AND ASSEMBLY

Multiple heating and temperature-sensing elements within a single chip are needed to quantify the effect of heat spreading, which makes Thermal Test Chips (TTC) best suited for this application. Several research activities focus primarily on developing test chips [14–16]. Application of TTC for package-level reliability assessment has been previously investigated [17, 18]. A commercial TTC [13] is used in this research, and a schematic of the TTC is shown in figure 6.2a. The resistive heating and sensing elements highlighted in figure 6.2a have a linear temperature dependency. The resistance sensitivity of Resistors 1-10 is $0.46\Omega/^oC$, and the resistance sensitivity of the spiral resistor is $7\Omega/^oC$ (figure 6.2b). The differences in the resistance sensitivity of the various elements in the test chip are due to their geometrical differences. Normalizing the resistance sensitivity with the base resistance results in its material's Temperature Coefficient Resistance (TCR). A Printed Circuit Board (PCB) was designed with 4-point kelvin connections (figure 6.2c) to measure the resistance of the elements in the test chip (figure 6.2a). The front side of the PCB was patterned for connections to a Power Quad Flat No-Lead (PQFN) surface mount package, and the backside has a copper ground plane for Electromagnetic Interference reduction. A test setup for accommodating the test boards was built inside a temperature-cycling (TMCL) industrial oven (figure 6.2d). The test boards were connected to a source unit and a digital multi-meter via a switch matrix.

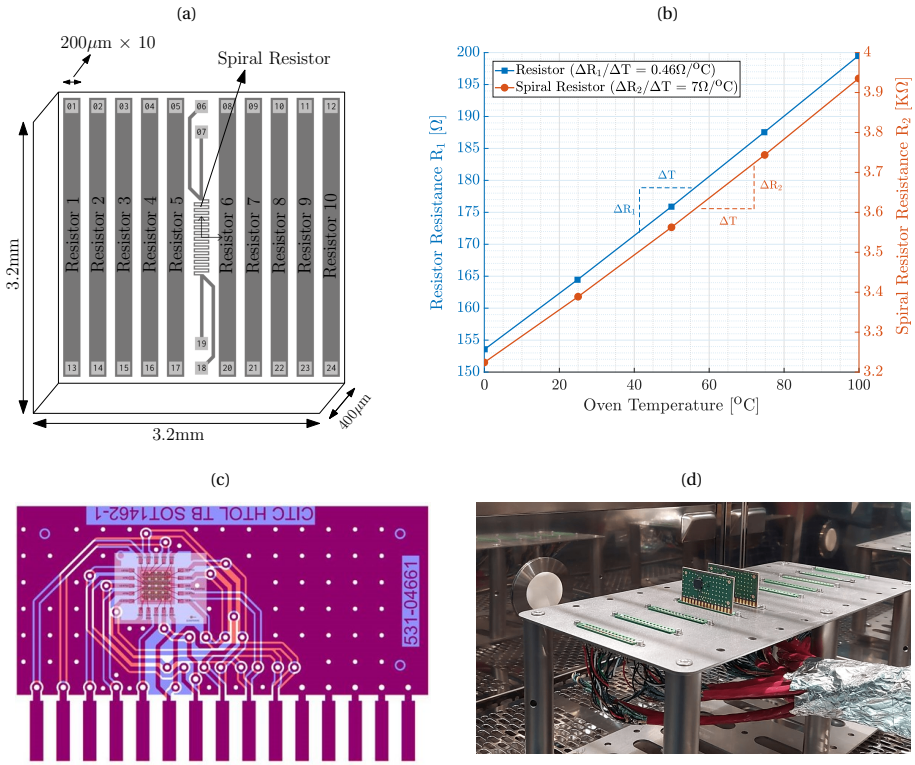

Figure 6.2: (a) A schematic layout of the Thermal Test Chip (TTC) from [13]. The TTC has 10 Resistors with a resistance of ~165Ω and a spiral resistor with a resistance of ~3.4KΩ (typical at 25°C). (b) Calibration of the device resistance from 0°C and 100°C. The device shows a perfectly linear response with temperature. (c) A test board layout with double-side metallic tracks for electrical connection from the device to the equipment. (d) A test setup accommodating test boards inside thermal cycling (TMCL) oven for temperature-dependent electrical measurements.

Material optimization is required to realize a thermally enhanced electronic package. Despite the diamond's superior thermal conductivity, the TTC (Silicon) substrate thickness also influences thermal dissipation. Hence, a parametric numerical simulation study was conducted using Finite Element Methods (FEM) to identify optimal Silicon and Diamond layer thicknesses. A complete PQFN package design with the test board (figure 6.2c) was simulated to represent the experimental conditions. A 3D Hexahedron mesh of the PQFN package materials with the test board is shown in figure 6.3. The Von-Neumann stability criterion for thermal diffusivity needs to be satisfied to ensure a numerical convergence of the transient thermal simulation. To briefly explain the stability criterion, let us assume that the heat transfer through the system happens only through Conduction (i.e., ignoring the effect of Convection and Radiation). Accordingly, a one-dimensional temperature distribution equation can be expressed (equation 6.1), where x denotes the spatial coordinates, T denotes the temperature, t denotes the time and α denotes the thermal diffusivity. Discretizing the one-dimensional equation results in the critical mesh

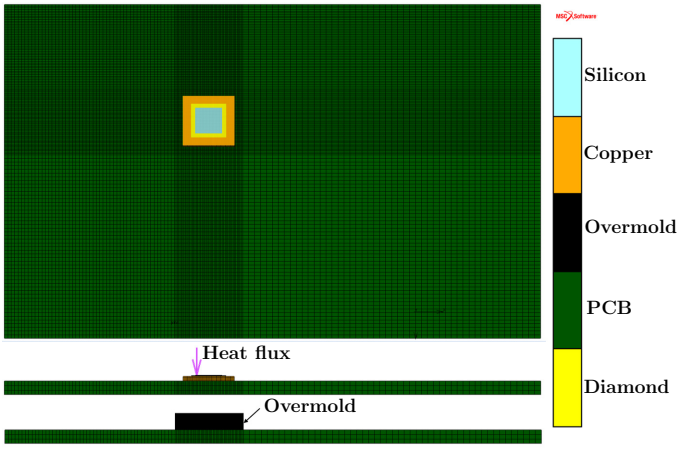

Figure 6.3: A finite element Hexahedron mesh for transient thermal simulations with different layers (indicated in colors). The Von-Neumann stability criterion for thermal diffusivity was satisfied by limiting all layers' mesh ratio to less than the critical mesh ratio r_c.

ratio $r_c = \frac{\alpha \Delta t}{\Delta x^2}$, which must be less than or equal to 0.5. More details on the discretization and stability criterion are given in [17, 19].

$$\frac{\partial^2 T}{\partial x^2} = \left(\frac{1}{\alpha}\right) \cdot \frac{\partial T}{\partial t} \tag{6.1}$$

The geometrical inputs for the simulation are given in table 6.1, and the material properties at room temperature are provided in table 6.2. The thickness parameter of the die (Silicon) a is varied from 50μm to 400μm, and the heat spreader (Diamond) b is varied from 0μm to 400μm. The contact resistances between the Die-Heat spreader and the Heat spreader-leadframe were chosen based on the thermal conductivity of Silver [20]. Likewise, the contact resistance between the Leadframe-PCB was chosen based on the thermal conductivity of the SAC305 solder paste. Glued contacts were assumed for all other contact points in the simulation.

Table 6.1: Geometrical dimensions of different layers (figure 6.3) is provided. The thickness of the TTC and the heat spreader are kept parametric. The overall thickness of the molding compound remains the same. However, the thickness of the molding compound above the die varies according to the defined parameters (***a*** and ***b***).

Material	Width [mm]	Length [mm]	Thickness [mm]
Die	3.2	3.2	***a*** = [0.05 - 0.4]
Heat spreader	4	4	***b*** = [0 - 0.4]
Leadframe	6	6	0.55
PCB laminate	40	63	1.65
Overmold	8	8	2

Table 6.2: Silicon and copper thermal properties at room temperature were obtained from [21–23]. The properties of CVD Diamond were obtained from the supplier. The PCB design was simplified by assuming the properties of Polyimide (PCB laminate core). The Epoxy Molding Compound properties were taken from the datasheet of Sumitomo EME-G700LA.

Material	Density (ρ)[g/mm^3]	Conductivity (k) [W/mmK]	Specific heat (c_p) [J/gK]
Silicon	$2.32e^{-3}$	0.148	0.7
Diamond	$3.52e^{-3}$	1.8	0.5
Copper	$8.96e^{-3}$	0.401	0.385
Polyimide	$1.88e^{-3}$	0.00173	1.13
Epoxy	$0.95e^{-3}$	0.00096	1.9

An input power of 6.6W is applied at the Resistor 1 location (figure 6.2a) for a duration of 1 second, which is equivalent to the input heat flux of ~10.5W/mm^2. The input power and heating time were chosen according to the experimental limitations (max. 40V restriction with the source unit). The Junction temperature was chosen as a metric to compare the effect of reducing the chip thickness (parameter *a*) and increasing the heat spreader thickness (parameter *b*). The simulation results shown in figure 6.4 highlight the influence of the silicon and the heat spreader thicknesses on thermal dissipation. Reducing silicon thickness is favorable for achieving improved thermal performance, and adding a diamond heat spreader further reduces the junction temperature (figure 6.4). However, it can be observed that the junction temperature reduction doesn't scale linearly with the Diamond thickness for 50μm Silicon. In other words, the maximum percentage difference for 50μm Silicon is observed between 0μm and 100μm Diamond. Hence, 50μm TTC thickness with 100μm Diamond heat spreader was chosen for this experimental study.

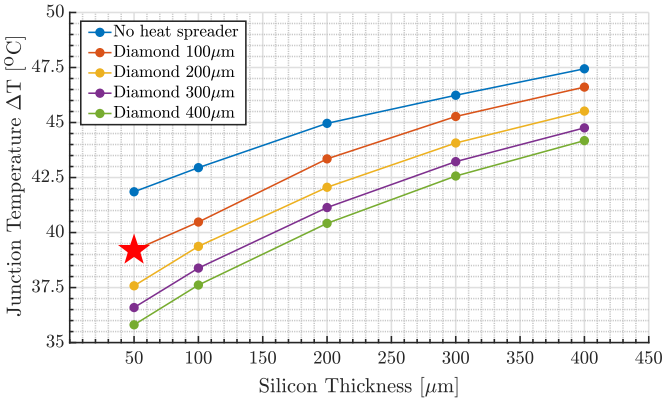

Figure 6.4: Parametric transient thermal simulation results with input power of 6.6W (~10.5W/mm^2) applied at Resistor 1 location (figure 6.2a) for a duration of 1 second. The Junction temperature recorded from simulations is the ΔT caused by the applied input power at the end of 1 second. As highlighted, the 50μm TTC thickness with 100μm Diamond heat spreader was chosen as an optimal point for this study.

To realize a thermally enhanced packaged product (based on simulation results) requires a series of assembly processes to be carried out as depicted in schematics (figure 6.5). The first step is to thin down the substrate thickness of the TTC. Since the lithographically defined active layers are at the top of the die, the back side of the TTC was polished to reduce the substrate thickness from 400μm to 50μm. The polished TTCs were cleaned with an ultra-sonic bath, and the chip was electrically probed to test its functionality. The polishing process removed the backside metallization, which is needed to promote its adhesion with the interconnect material. Hence, the polished backside of the test chips was sputter coated with Ti/Pt/Au of 100/200/600nm. Subsequently, the CVD diamond wafer of 110μm thickness was diced at 4mm × 4mm and sputter coated with Ti/Pt/Au of 100/200/600nm.

Nano-Silver sinter paste was dispensed on the metalized diamond slab using a time (or) pressure-controlled dispensing machine. The metalized thinned TTC was wet mounted to the diamond substrate using a die-bonder. Post wet-mounting, the die-diamond stack

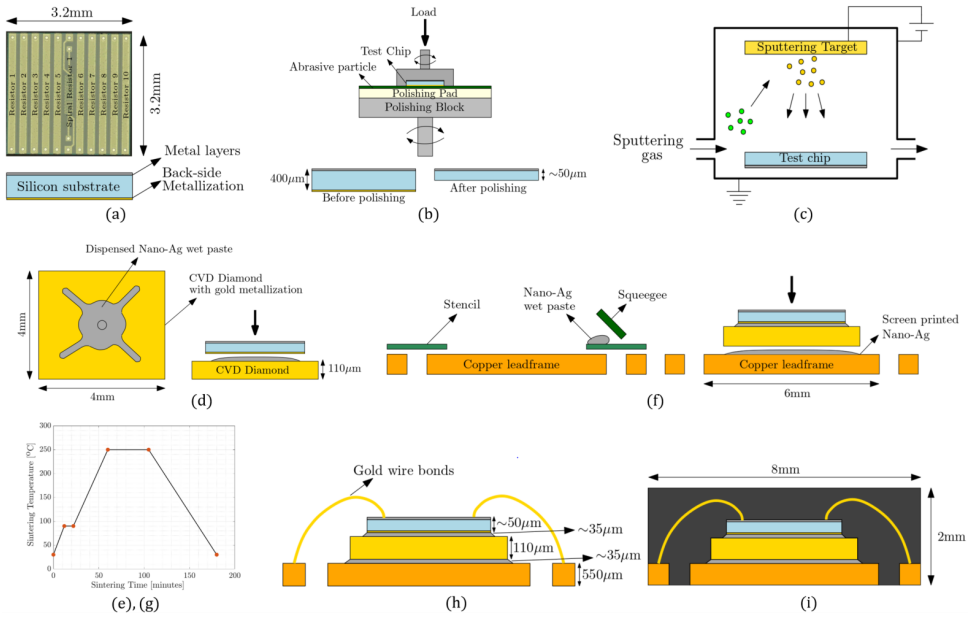

Figure 6.5: (a) A Schematic of a TTC's geometry and different layers. (b) The thickness of the TTCs were reduced from 400μm to 50μm by back-side polishing process. (c) The backside of the test chip was metalized with Ti/Pt/Au of 100/200/600nm by sputtering. (d) Nano-Ag paste was dispensed on the Diamond slabs (also coated with Ti/Pt/Au of 100/200/600nm), and the metalized TTCs were placed using a die-bonder. (e) The wet-mounted TTC with the Diamond is sintered using a pressureless sintering process in a nitrogen-filled chamber of a sintering oven. (f) The Sintered Die-Diamond stack is then assembled on a lead frame with a nano-Ag paste screen printed on it. (g) The complete stack is sintered again by a pressureless sintering process. The sintered layer thicknesses are in the range of ~35μm. (h) The sintered samples are then wire-bonded with a 99.99% pure gold wire-bonds of 25μm thickness with a bond bump of 50μm. (i) The final stage of the assembly process involves transfer molding with an epoxy molding compound.

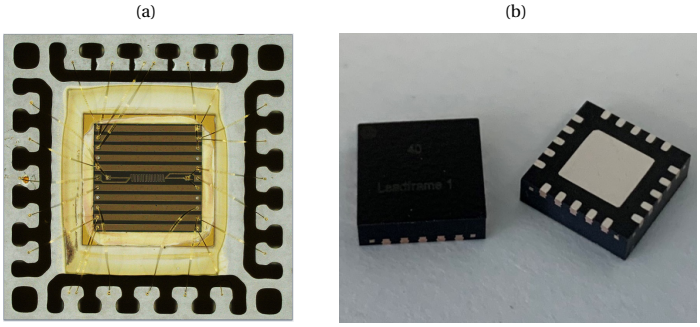

Figure 6.6: (a) An optical micrograph of the TTC with a Diamond heat spreader sintered to the die-pad of the lead frame. Electrical connections to the chip are established by wire bonds connecting the chip to the package bond pads. (b) Final optimized thermally enhanced PQFN packages are over-molded and singluated.

was sintered by a pressureless sintering process under Nitrogen. The sintering process happens in multiple stages; The first stage is the pre-sintering stage, during which the solvent evaporates, leaving behind nano-Ag particles. The second stage is the sintering stage, during which the particles agglomerate. The matching CTE of the Die-Diamond favors sintering with lower thermo-mechanical stresses on the interface. The subsequent step involves screen printing of the nano-Ag paste to the die pad of the copper lead frame, and the sintered die-diamond stack is wet mounted. The complete stack is sintered again with a similar pressureless sintering process under Nitrogen. The sintered interface thicknesses are in the range of ~35μm, which is based on the dispensed volume, the stencil thickness, and the material shrinkage.

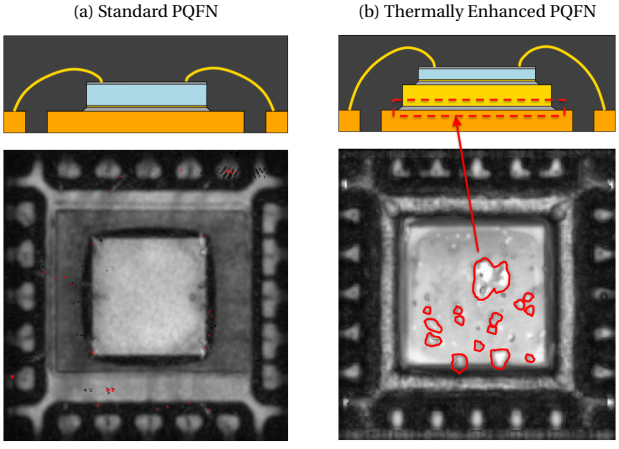

Figure 6.7: (a) CSAM imaging of the standard PQFN (400μm TTC without heat spreader) indicates a homogeneous interface. (b) CSAM imaging of the thermally enhanced PQFN (50μm TTC with 110μm heat spreader) highlights the presence of voids in the Diamond-Lead frame interface (highlighted in red).

After sintering, the electrical connections to the test chips are established using 99.99% pure gold wire bonds with 25μm bond wire and 50μm bond bump. An optical micrograph of the complete stack with wire bonds is shown in figure 6.6a. Due to the limitation of the bond pads of the lead frame (20 pads), only resistors (1-3, 5-6, 8-10) and the spiral resistor (figure 6.2a) are electrically connected. The resistors 2, 9, and the spiral resistor are connected with 4-point connections up to the TTC. The resistors 1, 3-8, and 10 are connected with 4-point Kelvin contacts until the bond pad of the lead frame. Once wire-bonded, the complete stack with the wire bonds is transfer molded with an epoxy molding compound and singulated into separate PQFN packages as shown in figure 6.6b. The singulated packages are then soldered to a test board (figure 6.2c) using a SAC305 solder paste.

Standard PQFN packages (chip thickness 400μm without heat spreader) were also made in a similar processing condition to quantitatively analyze the heat spreading effects. Confocal Scanning Acoustic Microscopy (CSAM) analysis was conducted on standard PQFN and thermally enhanced PQFN to evaluate the package integrity (figure 6.7). Comparing the CSAM results of the standard PQFN (figure 6.7a) and thermally enhanced PQFN (figure 6.7b), it can be observed that the latter has voids (highlighted in red) in the interface material, i.e., in the nano-Ag sinter layer. From CSAM analysis, the location of voids was found to be in the Diamond-Leadframe interface. The presence of voids can be avoided by improving the sintering process. Nevertheless, the performance of the thermally enhanced PQFN can be assessed and compared against the standard PQFN despite the inhomogeneity in the interface layer.

6.3. EXPERIMENTAL RESULTS

The standard PQFN and the thermally enhanced PQFN packages were tested inside the temperature cycling oven, and the testing conditions are the same as explained in the simulations. An input power of 6.6W is applied at Resistor 1 (figure 6.2a) for a duration of 1 second, which corresponds to ~10.5W/mm^2 heat flux, and the device temperature was measured at 9 locations for a duration of 10 seconds. Multiple sourcing units are connected to Resistor 1 for simultaneous heating and measuring as depicted in figure 6.8a, whereas the Resistors 2-3, 5-6, 8-10, and the spiral resistor are connected with a single source for sensing application (figure 6.8b). The electrical resistance measurements were translated into thermal readings based on the temperature dependency shown in figure 6.2b.

The heat spreading effect is demonstrated by measuring the device temperature at ambient room conditions (25^{o}C), and the experimental results are shown in figure 6.9. The results (figure 6.9) shown is an average of two devices per package type. The maximum device junction temperature and the minimum temperature are highlighted in figures 6.9a & 6.9c. Comparing the standard PQFN against the thermally enhanced PQFN, the following are the significant differences observed:

- The maximum device junction temperature (figure 6.9a & 6.9c) shows a ~9.6% reduction with the thermally enhanced PQFN as compared to the standard PQFN.

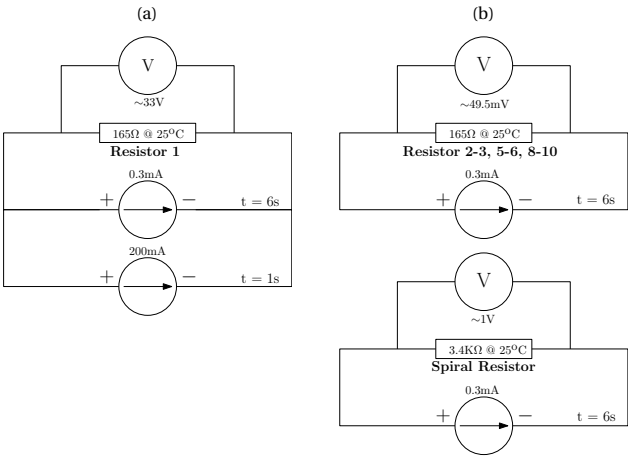

Figure 6.8: (a) The electrical circuit of Resistor 1 is connected to two source units for simultaneous heating and sensing. (b) The electrical circuit of Resistor 2-3, 5-6, 8-10 (top), and spiral resistor (bottom) is connected to a single source unit for sensing application only. (a) and (b) The measurement current (0.3mA) was chosen accordingly to avoid self-heating effects.

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- Likewise, the minimum device temperature (figure 6.9a & 6.9c) indicates that the heat spreader redistributes the heat along the device surface, resulting in a lower thermal gradient. The same can be visually seen in figure 6.9b & 6.9d.

Subsequently, the thermal performance of the regular PQFN and the thermally enhanced PQFN were measured at different input power from 1.65W to 6.6W. The percentage reduction in the device junction temperature was chosen as a metric to compare the heat-spreading effect as a function of the input power (figure 6.10a). The experimental measurements highlight that the percentage reduction in the junction temperature is strongly dependent on the applied heat input. An increase in the percentage from 3.57% to 9.6% was observed for the input power range from 1.65W to 6.6W (figure 6.10a). Similar dependence was also observed from simulations. However, semiconductor materials such as Silicon and Diamond have non-negligible temperature-dependent thermal properties, which need to be considered. Hence, the dependence of the percentage reduction in the junction temperature to its input power was simulated by considering the temperature-dependent properties of Silicon and Diamond. The effect of convective heat transfer to the environment was also included for the Overmold and the PCB. The simulation results are shown in figure 6.10b with a tabulation of the temperature-dependent properties and the convective heat transfer coefficient used in the simulation.

The transient thermal simulation results (figure 6.10b) indicate an increasing trend in the percentage reduction of the junction temperature as a function of input power (1.65W to 10W) as observed from the experiments. However, simulation results depict a much higher percentage reduction in junction temperatures (figure 6.10b) than the experimental measurements (especially at a low power range). The primary reason for the mismatch between the simulation and experimental results is the overestimation of the contact

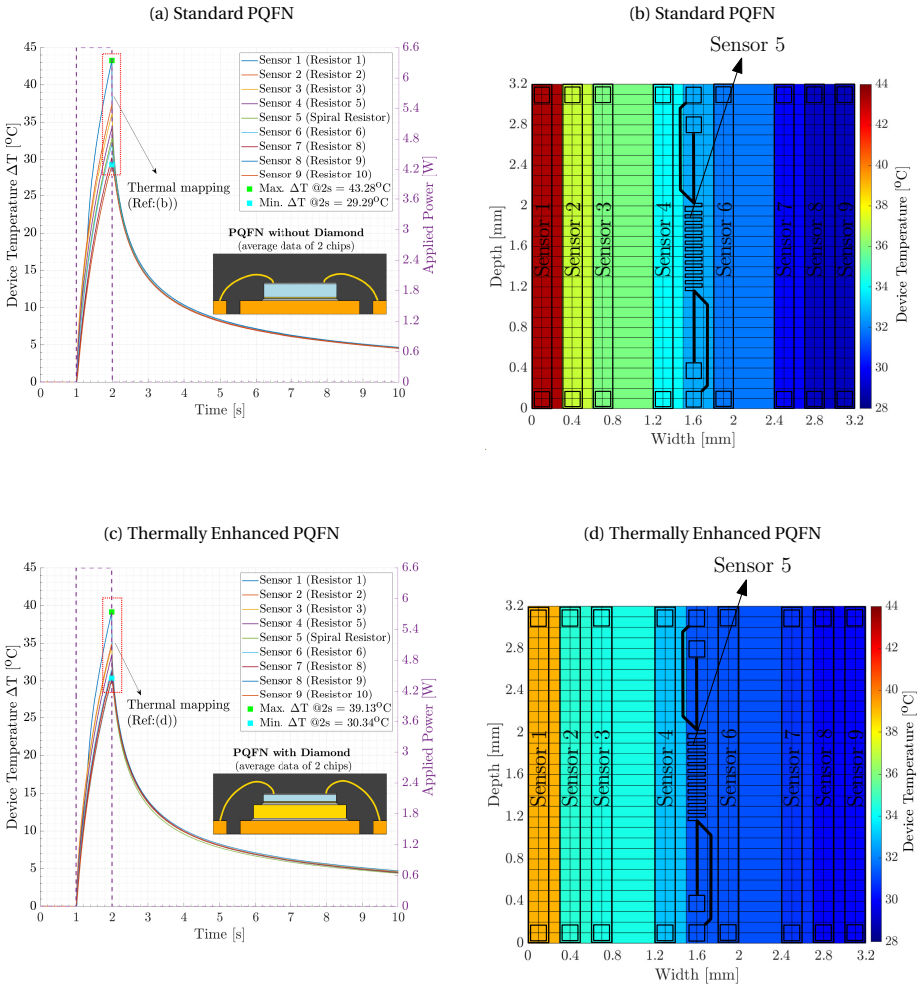

Figure 6.9: (a) & (c) The device temperature ΔT measured (@25°C) at nine locations are shown (left axis) along with the power input (right axis). A maximum junction temperature (Max. ΔT) of 43.28°C is recorded for the standard PQFN, which is reduced to 39.13°C (~9.6% lower) for the thermally enhanced PQFN. Likewise, the standard PQFN records a minimum temperature (Min. ΔT @t = 2s) of 29.29°C, as compared to 30.34°C with the thermally enhanced PQFN. This shows that the standard PQFN concentrates the heat, and the thermally enhanced PQFN redistributes the heat. (b) & (d) The device temperature measured at t = 2s is mapped along the surface of the device for visual representation.

thermal resistances in the simulation. CSAM imaging of the thermally enhanced PQFN (figure 6.7b) indicated the presence of voids, which results in higher thermal resistance. To evaluate the influence of the contact thermal resistance, the junction temperature of the thermally enhanced PQFN was simulated as a function of Die-Diamond and Diamond-Leadframe interface thermal conductivity. The simulation results are shown in figure 6.10c, and it is evident that the contact heat transfer coefficient parameter has a significant influence, especially for conductivity values lower than 100W/mK. Poor interface

(a) Percentage reduction in Junction temperature as a function of applied heat input was experimentally measured for four different power inputs from 1W to 7W range. The efficiency of the heat spreader is observed to increase with increasing power input. Hence, the cost of developing thermally enhanced packages is truly beneficial for high-power applications.

(b) Percentage reduction in Junction temperature as a function of applied heat input was simulated from 1W to 10W power range. The transient thermal results were simulated using the temperature-dependent material properties of Silicon and Diamond. The effect of convective heat transfer on the environment was also included in the simulation. The simulation results validate the claim from the experimental measurements on the effect of heat spreader efficiency increases with increasing power.

(c) The influence of the interface contact resistance was simulated by varying the contact heat transfer coefficient between the Die-Diamond and the Diamond-Leadframe interface. It can be observed that there is a significant difference in the device junction temperature for interface thermal conductivity less than 100W/mK. The simulation included the temperature-dependent properties and the convective heat transfer coefficient shown in (b).

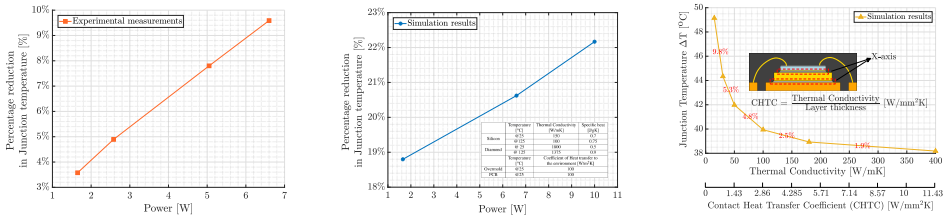

Figure 6.10: (a)-experimental and (b)-simulation explains the influence of the applied power input on the heat spreading effect. (c) highlights the influence of interface resistance as a barrier to transport heat. It is evident that simulated results depict similar responses to the experimental results. However, the absolute values in the simulations don't match the experiments due to the overestimation of the interface resistance in the simulation and the mismatch in the thermal properties between the simulation and experiments.

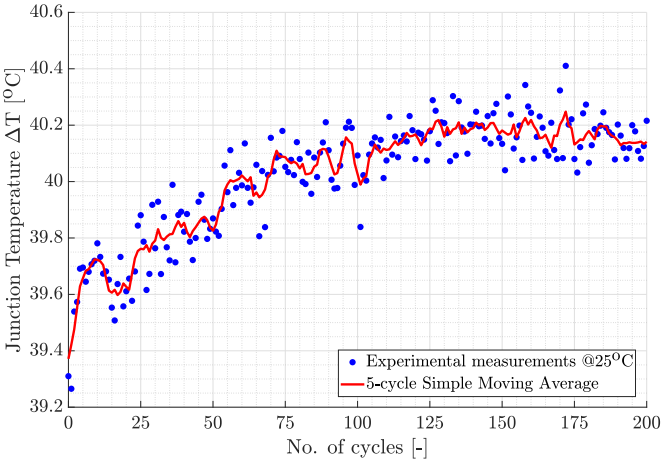

Figure 6.11: The reliability of a thermally enhanced PQFN was tested by thermal cycling from −55°C to 150°C.The devices were first calibrated to the measurement conditions, and the experimental data was averaged using a Simple Moving Average. The percentage of thermal degradation after two hundred cycles is observed to be less than 2%.

contacts decrease the efficiency of the heat spreader, which emphasizes the need for more research on interface materials in power packaging applications.

Furthermore, the reliability of the thermally enhanced PQFN was assessed by thermal cycling from −55°C to 150°C. During every cycle, the Junction temperature was in-situ measured at 25°C (figure 6.11). The measurement results are plotted with a 5-cycle Simple Moving Average, and signs of degradation due to continuous stress testing can be observed. The junction temperature has increased by ~1.95% after two hundred thermal cycles as compared to its initial state. Yet the Junction temperature of the thermally enhanced package after two hundred cycles is ~7.25% lower than the junction temperature of the standard package at 0-cycle (figure 6.9a).

6.4. CONCLUSION

The effect of the diamond heat spreader in high-power applications and the importance of tuning the semiconductor substrate and the heat spreader thicknesses are empirically analyzed in this research. A thermal test chip was used to characterize the heat-spreading effect. A heterogeneous integration approach was adapted for developing passive heat spreaders on thinned-down active devices. Accordingly, a thermally enhanced PQFN package was realized, and its performance was experimentally measured and compared against a standard PQFN package (without a heat spreader).

- For an applied input power of 6.6W, the thermally enhanced PQFN provides ~9.6% reduction in Junction temperature as compared to a standard PQFN.
- A more uniform distribution of heat is observed with the thermally enhanced PQFN due to the presence of a heat spreader. Meanwhile, the standard PQFN has concentrated heat sources.
- The percentage reduction in the junction temperature has a strong dependence on the applied heat input. Hence, the efficiency of a diamond heat spreader scales with the input power.
- Package degradation is inevitable. The thermally enhanced PQFN shows around 2% thermal degradation due to temperature cycling from −55°C to 150°C over two hundred cycles. Yet, the Junction temperature measured after two hundred cycles is ~7.25% lower than the junction temperature of the standard package at 0-cycle.

Advanced thermal solutions are needed to enhance the packaged device's performance, and the diamond's superior properties have proven beneficial. Besides, the cost of manufacturing CVD diamonds is decreasing due to technological advancements, whereas the thermal issues in high-power electronics are increasing, especially in harsh applications. Hence, the benefits of incorporating diamonds in high-power electronics are evident despite its cost. Furthermore, the beneficial properties of diamonds attract future research toward multi-chip high-power packaging applications.

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7

Co-Packaging Electronics with Microfluidics for Power Electronics Application

Co-packaging electronics with microfluidics is a promising solution to the global thermal management challenges in high-power, high-density devices. Traditional power devices rely on module-level heat sinks with substantial coolant volumes. In contrast, recent advancements focus on complex processes to integrate cooling techniques within semiconductor substrates (silicon). Our innovative approach embeds microchannels onto the passive electronic package substrate (leadframe), eliminating the need for external cooling components and reliance on front-end fabrication. Here, we demonstrate integrating a serpentine microchannel network within a 6mm x 6mm footprint of a leadframe. The package performance was tested up to ~213W/cm^2 heat flux, limiting the maximum steady-state junction temperature to ~300^{o}C. The co-packaged device demonstrated a six-fold increase in power rating and a seven-fold reduction in junction-to-ambient thermal resistance compared to conventional packages with bulk copper substrates. Likewise, the proposed solution outperformed packages mounted onto liquid-cooled heat sinks, doubling the power rating and halving the thermal resistance while consuming only a fraction of the coolant volume. We anticipate this approach applies to lateral and vertical transistor configurations, provided the coolant is electrically isolated to prevent parasitic losses. This scalable and efficient solution addresses the thermal management challenges in high-power electronics across various applications.

7.1. Introduction

The drive towards miniaturization and increasing power density exacerbated the thermal management challenges in electronics. Power inverters in Electric Vehicles (EVs) experience temperature fluctuations exceeding >110°C, and heat flux ranges from ~100W/cm^2 to ~1000W/cm^2 [1, 2]. Prolonged exposures to heightened temperatures reduce device lifespan and compromise system efficiency and performance. Wang et al. [3] reported up to ~55% failures in power converters are due to thermal stresses. Consequently, the global demand for thermal management technologies is expected to reach USD 8.9 billion by 2024 [4], driven primarily by automotive EVs, telecommunication devices, consumer electronics, and high-performance computing applications. In the automotive sector, traction inverters and rectifiers predominantly rely on single-phase liquid-cooled heat sinks.

- **2016 Chevrolet Volt:** Utilizes a double-side cooled IGBT module with copper heat sinks (Metal Injected Molded) developed by Delphi Technologies [5–7].
- **Fourth-generation Toyota Prius:** Features a resin-molded IGBT module integrated into a double-side cooled heat exchanger with thermal grease [5, 8].
- **2012 Nissan Leaf:** Employs a serpentine-structured cooling channel with water ethylene glycol coolant. The IGBT modules are mounted on a cast-aluminum cold plate with a dielectric pad for electrical isolation and a Thermal Interface Material (TIM) [5, 9].
- **2014 Honda Accord:** Uses metalized-ceramic (DBC) substrates for electrical isolation of its IGBT inverter modules, mounted without TIM onto an intricate finned-structured cold plate [5, 9].
- **2015 Tesla Model-S 70D:** Features 36-paralleled TO-247 discrete package IGBTs with an internal cavity heat sink for liquid cooling [5, 10].

While module-level liquid-cooled heat sinks are widely used in automotive inverters, they are bulky, expensive, require large coolant volumes, and are not an integral part of the power device. For instance, the inverter module in Tesla Model S 2015 weighs 5.8 kilograms and requires 6.4 liters of coolant [5]. In contrast, recent advancements in cooling technologies have shifted towards chip-level integration, though this introduces significant fabrication complexity. [11, 12] demonstrated co-designing a GaN-on-Silicon AC-DC converter with monolithically integrated microchannels on a passive silicon substrate. Although chip-level integration provides distinct thermal management benefits, it necessitates wafer-level, front-end fabrication processes. Similarly, researchers at TSMC developed a direct silicon water-cooling solution by bonding an external silicon lid onto a silicon substrate [13]. Further insights into single-phase cooling concepts and thermal management challenges are provided in [14–19], while cooling based on phase-transition (liquid to vapor) and phase-change materials are discussed in [20–23].

This paper presents a novel co-packaging approach that integrates microfluidic cooling directly onto the package substrate (leadframe), offering a compact, efficient, and

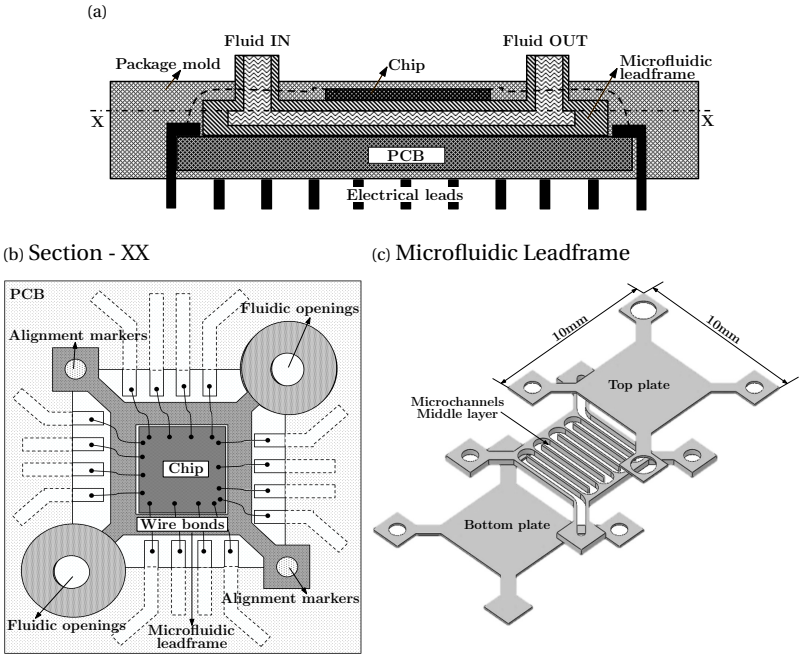

Figure 7.1: Conceptual co-packaged electronics with microfluidics schematic.

easy-to-manufacture solution (see figure 7.1). By co-packaging electronics and microfluidics, we aim to overcome the limitations of traditional cooling methods and offer the following key advancements:

- **Rapid thermal response:** Achieves a steady-state junction temperature within 20seconds under a maximum heat flux of ~213W/cm^2, utilizing only ~2ml of demineralized water as coolant.
- **Improved power rating:** Demonstrates a sixfold increase in device power rating compared to a standard package with natural convection and twice that of conventional heat sink cooling technology, while the maximum junction temperature capped at 300^{o}C.
- **Improved thermal efficiency:** Reduces total system thermal resistance (junction-to-ambient) by a factor of seven compared to a standard package and by half compared to heat sink cooling.
- **High heat transfer efficiency:** Achieves a high Nusselt number of 6.77 with a flow rate of 200μl/s.

The following section presents the performance and heat transfer efficiency of the proposed co-packaging approach of integrating electronics with microfluidics compared to standard packages with natural convection cooling and external water-cooled heat sinks. Subsequently, concluding remarks on the proposed approach are presented with

suggestions for future improvements. Finally, the methods section demonstrates the design and assembly of the microfluidic package.

7.2. MICROFLUIDIC PACKAGE: DESIGN AND ASSEMBLY

The design and assembly of a microfluidic package involves the following steps: (A.) Selection of semiconductor device, (B.) Design and fabrication of microfluidic leadframe, and (C.) Package assembly processes.

7.2.1. SELECTION OF SEMICONDUCTOR DEVICE

The choice of semiconductor device is crucial to demonstrate the effectiveness of the microfluidic package. Thermal Test Chips (TTC) are specialized devices fabricated using the same process technology as semiconductor devices. The design and development of TTCs can be found in [24, 25]. The TTC used in this study is a commercially available Silicon-based lateral device with integrated heating and temperature-sensing elements (see figure 7.2a). Each heating element has a resistance of 165Ω @25°C, and the Resistance-based Temperature Detector (RTD) features a 4-point probe configuration with 3.7kΩ @25°C.

The temperature sensitivity of the TTC was determined through a two-step calibration process. For RTD resistance calibration below 150°C, the TTCs were measured inside an oven at different ambient temperatures. For temperatures above 150°C, an input power of 3W was applied to the heaters by connecting all heating elements in parallel, and the change in RTD resistance was measured while simultaneously measuring the device junction temperature using an Infra-Red (IR) camera. The measured RTD resistance and

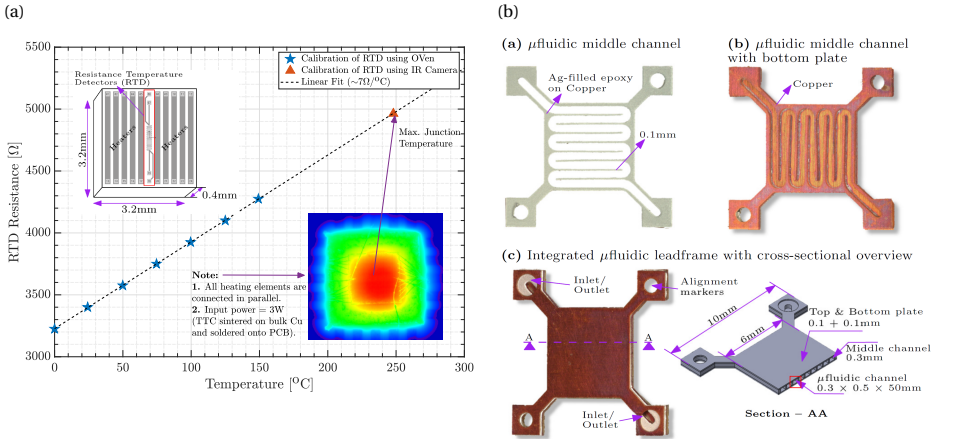

Figure 7.2: (a) Two-step calibration process: Calibration of RTD resistance at different ambient temperatures using an oven and calibration based on self-heating and recording the temperature using an IR camera. (b) An overview of microfluidic leadframe assembly. (a) Microfluidic middle channel laser cut from copper with a minimum feature size of 0.1mm. The surface of the channel is deposited with conductive Ag-filled epoxy glue for adhesion to the top and bottom plate. (b) Glued middle channel with bottom plate. (c) Glued top plate to complete the microfluidic leadframe assembly. A 3D cross-sectional view is provided with dimensional details.

the junction temperature were in a steady state. A linear relationship was established by fitting both calibration measurements, resulting in a sensitivity of ~7Ω/°C (see figure 7.2a). For IR measurements, the TTC was sintered on a bulk copper substrate, which was further soldered onto a PCB and wire bonded. The backside of the TTC (Silicon substrate) is metalized with TiPtAu (100/100/100nm) to promote adhesion to the die-attach material.

7.2.2. DESIGN AND FABRICATION OF MICROFLUIDIC LEADFRAME

Inspired by the serpentine-structured cooling channel cold plate from 2012 Nissan Leaf IGBT modules [5, 9], this study employs a similar design for the microfluidic leadframe. While optimization of the microchannel geometry is beyond the scope of this work, the serpentine configuration is expected to induce localized turbulence, enhancing heat dissipation compared to straight channels. The microchannel dimensions were standardized at a width of 0.3mm and a height of 0.5mm, with a total channel length of ~50mm between the inlet and outlet.

The microfluidic leadframe prototype consists of three laser-cut copper layers: a 0.1mm top plate, a 0.3mm microchannel middle layer, and a 0.1mm bottom plate (see figure 7.2b). These layers were assembled using conductive Ag-filled epoxy adhesive. The microfluidic inlet and outlet were placed along the diagonals of the leadframe, with additional alignment markers positioned along the counter-diagonal for assembly.

7.2.3. PACKAGE ASSEMBLY PROCESSES

Conventional backend packaging encompasses three primary steps: die-bonding, wire-bonding, and over-molding. Two package configurations were assembled to evaluate the efficiency of the proposed solution:

- **Reference packages:** Utilizing a standard copper leadframe, and
- **Microfluidic packages:** Incorporating the designed microfluidic leadframe.

Ag-sintering was selected as the die-attach material due to its superior thermal conductivity compared to traditional solder alloys. The Ag-sinter paste was applied to the

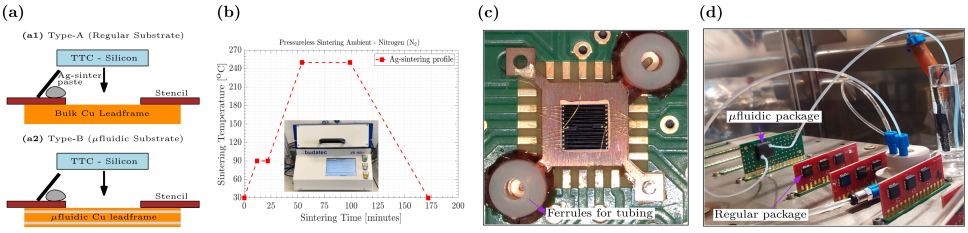

Figure 7.3: An overview of package assembly processes. (a) Stencil printing of Ag-sinter pastes on package substrate and die-placement. Two types of packages were assembled in this study: Type-A – Regular package with bulk copper leadframe and Type-B – Microfluidic package with microfluidic leadframe. (b) Sintering of Ag-paste under nitrogen. (c) Sintered TTC onto a microfluidic substrate, which is soldered onto a PCB and wire-bonded. Ferrules for inlet and outlet tubings are glued. (d) An indicative image of regular packages on PCBs and microfluidic packages with fluidic connections.

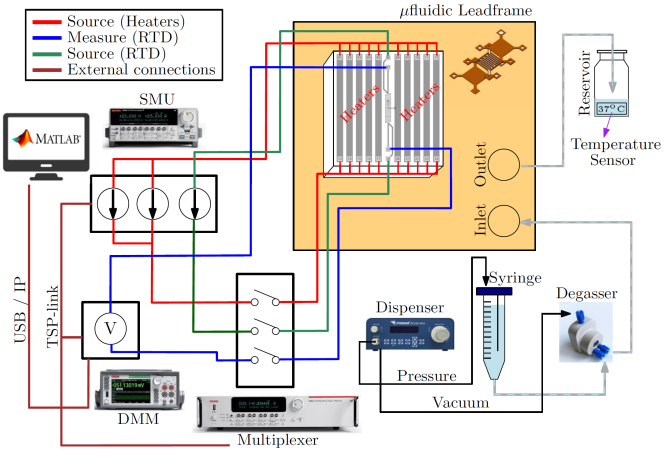

Figure 7.4: Schematic illustration of the electrical and microfluidic layout with different connections color-coded.

leadframe's die pad using stencil printing (see figure 7.3a). The TTC was then positioned on the wet paste and cured in a nitrogen atmosphere in a hot plate oven. The Ag-sintering profile is detailed in 7.3b. Following die bonding, the packages were soldered to a PCB and wire bonded (see figure 7.3c). To ensure uniform heating across the device, all heating elements on the TTC were connected in parallel. For microfluidic packages, inlet and outlet ferrules were secured using an adhesive. Finally, both package types were encapsulated with DAM and Fill encapsulants to provide environmental protection. A visual comparison between the standard Power QFN package and the microfluidic package is presented in Figure 7.3d.

7.3. EXPERIMENTAL SETUP AND DEVICE CHARACTERIZATION

To assess the performance of the co-packaged electronics with microfluidics, a dedicated experimental setup was developed, as illustrated schematically in figure 7.4. Devices soldered to a test board (PCB) were securely mounted in a test socket, enabling electrical connections between the TTC and the measurement equipment via a multiplexer. The input currents for the heaters were sourced using a parallelly connected Source Measurement Unit (SMU) with compliance of 40V up to 2A continuous current. The change in RTD resistance was measured using a Digital MultiMeter (DMM), which has a resolution of 1μV for measurements up to 10V and an accuracy of ±0.1mV. The SMU, DMM, and Multiplexer were synchronized through a Trigger Synchronization and Communication (TSP) protocol, and the measurement sequence was programmed using a user-defined MATLAB program.

An open-loop microfluidic system was implemented to evaluate the cooling performance. A pressure dispenser with a maximum pressure of 675kPa was connected to a 10ml syringe carrying demineralized water as the coolant. Inlet coolant temperature was

recorded, and the fluid was subsequently passed through a 300μl degasser to eliminate air bubbles. The degasser removes air bubbles from the fluid, preventing blockage and localized explosions. The fluid outlet was collected in a reservoir, and the outlet temperature was measured with a thermocouple at one millisecond intervals. The pressure drop across the microfluidic system was not measured.

As previously outlined, two distinct package configurations were fabricated: standard leadframe packages and microfluidic leadframe packages. To facilitate comparative analysis, three experimental test cases were defined (see figure 7.5):

- **Test Case – A:** Reference PQFN package with a standard leadframe and natural convection cooling,
- **Test Case – B:** Reference PQFN package with a standard leadframe mounted on a water-cooled (demineralized) copper heat sink using thermal interface material (TIM), and
- **Test Case – C:** PQFN package with a water-cooled (demineralized) microfluidic leadframe.

Considering the epoxy encapsulant's glass transition temperature below 180^{o}C and the target maximum test temperature approaching the PCB solder reflow temperature (~300^{o}C), over-molding was excluded from the experimental protocol. To assess package performance, the junction temperature of the test chip was monitored until thermal equilibrium (steady state) was achieved for each test case (see figure 7.5). A constant power input of 2.64 W was applied across ten parallelly connected heaters, resulting in a power density of 25.78W/cm^2. Temperature variations over time are presented in figure 7.6a.

- **Test Case – A:** The reference PQFN package with a standard leadframe under ambient conditions reached a steady-state junction temperature of ~220^{o}C over 1000 seconds (see figure 7.6a).

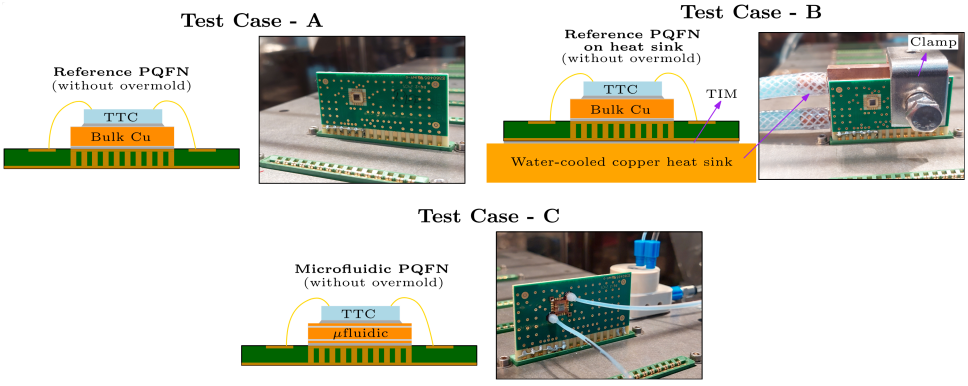

Figure 7.5: Overview of three different test cases with two package types assessed in this study. The tests were performed on samples without overmold.

- **Test Case – B:** The reference PQFN package mounted on a water-cooled heat sink attained a steady state junction temperature of ~78°C in 100 seconds. A constant flow rate of 30ml/s was maintained (see figure 7.6a).

- **Test Case – C:** The PQFN package with the microfluidic leadframe achieved a steady-state junction temperature of ~43°C in less than 20 seconds. The device was subjected to three different flow rates: 100μl/s, 150μl/s, and 200μl/s (see figure 7.6a). Due to lower thermal capacitance than standard lead frames, the microfluidic packages indicate a shift in time scale. Minimal junction temperature variations (±0.5°C) were observed at different flow rates for an applied power of 2.64W, likely due to insufficient heating.

The results depicted in figure 7.6a demonstrate the advantages of integrating microfluidics within the package compared to standard PQFN packages and conventional heat sink cooling technologies. Additional experiments are needed to better understand the performance enhancements offered by co-packaging electronics with microfluidics.

7.4. EXPERIMENTAL RESULTS

The experimental procedure was replicated using varying power inputs to the heating elements. The resulting steady-state junction temperature changes are presented in figure 7.6b. As previously noted, the maximum junction temperature was constrained to the solder reflow temperature of 300°C, limiting a maximum ΔT of 275°C in figure 7.6b. A linear regression line was fitted to the measured temperature changes as a function of input power, yielding the following observations:

- **Test Case – A:** The reference PQFN with ambient cooling resulted in a ΔT of ~275°C for power inputs less than 4W.

- **Test Case – B:** The reference PQFN with a water-cooled heat sink reached a ΔT of ~170°C at 5.9W input power. A maximum ΔT of 275°C can be reached at ~1OW, which indicates a three-fold increase in power input over Test Case – A.

- **Test Case – C:** The microfluidic package varies performance based on flow rate, with significant differences apparent at higher operating temperatures.

  - At a flow rate 100μl/s, a ΔT of ~275°C was achieved at a power input of ~22W, marking a six-fold increase compared to the reference and a two-fold improvement over the heat sink.

  - At a flow rate of 150μl/s and 200μl/s, a ΔT of ~275°C corresponds to power inputs of ~26W and ~27.5W, respectively.

The maximum power input for each test case at a ΔT of 275°C is summarized in table 7.1. The total thermal resistance of the system R_{total} was analyzed to evaluate the heat dissipation capability of the microfluidic packages. R_{total} is a summation of caloric

thermal resistance $R_{caloric}$, convective thermal resistance R_{conv}, and conductive thermal resistance R_{cond} (see equation 7.1).

$$R_{total} = R_{caloric} + R_{conv} + R_{cond} \tag{7.1}$$

The total junction-to-ambient thermal resistance R_{total} can be determined using equation 7.2, which corresponds to the slope of the linear line shown in figure 7.6b.

$$R_{total} = \frac{\Delta T_J}{\Delta P_{in}} \tag{7.2}$$

To quantify the caloric thermal resistance $R_{caloric}$ of the water, the change in water temperature (ΔT_{water}) was determined by subtracting the inlet temperature from the maximum outlet temperature for various heater power inputs. The results are shown in figure 7.6c. It is important to note that while the inlet water temperature is in thermal equilibrium, the outlet temperature exhibits a transient behavior, though the device junction reached a thermal equilibrium. Therefore, the maximum outlet temperature was considered. A linear relationship between ΔT_{water} and input power was observed with $R_{caloric}$ corresponding to the slope of the linear line, as expressed in equation 7.3.

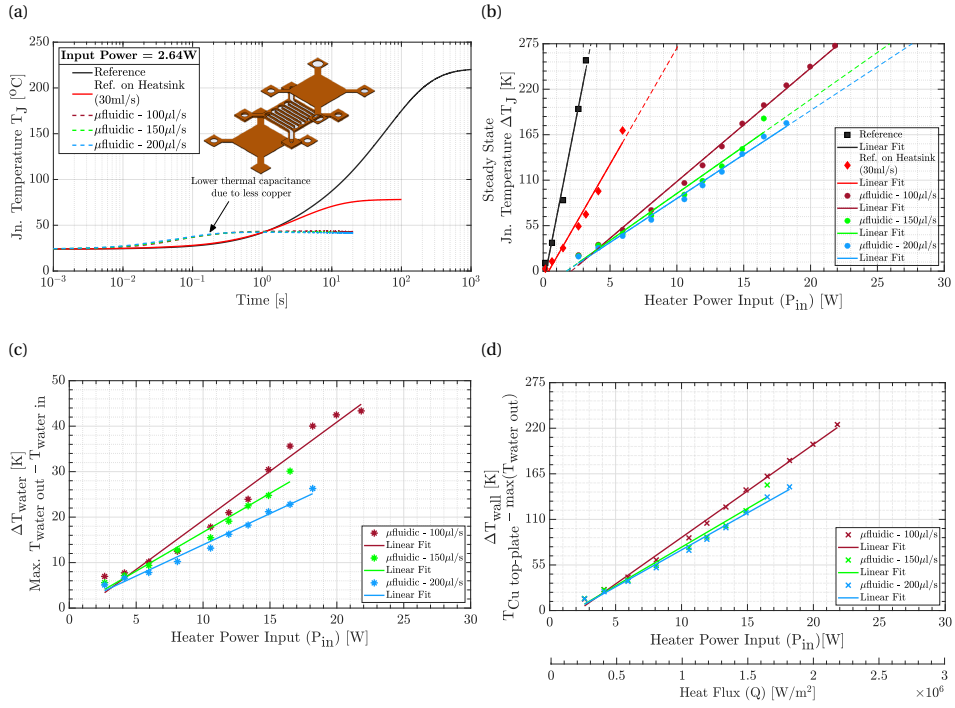

Figure 7.6: (a) Transient to steady-state temperature measurement over time for all three test cases. (b) Change in TTC surface temperature at steady state, (c) difference in water temperature, and (d) difference in wall temperature is shown for varied heater power input. A linear relationship was established for each test case.

$$R_{caloric} = \frac{\Delta T_{water}}{\Delta P_{in}} \tag{7.3}$$

To determine the convective thermal resistance R_{conv}, the temperature difference across the wall ΔT_{wall} needs to be calculated. A one-dimensional heat transfer model was assumed between the TTC and the microfluidic top plate, as depicted in figure 7.7. Neglecting ambient heat transfer and contact resistances, the heat transfer network can be represented by equation 7.4:

$$Q = \frac{-k_1(T_2 - T_J)}{L_1} = \frac{-k_2(T_3 - T_2)}{L_2} = \frac{-k_3(T_4 - T_3)}{L_3} \tag{7.4}$$

The wall temperature difference, ΔT_{wall}, was calculated as the difference between the top copper plate temperature (T_4) and the maximum water outlet temperature (see figure 7.6d). Subsequently, R_{conv}, was derived from equation 7.5, which represents the slope of the linear line in figure 7.6d.

$$R_{conv} = \frac{\Delta T_{wall}}{\Delta P_{in}} \tag{7.5}$$

Given the calculated values of R_{total}, $R_{caloric}$, and R_{conv}, the conductive thermal resistance, R_{cond}, was determined using equation 7.1. The results are presented in figure 7.8 and summarized in table 7.1. The analysis revealed that convective thermal resistance (R_{conv}) significantly contributes to the overall thermal resistance of the system R_{total}, while conductive resistance R_{cond} remains relatively constant and less influential. Reducing R_{conv} by modifying the fluid velocity, fluid properties, or active heat transfer area is essential to optimize the system. To further characterize the cooling performance, the fluid flow regime was analyzed. In typical single-phase microfluidic systems, laminar flow patterns are predominant. The dimensionless Reynolds number (Re) was calculated to assess the flow conditions. A Reynolds number exceeding 1800 to 2100 signifies the transition from laminar to turbulent flow [26]. For flow through a pipe, the Reynolds number is

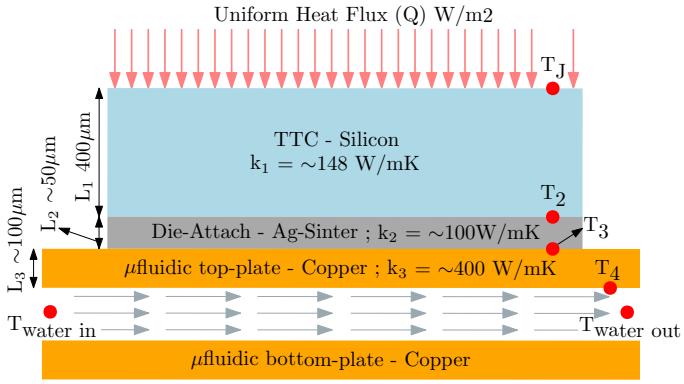

Figure 7.7: Schematic illustration of input heat flux applied onto the Silicon surface with geometrical and material parameters of various layers.

determined from equation 7.6, where ρ is the fluid density (ρ_{water} = 1000 kg/m^3), v is the fluid velocity (m/s), D_H is the hydraulic diameter of the microchannel (m), and μ denotes the dynamic viscosity of the fluid in ($\mu_{water} = 1 \times 10^{-3}$ kg/m·s [27]).

$$Re = \frac{\rho v D_H}{\mu} \tag{7.6}$$

The fluid velocity was determined from the volumetric flow rate (in m^3/s) and the microchannel cross-sectional area (see figure 7.2bc). The hydraulic diameter of the channel is given by $D_H = \frac{4wh}{2(w+h)}$, where w is the channel width, and h is the channel height (see figure 7.2bc). Based on these calculations, the Reynolds numbers for different flow rates were found to be:

- Re = 250 for a flow rate of 100μl/s,
- Re = 375 for a flow rate of 150μl/s, and
- Re = 500 for a flow rate of 200μl/s.

The fluid velocity and the obtained Reynolds numbers for all three flow rates are summarized in table 7.1. These values indicate that the flow remains laminar under all tested conditions. However, it is important to know that the serpentine channel design might induce localized turbulence within the fluidic substrate.

To evaluate heat transfer efficiency, the dimensionless Nusselt number was calculated using equation 7.7, where h is the convective heat transfer coefficient in W/m^{2}K, and k is

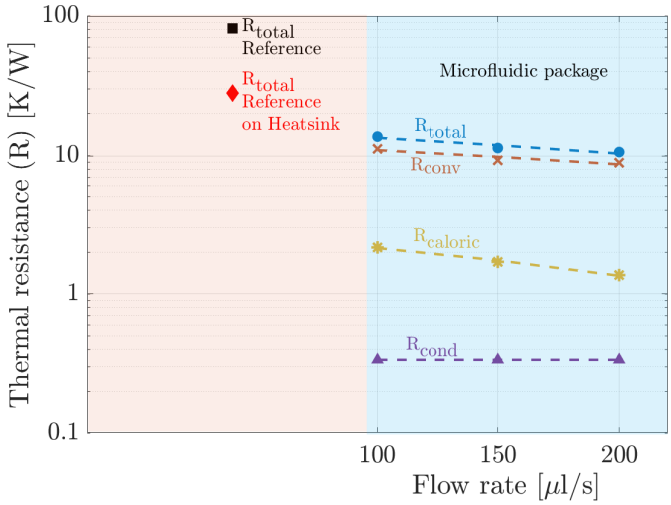

Figure 7.8: A comparison of total thermal resistance R_{total} for reference PQFN, reference PQFN on a heat sink, and microfluidic packages are shown. The contribution of convective R_{conv}, conductive R_{cond}, and caloric $R_{caloric}$ thermal resistances is also shown for microfluidic packages. The graph is displayed in log-normal to highlight the differences.

the thermal conductivity of the fluid (k_{water} = 0.6065 W/(m·K) [28]). Nusselt number is the ratio of the total heat transfer to fluid conductive heat transfer. A Nusselt number of 1 would indicate conduction-dominated heat transfer. For fully developed laminar velocity profiles in non-circular pipes, the Nusselt number ranges less than ten [29].

$$Nu = \frac{\text{Total heat transfer}}{\text{Fluid conduction heat transfer}} = \frac{h \cdot D_H}{k} \tag{7.7}$$

The convective coefficient was determined by dividing the input heat flux by the wall temperature difference, as shown in equation 7.8.

$$h = \frac{Q}{\Delta T_{wall}} \tag{7.8}$$

This coefficient corresponds to the inverse slope of the fitted line in figure 7.6d, where heat flux is plotted against the wall temperature difference. The calculated Nusselt numbers are as follows:

- Nu = 5.38 for a flow rate of 100μl/s,
- Nu = 6.48 for a flow rate of 150μl/s, and
- Nu = 6.77 for a flow rate of 200μl/s.

The Nusselt numbers obtained indicate that convective heat transfer through the fluid is more dominant than conductive heat transfer, emphasizing the benefits of microfluidic integration within the package. The convective coefficient and the Nusselt numbers are summarized in table 7.1. While [11] reports Nusselt numbers ranging from 2.6 to 6.5 for straight-parallel microchannels on semiconductor substrates and a maximum of 16 for monolithic manifold microchannels, these configurations require complex fabrication

Tab.1: A comparative summary of experimental results for all three test cases.

	Test Case – A (Reference)	**Test Case – B (Ref. on HS)**	**Test Case – C (Microfluidic package)**		
			100ul/s	**150ul/s**	**200ul/s**
Max. P_{in} [W] @T_j = 300°C	3.5	10	22	26	27.5
R_{total} [K/W]	81.68	28.14	13.72	11.37	10.63
$R_{caloric}$ [K/W]	-	-	2.16	1.71	1.37
R_{conv} [K/W]	-	-	11.22	9.32	8.92
R_{cond} [K/W]	-	-	0.337	0.337	0.337
Fluid velocity [m/s]	-	-	0.67	1	1.33
Reynolds number [-]	-	-	250	375	500
Convective Heat transfer coefficient [W/m^{2}K]	-	-	8702	10474	10943
Nusselt number [-]	-	-	5.38	6.48	6.77

processes. The current study demonstrates a more straightforward, industry-compatible co-packaging approach with a relatively high Nusselt number (Nu = 6.77). In summary, this research demonstrates the potential of co-packaging electronics with microfluidics to improve device power ratings, reduce thermal resistance, and establish controlled laminar flow with dominant convective heat transfer through conventional backend packaging processes.

7.5. DISCUSSIONS AND CONCLUSIONS

This study introduced a novel co-packaging approach by integrating microfluidics within electronic package substrates (leadframes) to address thermal management challenges. Conventional cooling technologies for automotive power inverters rely on bulky external liquid-cooled heat sinks that require substantial coolant volume. In contrast, state-of-the-art (SOA) technologies focus on integrating microfluidics onto semiconductor substrates, less likely to be commercialized due to their economics and reliance on complex front-end cleanroom fabrication. The proposed methodology demonstrated a sixfold increase in power handling capacity and a sevenfold reduction in thermal resistance compared to a standard package in convective ambient cooling. Likewise, the proposed methodology outperformed standard packages mounted onto external water-cooled heat sinks by doubling its power rating and halving thermal resistance while consuming considerably less coolant. The co-packaged device indicated a high heat transfer efficiency with a Nusselt number of 6.77, which is on par with straight-parallel microchannels integrated on semiconductor substrates shown in [11]. We also noticed that by modifying the fluid velocity, fluid properties, and the active heat transfer area, the convective thermal resistance can be reduced, further improving the heat transfer efficiency.

While this study established the proof-of-concept, future research should focus on optimizing the microchannel design and exploring different materials and fabrication techniques. For instance, simplifying the three-layered substrate into a two-layered substrate with half-etched microchannels bonded using laser welding is recommended. Furthermore, fluid delivery in real-life applications could be implemented through PCBs or external systems similar to current automotive inverter module cooling technology. Besides, we anticipate that the co-packaging approach is not limited to lateral semiconductors but also to vertical devices provided, the coolant needs to be electrically isolated to avoid parasitic losses. The successful integration of microfluidics into electronic packaging holds immense potential for addressing the thermal challenges faced by high-power electronic devices across various applications. By enabling efficient and compact cooling solutions, the co-packaging approach can contribute to developing more reliable and sustainable electronics.

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8

CONCLUSION

8.1. OVERVIEW OF RESEARCH FINDINGS

This dissertation has demonstrated several advancements in prognostics and thermal management of power electronic packages. By focusing on early fault detection, material characterization, and innovative thermal solutions, this research aimed to improve power electronic systems' overall performance and longevity.

- Chapter 1 provided an outlook on the current state of power semiconductor devices, field-critical applications, dominant degradation mechanisms, and emerging measurement techniques for condition monitoring.
- Chapter 2 introduced a non-intrusive methodology for continuously monitoring the package's thermal performance during operation that applies to real-life scenarios.
- Chapter 3 provided insights on four distinct silver sintered materials, each varying in material composition and process condition, by co-relating the package performance degradation to die-attach interface behavior.
- Chapter 4 demonstrated the robustness of hybrid silver sintering materials with stress-absorbing polymers according to Grade-0 Automotive standard reliability test requirements.
- Chapter 5 introduced a novel methodology for characterizing the thermal properties of sintered silver interfaces with appropriate form factors for semiconductor packaging applications.
- Chapter 6 explored a heterogeneous method of integrating diamond heat spreaders onto semiconductor substrates through back-end packaging processes, demonstrating a reduction in concentrated thermal hot spots.
- Chapter 7 introduced a novel co-packaging approach of integrating electronics with microfluidics on a package level and offering a compact, efficient, and easy-to-manufacture solution.

8.2. SCIENTIFIC CONTRIBUTIONS AND SOCIETAL IMPLICATIONS

The scientific contributions of this research are multifaceted, extending the boundaries of current knowledge in reliability engineering, material science, and heat transfer.

- This research introduced innovative methods for reliability assessment. The development and validation of time-transient temperature-dependent thermal impedance '$Z_{th}(t,T_{amb})$' parameter as a diagnostic tool offers a new approach to identifying early signs of thermal performance degradation in power devices. Such tools enhance the scientific understanding of degradation mechanisms, particularly in process-dependent materials like silver sintering, and provide a foundation for future studies.

- This dissertation highlighted the critical role of material properties on the reliability of power electronic devices. An experimental method of characterizing thin interface thermal properties in the right form factor based on the '$\Delta Z_{th}(t,\Delta x)$' parameter was demonstrated. Besides, investigating silver sintering materials varying in compositions and processing conditions provided valuable insights into the die-attach interface characteristics under operational stresses. This contributes to the broader scientific dialogue on developing Pb-free alternatives for die-attach materials, which is crucial for environmental sustainability and regulatory compliance.

- This research emphasized the importance of thermal management for efficient heat transfer. Integrating diamond heat spreaders to thin semiconductor substrates reduced concentrated thermal hotspots. Likewise, co-packaging electronics with microfluidics by integrating microchannels on the package substrate demonstrated a significant increase in device power rating and a reduction in the total thermal resistance of the system. Such technologies advance our understanding of heat transfer, which is crucial for developing reliable and robust power semiconductor devices.

The findings of this research on Prognostics and Thermal Management of Power Electronic Packages carry certain societal implications, influencing various sectors and contributing to a broader audience. These implications are not just relevant to academia but also to industry practices, which are elaborated as follows:

- This research introduced experimental methods to detect early signs of failures through real-time monitoring and advanced thermal management strategies for improving the device's performance. The real-time monitoring approach can benefit field-critical applications where failures can have severe consequences. For automotive electric vehicles, real-time monitoring can boost customer confidence and promote sustainable transportation by enabling de-rating strategies or preventive maintenance. Likewise, the proposed advanced thermal management strategies, like integrating electronics with microfluidics, can improve the device efficiency, reduce overall energy consumption, repurpose heat generated from the chip, and extend the longevity of the devices.

- This research evaluated several silver sintering materials' thermal and thermo-mechanical performance. Silver sintering has the potential to become a drop-in lead solder replacement for high-power devices, which are toxic to human health and hazardous to the environment. Environmental concerns over other chemicals, such as Per-and-Poly FluroAlkyl Substances (PFAs) and 1-methyl-2-pyrrolidone (NMP), are also being regulated, forcing material suppliers to review the chemicals used in their manufacturing processes. With continuous efforts, silver sintering can become a reliable and safe material for electronic packaging.

8.3. RECOMMENDATIONS

While this dissertation has demonstrated the benefits of prognostic approaches for monitoring the reliability of power electronic packages, implementing them in real-life scenarios requires further refinements. The device's electrical and thermal performance can be measured in real-time at a predefined interval without interrupting the system's operation. It is also necessary to capture the ambient conditions, such as environmental humidity, temperature, vibrations, etc., while monitoring the device's performance. Categorizing the dataset according to the measurement conditions would help identify the degradation patterns that trigger preventive maintenance strategies. Besides, creating collaborative platforms for data sharing is essential, as it can enable data aggregation from multiple devices and applications. Hence, it is recommended that future research focus on standardizing the monitoring tools, creating infrastructures for data collection, and integrating them with machine learning methods for Remaining Useful Life (RUL) prediction.

Die-attach materials are crucial in transmitting the device's electrical, thermal, and mechanical signals to its surroundings. In this dissertation, a specific focus was laid on silver sintering materials. However, other materials, such as copper sintering, can also be a potential Pb-free alternative for die-attachments. Likewise, materials for clip attachments are gaining increasing focus as clips replace wire bonds for high-power applications. Hence, it is recommended that future research should focus on developing and applying materials with tailored properties to meet specific operational requirements for die and clip attachments. Additionally, sustainability is becoming an increasingly important factor in material development. Future work should investigate the potential of recycling and reusing materials for sustainable electronics. It is also necessary to consider the environmental impact of the manufacturing processes associated with material development. Developing environmentally friendly manufacturing techniques that minimize waste and energy consumption is a necessary consideration.

The challenges in implementing advanced thermal management strategies are related to cost and complexity. In this dissertation, the integration of diamond heat spreaders and co-packaging electronics with microfluidics was presented. While these technologies offer benefits in terms of performance, their widespread adoption depends on balancing the cost of implementation. Future research should optimize thermal management technologies to make them commercially viable. Hybrid approaches combining active and passive cooling components or incorporating phase change materials may offer a

balanced cost-performance ratio. However, the durability of these advanced thermal management systems needs to be studied in future research. Additionally, with the rapid adoption of liquid-cooled technologies in data centers, where substantial thermal energy is transferred from processing devices to coolants, it is recommended to continue further research on thermal energy storage and repurposing, which are crucial for developing a sustainable future.

SUMMARY

Developing reliable and efficient power semiconductors is essential to realizing a sustainable future. Packaging materials for high-power applications are electrically overstressed, are exposed to harsh environmental conditions, and are subjected to heightened temperature swings, thereby compromising the device's stability and longevity. In this dissertation, a series of experimental methodologies were explored for monitoring the package conditions, particularly the die-attach interface, which transmits the necessary electrical, thermal, and mechanical signals from the device to the system. Furthermore, advanced thermal management strategies were investigated to circumvent concentrated microthermal hot spots and improve the device's power rating.

In Chapter 1, an outlook on power electronics reliability and reliability monitoring methods was presented, highlighting the evolution of reliability qualification and stringent requirements. A thorough summary of dominant chip-level and package-level degradation mechanisms was reviewed, and numerous measurement methods for real-time monitoring were investigated. The significance of early fault detection was emphasized in this chapter to potentially reduce system downtime and enhance operational efficiency.

In Chapter 2, a novel online condition monitoring strategy was introduced. A temperature dependent transient thermal impedance parameter was used as a metric to detect thermal performance degradation. The methodology was demonstrated using a thermal test chip assembled in a Power QFN package and monitored continuously during Thermo-Mechanical Cycling Lifetime (TMCL) experiments. The study successfully identified multiple failure mechanisms and validated the effectiveness of this approach compared to industry-standard methods. This chapter underscores the practical applicability of this methodology in real-life scenarios, highlighting its potential for early detection of failures in power electronics.

In Chapter 3, prognostic monitoring of PQFN packages with distinct silver-sintered materials was investigated. Each silver sinter material was varied in composition and processing methods. The findings highlighted that pressureless Ag-sinter material with dense microstructure can yield performance comparable to pressure-assisted methods. The study also identified reliability issues with resin-reinforced hybrid-Ag materials, indicating the need for further development. Chapter 4 continued the exploration of silver sintering by emphasizing the development and testing of hybrid silver sinter materials. The silver pastes were formulated with special filler materials and stress-absorbing additives to improve the lifetime reliability of sintered interconnects. The new class of hybrid silver sintering materials demonstrated high die-shear strength at 260^{o}C on NiPdAu and Ag metalized leadframes. Besides, they exhibited resilience to thermo-mechanical loading conditions with less than 10% deviation in electrical on-state resistance over 2000 thermal

cycles. The lifetime performance of various silver sinter materials in chapters 3 and 4 contributed to the ongoing search for reliable, lead-free alternatives in power electronics packaging.

In Chapter 5, a novel thermal characterization methodology for thin bond-line interfaces with high-conductive materials was introduced. Estimating the interface thermal properties of complex materials, such as silver sintering, presents several challenges due to processing conditions' influence on material properties. The study introduced a unique approach to measuring the transient heat flux impedance across sintered interfaces, addressing the limitations of conventional measurement methods. The findings revealed the process-dependent nature of sintered silver's thermal properties, with significant implications for the design and reliability of die-attach interfaces. This chapter also discussed the influence of material processing on thermal behavior, providing a foundation for further research into advanced thermal management solutions.

In Chapter 6, a heterogeneous method of integrating diamond heat spreaders into power electronic packages was demonstrated. The research highlighted the effectiveness of diamond heat spreaders in reducing junction temperatures and enhancing thermal performance in PQFN packages, potentially minimizing concentrated hot spots. The study also validated the reliability of these enhanced packages with heat spreaders by subjecting them to thermal cycling conditions. The results suggest that diamond-based thermal solutions can improve the performance and longevity of high-power electronic devices. This chapter contributes to the development of advanced thermal management technologies necessary for next-generation high-power electronic devices.

In Chapter 7, a novel approach to thermal management by co-packaging electronics with microfluidics was introduced. A serpentine microchannel was integrated onto a surface mount package substrate, demonstrating a substantial improvement with a six-fold increase in device power rating and a significant reduction in junction-to-ambient thermal resistance. This innovative concept addresses the heat dissipation challenges of high-power devices and paves the way for more compact and powerful electronic systems.

To conclude, this dissertation made significant contributions to the field of power electronics by addressing critical challenges in reliability and thermal management. Such efforts in developing prognostic monitoring methods and novel thermal management strategies are required to enhance the understanding and capabilities of power electronic systems. The findings broadly affect various industries where reliable and efficient power electronics are essential for achieving sustainable, high-performance solutions. As the demand for more robust and compact electronic systems continues to grow, the advancements presented in this dissertation will play a crucial role in shaping the future of power electronics.

SAMENVATTING

Het ontwikkelen van betrouwbare en efficiënte vermogenshalfgeleiders is essentieel voor het realiseren van een duurzame toekomst. Verpakkingsmaterialen voor toepassingen met een hoog vermogen worden elektrisch overbelast, worden blootgesteld aan zware omgevingsomstandigheden en worden onderworpen aan verhoogde temperatuurschommelingen, waardoor de stabiliteit en levensduur van het apparaat in gevaar komen. In dit proefschrift werd een reeks experimentele methodologieën onderzocht voor het bewaken van de verpakkingsomstandigheden, met name de die-attach-interface, die de benodigde elektrische, thermische en mechanische signalen van het apparaat naar het systeem verzendt. Verder werden geavanceerde thermische beheerstrategieën onderzocht om geconcentreerde microthermische hotspots te omzeilen en het vermogen van het apparaat te verbeteren.

In Hoofdstuk 1 werd een visie op de betrouwbaarheid van vermogenselektronica en methoden voor betrouwbaarheidsmonitoring gepresenteerd, waarbij de evolutie van de betrouwbaarheidskwalificatie en strenge eisen werden benadrukt. Er werd een grondige samenvatting van de dominante degradatiemechanismen op chip- en package-niveau beoordeeld, en verscheidene meetmethoden voor realtime monitoring werden onderzocht. In dit hoofdstuk werd het belang van vroege foutdetectie benadrukt om de uitvaltijd van het systeem mogelijk te verminderen en de operationele efficiëntie te verbeteren.

In Hoofdstuk 2 werd een nieuwe online strategie voor conditiemonitoring geïntroduceerd. Een temperatuurafhankelijke transiënte thermische impedantieparameter werd gebruikt als maatstaf om verslechtering van de thermische prestaties te detecteren. De methodologie werd gedemonstreerd met behulp van een thermische testchip, geassembleerd in een Power QFN-package en continu gevolgd tijdens Thermo-Mechanical Cycling Lifetime (TMCL)-experimenten. De studie heeft met succes meerdere faalmechanismen geïdentificeerd en de effectiviteit van deze aanpak gevalideerd in vergelijking met industriestandaardmethoden. Dit hoofdstuk onderstreept de praktische toepasbaarheid van deze methodologie in real-life scenario's, waarbij het potentieel ervan voor vroege detectie van storingen in vermogenselektronica wordt benadrukt.

In Hoofdstuk 3 werd de prognostische monitoring van PQFN-packages met verschillende zilvergesinterde materialen onderzocht. Elk zilversintermateriaal was gevarieerd qua samenstelling en verwerkingsmethoden. De bevindingen benadrukten dat drukloos zilversintermateriaal met een dichte microstructuur prestaties kan opleveren die vergelijkbaar zijn met drukondersteunde methoden. De studie identificeerde ook betrouwbaarheidsproblemen met met hars versterkte hybride-zilversintermaterialen, wat aangeeft dat er behoefte is aan verdere ontwikkeling. Hoofdstuk 4 vervolgde de verkenning van zilversinteren door de nadruk te leggen op de ontwikkeling en het testen van

hybride zilversintermaterialen. De zilverpasta's zijn geformuleerd met speciale vulmaterialen en spanningsabsorberende additieven om de levensduurbetrouwbaarheid van gesinterde verbindingen te verbeteren. De nieuwe klasse hybride zilversintermaterialen vertoonde een hoge die-shear strength bij 260^{o}C op NiPdAu- en Zilver-gemetalliseerde leadframes. Bovendien vertoonden ze veerkracht gedurende thermomechanische belastingsomstandigheden met een afwijking van minder dan 10% in de elektrische weerstand in de toestand gedurende 2000 thermische cycli. De levensduurprestaties van verschillende zilversintermaterialen in de hoofdstukken 3 en 4 hebben bijgedragen aan de verdere zoektocht naar betrouwbare, loodvrije alternatieven in verpakkingen voor vermogenselektronica.

In Hoofdstuk 5 werd een nieuwe thermische karakteriseringsmethodologie voor dunne verbindingslijngrensvlakken met hooggeleidende materialen geïntroduceerd. Het schatten van de thermische interface-eigenschappen van complexe materialen, zoals het sinteren van zilver, brengt verschillende uitdagingen met zich mee vanwege de invloed van de verwerkingsomstandigheden op de materiaaleigenschappen. De studie introduceerde een unieke benadering voor het meten van de transiënte warmtefluximpedantie over gesinterde grensvlakken, waarbij de beperkingen van conventionele meetmethoden werden aangepakt. De bevindingen brachten de procesafhankelijke aard van de thermische eigenschappen van gesinterd zilver aan het licht, met aanzienlijke implicaties voor het ontwerp en de betrouwbaarheid van die-attach-interfaces. In dit hoofdstuk werd ook de invloed van materiaalverwerking op thermisch gedrag besproken, wat een basis vormde voor verder onderzoek naar geavanceerde oplossingen voor thermisch beheer.

In Hoofdstuk 6 werd een heterogene methode gedemonstreerd voor het integreren van diamanten warmteverspreiders in vermogenselektronicapakketten. Het onderzoek benadrukte de effectiviteit van diamanten warmteverspreiders bij het verlagen van de junctietemperaturen en het verbeteren van de thermische prestaties in PQFN-package, waardoor geconcentreerde hotspots mogelijk worden geminimaliseerd. De studie valideerde ook de betrouwbaarheid van deze verbeterde packages met warmteverspreiders door ze te onderwerpen aan thermische cycli. De resultaten suggereren dat op diamanten gebaseerde thermische oplossingen de prestaties en levensduur van elektronische apparaten met hoog vermogen kunnen verbeteren. Dit hoofdstuk draagt bij aan de ontwikkeling van geavanceerde technologieën voor thermisch beheer die nodig zijn voor de volgende generatie elektronische apparaten met hoog vermogen.

In Hoofdstuk 7 werd een nieuwe benadering van thermisch beheer geïntroduceerd door elektronica samen met microfluïdica te verpakken. Een kronkelig microkanaal werd geïntegreerd op een package substraat, wat een substantiële verbetering aantoonde met een zesvoudige toename van het vermogen van het apparaat en een significante vermindering van de thermische weerstand van de overgang naar de omgeving. Dit innovatieve concept pakt de uitdagingen op het gebied van warmteafvoer van apparaten met een hoog vermogen aan en maakt de weg vrij voor compactere en krachtigere elektronische systemen.

Concluderend kan worden gesteld dat dit proefschrift een belangrijke bijdrage heeft geleverd aan het veld van de vermogenselektronica door kritische uitdagingen op het gebied van betrouwbaarheid en thermisch beheer aan te pakken. Dergelijke inspanningen bij het ontwikkelen van prognostische monitoringmethoden en nieuwe strategieën voor thermisch beheer zijn nodig om het begrip en de mogelijkheden van vermogenselektronische systemen te vergroten. De bevindingen hebben grote gevolgen voor verschillende industrieën waar betrouwbare en efficiënte vermogenselektronica essentieel is voor het bereiken van duurzame, hoogwaardige oplossingen. Naarmate de vraag naar robuustere en compactere elektronische systemen blijft groeien, zullen de ontwikkelingen die in dit proefschrift worden gepresenteerd een cruciale rol spelen bij het vormgeven van de toekomst van vermogenselektronica.

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The chip featured on the cover page was developed by Romina Sattari, assembled and photographed by Sander Dorrestein, and wire-bonded by Martien Kengen.

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List of Publications

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BOOK CHAPTER

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PATENT

1. **P137764EP00**, **H. A. Martin**, E. C. P. Smits, *Integrated Microfluidics on Electronic Package Leadframe* (Patent Pending).