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Quantifying Biomedical Amplifier Efficiency

The noise efficiency factor

here has been a longstanding interest in controlling and instrumenting the human body. Whether to restore lost function with neural prosthetics, monitor blood glucose levels, or augment human capabilities, there are countless opportunities for sensors inside (e.g., ingestible, injectable, and implantable) and outside (e.g., wearable) the body. However, many challenges exist when instrumenting the body. First, many use cases (e.g., implanted sensors) require long-term recording to capture anomalous behavior sometimes with limited accessibility

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—necessitating ultralow power consumption. Second, the power reduction challenge is further exacerbated by size constraints, which limit battery capacity or harvestable energy levels. Third, the signals of interest are often low bandwidth (kHz) and small in amplitude (μV to mV); thus, low-noise front ends are needed. Addressing these challenges has led to a large body of work on the design of highly power-efficient, low-noise amplifiers for biomedical integrated circuits.

Many metrics have been devised to capture the performance of these amplifiers. For example, the well-known gain-bandwidth product quantifies the tradeoff between gain and bandwidth. Another example is the noise efficiency factor (NEF),

which quantifies the tradeoff between the bias current of an amplifier and its input-referred noise. This article describes the history of the NEF and provides examples of its application to address common misunderstandings, followed by some circuit techniques to improve noise efficiency.

History

In 1987, in their seminal paper [1], Steyaert, Sansen, and Zhongyuan proposed the NEF. They aimed to quantify the fundamental tradeoff between the supply current of an amplifier and its input-referred noise. Intuitively, this tradeoff is obvious: more current should lead to lower input-referred noise. To obtain a unitless quantity, the NEF is defined

with respect to the input-referred noise of a BJT-based amplifier. At the time, such amplifiers were believed to achieve the best noise efficiency—the lowest noise for a given supply current. In recent years, however, even better amplifier topologies have been invented. However, before we discuss them, we will first go through a few examples to illustrate the somewhat confusing use of the NEF. As described in [1], the NEF is defined as

$$NEF \triangleq v_{n,rms} \sqrt{\frac{2I_{tot}}{4V_T k_B T f_{BW} \pi}}$$

where $\nu_{n,rms}$ is the input-referred noise of the amplifier being compared, assuming a single-pole low-pass filter located at the signal bandwidth of f_{BW} ; I_{tot} is the amplifier dc current; V_{T} is the thermal voltage; $k_{\rm B}$ is Boltzmann's constant; and T is the temperature. This definition of input-referred noise has created some confusion about how the NEF should be calculated, but we will discuss this more later. Thus, the NEF captures the fundamental tradeoff between an amplifier's supply current and its input-referred noise (with a few constants and an extra factor of 2 sprinkled in for good measure).

For the common-emitter BJT amplifier shown in Figure 1, the noise power spectral density (PSD) of the output current, i_C , is given by

$$\frac{i_{\rm C}^2}{\Delta f} = 2qI_{\rm C} = 2k_{\rm B}Tg_{\rm m}$$

where I_C is the dc collector current and q is the electron charge. Note

that this only accounts for the collector current's shot noise and neglects its flicker noise, the base current's shot noise, and the base resistance's thermal noise. Furthermore, the transconductance, $g_{\rm m}$, of a BJT is $I_{\rm C}/(k_{\rm B}T/q)$, allowing us to simplify the noise PSD expression. The total input-referred voltage noise, assuming that the amplifier exhibits a single-pole response with a bandwidth of $f_{\rm BW}$, is

$$\begin{split} \nu_{\text{n,rms_bjt}} &= \sqrt{\frac{2 \, k_{\text{B}} T g_{\text{m}}}{g_{\text{m}}^2} f_{\text{BW}} \frac{\pi}{2}} \\ &= \sqrt{\frac{2 \, V_{\text{T}} \, k_{\text{B}} T}{I_{\text{C}}} f_{\text{BW}} \frac{\pi}{2}}. \end{split}$$

Including the $\pi/2$ factor, which accounts for the *equivalent noise bandwidth* of the single-pole response, is a necessary step since brickwall filters do not exist; hence, the noise PSD at frequencies beyond $f_{\rm BW}$ must also be taken into account. Over the years, many authors have neglected the $\pi/2$ term, thus artificially reducing their reported NEF by 20% by only integrating their amplifier's noise density up to the signal bandwidth.

Finally, the NEF of the commonemitter BJT amplifier is

$$NEF_{bjt} = \nu_{n,rms_bjt} \sqrt{\frac{2I_{tot}}{4V_T k_B T f_{BW} \pi}}$$

$$= \sqrt{\frac{2V_T k_B T}{I_C}} f_{BW} \frac{\pi}{2}$$

$$\times \sqrt{\frac{2I_{tot}}{4V_T k_B T f_{BW} \pi}}$$

$$= \frac{1}{\sqrt{2}}$$

where $I_{\rm tot}=I_{\rm C}.$ Note that contrary to what is commonly thought, $NEF_{\rm bjt}$ is not equal to 1. So, an NEF of $1/\sqrt{2}$ means that an amplifier has the

same noise efficiency (input-referred noise for current invested) as a BJT common-emitter amplifier with a noiseless load. Since a BJT-based differential pair has two uncorrelated noise sources and consumes twice the current for the same transconductance, it has an NEF of $\sqrt{2}$.

What about MOSFET-based amplifiers? The input-referred noise of a common-source amplifier with a noiseless load is

$$v_{\rm n,rms_mos} = \sqrt{\frac{4k_{\rm B}T\gamma g_{\rm m}}{g_{\rm m}^2}f_{\rm BW}\frac{\pi}{2}}$$

where γ is the noise coefficient (~2/3 for a long-channel MOSFET). So, the NEF is

$$\begin{split} \textit{NEF}_{mos} &= \nu_{n,rms_mos} \sqrt{\frac{2I_{tot}}{4V_T k_B T f_{BW} \pi}} \\ &= \sqrt{\frac{4k_B T \gamma g_m}{g_m^2}} f_{BW} \frac{\pi}{2} \\ &\times \sqrt{\frac{2I_{tot}}{4V_T k_B T f_{BW} \pi}} \\ &= \sqrt{\frac{\gamma}{V_T} \frac{I_D}{g_m}} \end{split}$$

where $I_{\rm D}$ is the drain current. This indicates that to minimize the NEF, we should maximize $g_{\rm m}/I_{\rm D}$ — the transconductor efficiency — by operating the MOSFET in the subthreshold region. Here carrier movement is no longer predominantly due to drift but rather is due to diffusion; hence, the noise in the drain current behaves like shot noise and is

$$\frac{\dot{I}_{\rm D}^2}{\Delta f} = 2qI_{\rm D} = 2qg_{\rm m}V_{\rm T}/\kappa = 2k_{\rm B}Tg_{\rm m}/\kappa$$

where κ is the gate coupling coefficient that quantifies the capacitive division between the gate oxide and

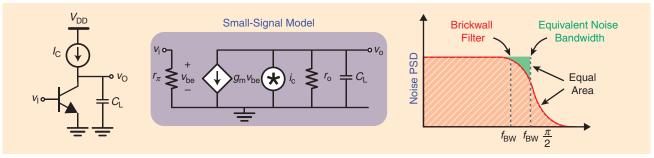


FIGURE 1: The common-source BJT amplifier used as the reference point for NEF and the equivalent small-signal model.

While the NEF decreases as the number of stacked transconductors increases, the minimum supply voltage also increases, reducing the benefit of continued stacking.

the depletion capacitance (or alternatively, the subthreshold slope parameter, $n = 1/\kappa$). Thus, the NEF of a common-source amplifier biased in subthreshold is

$$\begin{aligned} \textit{NEF}_{\text{mos}} &= \sqrt{\frac{2 \, V_{\text{T}} \, k_{\text{B}} \, T}{\kappa^2 \, I_{\text{D}}}} \, f_{\text{BW}} \frac{\pi}{2} \\ &\times \sqrt{\frac{2 \, I_{\text{tot}}}{4 \, V_{\text{T}} \, k_{\text{B}} \, T f_{\text{BW}} \pi}} \\ &= \sqrt{\frac{1}{2 \kappa^2}} \, . \end{aligned}$$

It is thus $1/\kappa$ times worse than that of a common-emitter amplifier. For $\kappa=0.7$, the NEF is 1.01. For a differential pair, the NEF is 2.02, a value long considered to be the lower limit on the achievable NEF of a MOSFET-based amplifier.

Structures That Beat the NEF "Limit"

The inverter-based amplifier shown in Figure 2(a) is a simple way to improve on the NEF of a differential pair. It has twice the transconductance $(G_{\rm m} = g_{\rm mn} + g_{\rm mp})$ for the same bias

current, reducing its input-referred noise and resulting in a $1/\sqrt{2}$ NEF improvement (from 2.02 to 1.43) [2], [3]. Extending this concept by stacking more transconductors can further increase the extent of the current reuse. To the authors' knowledge, this was originally proposed in a patent [4], in which the same current was reused by independent amplifiers in a multichannel configuration to save power. More recently, in a neural recording front end [5], PMOS differential pairs are stacked for orthogonal current reuse among multiple channels. A similar singlechannel chopper amplifier was subsequently proposed [6], in which the same input is modulated/chopped at different frequencies and then applied to stacked differential pairs, as shown in Figure 2(b). This concept was further generalized in [7] and implemented in [8], where sub-unity NEF was achieved for the first time,

as shown in Figure 2(c). This work stacked five differential pairs with ac-coupled inputs for an ECG amplifier that consumed just 13.9 nA from a 1.35 V supply and achieved a 0.86 NEF. While the NEF decreases as the number of stacked transconductors increases, the minimum supply voltage also increases, reducing the benefit of continued stacking. It is also worth pointing out that while transconductor stacking boosts the total transconductance (the reason why it is often referred to as $G_{\rm m}$ -boosting), the output impedance goes down by the same amount; thus, the resulting voltage gain is the same as that of an inverter-based amplifier! Despite these limitations, $G_{\rm m}$ -boosting is a simple, but highly effective, way of achieving lower NEF.

The NEF limitation for MOSFET-based amplifiers stems from their current noise $(4k_{\rm B}T\lambda\,g_{\rm m})$ and maximum $g_{\rm m}/I_{\rm D}$. These can be overcome if amplification is performed without using MOSFETs as transconductances. One such structure that does this is a series-parallel amplifier (SPA), a well-known building block in switched capacitor dc-dc converters. As shown in Figure 3, this

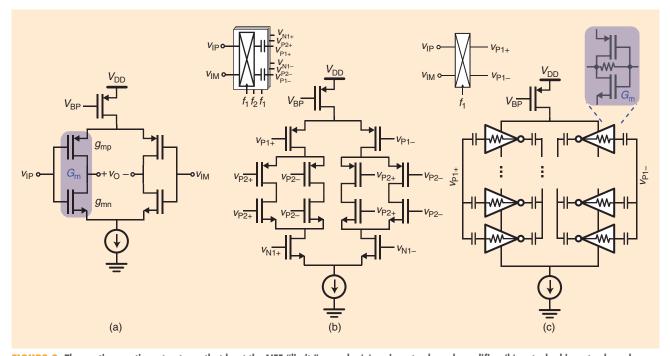


FIGURE 2: The continuous-time structures that beat the NEF "limit," namely, (a) an inverter-based amplifier, (b) a stacked inverter-based amplifier, and (c) a G_m-boosted stacked amplifier.

amplifier samples an input voltage on N parallel capacitors and produces an amplified output by connecting the capacitors in series, thus achieving a gain of N, where N is the number of capacitors [9]. The sampling results in a non-infinite input impedance of $1/sNC_S$; however, this is typically quite large, e.g., $1.6 \,\mathrm{M}\Omega$ at 1 kHz, even with $NC_s = 100 \text{ pF}$ [9]. The sampling noise, k_BT/NC_S , is spread from 0 to $f_s/2$, making the noise PSD = $2k_BT/NC_Sf_s$. Due to the sample-and-hold nature of switched capacitor circuits, the noise spillover to frequencies higher than $f_s/2$ is sinc-shaped. However, this effect is negligible, assuming that $f_{\rm s}$ is much higher than f_{BW} . Therefore, the input-referred noise of the SPA is

$$v_{\rm n,SPA} = \sqrt{\frac{2k_{\rm B}T}{NC_{\rm S}f_{\rm S}}f_{\rm BW}\frac{\pi}{2}}.$$

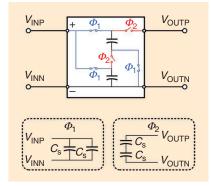


FIGURE 3: A simplified schematic of a 1:2 switched capacitor circuit.

The stringent energy budget of implantable and wearable systems has motivated the design of amplifiers with high noise efficiency for sensor interface circuits, particularly in arrayed applications such as multichannel neural recording.

While an SPA does not have a bias current, it does draw supply current to charge the switch's gate capacitance, $C_{\rm g,tot}$, where $C_{\rm g,tot}$ is proportional to $NC_{\rm S}$, as the switch must be sized to ensure that the voltage on $C_{\rm S}$ settles during the sampling phase. The total current is

$$I_{SPA} = \beta N C_S V_{DD} f_s$$

where β is the ratio of $C_{g,tot}/NC_{S}$. Finally, the NEF of the SPA is

$$\begin{aligned} \textit{NEF}_{\text{SPA}} &= \nu_{\text{n,SPA}} \sqrt{\frac{2I_{\text{SPA}}}{\pi 4 V_{\text{T}} k_{\text{B}} T f_{\text{BW}}}} \\ &= \sqrt{\frac{\pi k_{\text{B}} T}{N C_{\text{S}} f_{\text{s}}}} f_{\text{BW}} \sqrt{\frac{2\beta N C_{\text{S}} V_{\text{DD}} f_{\text{s}}}{\pi 4 V_{\text{T}} k_{\text{B}} T f_{\text{BW}}}} \\ &= \sqrt{\frac{\beta V_{\text{DD}}}{2 V_{\text{T}}}}. \end{aligned}$$

Table 1 summarizes the noise performance of a continuous-time stacked amplifier and an SPA. The continuous-time amplifier's NEF is limited by the $g_{\rm m}/I_{\rm D}$ ratio, while that of the SPA depends on the capacitance ratio, β , and can be much lower than 1. For example, in a 180-nm process, with $V_{\rm DD}$ = 1 V and $\beta = 0.01$, an NEF of 0.45 was achieved [9]. However, β improves with technology scaling, making the SPA more attractive in advanced technology nodes. Note that the SPA operates like a transformer that amplifies an input voltage at the expense of load-driving capability. Therefore, it is important to

	PARISON OF CONTINUOUS-TIME AMPLIFIERS AND SPA.	
	CONTINUOUS-TIME AMPLIFIERS	SPA
Noise spectral density	$\propto \frac{k_{\rm B}T}{g_{\rm m}}$	$\propto \frac{k_{\rm B}T}{NC_{\rm s}f_{\rm s}}$
Current consumption	∞ I _D	$\propto \beta N C_s f_s$
NEF	$\propto \sqrt{\frac{I_{\rm D}}{I_{\rm D}}} \frac{1}{V_{\rm C}}$	$\sqrt{BV_{\rm DD}}$

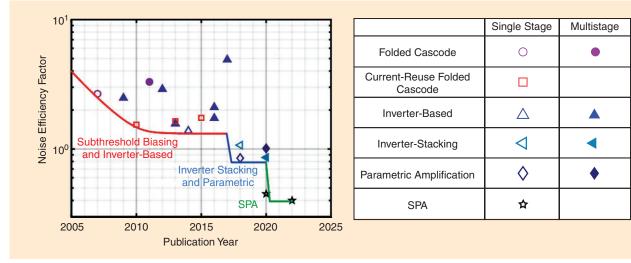


FIGURE 4: A survey of the reported NEF for biomedical amplifiers from 2007 to 2022.

Thus, the NEF is not dependent on nonfundamental parameters such as technology node, area, and supply voltage and thus provides a fair way of comparing the noise efficiency of different amplifier topologies.

minimize the input capacitance of the following stage; thus, a unity gain buffer is typically adopted [9], [10]. At the same time, the bottom capacitance of the C_S reduces the gain or the input impedance of the SPA, which can be resolved by adopting an adiabatic switching technique [10].

Trends

The stringent energy budget of implantable and wearable systems has motivated the design of amplifiers with high noise efficiency for sensor interface circuits, particularly in arrayed applications such as multichannel neural recording. As a result, the NEF of biomedical amplifiers has slowly decreased over the last several decades, as shown in Figure 4. From 2006 to 2016, the NEF was primarily reduced by operating MOSFETs in subthreshold and using inverter-based amplifiers. However, as shown earlier, the reduced transconductor efficiency of MOSFETs limits the NEF of a common-source amplifier to ~1, which is why these designs saturated at ~1.2. In 2017, inverter-stacking amplifiers were reported, resulting in NEFs below one. In 2020, the discrete-time SPA was introduced, resulting in NEFs below 0.5 for the first time. In the meantime, many of these new topologies have spread beyond biomedical applications and have been used in ADCs [11], general-purpose amplifiers [12], and oscillators [13].

Concluding Remarks

In this article, we introduced the implication and application of the NEF, which aims to quantify the fundamental tradeoff between the supply current of an amplifier and its

input-referred noise. Therefore, the NEF of an amplifier can be interpreted as "how much noise it generates for a given bias current" or "how much current must be invested to achieve a given input-referred noise."

We also explained a common mistake in the measurement of the NEF. The definition of the NEF assumes that the amplifier's bandwidth is limited by a 1st order low-pass filter. If this is not the case, the filter's equivalent noise bandwidth should be accounted for by scaling the integrated input-referred noise in the signal bandwidth by $\pi/2$. If the filter is implemented, the full spectrum of the input-referred noise beyond the maximum signal bandwidth needs to be integrated.

Unlike other empirical FOMs, the NEF describes the fundamental noise and current tradeoffs between the input-referred noise, current consumption, and bandwidth based on their physical relationship. Thus, the NEF is not dependent on nonfundamental parameters such as technology node, area, and supply voltage and thus provides a fair way of comparing the noise efficiency of different amplifier topologies.

Finally, it should be noted that the NEF is limited to the tradeoff between supply current and noise and does not capture all aspects of amplifier performance. For example, it does not take the technology into account, so for the same topology, BJT-based amplifiers will outperform their MOSFET-based counterparts. It also does not consider frequency-dependent noise sources like flicker or induced gate noise. So, for a given bandwidth and topology, low-frequency amplifiers whose

in-band noise PSD is dominated by flicker noise will have a higher NEF than amplifiers whose in-band noise PSD is dominated by thermal noise. Last, besides reducing noise, the supply current is also required to improve other aspects of amplifier performance. For instance, achieving a wide bandwidth, high CMRR or PSRR, good linearity, or good input and output impedance may increase current consumption without reducing the noise, which worsens NEF. So, besides the NEF, other performance metrics must always be considered when evaluating an amplifier's performance.

References

- M. S. J. Steyaert, W. M. C. Sansen, and C. Zhongyuan, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol. 22, no. 6, pp. 1163–1168, Dec. 1987, doi: 10.1109/JSSC.1987.1052869.
- [2] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, Feb. 1991, doi: 10.1109/4.68134.
- [3] M. S. Chae, Z. Yang, M. R. Yuce, L. Hoang, and W. Liu, "A 128-channel 6 mW wireless neural recording IC with spike feature extraction and UWB transmitter," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 17, no. 4, pp. 312–321, Aug. 2009, doi: 10.1109/TN-SRE.2009.2021607.
- [4] G. Cecchin and F. H. Hilbert, "Stacked differential amplifiers," U.S. Patent US3603894A, Sep. 7, 1971.
- [5] B. Johnson and A. Molnar, "An orthogonal current-reuse amplifier for multi-channel sensing," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1487–1496, Jun. 2013, doi: 10.1109/JSSC.2013.2257478.
- [6] Y.-P. Chen, D. Blaauw, and D. Sylvester, "A 266nW multi-chopper amplifier with 1.38 noise efficiency factor for neural signal recording," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2, doi: 10.1109/VLSIC.2014.6858431.
- [7] S. Mondal and D. A. Hall, "An ECG chopper amplifier achieving 0.92 NEF and 0.85 PEF with AC-coupled inverter-stacking for noise efficiency enhancement," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4, doi: 10.1109/ISCAS.2017. 8050957.
- [8] S. Mondal and D. A. Hall, "A 13.9-nA ECG amplifier achieving 0.86/0.99 NEF/PEF using AC-coupled OTA-stacking," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 414–425, Feb. 2020, doi: 10.1109/JSSC.2019. 2957193.
- [9] G. Atzeni, A. Novello, G. Cristiano, J. Liao, and T. Jang, "A 0.45/0.2-NEF/PEF 12-nV/\Hz highly configurable discrete-time low-noise amplifier," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 486–489, Oct. 2020, doi: 10.1109/ LSSC.2020.3029016.
- [10] G. Atzeni et al., "An impedance-boosted switched-capacitor low-noise amplifier achieving 0.4 NEF," in Proc. IEEE Symp. VLSI Technol. Circuits, Jun. 2022,

pp. 116-117, doi: 10.1109/VLSITechnologyandCir46769.2022.9830399.

[11] S. Mondal, O. Ghadami, and D. A. Hall, "A 139 μ W 104.8dB-DR 24kHz-BW CT ΔΣΜ with chopped AC-coupled OTA-stacking and FIR DACS," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2021, vol. 64, pp. 166–168, doi: 10.1109/ISSCC42613. 2021.9366002.

[12] L. Shen, A. Mukherjee, S. Li, X. Tang, N. Lu, and N. Sun, "A 0.6-V tail-less inverter stacking amplifier with 0.96 PEF," in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. C144–C145, doi: 10.23919/VLSIC.2019.8778011.

[13] S. Iguchi, T. Sakurai, and M. Takamiya, "A low-power CMOS crystal oscillator using a stacked-amplifier architecture," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3006–3017, Nov. 2017, doi: 10.1109/ JSSC.2017.2743174.

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