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Efficiency and Linearity of Digital "Class-C Like" Transmitters

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***Abstract* — An energy-efficient, intrinsically linear, digital "class-C like" operation-mode is investigated for use in high-power digital transmitters (DTXs), which target next generation mMIMO base stations that offer lower costs, higher integration, and improved system efficiency. The proposed operation utilizes class-B/C output matching in combination with duty-cycle reduction and current-mode operation of a segmented output stage. Its performance in terms of efficiency, output power, and linearity is benchmarked with analog class-B/C operation. The proposed digital "class-C like" operation has been experimentally verified using a fully-digital, dual TX line-up with V_T-shifted segmented LDMOS output stages. All output stage segments are individually controlled by high-speed digital drivers implemented in 40 nm CMOS technology. The realized prototype provides 25.9 W (CW) output power with 75.7 % drain and 72.9 % system efficiencies, at 930 MHz and at 28 V drain supply.**

***Keywords* — Class-C, digital transmitter, efficiency, linearity, LDMOS, CMOS RFIC, polar transmitter, RFDAC, digital power amplifier.**

I. Introduction

The successful introduction of sub-6 GHz fifth-generation (5G) wireless networks relies on the availability of low-cost, energy-efficient massive multiple-input and multiple-output (mMIMO) base stations. It is expected that these new mMIMO systems will feature up to 64 or even 256 times more transmit (TX)/receive (RX) signal paths than their 4G predecessors. This massive change demands higher integration and more energy-efficient RF frontends at lower costs. To do so, drastic changes in the TX line-up are required, since traditional analog TX architectures suffer from low integration, while dealing with severe linearity–efficiency trade-offs. To improve both system integration and efficiency, fully-digital transmitter (DTX) solutions for mMIMO base-stations are rapidly gaining interest, since they benefit most from the progress in advanced semiconductor technologies, yielding already promising results at various power levels [1–7].

This work aims to investigate suitable operation classes for segmented power output stages in DTX architectures that target higher TX powers. Emphasis is placed on achieving the best overall performance in terms of drain and system efficiency, output power, bandwidth, and their amplitude code word (ACW) to output transfers in terms of ACW–AM.

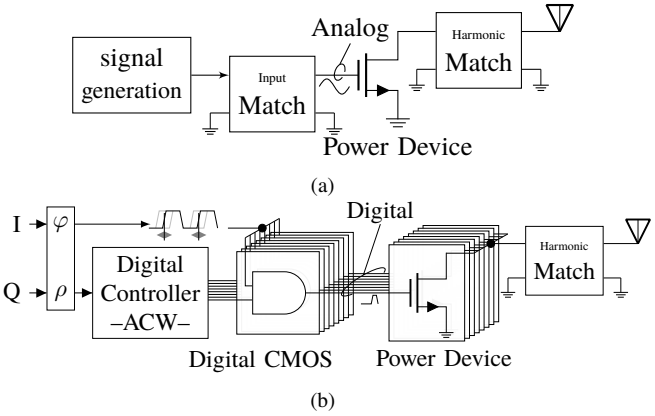


Fig. 1. Conceptual diagrams of: (a) An analog transmitter; (b) A fully digital polar transmitter featuring a segmented output power stage.

II. DTX Principles

Over the last two decades, various DTX architectures have been introduced [1, 2, 4–7]. This work focuses on a polar DTX using segmentation in its final power output stage. The architecture of a simplified fully-digital polar TX architecture is depicted in Fig. 1b. In this DTX, the original IQ baseband data is converted into an ACW and its digital phase representation, which is used to modulate an RF carrier. Logic gates controlled by the ACW determine the number of active output stage segments that are driven by the phase modulated RF carrier. The (combined) output signal of the segmented power devices is fed to the harmonic matching network.

In a similar configuration using an analog operated power amplifier (PA) output stage (Fig. 1a), the output stage device is driven by a single continuous amplitude modulated RF signal. Depending on the exact biasing of this output stage, a truncated sine-wave current appears at its output. Amplitude modulation is implemented by varying the amplitude of the drive voltage. In a DTX approach the segments in the DTX can only be "fully-on" or "fully-off", consequently, a discretized current waveform will appear at its (combined) output. The amplitude of the waveform is determined by the number of activated segments, modulating the effective width of the output stage. The precise shape of this waveform depends on the applied matching conditions and segmented output stage operation. Namely, when these segments are hard-driven, and their combined R_{on} is significantly smaller than the effective load impedance at the

device plane, the output stage toggles between the off-state and linear (triode) operation. In this mode, the segmented power device acts as a simple switch with related R_{on}. The use of class-E with related matching network is, in this condition, the most natural option and has been addressed in [6–9]. The use of class-E has some profound advantages for DTX operation, e.g., a theoretical peak drain efficiency of 100 %, and it can be linearized using dedicated circuit techniques [7]. However, there are also some drawbacks. First, class-E is constrained for its operating frequency, as $f_{maxE} \propto I_{DSmax}/C_{out}V_{DD}$, hence limiting the achievable output power at a given RF frequency for a practical power device. Secondly, its ACW–AM and ACW–PM transfers are not constant over frequency, due to its reactive loading. This sets an upper limit in handling signals with large modulation bandwidth without using more advanced DPD techniques [8]. Lastly, class-E demands some over-dimensioning of the output stage and overdrive conditions to make R_{on} sufficiently low. This puts high demands on the drivers used for these power device segments in terms of their output voltage swing and drive current.

III. Current-Mode DTX

A different strategy for a DTX is to always keep the segmented output stage in current-mode operation, by using the saturation region of the segmented FET power output stage. The resulting drain current is close to a square-wave which is fed to the (harmonic) output matching network. In ideal current-mode DTX operation, the amplitude of this square-wave current is directly proportional to the applied ACW, indicating an intrinsically linear digital ACW-to-RF transfer. The square-wave current resulting from the DTX output, at first glance, suggests the use of inverse class-F operation. However, when considering realistic power devices with unneglectable output capacitance, it is close to impossible to realize a wideband inverse class-F matching network that can handle the aimed bandwidths of 5G.

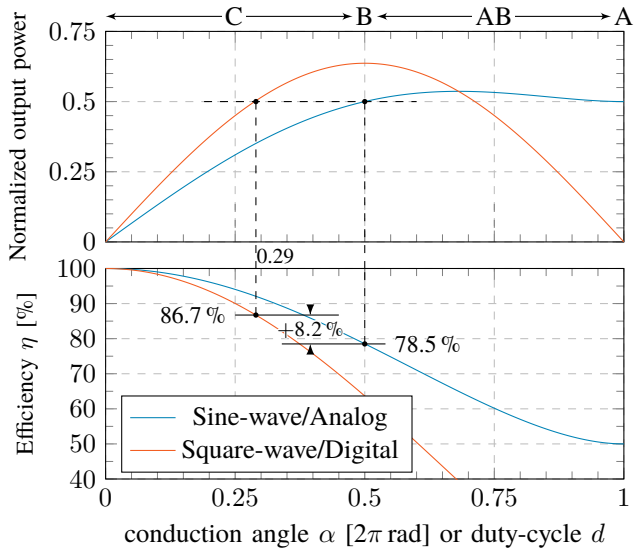


Fig. 2. Analog and digital class-AB/C behavior: Normalized output power and drain efficiency vs. conduction angle/duty-cycle.

In contrast, class-B operation/matching uses only short-circuited conditions for its baseband and higher harmonics, yielding relatively easy implementation. Furthermore, these shorts will limit the voltage stress of the output stage and provide excellent decoupling, as such enabling relatively large RF/modulation bandwidths, even for devices with a large output capacitance. These advantages come without any penalty in the operating frequency or linearity, explaining the widespread popularity of class-B operation in commercial applications.

A. Efficiency

Analog class-B operation theoretically provides 78.5 % (drain) efficiency for a half-sine wave output current with a conduction angle α of π rad. In contrast, DTX "class-B like" operation, assuming a square-wave drain current with π rad conduction angle/50 % duty-cycle, results in a relatively large overlap in the output stage's $V_{DS}(t)$ and $I_{DS}(t)$ waveforms. This increases its power dissipation, as such degrading the achievable drain efficiency. The theoretical efficiency as a function of the duty cycle can be calculated as follows [9],

$$\eta_{DTX}(d) = \frac{\sin(\pi d)}{\pi d}, \tag{1}$$

where d is the duty-cycle between 0 and 1. For a 50 % duty-cycle, the theoretical DTX peak efficiency, $\eta_{DTX}(0.5)$, is only 63.6 %. However, just like in the analog case, reducing the conduction angle improves the achievable DTX efficiency. This comes at the cost of a reduced RF output power capability.

To allow a comparison between analog class-C and digital "class-C like" operation, the maximum drain current (I_{DSmax}), and maximum drain voltage (V_{DSmax}) are normalized to 1 and 2 respectively, which sets the normalized voltage amplitude (V_a) to 1. Using these normalizations, Fig. 2 can be constructed, which compares the output power and drain efficiency for the analog driven and digital driven output stage (DTX) vs. conduction angle/duty-cycle. The square-wave current for the DTX case yields a $4/\pi$ higher fundamental output power for the same I_{max}, at a conduction angle of π rad. This provides a degree of freedom in trading-off RF output power capability in favor of efficiency by reducing its duty-cycle/conduction angle. Doing so, we find that a DTX has a significantly better efficiency–output power trade-off. Namely, at 29 % duty-cycle, the DTX has a drain efficiency of 87 %, while providing the same output power as a traditional analog class-B operated

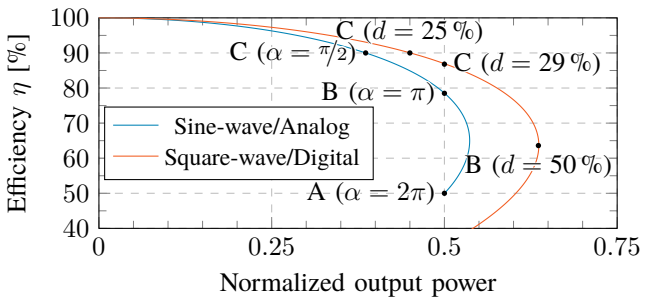


Fig. 3. Theoretical drain efficiency for the analog and digital class-AB/C vs. normalized output power [9].

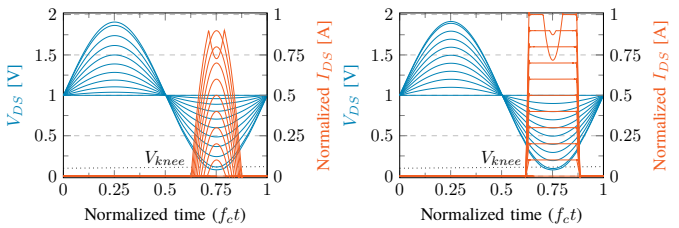


Fig. 4. Time domain waveforms for varying input quantity: (a) Analog class-C ($\alpha = \pi/2$); (b) Digital "class-C like" ($d = 25\,\%$).

device. Further decreasing the RF duty-cycle to 25 %, which is a very convenient choice for DTX implementations, the theoretical DTX drain efficiency increases to 90 %, while its normalized output power reduces only from 0.50 to 0.45. In comparison, to achieve a 90 % peak efficiency using analog class-C operation, the related normalized output power reduces from 0.50 to 0.38. In Fig. 3, the efficiency–output power trade-off for both cases are visualized in detail. Note that the digital "class-C like" operation provides higher drain efficiency for a comparable, or even higher, output power than its analog counterpart. An observation that was made by [9], who indicated this option "to have useful potential", but also recognized its very challenging drive(r) conditions, which will be addressed in more detail in the measurement section.

B. AM–AM and ACW–AM Transfers

For a fictitious ideal active device with a linear V_{GS}-to-I_{DS} relation for $V_{GS} > 0$, ($I_{DS} = 0$ for $V_{GS} < 0$), the analog class-B operation (π rad conduction angle) results in a perfectly linear signal transfer [9]. Moving towards class-C yields gain expansion. This linearity degradation, can be intuitively understood by considering that, in the analog class-C operation, with the input signal (V_{GS}) not only the instantaneous amplitude of I_{DS} linearly changes, but also its effective conduction angle (Fig. 4a). The latter issue yields an extra push in fundamental output power and shows up as gain expansion. In contrast, the DTX effectively uses dynamic scaling of its power device width by activating the segments proportional to the applied ACW, while the segment drive is the same for all segments . The ACW-to-I_{DS} is independent of the drive voltage waveforms, yielding perfect linearity (Fig. 5), even for a non-linear (e.g., quadratic) V_{GS}-to-I_{DS} relation, under the condition that the active device remains in the current-mode region. It is worth mentioning that the analog class-B ($\alpha = \pi$) case, using a perfect square-law device, is special and can still provide linear amplification [10]. For all operation modes, at larger signal excursions, compression starts to occur when the load-line reaches the triode region of the output stage.

IV. Measurements

To verify the forgoing theory, a highly-integrated, bits-in–RF-out, high-power, DTX configuration has been utilized [2]. It features two fully-digital TX line-ups that can be independently controlled. Each TX line-up has 15

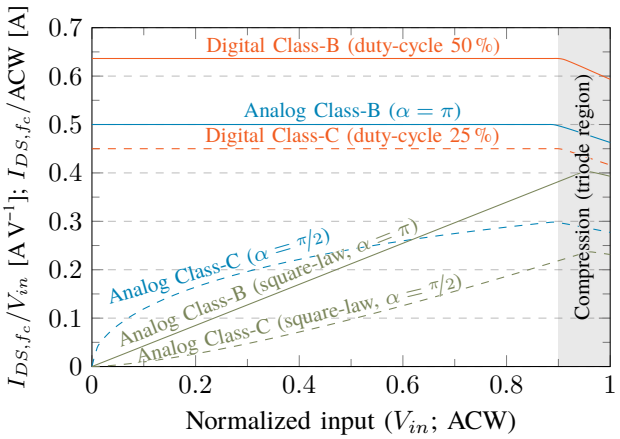
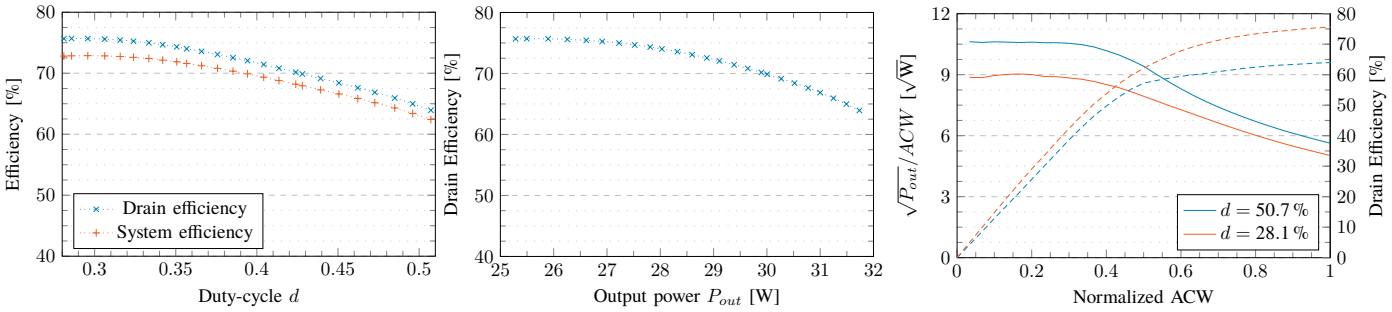


Fig. 5. Fundamental drain current ($I_{DS,fc}$) normalized to the normalized input quantity (V_{in} or ACW) vs. input drive V_{in}; ACW, using $I_{DSmax} = 1$ A and $R_L = R_{opt}$. Dashed lines show class-C operation ($\pi/2$ conduction angle/25 % duty-cycle), clearly indicating gain expansion in the analog cases.

thermometer and 7 binary bits (11-bit in total), which are implemented as segments of the power output stages in V_T-shifted LDMOS technology. These segments can be digitally activated/deactivated at RF speed. The duty-cycle of the activation pulse is varied between 28 % and 51 %, using a programmable on-chip duty-cycle controller. The LDMOS output stage is driven by thick-oxide IO devices that facilitate 2.5 V square-wave (nominal) drive conditions to the output stage segments, implemented in TSMC 40 nm CMOS technology. The dual-DTX line-up can be configured to operate with various external matching or power combining networks to implement, e.g., a polar Doherty, push-pull, or outphasing transmitter. In [2], the dual-DTX line-up was configured for polar class-BE operation and digital pre-distortion (DPD) was used to correct its ACW–AM and ACW–PM linearity. In contrast, this work is focused on highlighting the benefits of digital "class-C like" operation. For this purpose both TX line-ups have been synchronized such that they effectively act like one larger unified segmented output stage, which is terminated using a class-B/C output matching network (short-circuited conditions for the harmonics). A photograph of the realized hardware is given in Fig. 8.

The LDMOS output stages' drains are biased at 28 V, the thick-oxide CMOS drivers and the digital controller use a 2.5 V and 1.1 V supply respectively. Pulsed RF envelope operation with a 10 % envelope duty-cycle is used to avoid excessive heating, while applying the described RF pulse duty-cycle control, at 930 MHz. A spectrum analyzer is used to measure the in pulse RF output using a zero-span measurement. The absolute read-out of the spectrum analyzer is referenced to a power meter. The drain efficiency is calculated as: $\eta_d = P_{RFout}/P_{28Vsupply}$, and the system efficiency as: $\eta_s = P_{RFout}/(P_{static} + P_{2.5Vdrive} + P_{28Vsupply})$, in which the latter includes the total power consumption of the digital controller and the CMOS drivers, corrected for the applied envelope pulse duty-cycle. In Fig. 6a the measured drain and system efficiencies vs. RF duty-cycle are given, Fig. 6b provides the measured drain



(a) (b) (c)

Fig. 6. Pulsed envelope RF measurements (10 % envelope duty-cycle) using digital "class-C like" operation at 930 MHz with segmented LDMOS power devices: (a) Drain and system efficiency vs. RF duty-cycle; (b) Drain efficiency vs. output power for an RF duty-cycle ranging from 30 % to 52 %; (c) Normalized ACW-to-RF output signal transfer (dashed: drain efficiency).

efficiency vs. output power, and Fig. 6c gives the measured $\sqrt{P_{out}}/ACW$ which is proportional to $I_{DS,f_c}/ACW$. As one can observe, a maximum drain and system efficiency for the LDMOS device of respectively 75.7 % and 72.9 % is achieved at 25.9 W output power, while the expected linear $I_{DS,f_c}/ACW$ can be clearly noted until triode region related compression of the output stage sets in. Note that the high system efficiency is a direct consequence from the digital nature of the proposed DTX approach, which consumes practically no static power, while its dynamic power consumption is dominating and proportional to the ACW [2]. Dynamic measurements using a 8.8 MHz 256-QAM signal, using only the linear region show an ACLR of −36.0 dBc without DPD, −43.3 dBc with phase correction only, and −48.3 dBc with static DPD, combined with an EVM of 3.0 %, 1.4 % and 1.1 % respectively. The measured output spectra are shown in Fig. 7.

V. Conclusion

Digital "class-C like" operation has been investigated for use with highly-integrated DTX line-ups featuring segmented output power stages. Emphasis was placed on achieving the best performance in terms of: drain/system efficiency and linearity in the 5 W to 50 W peak power range to address the needs of the upcoming 5G mMIMO base stations. Doing so, 75.7 % drain efficiency and 72.9 % system efficiency at 25.9 W output power was achieved, while typical class-C gain expansion was avoided, which provides an excellent starting point for the development of the next-generation fully-digital, low-cost, energy-efficient, sub-6 GHz 5G wireless networks.

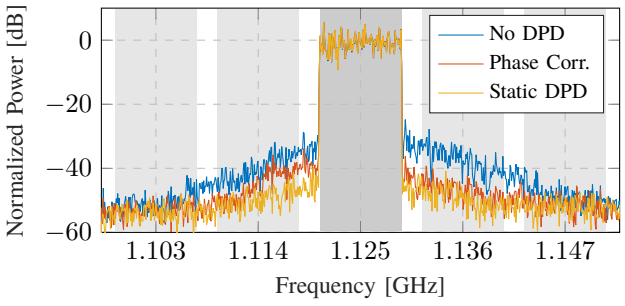


Fig. 7. Measured spectra of the 8.8 MHz 256-QAM signal.

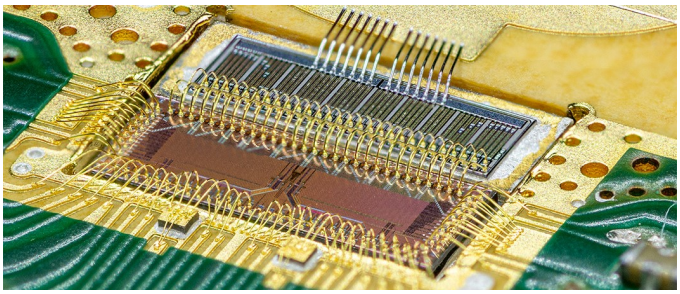


Fig. 8. The bits-in–RF-out, high-power DTX featuring a segmented LDMOS output stage with class-B output match.

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