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Changhao Wang[1,4] Sicong Yuan[2] Hanzhi Xun[2] Chaobo Li[4] Mottaqiallah Taouil[2] Moritz Fieback[2]
Danyang Chen[3] Xiuyan Li[3] Lin Wang[3] Riccardo Cantoro[1] Chujun Yin[4] Said Hamdioui[2]
[1] Politecnico di Torino, Torino, Italy [2]TU Delft, Delft, The Netherlands [3]Shanghai Jiao Tong University, Shanghai, China
[4] Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
Email: {riccardo.cantoro}@polito.it {s.yuan-4, h.xun, m.taouil, m.c.r.fieback, s.hamdioui}@tudelft.nl
{lin_wang, c19970528, xiuyanli}@sjtu.edu.cn {wangchanghao, lichaobo, yinchujun}@ime.ac.cn

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***Abstract*—As emerging non-volatile memory (NVM) devices, Ferroelectric Field-Effect Transistors (FeFETs) present distinctive opportunities for the design of ultra-dense and low-leakage memory systems. For matured FeFET manufacturing, it is extremely important to have an understanding of manufacturing defects and accurately model them to develop effective test solutions. This paper introduces a comprehensive framework for defect and fault modeling, which enables the development of test solutions. First, a classification of FeFET manufacturing defects is provided; both conventional defects (such as contacts and interconnect defects) as well as unique FeFET defects are discussed. The latter FeFET specific defect leads to unique faults that cannot be adequately described using traditional modeling approaches. Then, the Device-Aware Test (DAT) method is used to effectively and appropriately model, analyze and develop test solutions for such unique defects; the approach will be illustrated for Stuck-at-Polarization (SAP) defects.**

I. Introduction

Ferroelectric Field-Effect Transistors (FeFETs) are emerging as one of the most promising Non-Volatile Memories (NVMs) technologies, owing to their low driven voltage, low power consumption, high speed, and high compatibility with CMOS [1]. However, these FeFETs exhibit high susceptibility to manufacturing defects due to the specific working mechanisms, like the multi-domain switching mechanism in the FE layer [2]. Hence, dedicated test solutions are critical for the future development of FeFET manufacturing.

In this paper, we present the framework of test development for FeFETs. Firstly, we categorize the defects in FeFETs into two types: 1) conventional defects, and 2) unique defects. Conventional defects are modeled with *linear resistors*; unique defects are modeled using the device-aware test (*DAT*) approach [3–5]. Taking Stuck-at-Polarization (*SAP*) defects as an example, we illustrate the effectiveness of the DAT approach for FeFET testing. To the best of our knowledge, this is the first work to introduce a framework for FeFET testing, effectively and accurately modeling and simulating FeFET defects. The main contributions of this paper are as follows:

- Establish guidelines for testing conventional and unique defects in FeFETs.
- Design the device-aware defect model for SAP defects and calibrate it with the measurement data.
- Apply the DAT approach for SAP defects to develop a fault model and test solution.

The rest of this paper is structured as follows. Section II establishes the background of FeFET from the device to the circuit level. Section III provides an overview of the FeFET testing framework. Section VI to IV applies DAT approach to SAP defects. Finally, Section VII discusses and concludes the paper.

II. Background

This section outlines the FeFET structure, the 1T-1R cell configuration, and the FeFET array.

A. FeFET Device

FeFETs share a similar structure with Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). The primary distinction lies in replacing the high-κ dielectric layer with a ferroelectric (FE) layer. Typically, FeFET adopts a metal-FE–metal-insulator-semiconductor (MFMIS) structure, as depicted in Fig. 1a [6]. FE materials exhibit a characteristic polarization–voltage (PV) hysteresis. The two polarization states signify distinct stored values (see Fig. 1b). For n-type FeFET, downward polarization attracts minority carriers toward the channel, enhancing its conductivity and resulting in a low threshold voltage state (LVT). Conversely, upward polarization repels these carriers, diminishing channel conductivity and inducing a high threshold voltage (HVT) [6]. These two distinct threshold voltage states are employed for binary information storage (HVT-logical '0', LVT-logical '1'). The difference in threshold voltages corresponding to a current level of $1 \cdot 10^{-9}$ is the Memory Window (MW), defined as $\mathrm{MW} = \mathrm{HVT} - \mathrm{LVT}$ [7].

B. FeFET Cell and Array

The FeFET cell configuration utilized in this work is the 1T (FeFET)-1R (Resistor) structure. As shown in Fig. 1c, BL, WL, and SL refer to bit line, word line, and select line, respectively. WL is used to control the conduction of the transistors for accessing data stored in the desired unit. BL and SL are set to voltages suitable for write and read operations. Fig. 1d illustrates the 1T-1R NOR memory architecture. Cells within the same row share common WL and SL connections, while those within the same column share the same BL connections. The peripheral circuits consist of the BL decoder

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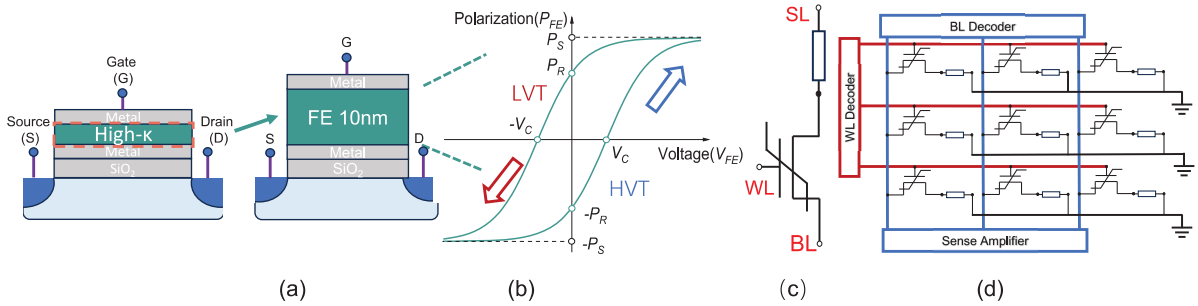

Fig. 1. (a) FeFET structure. (b) PV hysteresis. (c) 1T-1R cell. (d) A 3 × 3 FeFET NOR memory architecture.

Fig. 2. FeFET test development framework.

(BLD), the SL decoder (SLD), the WL decoder (WLD), and the Sense Amplifier (SA). During a read operation, the SA detects the current flowing through the cell and compares it to a reference [8, 9]. This study employs the MFMIS FeFET and NOR array. The proposed framework and results remain applicable to other structures and array configurations.

III. Framework of FeFET Test Development

In this section, we describe the proposed FeFET testing framework as illustrated in Fig. 2. Subsequently, we systematically categorize and classify all potential defects that might arise during the fabrication of FeFETs.

A. Test Development Approach

Our proposed FeFET testing framework relies on precise defect and fault modeling to generate better-quality test solutions with higher time efficiency. The framework shown in Fig. 2 is comprised of three steps as follows:

- Defect modeling: This framework begins by categorizing defects and then employs different defect modeling approaches for two defect types. Conventional defects may occur during standard CMOS fabrication steps. These defects are typically modeled using linear resistors. However, due to the nonlinear characteristics of unique defects, such models struggle to accurately capture the behavior of devices with unique defects [10]. Therefore, device-aware modeling is employed for the unique defects model.
- Fault modeling: Initially, the fault space is defined to describe all potential faults in the presence of defects. Conventional defects are typically represented using linear resistor fault models, while the developed FeFET fault models accurately capture the faulty behavior of unique defects.
- Test development: Test solutions, including the March algorithm and specialized Design-for-Testability (DfT), are generated to detect the faults within the previously fault space.

B. Defects in FeFET

The manufacturing process of FeFET involves standard CMOS manufacturing steps along with the deposition of the FE layer. According to the manufacturing stage, defects in single-cell can be categorized into Front-End-of-Line (FEOL) and Back-End-of-Line (BEOL) defects. Fig. 3b depicts the FEOL process used in this work, which is a typical manufacturing process for FeFETs [11].

1) Conventional defects: Given the extensive research on conventional defects potentially arising during typical CMOS fabrication processes, only a concise overview is provided here. Table I lists most known potential conventional defects. Resistors commonly model these well-studied conventional defects [12, 13].

2) Unique defects: Unique defects that are primarily concentrated in the FE layer (the HZO depicted in Fig. 3a), hence they typically belong to FEOL defects. Next, we will comprehensively outline the potential unique defects at each stage of the distinct FeFET fabrication process.

The FE layer is typically deposited through Atomic Layer Deposition (ALD), as shown in Fig. 3b. The deposition temperature affects the material and electrical properties. However, factors such as uneven heating can cause temperature variations, significantly affecting the performance of FeFETs [14].

The subsequent critical step involves depositing the insulator layer (see insulator deposition step in Fig. 3b). The FE layer is closely linked to the insulator layer, making this step prone to unique defects [15]. For instance, line roughness in the insulator layer can prevent it from supplying the necessary charges for FE polarization balance, thereby diminishing the MW and reducing retention and endurance of FeFET [16].

Following the insulator deposition, the next crucial step is crystallization annealing, as illustrated in the crystallization annealing step of Fig. 3b. Annealing temperature and duration directly affect the degrees of crystallinity and polymorph composition in the FE layer, thereby increasing the likelihood of unique defects [17].

In the rest of this paper, we will use the DAT approach [3–5] to develop test solutions for defective FeFETs; we will apply this for SAP defects that are identified based measurements. DAT approach follows the similar framework as shown in

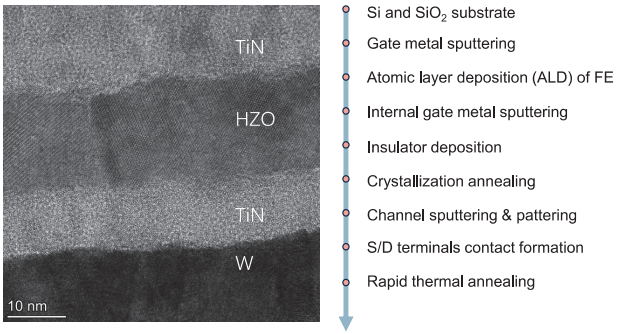

Fig. 3. (a) Cross-section TEM. (b) FEOL processing flow.

TABLE I
CONVENTIONAL DEFECTS CLASSIFICATION.

FEOL	BEOL
Material impurity	Open vias/contacts
Crystal imperfection	Irregular shapes
Polish variations	Big bubbles
Shifting of dopants	Small particles
Patterning proximity	
Line roughness	

Fig. 2, where the defect modeling is a major. Next, the DAT three steps will be applied to SAP defects.

IV. Device-Aware Defect Modeling of SAP

The SAP defects model is designed following these steps.

1) Characterization: While analyzing the measurement data, we observed a significant decrease in the MW for some devices. In Fig. 4, the $I_D - V_G$ curves are compared to characterize devices with and without defects, illustrating their distinct electrical behaviors.

2) Defect-free Model: The defect-free FeFET model is developed by calculating the key parameter 'FE polarization P_{FE}', as follows [18]:

$$\begin{aligned} P_{\text{FE}} &= P_S \cdot \tanh\big(V_{\text{FE}} - \text{dir} \cdot E_C \cdot t_{\text{FE}}\big) \\ V_g &= V_{FE} + V_{MOS} \end{aligned} \tag{1}$$

P_{FE}	FE polarization	P_S	FE layer maximum polarization
V_{FE}	Voltage across the FE layer	dir	Polarization direction
E_C	Coercive field	t_{FE}	FE layer thickness
V_g	Gate voltage	V_{MOS}	Voltage across MOS structure

The relationship between I_d and V_g follows the conventional MOSFET model [19].

3) Physical Defect Modeling: This step models physical defects. To properly model the impact of non-switchable domains on FE polarization. A new parameter α is introduced to represent the percentage of non-switchable domains. presenting SAP-defective FeFET as follows:

$$\text{SAP}^0 : P_{\text{FE}} = P_S \cdot \tanh\big(V_{\text{FE}} - \text{dir} \cdot \alpha \cdot E_C \cdot t_{\text{FE}}\big) \tag{2}$$

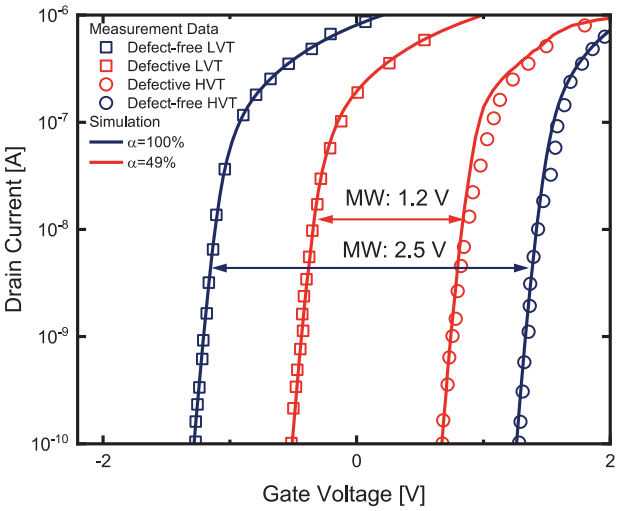

Fig. 4. Defective and device-free devices fitting in the logarithmic y-axis.

$$\begin{aligned} \text{SAP}^{\pm} : P_{\text{FE}} = P_S \cdot \Big(&\tanh\Big(V_{\text{FE}} - \text{dir} \cdot \alpha \cdot E_C \cdot t_{\text{FE}}\Big) \\ &\pm \tanh\Big((1-\alpha) E_C \cdot t_{\text{FE}}\Big)\Big) \end{aligned} \tag{3}$$

Here, α refers to the defect strength, representing the percentage of domains capable of free conversion. When α equals $100\,\%$, it indicates defect-free devices. As α decreases, fixed domains begin to appear and gradually increase in number. The vertical cross-section in the Fig. 5 depicts the process from alpha $100\,\%$ to $0\,\%$, where eventually all domains become non-switchable. The horizontal cross-section illustrates the upward polarization situation, showing that defective domains fail to provide polarization charge. For SAP^0 defect (Equation 2), α represents domains capable of normal conversion. However for $\text{SAP}^{\pm}$ defects, non-switchable domains are fixed in upward or downward polarization. Therefore, defective domains collectively influence the polarization of the FE layer with the normal domains. Consequently, an additional constant term to represent the domains providing fixed polarization (Equation 3). Since the methods and results obtained for both types of defects are similar, this paper primarily discusses SAP^0 defects and highlights the differences with $\text{SAP}^{\pm}$.

4) Electrical Defect Modeling: Following the physical defect analysis, the impacted physical parameters (V_C, α) are integrated into the electrical parameters in this step. The compact Preisach model is described in Verilog-A and integrated into the FeFET compact model [18]. The SAP-defective FeFET model allows for seamless integration into SPICE simulators to further examine how the defect affects the electrical behavior (e.g., current, MW).

α represents the percentage of domains capable of free conversion, which affects V_C, further directly impacting MW. If all domains can switch normally (α = $100\,\%$), MW is maximized. However, MW decreases proportionally when

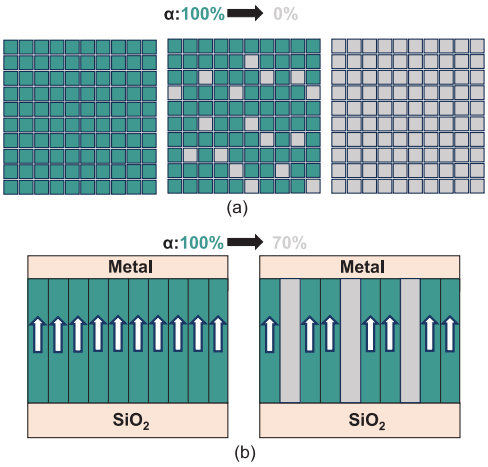

Fig. 5. Upward-polarized FE layer with SAP defects. (a) Vertical cross-section. (b) Horizontal cross-section.

there is a certain percentage of non-switchable domains. As illustrated by the inset graph in Fig. 6, MW and α exhibit a fundamental linear relationship. Although SAP defects all cause the same decrease in MW, they differ in their effects. For SAP^0 defect, the I_D-V_G curves of LVT and HVT change simultaneously, resulting in a decrease of MW. For SAP$^+$ defect, due to the presence of domains fixed in the upward polarization state, the transfer curve exhibits minor changes for all upward-polarized HVT because all domains in this state are 'correct' (albeit with defects). However, for the downward-polarized LVT, the upward-polarized non-switchable domains will counteract with partially downward-polarized domains, leading to a faster rise in the threshold voltage of LVT.

5) Fitting and Optimization: In this step, we calibrate the model obtained in the previous step using measurement data. The fitting is carried out by SPICE simulation and involves two steps: 1) Fitting the performance of the defect-free device. 2) Fitting the performance of the defective device with the parameter α. Fig. 4 illustrates a comparison of I_D-V_G curves between defective and defect-free FeFETs. Firstly, the data of defect-free FeFET is used to calibrate the defect-free model. Then, the defect model is calibrated using data of defective FeFET with $\alpha = 49\,\%$ in Verilog-A. The fitting results indicate that the model accurately describes the behavior of the SAP-defective device, which enables further steps of fault modeling.

V. Device-Aware Fault Modeling of SAP

1) Simulation Setup: Cadence Spectre is employed for circuit-level simulations. The simulation circuit is depicted in Fig. 1d. SAP defects injection is carried out by replacing the defect-free Preisach models with the defective device model [18]. The defect strength is modeled by sweeping alpha from 0 to $100\,\%$, with each α level corresponding to a curve. Besides, We set values above $1 \cdot 10^{-7}$ as storing '1' and values below $1 \cdot 10^{-9}$ as storing '0', so the minimum I_{on}/I_{off} can reach $1 \cdot 10^2$. If the current value lies between the two, 'U' indicates that it flips to an incorrect, undefined state, which may lead

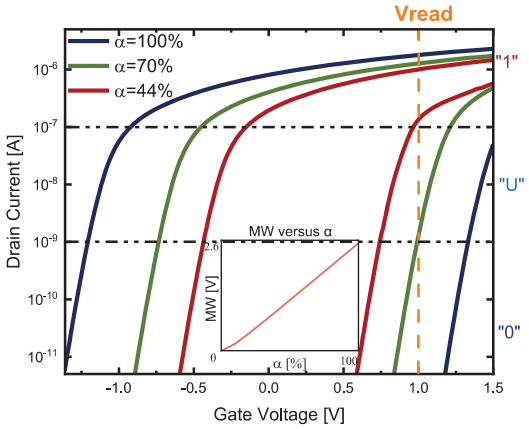

Fig. 6. Faulty behaviors with different α values.

TABLE II
FAULT ANALYSIS RESULTS.

$\alpha\%$	MW[V]	Fault	Type
$(0, 44\%)$	0-0.98	$\langle 0w0/1/-\rangle$	EtD
		$\langle 1w0/1/-\rangle$	
		$\langle 0r0/1/1\rangle$	
$(44\%, 59\%)$	0.98-1.43	$\langle 0r0/U/1\rangle$	
		$\langle 0w0/U/-\rangle$	HtD
		$\langle 1w0/U/-\rangle$	
$(59\%, 70\%)$	1.43-1.76	$\langle 0r0/U/0\rangle$	
		$\langle 0w0/U/-\rangle$	
		$\langle 1w0/U/-\rangle$	
$(70\%, 100\%)$	1.76-2.53	Fault free	

to functional errors during reading. Moreover, $1\,\mathrm{V}$ is chosen as the read voltage, which is a reasonable and conservative value. In practical applications, a higher read voltage is often used to achieve faster reading [20]. As shown in Fig. 6, when a read voltage is fixed, as MW decreases, the difference between high and low threshold voltages narrows. When it narrows to a certain extent, functional errors occur.

2) Device-Aware Fault Modeling and Analysis: The results are shown in Table II. It indicates that SAP defects have a stronger effect on the '0' state. As α decreases to $70\,\%$, the stored value becomes 'U', and The readout may be either '1' or '0' resulting in faults classified as *Hard-to-Detect (HtD)*. While α is $44\,\%$, the stored value is the incorrect '1' (see Fig. 6) leading to faults as *Easy-to-Detect (EtD)*. In practical applications, when selecting a higher read voltage and I_{on}/I_{off}, a smaller defect strength is sufficient to cause functional errors. In addition, since the choice of read voltage is typically high, The impact of SAP$^-$ defect is relatively minor because it hardly affects the HVT I_D-V_G transfer curve. While the faults caused by SAP$^+$ defect are more serious.

VI. Device Aware Test Development of SAP

The last step of the DAT approach involves devising effective test solutions for faults induced by SAP defects. As depicted in Table II, SAP defects result in faults during read '0'

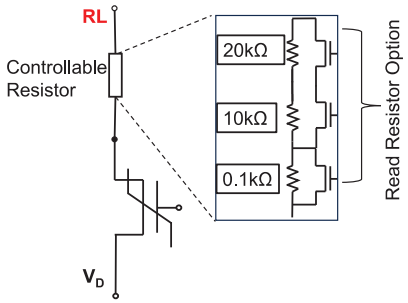

Fig. 7. Controllable resistor to adjust the current.

and write '0' operations. Detecting EtD faults can be reliably achieved by implementing March algorithm [3]:

$$March - SAP = \{\Updownarrow (w1); \Updownarrow (w0, r0)\}$$

The procedure begins by writing 1 to initialize the memory cell to state '1', followed by writing '0' and reading '0' operations to detect faults. This test algorithm ensures the detection of EtD faults.

However, DfT is required to detect HtD faults because the March algorithm fails to meet the fault detection with the 'U' state, which can lead to random read outputs [21]. Specifically, this involves adding reference resistors so that the SA can differentiate current states between 'U'/'1' or 'U'/'0' instead of solely distinguishing the regular '0'/'1' [22]. In Fig. 7, We use a controllable resistor to adjust the magnitude of the reference current. This enables the detection of the 'U' state, with reference line (RL) connecting to the current-steering SA [23]. Our work employs a 1T1R cell where the resistor Value is $1\,\mathrm{k}\Omega$. The controllable resistor is set to $20\,\mathrm{k}\Omega$ for detecting the '1' and '0' states with a current of I_{ref1}. Then the current for reading the '0' state of the defective device is set to I_{sap}, which is close to I_{ref1} (within the SA margin), so the correct state cannot be read. I_{ref2} (with the controllable resistor set to $10\,\mathrm{k}\Omega$) is established to distinguish between the '1' and 'U' states. Therefore, after performing a read '0' operation for the defective device, employing the I_{ref2} allows for correct differentiation between the '1' and 'U' states based on the readout values.

VII. Discussion and Conclusion

In this paper, we present a comprehensive, high-quality testing framework for FeFETs. Although FeFET circuits vary in their configurations, the proposed framework can be applied to different circuit designs. Firstly, we outline the defects present in FeFETs. Subsequently, we propose different modeling and testing methods tailored to various types of defects. Conventional defects, such as interconnect and contact defects, are modeled using linear resistor defect modeling. For unique FeFET defects, we employ the DAT approach, with SAP defects serving as an illustrative example. This demonstrates the effectiveness of applying specific modeling techniques to different defect types, with the DAT approach proving particularly powerful for appropriately testing unique FeFET defects.

References

[1] J. Muller *et al.*, "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," en, in *2013 IEEE International Electron Devices Meeting*, Washington, DC, USA: IEEE, Dec. 2013, pp. 10.8.1–10.8.4.

[2] S. Hamdioui *et al.*, "Test and Reliability of Emerging Non-volatile Memories," en, in *2017 IEEE 26th Asian Test Symposium (ATS)*, Taipei City, Taiwan: IEEE, Nov. 2017, pp. 175–183.

[3] M. Fieback *et al.*, "Device-Aware Test: A New Test Approach Towards DPPB Level," en, in *2019 IEEE International Test Conference (ITC)*, Washington, DC, USA: IEEE, Nov. 2019, pp. 1–10.

[4] L. Wu *et al.*, "Electrical Modeling of STT-MRAM Defects," en, in *2018 IEEE International Test Conference (ITC)*, Phoenix, AZ, USA: IEEE, Oct. 2018, pp. 1–10.

[5] M. Taouil *et al.*, *Device aware test for memory units*, US Patent 11,869,612, Jan. 2024.

[6] H. Mulaosmanovic *et al.*, "Ferroelectric field-effect transistors based on HfO_2: A review," en, *Nanotechnology*, vol. 32, no. 50, p. 502 002, Dec. 2021.

[7] N. Zagni *et al.*, "A memory window expression to evaluate the endurance of ferroelectric FETs," en, *Applied Physics Letters*, vol. 117, no. 15, p. 152 901, Oct. 2020.

[8] T. Soliman *et al.*, "Ultra-Low Power Flexible Precision FeFET Based Analog In-Memory Computing," en, in *2020 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA: IEEE, Dec. 2020, pp. 29.2.1–29.2.4.

[9] M. Ullmann *et al.*, "Disturb free programming scheme for single transistor ferroelectric memory arrays," *Integrated Ferroelectrics*, vol. 34, no. 1-4, pp. 155–164, 2001.

[10] M. Fieback *et al.*, "Defects, fault modeling, and test development framework for rrams," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 18, no. 3, pp. 1–26, 2022.

[11] T. Cui *et al.*, "Can interface layer be really free for hf x zr 1-x o 2 based ferroelectric field-effect transistors with oxide semiconductor channel?" *IEEE Electron Device Letters*, 2024.

[12] J. C.-M. Li *et al.*, "Diagnosis of resistive-open and stuck-open defects in digital cmos ics," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 11, pp. 1748–1759, 2005.

[13] M. Sachdev *et al.*, *Defect-oriented testing for nano-metric CMOS VLSI circuits*. Springer Science & Business Media, 2007, vol. 34.

[14] D. Triyoso *et al.*, "Impact of deposition and annealing temperature on material and electrical characteristics of ald hfo2," *Journal of the Electrochemical Society*, vol. 151, no. 10, F220, 2004.

[15] K. Ni *et al.*, "Critical Role of Interlayer in $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric FET Nonvolatile Memory Performance," en, *IEEE Transactions on Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018.

[16] M. Si *et al.*, "The critical role of charge balance on the memory characteristics of ferroelectric field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 68, no. 10, pp. 5108–5113, 2021.

[17] H.-K. Peng *et al.*, "Improved Memory Window and Robust Endurance for Ge P-Channel Ferroelectric FET Memory Using Microwave Annealing Followed by Rapid Thermal Annealing," en, *IEEE Electron Device Letters*, vol. 43, no. 12, pp. 2073–2076, Dec. 2022.

[18] K. Ni *et al.*, "A Circuit Compatible Accurate Compact Model for Ferroelectric-FETs," in *2018 IEEE Symposium on VLSI Technology*, ISSN: 2158-9682, Jun. 2018, pp. 131–132.

[19] B. J. Sheu *et al.*, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE J. Solid-State Circuits*, vol. 22, no. 4, pp. 558–566, 1987.

[20] M. M. Dahan *et al.*, "C-AND: Mixed Writing Scheme for Disturb Reduction in 1T Ferroelectric FET Memory," en, *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 4, pp. 1595–1605, Apr. 2022.

[21] H. Xun *et al.*, "Device-Aware Test for Ion Depletion Defects in RRAMs," en, in *2023 IEEE International Test Conference (ITC)*, Anaheim, CA, USA: IEEE, Oct. 2023, pp. 246–255.

[22] D. Chang *et al.*, "Algorithmic read resistance trim for improving yield and reducing test time in mram," in *2023 IEEE International Test Conference (ITC)*, IEEE, 2023, pp. 87–92.

[23] S. Ghosh, *Sensing of Non-Volatile Memory Demystified*. Springer, 2019.

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