# Dual Voltage and Current Feedback Class-D Amplifiers with High LC Filter Cut-off Frequency and Nonlinearity Suppression

**Master of Science Thesis**

**by**

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# Abstract

Class-D amplifiers have gained significant importance in automotive applications due to its high efficiency. However, to meet strict electromagnetic interference (EMI) requirements, an LC filter is necessary, which, unfortunately, introduces nonlinearity to the system. This project proposes an architecture by implementing a dual voltage/current feedback loop to suppress the nonlinearity of the LC filter. The voltage feedback is put after the LC filter to suppress its nonlinearity. The current feedback splits the complex poles from the LC filter to stabilize the system.

By implementing current feedback as the inner loop, this design achieves a significant reduction in the LC filter's bulk and cost in comparison to state-of-the-art, while maintaining a good total harmonic distortion (THD) level of around -110 dB. This architecture is also robust to +/-30% variations in LC filter cut-off frequency. The chip is fabricated using a 180-nm BCD process, with a die size of 3 mm × 2.28 mm.

**Index items:** Class-D amplifier, LC filer, current feedback, nonlinearity suppression, THD.

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My thesis started in August 2022, when I was still not very familiar with Cadence. Therefore, the starting point was quite difficult for me, and I want to thank those who helped me get through this hard time in the beginning.

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# Chapter 1 Introduction

## 1.1 Backgrounds

Due to their high-efficiency behavior (>90% efficiency), Class-D amplifiers are very suitable to drive a loudspeaker (typically modelled as a low-Ohmic resistor in series of an inductor as shown in Fig. 1.3) in consumer electronics and automotive audio systems. However, compared to conventional Class-AB amplifiers, Class-D amplifiers exhibit high-frequency switching at the output that can result in electromagnetic interference (EMI). The finite rise/fall time of the switching and the commonly applied deadtime control introduces extra nonlinearity.

### 1.1.1 LC filter nonlinearity

In Class-D amplifier applications of automotive systems, an LC filter is necessary due to EMI. However, the inductor and capacitor itself will introduce nonlinearity to the system and affect the overall performance. To mitigate the LC filter nonlinearity's influence, the inductor and capacitor with good linearity should be used in CDAs without LC filter nonlinearity suppression. However, those components with good linearity are often bulky and expensive compared to those with poor linearity, as shown in Table 1.1 and 1.2 [2].

People are trying to reduce the bulk and cost of the LC filter by implementing a feedback loop to suppress the LC filter nonlinearity, known as feedback-after-LC structure. A feedback-after-LC structure with high LC nonlinearity suppression is preferred as it can accommodate the inductor and capacitor with poor linearity without sacrificing system performance to save the bulk and cost. To further reduce the LC filter's bulk and cost, an LC filter with a higher cut-off frequency $f_{\mathrm{LC}}$, i.e., smaller component values is also expected.

Table 1.1 Inductors with different linearity and saturation currents [2]

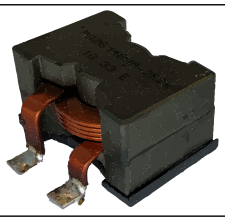
| |  |  |  |
|---|---|---|---|
| Dimension (mm) | 28 x 20 x 16 | 8 x 8 x 7 | 4 x 4 x 2 |
| $I_{SAT}$ | 100 A | 19 A | 3.7 A |
| THD* | -102 dB | -102 dB | -60 dB |
| Cost | $$$ | $$ | $ |

Table 1.2 Capacitors with different linearity

| |  |  |
|---|---|---|
| Dimensions (mm) | 5.7 x 5 x 1 | 2 x 1.2 x 0.5 |
| THD | -100 dB | -60 dB |
| Cost | $$$ | $ |

### 1.1.2 PWM modulation

The PWM modulation produces a square wave whose duty cycle represents the information of the input signal. This is realized by comparing the input signal with a triangle wave with the frequency of $f_{SW}$, which is shown in Figure 1.1.

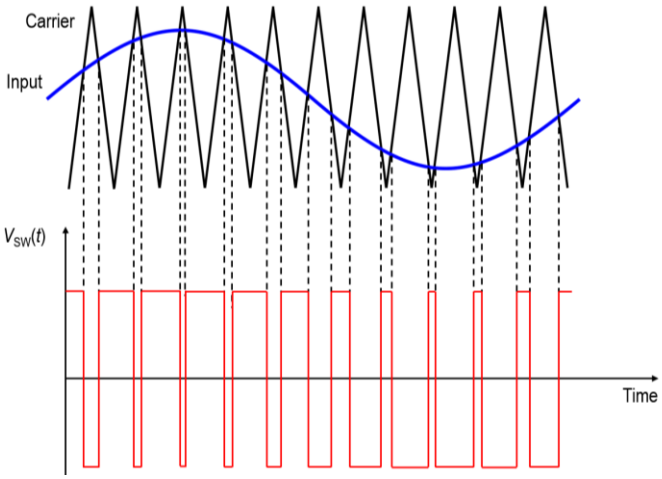



Figure 1.1 Timing diagram of natural sampling PWM. [2]

After PWM modulation, the output signal can be expressed as below:

$$\text{PWM} = M\cos(\omega_s t) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{J_n\left(Mm\frac{\pi}{2}\right)}{m\frac{\pi}{2}} \sin\left((m+n)\frac{\pi}{2}\right)\cos(n\pi)\cos\big((m\omega_c + n\omega_s)t\big)$$

Where M represents the modulation index, $\omega_s$ represents the signal frequency, $\omega_c$ represents the PWM carrier frequency, and $J_n(x)$ represents the $n^{\text{th}}$ order Bessel Function.

Figure 1.2 shows the PWM spectrum with a 2 kHz -20 dB input signal, and $f_{\text{PWM}} =$ 100 kHz. By incorporating an LC low-pass filter, the input signal can be recovered.

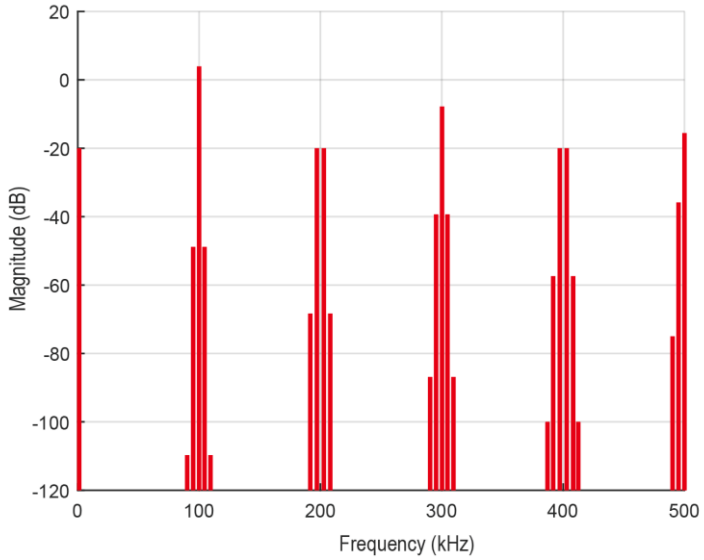



Figure 1.2 PWM spectrum

### 1.1.3 Class-D output stage

The high efficiency of Class-D amplifiers comes from their distinct switching behavior, which sets them apart from conventional Class-AB amplifiers. In Class-D amplifiers, power transistors function as switches (operates in linear region) and ideally have no power loss. However, in real-world scenarios, power transistors operating in the linear region still experience power loss due to their on-resistance. Nevertheless, this power loss is typically much smaller than that of Class-AB amplifiers, resulting in high power efficiency, often exceeding 90%.

Figure 1.3 illustrates the bridge-tied-load (BTL) configuration, also known as the H-bridge [1], in which the speaker can be modelled as a resistor $R_{\text{SPK}}$ in series with an inductor $L_{\text{SPK}}$. This configuration is widely employed in Class-D amplifiers as it eliminates the need for a negative supply which is often needed in a singled-ended configuration. The audio signal can be recovered from the PWM waveform using an LC

low-pass filter or, in some cases, by the speaker itself, which can be modelled as an R-L series network [2].

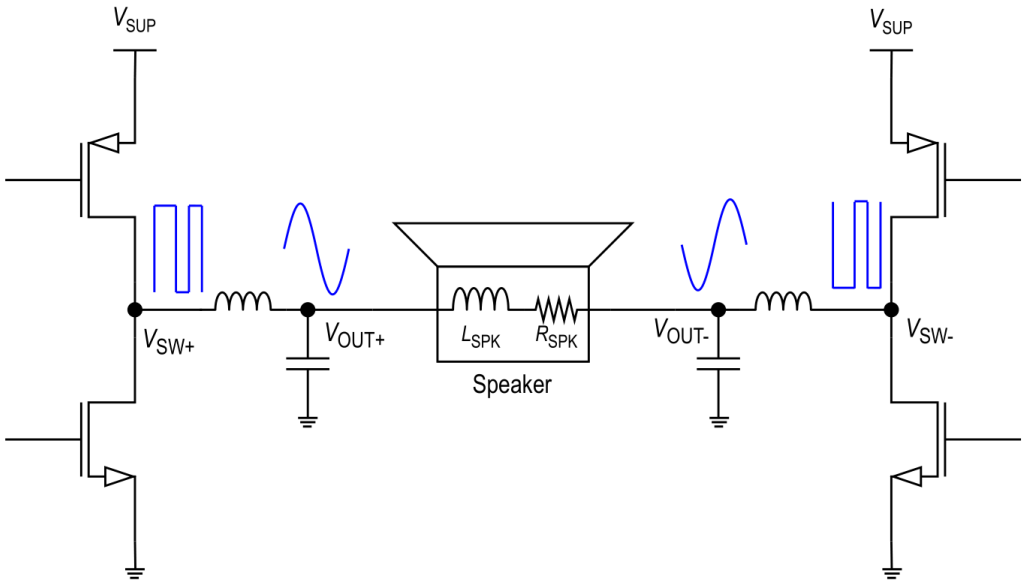



Figure 1.3 Class-D output stage with bridge-tied-load (BTL) configuration. [2]

## 1.2 Open-loop and Closed-loop CDAs

As mentioned in **Section 1.1**, Class-D amplifiers are gaining popularity in automotive applications because of their high-power efficiency. However, Class-D amplifiers also suffer from EMI, which mainly comes from the high-frequency switching behavior in the output stage and is radiated by the long connection cables. Therefore, Class-D amplifiers must fulfil strict EMI standards to achieve good performance.

EMI can be suppressed by implementing fully differential switching behavior and twisting the cables such that their EMI can cancel ideally. However, in reality, this cannot be done perfectly and any mismatch in the fully differential structure could lead to common-mode EMI. Due to the strict EMI requirements, it is also necessary to have an LC filter in the output of the Class-D amplifier to suppress the residual EMI. However, the external LC components are bulky and costly. An LC filter with smaller-sized inductors and capacitors, resulting in a high cut-off frequency, is helpful in achieving lower costs.

As mentioned before, because of the finite rise/fall time of the switching and the commonly applied deadtime control, the output stage of CDAs will introduce significant distortion to the system and reduce the linearity. This becomes more severe

when the switching frequency becomes higher. Therefore, open-loop CDAs without a feedback loop, i.e., output stage nonlinearity suppression can only achieve limited THD value [5], which limits the performance of CDAs. The block diagram for open-loop CDAs is shown in Figure 1.4 (a).

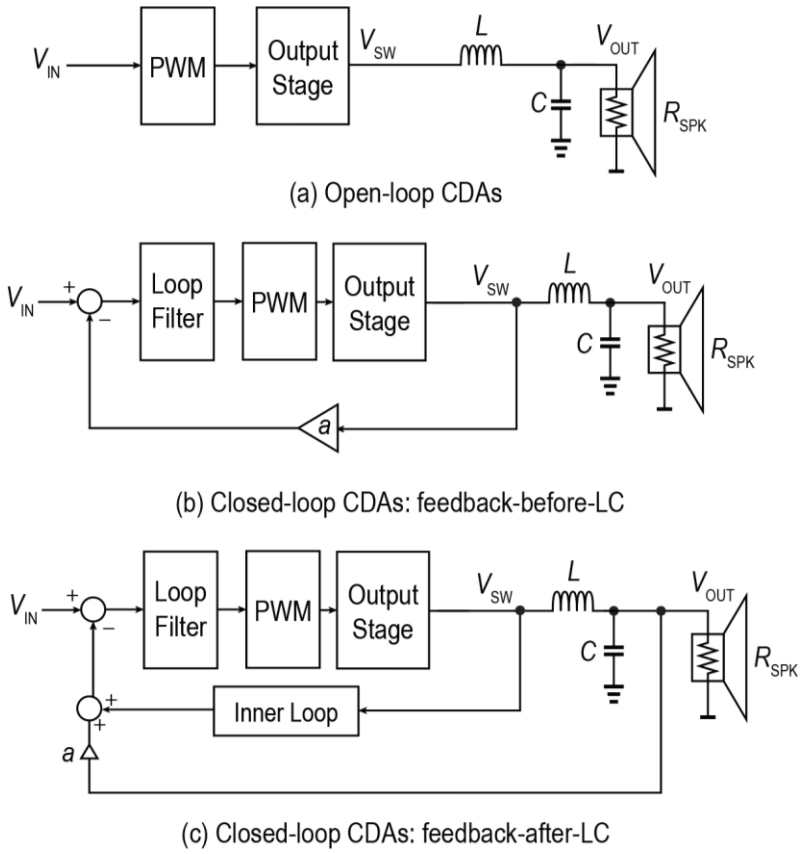



Figure 1.4 Block diagrams for open-loop and closed-loop CDAs.

To address the issue, closed-loop CDAs are implemented to suppress the nonlinearity due to the output stage and LC filter. Figure 1.4 (b) shows the block diagram of the closed-loop CDAs with feedback-before-LC structure. This structure can effectively suppress the nonlinearity of the output stage by incorporating a high gain loop filter. However, this structure cannot suppress the nonlinearity comes from the LC filter, and therefore, can only work with the inductor and capacitor with good linearity.

Figure 1.4 (c) gives the block diagram of feedback-after-LC structure, which uses a dual voltage feedback loop. The outer loop is taken after the LC filter to suppress the nonlinearity. However, this will introduce the LC filter complex poles to the system transfer function and makes the loop unstable. Therefore, an inner loop should be implemented to stabilize the system. By taking the feedback loop after the LC filter, this architecture enables the use of inductors and capacitors with poor linearity while still achieving overall good linearity for the CDAs.

## 1.3 Literature Review

In [3], the authors implemented a fully differential multilevel output stage that operates at a high switching frequency of 4.2 MHz. Thanks to the high switching frequency, the LC filter is designed to be small with a high cut-off frequency of 580 kHz, using a 470 nH inductor and a 160 nF capacitor.

Additionally, this design incorporates a third-order loop filter, enabling a high loop gain of over 82 dB in the audio band. This high loop gain significantly suppresses the nonlinearity of the output stage. By implementing a fully differential multilevel output stage, utilizing a LC filter with small component sizes, and incorporating a third-order loop filter with high loop gain for nonlinearity suppression, this design effectively addresses the challenges of achieving high linearity and low EMI in Class-D amplifiers.

However, a drawback of this approach is that the feedback loop, shown in Figure 1.5, is unable to suppress the nonlinearity introduced by the LC filter. This limitation arises because the feedback is taken from the switching nodes, which are positioned before the LC filter. Consequently, this structure requires the use of inductors and capacitors with good linearity to maintain good performance. Unfortunately, components with good linearity typically have larger physical sizes and higher costs compared to those with poorer linearity.

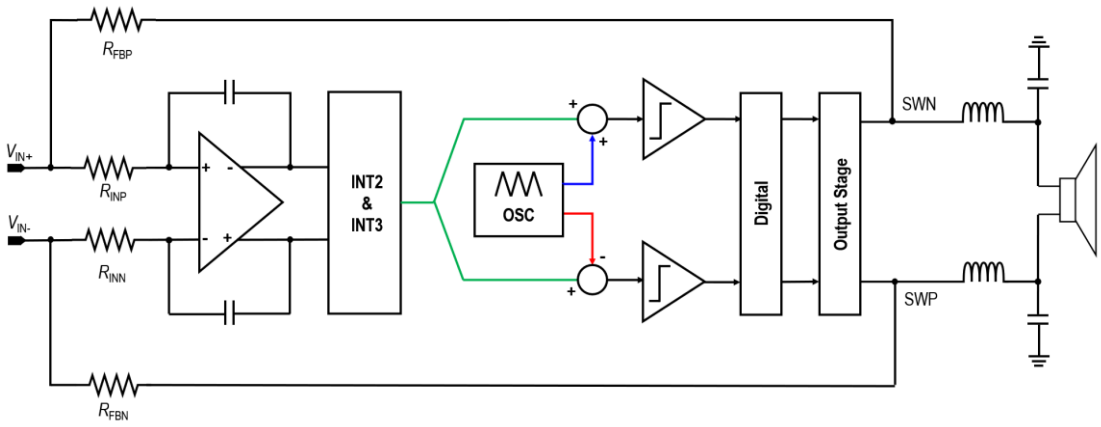



Figure 1.5 System-level block diagram of the Class-D amplifier in [3].

To suppress the nonlinearity of the LC filter, [4] proposes a feedback-after-LC structure, as shown in Figure 1.6. The inner loop consists of an integrator, a forward path with a PI compensator, a 1$^{st}$ order low-pass filter, and a PWM generator. The inner loop's closed-loop response has one low-frequency zero and another high-frequency pole, which acts as a lead compensator to provide extra PM. The outer loop is implemented after the LC filter and suppresses the nonlinearity introduced by nonlinear inductor and

capacitor. In this structure, the capacitor's error source is modelled as a current source $I_{NL,C}$ in parallel with the capacitor, which is equivalent to the voltage source $V_{NL,C} \approx sL \cdot I_{NL,C}$ in audio band. Therefore, both the inductor and capacitor's nonlinearities are suppressed by $\frac{L_2+L_1}{1+L_1}$, since $V_{\mathrm{SW}} + a \cdot V_{\mathrm{OUT}} \approx 0$. Therefore, when $L_2$ >> $L_1$ and $L_1$ >>1 the LC filter nonlinearity is suppressed by $\frac{L_2}{L_1}$, but when $L_2$ << $L_1$, the suppression vanishes. The output stage's nonlinearity is suppressed by $L_1 + L_2$, or whichever loop gain that dominates.

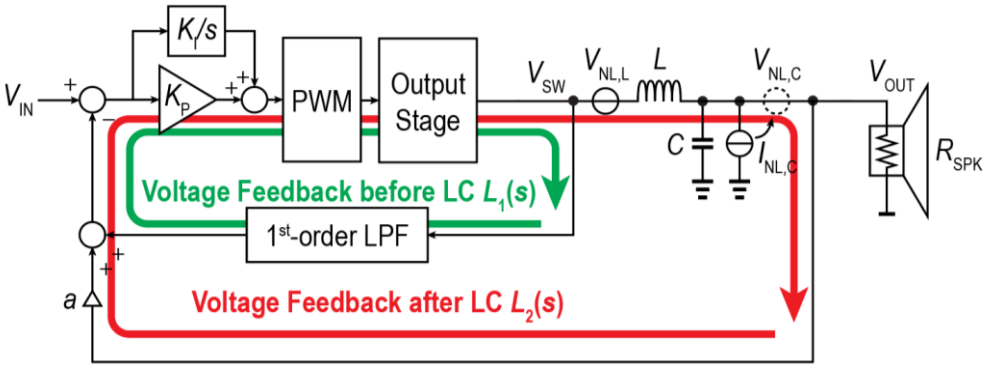



Figure 1.6 Block diagram of the Class-D amplifier in [4].

With the dual-feedback structure, this design can suppress the LC filter nonlinearity by 49 dB and is robust to +/-30% LC filter cut-off frequency variation. Because of the feedback-after-LC structure, this architecture can use the inductor and capacitor with poorer linearity without compromising the system's linearity. The inductor and capacitor with poorer linearity usually have smaller sizes and lower prices, which contributes to reducing system bulk and cost. With +/-30% LC filter cut-off frequency variation, this structure is robust to 62~106 kHz $f_{LC}$ without extra programming.

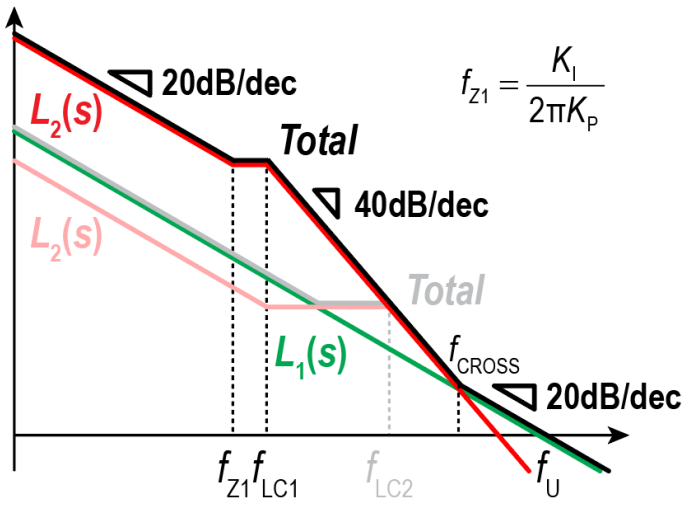



Figure 1.7 Loop gain around LC filter with two $f_{LC}$ values [6].

However, if the LC filter's cut-off frequency is increased to a higher value, the in-band loop gain will have to be reduced [6], as explained below. Figure 1.7 shows the loop gain around the output stage with two LC cut-off frequencies: $f_{\mathrm{LC1}}$ and $f_{\mathrm{LC2}}$, and $f_{\mathrm{z1}}$ represents the zero introduced by the PI compensator. When the $f_{\mathrm{LC}}$ is increased from $f_{\mathrm{LC1}}$ to $f_{\mathrm{LC2}}$, to maintain the same phase margin for stability, $f_{\mathrm{CROSS}}$ should stay the same, and therefore the outer loop gain $L_2(s)$ must be reduced accordingly. This is undesirable since $\frac{L_2+L_1}{1+L_1}$ determines the LC filter nonlinearity suppression and should be as high as possible. Increasing both $f_{\mathrm{PWM}}$ and $f_{\mathrm{CROSS}}$ can solve the issue but is also undesirable as higher $f_{\mathrm{PWM}}$ leads to higher idle power consumption.

Based on the previous discussion, it is not possible to allow a LC cut-off frequency higher than 106 kHz in this structure due to the in-band loop gain's requirement. Although this architecture can work with the inductor and capacitor with poorer linearity, the achievable LC cut-off frequency has been significantly reduced compared to [3].

## 1.4 Design Targets

[3] needs to work with the inductor and capacitor with good linearity, and although [4] can work with the inductor and capacitor with poorer linearity, the component values become larger. To address the drawback in both [3] and [4], the following design targets should be considered:

- High LC cut-off frequency with ±30% tolerance: The main advantage of this work is to achieve a higher LC cut-off frequency in the feedback-after-LC structure. Therefore, smaller inductors and capacitors can be used, which helps to further reduce LC filter bulk and cost. It is essential to ensure that the design remains robust with a +/- 30% variation in the values of the inductors and capacitors.
- Total Harmonic Distortion (THD) < -110 dB: This specification can be achieved by implementing a third-order loop filter that provides nonlinearity suppression of at least 70 dB. The loop filter's design should be optimized to effectively reduce distortion and maintain high audio quality.
- Stability: The design should remain stable in the presence of LC variations mentioned above. Additionally, the unity-gain frequency should be kept lower than $f_{PWM}/\pi$ to guarantee stable PWM operation [1].

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# Chapter 2 Architecture-level Design

In **Chapter 1**, the basics of the Class-D amplifier has been discussed. By analyzing the existing literature, the design target has been put forward. This chapter will focus on the system-level design with ideal OTAs and ideal current sensing blocks with realistic specifications to verify whether the system can achieve the design target or not.

## 2.1 Block diagram

In this project, a feedback-after-LC structure implementing current feedback as the inner loop is proposed based on the discussions in **Sections 1.2 and 1.3**. The proposed architecture-level block diagram is shown in Figure 2.1.

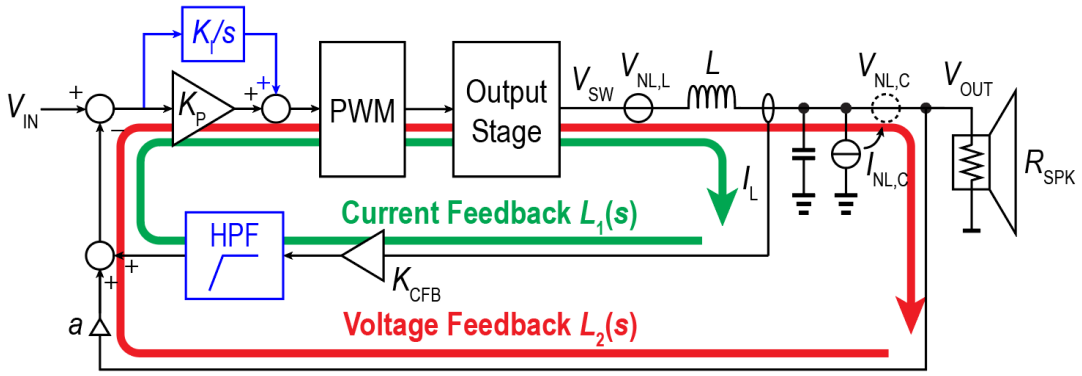



Figure 2.1 Block diagram of the proposed structure.

This structure implements a dual voltage/current feedback loop, comprising an inner and outer loop. The outer loop, referred to as the voltage feedback $L_2(s)$, is positioned after the LC filter, with the purpose of suppressing its nonlinearity. The inner loop, marked as the current feedback $L_1(s)$, serves to split the complex poles of the LC filter and stabilize the system. A thorough analysis of this will be presented in **Section 2.4.**

A HPF is integrated into the current feedback $L_1(s)$ to improve the capacitor's nonlinearity suppression in the audio band. Details will be given in **Sections 2.2 and 2.5**.

$K_P$ and $K_I/s$ forms a PI compensator in the inner loop, which is used to boost the in-band loop gain to better suppress the nonlinearity of the output stage and LC filter. To achieve the design target of > 70 dB loop gain, a second-order resonator will later be placed in the outer loop to further boost the loop gain. The PI compensator and resonator's transfer functions are chosen to fulfill both the phase margin and in-band

loop gain requirement. A comprehensive discussion on the design process of the resonator and PI compensator will be provided in **Chapter 3**.

This structure shows different behavior at low and high frequencies due to the presence of the HPF. At low frequency, the HPF and PI compensator's pole and zero cancel each other, making $L_1(s)$ a constant small value. Therefore, the voltage feedback $L_2(s)$ is dominated. The PI compensator contributes a higher loop gain, enabling the voltage feedback loop to better suppress the nonlinearity of both the LC filter and output stage within the audio band, which will be explained in detail in **Section 3.5**.

At high frequency, the transfer function of the HPF is 1. Consequently, the current feedback path will play its role to split the complex poles from the LC filter. Detailed calculations for the transfer function of the current feedback loop will be discussed in **Section 2.4**. Since the complex poles are distributed across two different frequencies, they do not instantaneously reduce the phase margin from 180 degrees to 0 degrees. Thus, this structure can maintain some PM, contributing to system stability.

The subsequent subsection will provide an in-depth analysis of the loop gain around the output stage and the LC filter, examining the influence of the inductor and capacitor values on the inner and outer loop's transfer functions.

## 2.2 *L* and *C* nonlinearity suppression

As shown in Figure 2.1, because of the current feedback, the inductor and capacitor have been split, and their nonlinearity should be analyzed separately. Regarding the inductor, the nonlinearity can be modelled as a voltage source ($V_{\mathrm{NL,L}}$) in series with the inductor. Therefore, the inductor nonlinearity suppression can be expressed as $L_1 + L_2$, which is the same as in [2]. Regarding the capacitor, the nonlinearity can be modelled as a current source ($I_{\mathrm{NL,C}}$) in parallel with the capacitor.

By implementing the current feedback loop, the inner loop acts as a voltage-controlled current source, whose output impedance has been increased significantly compared to the conventional dual voltage feedback inner loop case. Because of the high inner loop output impedance, the nonlinearity of the capacitor modeled by $I_{\mathrm{NL,C}}$ in Figure 2.1 would mostly flow into the load $R_{\mathrm{SPK}}$, rather than flow through the low-impedance inductor in the dual voltage feedback case, result in an equivalent voltage error source $V_{\mathrm{NL,C}} \approx R_{\mathrm{SPK}} \cdot I_{\mathrm{NL,C}}$, which is much larger than $V_{\mathrm{NL,C}} \approx sL \cdot I_{\mathrm{NL,C}}$ in [2] at the audio band. Therefore, to suppress $V_{\mathrm{NL,C}}$ at the audio band, it is necessary to implement an HPF in the inner loop.

After implementing the HPF, $L_1 \approx \frac{H_{\mathrm{PI}}}{R_{\mathrm{SPK}}} \cdot K_{\mathrm{CFB}} \cdot H_{\mathrm{HPF}}$ at the audio band, and $L_2 = H_{\mathrm{PI}} \cdot H_{LC} \cdot a \approx a \cdot H_{\mathrm{PI}}$ at the audio band. Because of the integrator, $\frac{V_{\mathrm{SW}}}{R_{\mathrm{SPK}}} \cdot K_{\mathrm{CFB}} \cdot H_{\mathrm{HPF}} + a \cdot V_{\mathrm{OUT}} \approx 0$. Therefore, the capacitor's nonlinearity is suppressed by $\frac{L_2+L_1}{1+L_1}$. Since in this case, $L_1 << L_2$, it can be simplified to $L_2/(1+L_1)$.

Figure 2.2 shows the plot of the $L_1(s)$ and $L_2(s)$. With $f_{\mathrm{LC2}}$, i.e., a reduced $L$ and $C$, to keep the same $f_{\mathrm{CROSS}}$, $L_1(s)$ and $L_2(s)$ should decrease accordingly since $H_{\mathrm{PI}}$ has to reduce. This would lead to a reduced nonlinearity suppression to the output stage and inductor since $L_2(s)$ reduces. However, since the capacitor nonlinearity is suppressed by $L_2/(1+L_1)$, and $L_1 << L_2$, therefore it stays the same.

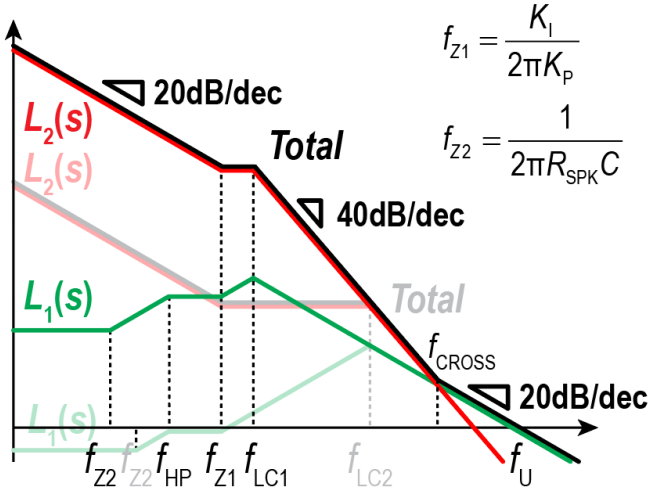



Figure 2.2 Plot for $L_1(s)$ and $L_2(s)$ with two $f_{\mathrm{LC}}$ values.

## 2.3 Inner loop's transfer function

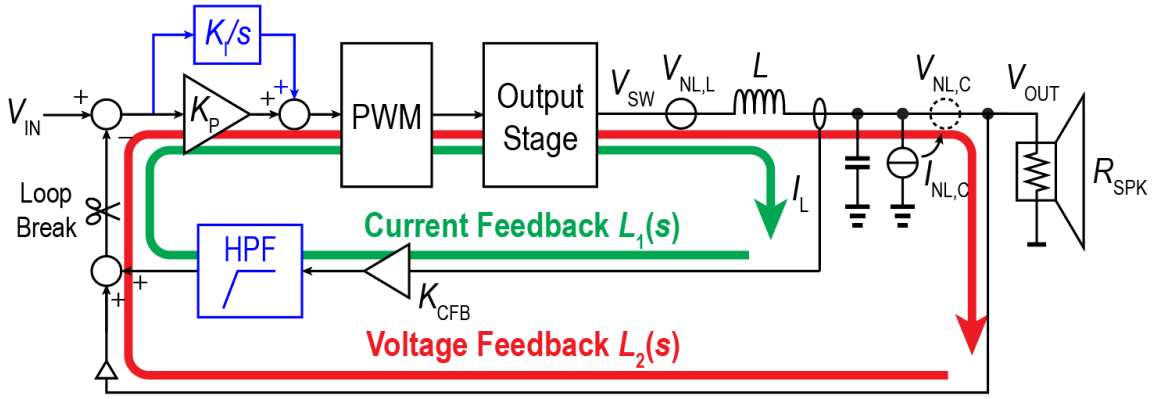



Figure 2.3 Inner loop break point.

To calculate the inner loop's transfer function, the loop should be broken at the point shown in Figure 2.3. $K_{\mathrm{cfb}}$ is the gain factor of the current feedback loop, $C_1(s) = K_P + K_I/s$ represents the transfer function of the PI compensator and therefore, the inner loop's transfer function can be calculated as follows:

$$G_{\mathrm{loop,inner}} = C_1(s)G_{\mathrm{PWM}} \cdot \left[\frac{K_{cfb}}{sL + Z_L} \cdot \frac{s}{s + 2\pi f_{\mathrm{HP}}} + H_{\mathrm{LC}}(s)\right]$$

$$Z_L = \frac{1}{sC} // sL_s + R_s$$

Where $f_{\mathrm{HP}}$ represents the corner frequency of the HPF, and $G_{PWM}$ represents the gain factor of PWM modulation.

As discussed before, because of the HPF, it is more convenient to analyze the loop at low-frequency and high-frequency separately:

At low frequency (audio band), $L_1(s)$ is much smaller than $L_2(s)$. Therefore, the inner loop's transfer function can be simplified as follows:

$$G_{loop,inner} \approx C_1(s)G_{\mathrm{PWM}}$$

At high frequency, the current feedback $L_1(s)$ becomes non-neglectable. Therefore, the inner loop's transfer function can be simplified as follows:

$$G_{\mathrm{loop,inner}}(s) \approx \frac{G_{\mathrm{PWM}}K_{\mathrm{p}}K_{\mathrm{cfb}}C \cdot s + G_{\mathrm{PWM}}K_{\mathrm{p}}}{s^2LC + 1} \approx \frac{G_{\mathrm{PWM}}K_{\mathrm{p}}K_{\mathrm{cfb}}}{sL}$$

From the above equation, the unity-gain bandwidth can be estimated as follows:

$$f_{ug,inner} = \frac{G_{\mathrm{PWM}}K_{\mathrm{p}}K_{\mathrm{cfb}}}{2\pi L}$$

Therefore, the inner loop's unity-gain bandwidth is inversely proportional to the inductor value. If the inductor gets smaller, due to the unity-gain frequency requirement that $f_{ug} < f_{PWM}/\pi$, either $K_{\mathrm{p}}$ or $K_{\mathrm{cfb}}$ needs to be reduced. If $K_{\mathrm{p}}$ is reduced, to maintain the in-band loop gain, PI compensator's zero frequency must increase, resulting in a lower PM, as shown in Figure 2.4 (left). On the other hand, $K_{\mathrm{cfb}}$ can be reduced, but this will result in a larger outer loop's unity-gain frequency $f_{\mathrm{ug,outer}}$, which will be discussed in **Section 2.4**. This will bring $f_{\mathrm{ug,inner}}$ and $f_{\mathrm{ug,outer}}$ closer, resulting in a lower system PM. To meet the PM requirement, $K_{\mathrm{I}}$ must reduce to keep the zero frequency the same, resulting in a smaller in-band loop gain, as shown in Figure 2.4 (right).

Hence, to maintain an enough PM, there is a lower limit for the inductor's value.

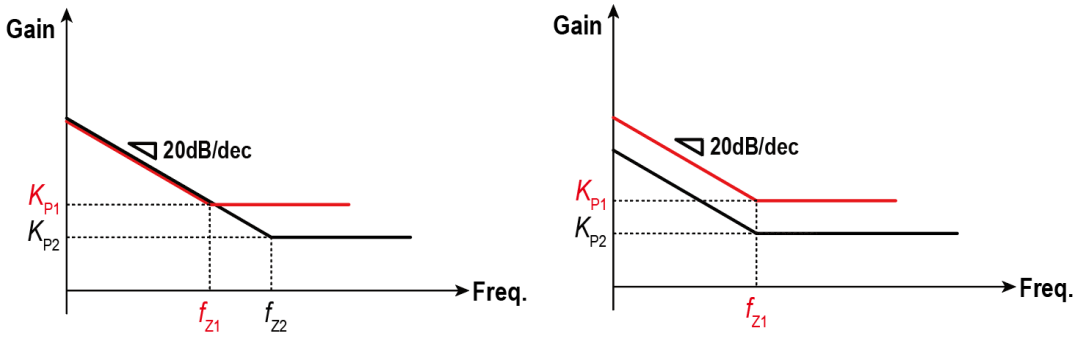



Figure 2.4 PI compensator with different $K_P$ values

With a different inductor value, the achievable phase margin will also change. Assume the capacitor value is kept the same and only the inductor value is changed. The inner loop's gain and phase plots with different inductor values are shown in Figure 2.4.

The inner loop's transfer function can be simplified as follows:

$$G_{\text{loop,inner}}(s) \approx \frac{G_{\text{PWM}}K_{\text{p}}K_{\text{cfb}}C \cdot s + G_{\text{PWM}}K_{\text{p}}}{s^2LC + 1} = (A + B \cdot s) \cdot H_{LC}(s)$$

In Figure 2.5, the black and red curves are used to represent $H_{\text{LC}}(s)$ with two inductor values. The yellow curve represents the constant transfer function $A + B \cdot s$. The blue and green curves are used to represent the inner loop's transfer function with two inductor values. In Figure 2.4, $L_1 < L_2$, and therefore $f_{LC1} > f_{LC2}$.

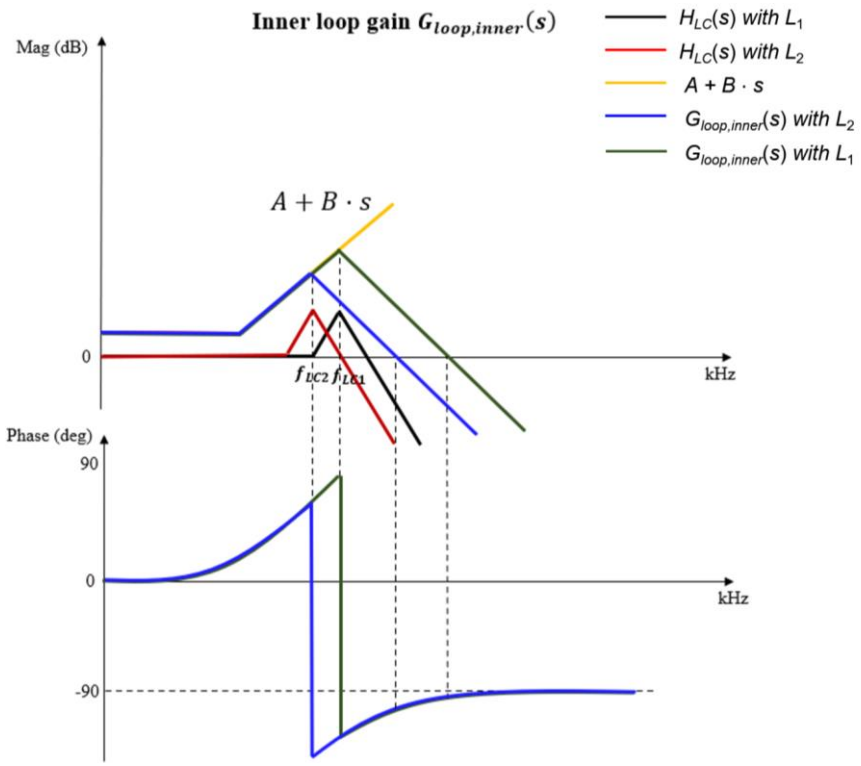



Figure 2.5 Phase plot for inner loop's transfer function with two inductor values.

From Figure 2.5, a larger inductor value $L_2$ will decrease the unity-gain frequency and therefore reduce the phase margin. Therefore, the inductor value in this structure also cannot go too large, as this will decrease the phase margin and makes the system unstable.

Assume the inductor value is kept the same and only the capacitor value is changed, a similar plot as Figure 2.5 can be drawn. It turns out that a larger capacitor will move the zero to a lower frequency, which contributes to improving the phase margin. On the other hand, a smaller capacitor will move the zero to a higher frequency, reducing the PM.

## 2.4 Outer loop's transfer function

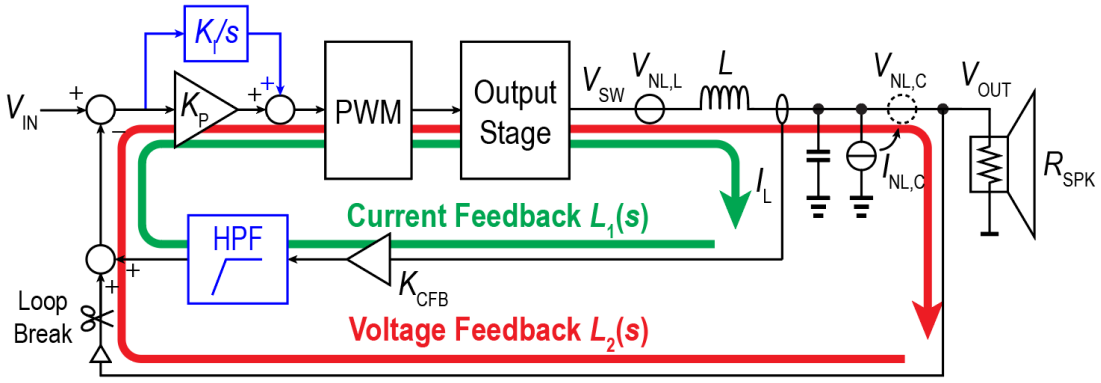



Figure 2.6 Outer loop break point

To verify the stability of the outer loop, it is necessary to break the loop at the point shown in Figure 2.6. To facilitate the calculation of the outer loop's transfer function, it can be calculated as follows:

$$G_{\text{loop,outer}}(s) = H_{\text{CL,inner}}(s) \cdot Z_L \approx \frac{H_{\text{CL,inner}}(s)}{sC}$$

The closed-loop transfer function can be calculated as follows:

$$H_{\text{CL,inner}}(s) = \frac{C_1(s)G_{\text{PWM}} \cdot sC}{s^2LC + 1 + C_1(s)G_{\text{PWM}}K_{\text{cfb}} \cdot sC \cdot \frac{s}{s + 2\pi f_{\text{HP}}}}$$

From the above equation, with the current feedback path, the denominator for the inner loop has changed form, from $(A \cdot s^2 + B)$ to $(A \cdot s^2 + Bs + C)$, showing how the inner loop splits the complex poles. With details of $H_{\text{CL,inner}}(s)$, it is easy to calculate the outer loop's transfer function as shown below:

$$G_{\text{loop,outer}}(s) = \frac{H_{\text{CL,inner}}(s)}{sC} = \frac{C_1(s)G_{\text{PWM}}}{s^2LC + 1 + C_1(s)G_{\text{PWM}}K_{\text{cfb}} \cdot sC \cdot \frac{s}{s + 2\pi f_{\text{HP}}}}$$

By plotting the transfer function of $H_{\text{CL,inner}}(s)$ in MATLAB, the magnitude close to the outer loop's unity-gain frequency $f_{\text{ug, outer}}$ is found to be almost constant and is equal to $1/K_{\text{cfb}}$, as shown in Figure 2.7.

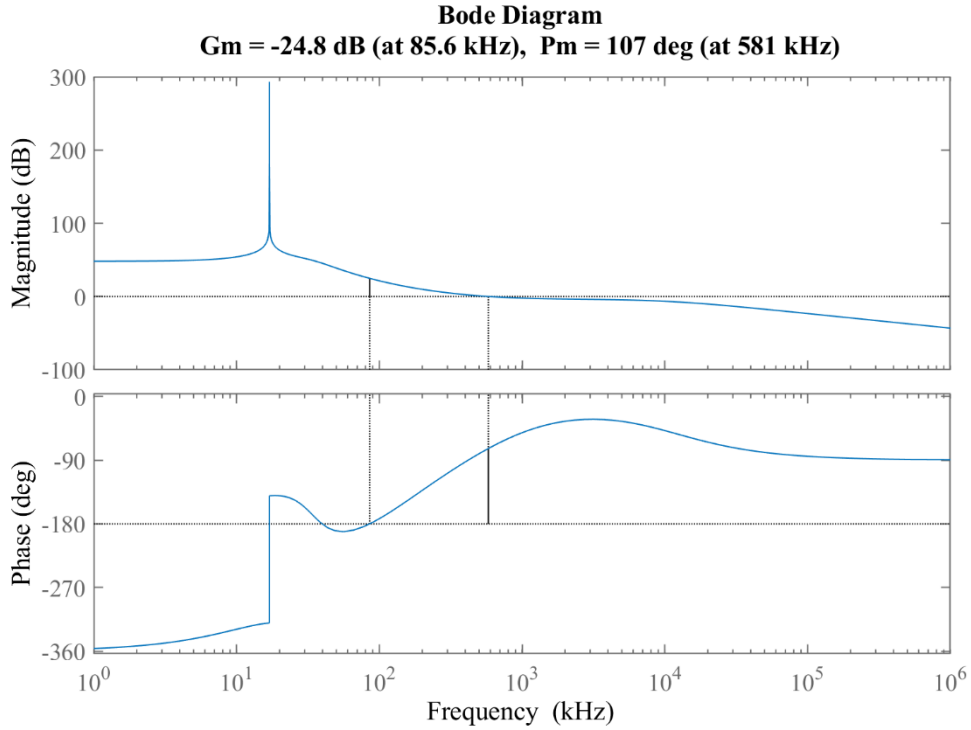



Figure 2.7 Bode diagram of $H_{\text{CL,inner}}(s)$.

Therefore, at high frequency, the outer loop's transfer function and its unity-gain bandwidth can be simplified to:

$$G_{\text{loop,outer}}(s) = \frac{H_{\text{CL,inner}}(s)}{sC} \approx \frac{1}{sC \cdot K_{\text{CFB}}}$$

$$f_{\text{ug, outer}} \approx \frac{1}{2\pi C \cdot K_{\text{CFB}}}$$

The unity-gain frequency of the outer loop is inversely proportional to the capacitor value, and a smaller $K_{\text{CFB}}$ will result in a larger $f_{\text{ug, outer}}$. Based on the discussion in **Section 2.3**, since $L$ is inversely proportional to $f_{\text{ug, inner}}$ while $C$ is inversely proportional to $f_{\text{ug, outer}}$. For the same $f_{LC}$, a large $C$ and small $L$ can be favorable for system PM since $f_{\text{ug, inner}}$ and $f_{\text{ug, outer}}$ are separated further apart.

Based on the simplified equation of the outer loop's transfer function, the inductor value does not significantly impact the outer loop's unity-gain frequency. Hence, assuming two different inductor values, the outer loop's unity-gain frequencies are assumed to be the same. Figure 2.8 shows the magnitude and phase plots of the outer loop's transfer function with these two different inductor values.

**Bode plot of $G_{outer}(s)$**

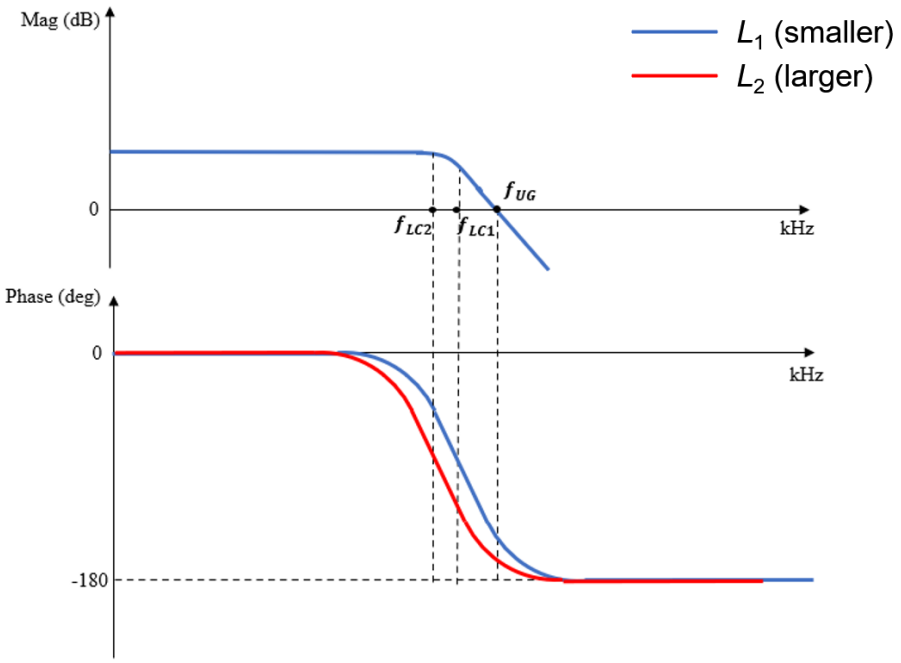



Figure 2.8 Outer loop magnitude & phase plot with different inductor values.

Since

$$G_{\text{loop,outer}}(s) = \frac{C_1(s)G_{\text{PWM}}}{s^2LC + 1 + C_1(s)G_{\text{PWM}}K_{\text{cfb}} \cdot sC \cdot \frac{s}{s + 2\pi f_{\text{HP}}}} = \frac{K_{\text{eq}}}{s^2LC + B \cdot s + 1}$$

It follows that for $L_1 < L_2$ (i.e., $f_{LC1} > f_{LC2}$), the phase plot shifts from the blue curve to the red curve, indicating a reduced PM when the inductor value increases from $L_1$ to $L_2$

## 2.4 Choice of L and C

To achieve the +/- 30% tolerance for the LC filter, four extreme cases with a large inductor and a large capacitor, a large inductor and a small capacitor, a small inductor and a large capacitor, a small inductor a and small capacitor are simulated to verify their unity-gain frequencies and phase margin values.

Based on the discussion in **Sections 2.3 and 2.4**, the cases with large inductor values show smaller PM, and if the nominal inductor value is chosen to be 820 nH, the minimum phase margin value will decrease to below 40 degrees, which is not desired. On the other hand, Since $L$ is inversely proportional inner loop's unity-gain frequency $f_{\text{ug, inner}}$, a smaller $L$ will move $f_{\text{ug, inner}}$ to a higher frequency, and if the nominal inductor value is chosen to be 470 nH, to meet the $f_{\text{PWM}}/\pi$ and PM requirement, the loop gain at audio band will have to decrease to below 70 dB and cannot suppress the output stage's nonlinearity efficiently.

Regarding the capacitor, as mentioned in **Sections 2.3 and 2.4**, a large capacitor reduces the outer loop's unity-gain frequency $f_{\text{ug, outer}}$, which will bring $f_{\text{ug, outer}}$ and $f_{\text{ug, inner}}$ far away, contributing to increasing system PM. However, if the capacitor keeps increasing, a too small $f_{\text{ug, outer}}$ will also result in a reduced PM for outer loop. Besides, larger capacitor can be bulky and more expensive.

To summarize, a small inductor and a large capacitor value are favorable for the system PM as $f_{\text{ug, inner}}$ and $f_{\text{ug, outer}}$ are moving apart. The optimal nominal values for the inductor and capacitor in this structure are determined to be 680 nH and 270 nF, respectively. Compared to the nominal values mentioned in [2], which are 3.3 μH and 1 μF, respectively, the LC filter's bulk and cost have been reduced.

## 2.5 High-pass filter corner frequency

The corner frequency of the HPF should be larger enough to eliminate $L_1(s)$ at the audio band. However, the corner frequency cannot be too high, as the HPF introduces an extra pole and will reduce the phase margin as explained below:

In **Section 2.4**, the outer loop's transfer function has been calculated and simplified as follows:

$$G_{\text{loop,outer}}(s) = \frac{C_1(s)G_{\text{PWM}}}{s^2LC + 1 + C_1(s)G_{\text{PWM}}K_{\text{cfb}} \cdot sC \cdot \frac{s}{s + 2\pi f_{\text{HP}}}} = \frac{K_{\text{eq}}}{s^2LC + B \cdot s + 1}$$

By increasing the corner frequency $f_{HP}$, the value of $B$ decreases, resulting in a shift of the phase plot of the outer loop from the blue curve to the red curve, indicating a reduction in phase margin, as shown in Figure 2.9.

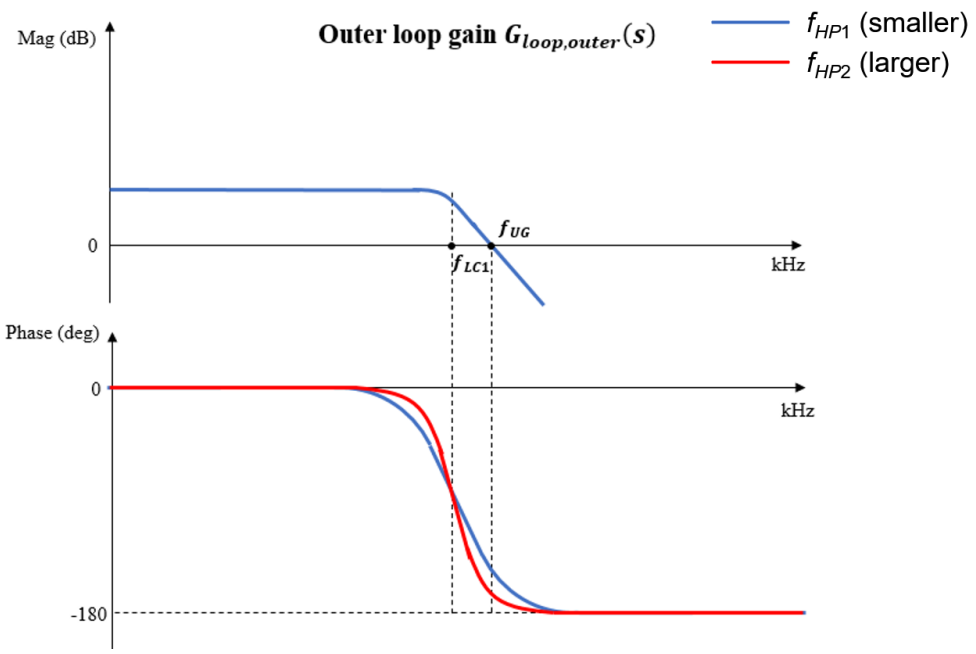



Figure 2.9 Outer loop's gain and phase with different $f_{HP}$ values.

The corner frequency of the HPF has been determined to be 90 kHz based on the phase margin requirement. By implementing the HPF to reduce $V_{NL,C}$ by >13dB, the residual nonlinearity of the capacitor at audio band is similar to that for the inductor and output stage, which has been verified by plotting the Noise Transfer Function (NTF) for output stage + inductor ($NTF_{OS+L}$) and capacitor ($NTF_C$) over PVT, shown in Figure 2.10. The black lines show the Signal Transfer Function (STF) over PVT.

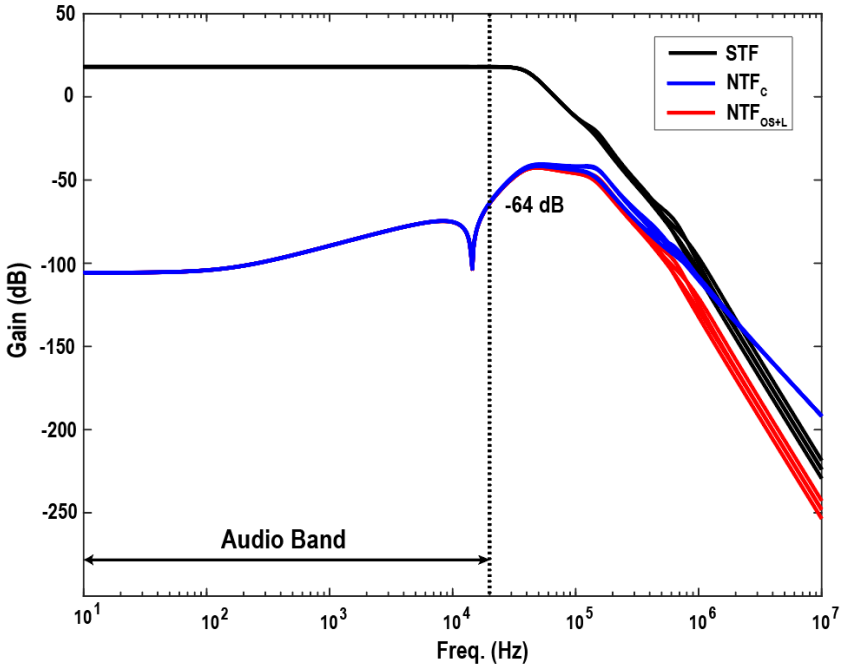



Figure 2.10 NTFs over PVT

## 2.6 Summary

In this architecture-level design, a higher LC cut-off frequency in the feedback-after-LC structure is achieved by employing a current feedback inner loop structure. In [2], it has been discussed that increasing the LC cut-off frequency beyond 106 kHz can lead to a decrease in outer loop gain, which also decreases the LC filter nonlinearity suppression.

With the current feedback path serving as the inner loop, it becomes possible to select smaller inductor and capacitor values, enabling a higher LC cut-off frequency. In this design, the LC cut-off frequency can range from 306 kHz to 531 kHz, still maintaining the +/- 30% tolerance. This implementation allows for a higher LC cut-off frequency, comparable to the values reported in [1], while using the feedback-after-LC structure to suppress the nonlinearity.

Therefore, the minimum volume of the inductor in this work is further reduced compared to the smallest one used in [2] by 7 times, maximally reducing the bulk and cost of the LC filter in the feedback-after-LC structure.

## Reference

[1] H. Zhang et al., “A High-Linearity and Low-EMI Multilevel Class-D Amplifier,” IEEE J. Solid-State Circuits, vol. 56, no. 4, pp. 1176–1185, Apr. 2021, doi: 10.1109/JSSC.2020.3043815.

[2] H. Zhang, M. Berkhout, K. A. A. Makinwa, and Q. Fan, “A −121.5-dB THD Class-D Audio Amplifier With 49-dB LC Filter Nonlinearity Suppression,” IEEE J. Solid-State Circuits, vol. 57, no. 4, pp. 1153–1161, Apr. 2022, doi: 10.1109/JSSC.2021.3125526.

# Chapter 3 Schematic–level Design

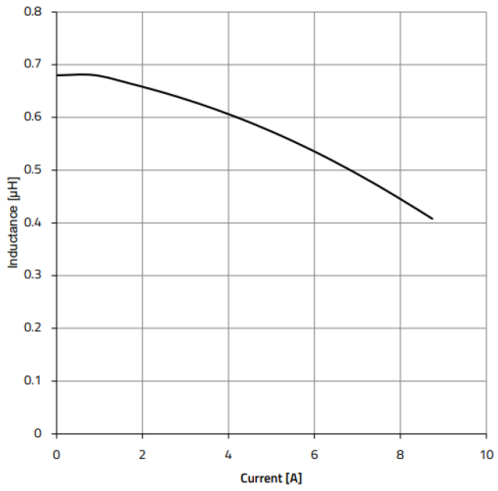
In the schematic-level design, the ideal blocks or Verilog-A models used in the architecture-level design need to be replaced with real circuits. This chapter will concentrate on the implementation of the ideal blocks at the schematic-level.

For example, the ideal OTA used in the architecture-level design will be replaced with a real OTA that incorporates the OTA's nonlinearity such as finite gain, input/output impedance, and frequency response. Similarly, the ideal switches, resistors, capacitors, and other components will be replaced with their real models, accounting for their non-ideal characteristics.

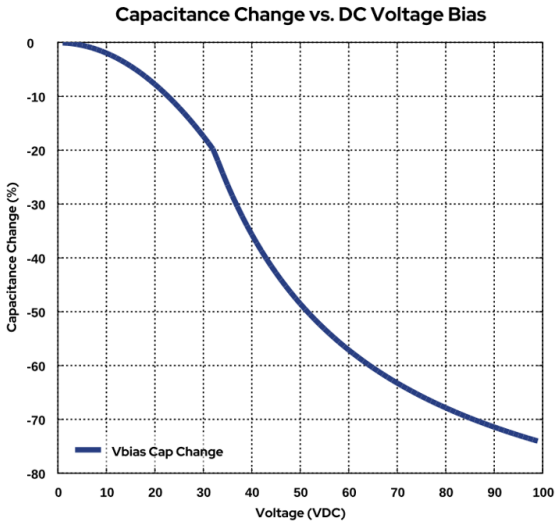
## 3.1 Verilog-A model for the LC filter

The LC filter is placed off-chip. However, its nonlinearity cannot be ignored and should be reflected in the simulation to verify whether the outer loop plays its role in suppressing the nonlinearity of the LC filter. Therefore, the Verilog-A model should be created to represent the nonlinearity of the inductor and capacitor.

The Verilog-A model is created based on the component's datasheet, the *I-A* curve and *C-V* curve for the inductor and capacitor can be used to model their nonlinearity, as shown in Figure 3.1.




*I-A* curve for 680 nH inductor




*C-V* curve for 270 nF capacitor

Figure 3.1 *I-A* curve and *C-V* curve for the inductor and capacitor.

These curves are fitted to polynomials and then implemented in the Verilog-A code to represent the nonlinearity of the inductor and capacitor.

To verify the suppression of LC filter nonlinearity, a set of transient simulations can be performed using both the ideal LC filter and the Verilog-A model LC filter. By comparing the THD results between the ideal LC filter and the Verilog-A model LC filter, whether the nonlinearity has been effectively suppressed can be determined.

## 3.2 Current feedback loop implementation

The proposed circuit diagram for the current feedback loop is shown in Figure 3.2, which is used to measure the current flow through the LC filter by implementing a pair of sense resistors placed after the inductor to avoid high-frequency interference from the switching nodes. These sense resistors are designed to have a resistance value of ~ 30 mΩ. The resistance value is chosen to be a small value to avoid a significant decrease in the entire system's efficiency.

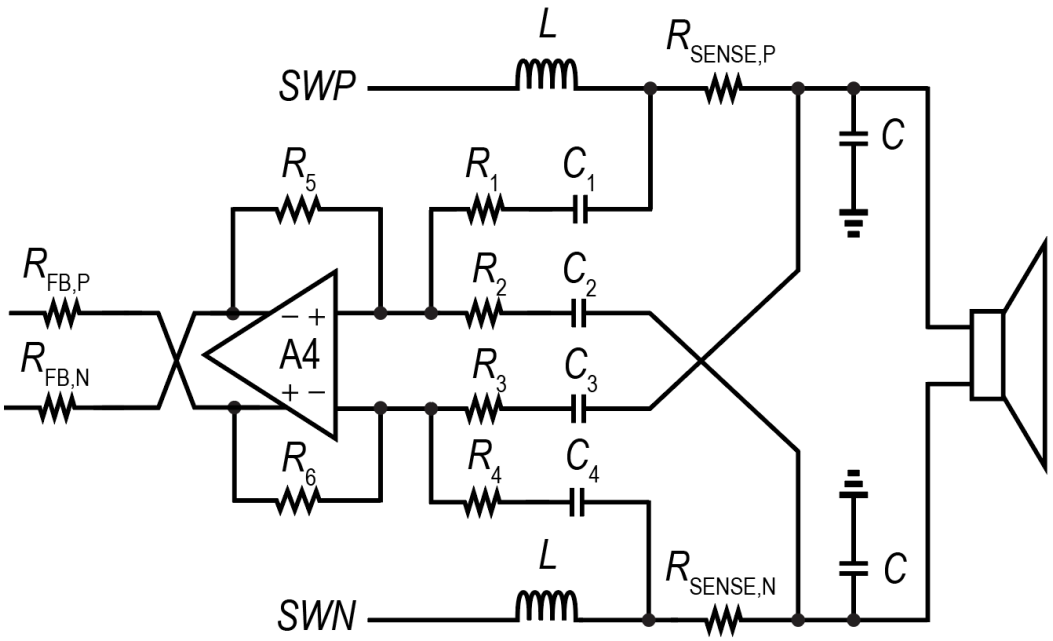



Figure 3.2 Current feedback loop implementation

Within the circuit, $R_1$ is in series with $C_1$, forming the HPF. At low frequency, the impedance of the capacitor is high, resulting in the elimination of the current feedback loop gain $L_1(s)$. However, at high frequency, the impedance of the capacitor can be disregarded, allowing the current feedback loop to play its role.

The gain of the current feedback loop, $K_{\mathrm{cfb}}$, can be adjusted by changing the value of the feedback resistor pair, $R_{\mathrm{FB,P}}$ and $R_{\mathrm{FB,N}}$. This allows for flexible modification of the loop's gain according to specific requirements. Additionally, $R_{\mathrm{FB,P}}$ and $R_{\mathrm{FB,N}}$ serves to convert the voltage at the OTA's output to a corresponding current.

Considering the high frequency signal in the current feedback loop, the bandwidth of poly resistors $R_1$ to $R_4$ should be considered. By choosing $R_1$ to $R_4$ as $98.25\ \mathrm{k\Omega}$, a bandwidth of 9 MHz, which should be much larger than $f_{\mathrm{PWM}} = 4.2$ MHz, is achieved. The cut-off frequency of the HPF, $f_{\mathrm{HP}}$, is set to 90 kHz. By substituting the values of $R$ and $f_{\mathrm{HP}}$ into the formula, the capacitor values are determined. The values of $C_1$ to $C_4$ can be calculated as $1/(2\pi R_{1/4} \cdot f_{\mathrm{HP}})$ = 18 pF, which is not too big.

At high frequency, the capacitor can be treated as a short circuit. Therefore, the output current of the current feedback loop is given by:

$$I_{\mathrm{OUT}} = \frac{\Delta V}{R_1} \cdot \frac{R_5}{R_{\mathrm{FB,P/N}}} = \frac{I_{\mathrm{L}} \cdot R_{\mathrm{SENSE,P/N}}}{R_1} \cdot \frac{R_5}{R_{\mathrm{FB,P/N}}}$$

The sense resistor pair, $R_{\mathrm{SENSE,P/N}}$, is placed on a separate chip and implemented as a diffusion resistor. $R_{\mathrm{FB,P/N}}$ are also chosen as diffusion resistors to ensures that $I_{\mathrm{OUT}}$ remains stable across process corners.

To achieve better matching performance, $R_5$ is implemented as poly resistor and is set to have the same value as $R_1$. The value of the feedback resistor, $R_{\mathrm{FB,P/N}}$, can be calculated based on the desired transfer function. Since the current is copied with a gain factor of $K_{\mathrm{cfb}}/90\ \mathrm{k\Omega}$, $I_{\mathrm{OUT}}$ should have the following relation with $I_{\mathrm{L}}$:

$$I_{\mathrm{OUT}} = \frac{I_{\mathrm{L}} \cdot R_{\mathrm{SENSE,P/N}}}{R_1} \cdot \frac{R_5}{R_{\mathrm{FB,P/N}}} = I_{\mathrm{L}} \cdot \frac{K_{\mathrm{cfb}}}{90\ \mathrm{k\Omega}}$$

Therefore, $R_{\mathrm{FB.N}}$ can be calculated as:

$$R_{FB,N} = \frac{90\ \mathrm{k\Omega} \cdot R_{\mathrm{SENSE,P/N}}}{K_{\mathrm{cfb}}}$$

In this design, the value of $R_{\mathrm{SENSE,P/N}}$ is ~ 30 mΩ, and $K_{\mathrm{cfb}}$ is 0.25. Substituting these values into the equation, $R_{\mathrm{FB,P/N}}$ is determined to be 11 kΩ.

OTA4 is a fully differential amplifier, which can minimize the high-voltage CM disturbance at the virtual ground of the amplifier.

## 3.3 Sense resistors

To minimize the impact of parasitic inductance on the sense resistor, it is necessary to fabricate them on a separate chip rather than using discrete sense resistors. The latter typically have parasitic inductance greater than 5 nH, which can significantly alter the impedance characteristics of the sense resistor at high frequency. This can disrupt the operation of the current feedback loop.

The sense resistor will be connected in a Kelvin configuration, using 4 Kelvin pins and 4 normal pins. The Kelvin pins are responsible for sensing the current and connecting to the current feedback loop. The normal pins are used to connect the sense resistor pair between the inductor and output. The implementation of the Kelvin connection ensures accurate current sensing by minimizing the influence of parasitic inductance.

One drawback of implementing the sense resistor pair in the current feedback loop is a potential decrease in power efficiency. The sense resistors introduce additional resistance which can result in power losses and reduced efficiency.

In the case of a Class-D amplifier with an 8 Ω load, the power efficiency drop can be calculated by comparing the sense resistor resistance to the load resistance. If the sense resistor pair has a total resistance of 2 × 30 mΩ, and the bonding wire's resistance is 5 mΩ each side. Since the load resistance is 8 Ω, the power efficiency drop can be estimated as:

$$\frac{2 \times 35\ \text{m}\Omega}{8\ \Omega} = 0.875\%$$

This means that approximately 0.875% of the power is dissipated across the sense resistor pair, leading to a decrease in overall power efficiency.

## 3.4 OTA design

In the schematic-level implementation, OTAs are no longer ideal with infinite gain and unity-gain bandwidth. Real-world OTAs have limited gain and bandwidth, which can affect the overall performance of the system.

To ensure that the OTAs do not significantly impact the system's performance, it is necessary to determine the minimum required values for the gain and unity-gain bandwidth of the OTAs to ensure that they would not affect the overall system's performance.

### 3.4.1 Design specifications

Since the OTAs used in the current feedback loop (OTA4) and third OTA in the loop filter (OTA3) need to handle signal with higher frequency in the current feedback loop $L_1(s)$, their unity-gain frequencies should be designed higher. To establish the minimum design requirements for the OTA3 and OTA4, an "ideal" OTA with a DC gain of 120 dB and a unity-gain bandwidth of 5 GHz is initially employed. This "ideal" OTA serves as a reference for the THD. The schematic of the ideal OTA, as shown in Figure 3.3, consists of a DC gain represented by $A_0$ and a RC low-pass filter to represent the finite bandwidth of the OTA.

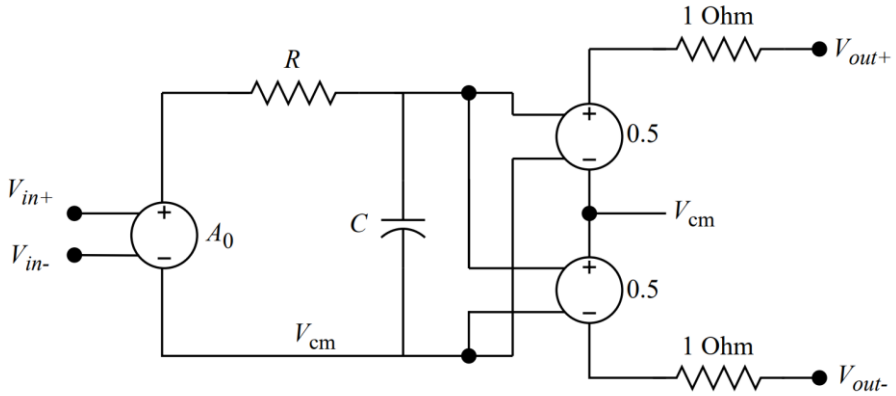



Figure 3.3 Ideal OTA structure.

To determine the design target for the OTA, the DC gain $A_0$ and unity-gain bandwidth values are gradually decreased. The THD is then measured for each set of DC gain and unity-gain bandwidth values, and the point at which the THD decreases by 1 dB is identified. This specific point, where the THD drops by 1 dB, serves as the minimum design specifications for the OTA.

Table 3.1 presents the THD results corresponding to different values of DC gain and unity-gain bandwidth for the OTA.

Table 3.1: THD results with different DC gain and unity-gain bandwidth values' OTAs.

| Specs | THD (dB) |
|---|---|
| DC gain = 120 dB, $f_{ug}$ = 5 GHz | 112.0 |
| DC gain = 70 dB, $f_{ug}$ = 1 GHz | 110.7 |
| DC gain = 70 dB, $f_{ug}$ = 2 GHz | 111.4 |
| DC gain = 70 dB, $f_{ug}$ = 3 GHz | 111.6 |

Based on the THD results and the criterion of a 1 dB decrease in THD, the design specifications for the OTAs are established as a DC gain of 70 dB and a unity-gain bandwidth of 2 GHz. These specifications ensure that the OTAs meet the required performance criteria.

### 3.4.2 Design procedure

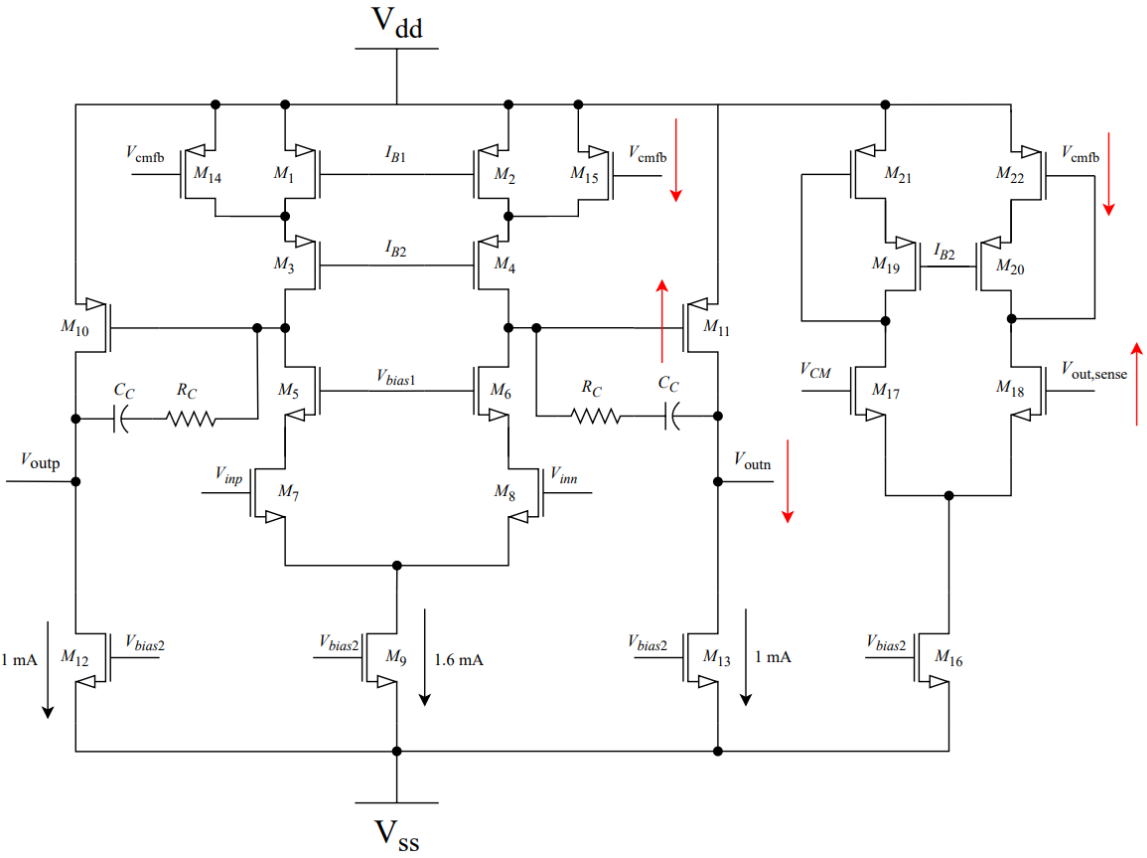



Figure 3.4 OTA structure.

For OTA3 and OTA4, they are designed as the two-stage miller-compensated amplifier structure with cascode in the first stage, as shown in Figure 3.4. Implementing a two-stage amplifier offers wider output swing capabilities compared to the folded cascode OTA. The transistor lengths are kept small as 180 nm to minimize parasitic capacitance. As a result, the cascode structure is employed in the first stage to maintain sufficient DC gain. In Figure 3.4, $C_c = 500$ fF and $R_c = 1.4$ kΩ.

### 3.4.3 Extra phase margin

The addition of an extra capacitor in parallel with the feedback resistor is a technique known as pole-zero compensation. It is employed in OTA3 and OTA 4 to compensate for the PM loss due to the extra pole. The input transistor's parasitic capacitance, along with the input resistance, forms an additional pole in the system transfer function, leading to a PM loss, which can destabilize the system.

Figure 3.5 shows the pole-zero compensation implemented in OTA4, which has an open-loop gain of *A*. By introducing an additional capacitor $C_{\mathrm{zero1}}$ in parallel with the feedback resistor $R_5$, an extra zero is created in the open loop gain $A\beta$ of the OTA4. This zero is placed to compensate for the PM loss introduced by the pole formed by the input parasitic capacitance. The goal is to achieve a compensation effect where the phase contributions from the pole and zero cancel each other, resulting in improved stability of $A\beta$. However, in the closed-loop transfer function, $C_{\mathrm{zero1/2}}$ and $R_{5/6}$ forms an LPF, which gives a pole and reduces the OTA's bandwidth. Therefore, it is necessary to add capacitors $C_{1\mathrm{P}}$ to $C_{4\mathrm{P}}$ in parallel with $R_1$ to $R_4$ to introduce an extra zero to the closed-loop transfer function and maintain the bandwidth of the OTA.

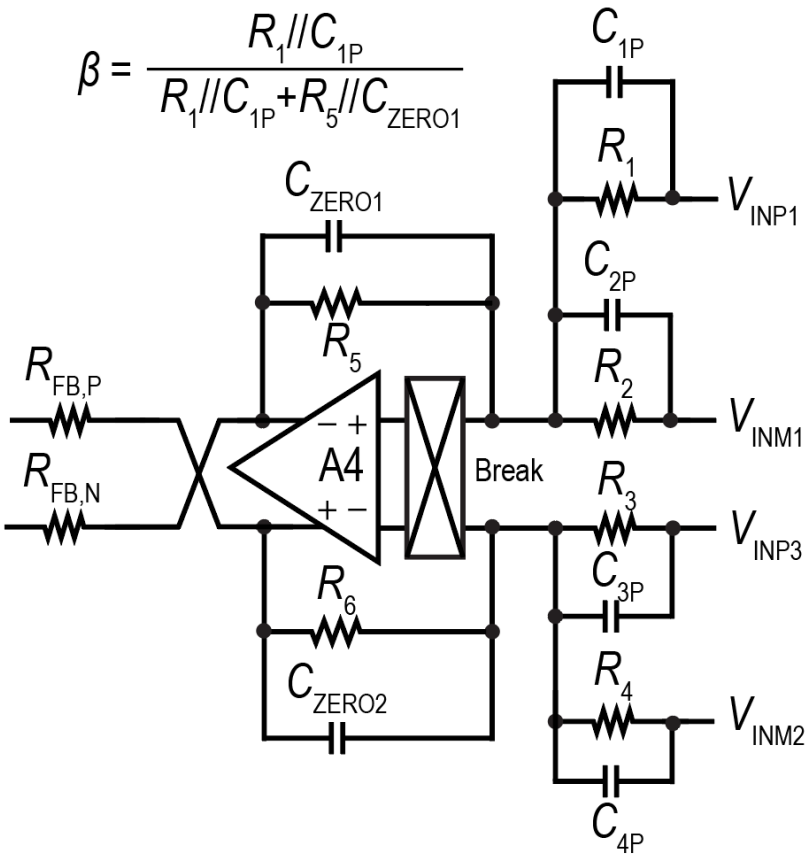



Figure 3.5 Pole-zero compensation.

From the time domain, the delay constant $\tau$ is determined by the parallel capacitor $C_{\text{zero1}}$ and feedback resistor $R_5$, and it is given by $\tau = R_5 C_{\text{zero1}}$. The values of capacitors $C_{1\text{P}}$ to $C_{4\text{P}}$ are chosen such that they satisfy the following relation to keep the delay constant the same:

$$\tau = R_5 C_{zero1} = R_1 C_{1\text{P}} = R_2 C_{2\text{P}} = R_3 C_{3\text{P}} = R_4 C_{4\text{P}}$$

Since $R_5 = R_1 = R_2 = R_3 = R_4$, $C_{zero1}$ should be the same with $C_{1\text{P}}$ to $C_{4\text{P}}$. To minimize the delay constant, $C_{\text{zero1}} = C_{1\text{P}} = C_{2\text{P}} = C_{3\text{P}} = C_{4\text{P}} = 100$ fF.

### 3.4.4 Performance verification

Two Spectre STB simulations, one with a common-mode (CM) probe and another with a differential-mode (DM) probe, are conducted to verify the OTAs' performance, whose results are presented below.

**a. The third OTA in the loop filter (OTA3)**

- Common-mode loop gain and phase

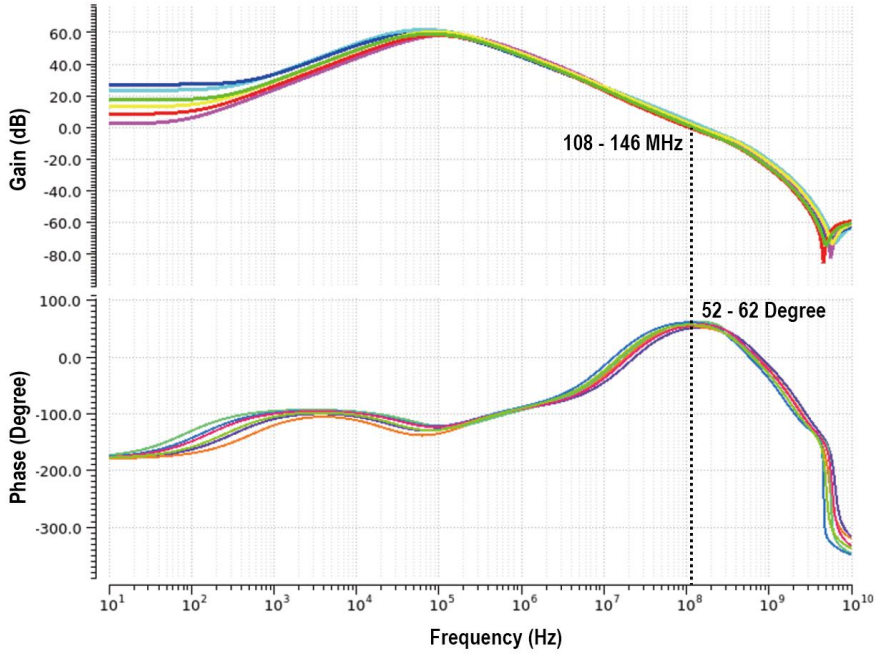



Figure 3.6 Common-mode loop gain and phase for OTA3

In Figure 3.6, the common-mode loop gain and phase plots for the first OTA in the loop filter are shown under different process corners. From Figure 3.7, the lowest phase margin for OTA3's CMFB occurs at the FF corner and a temperature of 25 °C, where it is measured to be 52 degrees.

- Differential-mode loop gain and phase

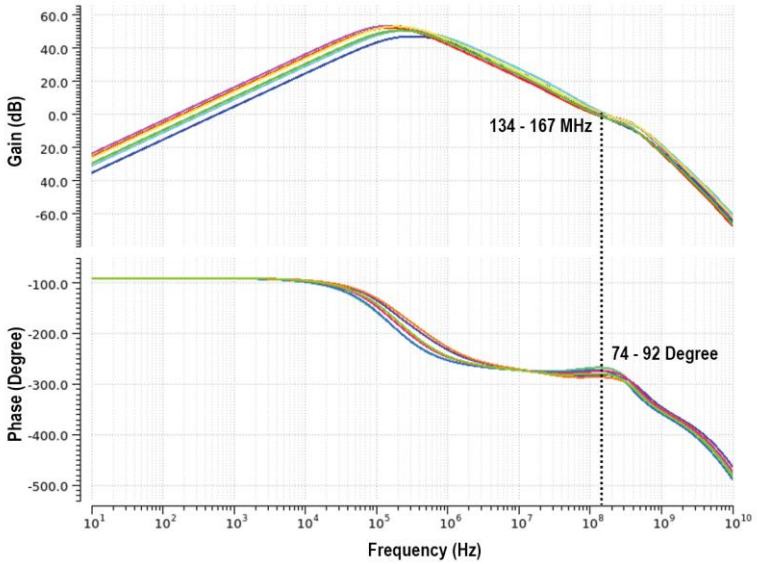



Figure 3.7 Differential-mode loop gain and phase for OTA3

From Figure 3.7, the loop gain at around 4 MHz is above 30 dB, which is similar to the result measured with the "ideal" OTA model with 70 dB DC gain and 2 GHz $f_{\mathrm{UG}}$, showing that it can meet the requirements. The lowest phase margin for OTA3 occurs at the FF corner and a temperature of 125 °C, where it is measured to be 74 degrees.

**b. Current feedback loop's OTA (OTA4)**

- Common-mode loop gain and phase

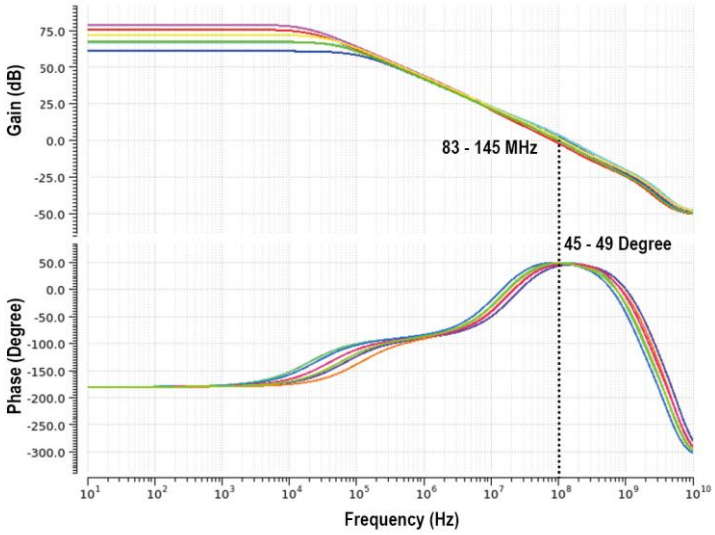



Figure 3.8 Common-mode loop gain and phase for OTA4

From Figure 3.8, the lowest phase margin for OTA4's CMFB occurs at the FF corner and a temperature of 25 °C, where it is measured to be 45 degrees.

- Differential-mode loop gain and phase

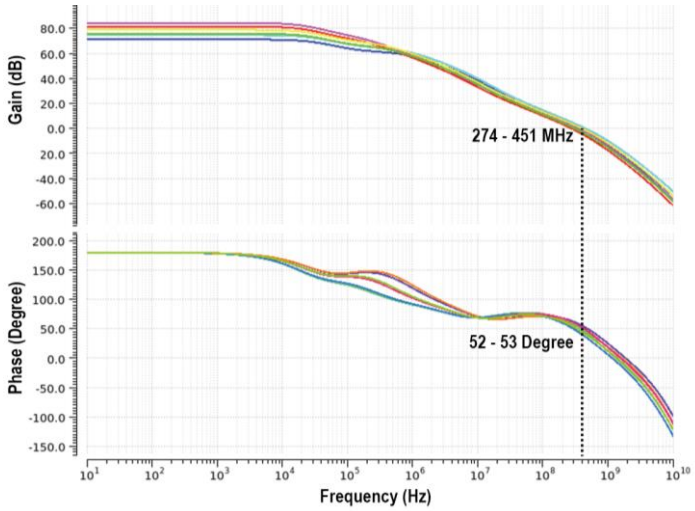



Figure 3.9 Differential-mode loop gain and phase for OTA4

From Figure 3.9, the loop gain at around 4 MHz is above 42 dB, which is similar to the result measured with the "ideal" OTA model with 70 dB DC gain and 2 GHz $f_{\mathrm{UG}}$, showing that it can meet the requirements. The lowest phase margin for OTA4 occurs is measured to be 52 degrees.

## 3.5 Loop filer implementation

To achieve sufficient gain for suppressing the nonlinearity of the output stage and the LC filter, a third-order loop filter with high loop gain is implemented. As mentioned in **Chapter 2**, the third-order loop filter consists of a 2nd order resonator and a PI compensator. Circuit implementation of the loop filter is shown in Figure 3.10.

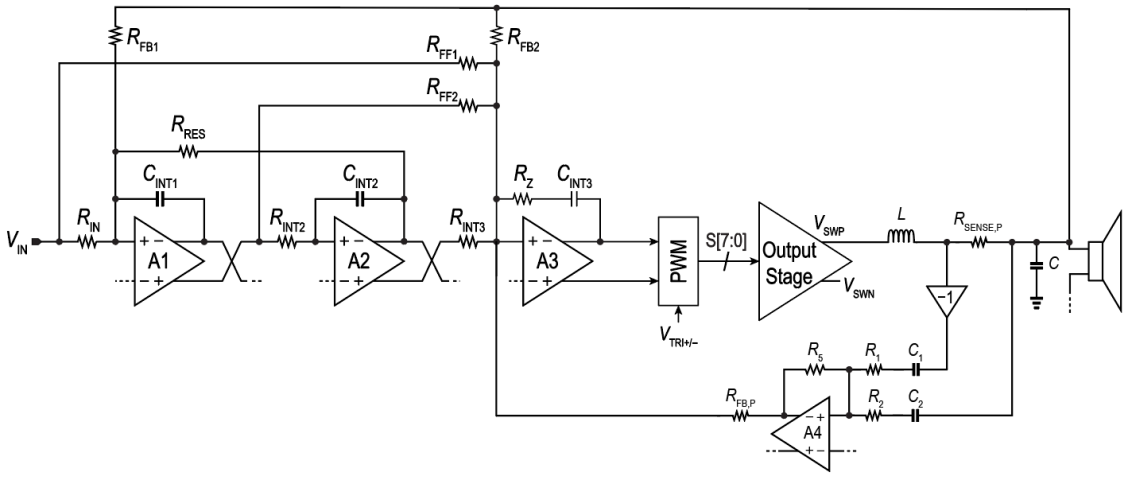



Figure 3.10 Circuit implementation of the loop filter

The circuit diagram for the second-order resonator is shown in Figure 3.11. $R_{\text{poles}}$ is implemented to introduce complex poles in the audio band. By controlling $R_{\text{poles}}$ value, the complex poles will shift from DC to an optimal location in the audio band to boost the in-band loop gain. In the nominal case, the complex poles' optimal frequency is set at 14 kHz.

To compensate for the phase shift caused by the complex poles resulting from $R_{\text{poles}}$, two additional resistors, $R_{\text{zero1}}$ and $R_{\text{zero2}}$, are incorporated to provide complex zeros. The resonator's output is in the form of a current, which is injected into the PI compensator.

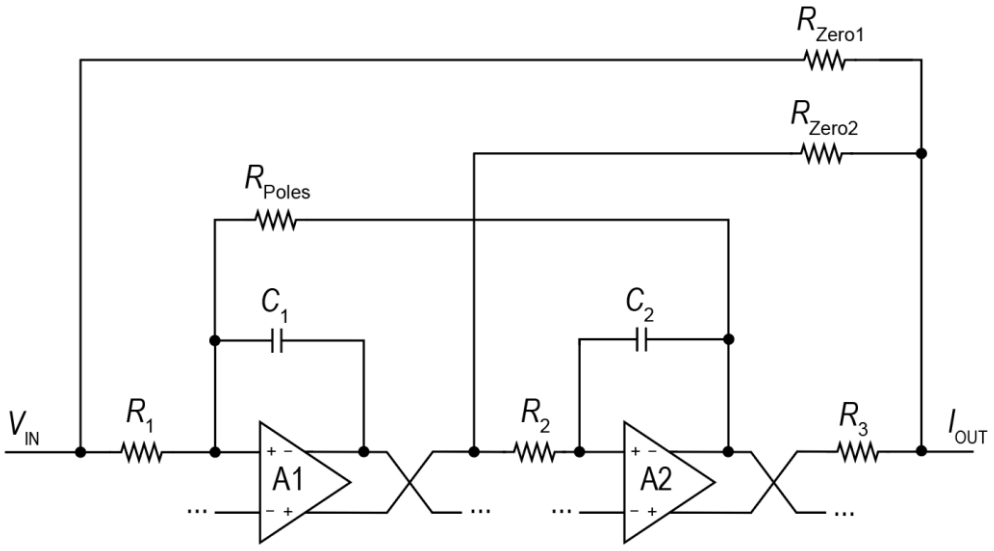



Figure 3.11 Circuit implementation for the resonator.

In Figure 3.12, the circuit diagram for the PI compensator is presented. The current input from the resonator is converted to a voltage output by passing through resistor $R_4$ and capacitor $C_3$. Since the input current also includes the current from the current feedback loop $L_1(s)$, which includes high-frequency signal because of the HPF in $L_1(s)$, it is necessary to design an OTA with a high unity-gain bandwidth of 2 GHz in the PI compensator, which has been designed in **Section 3.4**.

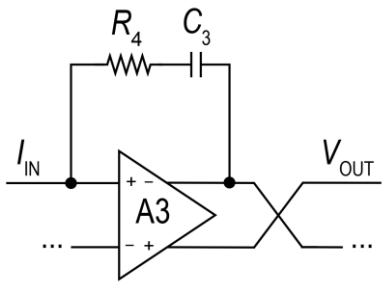



Figure 3.12 Circuit diagram for PI compensator.

The resonator, in combination with the PI compensator, forms the third-order loop filter, boosting the in-band loop gain, which is used for nonlinearity suppression of the output stage and LC filter.

## 3.6 Capacitor trimming

In the case of the MOM capacitor used in the HPF, conventional two-side trimming methods involving transmission gates cannot be employed. This is because one side of the mom capacitor is connected to the switching node, which experiences a high voltage ranging from 0 to 14.4 V.

Due to the presence of this high CM voltage at right side of the MOM capacitor, implementing transmission gates in high CM voltage side is not feasible. To address this challenge, a straightforward solution is adopted. The side of the trimming capacitor with a high CM voltage of 7.2 V is directly connected to the capacitor. The trimming can still be realized with left-side transmission gates with a low CM voltage of 0.9 V, as shown in Figure 3.13, and can therefore prevent the overload voltage in the transmission gate.

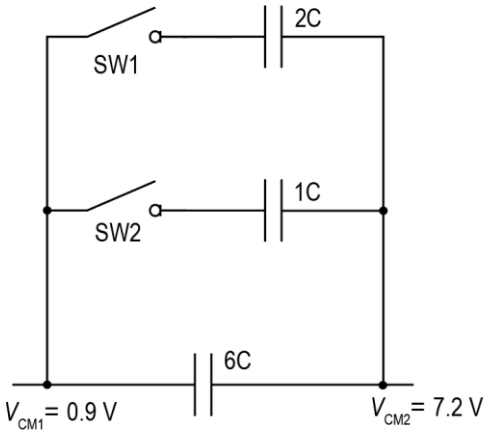



Figure 3.13 Trimming for the MOM capacitor in the HPF.

The implementation of the SW1 and SW2 in Figure 3.13 is shown in Figure 3.14. The switch consists of three transistors that are controlled by $V_{\mathrm{trimb}}$ and $V_{\mathrm{trim}}$.

When the $V_{\mathrm{trim}}$ signal is high, $M_2$ and $M_3$ are turned on, and the trimming capacitor is connected to the baseline capacitor, which increases the overall capacitance value. When the $V_{\mathrm{trim}}$ signal is low, $M_2$ and $M_3$ are turned off, and the trimming capacitor is disconnected. However, M1 is turned on since $V_{\mathrm{trimb}}$ is high, and the trimming capacitor is therefore connected to the ground.

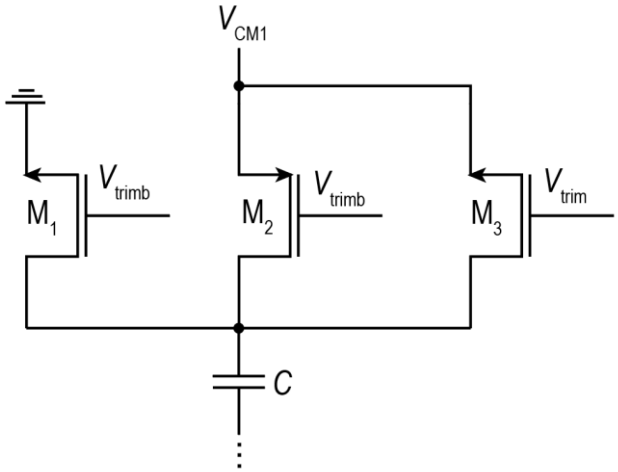



Figure 3.14 implementation of SW1 and SW2

By implementing this approach, the trimming of the MOM capacitor can still be achieved by controlling only the low CM voltage side, enabling adjustments to the capacitor value to maintain a relatively constant *RC* product across process corners.

## Reference

[1] R. Gupta and S. Jain, “A Review Paper on Frequency Compensation of Transconductance Operational Amplifier (OTA),” vol. 4, no. 4, 2013.

# Chapter 4 Simulation Results

This chapter presents the post-layout simulation results. The verification process will assess the performance of the system by analyzing various parameters including loop gain, phase margin, THD, PSRR, SNR, and overdrive performance.

## 4.1 Chip layout

The chip has the die size of 3 mm × 2.28 mm. The chip is fabricated using a 180-nm BCD process. The output stage of the CDA is powered by a 14.4 V supply, while the loop filter and PWM components will operate with a 1.8 V supply. The layout floorplan for the prototype chip is shown in Figure 5.1.

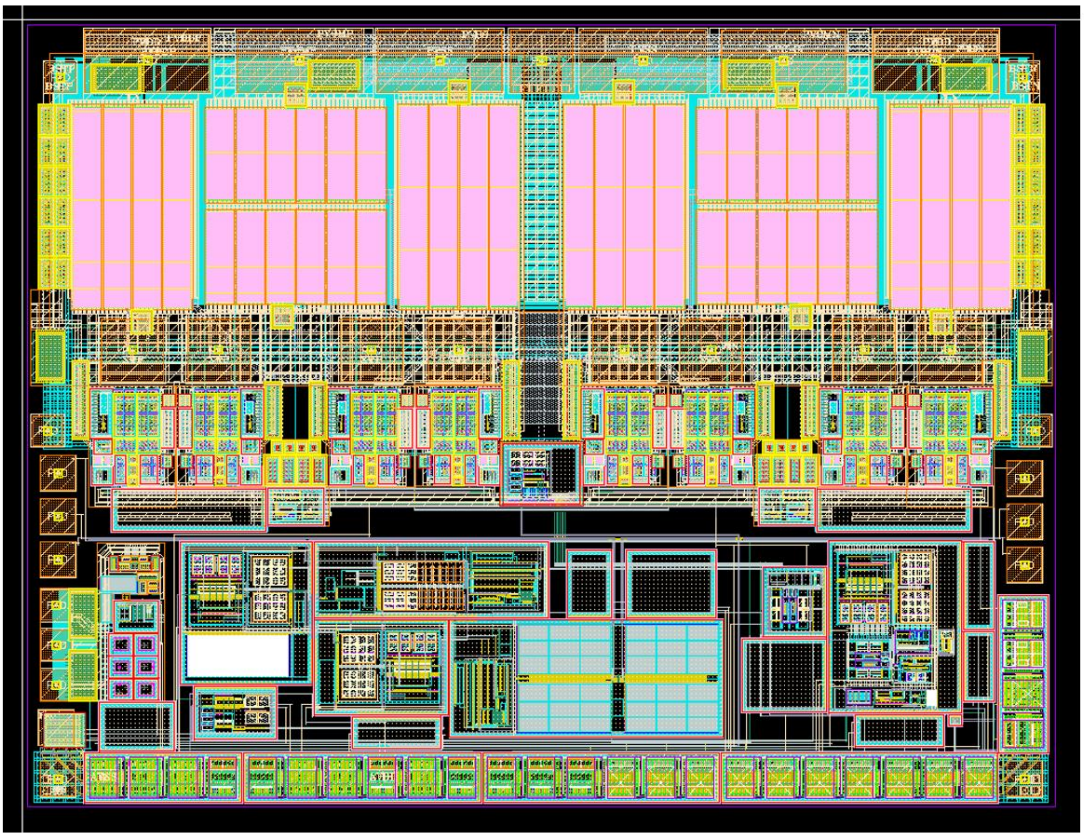


Figure 4.1 Layout for the chip

## 4.2 Stability test of the inner and outer loops

To verify the stability of the system, it is important to analyze the loop gain and phase of both the inner and outer loops, as discussed in **Sections 2.3 and 2.4**. By cutting off the loop at specific points and examining the gain and phase response, the stability performance of the system can be assessed.

Since the design maintains a +/- 30% tolerance for the LC filter, it is necessary to perform stability tests at four extreme cases for the LC filter. These four extreme cases represent the maximum and minimum values of the LC filter's component values to ensure stability across the entire tolerance range.

### a. Outer loop's gain and phase

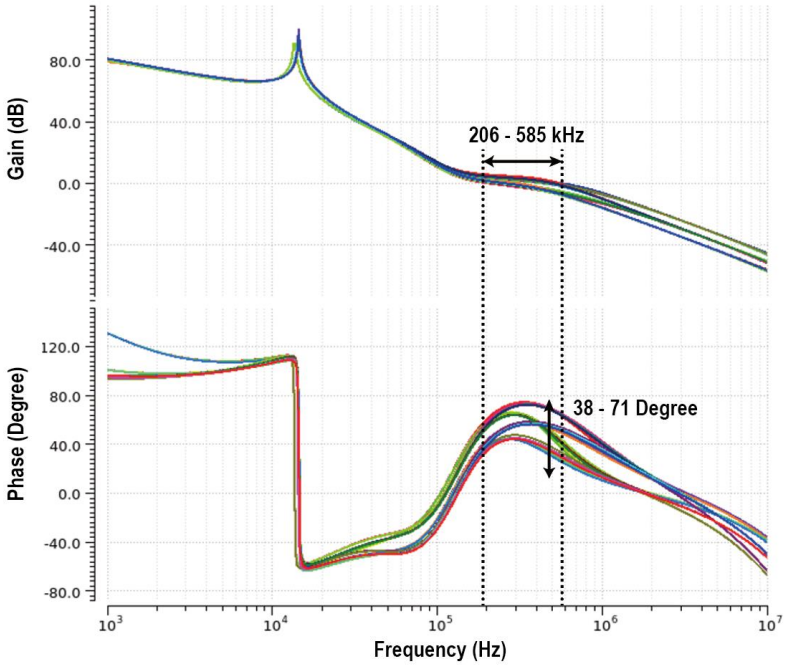



Figure 4.2 Outer loop's gain and phase

Figure 4.2 displays the gain and phase plots for the outer loop under four extreme cases for the LC filter's component values, considering process corners. Among these cases, the minimum phase margin is observed when the inductor value is increased by 1.3x and the capacitor value is decreased by 0.7x. In this situation, at the FF corner and a temperature of 125 °C, the minimum phase margin is measured to be 38 degrees. For the outer loop cases, the maximum unity-gain frequency among all situations is much smaller than $f_{\mathrm{PWM}}/\pi$.

The unity-gain frequencies and PM values of the outer loop with different process corners, temperatures, and LC variations are shown in Table 4.1.

Table 4.1 The unity-gain frequencies and phase margin values of the outer loop

| Conditions | | TT @25℃ | TT @125℃ | SS @25℃ | SS @125℃ | FF @25℃ | FF @125℃ |
|---|---|---|---|---|---|---|---|
| **Small L** | $f_{ug}$ (kHz) | 484.7 | 498.7 | 437.2 | 451 | 572.5 | 585.1 |
| **Small C** | PM (°) | 68 | 67 | 71 | 70 | 63 | 61 |
| **Large L** | $f_{ug}$ (kHz) | 504.3 | 512.5 | 471.7 | 481.3 | 552.5 | 557.5 |
| **Small C** | PM (°) | 47 | 45 | 53 | 51 | 40 | 38 |
| **Small L** | $f_{ug}$ (kHz) | 231.6 | 238.2 | 206 | 211.5 | 287.2 | 295 |
| **Large C** | PM (°) | 47 | 48 | 44 | 44 | 55 | 55 |
| **Large L** | $f_{ug}$ (kHz) | 255.3 | 263.2 | 224.8 | 232 | 312.8 | 320.1 |
| **Large C** | PM (°) | 43 | 43 | 43 | 43 | 44 | 42 |

## b. Inner loop's gain and phase

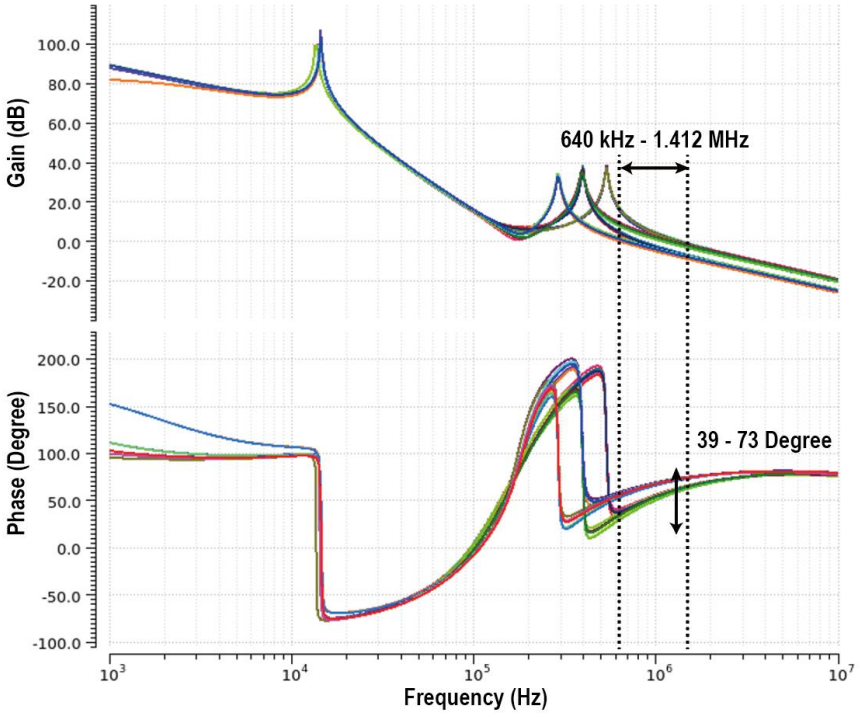



Figure 4.3 Inner loop's gain and phase

Figure 4.3 displays the gain and phase plots for the inner loop under four extreme cases for the LC filter's component values, considering process corners. Among these cases, the minimum phase margin is observed when the inductor value is increased by 1.3x and the capacitor value is decreased by 0.7x. In this situation, at the FF corner and a temperature of 125 °C, the minimum phase margin is measured to be 39 degrees.

The unity-gain frequencies and PM values of the inner loop with different process corners, temperatures, and LC variations are shown in Table 4.2.

Table 4.2 The unity-gain frequencies and phase margin values of the inner loop

| Conditions | | TT @25℃ | TT @125℃ | SS @25℃ | SS @125℃ | FF @25℃ | FF @125℃ |
|---|---|---|---|---|---|---|---|
| **Small L Small C** | $f_{ug}$ (MHz) | 1.355 | 1.327 | 1.412 | 1.381 | 1.257 | 1.227 |
| | PM (°) | 63 | 62 | 65 | 64 | 59 | 57 |
| **Large L Small C** | $f_{ug}$ (kHz) | 827.9 | 814.2 | 855 | 839.5 | 785.8 | 771.6 |
| | PM (°) | 47 | 46 | 50 | 49 | 41 | 39 |
| **Small L Large C** | $f_{ug}$ (MHz) | 1.249 | 1.22 | 1.318 | 1.286 | 1.13 | 1.098 |
| | PM (°) | 72 | 72 | 73 | 73 | 69 | 68 |
| **Large L Large C** | $f_{ug}$ (kHz) | 716.5 | 701.2 | 753.4 | 738.2 | 656.4 | 640.1 |
| | PM (°) | 60 | 59 | 62 | 61 | 55 | 53 |

Based on the simulation results, the maximum unity-gain frequency of the inner loop is found to be 1.412 MHz, occurring at the SS corner at a temperature of 25 °C. This maximum unity-gain frequency is achieved when both the inductor and the capacitor values are reduced by 0.7x. Considering that the designed PWM frequency ($f_{PWM}$) is 4.42 MHz, the maximum inner loop unity-gain frequency of 1.412 MHz is still within the system requirements.

## 4.3 Distortion

To measure the distortion, a series of simulations have been performed to calculate the THD values under different LC filter configurations. The input signal used in these simulations has 0.85 full-scale amplitude and 6 kHz frequency, and the load resistance is 8 Ω. The simulation results are shown in Tables 4.3 to 4.5.

### a. Nominal LC filter

Table 4.3 THD results with nominal LC filter.

| THD (dB) | TT | SS | FF |
|---|---|---|---|
| **25°C** | 111.8 | 109.3 | 112 |
| **125°C** | 116.8 | 111.2 | 120.3 |

### b. LC filter with smaller inductor and smaller capacitor

Table 4.4 THD results with smaller LC filter.

| THD (dB) | TT | SS | FF |
|---|---|---|---|
| **25°C** | 106 | 104 | 105.4 |
| **125°C** | 109.9 | 107.2 | 108.9 |

### c. LC filter with larger inductor and larger capacitor

Table 4.5 THD results with larger LC filter.

| THD (dB) | TT | SS | FF |
|---|---|---|---|
| **25°C** | 112.8 | 109.4 | 114.5 |
| **125°C** | 113.6 | 111.4 | 117.2 |

### d. Spectrum

Figure 4.4 is the spectrum plot for calculating the THD. Since the input signal has a 6 kHz frequency, the dominate distortion occurs at 18 kHz.

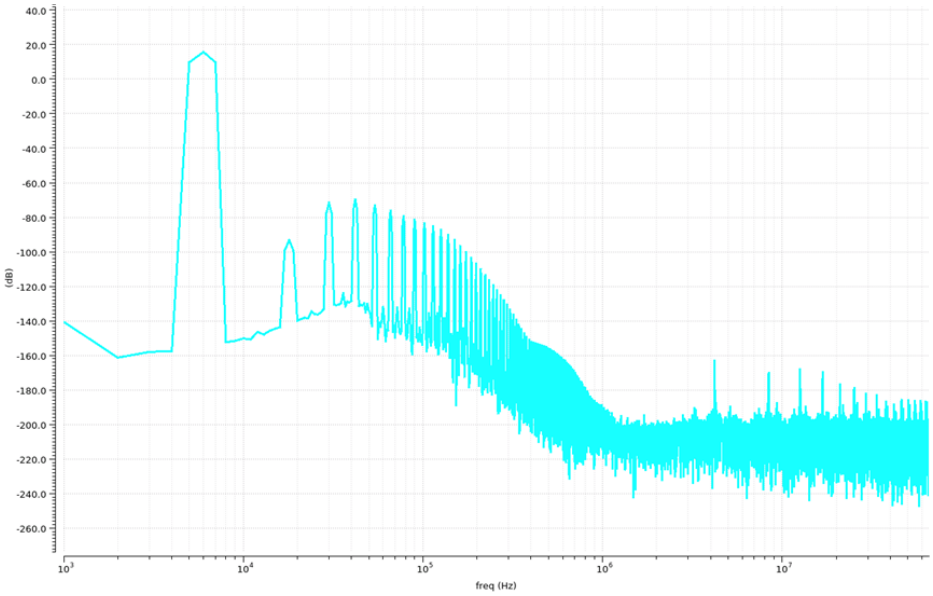



Figure 4.4 Spectrum for calculating THD.

## 4.4 PSRR

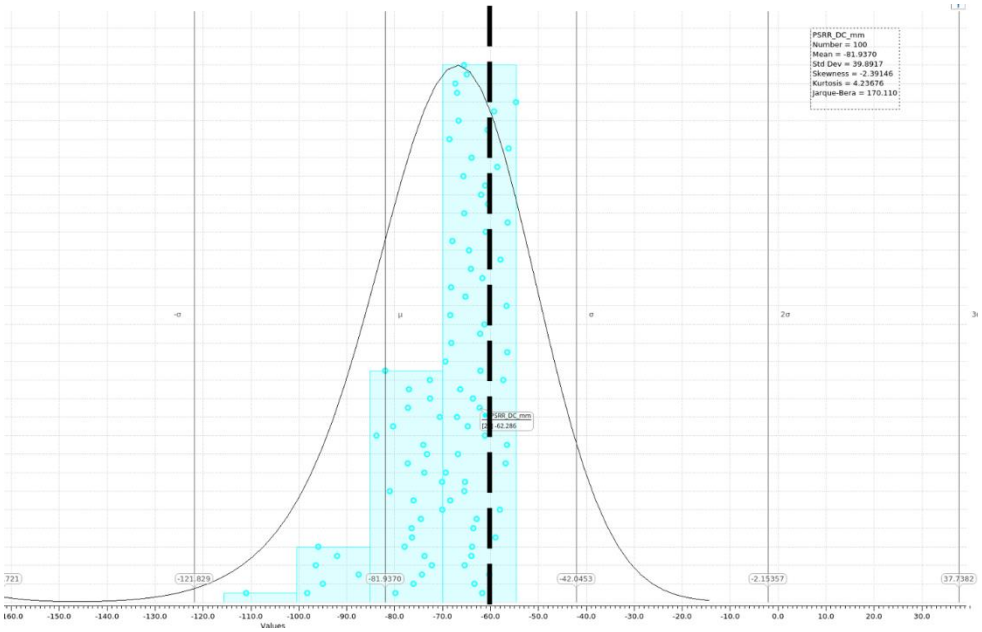



Figure 4.5 Power-Supply Rejection Ratio

Figure 4.5 presents the simulation results for the Power-Supply Rejection Ratio (PSRR) of the system. To account for the mismatch between resistors and capacitors, 100 Monte Carlo simulations have been performed. The results show that in 88% cases, the PSRR are above 60 dB at 20 Hz. As discussed in [1], the PSRR is mainly determined by the mismatch between the input resistor pair $R_{\mathrm{IN}}$. the PSRR limit due to $R_{\mathrm{IN}}$ is given by:

$$\mathrm{PSRR}_{\Delta R_{\mathrm{IN}}} = \frac{R_{\mathrm{IN}}}{\Delta R_{\mathrm{IN}}} \cdot \frac{2A+2}{A}$$

Where A represents the closed-loop gain of CDAs, which is much larger than 1. To reduce the $R_{\mathrm{IN}}$'s limitation to the PSRR, in layout, $R_{\mathrm{IN}}$ pair is implemented as 8 resistors in parallel, which has a larger size to reduce its mismatch and improve the PSRR.

## 4.5 Noise

Based on the Spectre noise simulation, the A-weighted integrated output noise is 36.9697 μV. Hence, the Signal-to-Noise Ratio (SNR) is:

$$\mathrm{SNR} = 20\log\frac{14.4\ \mathrm{V}/\sqrt{2}}{36.9697\ \mu\mathrm{V}} = 108.8\ \mathrm{dB}$$

## 4.6 Clipping Recovery

Testing the stability of the system with an overdrive input signal is an important step to ensure that the system can handle high-amplitude signals without causing oscillations or instability. By using an input signal with 1.2 times the full-scale value, the system can be pushed to the overdrive state to observe any potential issues. The simulation results are shown in Figure 4.6, which proves that the system can remain stable with a 1.2 FS overdrive input signal.

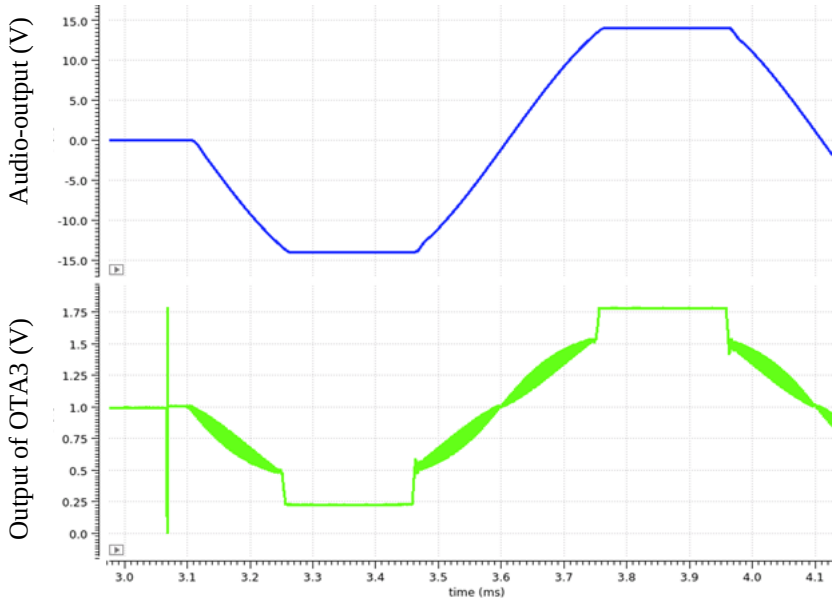



Figure 4.6 Overdrive test.

## Reference

[1] H. Zhang, N. N. M. Rozsa, M. Berkhout, and Q. Fan, “A Chopper Class-D Amplifier for PSRR Improvement Over the Entire Audio Band,” IEEE J. Solid-State Circuits, vol. 57, no. 7, pp. 2035–2044, Jul. 2022, doi: 10.1109/JSSC.2022.3161136.

# Chapter 5 Conclusion

As an extension of [1], this project has put forward a different inner loop approach using the current feedback to stabilize the system. The aim is to further reduce the LC filter's size in the feedback-after-LC architecture.

The proposed architecture-level design introduced a dual voltage/current feedback loop, consisting of an outer voltage feedback loop and an inner current feedback loop. This design aimed to suppress nonlinearity in the LC filter and stabilize the system by splitting the complex poles using the current feedback loop. The inclusion of an HPF reduces the high output impedance of the inner loop, which contributes to increasing the nonlinearity suppression of the capacitor.

The post-layout simulation and verification process were carried out after the schematic-level design and layout design to test the performance of the proposed design. The main chip, fabricated in a 180-nm BCD process, accommodated all blocks except for the sense resistor pair, which was fabricated on another chip using Kelvin connection for smaller parasitic inductance.

The results of the project demonstrated that the proposed design achieved the desired design targets. The use of the current feedback architecture allowed for a higher LC cut-off frequency and reduced the size of the LC filter compared to the state-of-the-art. Based on simulation results, this design also increased the LC filter nonlinearity suppression by > 13 dB.

Overall, this project has implemented current feedback in the feedback-after-LC structure, achieving a reduced size and cost of the LC filter in the Class-D amplifier.

## Reference

[1] H. Zhang, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A −121.5-dB THD Class-D Audio Amplifier With 49-dB LC Filter Nonlinearity Suppression," IEEE J. Solid-State Circuits, vol. 57, no. 4, pp. 1153–1161, Apr. 2022, doi: 10.1109/JSSC.2021.3125526.