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Gate effect in charge-density wave nanowires

E. Slot[1], M.A. Holst[1] and H.S.J. van der Zant[1]

[1] *Kavli Institute of Nanoscience Delft, Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, The Netherlands*

Abstract. We have investigated transport characteristics of charge-density wave nanowires with a few hundred parallel chains. At temperatures below 50 K, these samples show power-law behavior in temperature and voltage, characteristic for one-dimensional transport. In this regime, gate dependent transport has been observed.

1. INTRODUCTION

The reduction of sizes in charge-density wave (CDW) devices has revealed new microscopic aspects of CDW transport [1]. An example is the observation of one-dimensional conduction in CDWs containing on the order of two thousand chains or less [2, 3]. Several methods now exist for preparing such CDW nanowires with cross sections less than 1000 nm^2. Early experiments have been performed with a cleavage technique that has been applied both to $NbSe_3$ and *o*-TaS_3 [2]. More recently, ultrasonic dispersion of bulk crystals has been used to obtain small $NbSe_3$ nanowires [3, 4]. Subsequently, direct growth methods have been developed by either a reaction of Nb and Se to obtain $NbSe_3$ nanowires and ribbons [5] or by chemical vapor transport to synthesize *o*-TaS_3 nanoscale systems from pure tantalum sheets and sulphur powder [6].

In previous work [3] we have performed a systematic study of the transport properties of $NbSe_3$ nanowires with different cross sections. When the number of chains is more than about 2000, we observed metallic behavior down to the lowest temperatures. When there are less than 2000 chains, the low-temperature state is non-metallic: the resistance increases as the temperature decreases. Transport shows a power-law behavior in temperature and voltage, characteristic for one-dimensional transport and a detailed analysis indicates that the non-metallic behavior is due to to quasi-particles. Here, we report on the gate effect in $NbSe_3$ nanowires with a few hundred parallel chains. The samples have been made by the ultra sonic dispersion method [3, 4]. In short, bulk $NbSe_3$ crystals were put in a bottle with pyridine and were ultra-sonically cleaved. After several hours of cleaving, a suspension of $NbSe_3$ nanowires with widths ranging from 30 to 300 nm and lengths from 2 to 20 μm emerges. A drop of the suspension is deposited onto a degenerately doped Si substrate with a 1 μm thick SiO_2 layer. The Si substrate serves as a backgate isolated from the wires by the insulating SiO_2. Nanowires are selected and located with an optical microscope with respect to predefined markers on the substrate and subsequently a contact pattern is defined with e-beam lithography. Gold and a Ti sticking layer are deposited within minutes after a 3 second dip in ammonium buffered hydrofluoric acid to optimize contact resistances. An example of a contacted nanowire is shown in Fig. [1] .

2. RESULTS AND DISCUSSION

We have investigated the gate dependence of several samples that exhibited power-law temperature dependences. In general, changes are observed when varying the voltage on the gate, but no systematic study could be performed because frequent switches often occurred. This is most clearly illustrated when comparing current-voltage (*I*-*V*) characteristics with the gate floating and with the gate grounded.

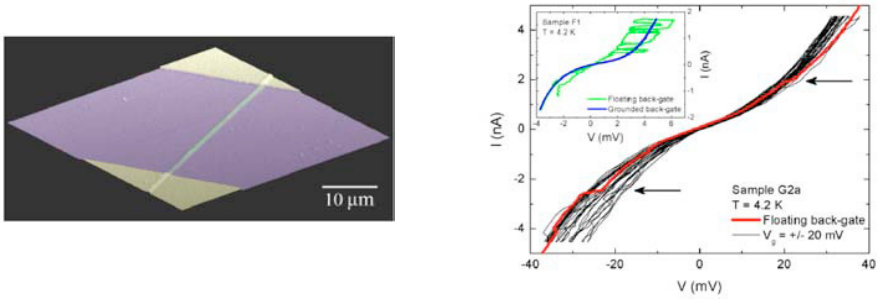

Figure 1. Left: An atomic force image of a $NbSe_3$ nanowire with a thickness of 60 nm and a width of 160 nm. Right: Current-voltage curves of a nanowire with about 350 chains (250 nm^2 cross section) and a length of 2.6 µm. The red curve is recorded with a floating back gate. The thin black curves are recorded during 10 minutes at a rate of 10 mHz while sweeping the gate voltage between –20 and +20 mV at a rate of 3 mHz. Inset: Current-voltage curves for a nanowire with about 300 chains and a length of 1.5 µm. With the back gate floating, switches are observed.

In the latter case, the I-V curves are smooth whereas in the former case switches often occur (see Fig. 1). This behaviour also manifests itself when recording the zero-bias resistance as a function of temperature. With the gate floating, large variations in the resistance can be observed which grow in magnitude as the temperature is lowered. The switches are most likely due to changes in the electrostatic environment but the precise mechanism remains unclear.

As no systematic gate dependence could be observed, we have mapped out the possible traces by recording the current as a function of voltage while sweeping the gate voltage. The result is shown in Fig. 1 (right hand side; main figure). The capacitance to the back-gate (C) for this sample is estimated to be 10 aF corresponding to a voltage (e/C) of 6 meV, where e is the elementary charge. With a gate voltage range of 40 meV, about 6e of charge can be induced on the nanowire. Clearly, the figure shows that I-V curves are modulated by the gate appreciably, resembling the behaviour of a few charging islands in series. The gap size (the region of current suppression) is in reasonable agreement with this observation given the estimate given above of the charging energy.

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