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A Fully Integrated Recursive Switched-Capacitor DC-DC Converter with Hybrid Hysteresis-CFM Control

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***Abstract*—This work presents a switched capacitor power converter (SCPC) with instant transient response and minimized steady-state output ripple. The proposed SCPC employs a hybrid control strategy that amalgamates the strengths of hysteresis and continuous frequency modulation (CFM) controls, thus elevating transient performance while maintaining a small steady-state ripple. The system adopts a 10-phase interleaved recursive switched capacitor (RSC) topology with adaptive capacitor sizing to achieve configurable voltage-conversion ratios (VCR) with heightened efficiency, power density, and load ability. Additionally, a novel adaptive switch-sizing technique is introduced to improve light-load efficiency. Fabricated in 180-nm BCD technology, the chip supports a wide-range load current of 0.7mA-120mA and converts a 0.8-to-3.6V input to a 0.25-to-2.4V output with a peak efficiency of 87.1%. The proposed converter simultaneously achieves a low voltage ripple of 12mV and an over-/under-shoot voltage of less than 50mV even under significant load transient steps (171X).**

***Index Terms*—Switched capacitor, continuous frequency modulation (CFM), hysteresis control, hybrid control.**

I. Introduction

Fully integrated SCPCs have showcased their substantial advantages over inductive power converters due to full CMOS integration capability. Prior SCPCs have provided pragmatic techniques employing multiple VCR topologies to enhance power conversion efficiency (PCE). Besides the PCE, transient performance is crucial, especially for supply-sensitive and fast-changing loads. To address this, multiple control techniques have been proposed, as shown in Fig. 1. Many conventional SCPCs adopt hysteresis control due to its inherent stability and rapid transient response. However, this approach suffers from substantial output ripple attributed to the inherent nature of the hysteresis window [1]. Alternatively, pulse-skipping control mitigates the demand for the buffer capacitor while reducing the output ripple; however, it necessitates one comparator in each time-interleaving channel, leading to an increase in silicon area and power consumption. Meanwhile, its average output voltage varies with changes in the load current, resulting in poor regulation performance [2]. Comparatively, time-interleaved CFM control presents a noteworthy advantage in achieving a low output voltage ripple and an enhanced PCE compared with other techniques; however, it shows poor transient responses due to its integral feedback loop [3]. While different control techniques have their own advantages in either transient responses or output voltage ripples, a new strategy achieving both is urgently needed.

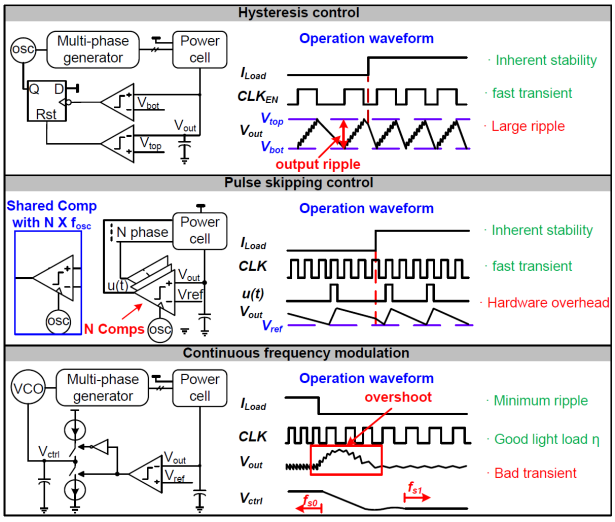


Fig. 1: Conventional control strategies.

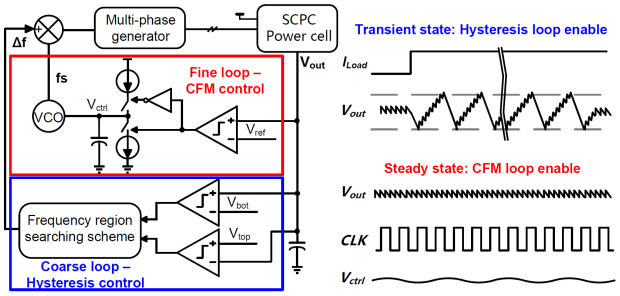


Fig. 2: Conceptual architecture of the proposed HHC system.

This paper proposes a hybrid hysteresis-CFM (HHC) control strategy to achieve low steady-state output ripple and enhanced transient performance simultaneously, by taking the strengths of both techniques. In addition, to achieve extended VCR range and high PCE, the proposed system adopts RSC topology [4] with adaptive capacitor sizing, for optimal load-driving capability at different VCRs. Adaptive switch-sizing is also employed to optimize the switch sizes for different loads,

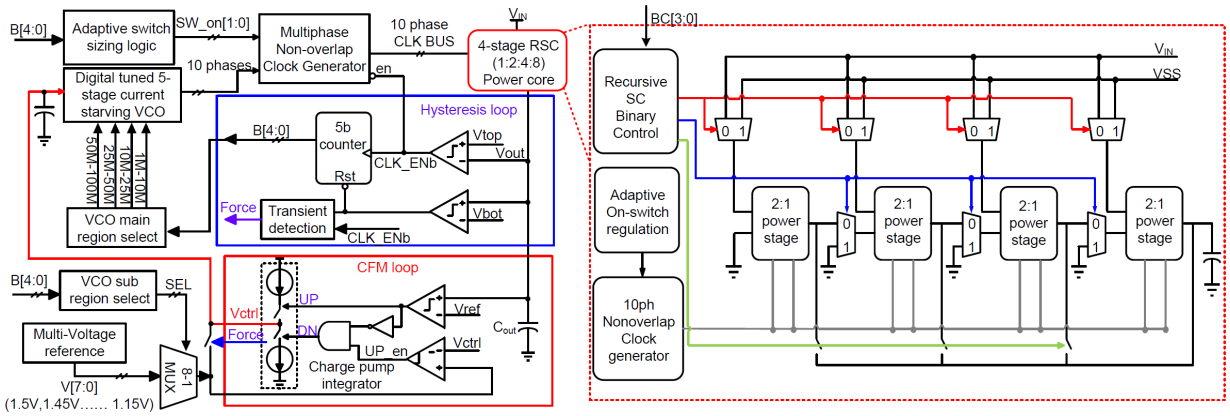


Fig. 3: Implementation overview of the proposed Hybrid Hysteresis-CFM control strategy.

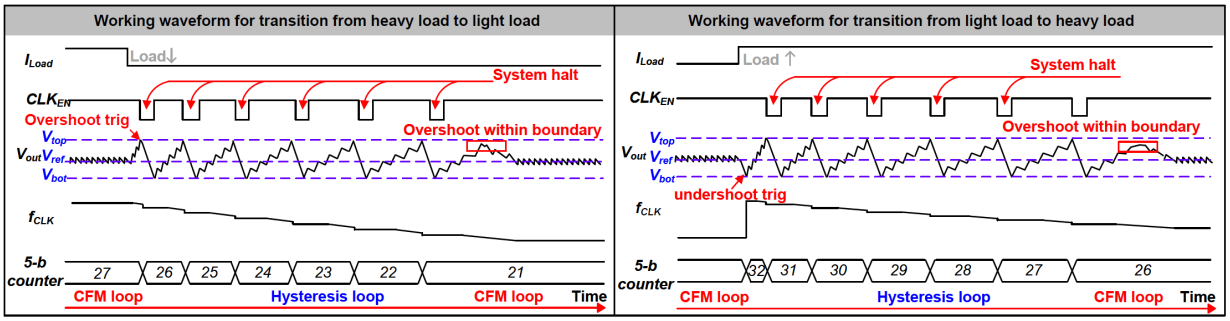


Fig. 4: Proposed HHC system ideal working waveform.

significantly reducing switching losses for light loads.

II. Proposed Hybrid Hysteresis CFM Control

A. Charge accumulation analysis

In a conventional CFM control loop, the transient response is relatively slow due to the Proportional-Integral (PI) control mechanism. The CFM control regulates the switching frequency (f_{s0}) corresponding to a specific load current (I_0). When the load current instantly changes to I_1, this control mechanism embodies a second-order feedback system to converge the switching frequency from f_{s0} to f_{s1}. Noting $\triangle f = f_{s0} - f_{s1}$, the shooting voltage significantly depends on the value of $\triangle f$ and f_s. By linearizing the model, the voltage variation curve can be expressed as

$$\triangle V(t) = \int \frac{I_{in} - C_{fly}(\frac{1}{2}V_{in} - V_{out} - \triangle V_1)f_{VCO}}{C_{out}}. \quad (1)$$

where $f_{VCO} = f_s + \triangle f - K_{VCO}\frac{I_{CP}}{C_{CP}}t$. The shooting voltage can then be determined as the peak value of the curve. There exists a strong correlation between the $\triangle f$ and shooting voltage, smaller $\triangle f$ results in lower shooting voltage and vice versa. The proposed system operates based on the previous principle. By constraining the frequency, the overshoot voltage can be limited. The conceptual architecture is shown in Fig. 2. During a transient moment, the system regulates the output through hysteretic control to achieve fast transient and limited voltage shooting, while, in the steady state, the system regulates the output through CFM control to keep the ultra-low output voltage ripple.

B. Top-level Architecture & Working principle

Fig. 3 shows the architecture of the proposed system, which consists of a power core, a hysteresis feedback loop, a CFM feedback loop, and control blocks. The power stage employs a 4-stage RSC topology, encompassing 15 2:1 power cell units for adaptive capacitor sizing. The four stages have a ratio of 1:2:4:8 for minimizing the equivalent output resistance, thus enhancing the load ability. Each 2:1 power cell unit consists of 10-phase time-interleaved 2:1 SC sub-cells. The 10-phase clocks are inherently generated by the on-chip VCO.

Fig.4 shows the working waveform. During steady state, the system regulates the output voltage, V_{out}, in the CFM loop to minimize the output voltage ripple. When the load current suddenly becomes heavier, V_{out} decreases since the current clock frequency, f_{CLK}, cannot sustain the heavier load. When V_{out} touches the lower hysteresis threshold V_{bot}, the hysteresis control loop of the proposed HHC control system is activated to prevent V_{out} from going too low. Then, the system uses an interleaved coarse-fine frequency tuning scheme to determine the target f_{CLK}. In the coarse loop, f_{CLK} jumps among 32 discrete frequency steps, starting from the highest one. Every time f_{CLK} jumps to a new value, the fine loop is engaged to let the CFM loop try to regulate V_{out} with the

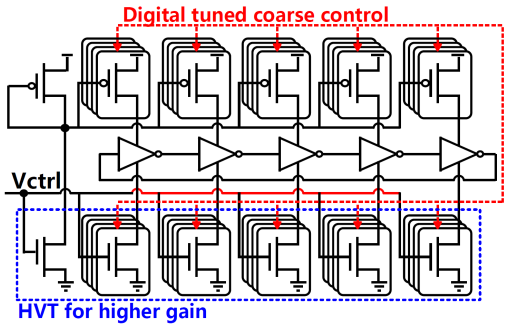


Fig. 5: Digitally tuned current-starving VCO.

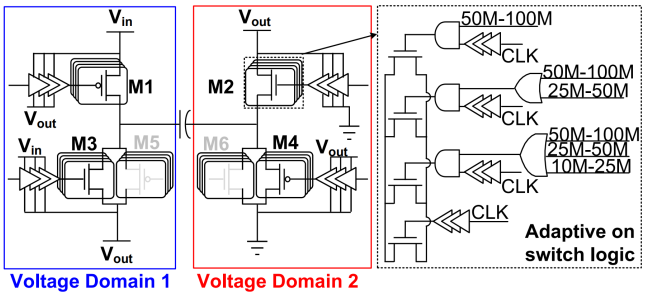


Fig. 6: Circuit diagram of a power cell.

current f_{CLK} as an initial frequency. If the current f_{CLK} step is too high, V_{out} cannot be pulled by the CFM loop and it will reach the higher hysteresis threshold, V_{top}. The system then halts to let the V_{out} drop, so that V_{out} does not go beyond the hysteresis threshold. When V_{out} drops to V_{bot} again, the system reboots, and f_{CLK} switches to the next frequency to start the CFM fine-tuning again. This interleaved coarse-fine tuning repeats until V_{out} can be pulled back by the CFM loop without reaching V_{top}. Subsequently, the system stays in the CFM loop to finely tune the frequency to achieve a low output ripple. Similarly, when the load current decreases abruptly, V_{out} reaches V_{top}, and the aforementioned interleaved coarse-fine process starts. In essence, the proposed system effectively confines overshoot and undershoot voltages within the predefined hysteresis window demarcated by V_{top} and V_{bot}, while simultaneously achieving minimal V_{out} ripple during steady-state CFM operations.

C. Digital tuned current-starving VCO

Fig.5 depicts the circuit diagram of the key component of the proposed HHC system, a 5-stage digitally tuned current-starving VCO, which is capable of inherently generating 10-phase interleaved clock signals. The VCO is controlled by the switching current, which is determined by the control voltage (V_{ctrl}), and can be digitally tuned by adjusting the number of current sources. Thus, resulting in finely partitioned output frequency regions. The digital tuning divides the VCO frequency regions into 4 main frequency regions, and the voltage control further divides each main region into 8 sub-regions. This yields a total of 32 clock frequency regions. Slight overlaps between two adjacent regions are designed

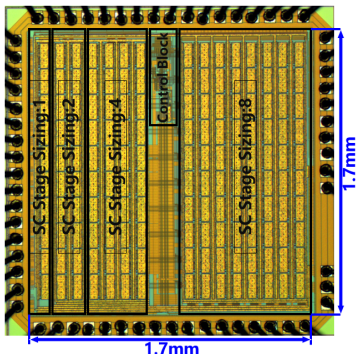
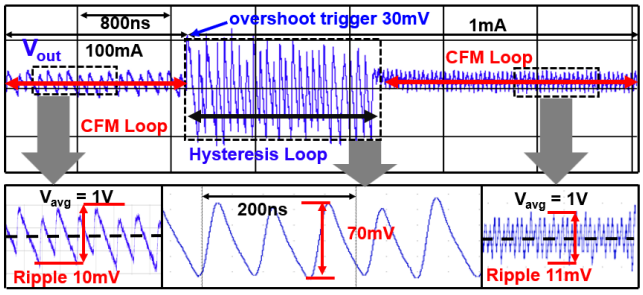
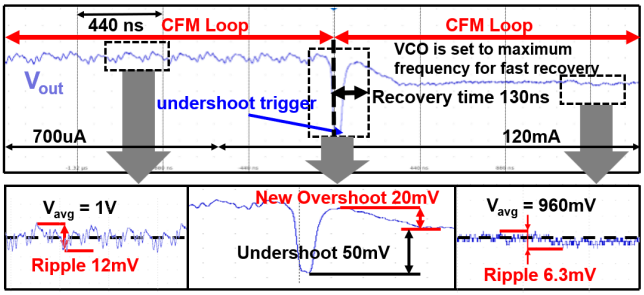


Fig. 7: Die photo.



(a) Transient wavefrom from heavy load to light load



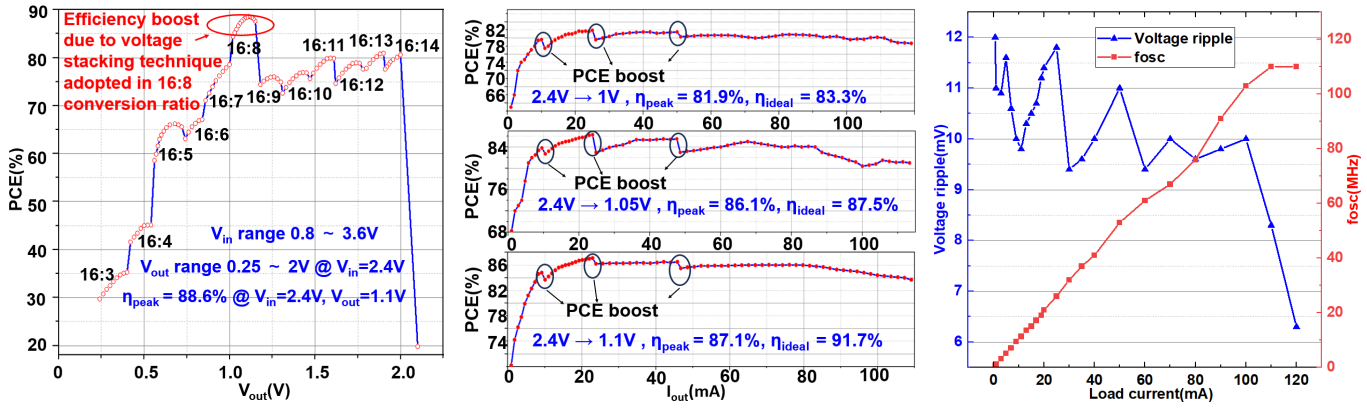
(b) Transient waveform from light load to heavy load

Fig. 8: Measured transient waveform.

intentionally, ensuring seamless tracking of the load current. The control voltage (V_{ctrl}) is generated via a charge pump-based integrator meticulously designed to uphold a favorable phase margin for the system.

D. Power cell implementation

Fig. 6 shows the circuit diagram of the power cell. To minimize switching losses and prevent breakdown. A voltage-domain stacking technique is employed for the VCR=1/2 case with M5 and M6 deactivated to reduce switching loss. For VCR cases other than 1/2, M5 and M6 are activated to form transmission gates for voltage transfer. An adaptive switch-sizing technique is proposed to optimize the switch sizes for different clock frequency regions, leveraging the HHC system. In lower frequency regions, corresponding to lighter loads, fewer parallel switches are activated, resulting in smaller switch sizes. This approach effectively mitigates switching losses, particularly in light load conditions.



(a) (b) (c)

Fig. 9: Performance measurement: (a)Power conversion efficiency for open loop, (b)Power conversion efficiency for close loop, (c) Ripple and switching frequency vs load current.

III. Measurement Results

The proposed HHC SCPC was implemented in a 180nm BCD technology, utilizing total MIM capacitors (C_{FLY}) of 1.8 nF and MOS capacitors (C_{OUT}) of 3.4 nF. Fig.7 shows the die photo. Fig.8 presents the measured waveform of V_{OUT} when load current goes from 100 mA to 1 mA, and from 700 µA to 120 mA, respectively. Thanks to the hysteresis boundaries during load variation transitions, the over-/undershoot voltages are limited to 30 mV and 50 mV, respectively. During the hysteresis control periods in Fig.8(a), the frequency of the CFM loop is performing coarse-fine searching, resulting in a zigzagged V_{OUT} waveform, as expected in Fig. 4. The V_{OUT} is not zigzagged in Fig.8(b) because the frequency coarse searching starts from the highest frequency range, which matches the heavy load condition (120 mA). Hence, the system enters the fine searching right after the first coarse searching. During the steady state, due to the engagement of the CFM control, the system achieves an ultra-low output voltage ripple of up to 12 mV.

The performance measurement for the proposed converter is shown in Fig.9. PCE measurement has been conducted for both open loop and closed loop. The proposed system achieves a peak efficiency of 88.6% and 87.1% in open and closed loop measurements, respectively. Thanks to the HHC control technique, the proposed converter achieves the lowest output voltage ripple and shooting voltage simultaneously, with the largest load transient step (170×).

IV. Conclusion

This paper introduces a novel Hybrid Hysteresis-CFM controlled RSC DC-DC converter. The proposed system demonstrates noteworthy achievements in minimizing shooting voltage and reducing output ripple simultaneously. The transient measurements proved the efficacy of the Hybrid Hysteresis-CFM (HHC) control strategy, establishing it as a robust choice for implementing control schemes in SCPCs to power fast-changing and supply-sensitive loads.

TABLE I: Comparison table with prior arts.

	ISSCC'14[6]	ISSCC'18[7]	JSSC'19[3]	ISSCC'23[5]	This work
Process	32nm	65nm	65nm	65nm	**180nm**
Fully-integrated	Yes	Yes	Yes	Yes	**Yes**
Active Area	0.15 mm²	2.42 mm²	0.61 mm²	4.76 mm²	**2.89 mm²**
Topology	2:1, 3:2 SC	AVFI	2:1 SC	RCSC	**RSC**
Cap type	Deep Trench	MIM+MOS	MOS	MOS+MOM	**MIM+MOS**
C_{fly}/C_{out}	1 nF/0	8 nF/6 nF	2.56 nF/0	19.8 nF/0	**1.8 nF/3.4 nF**
Interleaving phases	16	4	15	66	**10**
Vin	1.8 V	0.22-2.4 V	2.4 V	0.4-2.5 V	**0.8-3.6 V**
Vout	0.7-1.1 V	0.85-1.2 V	1 V	0.2-2 V	**0.25-2 V @ Vin=2.4 V**
Max I_{load}	365 mA	80.1 mA	138 mA	20 mA	**120 mA**
Power density	5600 mW/mm²	33 mW/mm²	240 mW/mm²	6.3 mW/mm²	**41.5 mW/mm²**
Peak eff	86.4%	84.1%	82.8%	83.9%	**87.1%(close loop) 88.6%(open loop)**
Control Strategy	Pulse skipping	Pulse skipping	CFM	CFM	**Hybrid Hysteresis-CFM**
Load transient step	30 mA-365 mA (12X)	4 mA-25 mA (6X)	11 mA-138 mA (12.5X)	1 mA-19.8 mA (20X)	**0.7mA-120mA (171X)**
Overshoot/Undershoot	125 mV	60 mV	200 mV	600 mV	**50 mV**
Voltage ripple	30 mV	36 mV	60 mV	200 mV	**12 mV**

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