Inverter Stage and Controller Architecture Design for a Modular Solid-State Transformer

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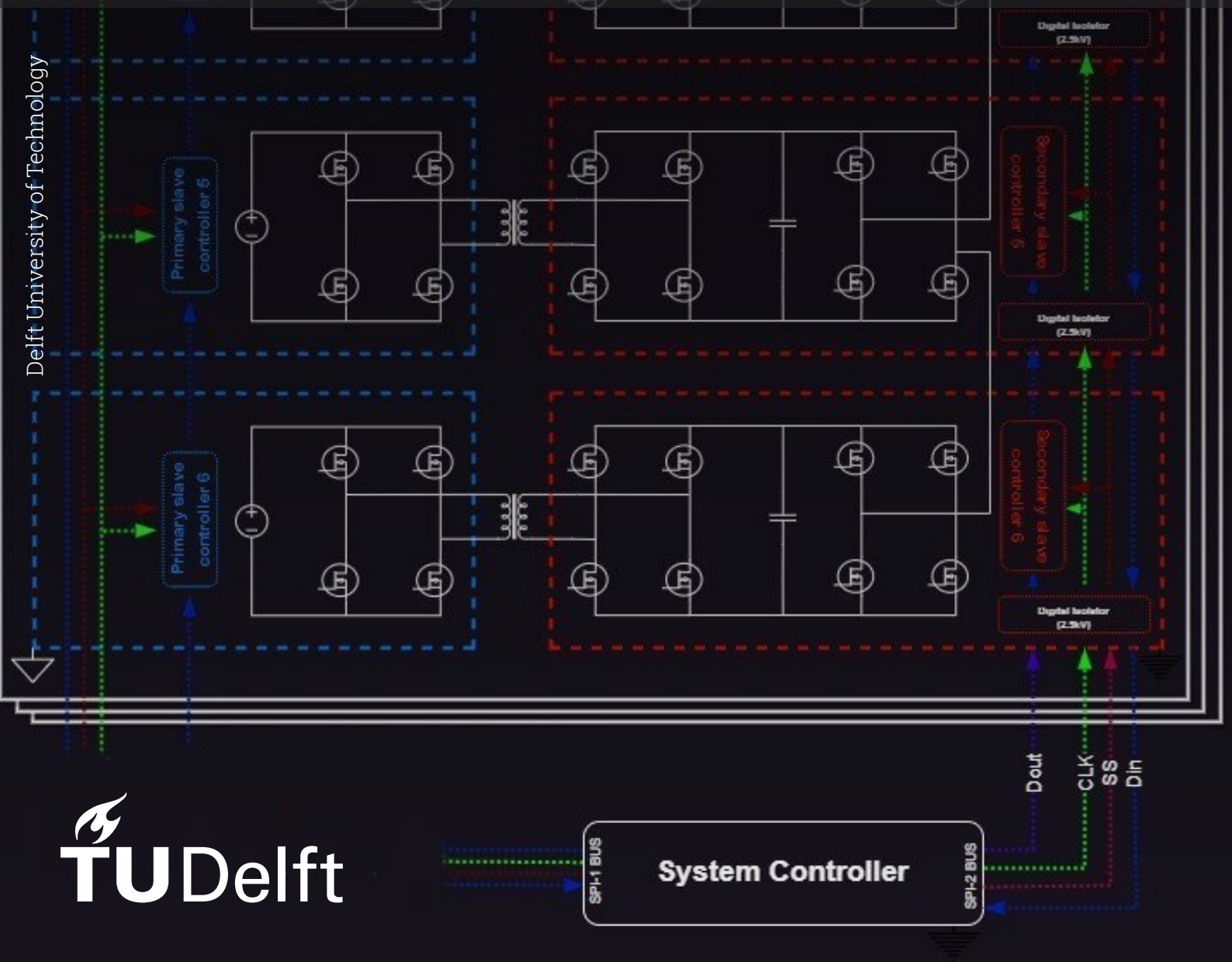

TU Delft

Inverter Stage and Controller Architecture Design for a Modular Solid-State Transformer

by

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Abstract

This master's thesis presents the design and analysis of the inverter stage and controller architecture for a modular solid-state transformer (SST) to interconnect DC microgrids and a 10kV AC grid for bidirectional power flow. The research focuses on inverter topologies, modulation techniques, and modular controller architecture.

The inverter stage, a crucial stage of the modular SST, converts DC power from microgrids to AC power suitable for the 10kV AC grid. The most popular inverter topologies for modular converters are researched and investigated based on their compatibility with the specific application. Factors such as efficiency, power quality, harmonic distortion, number of components, control complexity, and scalability are considered for this process. Along with the topology, modulation techniques are important in producing high-quality output waveforms and efficient power transfer. Different modulation strategies, including pulse width modulation (PWM) techniques and space vector modulation schemes specifically for multilevel converter applications, are reviewed and discussed in terms of how they affect the system's performance.

In addition to the inverter stage, the thesis focuses on designing a modular controller architecture for the SST. The controller design prioritizes maintaining flawless data flow and synchronization between all controllers for converter and AC grid coordination. The central controller and distributed control architectures are studied and evaluated for scalability, modularity, and flexibility. The distributed architecture enhances the system's overall flexibility but is subject to synchronization issues and limitations in communication bandwidth. These issues are addressed in the developed design.

To evaluate the performance of the proposed inverter stage and controller architecture, extensive simulations and experimental validations are carried out. The simulations consider various operating conditions, such as islanded and grid-connected modes, to assess the system's stability, control, harmonic content, and power quality in the output waveforms. The simulation results indicate that the chosen inverter design and modulation strategies successfully attain high efficiency and minimal harmonic distortion in the operation of the converter. The modular, distributed controller design demonstrates its ability to provide seamless operation and effective coordination between DC microgrids and the AC grid.

Overall, this master's thesis contributes to the advancement of solid-state transformer technology by delving into the design of the inverter stage and controller architecture for interconnecting DC microgrids and a 10kV AC grid and providing useful insights. The findings and recommendations can be a valuable framework for future research and development of modular SSTs for grid-connected applications.

Acknowledgement

I would like to express my deepest gratitude and appreciation to all those who have supported me throughout this phenomenal journey of finishing my master's thesis. This work would not have been possible without their unwavering encouragement, guidance, and love.

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Nomenclature

Abbreviations

Abbreviation	Definition
SST	Solid-State Transformer
DC	Direct Current
AC	Alternating Current
PWM	Pulse-Width Modulation
DES	Distributed Energy Systems
THD	Total Harmonic Distortion
SVPWM	Space vector Pulse-Width Modulation
SPWM	Sinusoidal Pulse-Width Modulation
RMS	Root Mean Square
NPC	Neutral Point Clamped
FC	Flying Capacitor
MMC	Modular Multilevel Converter
CHB	Cascaded H-Bridge
HNPC	H-Bridge Neutral Point Clamped Converter
EMI	Electromagnetic Interference
HB	Half-Bridge
SM	Sub-Module
PS-PWM	Phase-Shifted Pulse-Width Modulation
LS-PWM	Level-Shifted Pulse-Width Modulation
PD-PWM	Phase Disposition Pulse-Width Modulation
POD-PWM	Phase Opposition Disposition Pulse-Width Modulation
APOD-PWM	Alternate Phase Opposition Disposition Pulse-Width Modulation
BW	Bandwidth
SPI	Serial Peripheral Interface
CAN	Controller Area Network
DC	Distributed Clocks
MOSI	Mater-Out Slave-In
MISO	Master-In Slave-Out
CLK	Clock Signal
SS\CS	Slave Select\Chip Select
SDO	Slave Data-Out
SDI	Slave Data-In
MSB	Most Significant Bit
LSB	Least Significant Bit
PLL	Phase Locked Loop
PI	Proportional Integral
CMC	Common Mode Current

1 Introduction

1.1. Background Information

Distributed Energy Systems (DES), like microgrids, are becoming increasingly important as the world shifts towards more renewable energy sources. A microgrid is a small-scale grid that can either co-exist and operate with the primary power grid or operate independently. It consists of several interconnected power sources and loads that can be controlled and managed as a single entity. Many challenges are being faced by traditional centralized power systems, including energy security, resilience, and sustainability, and microgrids are emerging as promising solutions.

The concept of DC microgrids has been gaining popularity over recent years. A DC microgrid, similar to any other microgrid, is a self-contained power system. However, it operates using direct current (DC) rather than alternating current(AC), which traditional power grids use. Renewable energy sources such as solar panels and wind turbines naturally produce DC power and are well suited for integrating into a DC microgrid. Integrating these renewable sources with DC microgrids can help reduce the energy losses within a grid by eliminating the need for DC/AC conversion and, thus, improve the efficiency of the entire power system.

There are several reasons why DC microgrids are becoming increasingly important. The ability to operate independently of the main power grid, providing a reliable source of electricity in the event of a power outage, is one of the primary and most significant advantages. DC microgrids can also help to reduce the environmental impact of energy production by incorporating more renewable energy sources and improving energy efficiency.

In addition to these benefits, DC microgrids can help tackle some of the issues confronting traditional power grids. For example, by providing localized power generation and distribution, they can help reduce the demand for expensive upgrades in the current infrastructure and transportation needs. They can also help minimize the dependence on centralized power systems vulnerable to cyber-attacks and other security threats, thus, enhancing energy security. Overall, DC microgrids have the potential to be critical in the transition to a more sustainable and resilient energy system. As technology evolves and prices drop, we expect to see increasing adoption of DC microgrids in various applications.

The electrical grid is one of modern society's most vital infrastructure systems, delivering electricity to homes, businesses, and industries. With the increasing adoption of renewable en-

ergy sources as explained in [1] and the electrification of transportation systems, the traditional power grid faces new challenges, including improved reliability, efficiency, and flexibility. Solid-State Transformers (SSTs) are emerging as a promising solution to these challenges, offering a range of benefits over traditional transformers with application areas, as shown in Fig.1.1.

For over a century, traditional transformers have been used to step up or down the AC voltage. However, with the changing grid design for the future, they are unsuitable and have several limitations. This includes factors such as being bulky, inefficient, and vulnerable to voltage fluctuations and other disturbances. Integrating renewable and distributed energy resources into the current utility grid requires adapting advanced power electronics technology.

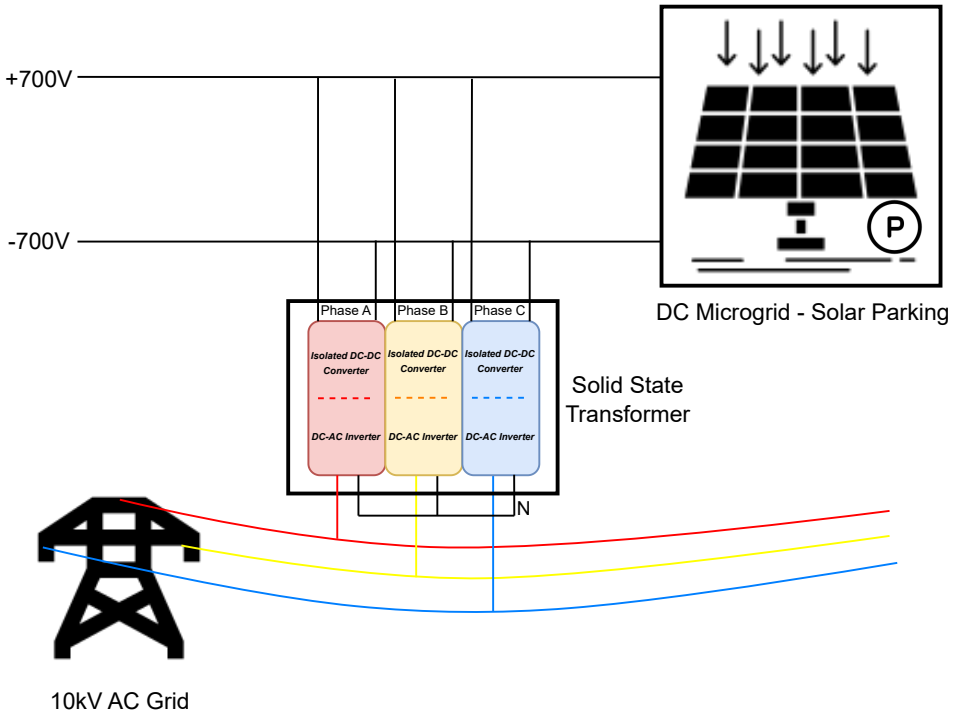


Figure 1.1: Application of Solid-State Transformers

To overcome all these drawbacks of conventional transformers and provide more flexibility, solid-state transformers can be utilized as explained in [2]. They incorporate semiconductor technology to convert AC power to DC power and back to AC power at the desired voltage level. They offer several advantages [3] over traditional transformers, including:

1. **Increased efficiency:** SSTs are more efficient than conventional transformers due to the usage of semiconductors, which aids in lowering overall energy losses and, thus, helps lower electricity prices.

2. **Better voltage regulation:** SSTs with proper control techniques can help regulate the voltage better. Their inherent support for advanced power electronics is essential for integrating renewable energy sources and other distributed energy resources.

3. **Improved reliability:** SSTs are more reliable than conventional transformers, as they are less susceptible to failures. They also can operate in a wider range of conditions.

4. **Reduced size and weight:** SSTs are more compact and lighter than conventional transformers due to advanced semiconductor technology, which helps reduce the overall space required for substations and makes the installation process easier. Their ability to operate at high switching frequencies helps reduce the required inductance and overall size, increasing power density.

Overall, SSTs have the potential to play a critical role and be an integral part of the future grid, as they can aid in improving the efficiency, reliability, and modularity of the power system. As semiconductor technology continues to grow and prices reduce in the future, there lies a huge potential for SSTs to be used in a wide range of applications.

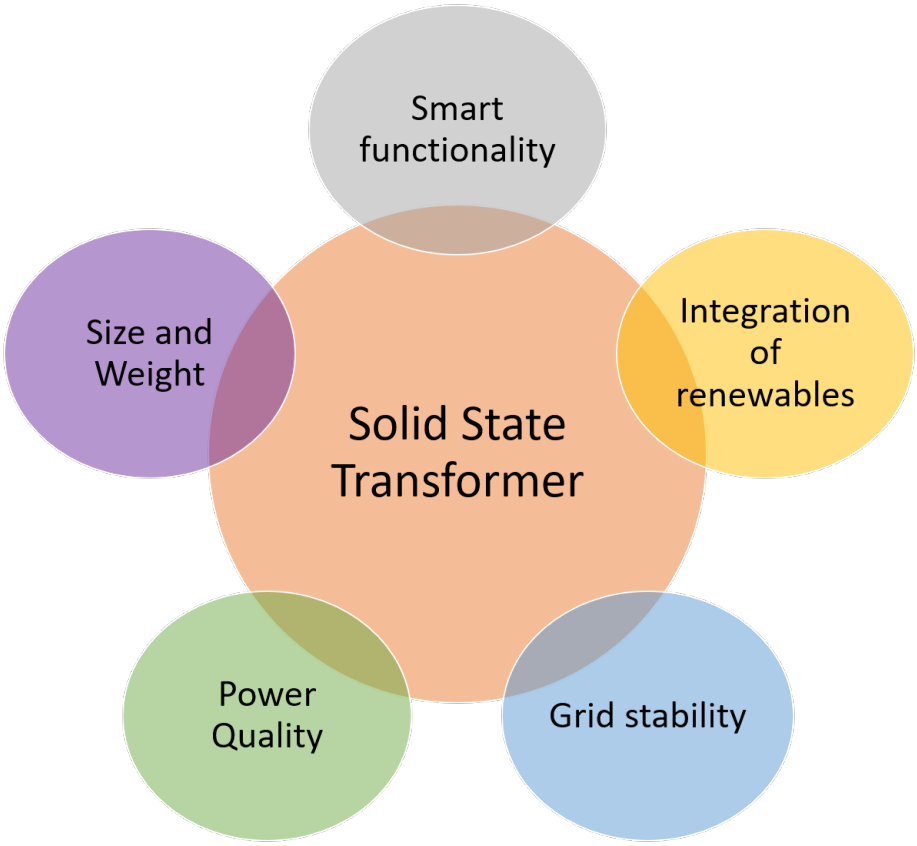


Figure 1.2: Advantages of Solid-State Transformers

1.2. Motivation and Research Questions

Traditional power distribution systems fail to adapt to the power grid's rapidly changing power requirements as the demand for renewable energy sources rises. Conventional transformers cannot provide the essential control and power conditioning required to efficiently integrate renewable energy sources into the existing grid, resulting in power quality concerns and diminished system stability. Solid-state transformers (SSTs) have emerged as a viable alternative to conventional transformers, providing increased efficiency, reliability, and flexibility.

However, further research is required into the design, control, and deployment of SSTs in power distribution systems. As a result, there is an immediate need to investigate the potential

benefits of SSTs and solve the issues associated with integrating renewable energy sources into the grid. SST research studies can give insights into the design, control, and performance of SSTs in real-world applications, allowing power engineers to design and build more efficient, modular, and sustainable power distribution systems capable of meeting the rising demand for renewable energy sources. The following research questions are addressed in this thesis:

1. *Which topology is best suited for a medium voltage (10kV) DC/AC converter in a solid-state transformer (SST)?*

2. *What are the different modulation techniques for multilevel grid-connected power converters and how to implement them?*

3. *What is a suitable control architecture for a modular solid-state transformer (SST), and how to design it?*

1.3. Thesis Outline

Following a thorough literature review and several simulations, the research questions are addressed in several sections of this thesis. The synopsis of each section of the research work is given below:

- **Chapter 1** provides the required background information, the need and motivation for research, and the structure of the thesis.
- **Chapter 2** discusses a literature review of multilevel converters, including the most preferred topologies for similar application converters and their modulation techniques. It also focuses on specific parameters, such as the switching frequency, Total Harmonic Distortion (THD), output filter sizing, and the associated challenges in designing the system.
- **Chapter 3** focuses on developing a suitable controller architecture for modular SSTs. It starts with a comparison of central and distributed designs and addresses the scalability and flexibility issues. It also provides solutions to overcome constraints such as communication bandwidth, isolation requirements, and data synchronization in distributed control architecture.
- **Chapter 4** focuses on the developed space vector algorithm for multilevel converters. The challenges in using SVPWM for higher-level converters are compared with SPWM modulation strategies regarding THD levels and switching losses. It also provided insight into the computational aspect of using such algorithms on microcontrollers.
- **Chapter 5** provides insights into the implemented hardware boards and testing results. Several considerations for the hardware prototype design are discussed in this chapter. Several tests on the developed hardware to validate the design and their outcomes are discussed.
- **Chapter 6** concludes the work done in this thesis and briefly describes potential future developments to further the work into modular SSTs.

1.4. Summary

The introduction chapter provides an overview of the background information, research objectives, motivation, and scope of the thesis project. The chapter begins by emphasizing the increasing relevance of solid-state transformers (SSTs) in modern power systems, notably in interconnecting DC microgrids with the AC grid. It underlines the importance of efficient power

flow between the grids, which can be accomplished by designing a modular inverter stage and controller architecture.

The introduction chapter concludes by outlining the methodology adopted in the research and the chapters' overview classification. The introduction chapter sets the stage for the subsequent chapters, highlighting the importance of designing an efficient inverter stage and controller architecture for interconnecting DC microgrids and a 10kV AC grid with bidirectional power flow.

2

Literature Review: Inverter Topology and Modulation Techniques

Solid State Transformer was first mentioned way back in 1980 [4]. However, it was not considered feasible with the hardware and technology solutions back then. There has been continuous research and evolution in the field of power electronics. The research work made the concept of SSTs more and more feasible and exciting. This tremendous amount of research enables us to develop different hardware architectures and topologies. It also gave rise to several application areas for SSTs, such as traction systems, smart grids, and energy generation systems, as mentioned in [3]. This thesis will limit its focus to the interconnection between DC microgrids and the existing AC grid. This chapter focuses on the research conducted in different converter topologies and their modulation techniques.

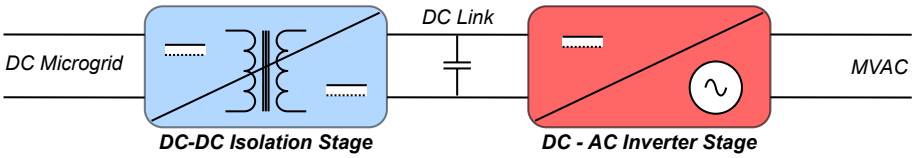


Figure 2.1: Type of SST

For interconnecting a DC microgrid with the existing medium voltage AC grid, a two-stage SST [2] is required.

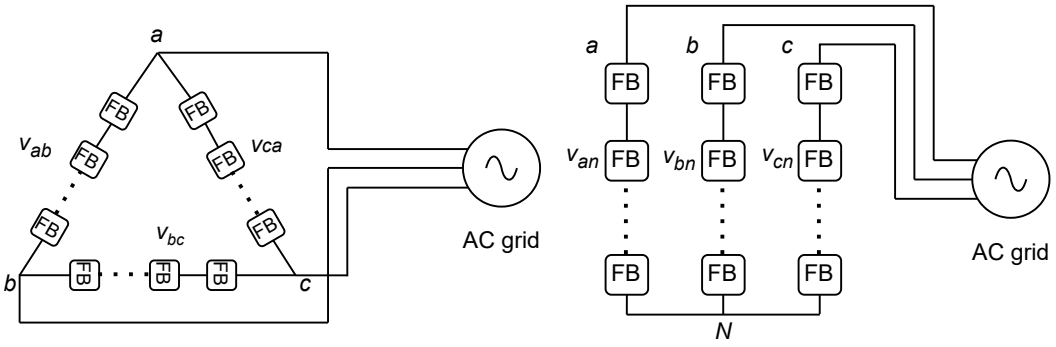
S.No.	**Parameter**	**Value**
1.	DC Voltage	+-700V
2.	AC Voltage	10kV, line-line, rms
3.	Power Rating	100-150 kVA
4.	Power Flow	Bidirectional
5.	Design Methodology	Modular and Scalable
6.	Control Requirement	Microcontroller based system

Table 2.1: Initial Design Parameters

For this application, SST involves an isolated DC-DC converter with a high-frequency isolation transformer and a DC-AC converter at the secondary side with a DC link between the two

power electronics converters, as shown in Fig.2.1. The isolation stage ensures that the fault currents from one grid do not affect the other grid. The converter enables bidirectional power flow between the two grids with all the merits of an SST mentioned earlier. The following parameters, as shown in Table 2.1, are considered for the initial design phase.

Before delving into converter topologies and their suitability for specific applications, the two converter configurations - star and delta topologies must be compared. A simple configuration of delta and star inverters is shown in Fig. 2.2.



(a) Delta-connected Inverter **(b)** Star-connected Inverter

Figure 2.2: Delta and Star Configurations

As can be seen in Fig.2.2, for a grid-connected inverter, the full bridges in each of the legs of the inverter must be rated for a higher voltage in the case of delta configuration ($V_{line} = V_{phase}$) than in the case of star configuration ($V_{line} = \sqrt{3} * V_{phase}$). This is because each of the legs in a delta inverter has to be rated to handle the line-line voltage as compared to a star inverter, where each of the inverter legs has to be rated to handle only the line-neutral voltage, which is lower than line-line voltage by a factor of $\sqrt{3}$. An alternative to using full bridges with higher voltage-rated switches is using a higher number of cascaded full bridges.

A delta-connected inverter allows for significant advantages such as the potential to deal with inter-phase power imbalance in PV applications, as explained by [5]. However, these advantages are irrelevant to this project, so only star-connected configurations are considered in this thesis.

2.1. Multilevel Converter Topologies

To approach this design, research into multilevel converters is required. A multilevel converter uses several commercially available, inexpensive, and comparatively low voltage-rated power electronics devices and is scalable to higher voltage levels. This results in a complex design and several challenges in the implementation phase. However, with proper research and further development, multilevel converters are becoming attractive for power electronics converter designs. On the other hand, using simple two-level converter results in a more straightforward overall design. However, it requires high-power semiconductor technology, and the device ratings limit the overall system scalability. As demonstrated in [6], the differences between the conventional and multilevel inverter topologies are summarized in the following Table 2.2:

Parameter	Two-Level Inverter	Multilevel Inverter
Total Harmonic Distortion (THD)	High	Low
Switching Losses and Stress	High switching frequency, high losses, high stress	Low switching frequencies, low losses, low stress
dv/dt	High	Low
Voltage Levels/ Application	Lower voltage levels	Higher voltage levels

Table 2.2: Two-Level vs. Multilevel Inverter

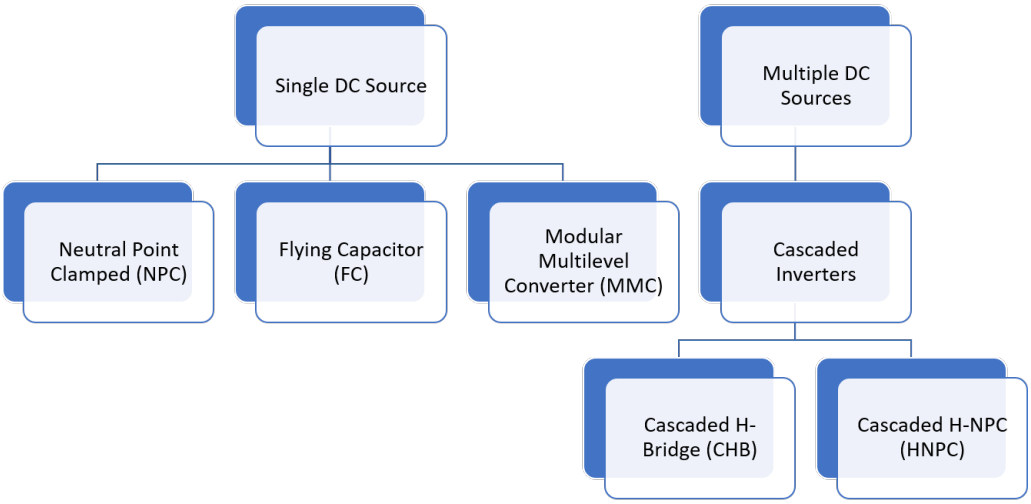


Figure 2.3: Multilevel Inverters Classification

There are two different types of multilevel topologies [6, 7] according to the voltage sources at the input of the inverter, as shown in Fig.2.3. In the DC-AC conversion stage of SST, multiple DC sources are available as input from the respective DC-DC converter stages. Therefore, for this application, multiple DC source inverter topologies are suitable. The two cascaded topologies are compared and summarised in the following sections. By cascading all the DC sources, MMC topology can also be investigated for this design, as it has become a popular choice in power electronics inverters.

2.1.1. H-Bridge Neutral Point Clamped Converter

The H-NPC multilevel inverter topology is based on connecting several H-Bridge NPC converters [7] in series, each with a separate DC source and split capacitors. A typical structure of H-NPC is shown in Fig.2.4. As can be seen from the figure, the output terminals of each H-bridge are connected in series, and the input consists of separate isolated DC sources with DC split capacitors. Apart from the general advantages of a multilevel inverter topology, a cascaded H-bridge multilevel PWM inverter also uses identical units of the H-bridge inverter, thus improving the modularity aspect of the system.

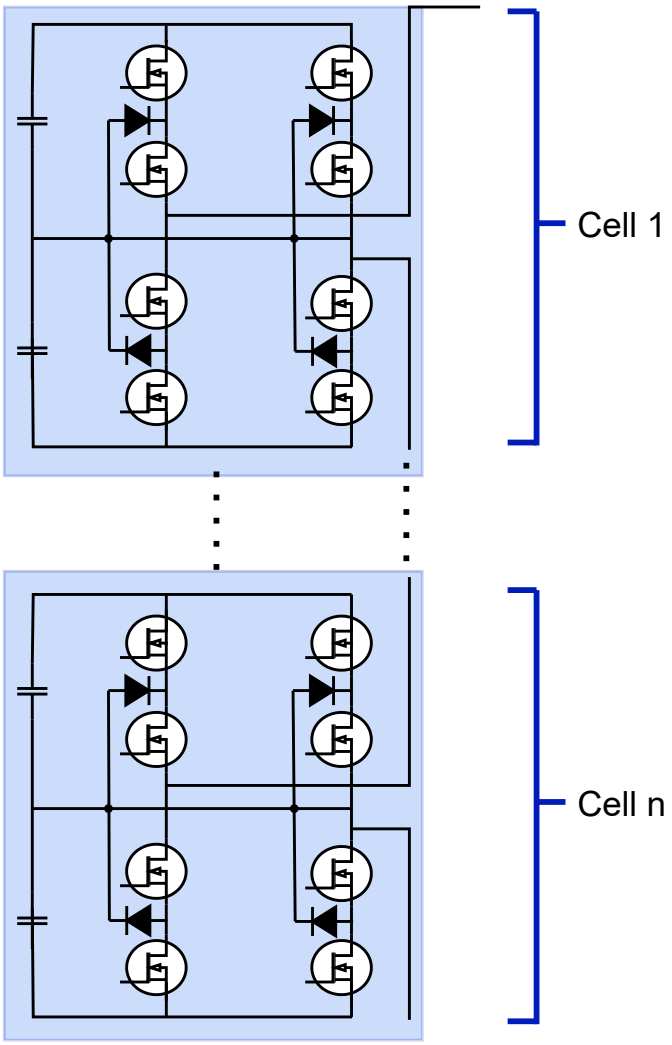


Figure 2.4: Typical H-Bridge Neutral Point Clamped Inverter

The main advantages of the H-NPC topology are:

- Each H-Bridge NPC can output five (+V, +V/2, -V/2, -V and 0) voltage levels. This translates to four times the number of DC voltage sources plus one (4N+1) for total output voltage levels. Here, N is the number of DC voltage sources.
- The switching frequency for each power device is low, reducing the overall switching losses.
- Due to the cascaded structure and split capacitor design, each power switch can be rated only for half the maximum DC source voltage. This also results in a lower dv/dt during each switching event and helps reduce Electromagnetic Interference (EMI).

The disadvantages of the H-NPC topology are:

- The number of components increases largely for every H-bridge and requires split capacitor voltage balancing. This requires a complex control strategy and many PWM pins to drive the power switches.
- High voltage applications require multiple isolated DC sources, which are not always available.

2.1.2. Cascaded H-Bridge

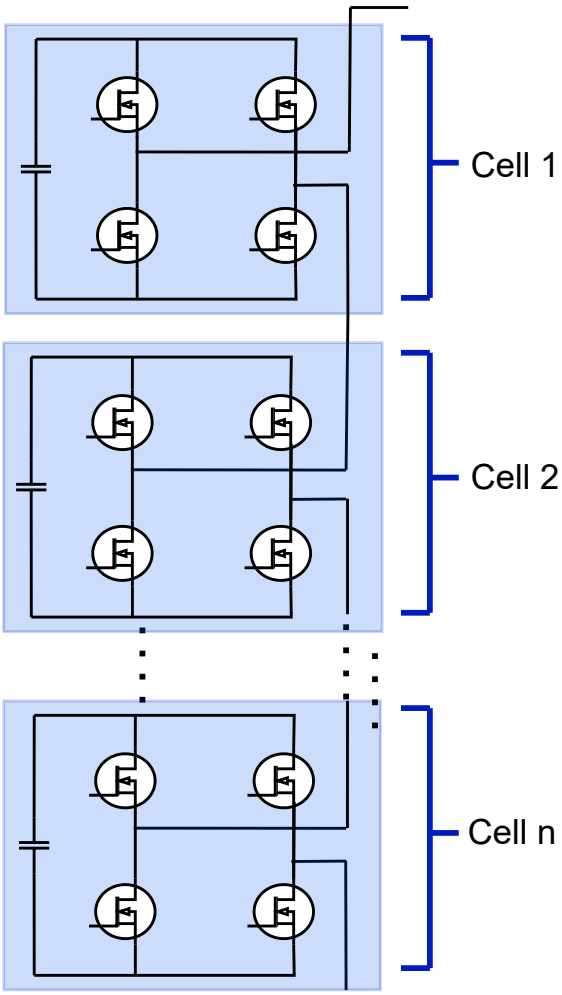


Figure 2.5: Typical Cascaded H-Bridge Inverter

The CHB multilevel inverter topology is based on connecting several H-Bridges in series [6], each with a separate DC source. A typical structure of CHB is shown in Fig.2.5. As shown in the figure, the output terminals of each H-bridge are connected in series, but the input consists of separate isolated DC sources. Like H-NPC, the CHB multilevel PWM inverter also uses identical units of the H-bridge inverter, thus improving the modularity aspect of the design.

The main advantages of the CHB topology are:

- Each H-Bridge can output three (+V, -V and 0) voltage levels. This translates to twice the number of DC voltage sources plus one (2N+1) for total output voltage levels. Here, N is the number of DC voltage sources.
- The switching frequency for each power device is low, reducing the overall switching losses.
- Due to the cascaded structure, each power switch can be rated only for the maximum DC source voltage. This also results in a lower dv/dt during each switching event and helps reduce Electromagnetic Interference (EMI).

The disadvantages of the CHB topology are:

- As the number of voltage levels increase at only a (2*N + 1) rate, several H-Bridges are required in series to achieve a nearly sinusoidal output voltage with minimum THD.
- High voltage applications require multiple isolated DC sources, which are not always available.

2.1.3. Modular Multilevel Converter

An MMC [7] consists of several identical power modules with a parallel link capacitor forming sub-modules which are then connected in series to obtain an AC voltage output. A typical structure of MMC with half-bridge sub-modules is shown in Fig.2.6. The power module operates either to connect or bypass the link capacitor to the other capacitors in the leg. This topology is currently receiving a lot of interest due to the modularity of the design and usage of low-voltage-rated devices.

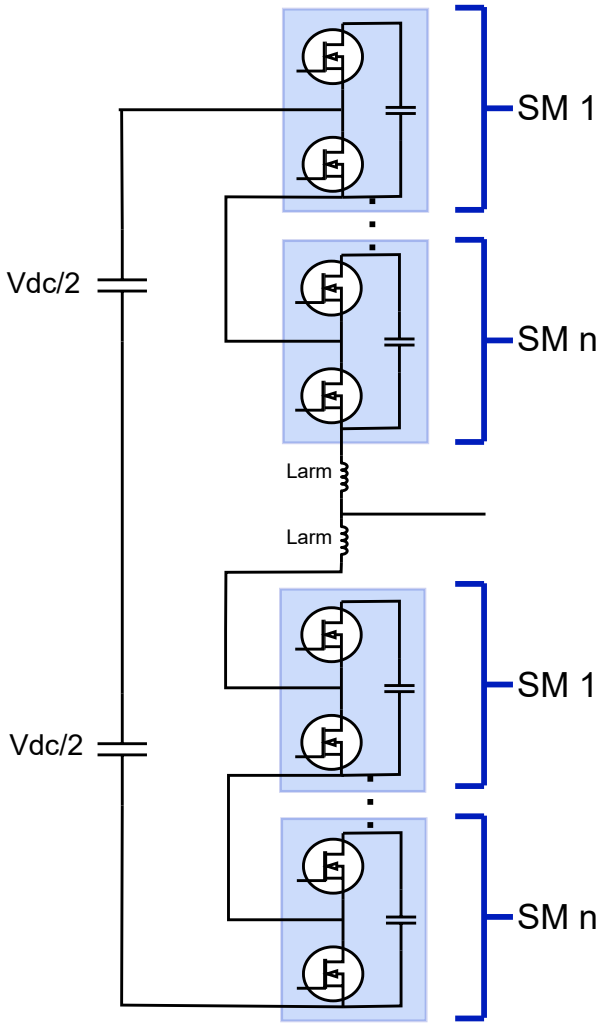


Figure 2.6: Typical MMC Inverter

The main advantages of the MMC topology are:

- MMC is a modular and scalable topology making it feasible for medium voltage applications.
- Due to the number of sub-modules, it requires a small filter size at the output and inherently produces low harmonic content.

- The sub-module capacitors eliminate the need for any high-voltage link capacitors.
- Due to the high number of sub-modules, power quality can be maintained while reducing the switching frequency, thus, reducing the switching losses.

The disadvantages of the MMC topology are:

- The sub-module capacitors must be pre-charged, and the average voltage across all the submodules must be balanced.
- Due to a large number of power devices and capacitors, a complex control circuitry needs to be developed for the converter, which limits the number of levels that can be stacked.

2.1.4. Comparison between Cascaded H-Bridge, Modular Multilevel Converter, and H - Neutral Point Clamped Converter

S. No.	Parameter	Cascaded H-Bridge	Modular Multilevel Converter	H-Neutral Point Clamped Converter
1.	**Modularity**	All cells are identical but requires specific changes in control to add/remove additional cells	Several identical sub-modules can be stacked to achieve different power levels. Each submodule can also be easily replaced in case of fault conditions	All cells are identical but requires specific changes in control to add/remove additional cells
2.	**Efficiency**	High efficiency but requires higher switching frequencies than MMC	Very high efficiency	High efficiency but requires higher switching frequencies than MMC
3.	**Complexity**	Simpler structure with very few components in each cell	Complex structure with added components (sub-module capacitors) and requires highly complex control and voltage balancing circuitry	Complex structure with added components (double the number of switches compared to CHB, diodes and split capacitors) and requires complex control and balancing circuitry
4.	**Cost**	Lower cost due to lower number of components and simpler control requirements	High cost due to added components and complex control requirements	High cost due to added components and complex control requirements
5.	**Voltage Capability**	Can be configured to handle very high voltages	Typically used in medium voltage applications	Can be configured to handle very high voltages

Table 2.3: Comparison - CHB vs. MMC vs. H-NPC

All three topologies have advantages and disadvantages, and the choice between them depends on the specific requirements of the application. The following table shows a common comparison of the three topologies. It can be seen from the comparison in Table 2.3 that the disadvantages outweigh the advantages in the case of H-NPC topology for this specific application; MMCs are more modular and efficient but are more complex and expensive, while CHBs are simpler and less expensive but have a narrower range of voltage capability. Because of the complexity and cost disadvantages inherent to MMC topology, and the inherent drawbacks of H-NPC, it was decided to use CHB topology for this project's DC-AC stage of the SST. The following sections of the report consider CHB topology for the further design process and comparison of modulation strategies.

2.2. Modulation Strategies

For these multilevel converters, a huge challenge is to design and implement appropriate modulation strategies. Traditional modulation techniques are difficult to implement due to increased power switches and limited degrees of freedom. Most multilevel converters require a control design to average the power and losses in each cascaded cell. They also allow the implementation of better-switching patterns to reduce the harmonic content in the output waveform by utilizing the available additional switching states. Several modulation strategies have been developed with advantages/disadvantages for utilizing the maximum potential of multilevel converters depending on specific applications. As explained in [3, 8], a brief categorization is shown in Fig. 2.7.

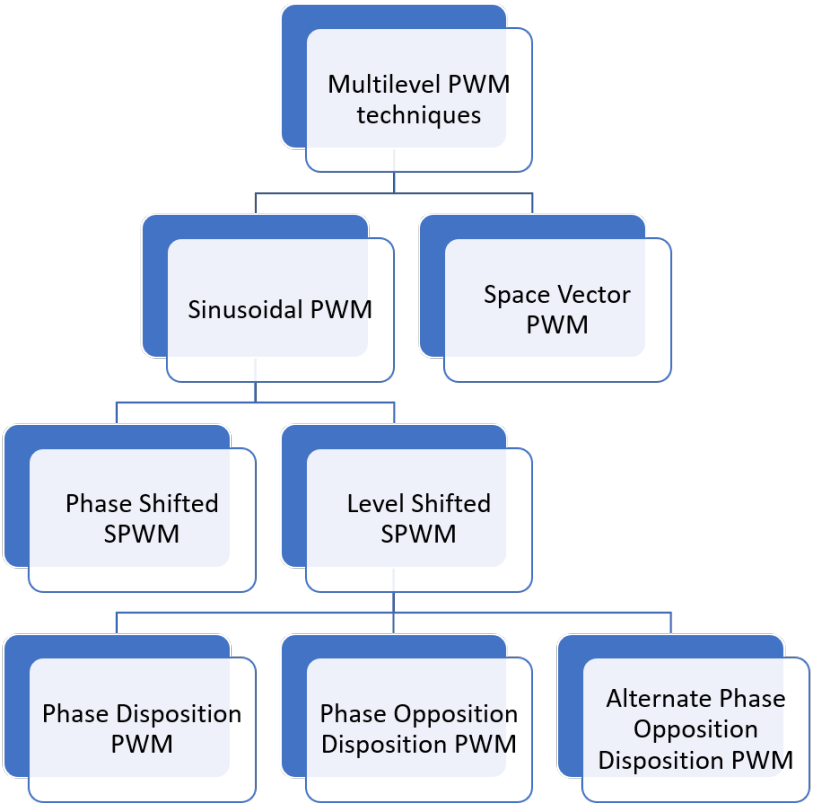


Figure 2.7: Modulation Strategies

This chapter analyzes the approaches for controlling voltage source inverters that have received much attention in recent years. Besides, as demonstrated in [9], the selected switching method to control the inverter will effectively suppress harmonic components while producing

the ideal sinusoidal voltage waveform at the output. Several pulse width modulation methods are used to control voltage source inverters. Some widespread methods are sinusoidal PWM (SPWM) and space vector PWM (SVPWM) techniques. These modulation techniques generate variable frequency and amplitude output voltage in voltage source inverters.

2.2.1. Sinusoidal PWM

Sinusoidal Pulse Width Modulation (SPWM) is a commonly used modulation technique in most power converter designs to regulate the output voltage. It generates a PWM signal with varying widths of the pulse based on the required amplitude of the sine wave. This process can achieve the average output voltage of a converter. SPWM technique requires a reference wave and a carrier wave.

A reference sine wave of desired characteristics such as voltage and frequency is compared with a triangular or saw-tooth switching frequency waveform. The output of this comparator generates pulses known as the PWM signals, which are fed into the gate control pins of the power switches. If the reference wave is higher than the carrier wave, the PWM signal is set to a high state (ON state), and when the reference wave is lower than the carrier wave, the PWM signal is set to a low state (OFF state). Three reference sine waves are used for a three-phase converter; each phase shifted to the other by 120°. A typical SPWM switching operation is shown in Fig. 2.8.

The switching pulses S_a, S_b, and S_c are the upper switches of a typical 3-phase inverter. The bottom switches of each leg of the inverter use complementary signals for their operation. By adjusting the duty cycle or the pulse widths, the effective output voltage of the converter can be controlled. For multilevel inverters, the SPWM technique can be divided into two broad types [10, 11, 12].

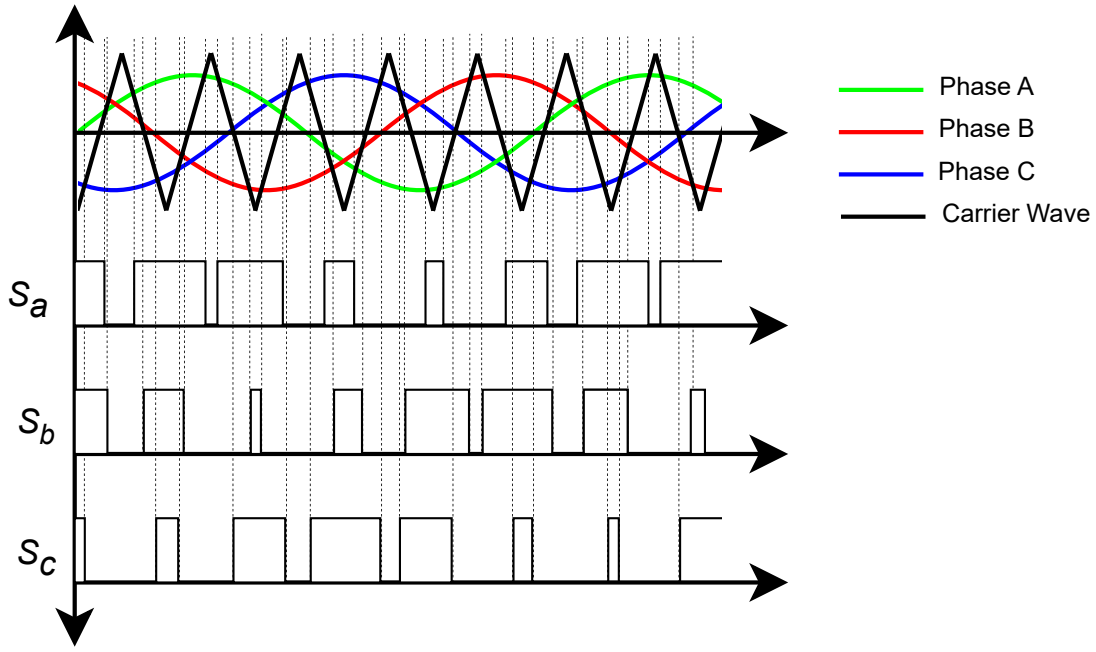


Figure 2.8: Sine PWM Switching Operation

Phase-Shifted SPWM is used in multilevel converters and consists of multiple carrier signals. Each half-bridge is assigned to a single carrier, and all carrier waves are phase shifted with respect to each other. This helps generate a staircase-type waveform following the reference sinusoidal waveform at the output with multiple levels. Also, as each carrier wave is of switching frequency, the switching events in each power switch occur at the carrier frequency. However, the output waveform of the converter has a frequency equal to the product of the number of carriers and switching frequency. This helps reduce the overall size of the output filter and, thus, the complete system. PS SPWM also inherently has the property to distribute the power among all the cells evenly in converters like the CHB. This eliminates the need to implement a power-balancing strategy for the multilevel converter. A typical 5-level PS SPWM waveform and its corresponding switching events [13] are shown in Fig. 2.9.

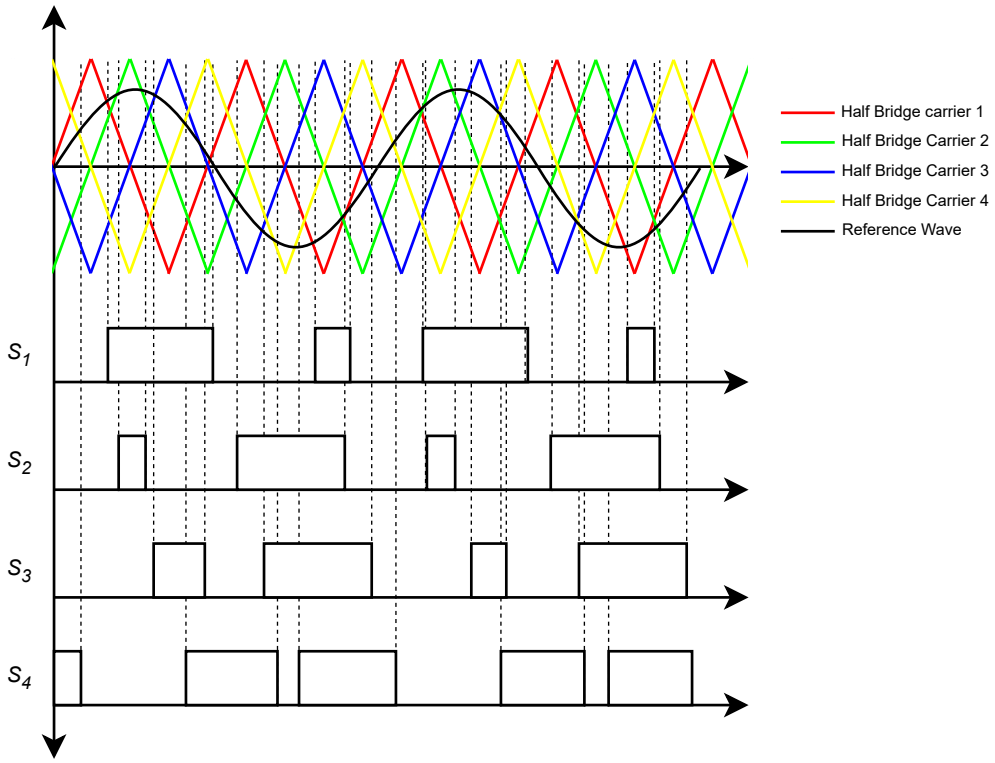


Figure 2.9: Phase-Shifted SPWM Switching Operation

Level-Shifted SPWM is also used in multilevel converters and consists of multiple carrier signals representing the possible voltage levels of the converter. Each half-bridge is assigned to a single carrier, and all carrier waves are level-shifted with respect to each other vertically. However, each carrier is of the same magnitude. This method also generates a staircase-type waveform at the output with multiple levels. However, as each carrier wave is of switching frequency and is vertically stacked, the output waveform of the converter has a frequency equal to the switching frequency. The LS-PWM method can result in lower harmonic content [14] but not by a huge margin compared to PS SPWM. LS SPWM inherently does not have the property to distribute the power among all the cells evenly in converters like the CHB [15]. Therefore, it requires implementing a power-balancing strategy for the multilevel converter. A typical 5-level LS SPWM waveform and its corresponding switching events are shown in Fig. 2.10.

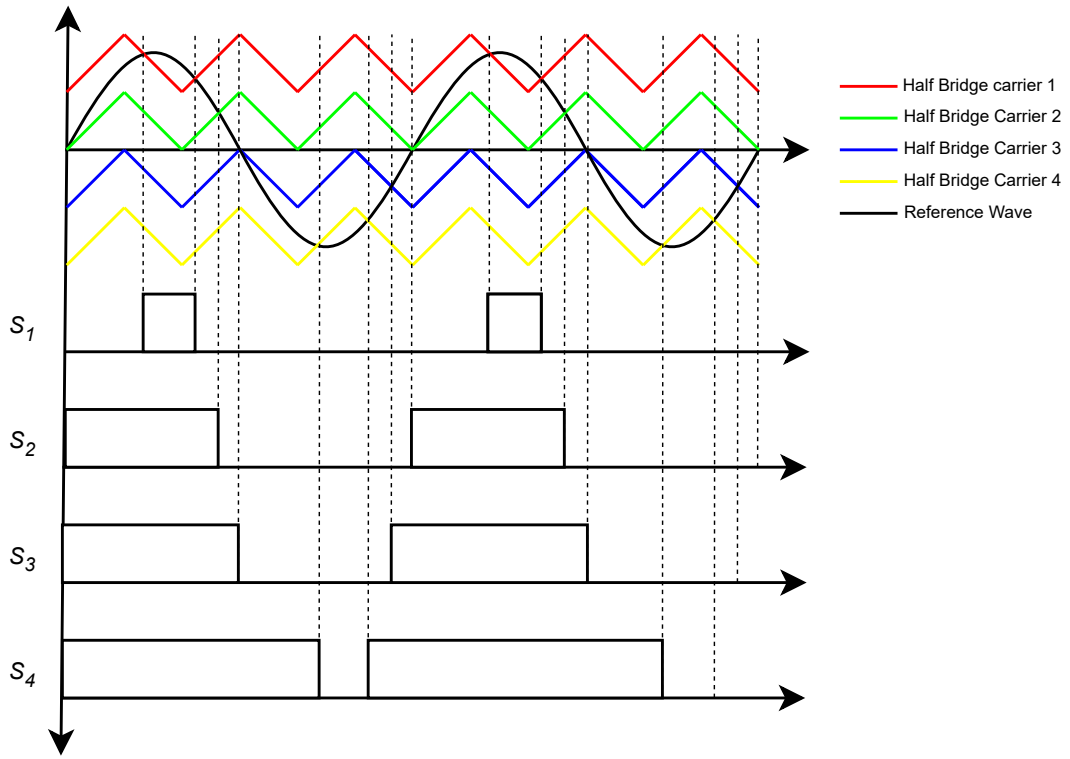


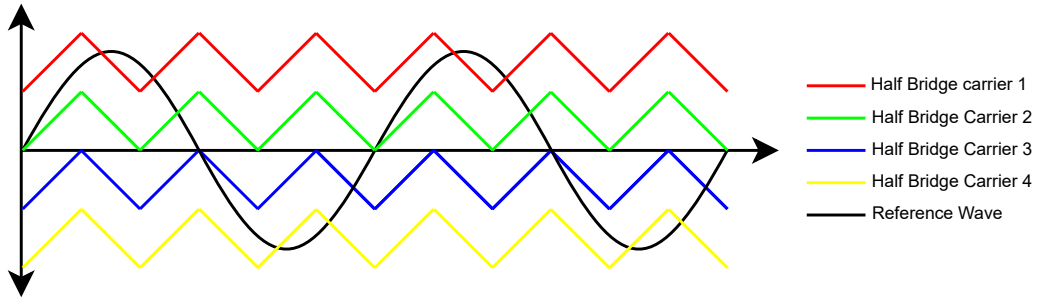
Figure 2.10: Level-Shifted SPWM Switching Operation

Based on the phase differences of the level-shifted carriers, this method can be further classified as:

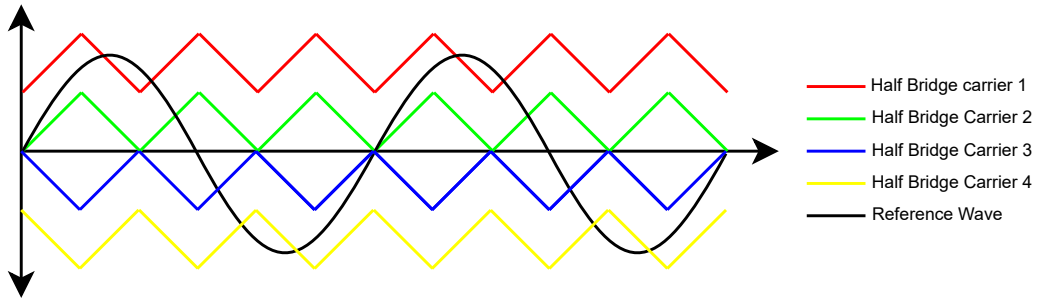
1. *Phase Disposition PWM (PD-PWM):* In this method, all the carriers of the converter are in phase and vertically shifted, as shown in Fig.2.11(a).

2. *Phase Opposition Disposition PWM (POD-PWM):* In this method, all the positive carriers of the converter are in phase and vertically shifted. All negative carriers are in phase and vertically shifted, but the positive and negative carriers are 180°phase shifted with each other as shown in Fig.2.11(b).

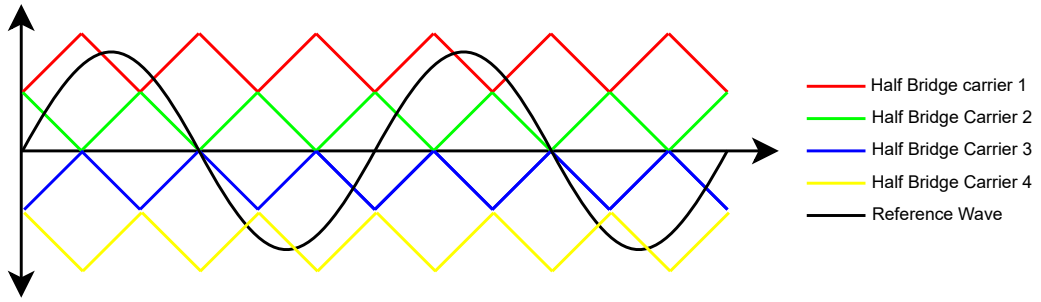
3. *Alternate Phase Opposition Disposition PWM (APOD-PWM):* In this method, each of the carriers of the converter is 180°phase shifted to the next carrier, and all carriers are again vertically shifted as shown in Fig.2.11(c).



(a) Phase Disposition SPWM



(b) Phase Opposition Disposition SPWM



(c) Alternate Phase Opposition Disposition SPWM

Figure 2.11: Types of Level-Shifted SPWM

2.2.2. Space Vector PWM

Space Vector Pulse Width Modulation (SVPWM) is a more complex modulation technique used in three-phase systems to generate output voltage waveform for a modulation index greater than one ($m > 1$). It is therefore considered to provide an improved DC voltage bus utilization and reduce the harmonic content [9] compared to the above-discussed sinusoidal PWM techniques. However, to achieve this high performance, SVPWM required complex calculations and higher computing power in the case of multilevel converters.

To understand the working of SVPWM in power electronics converters [13, 16], we take the example of a three-phase three-level inverter. The space vector diagram for this converter is shown in Fig.2.12 with the position of the reference vector and all the switching states in α - β frame:

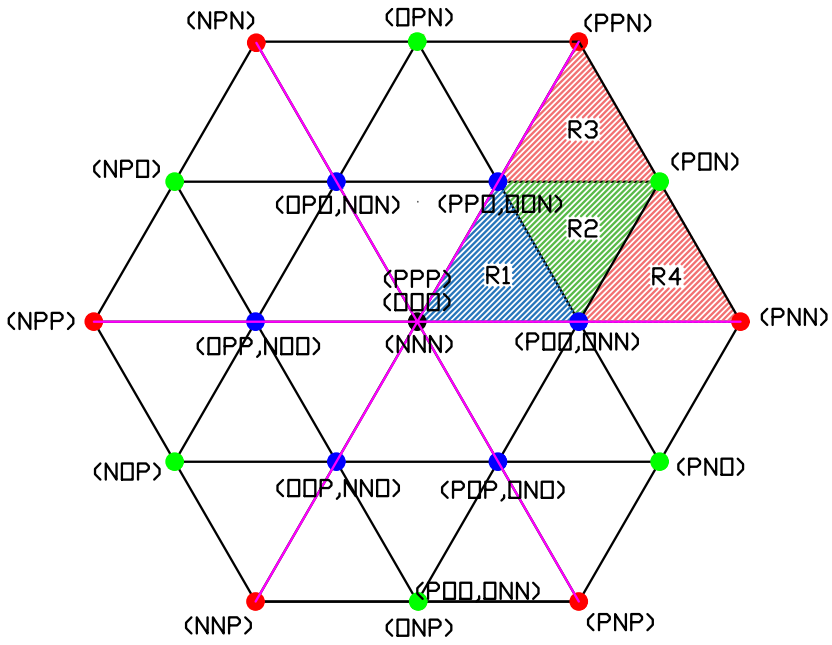


Figure 2.12: Space Vector Representation of three-phase three-level converter

1. First, the three-phase values of voltages and currents are transformed using Clark transformation from the standard abc stationary reference frame to a rotating reference frame. This is also called the stationary α - β frame or the synchronous $d-q$ frame.
2. The reference vector represents the required amplitude and phase of the output on the α - β frame. This reference vector sweeps through the area of the hexagon created by the first step representing all possible voltage magnitude and phase values.
3. Based on the position of the reference vector, the sector of that position is determined. The complete hexagon is divided into multiple triangles called 'sectors,' representing the nearest three switching states.
4. Then, based on the position of the reference vector inside the sector, the time duration for each of the nearest three switching states is calculated using simple geometry. There are several ways to realize multiple switching states at the same position. A few are designed to reduce the switching events, while others help reduce the common-mode voltage.
5. The switching states are realized by providing the gating pulses to the power switches for the calculated times to generate the desired waveform.

It can be observed that the number of switching states of the 'n' level multilevel converter is equal to 'n^3' with increasing redundant switching states as the levels increase. This problem makes SVPWM a less popular choice [17] in higher-level converters.

2.2.3. Comparison between Sinusoidal PWM and Space Vector PWM

As explained above, space vector pulse width modulation (SVPWM) and sine pulse width modulation (SPWM) are the common modulation techniques for inverters in power electronic applications. Both techniques have advantages and disadvantages, and their choice depends on the specific requirements of the application [9, 18]. Here is a final comparison of the two techniques:

S.No.	Parameter	Space Vector PWM	Sinusoidal PWM
1.	Complexity	Difficult to implement, requires complex algorithms to optimize switching pattern	Simpler technique with lesser calculations
2.	Harmonic Content	More precise control results in lower harmonic content in the output voltage	Produces more harmonic content than SVPWM
3.	Efficiency	By optimizing the switching pattern, it minimizes the number of switching transitions and helps increase the overall efficiency	Results in more switching transitions which results in more losses and reduced efficiency
4.	Output Voltage Quality	Controls the magnitude and phase of output voltage precisely resulting in fewer distortions and a smoother waveform	Generates a sinusoidal waveform of fixed-frequency, resulting in more distortions in the output waveform
5.	Implementation	Uses digital signal processing with complex algorithms, which requires a digital controller	Can be implemented using simpler analog circuits which are cost-effective

Table 2.4: Comparison - Space vector PWM vs. Sinusoidal PWM

Overall, both SVPWM and SPWM are viable options for modulation in power electronic inverters, and the choice between them depends on the specific requirements of the application. SVPWM offers better efficiency, lower harmonic distortion, and better output voltage quality but is more complex and requires digital implementation. SPWM is simpler, more cost-effective, and suitable for analog implementation but has higher harmonic distortion and lower output voltage quality.

Considering all the above-mentioned advantages, SVPWM offers, it seems to be the ideal modulation strategy for grid-connected inverter applications. However, on further research into the application of SVPWM on multilevel converters, it was discovered that the computational power requirement increases largely with the number of levels of the converter. This demands a smart, modular algorithm to implement SVPWM to make it feasible for such applications. This research and developed algorithm aspect are explained in detail in Chapter 4.

2.3. Dead time effect on output waveform

Dead time refers to the time period between switching intervals where both the top and bottom switches of a half-bridge are turned off. This is required to account for the finite turn-on and turn-off times inherent to any power switch in power converters. This helps avoid a shoot-through current through the converter, thereby protecting the power devices and the converter. The value for this blanking time depends on the type of switch used in the converter. Providing dead time is necessary for the input gating signals for over-current protection. However, introducing this period in the gate signals leads to distortions in the output voltage and current waveforms [19].

To understand this phenomenon better, we consider a full bridge inverter as shown in 2.13.

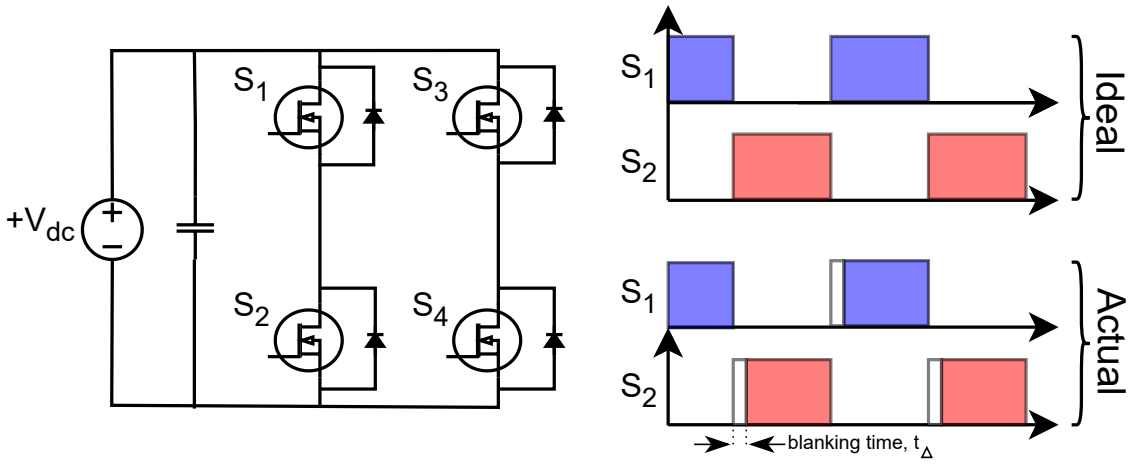


Figure 2.13: Full-bridge converter with ideal and actual switching signals

The effect of dead time can be divided into two cases, one with a positive output current and the other with a negative current. The output current direction is positive when switches S_1 and S_4 are in on-state and conducting current. At the end of this state, both switches are turned off, and the current flows through D_2 and D_3 before the switches S_2 and S_3 turn on, and then the current direction is reversed. This delay caused by the dead time reduces the output voltage amplitude as the duty cycle is effectively reduced.

Similarly, while transitioning from a negative to a positive current state, the dead time reduces the output voltage magnitude. This difference causes an undesired shift in output voltage waveform at the transition point in the current direction. This effect is shown in Fig.2.14.

Research conducted by [20, 21, 22] developed potential solutions to mitigate the effect of dead time in inverters. A few papers suggest solutions that dynamically decrease the dead time to a minimum value every switching cycle by accurately measuring the states of the power switches. However, the most common solution requires external analog circuitry and the control circuit. They require a high-frequency detector to detect the zero-crossing time instant of the current waveform. Further investigation is needed to develop these circuits and is not included in the scope of this thesis project. Instead, a safe value of dead time is included in all the simulations and design processes, and other system parameters are designed accordingly, as explained in the next section.

However, using a constant dead time in an inverter design restricts the maximum switching frequency, as demonstrated in [19]. This is because, for a smaller switching period, the ratio of dead time to on-time of a power switch is higher than for a larger switching period. This causes higher distortions in the waveform, making the output filter size difficult to realize.

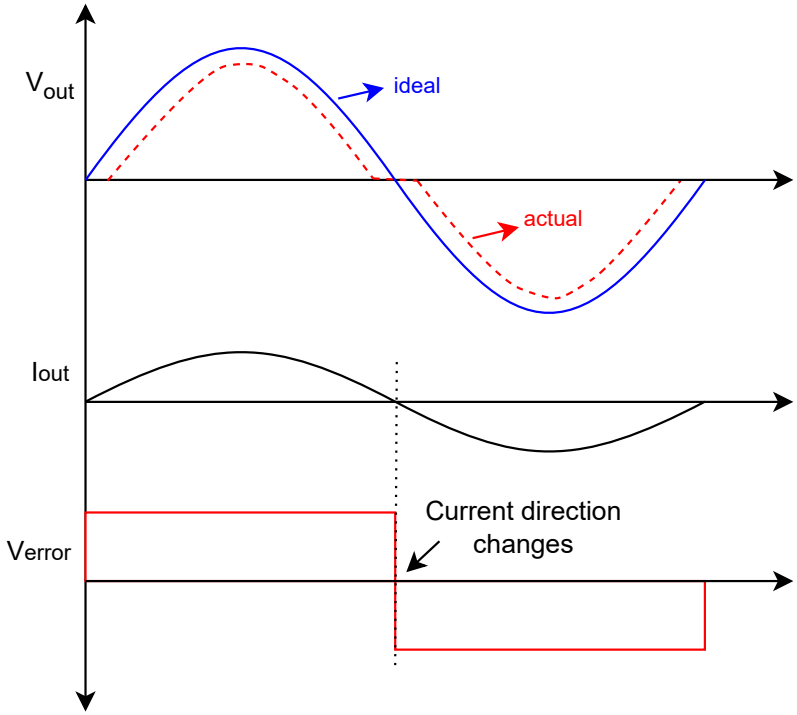


Figure 2.14: Distortion caused by dead-time in the output voltage waveform

2.4. Total Harmonic Distortion (THD) and Output Filter

Total Harmonic Distortion (THD) is a significant parameter to determine the output quality of a power electronic inverter. It represents the total harmonic content in the output voltage and current waveforms. Higher THD translates to lower power quality, increased losses, and possible interference with other systems connected to the grid. Therefore, lowering the THD content as much as possible is important. In grid-tied inverters, there exist standards that define the maximum allowable percentage of harmonics to that of the fundamental frequency.

Several aspects of an inverter influence the overall THD content. These include the switching frequency, modulation techniques, and the capability of the output filter to attenuate the harmonics. As explained in the previous section, including dead time in the models restricts the maximum possible switching frequency. Therefore, the output filter design and modulation techniques determine the harmonic content in the output voltage waveform. Various modulation techniques and their advantages are already discussed earlier. The results from simulations to compare the effectiveness of these modulation techniques will be discussed in 4.

An output filter is required to prevent injecting the harmonic distortion and any disturbance generated by the inverter into the grid, which is required to maintain high power quality. There are three common topologies used as output filters as discussed in [23] for power electronic inverters:

1. **L Filter -** An L filter typically uses an inductor placed in series with the inverter output. This type of filter is used to reduce the current ripple, provide high attenuation to high switching frequency components from the inverter, and allow the low-frequency fundamental component to pass through. L filter attenuates the harmonics with a -

20dB/decade roll-off rate.

2. **LC Filter -** An LC filter typically uses an inductor placed in series and a capacitor in parallel with the load at the output of an inverter. This type of filter provides higher attenuation to high switching frequency components, both L and C. The capacitor also provides a high impedance to the fundamental frequency component to improve the power factor. LC filter attenuates the harmonics with a -40dB/decade roll-off rate.

3. **LCL Filter -** A T network LCL filter typically uses two inductors placed in series and a capacitor between them at the output of an inverter. This type of filter provides the highest attenuation to switching harmonic components from the inverter, and the capacitor provides further filtering and power factor correction. LCL filter attenuates the harmonics with a -60dB/decade roll-off rate.

The decision to select a filter depends on the specific requirement of the application. L filters are simple and cost-effective but provide minimal harmonic attenuation. On the other hand, LCL filters are expensive and more complex to design but provide the best performance to maintain high power quality.

2.5. Summary

This chapter discussed the research and literature studied for the inverter design process. Several papers and notes are compared, discussed, and documented to understand the design parameters. The chapter begins by emphasizing the need for multilevel converters, the most popular multilevel topologies for inverter applications, and compares them to several parameters. Then, the significance of using the right modulation techniques for a power electronic converter and the requirements for a multilevel converter is discussed. Sinusoidal PWM and Space Vector PWM are introduced and compared for advantages and drawbacks while focusing on multilevel converter topologies.

The chapter also introduced concepts including dead time, switching frequency, THD, and output filter selection for an inverter. Each of these concepts is briefly discussed for a power electronic converter. Understanding these concepts is significant to follow the design process of the inverter stage explained in Chapter 4.

3

System Controller Architecture

In multilevel power converters, the controller architecture plays an important role in the overall system design. The controller architecture has to be flexible and modular to ensure system scalability. In general, it refers to controllers' overall layout and data transfer between them to ensure the ideal operation of the converter. As described in [24], two typical controller architectures are used for power converters: centralized controller architecture and distributed controller architecture. Each architecture has advantages and drawbacks, making selecting one design for all applications challenging. Therefore, an in-depth understanding of the specific system is required, along with research into both designs to employ a particular design for the system.

The following sections explain both architectures with specific implementations needed to properly control a multilevel converter, such as a modular SST. Communication protocols are the next most important aspect of control architecture design. Therefore, several available protocols are proposed in this chapter. The synchronization problem in distributed controller architecture design is addressed, and ways to mitigate this effect are discussed. The chapter concludes with a summary of all the challenges addressed and proposed solutions for the complete system and the initial prototype.

3.1. Central Controller Architecture

The central controller architecture uses a single controller, which is responsible for all the control tasks of the complete system. It is required to monitor and control all the cells. This includes receiving feedback signals from all the sensors distributed across the system, processing this information, and generating the required control and gating signals for all the power devices. However, this design is impractical at higher-level converters due to a large number of power devices and sensors requiring huge computational capability [25] in the controller. A few advantages and disadvantages of this type of architecture are explained below:

Advantages of Central Controller Architecture

- Enables a coordinated control of the entire system by using a single controller
- Helps optimize the system-level control algorithms by not causing any communication delays
- Eliminates the need for high bandwidth communication line requirements

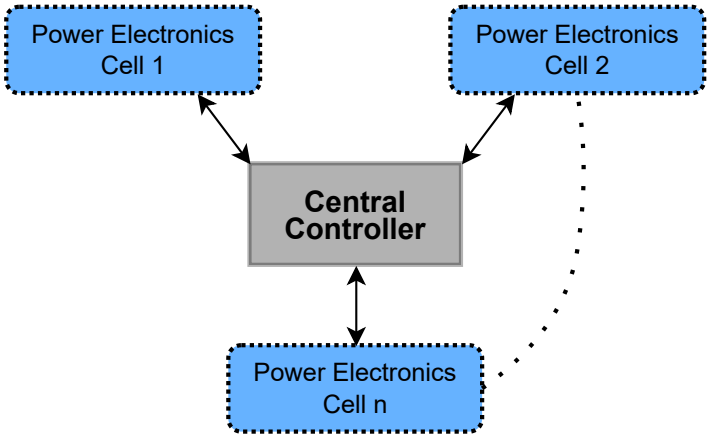


Figure 3.1: Central Controller Architecture

Disadvantages of Central Controller Architecture

- Difficult to implement as the control logic is very complex
- Very expensive as a very powerful central controller needs to be used with high computational power
- Single point of failure as the complete system is shut down in the event of any fault with the central controller
- Restricts the modularity and scalability aspect of the system by the limited hardware

3.2. Distributed Controller Architecture

The distributed controller architecture uses multiple controllers distributed across the system, where each one is responsible for managing the control tasks of only a specific part of the system. Each controller is required to monitor and control a specific cell. This includes receiving feedback signals from the sensors that are part of the specific cell, processing the information, and generating the required control and gating signals for the power devices of that cell. Apart from these tasks, it must send/receive the required data to the neighboring controllers for system-level operation [25]. However, this requires a robust communication network [26] connecting all the cell-level controllers. This design is ideal for higher-level converters as the computational requirement of each controller remains identical. This type of architecture requires precise coordination with other controllers in the system to ensure smooth operation. A few advantages and disadvantages of this type of architecture [27] are explained below:

Advantages of Distributed Controller Architecture

- Reduces the control complexity of each local controller
- The fault handling capability/redundancy of the system is increased as the failure of one local controller does not affect the complete system
- As each controller handles only a specific part of the system, less computational power is required, which translates into less expensive hardware

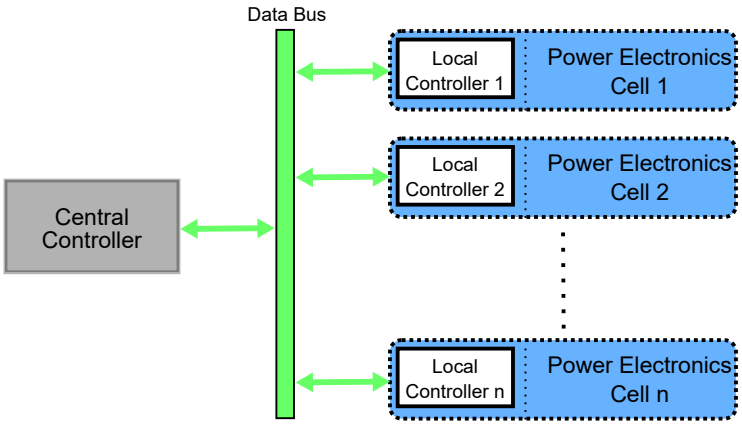


Figure 3.2: Distributed Controller Architecture

Disadvantages of Distributed Controller Architecture

- Coordinating all the local controllers is a huge challenge in terms of synchronizing the gating pulses and data
- Optimization of system dynamics is more challenging as local controllers have access to limited data

As seen from the above comparison, the selection between the two architectures [8] depends largely on the specific requirements and constraints of the application. A careful analysis must be performed as both have different advantages and drawbacks.

3.3. Communication Protocols

Traditional converters consist of a central controller, and all the voltage and current measurements are sensed and processed by it. This type of system requires a customizable hardware interface for specific applications. This type of system loses its modularity and scalability. Modern converters incorporate several local controllers for each building block, and a system-level controller communicates with all the local controllers.

Figure 3.3: Requirements in a communication protocol

Such distributed systems require a robust, synchronous communication system [28] to communicate efficiently with all the controllers. In the case of power converters, the output voltage quality is greatly influenced by the accuracy of this synchronization. Modular converters have a control period as low as 10 microseconds with switching frequencies in the order of tens

of kilohertz. A fast communication protocol must be employed to enable such high speeds for data transfer. High accuracy and low latency are among the key requirements [24] of the selected communication protocol.

Due to the above-mentioned synchronization requirements, non-real-time communication protocols such as Ethernet cannot be considered. There are several potential communication protocols for power converters applications. The most widely used protocols include EtherCAT, SPI, and CAN. The following sections investigate these three communication protocols and compare their advantages and disadvantages.

3.3.1. EtherCAT

EtherCAT has received particular attention among the protocols mentioned due to its high communication speed and scalability. This protocol is highly used in industrial automation and large companies. It is a real-time Ethernet-based field bus system with an extremely low synchronization jitter of less than 1μs. Apart from these advantages, EtherCAT includes an in-built synchronization technique called ”Distributed Clocks,” explained in detail in the following sections, which is extremely efficient and helps achieve very high accuracy of the control system.

Working Principle

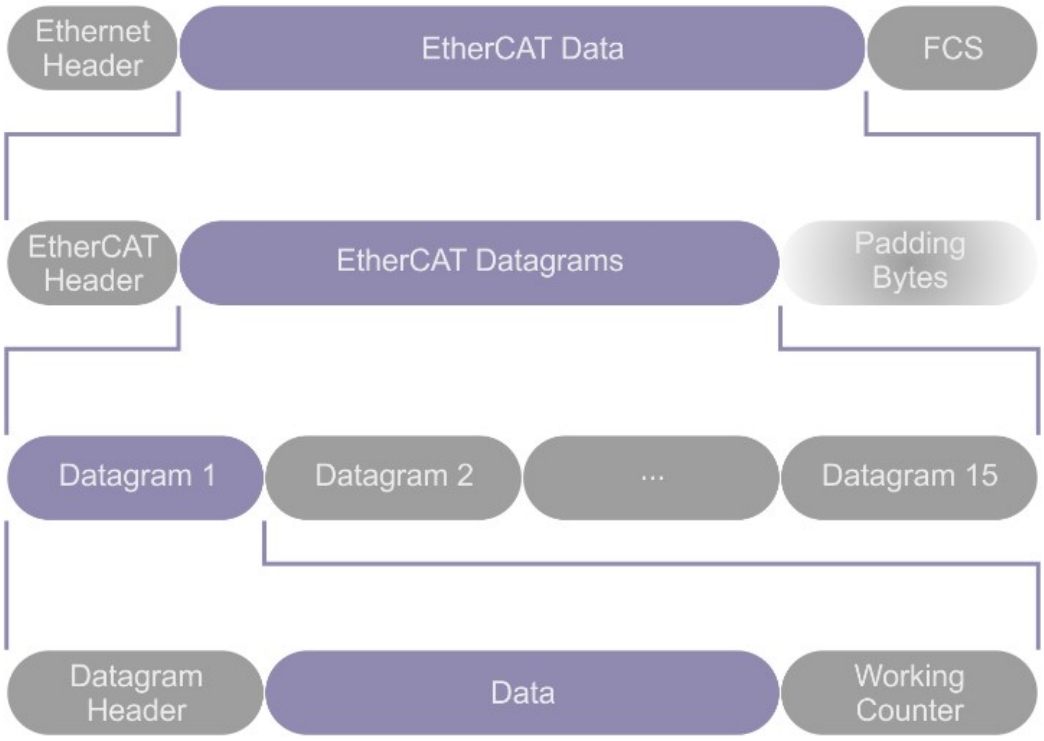


Figure 3.4: EtherCAT Telegram [29]

To understand the basic operation principle [28] of EtherCAT, it is important to understand the standard Ethernet frame, as the EtherCAT datagram is encapsulated in an Ethernet frame. EtherCAT uses a master-slave configuration to transfer data [30, 31] where only the master can initiate the communication. The EtherCAT master sends a telegram that travels through

each of the slave controllers. The data addressed to the slave is read ”on the fly,” and information is added to the frame as it travels to the next node. Unlike other protocols, the slaves do not copy the entire frame and forward it to the next node. This reduces any processing delays in the slave controllers and, thus, increases the effective data rate. The last slave controller sends the frame back to the master using the full-duplex feature of EtherCAT.

The above Fig. 3.4 shows the complete EtherCAT telegram, which consists of the EtherCAT datagrams and headers. Up to 15 datagrams can be included in one telegram. EtherCAT allows for complete flexibility with the topology, such as line, star, tree, or daisy chain. Along with these topologies, another useful feature is the use of ring topology in redundancy mode. This means the master can manage two ports and use the second port in case of a fault in the first one. It can connect to up to 65,535 devices using these topologies, making it suitable for modular power converters. Also, EtherCAT enables the data exchange between the master and slaves from 1 bit to 60k bytes.

Synchronization using Distributed Clocks (DC)

In power converters, highly precise synchronization is required between all the nodes. The most common synchronous communication methods face quality issues due to communication errors. EtherCAT overcomes these issues using synchronized distributed clocks as they have a high degree of jitter tolerance, explained in [24]. This technique is completely hardware-based and compensates for any propagation delays in the system as well.

The distributed clocks system distributes the exact time from the first slave controller to all the other controllers connected to the bus while incorporating the specific propagation delays for each node. This ensures that all the slave nodes are referenced to a single reference clock resulting in a jitter of less than 1μs. The synchronization method can be divided into two steps to understand this process clearly. The first step is the propagation delay measurement, and the second is the offset compensation of the slave’s internal clock to the reference clock.

Propagation delay: During this process, the master controller sends a data packet to the slave controllers. Each slave adds the timestamp of receiving this data packet and forwards it to the next slave. This also adds a processing time, t_p. The last slave on the bus repeats this process and sends it back to the master through all the slaves. This process adds a forwarding time, t_f, in each of the slaves. If these are assumed to be constant for all the slaves and the propagation delay, t_{prop} on the forward and return path for each of the adjacent slaves to be the same, we can calculate the propagation delay between each of the adjacent slave controllers.

As it can be seen in the Fig. 3.5, the propagation delay between slaves 1 and 2 can be measured as:

$$t_{delay,1-2} = \frac{1}{2}(t_{s,1} - t_{s,2}) + \frac{1}{2}(t_p - t_f) \tag{3.1}$$

The same process can be used to calculate the propagation delays between any two slave nodes connected to the bus.

Offset compensation: Using the calculated propagation delays from step one, an offset can be added to each node’s internal clocks to adjust their local time to the reference slave node’s

internal time. This process enables all the nodes to be synchronized within 1μs of each other. This task can be performed at the start of the network or regular intervals during the system's continuous operation, which also resolves synchronization issues caused due to any drift in the clock oscillators over time.

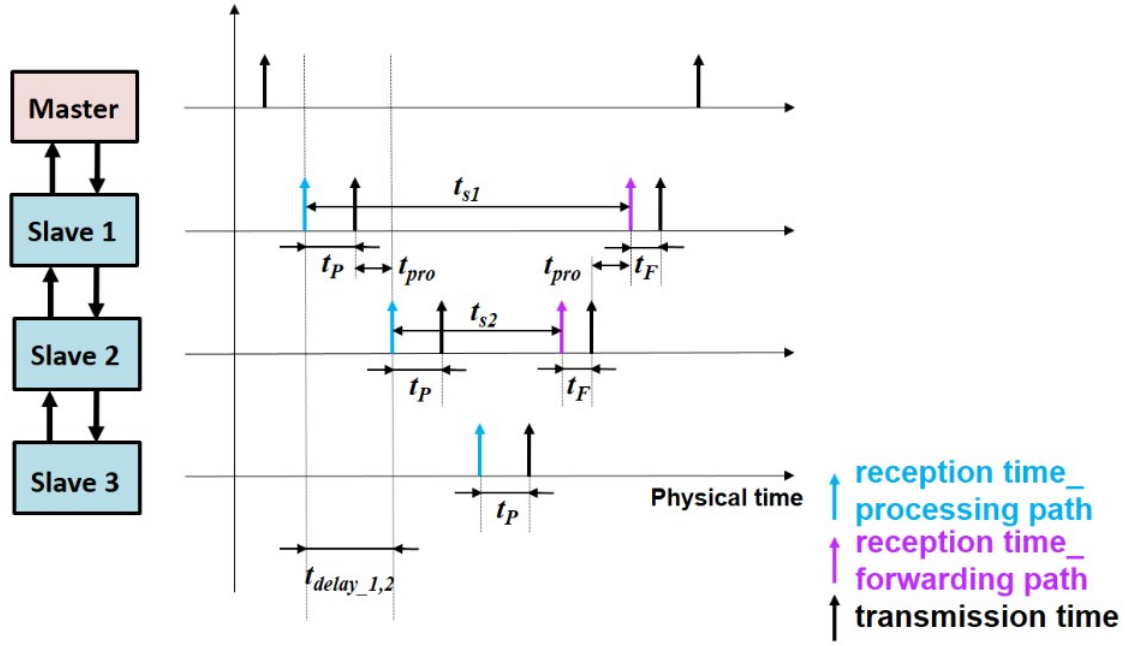


Figure 3.5: Propagation Delay Calculation in EtherCAT [24]

3.3.2. Serial Peripheral Interface (SPI)

SPI is a synchronous board-level communication that works on a shared clock line for synchronization. It is typically used in systems with operating bit transfer rates in the order of megahertz. SPI, by default, operates as a full-duplex protocol, meaning it can simultaneously send/receive data. This feature enables high transfer rates between the devices. Typically, the devices are configured into a master-slave configuration in an SPI bus. However, SPI requires more signal lines (typically a four-wire configuration but can also function in a three-wire configuration). SPI does not have a standard message protocol for communication. Often, the user defines their application-level protocols over the basic SPI protocol.

SPI is a short-distance communication protocol and is designed to operate for onboard applications. However, through optic fibers, SPI can be extended to longer distances, making it possible to be used in distributed controller architecture [28]. The use of optic fibers also helps in providing galvanic isolation to all communication lines. This design limits the final communication speed of SPI due to the limited speed of optic transceivers.

Working Principle

Standard SPI communication works with four signal lines, namely: MOSI (Master Out - Slave In), MISO (Master In - Slave Out), SCLK (Serial Clock), and the CS/SS (Chip/Slave Select). In a multi-slave connection, all the lines except the CS line are shared among all the controllers. The MOSI line transmits data from the master to the slave nodes, and the MISO line transmits data from the slave to the master nodes. The most important aspect of SPI is that the data stream can be sent without interruption, as there is no concept of data packets that limit the

number of bits. Instead, one bit of data is transferred for every clock signal.

Daisy Chain: When multiple slave configuration is used, the master controller requires multiple slave select pins to connect to all the slave controllers. However, if only one slave select pin is available, SPI allows for the slaves to be connected in a daisy-chained topology.

This feature highly makes SPI a suitable communication protocol for modular power electronic converters by not compromising scalability. An example of a daisy-chain SPI system with three slave nodes is shown below in Fig.3.6.

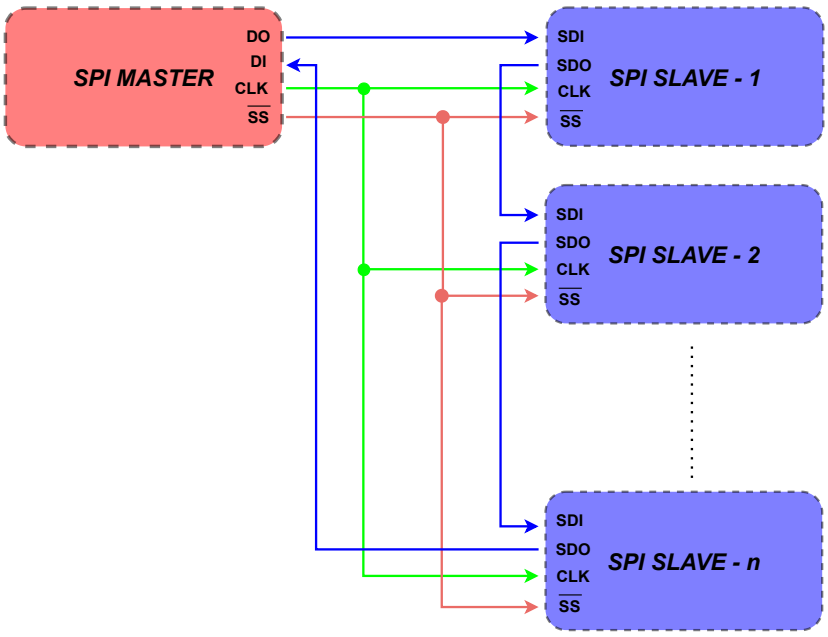


Figure 3.6: Daisy-Chain SPI Configuration

As seen in the figure, the MOSI line (commonly called SDO) of slave one is connected to the MISO line (commonly called SDI) of slave two, and so on. The clock and slave select pins are connected to all the slave nodes from the master. However, in this configuration, that data takes longer to reach the chain's lower nodes. This can be visualized as it takes six clock pulses in a 2-bit system for the data to reach the third slave node compared to two clock pulses to reach the first slave node.

Here is an example of the data transfer in a 2-bit daisy-chained system. A 2-bit system implies the use of controllers with 2-bit registers. The master initiates the communication by pulling the active low CS pin. The data from the shift register of the master is transferred to slave 1. Similarly, data from slave 1's shift register is transferred to slave 2, and so on. At the end of 6 clock cycles, all three slaves will contain the 6 bits of data, 2 bits of data in each slave, from the master, who will have six bits of data from all three slaves. At this point, the master pulls the CS pin high, executing the data in all the controllers.

SPI daisy-chained devices consist of *tx* and *rx* buffers apart from the shift registers. The slaves can now add data into the shift registers for the next transfer of the data cycle. This process is demonstrated in the figure.

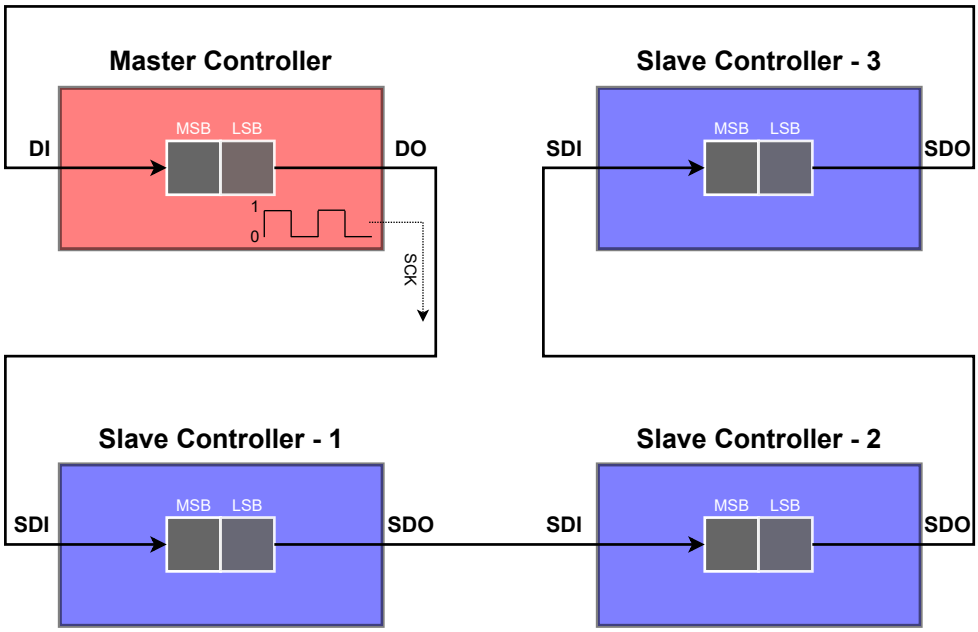


Figure 3.7: Daisy-Chain SPI data transfer in a 2-bit system

3.3.3. Controller Area Network (CAN)

CAN bus is a high-integrity communication protocol commonly used in automotive and industrial systems [32]. CAN provides a reliable bus system that enables serial communication between multiple devices. CAN bus offers data rates from 125 kbps to 1 Mbps with the standard 11-bit and extended 29-bit identifiers. Special versions of CAN, such as *CAN FD*, offer flexible data rates from 0 to 64 bytes per frame and bit rates up to 2 or even 5 Mbps.

Working Principle

It operates as a multi-master broadcast system, sending short messages to every node on the bus. The node can then determine if the message is relevant or not. The CAN-bus uses a two-wire differential pair(CANH and CANL) for communication between nodes. Differential signals allow for higher immunity against external influences such as high-voltage wiring, noise, etc. The bit fields of a standard CAN frame with their explanation are shown below:

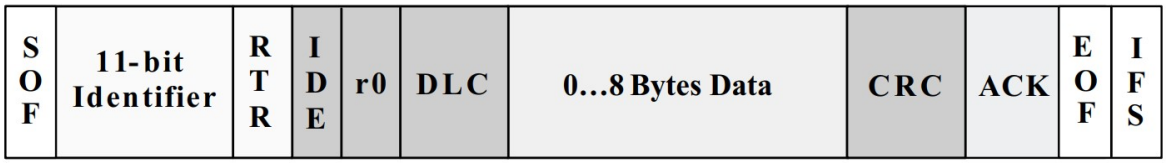


Figure 3.8: Standard 11-bit CAN [33]

- *SOF* - This bit synchronizes all the nodes on a bus after being idle and denotes the start of a message (SOF - Start Of Frame).

- *11-bit identifier* - This field sets the message's priority. 2^{11} = 2048 different messages can be sent using this 11-bit identifier. In CAN bus communication, each message consists of an identifier field. The message with a higher priority (lower binary value of the

identifier field) identifier gets access to the bus.

- *RTR* - This bit is used to specify the requirement of information from another node on the bus (RTR - Remote Transmission Request).

- *IDE* - This field is used to inform all the other nodes on the bus that only a standard CAN frame is being transmitted without any additional extensions to it (IDE - Identifier Extension).

- *r0* - A reserved bit.

- *DLC* - This field is used to specify the total length of the data being transmitted in that frame to all other nodes (DLC - Data Length Code).

- *Data* - The actual data to be transmitted is added to this field.

- *CRC* - This field is used for error detection using checksum, which denotes the number of bits being transmitted (CRC - Cyclic Redundancy Check).

- *ACK* - A standard CAN message frame includes an acknowledgment bit to ensure the transfer of an error-free message. This bit is updated by the receiving node on receiving an error-free message. Otherwise, the message is sent again, and the original corrupt message is discarded (ACK - Acknowledgement)

- *EOF* - It denotes the end of a message (EOF - End Of Frame).

- *IFS* - This field is used to pass enough time before another frame is sent on the bus for the node to receive the message into its buffer register completely (IFS - Inter Frame Space).

Similar to the above message structure, another type of CAN frame with a 29-bit identifier, known as extended CAN, can be used, which increases the total number of messages to approximately 537 million. CAN communication allows for both formats to exist on the same bus. As seen from the working principle, CAN communication helps eliminate any errors in the messages and ensures the high integrity of the data.

3.3.4. Comparison between EtherCAT, SPI, and CAN

Each of the above-discussed communication protocols offers several advantages, which makes them popular for various applications. To compare and select the right protocol for a specific application, as in the case of this project of a modular power converter, a comparison study of various features of these three protocols is required. This comparison is shown below in Table.3.1.

S. No.	Parameter	EtherCAT	SPI	CAN
1.	**Data rate**	Up to 100 Mbps	Depends largely on delays and number of nodes	Maximum 1 Mbps but can be extended to 5 Mbps using special versions
2.	**Distance**	Up to 100m between each node	Designed for short distances but can be extended	40m for 1 Mbps 500m for 125kbps
3.	**Transfer Mode**	Full Duplex	Full Duplex	Half Duplex
4.	**Implementation**	Requires specific knowledge about the data model to implement on a system	Requires custom application-level protocol	Standardized or proprietary application layer
5.	**Synchronization capability**	In-built using distributed clocks for very high accuracy	Requires external implementation	Requires external implementation
6.	**Complexity**	Complex system with external hardware and integration tasks	Easy to use but requires application layer design	Easy to integrate and understand
7.	**Overall Cost**	High cost due to very specific hardware requirement	Very low cost	Low cost
8.	**Modularity**	Scalable up to virtually unlimited devices on the bus	Scalable to a large number of devices in theory but limited by delays	Up to 127 nodes in CANopen, depends on controller's driving capability
9.	**Hardware**	Requires additional ASICs along with microcontrollers	In-built in most commonly used microcontrollers	In-built in many microcontroller but requires a CAN transceiver IC to generate the differential signals

Table 3.1: Comparison - EtherCAT vs. SPI vs. CAN

3.4. Synchronisation Techniques

As discussed in the above sections, synchronization between all the controllers in a distributed system is important to ensure the proper working of the converter. In such systems, multiple slave controllers operate in parallel, and their operation needs to be coordinated with the system-level central controller. This section delves into the significance, challenges, and solutions of such synchronization techniques that can be used in modular power converters.

By ensuring a synchronized operation, the computation power can be equally shared among all the controllers, which utilizes the potential of all the modules in the system. The communication protocol used for the system plays an important role in this process. As explained in the above section, a few communication protocols, such as EtherCAT, have the feature to enable hardware based-synchronization [24, 28] between all the nodes on the bus. This makes EtherCAT very useful and preferred in high-power distributed systems. However, the other protocols do not have this feature, and an external process has to be implemented to synchronize the controllers.

An effective synchronization among all the controllers in the system offers several advantages, such as minimized voltage and current ripple, improved output power quality, and immediate detection of faults in the system. However, there are many challenges associated with achieving accurate synchronization among all the controllers in large systems, including:

- **Propagation delays:** Depending on the physical distance between the bus nodes, there is a propagation delay introduced by the medium, such as wires, and also by the parasitic elements of devices like any converters in the path.

- **Communication delays:** The bandwidth of a communication protocol is always limited and hence introduces delays in communication. If synchronization is developed using a specific message on the communication line, the delay introduced affects the stability of the system.

- **Processing time delays:** The controller's software introduces a processing time delay which is the time between a pulse physically at the input of the controller and the time before it is detected in the software.

Several synchronization techniques have been proposed and implemented for large distributed systems. Depending on the available hardware and other system parameters, an appropriate technique has to be designed for every application. The most common synchronization techniques include:

1. **Time-based Synchronization -** Uses time references such as clock signals to synchronize the operation of the converter nodes.

2. **Event-based Synchronization -** Relies on the occurrence of particular events in the system to coordinate the system nodes.

3. **Consensus-Based Synchronization -** Uses algorithms to achieve a consensus about the operating states of the controllers in the system.

From these discussions, it can be seen that implementing the proper synchronization techniques in distributed control systems is significant for achieving coordinated operation of the entire system. Several constraints, including the communication capability and system layout, make designing these techniques more difficult to implement. By carefully considering all the factors in the design, a robust synchronization technique can be developed that is reliable and efficient for any variations in the system.

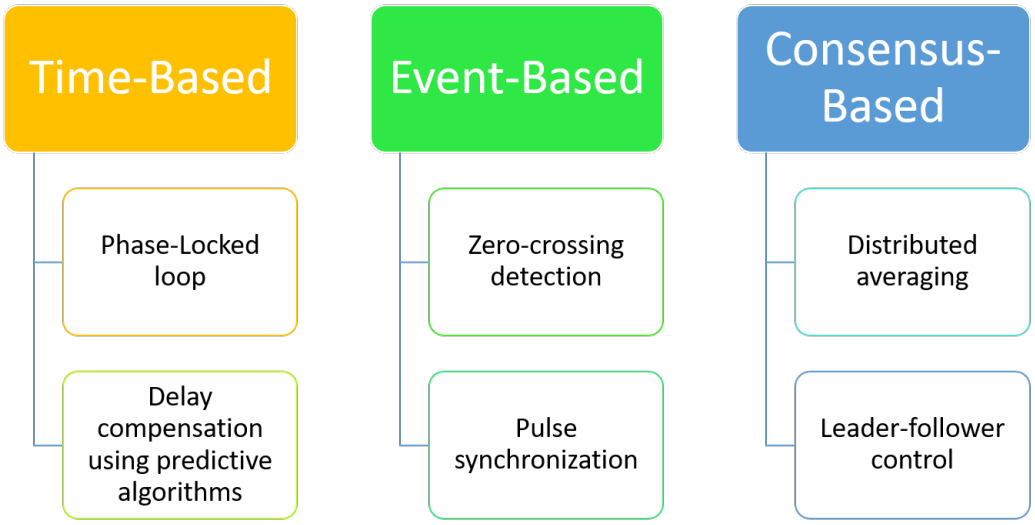


Figure 3.9: Synchronization techniques with examples

3.5. Developed Controller Architecture for SST

Considering all the factors discussed in this chapter, a careful design process is employed to develop the controller architecture for the converter system. Scalability, modularity, and overall efficiency were the most important aspects required in the hardware. The following decisions based on research of modular power converter systems were made:

1. **Type of Architecture -** Distributed controller architecture was required to keep the system's modularity and distribute the computational load to all the controllers. Due to a large number of nodes in the system, central controller architecture is not feasible to implement and requires a costly and powerful controller to handle all the control tasks. Also, it hinders the scalability aspect of the system by limiting the hardware, as discussed earlier in the chapter.

2. **Communication Protocol -** As a distributed system was decided to be implemented, a robust communication protocol with high data rates needs to be implemented. For this process, an initial estimate of data size between the controllers was made with 18 slave controllers (6 per phase) on each primary and secondary bus with one master system controller.

   This estimation shows that the CAN communication protocol cannot be designed for this system due to its limited data rate. However, both EtherCAT and daisy-chain SPI can provide this data rate and can be compared. The cost and implementation complexity of EtherCAT makes the design process for a prototype system difficult. However, it offers better features in terms of synchronization and flexibility for a converter like a Solid-State Transformer.

For the prototype design, it was therefore decided to implement a daisy-chain SPI system with digital isolators between the nodes. The microcontrollers selected for the hardware have in-built SPI capability, making implementation easier.

S.No.	Parameter	Primary Side	Secondary side
1.	Power Setpoint	18*32 = 576 bits	18*32 = 576 bits
2.	DC Microgrid - Voltage	18*32 = 576 bits	-
3.	AC Grid - Voltage (d,q)	-	18*32*2 = 1152 bits
4.	AC grid - Current (d,q)	-	18*32*2 = 1152 bits
5.	Fault and Status Bits	18*10 = 180 bits	18*10 = 180 bits
Total bits		1332 bits	3060 bits
Control Frequency		2 kHz	
Required Bandwidth		**2.66 Mbps**	**6.12 Mbps**

Table 3.2: An initial estimate of data size

3. **Synchronization Technique -** An external synchronization technique must be designed for a daisy-chained SPI distributed converter. To eliminate the delays caused by the communication protocol, an event-based synchronization between the controllers needs to be designed using an additional line connecting all the controllers.

   To implement this system, a timer pin on the system controller is connected through isolators to all the slave controllers in the system. The hardware propagation delays can be physically measured during the hardware implementation phase and set up in all the microcontrollers. A synchronization pulse is periodically sent from the master controller to all the slave nodes during the continuous operation of the converter, which can be used to reset the internal reference timers of all the slave nodes.

The complete design of the distributed control system using daisy-chained SPI is shown in Fig.3.10. The system uses a system controller referenced on the secondary side (AC grid), and digital isolators, each of 2.5kV, are provided between the secondary slave controllers. A 20kV optical isolator is provided on the primary side, and all the slave controllers are connected in a similar daisy-chain configuration. The configuration uses four SPI buses from the master controller for communication. The figure shows the communication design for a single phase. For a three-phase system, the topmost slave controller D_{out} is connected to the master. This results in three daisy-chain SPI buses on the secondary side, each with six slave controllers and one on the primary side with a single master controller for the complete three-phase solid-state transformer system.

3.6. Summary

This chapter investigated the complete aspect of controller architecture required in a modular high-power converter system. Several designs and considerations are introduced and compared to understand the significance of controller architectures. The chapter discussed the need for controller design in modular systems. The two popular types of systems are centralized and distributed. It then demonstrated the advantages and disadvantages of both these designs.

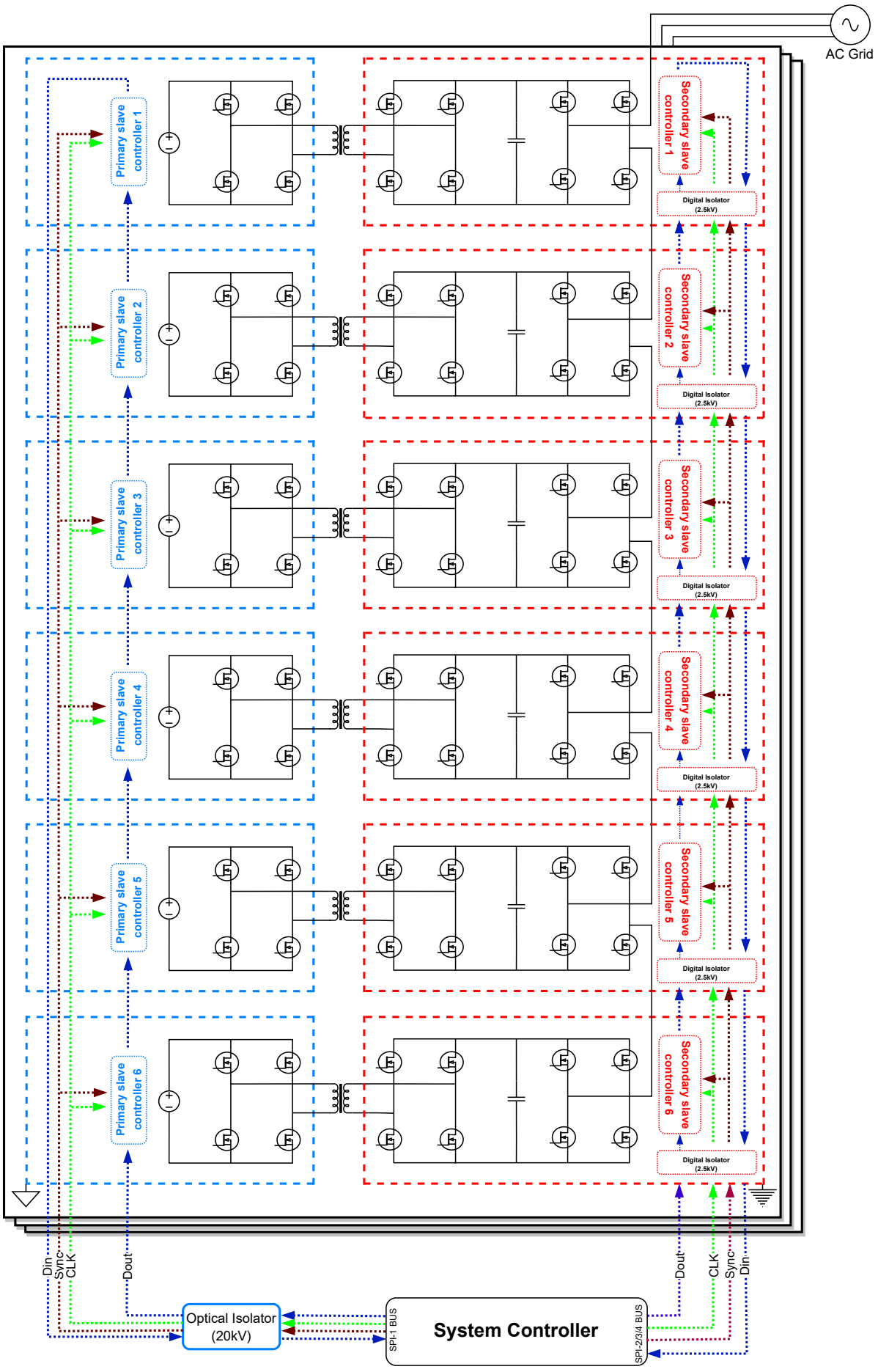


Figure 3.10: Designed Controller Architecture

The chapter then delves into the importance of communication protocols. Three popular protocols are discussed along with their working principles and finally compared on several parameters to understand their applications. Then, a vital aspect of distributed systems, the synchronization between the controllers, is introduced. The factors that affect the synchronization and potential solutions are discussed. Using all this information, a complete model of controller architecture is designed for the solid-state transformer.

4

Design and Control of the Inverter Stage

This chapter focuses on the design of the inverter topology, the modulation techniques used in simulations, and the feedback control loop for the operation of the multilevel cascaded H-bridge inverter. To begin with, a cascaded structure consisting of six cells of h-bridge converters(calculated using equation 4.1) is used to connect with a 10kV AC grid. This generates 13 voltage levels at the output AC voltage waveform. Each cell is connected to a separate, isolated DC/DC stage with DC microgrid as the source, as shown in Fig.4.1.

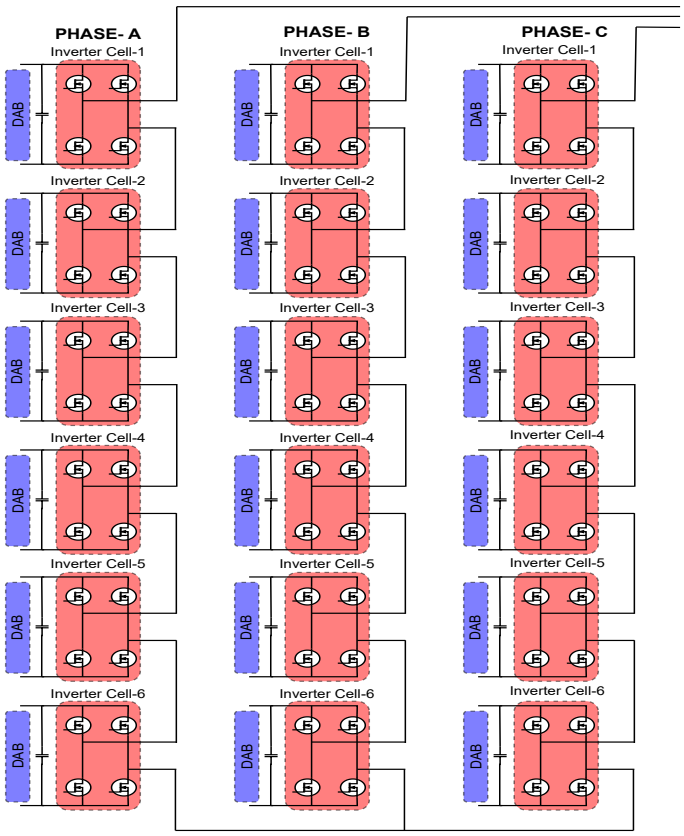


Figure 4.1: Inverter Connection

$$N_{cells} = \frac{V_{line-neutral,peak}}{V_{dc,microgrid}} = \frac{\frac{10000\times\sqrt{2}}{\sqrt{3}}}{1400} = 5.83 \approx 6 \tag{4.1}$$

Several models are simulated to test the converter's working in grid-connected mode. To connect to a medium-voltage AC grid, the converter must comply with the grid synchronization requirements while maintaining a sufficient safety margin. To adhere to these safety margins an adaptive modulation technique is implemented in the controller design. An output filter is designed at the output of the inverter to maintain the total harmonic content of the inverter below the specifications mentioned by the grid standards. This design process also calculates the common-mode voltage generated by the converter and tries to minimize it using modulation schemes and strategies to attenuate common-mode current injection into the grid.

4.1. Controller Design

This section explains the control requirement of a grid-connected three-phase inverter. With the help of defined switching states for power semiconductors, an inverter modulates DC input into a sinusoidal AC output. To fulfill the grid synchronization requirements, the sinusoidal AC output needs to be measured for three-phase voltages, their operating frequencies, and phase difference with respect to each phase. The measured parameters can then be used to generate a reference signal for the controller, which in turn helps to define the above-mentioned switching states for the individual inverter leg.

4.1.1. Reference Frames

A three-phase voltage measurement is required to measure the grid voltages. This results in a sinusoidal waveform and cannot be directly used as input to a voltage/current PI controller. This is due to the non-zero steady-state error in the controller caused by the continuously changing sine waves.

Instead, the sinusoidal values are converted into a synchronous reference frame known as the dq reference frame. This conversion process is performed in two steps. The first step is Clark Transformation, which changes the sinusoidal quantities into a fixed reference frame, known as the $\alpha - \beta$ frame. The second step is Park Transform, which translates the generated $\alpha - \beta$ quantities into a synchronous dq frame.

In the dq frame, sinusoidal quantities can be expressed as DC quantities as the frame rotates at the same frequency as that of the quantities it measures. This simplifies the controller design with simple DC quantities, as the error is now constant in the PI controller.

4.1.2. Phase Locked Loop (PLL)

Other important parameters the controller requires are the grid's frequency and phase. These parameters can be measured using a PLL. A PLL consists of a phase detector and a voltage-controlled oscillator to track the phase of any signal. It can also generate the frequency of the signal using the phase information. The phase measurement is required to convert the $\alpha - \beta$ quantities into synchronous dq quantities. The discussion on the types of PLL and their merits and demerits is beyond the scope of this thesis.

4.1.3. PI Controller

A grid-tied inverter requires a current controller to determine and control the power flow into the grid. A reference value for current can be generated using the desired power flow into or

from the AC grid and the calculated and transformed voltage of the grid. This current reference is used to calculate the error at the input of a PI controller, along with the value from the inverter current measurement.

The PI block provides an output proportional to the integrated error, and this output is added with a feedforward signal to generate the final control output signal. This output is used as reference dq voltages and as input to the modulator. At the input of the modulator, these values are transformed back to sinusoidal values in the case of sinusoidal PWM or $\alpha - \beta$ values in the case of space vector PWM. The complete control block is shown in Fig.4.2. Here, the q-axis current is set to zero to implement active power control and set the reactive power to zero.

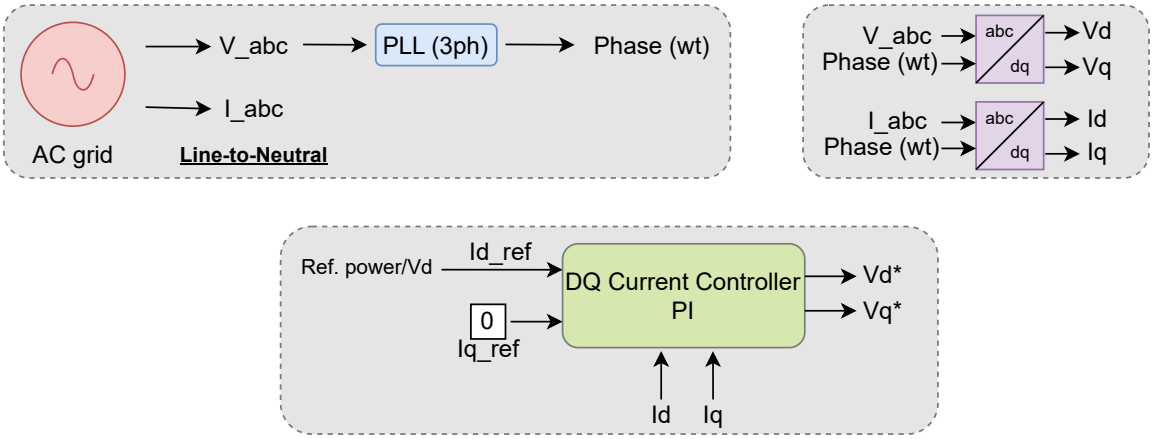


Figure 4.2: Control Block

4.1.4. Start-up procedure

During a regular start-up sequence, power flow cannot be initiated immediately. It is observed that the PLL requires a considerable time to settle with its phase output. Therefore, a contactor remains open at the output of the inverter during this period of time. Then, the contactor is closed, and the power flow can be initiated. This process can be seen in Fig.4.3 below.

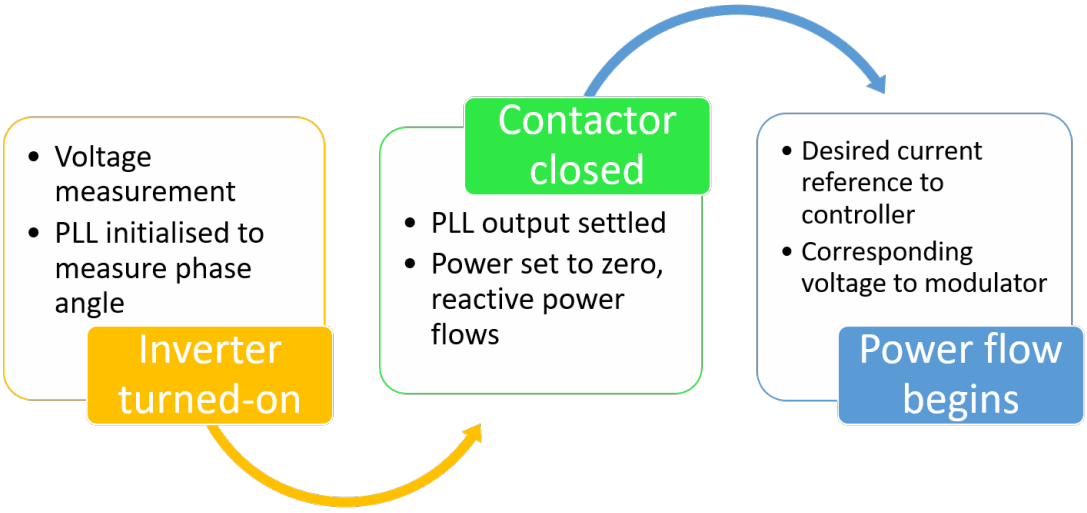


Figure 4.3: Start-up Sequence

In the start-up sequence shown above, the contactor is closed at $t = 0.1sec$, but the power reference is maintained at zero. A small amount of current flows into the capacitor at the output of the inverter in this state. At $t = 0.14sec$, the power reference is set to the desired value and an appropriate amount of current starts flowing into the grid.

4.2. Design of Output Filter

As discussed in Chapter 2, an output filter is required to reduce the harmonic content in the grid and attenuate the switching harmonics to increase the power quality. This section explains the design process and performance of the designed filter for the 13-level inverter.

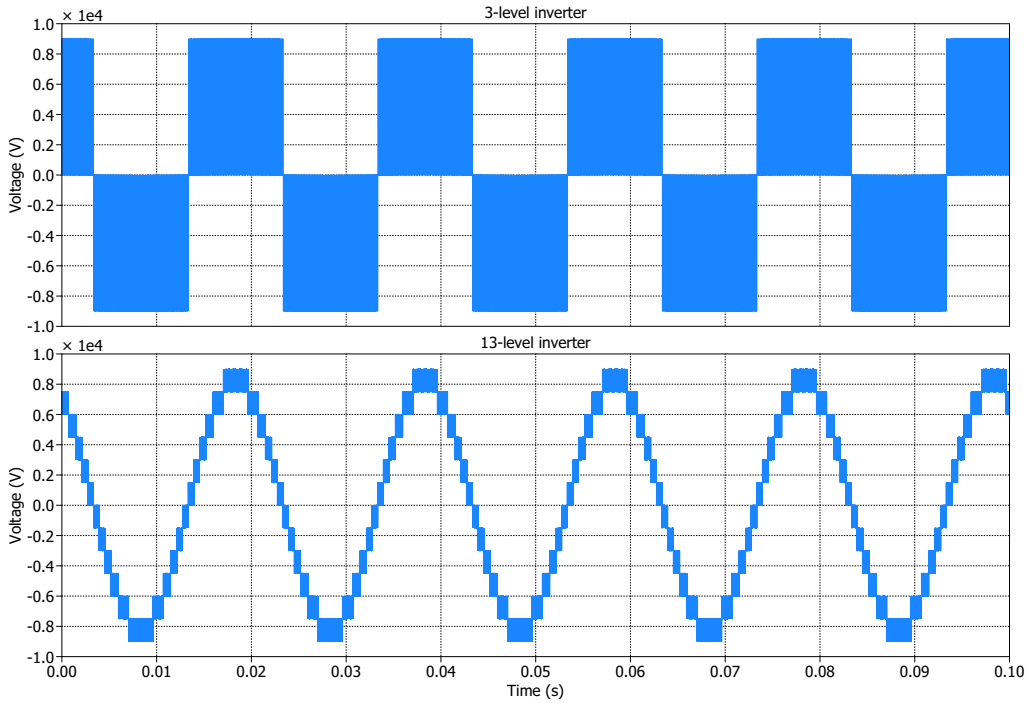


Figure 4.4: Difference between 3-level and 13-level waveform

A multilevel converter inherently reduces the size of the output filter as it follows the reference values with minimal error. This difference is highlighted in Fig.4.4. An iterative design procedure 4.5 is followed to size the output filter. An LCL filter is selected for this application due to its superior performance and higher attenuation capability [23, 34]. To determine the initial values of the filter, the procedure from [35, 36] is followed.

The converter side inductance is determined by calculating the current ripple in the output waveform and calculating the minimum inductance to limit the ripple to 20% at a modulation index of 0.5, where the ripple is maximum. This inductance can be given by:

$$L_c = \frac{V_{dc}}{4 \times f_{sw} \times \Delta i_{p-p,max}} \tag{4.2}$$

where,
L_c = Converter side inductance,
V_{dc} = DC side voltage,

f_{sw} = Switching frequency,
$\Delta i_{p-p,max}$ = Maximum peak-peak current ripple

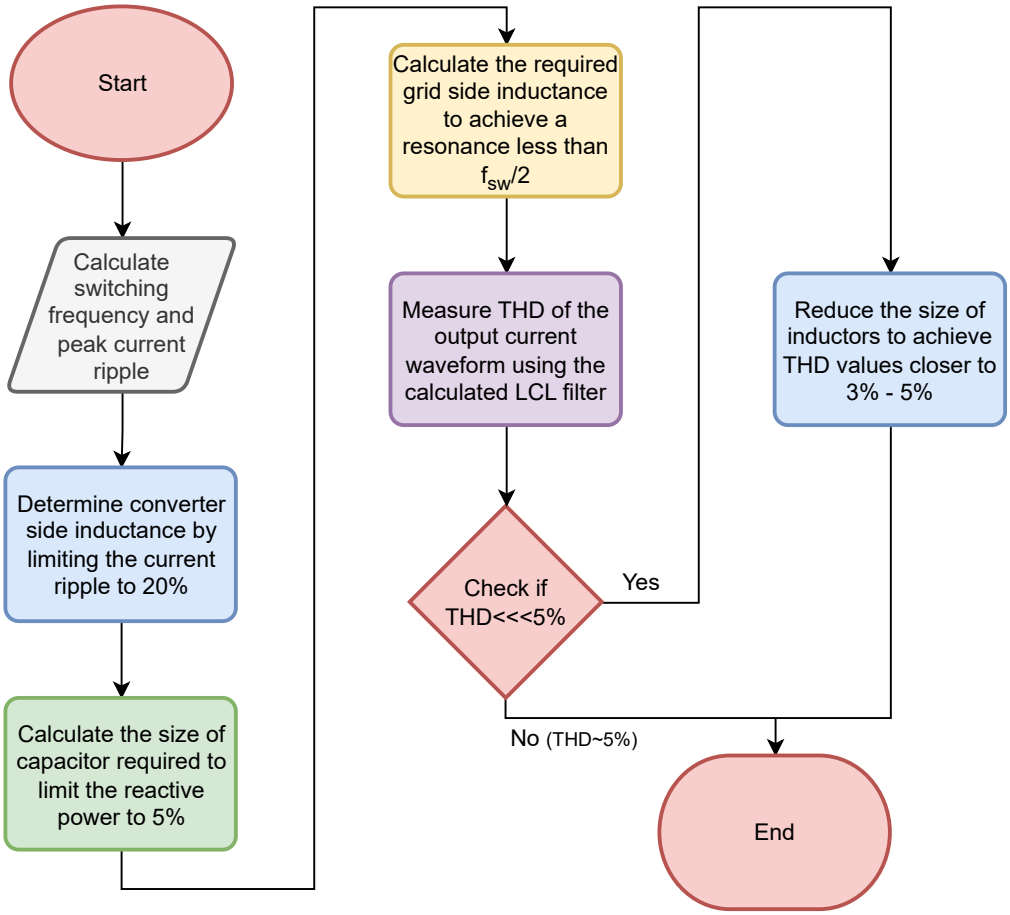


Figure 4.5: LCL filter iterative design process

For a multilevel converter, the DC side voltage used in this equation is of a single cell instead of the complete DC voltage [37, 38]. In the case of the 13-level inverter, the inductor size reduces by a factor of 6 due to this change in calculation. The capacitor is designed to maintain the reactive power of the inverter, typically less than 5%. The grid side inductance is then chosen to maintain the LCL resonance to at least ten times the grid frequency and lesser than $f_{sw}/2$.

4.2.1. THD

The initial values calculated from the above process are used for initial simulations with a switching frequency of f_{sw} = 10 kHz. As the inverter is simulated in grid-connected mode, the voltage waveforms show negligible harmonic content as an ideal grid is connected at the output, which has 0% THD. Therefore, only the harmonic content in the output current waveforms is of interest.

Increasing the switching frequency increases the THD due to the dead time phenomenon explained earlier in Chapter 2. Therefore, to reduce the overall THD to <5%, the LCL filter values are changed to a minimum size. The values iterated in the simulation models (using PS-PWM, explained further in the next section) are shown in Table 4.1.

Iterations	LCL Values	LCL Resonance Frequency	THD% in Current Waveform
Initial Calculation	L_c = 1.4mH; C = 185nF; L_g = 0.7mH	17.1 kHz	∼0%
Iteration 1	L_c = 0.5mH; C = 185nF; L_g = 0.25mH	28.6 kHz	0.5%
Iteration 2	L_c = 0.2mH; C = 185nF; L_g = 0.1mH	45.3 kHz	3.4%
Iteration 3	L_c = 0.1mH; C = 185nF; L_g = 0.05mH	64.1 kHz	15.8%

Table 4.1: LCL filter size

4.2.2. Common Mode Current

During the filter design process, another important aspect of the inverter to be considered is the common mode current flowing into the grid. A good hardware design with effective modulation techniques limits the magnitude of common-mode voltage and the current. However, this must be designed in the simulations, and certain modifications must be made in the design process.

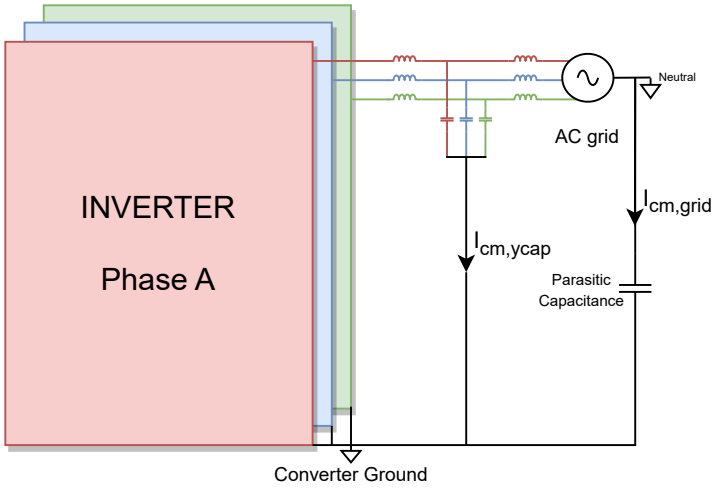


Figure 4.6: Parasitic Capacitance for common-mode current

To simulate this parameter, a small parasitic capacitance between the converter ground and neutral of the AC grid is placed as shown in Fig.4.6. X and Y capacitors rated for voltages of 10 kV are placed at the output to provide a path for common-mode current to return to the source and not flow through to the AC grid. These capacitors provide a lower impedance to the common-mode current, thus, helping reduce the amount of common-mode current in the grid. This can be seen in Fig.4.7.

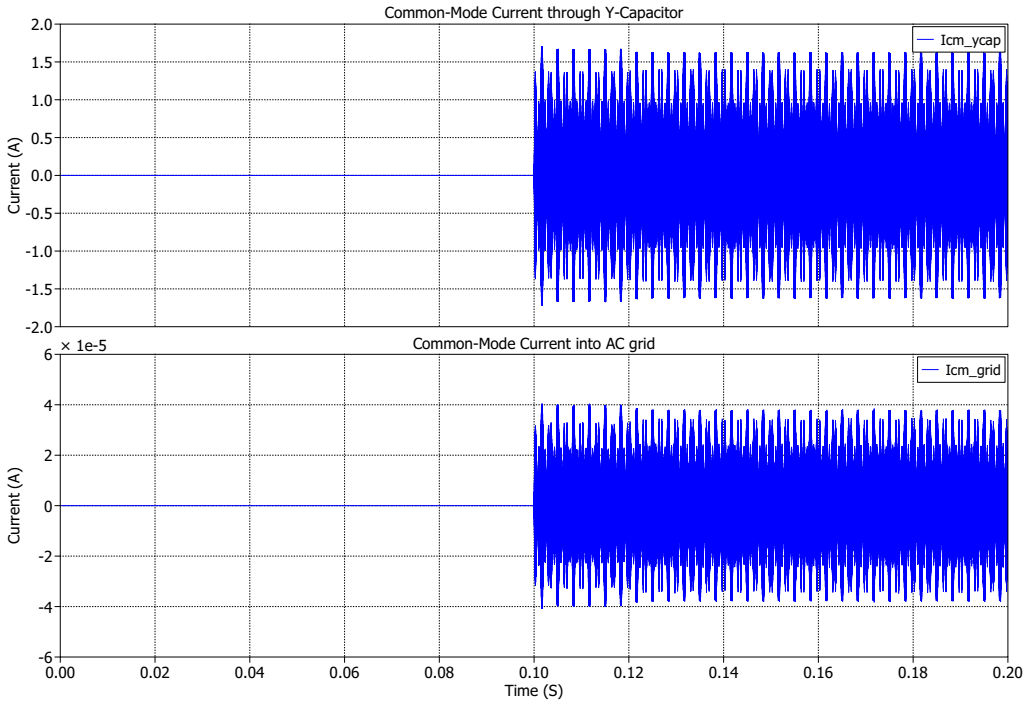


Figure 4.7: Common-mode current distribution

4.3. Modulation techniques

As discussed in Chapter 2, modulation strategies are a key aspect of a power electronic inverter design. The right modulation technique reduces the overall THD content generated from a power converter by optimizing the switching sequence. However, simple modulation techniques do not apply to multilevel inverters. Several modifications are required, making most methods too complex for implementation. The same problem applies to the space vector modulation scheme's application in multilevel inverters.

4.3.1. Modular Space Vector Modulation Algorithm

It can be seen from the comparison of SPWM and SVPWM techniques in Table2.4 that SVPWM results in a much superior performance for power electronic converters. This requires us to understand the problems of implementing SVPWM for multilevel inverters. Several papers [39, 40, 41, 42, 43] implement SVPWM for higher-level inverters with specific algorithms to reduce the computational power requirement. As mentioned earlier, the number of switching states of a 'n' level multilevel converter equals 'n^3' with increasing redundant switching states as the levels increase. This problem makes SVPWM a less popular choice in higher-level converters.

To overcome this issue in a 13-level inverter, a modular algorithm is required to decompose the hexagon into smaller sections with minimum decomposition steps. A similar decomposition can be applied for any level inverters, making this algorithm scalable to different applications. Fig.4.8 shows the decomposition pattern followed in the developed algorithm.

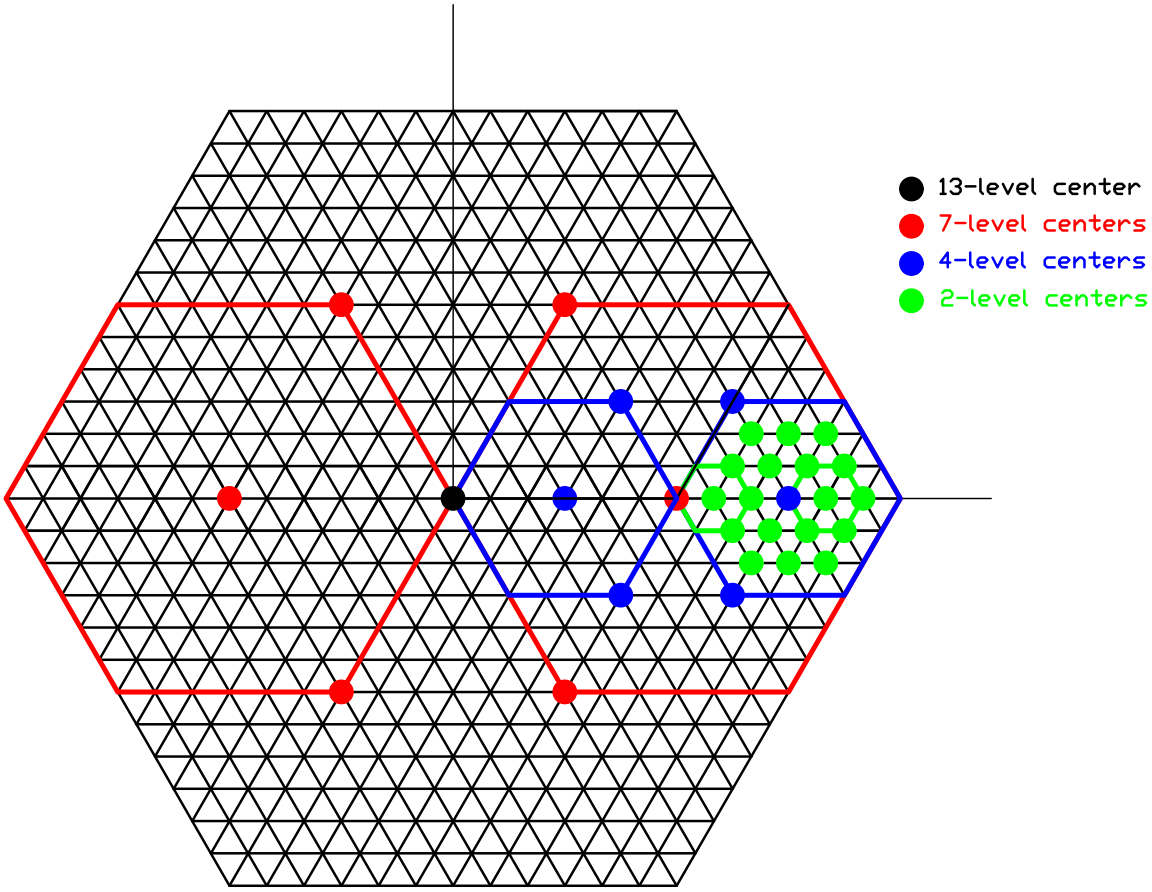


Figure 4.8: 13-level Decomposed Space Vector Diagram

The algorithm starts with an initial reference vector from the control block and calculates the vector's angle. At this stage, the algorithm determines the 7-level hexagon of interest and eliminates all other hexagons. By this step, the algorithm reduces the number of switching states and, thus, the computation steps by a factor of six. A new position for the reference vector is now calculated from the selected 7-level hexagon's center position. The same process is repeated to decompose into a 4-level hexagon and again for a 2-level hexagon. At this stage, a simple 2-level SVPWM process can be employed to determine the required switching states. The entire algorithm is shown in Fig.4.9 below and in Appendix A.

A MATLAB model was developed to realize this algorithm with a 13-level inverter and measure the THD content in the output voltage waveform. Several different values for switching frequency and LCL filter were iterated on the model to achieve optimal THD values. The following figure shows the THD content in the output current waveform of the model using a symmetrical switching sequence and the following input parameters:

Model Parameters: $f_{sw} = 40kHz; L_c = 0.8mH; C = 185nF; L_g = 0.4mH;$

Switching states in a sector: S_0 - 0; S_a - 1; S_b - 2; S_0 - 3;

Switching Sequence: 3 - 2 - 1 - 0 - 1 - 2 - 3

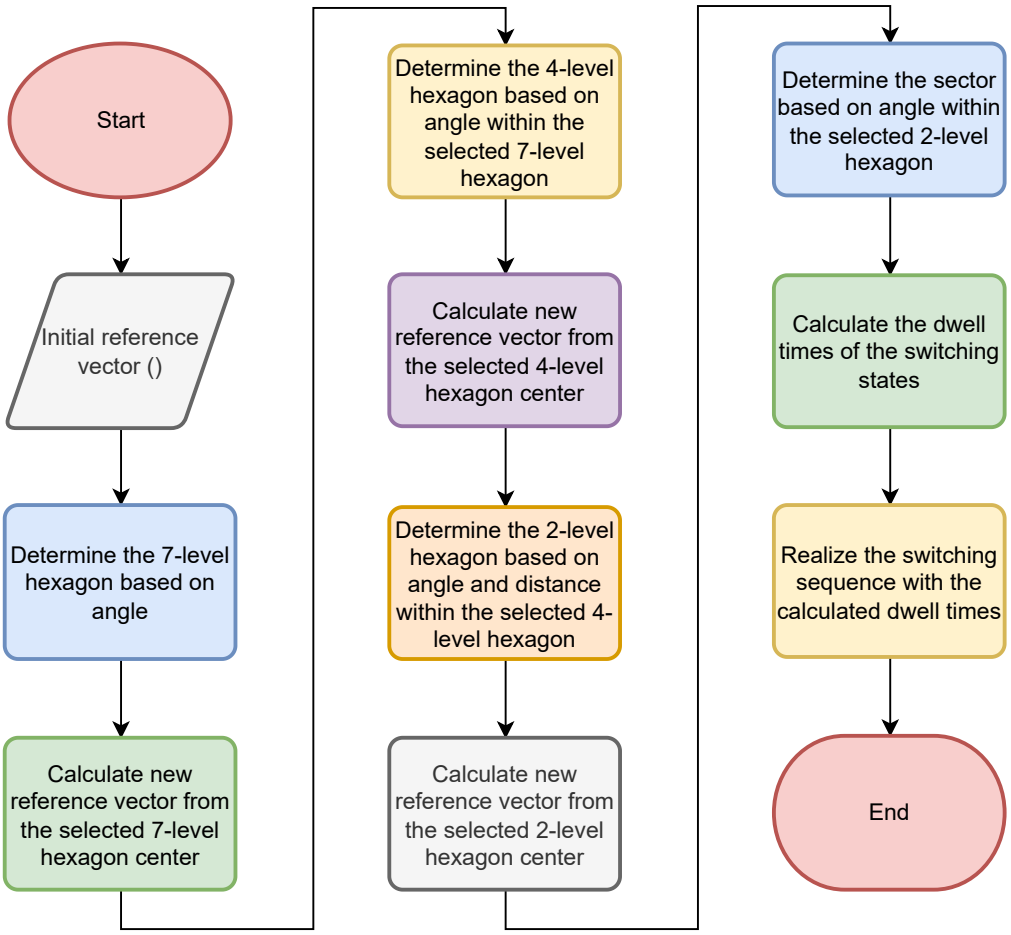


Figure 4.9: Reduced-level hexagon tracking for 13-level SVPWM technique

On observing the switching patterns realized in the model, there was a problem with how the algorithm finalizes a particular state from the multiple redundant switching states. This caused undesired switching transitions in the pattern during a change in the base 2-level hexagon, which reduced the overall efficiency of the modulation technique. To overcome this issue, a look-up table with an optimized switching sequence for every sector in the 13-level hexagon is necessary, as mentioned in [17]. In this report, the author mentions using a look-up table to store the optimized switching sequence for every sector. However, this process must be accomplished using an additional algorithm implementation and the developed design to maintain modularity.

The developed base algorithm proved to reduce the computation steps required to utilize the space vector PWM modulation technique for multilevel converters. Space Vector PWM can be modified and customized for specific applications, which could help reduce the common-mode voltage and lower power device switching losses. This is important to solve the false-tripping of Residual Current Devices (RCD) devices. However, this technique was limited to only 2, 3, and 5-level inverters due to the increasing complexity of SVPWM beyond these levels. These modifications can now be applied to higher-level inverters using this base algorithm, achieving all the advantages of SVPWM.

For this thesis, the overall THD content and LCL filter size are important aspects of the con-

verter design. The SVPWM algorithm requires further implementation and modifications to achieve the required performance. However, due to the project's objectives, it was decided to design and simulate other modulation schemes and select the most applicable technique for this application.

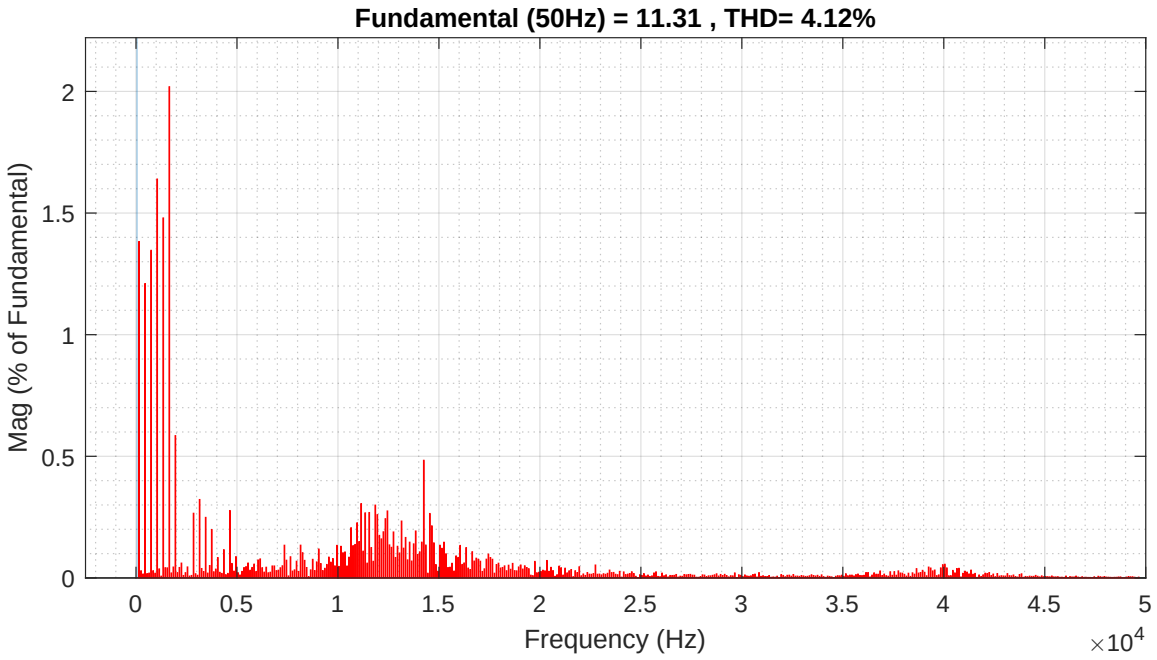
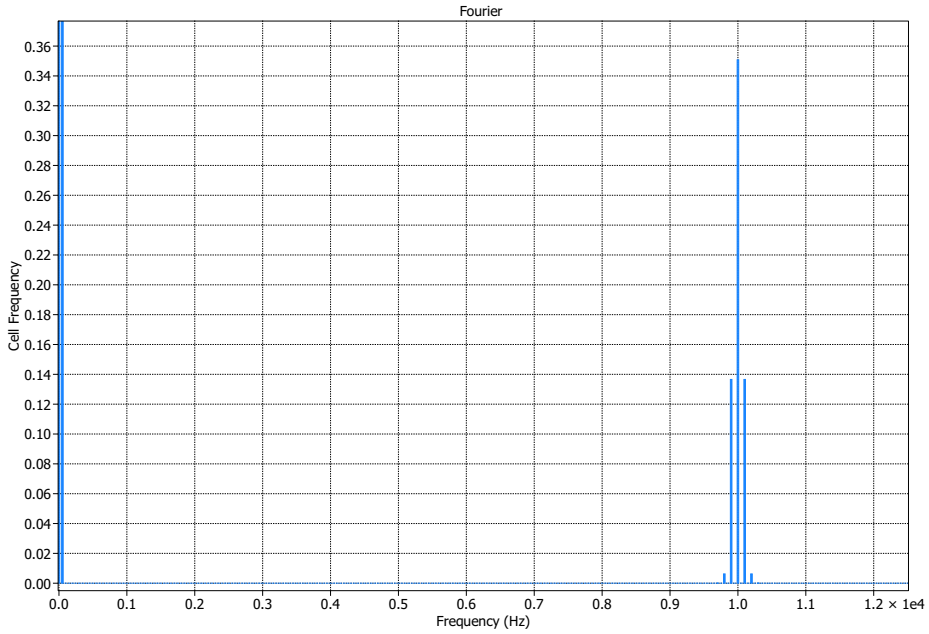


Figure 4.10: THD value in the developed SVPWM technique-based model

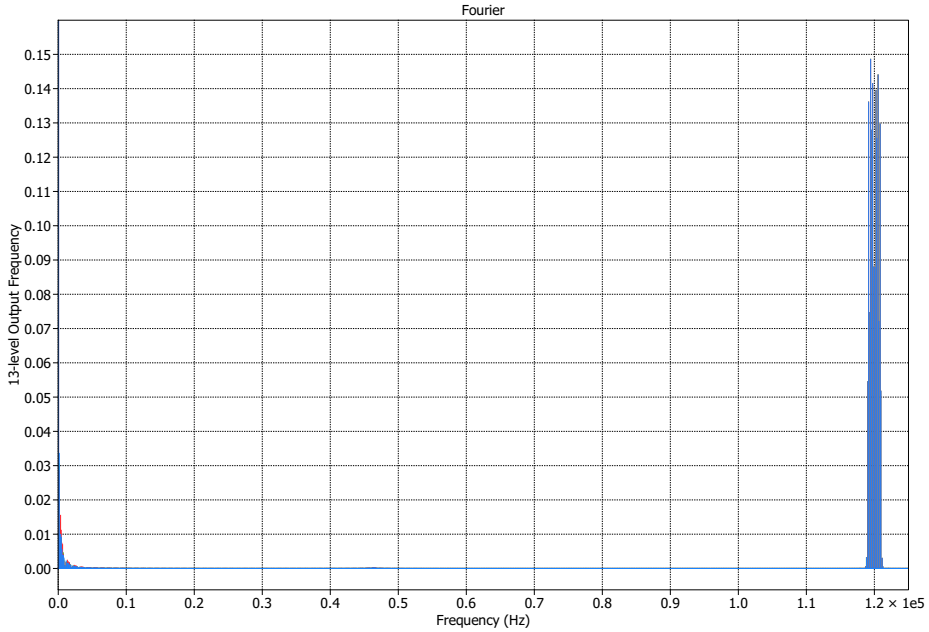
4.3.2. Sinusoidal Modulation Techniques

Sinusoidal PWM is the most popular modulation technique in the case of multilevel inverters. Their relatively easier implementation and good performance make them the ideal choice. Generally, multilevel converters inherently have the advantage of reducing the THD content [11], which allows the use of SPWM techniques over SVPWM strategy and still achieves a good performance in terms of overall output quality [44]. Two types of SPWM techniques are explained in Chapter 2, namely Phase-Shifted PWM and Level-Shifted PWM.

Phase-Shifted SPWM In the case of PS-PWM, the power is evenly distributed among all the cells. Another added advantage of this technique is that a switching frequency of $'x'$ Hz in each half-bridge results in a total switching frequency of $'n * x'$ at the output, where $'n'$ is the total number of carriers required for the multilevel converter. This helps in a huge reduction in the size of the output filter, thus, helping the overall size and cost of the converter. The following Fig. 4.11 shows the switching frequency component at the output of a 13-level inverter using the PS-PWM technique.



(a) Cell Frequency @ 10kHz



(b) 13-level Inverter Output Frequency @ 120kHz

Figure 4.11: Cell Frequency vs. Output Frequency in a 13-level inverter using PS-PWM technique

Level-Shifted SPWM Both these SPWM techniques are implemented and simulated for a 13-level inverter. This allows for a straightforward comparison between the two methods regarding overall THD content, power distribution among cells, switching losses, etc. It had been earlier discussed that the LS-PWM technique causes an uneven power distribution in the cells and requires an external process to compensate for this issue [15]. To overcome this,

a design with dynamic carrier distribution among the cells was developed in the model. This process re-assigns the carriers to each half-bridge at regular intervals to achieve an equal average power distribution every six sine cycles (120ms), as shown in Fig. 4.12.

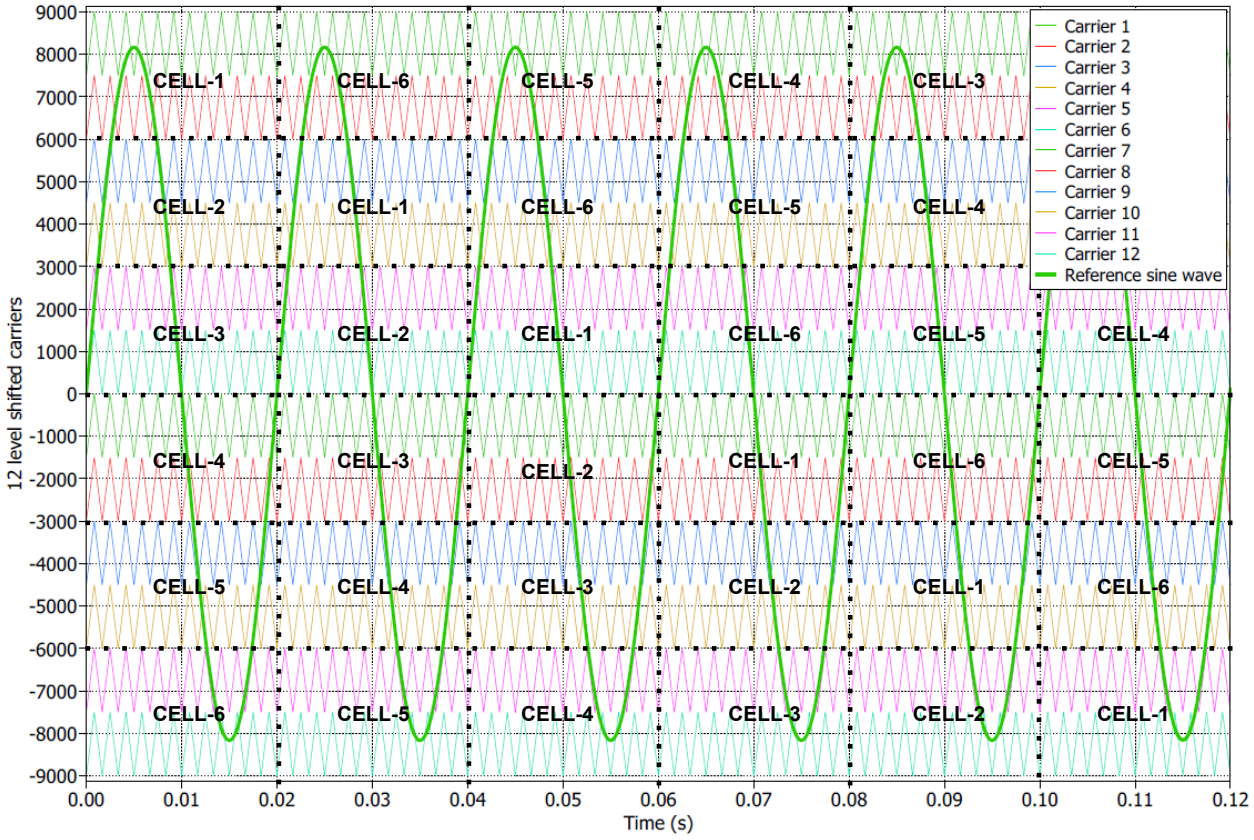


Figure 4.12: Dynamic Carrier Distribution in LS-SPWM Method

Comparison The overall THD content in the output current waveform using both these techniques in a 13-level converter are summarised in Table 4.2 below:

Type of SPWM	Switching Frequency	LCL Values	LCL Resonance frequency	THD% in Current Waveform
PS-SPWM	10 kHz	L_c = 1.4mH; C = 185nF; L_g = 0.7mH	17.1 kHz	∼0%
	10 kHz	L_c = 0.2mH; C = 185nF; L_g = 0.1mH	45.3 kHz	3.4%
LS-SPWM	40 kHz	L_c = 4.1mH; C = 185nF; L_g = 2.1mH	11.3 kHz	∼1%
	40 kHz	L_c = 0.8mH; C = 185nF; L_g = 0.4mH	22.6 kHz	4.1%

Table 4.2: Comparison of PSPWM and LSPWM Techniques

Conclusion It can be seen that PS-SPWM offers clear advantages over LS-SPWM and SVPWM in terms of reduced switching frequency, contributing to lower switching losses and LCL sizes. This is clearly due to the increased frequency in the output waveform. SVPWM performs similarly to LS-SPWM regarding the overall THD content (4.1%) with the same switching frequency and LCL filter values. However, as mentioned before, SVPWM switching can further be optimized to achieve better results. Based on these results, it was decided to use PS-SPWM for this inverter design.

4.4. Summary

This chapter illustrates the complete inverter design process and results from various simulations. It starts with the controller design for the inverter, which explains the developed current control and start-up sequence in grid-connected mode. The reference frame transformations and phase detectors are also introduced in this section. Then, the iterative design process used for designing the output filter and design consideration for reducing the common-mode current is explained.

The requirement of developing a modular space vector algorithm for multilevel inverters is established. The complete designed algorithm is explained using a flowchart and decomposition diagram and its performance on a 13-level inverter model. The shortcomings of the developed algorithm in optimizing the switching states are presented, and potential applications are suggested for the developed base algorithm. Sinusoidal PWM techniques for multilevel inverters with power-balancing designs are introduced along with THD content and switching frequency comparison. Finally, phase-shifted SPWM is selected for the design due to its clear advantages over the other techniques.

5

Hardware and Testing Results

This chapter focuses on the built hardware prototype board and the design considerations taken into account for the design process. It then delves into the testing process and the achieved results. These results help validate the designed hardware and also verify the converter simulations.

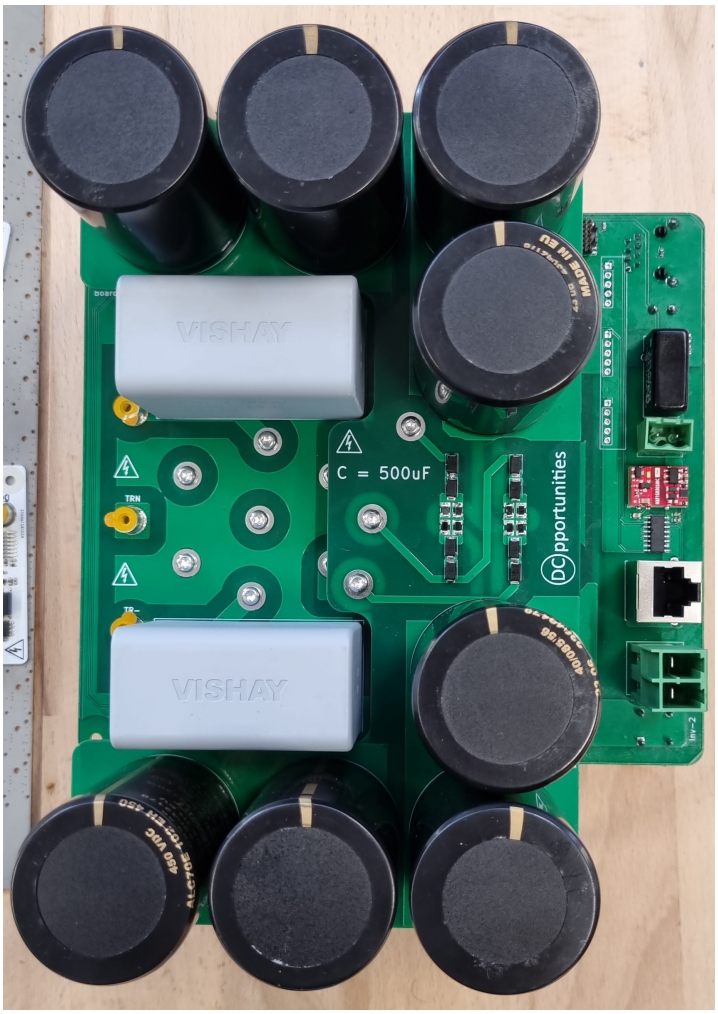


Figure 5.1: Implemented Hardware Setup - Top View

The prototype boards are designed and manufactured with all the required clearances for the complete voltage of 1500V between a pair of cascaded inverter cells. The implemented hardware board is shown in Fig.5.1.

5.1. Hardware Board Design

This section gives a clear and detailed explanation of the hardware components used in the prototype board and their interconnections. This board includes two full-bridge power boards, DC link capacitors, output connectors to the next cascaded inverter cells, an isolated communication bus, and the slave microcontroller with the required low-voltage circuitry. The input to this board is an isolated transformer, which is first rectified using the first full bridge. Here, sufficient DC link capacitance is provided and connected to another full bridge for inverter operation. Fig.5.2 provides a detailed block diagram explaining all the important aspects of the designed hardware.

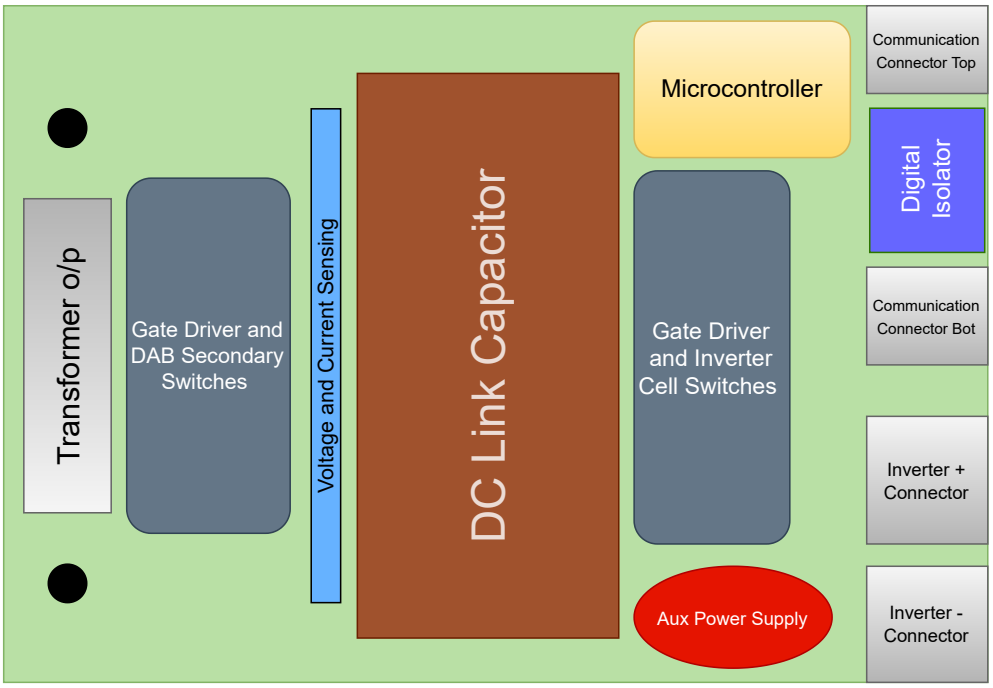


Figure 5.2: Block Diagram - Hardware Board Design

The full bridge circuitry is designed on aluminum PCBs for improved thermal performance. Single-layer aluminum board with isolated gate drivers and 1700V-rated SiC MOSFETs are designed. These are connected to the main board from the bottom using surface mount connectors and LV connectors for signals. STM32G4 series microcontroller is used as a slave controller on each secondary board. An additional board is designed with electrolytic capacitors as part of the DC link capacitance on top of the main board to reduce the main board's overall size, as seen in Fig.5.3.

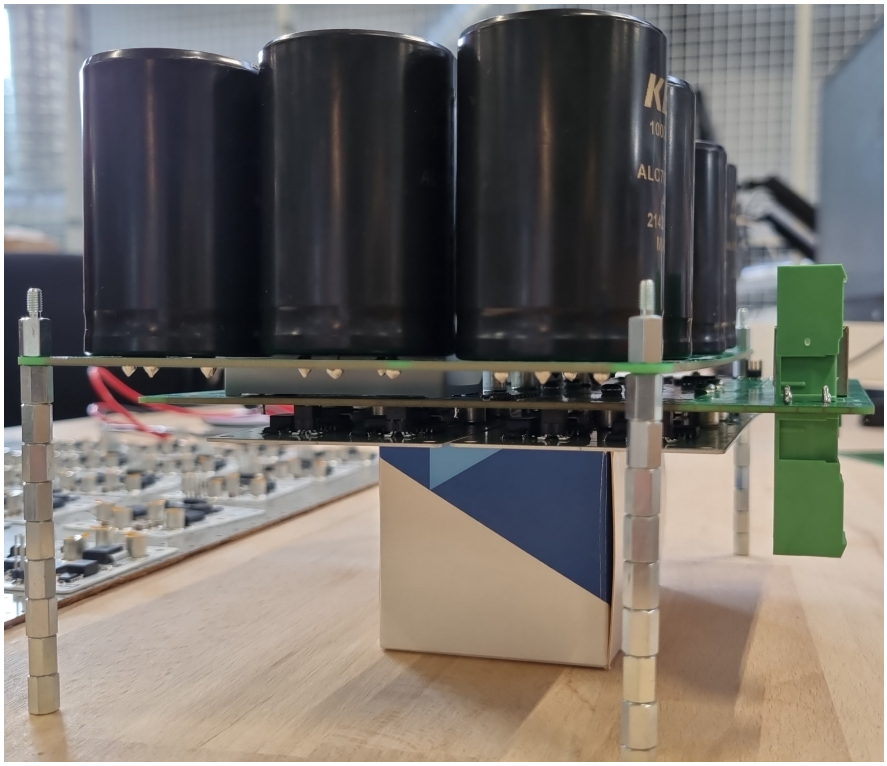


Figure 5.3: Implemented Hardware Setup - Side View

As explained in Chapter 3, digital isolators are used in each of the secondary boards for SPI communication. A 4-channel digital isolator with an isolated power supply is included on the main board to communicate with other cells in the cascaded network. Vertically mounted connectors are used throughout the design, and a continuous ground shield on all layers of the PCB is placed to reduce the field between a single connector/cable and the container of the complete system.

5.2. Testing and Validation

Synchronization is an important aspect of any distributed converter system. Each inverter cell works on a similar control loop and modulation technique. However, all the PWM signals and the data from the master controller must be accurately synchronized to ensure smooth operation of the converter. Several kinds of delays and their consequences are already explained in the previous chapters.

In theory, the developed synchronization technique helps mitigate this issue. A hardware setup with two inverter cells in a cascaded structure is connected to experimentally verify the synchronization technique, as shown in 5.4. A switching frequency of $f_{sw} = 10kHz$ and a constant duty cycle of $d = 0.5$ is used on both the inverter full-bridges.

In all the waveforms below, *Sync Signal 1* (blue) is the synchronization pulse at the output of the master controller, and *Sync Signal 2* (red) is the synchronization pulse at the input of the slave controller after the isolator. Similarly, *PWM Signal 1* (green) is the PWM signal from the master controller, and *PWM Signal 2* (yellow) is the output PWM signal from the slave controller.

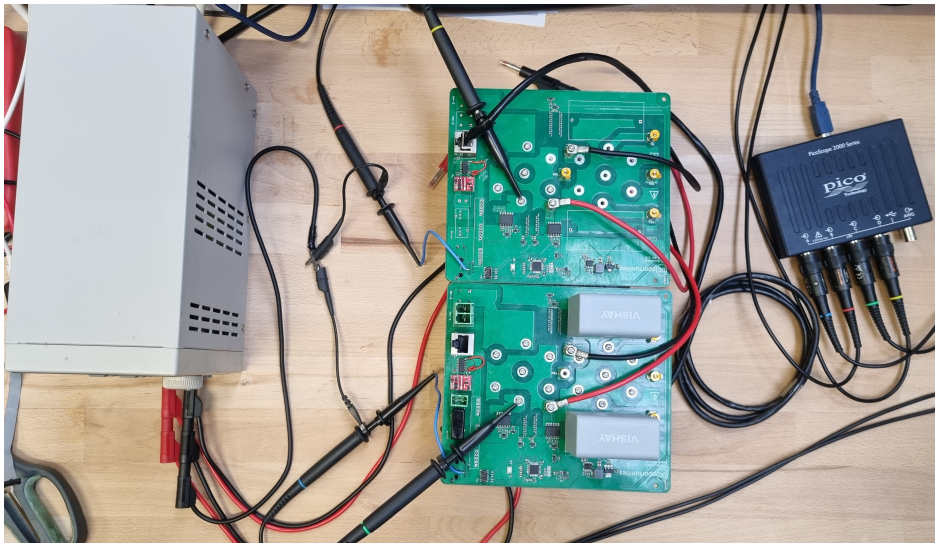
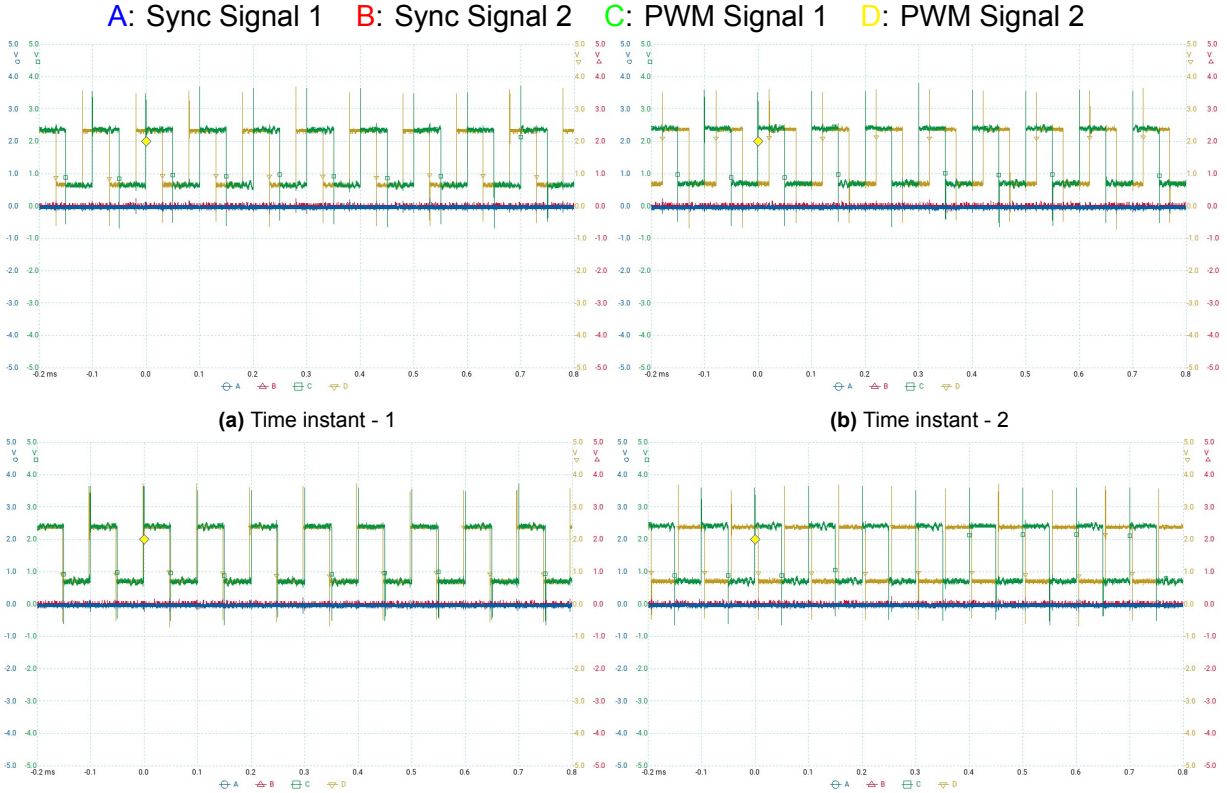


Figure 5.4: Synchronization Testing Setup

5.2.1. No synchronization

The boards are first tested without a synchronization pulse between the two slave controllers. This test is performed to understand the degree of mismatch between the two PWM signals and show the significance of accurate synchronization in power converters. It can be observed from Fig.5.5 at four different time instants that a continuously changing error exists; hence, this type of system cannot be used for power applications.



(a) Time instant - 1

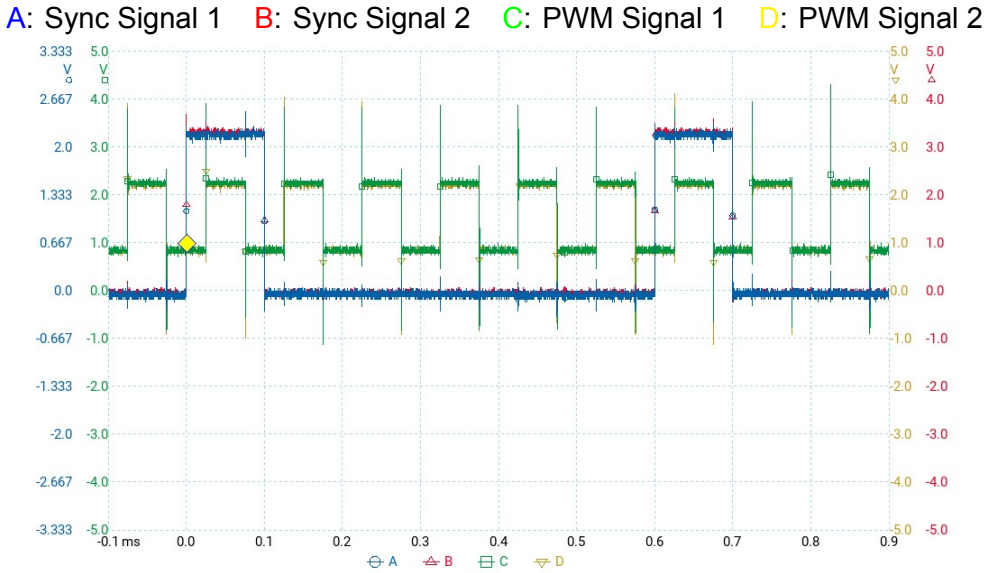
(b) Time instant - 2

(c) Time instant - 3

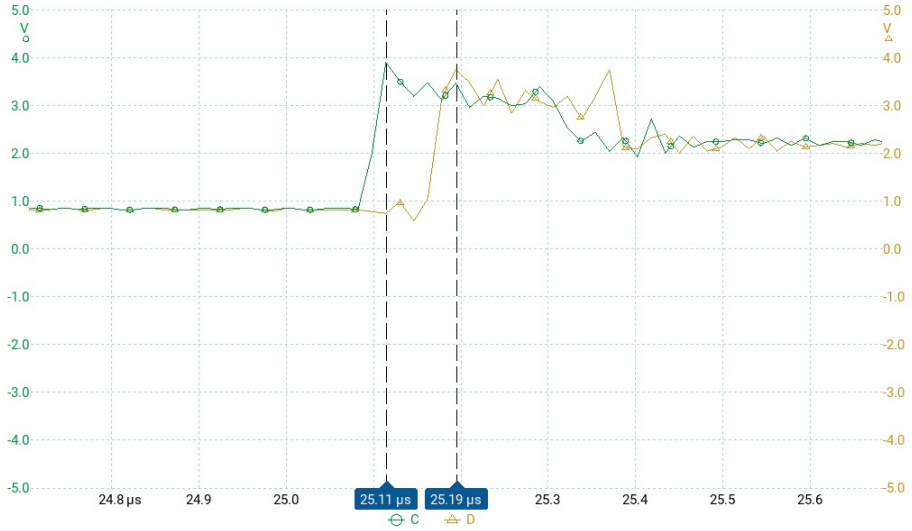
(d) Time instant - 4

Figure 5.5: PWM signals of two cells without synchronization

5.2.2. Slow synchronization



(a) Overall waveform with synchronization pulses every 5 periods



(b) Difference in PWM signals between t = 0.1ms and t = 0.2ms ($t_\Delta = 80.66ns$)

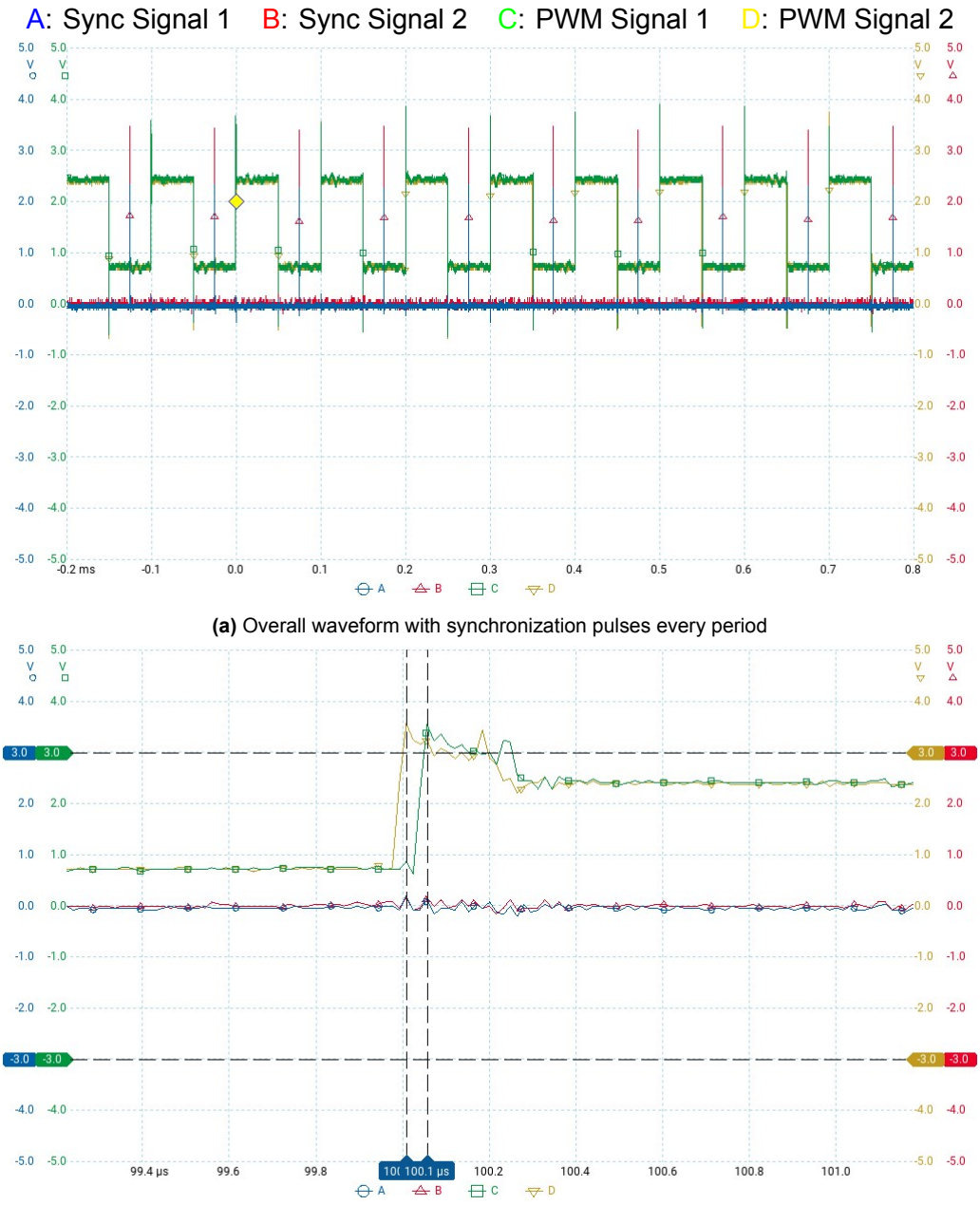
(c) Difference in PWM signals between t = 0.5ms and t = 0.6ms ($t_\Delta = 575.8ns$)

Figure 5.6: PWM signals of two cells with slow synchronization

Next, a timer is configured as a trigger output on one of the inverter boards. All the PWM timers of that controller are reset using this trigger output internal to the microcontroller. On the other controller, a timer is triggered using this external pulse from the first controller. This pulse is configured as an external trigger, and all the timer pins are synchronized to this pulse. This setup outputs a synchronization pulse every 5 switching periods for regular and consistent synchronization between the controllers.

It can be seen in Fig.5.6 that this setup reduces the change in error by a large value. However, a large delay still exists, continuously changing, making it difficult to compensate for the error.

5.2.3. Synchronization without compensations



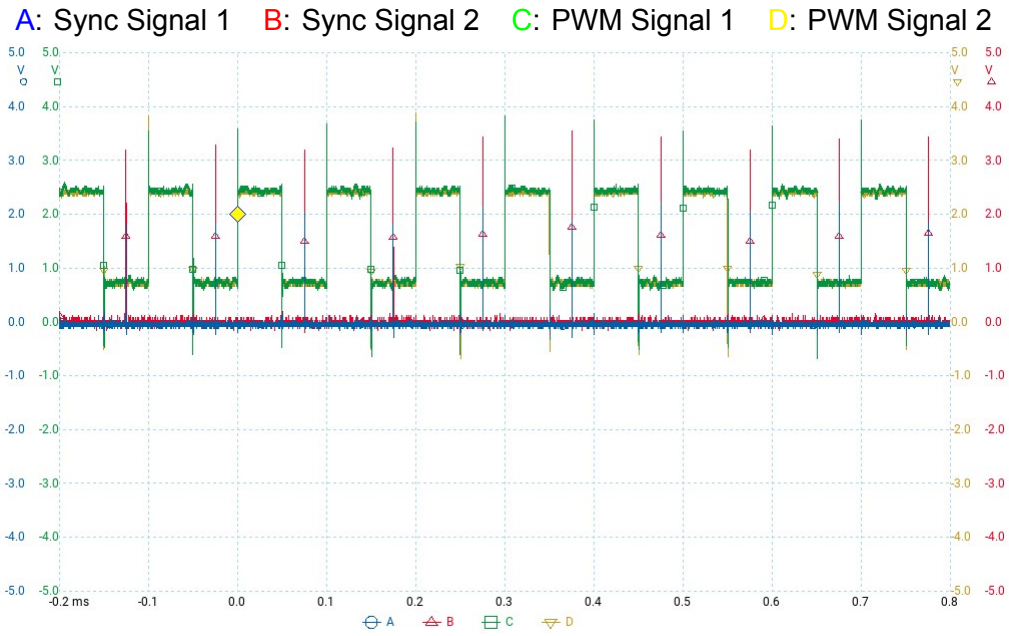
(a) Overall waveform with synchronization pulses every period

(b) Difference in PWM signals ($t_\Delta = 48.48ns$)

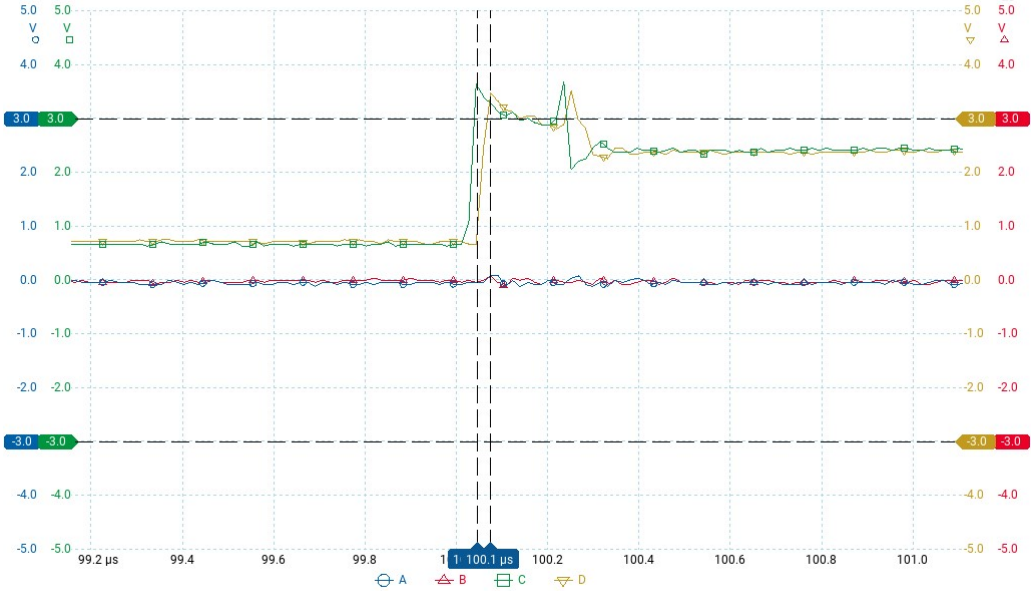
Figure 5.7: PWM signals of two cells with fast synchronization

It can be observed from the previous synchronization test that the timers require a more frequent synchronization pulse to eliminate the changing error between successive PWM signals. A synchronization pulse is generated every switching period from the first controller to test this theory. The pulse width of this synchronization pulse is set to a minimum value to ensure it reaches the high logic state. It must be determined during testing as it depends on the hardware design and the capacitance of the trace. It can be seen in Fig.5.7 that this setup reduces the changing error phenomenon observed in the previous tests. However, a large delay still exists between the PWM signals due to the various delays in a hardware setup, including propagation and processing delays.

5.2.4. Synchronization with delay compensation



(a) Overall waveform with synchronization pulses every period



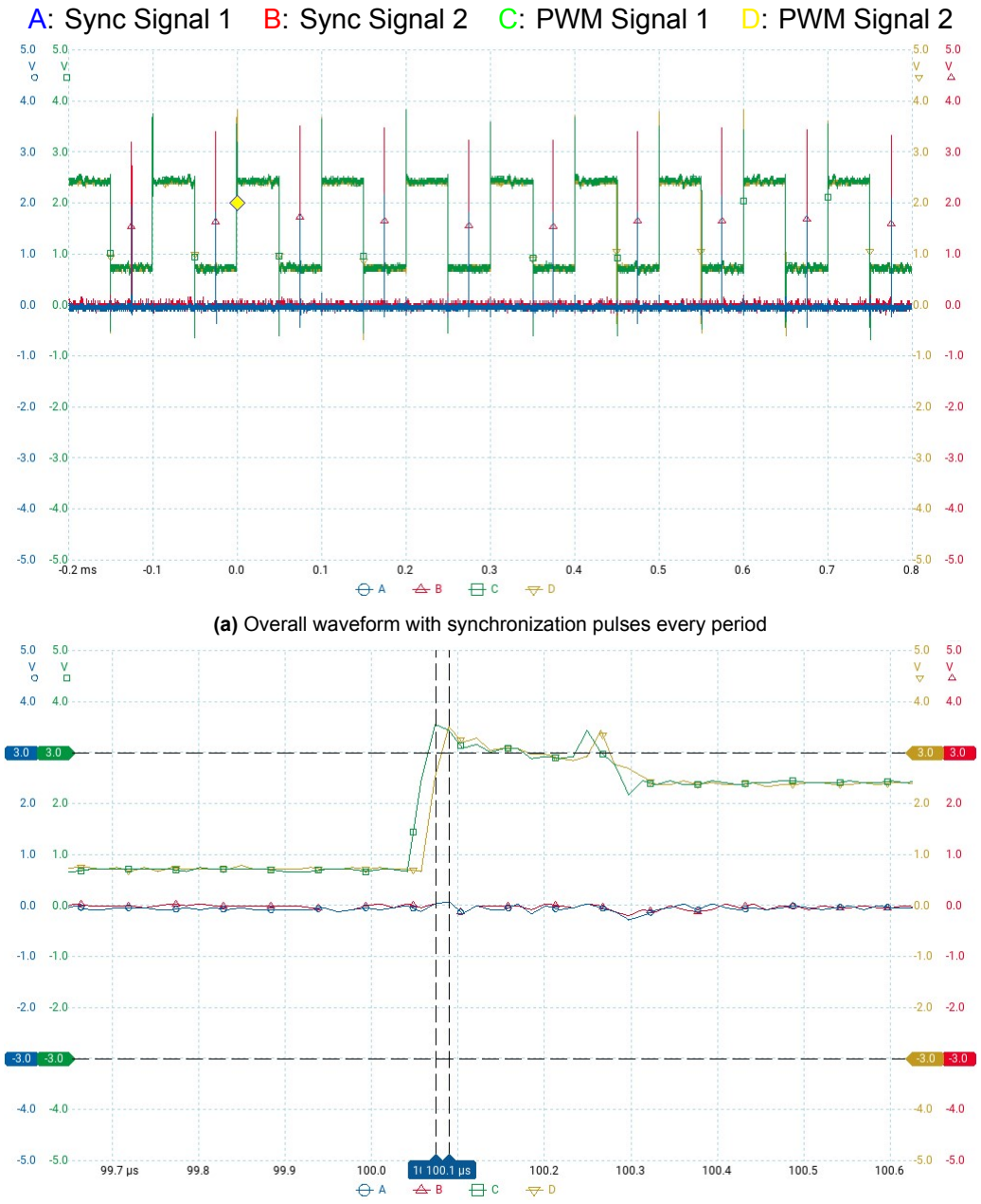
(b) Difference in PWM signals ($t_{\Delta} = 30.47ns$)

Figure 5.8: PWM signals of two cells with delay compensation

As discussed in Chapter 3, these delays can be externally measured and compensated for using software delays. However, these delays are highly dependent on the system's physical parameters, such as the length of cables connecting the inverter cells, etc. For the test setup, an overall delay of $t = 65ns$ to the synchronization trigger pulse is optimal for reducing the error between the PWM pulses.

It can be seen in Fig.5.8 that the included compensation technique reduces the error by a further value than that observed in the previous tests.

5.2.5. Synchronization with delay and drift compensations



(a) Overall waveform with synchronization pulses every period

(b) Difference in PWM signals ($t_{\Delta} = 15.24ns$)

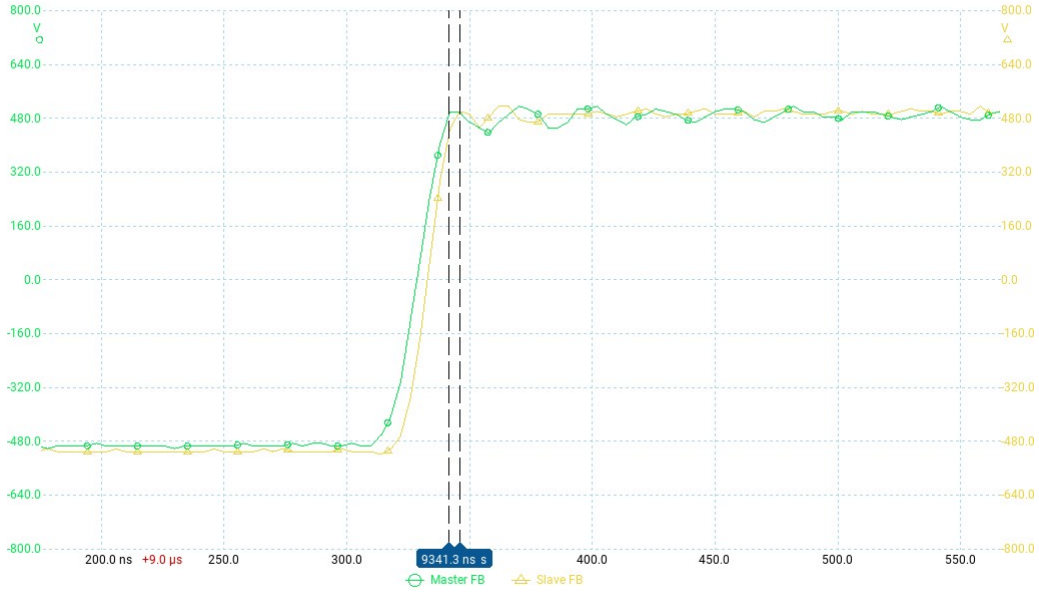
Figure 5.9: PWM signals of two cells with delay and drift compensation

Now, it was observed that the two controllers have an inherent difference in their timers. This is due to the internal oscillators' material properties and the difference in the parasitic values of the components involved. This can be understood as a drift in the timer counter and can be compensated by changing the total number of counts within a switching period. It can be seen in Fig.5.9 that this type of compensation technique reduces the error by a minimum value by eliminating all the delays and errors in the system.

5.2.6. Synchronization test with DC Bus Voltage

The above tests were conducted with an open DC bus setup to ensure safety while implementing the synchronization design. An accurate and reliable synchronization between the controllers is achieved, and a DC supply is connected at the input of the inverter board.

(a) Overall waveform with synchronization pulses at $V_dc = 500V$



(b) Difference in PWM signals ($t_\Delta = 13.57ns$)

Figure 5.10: PWM signals of two cells with synchronization

Using a similar testing setup with two inverter boards, one configured as master and the other as slave controller, the DC bus voltage is increased in steps of 50V. It was observed that a large noise was injected into the synchronization signal, which reset the slave controller's timer at undesired instants at DC input voltages above 100V. It was discovered that the cable carrying the synchronization signal was not shielded to the ground. A shielded RJ-45 cable between the controllers ensures no noise from the switching nodes into the synchronization signal.

The waveforms above show the synchronization between the two inverter cells at a DC bus voltage of 500V. A conformal coating is required on top of the PCBs to test at higher voltages to ensure sufficient clearance between the high-voltage tracks. However, the tests conducted with a 500V DC input prove the reliability of the synchronization method.

5.2.7. Findings

The conducted synchronization tests on the developed hardware prototype boards can be easily scaled to a higher number of cascaded cells. A minimum jitter of around $15ns$ to $20ns$ is observed on the test setup, a promising output for distributed controller systems in power applications. This value is further reduced as the switching frequency increases in the system as the number of steps for the counter is reduced, resulting in smaller errors.

The industry alternative, EtherCAT, promises a maximum jitter of <1μs, making the developed synchronization technique a far cheaper and more accessible system to achieve high performance. This system suffers from the disadvantage of the requirement of regular manual software compensation changes as compared to EtherCAT's hardware-based synchronized clock system, as discussed in Chapter 3. The errors in all five synchronization tests are summarised below in Table5.1.

S.No.	Sychronization Technique	Error between PWM signals
1.	No synchronization pulses	Variable (switching period)
2.	Slow Synchronization	Variable (80ns - 575ns)
3.	Fast Synchronization	$\sim$50ns
4.	Synchronization with delay compensation	$\sim$30ns
5.	Synchronization with delay & drift compensation	$\sim$15ns

Table 5.1: Comparison of Synchronization Techniques

5.3. Summary

This chapter focuses on explaining the developed hardware boards for inverter cells with a large focus on communication line design. The use of different PCBs as power modules and control boards is explained and justified. Next, the developed test setup and the importance of synchronization testing are presented.

Several synchronization techniques are implemented to reduce the error to a minimum value. The different compensations are explained and compared to achieve the final result. This result is compared to the industry-equivalent technology, EtherCAT, a costly system. However, it has several advantages, as explained in Table 3.1 compared to the developed software technique.

6

Conclusion and Future Developments

In this thesis, the design and analysis of the inverter stage and controller architecture for a modular solid-state transformer have been investigated thoroughly. The main objective of this project was to design and develop a suitable inverter stage for DC/AC power conversion, review and implement different possible modulation techniques, and design a suitable controller architecture for a modular SST. This work aims to enhance the overall integration of renewable energy sources into the grid by improving the flexibility and modularity of SSTs.

Valuable insights and significant findings in this field have been achieved through comprehensive research, simulations, and prototype development. The research on the power conversion stage focused on the overall distortion in the output, filter sizing, and switching frequency. Several simulations were performed to determine the performance of this system.

Chapter 1 introduces the need for research in the field of SSTs. It provides an overview of the thesis background and outlines the design methodology of the project. The importance of efficient power flow between DC microgrids and the AC grid is highlighted.

Chapter 2 reviews existing multilevel converter topologies and suitable modulation strategies. MMC, H-NPC, and CHB topologies are compared using several parameters to find the most suitable topology for SST inverter applications. Cascaded H-Bridge is the most suitable topology based on several factors, such as cost, complexity, and modularity. Types of sinusoidal PWMs and space vector PWM concepts are introduced concerning multilevel inverters. Based on the application, space vector PWM is the most optimal strategy for THD content and common-mode voltage optimization but needs further implementation to suit multilevel converters. PS-SPWM is an efficient alternative in applications prioritizing switching frequency and filter sizing.

Chapter 3 investigates the need for controller architecture design. A modular and efficient system is designed primarily focusing on parameters such as synchronization jitter, communication bus, and scalability. Several communication protocols are reviewed, and their features are compared to design a complete model of controller architecture for the solid-state transformer. SPI and EtherCAT emerge as the most applicable protocols, but SPI with daisy-chain topology is used concerning the added cost and complexity for EtherCAT controllers. An effective synchronization technique is developed using the trigger function of microcontrollers, which is tested in further chapters.

Chapter 4 illustrates the followed inverter design and simulation results. The output filter and inverter control designs are explained. The implemented space vector algorithm for thirteen-level inverters is explained, and THD results from the simulation model are compared with those from SPWM models. It was observed that the developed SVPWM technique, *Reduced-level hexagon tracking for 13-level converter* resulted in an overall THD content of 4.1%, similar to that of LS-SPWM with similar input parameters. The implemented multilevel space vector algorithm can be further optimized for applications requiring a common mode voltage reduction. Space vector modulation helps achieve this by utilizing the available switching states. However, the maximum modulation index is limited in these kinds of applications.

In this application, the modulation index cannot be limited below $m = 1.54$ to ensure 10kV AC grid compatibility. PS-SPWM showed superior performance due to an increased output frequency, resulting in 3.4% with a much lower filter at the output, making it the efficient technique for this application.

Chapter 5 focuses on the hardware design and considerations taken into account for the hardware prototype. The proposed controller design is primarily tested for synchronization. It demonstrated exceptional performance with a synchronization jitter of less than 20ns under bench testing. This opens a huge scope for overall controller development for modular SST systems.

The following research questions were answered during this thesis project:

1. **Which topology is best suited for a medium voltage DC/AC converter in a solid-state transformer (SST)?**

   Several converter topologies are investigated for DC/AC converter applications. The most popular multilevel converter topologies are compared based on modularity, efficiency, complexity, cost, and voltage capability. It was concluded that CHBs are simpler and easier to implement among these selected topologies.

2. **What are the different modulation techniques for multi-level grid-connected power converters and how to implement them?**

   Modulation strategies play an important role in maximizing the potential of multilevel converters. Several strategies exist for multilevel converters that allow for reducing the harmonic content in the output waveforms. Sinusoidal and space vector PWM techniques are compared for this specific application. An innovative space vector algorithm is implemented for application in multilevel converters. The phase-shifted SPWM technique proved to be the most suitable modulation technique that helps reduce the harmonic content and output filter size.

3. **What is a suitable control architecture for a modular solid-state transformer (SST), and how to design it?**

   Modern power converters include a large number of modules connected. The development of the controller architecture is a key aspect of modular SSTs. A flexible and efficient distributed controller architecture design is required to ensure a reliable and synchronous operation. To ensure this operation, a modular and distributed controller architecture is designed and implemented with an SPI-based communication bus and custom synchronization technique to help overcome various delays in the system. These

control aspects were integrated into the system to enable high output voltage quality, seamless data transfer between cells, and fault detection.

6.1. Implications and Future Directions

The successful design and implementation of the inverter stage prototype and controller architecture testing results ensure the significant advancement of power distribution systems. The modular SST system designed as part of this thesis presents a promising avenue for future energy grids, offering improved flexibility, scalability, and integration of renewable energy sources. The review work on inverter topology and modulation techniques, including the developed space vector algorithm for higher-level inverters, opens up a strong avenue for further research and development in the field of DC/AC power conversion stages.

The controller architecture established in this study can serve as a foundation for modular power systems of the future. Several algorithms and improved synchronization techniques can be researched and implemented using a similar design process. As technology evolves, several avenues exist for future research and refinement. Using this thesis as a reference, some of these developments can include:

1. **Modular Space Vector Algorithm -** The space vector algorithm developed in this thesis can be further developed and modified to achieve optimal switching patterns and reduced common mode voltages in lower modulation index applications. This requires a modification of the algorithm and an understanding of the exact switching sequences in every sector. Furthermore, the algorithm is specifically developed for thirteen-level inverters. To make this aspect of the system completely modular, it can be modified to apply to any number of levels.

2. **Thermal Design -** A detailed thermal analysis would help achieve optimal design of the inverter stage. A detailed comparison between aluminum PCBs and the commonly used FR-4 PCBs regarding thermal and electrical performance can be performed. This work can also help understand the maximum capability of the chosen power electronic switches for the SST.

3. **Controller Architecture -** The designed controller architecture and synchronization techniques demonstrate a good performance but can be further developed to suit various applications. Firstly, further research can be conducted to reduce the dependence on software-based synchronization, which is manual and not completely reliable. Hardware-based techniques, such as the one used in EtherCAT or the possibility of PLL-based clock synchronization, can be investigated. Also, more testing for fault and the converter's various operating conditions can be performed, providing insights into developing a better control system.

In conclusion, the design and implementation issues of the inverter stage and controller architecture for a modular solid-state transformer were addressed successfully in this master thesis. The proposed solutions have demonstrated remarkable performance through a comprehensive approach followed in this thesis, including theoretical analysis, simulation studies, and experimental validation, contributing to improving power distribution systems. The research findings from this project will serve as a stepping stone for future solutions in optimizing the issues associated with integrating renewable energy sources into the grid. This ultimately results in a clean and efficient power system for the world.

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A

Space Vector Algorithm

```
1
2  Vg_ll_rms = 10000;
3  % Vg_ll_rms = 11870;
4  Vg_rms = Vg_ll_rms/sqrt(3);
5  Vg_peak = Vg_rms*sqrt(2);
6  fac = 50;
7  Vdc = 1400;
8  fs = 10000;
9  Ron = 0.16;
10
11 Rd = 10;
12 Rc = 1e-3;
13 Rg = 1e-3;
14 Lg = L2;
15 Don = 0.01;
16 % P_ref = 100000;
17 Rl = 1000;
18 Ll = 0;
19 % Ll = 1e-4;
20
21
22 tol = 1e-10;
23 vd = Vdc; %Input voltage to each H-bridge
24
25 va_no = [6 5 4 3 2 1 0 -1 -2 -3 -4 -5 -6]; % Switching states of each phase of the
       CHB
26 vb_no = [6 5 4 3 2 1 0 -1 -2 -3 -4 -5 -6];
27 vc_no = [6 5 4 3 2 1 0 -1 -2 -3 -4 -5 -6];
28
29 va = va_no*vd; %Phase Voltage of each leg of CHB
30 vb = vb_no*vd;
31 vc = vc_no*vd;
32
33 for p = 1:13 %Generate all switching combinations in 3-dimensional array
34     for q = 1:13
35         for r = 1:13
36             van(p,q,r) = va(p); %converter side phase voltage
37             vbn(p,q,r) = vb(q);
38             vcn(p,q,r) = vc(r);
39         end
40     end
41 end
42
```

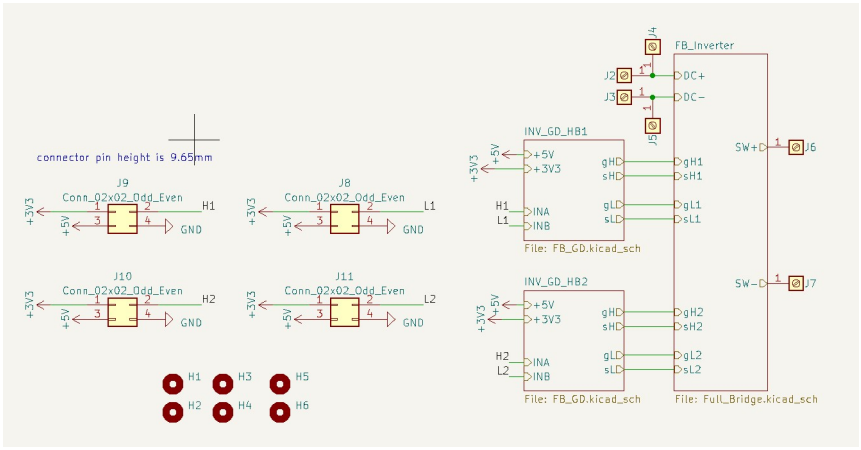
```
van_sw = reshape(van, 2197, 1); %3-dimensional to column vector
vbn_sw = reshape(vbn, 2197, 1);
vcn_sw = reshape(vcn, 2197, 1);

v_abc_sw1 = [van_sw vbn_sw vcn_sw]; %3 column vectors defining all states

vr_sw = (2/3)*(van + (vbn*exp(2*1j*pi/3)) + (vcn*exp(4*1j*pi/3))); %Clark tranform
    to generate switching positions in alpha-beta
vr_sw = round(reshape(vr_sw, 2197, 1), 2); %3-dimensional to column vector
vr_sw_pol = round([abs(vr_sw) angle(vr_sw)], 4); %rectangular to polar form


v_abc_sw2 = round([v_abc_sw1 vr_sw vr_sw_pol vr_sw_pol(:,2)/pi vr_sw_pol(:,2)*180/
    pi], 2); % Adding more columns with angle in degrees

v_sw_angles = v_abc_sw2(:, 8); %Extracting angles in degrees


hex7cen_all = v_abc_sw2(abs(v_abc_sw2(:,5)-(2*6*vd/3)) < tol, :); %Finding the
    centre of each 7 level hexagon by comparing all magnitudes in each hexagon with
     6000 (mid-point)

hex71cen = hex7cen_all(abs(hex7cen_all(:,8)-0) < tol, :); %Restricting it to 0
    degrees to eliminate the centres on the edges
hex72cen = hex7cen_all(abs(hex7cen_all(:,8)-60) < tol, :);
hex73cen = hex7cen_all(abs(hex7cen_all(:,8)-120) < tol, :);
hex74cen = hex7cen_all(abs(hex7cen_all(:,8)-180) < tol, :);
hex75cen = hex7cen_all(abs(hex7cen_all(:,8)+120) < tol, :);
hex76cen = hex7cen_all(abs(hex7cen_all(:,8)+60) < tol, :);

hex7cen = [hex71cen;hex72cen;hex73cen;hex74cen;hex75cen;hex76cen]; %Combining the
    above centres into a single matrix

[h7, ihex7] = unique(hex7cen(:, 8), 'stable'); %Finding single positions of
    centres using angle uniqueness
hex7centres = round(hex7cen(ihex7,:),2);

hex13centre(1:6, :) = 0+0j;
hex13centre = complex(hex13centre); %Mid-point of 13 level diagram

transform1(:, 1) = v_abc_sw2(:, 4) - hex7centres(1,4); %Finding new vectors from
    mid-point of 7 level hexagon - 1
dist_71 = abs(transform1(:,1)); %Finding the magnitude of the new vectors
dist_71 = round(dist_71, 2);

hex41cen =  v_abc_sw2(dist_71(:,1) == (2*3*vd/3), :); %Finding vectors which are
    3000 magnitude away from centre of 7 level hexagon - 1
[h4, ihex4] = unique(hex41cen(:, 4), 'stable');%Finding single positions of
    centres using vector uniqueness
hex4centres = hex41cen(ihex4,[1:4]);
hex4centres = hex4centres(:,4) - (2*6*vd/3); % Finding the general 4 level hexagon
     centres that can be added to any 7 level hexagon

hex4centres([1 6]) = hex4centres([6 1]); %Rearranging to go from 1 to 6 in anti-
    clockwise direction
hex4centres([2 5]) = hex4centres([5 2]);
hex4centres([4 6]) = hex4centres([6 4]);
%%

hex2incen = round(v_abc_sw2(round(abs((2*9*vd/3)+0i - v_abc_sw2(:, 4)), 2) ==
    round(2*vd/3, 2), [1:4]), 2); %Finding vectors which are 1000 magnitude away
```

```
    from centre of 4 level hexagon - 1
[h2i, ihex2i] = unique(hex2incen(:, 4), 'stable');
hex2incentres = hex2incen(ihex2i,:);
hex2incentres = round(hex2incentres(:,4) - ((2*9*vd/3)+0i), 2); % Finding the
    general 2 level inner hexagon centres that can be added to any 4 level hexagon
hex2incentres([1 6]) = hex2incentres([6 1]);
hex2incentres([2 5]) = hex2incentres([5 2]);
hex2incentres([4 6]) = hex2incentres([6 4]);

hex2outacen = round(v_abc_sw2(round(abs((2*9*vd/3)+0i - v_abc_sw2(:, 4)), 1) ==
    round(2*2*vd/3, 1), [1:8]), 2); %Finding vectors set a which are 2000 magnitude
     away from centre of 4 level hexagon - 1
[h2oa, ihex2oa] = unique(hex2outacen(:, 4), 'stable');%Finding single positions of
     centres using vector uniqueness
hex2outacentres = hex2outacen(ihex2oa,:);
hex2outacentres = round(hex2outacentres(:,4) - ((2*9*vd/3)+0i), 2); % Finding the
    general 2 level inner hexagon centres that can be added to any 4 level hexagon

hex2outbcen = round(v_abc_sw2(round(abs((2*9*vd/3)+0i - v_abc_sw2(:, 4)), 1) ==
    round(1.732050808*2*2*vd/(3*2), 1), [1:4]), 2); %Finding vectors set b which
    are 2000 magnitude away from centre of 4 level hexagon - 1
[h2ob, ihex2ob] = unique(hex2outbcen(:, 4), 'stable');%Finding single positions of
     centres using vector uniqueness
hex2outbcentres = hex2outbcen(ihex2ob,:);
hex2outbcentres = round(hex2outbcentres(:,4) - ((2*9*vd/3)+0i), 2); % Finding the
    general 2 level inner hexagon centres that can be added to any 4 level hexagon

hex2outcentres = [hex2outacentres ; hex2outbcentres]; %Set of all 2 level outer
    hexagons
hex2outcentres([1 6]) = hex2outcentres([6 1]);hex2outcentres([2 12]) =
    hex2outcentres([12 2]);hex2outcentres([3 5]) = hex2outcentres([5 3]);
    hex2outcentres([4 10]) = hex2outcentres([10 4]);hex2outcentres([6 8]) =
    hex2outcentres([8 6]);hex2outcentres([7 8]) = hex2outcentres([8 7]);
    hex2outcentres([9 12]) = hex2outcentres([12 9]);hex2outcentres([10 12]) =
    hex2outcentres([12 10]);hex2outcentres([12 11]) = hex2outcentres([11 12]);

hex2centres = [hex2incentres; hex2outcentres]; %Set of all 2 level hexagon centres

for p = 1:6
    for q = 1:6
        allhex4centres_cell{q,p} = complex(hex7centres(p,4) + hex4centres(q,1)); %
            Calculating all hex4centres in order
    end
end
allhex4centres = cell2mat(allhex4centres_cell); %cell to mat form conversion

for p = 1:6
    for q = 1:6
        for r = 1:18
            allhex2centres_cell{r,q,p} = complex(allhex4centres(q,p) + hex2centres
                (r,1)); %Calculating all hex2centres in order
        end
    end
end
allhex2centres = cell2mat(allhex2centres_cell); %cell to mat form conversion
```

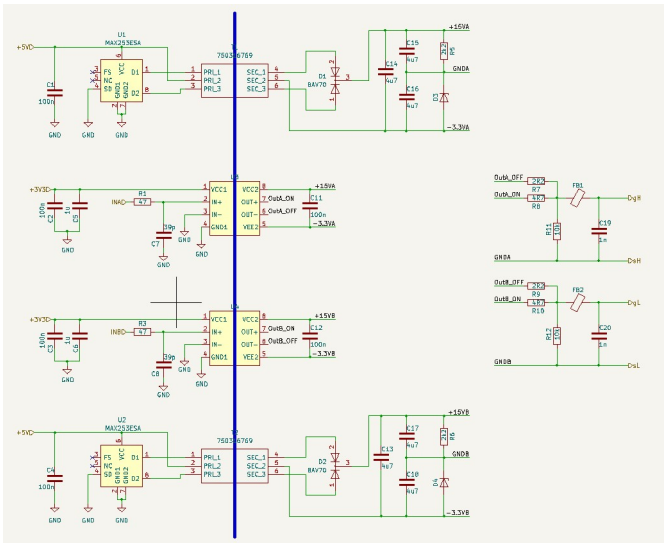
B

Printed Circuit Board

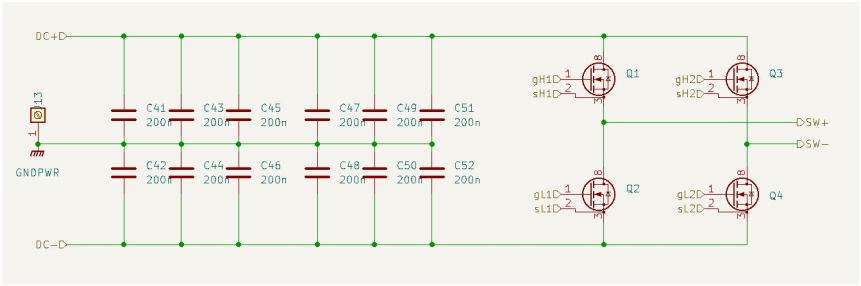
B.1 Schematic and layout of full-bridge aluminum power board



(a) Sheet - 1



(b) Sheet - 2



(c) Sheet - 3

Figure B.1: Schematic of Full-Bridge Aluminum Power Board

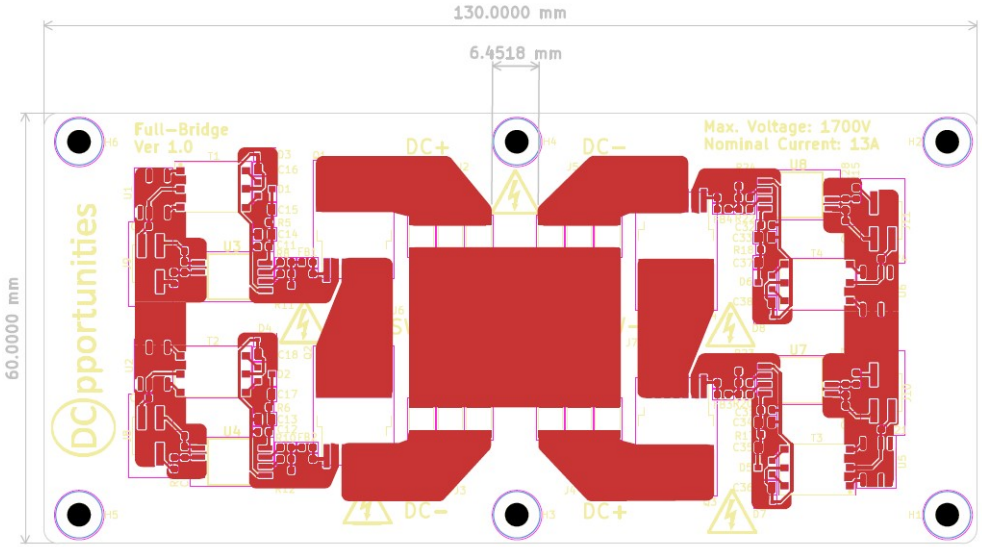


Figure B.2: Layout of Full-Bridge, 1-layer Aluminum Power Board

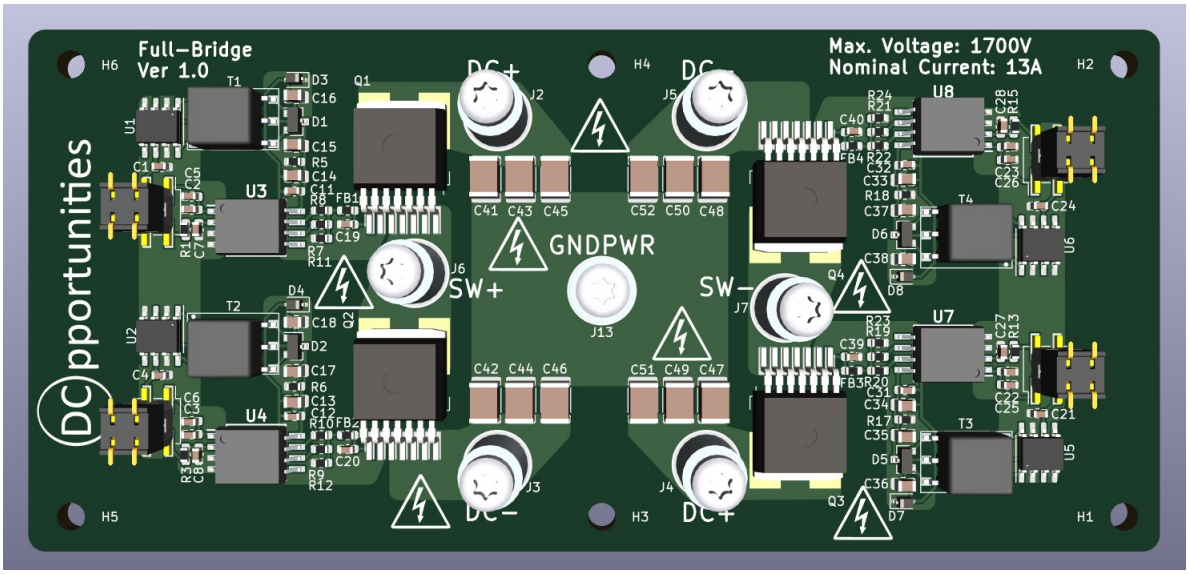


Figure B.3: 3D View of Full-Bridge Aluminum Power Board

B.2 Schematic and layout of SST Secondary board

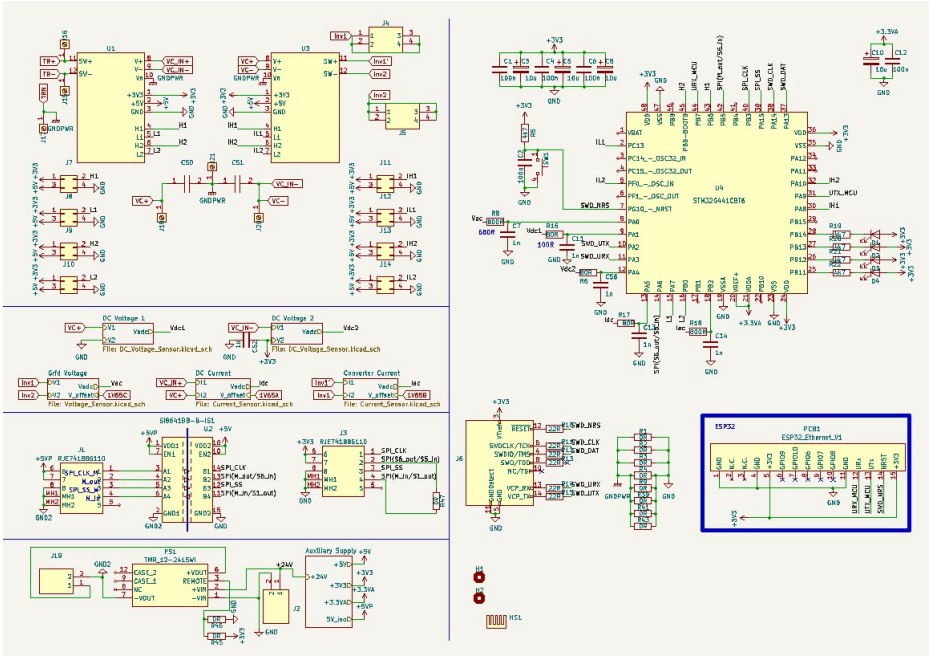


Figure B.4: Schematic of SST Secondary board

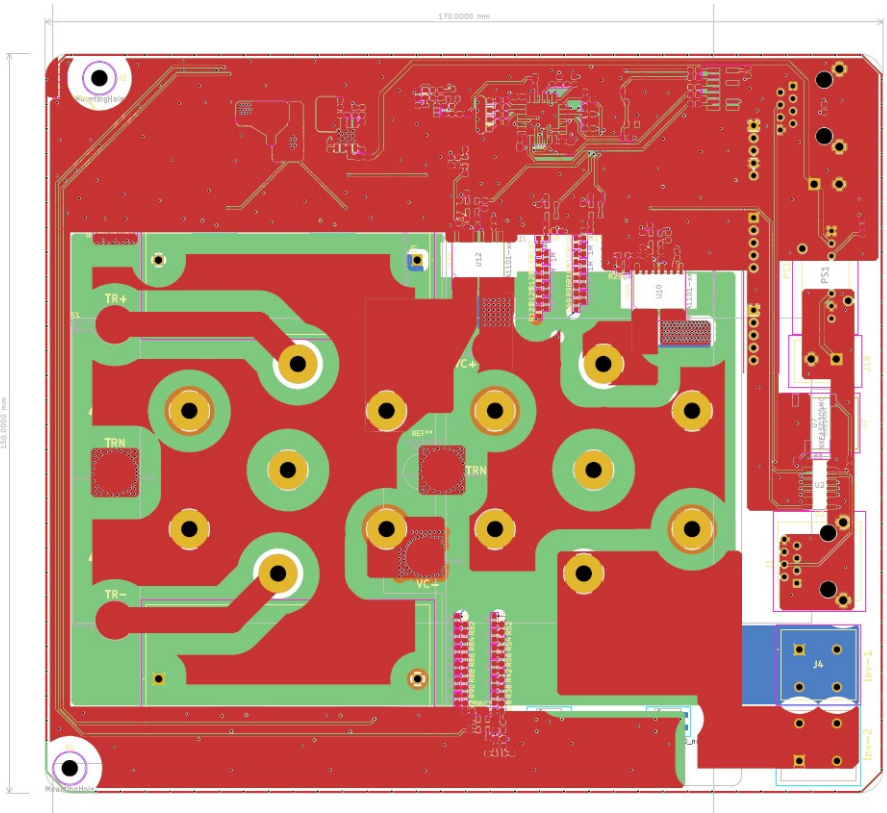


Figure B.5: Layout of SST Secondary board

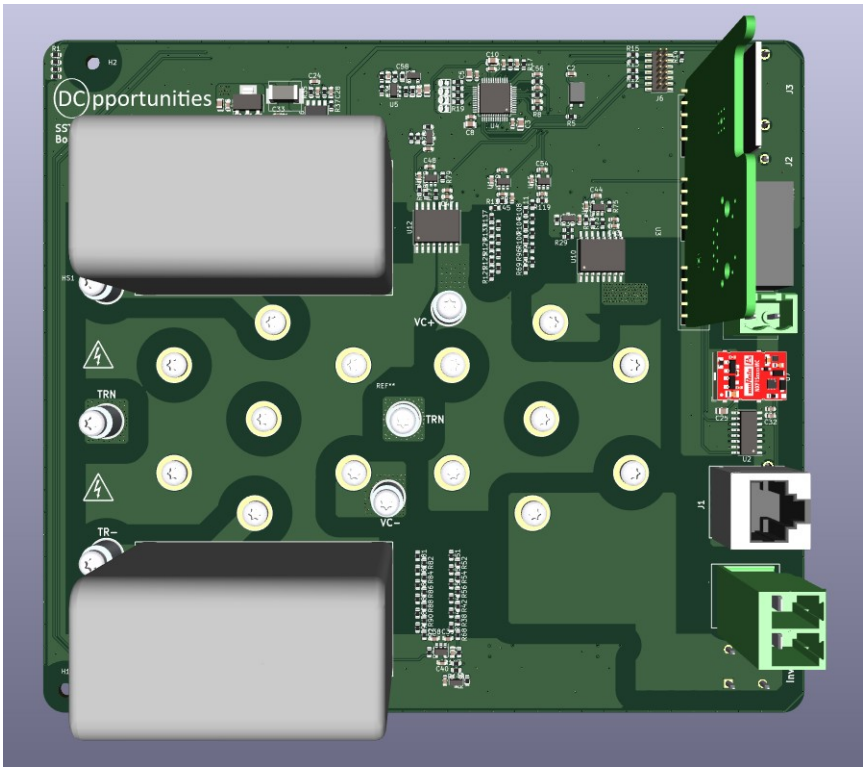


Figure B.6: 3D View of SST Secondary board

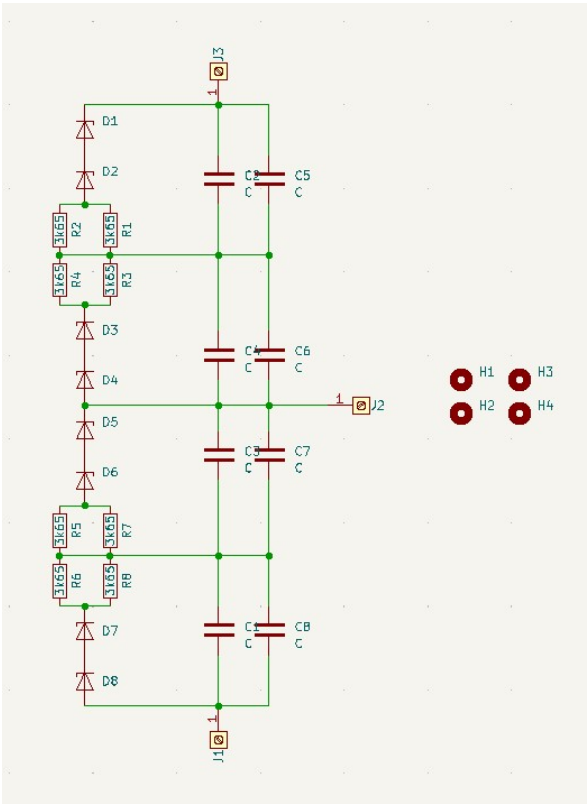


Figure B.7: Schematic of DC-Link Capacitor Board

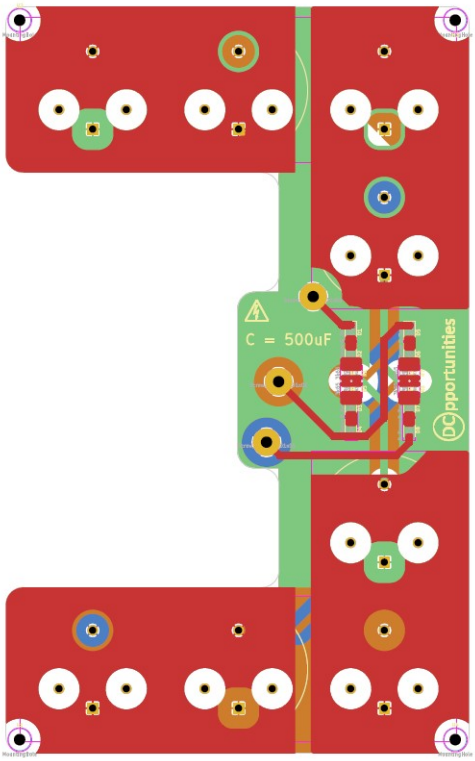


Figure B.8: Layout of DC-Link Capacitor Board

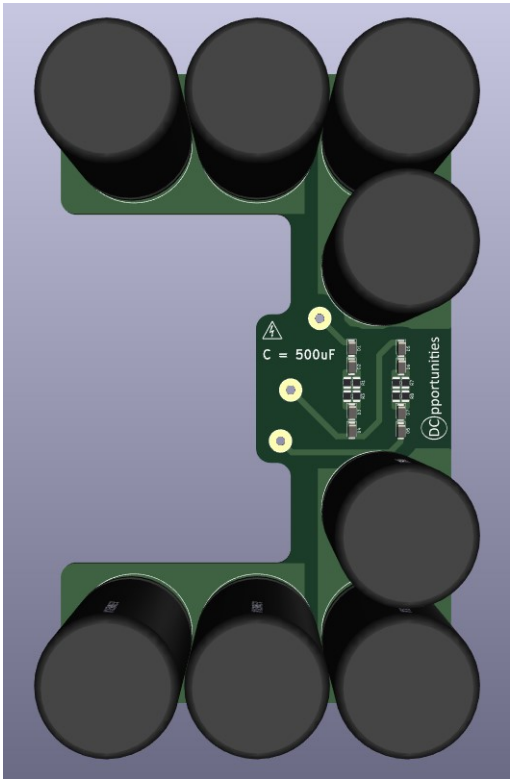


Figure B.9: 3D View of DC-Link Capacitor Board