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A 77/79-GHz Frequency Generator in 16-nm CMOS for FMCW Radar Applications Based on a 26-GHz Oscillator with Co-Generated Third Harmonic

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Abstract—This paper presents a digitally controlled frequency generator for dual frequency-band radar system that is optimized for 16 nm FinFET CMOS. It is based on a 21% wide tuning range, fine-resolution DCO with only switchable metal capacitors. A third-harmonic boosting DCO simultaneously generates 22.5–28 GHz and sufficiently strong 68–84 GHz signals to satisfy short-range radar (SRR) and medium/long range radar (M/LRR) requirements. The 20.2 mW DCO emits -97 dBc/Hz at 1 MHz offset from 77 GHz, while fully satisfying metal density rules. It occupies 0.07 mm^2 , thus demonstrating both 43% power and 47% area reductions. The phase noise and FoM_T (figure-of-merit with tuning range) are improved by 1.8 dB and 0.2 dB, respectively, compared to state-of-the-art.

Index Terms—Phase noise, DCO, oscillator, harmonic boost, common mode, FMCW, tuning range, automotive radar, 77 GHz

I. INTRODUCTION

With the latest promises of autonomously driven vehicles, automotive radar applications expect great commercial interests. Among the advanced radar systems, the E-band frequency range (76 GHz to 81 GHz) is the most commonly used. To achieve ubiquitous sensing with fine resolution in short/medium/long range radar (SRR/MRR/LRR) applications, high signal-to-noise ratio (SNR) and large chirp bandwidth are necessary. The demands they place on monolithic frequency synthesizers are particularly tough, especially on low power consumption, low phase noise (PN) and wide tuning range (TR) with good linearity.

Oscillators and high-frequency dividers are the key challenges in the radar PLL design. A 77/79-GHz PLL architecture employs a mm-wave oscillator, which feeds both a mm-wave frequency divider back for a phase detection with a frequency reference clock, and a power amplifier (PA) to drive an antenna [1]. The oscillator PN is severely affected by a poor Q-factor of the resonant tank at 77 GHz. The dividers are typically power hungry and occupy large silicon area, and suffer from limited locking range. The frequency doubler/tripling PLL [2][3] relieves the aforementioned design challenges but shifts them to the frequency doubler or injection-locked frequency tripler (ILFT), so the solution-level issues remain.

To alleviate the above challenges of radar oscillators and dividers with minimum impact on other circuitry, a mm-wave radar LO with an implicit $3\times$ multiplier is proposed here.

II. CANCELLATION OF FUNDAMENTAL OF OSCILLATOR

The basic concept of the presented idea (continuation of our earlier work for 60 GHz [8] [9]) is that the oscillator

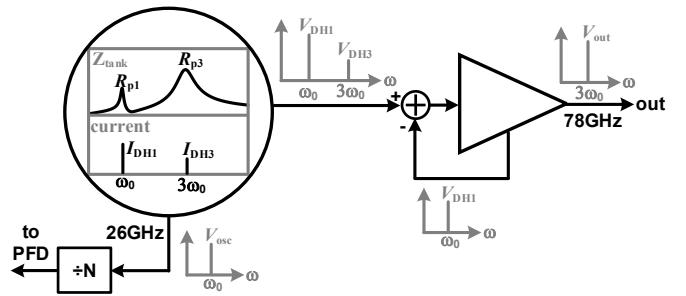


Fig. 1. Working principle of the proposed 77/79 GHz frequency generator with the sub-harmonic soft-cancellation buffer.

simultaneously generates the *fundamental* at 22.5–28 GHz and its 3rd harmonic at 68–84 GHz. The E-band radar carrier is fed forward to the buffer/PA, while the 23–28 GHz signal is fed back for phase detection (e.g. TDC in an ADPLL). Consequently, the implicit $3\times$ divider functionality is inherent with the oscillator thus avoiding any physical divider operating at the E-band carrier. This leads to a dramatic increase of the system-level efficiency.

However, the ~ 26 GHz fundamental harmonic must be suppressed in the buffer that follows the PLL. Otherwise, it can degrade the blocker tolerance of the radar receiver or even violate the emission mask in the transmitter. Hence, the feed-forward path should exhibit strong suppression of the 26 GHz tone. In this work, a soft cancellation technique of the 26 GHz component is employed. Effectively, the buffer/PA does not actively respond to the 26 GHz component input. It rejects the 26 GHz fundamental by not providing a transconductance gain at this frequency.

For the PLL to cover the overall SRR/MRR/LRR radar requirements (24–28 GHz, 75–81 GHz), the DCO core should support a wide TR. Therefore, there are 5-bit binary PVT switched capacitors for coarse tuning, and 32-bit unary MSB and 64-bit unary LSB switched capacitors for fine tuning. This ensures the DCO core can cover full E-band frequency range with acceptable PN performance. Moreover, in the ADPLL design for radar applications, the strictest requirements are PN and power consumption. Thus, the DCO design is very critical since it dominates the ADPLL out-of-bandwidth performance.

III. CIRCUIT IMPLEMENTATION

The schematic and layout of the DCO are shown in Fig. 2(a)(b). To meet the strict PN and wide TR requirements,

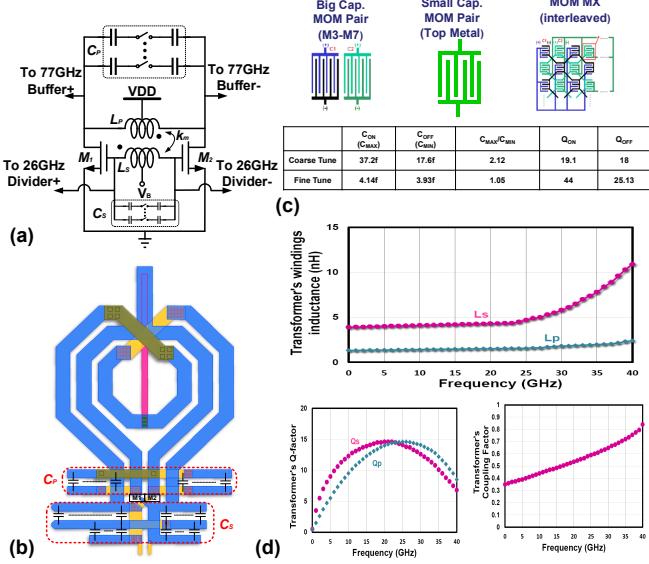


Fig. 2. (a) Schematic of the 77/79 GHz DCO; (b) Concept layout of the DCO; (c) single/multi-layer MoM capacitors and transformer effects with dummy metal fills on the 16 nm FinFET CMOS.

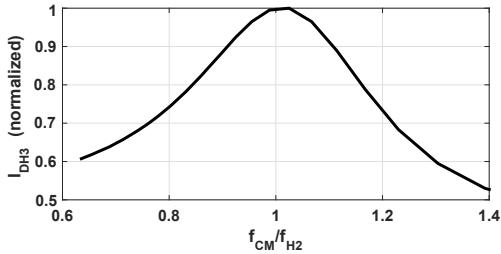


Fig. 3. Dependency of the H3 current in DCO on the CM resonant frequency. CM resonance at the second harmonic increases the third harmonic content.

it is of utmost importance to optimize the quality (Q) factors of transformer and switched capacitors.

In this design, several new process and circuit techniques are exploited to enhance the PN: First, porting of the oscillator design from 40-nm & 28-nm CMOS ([8] [9]) to 16-nm FinFET CMOS has contributed to a lower power consumption and faster speed [10]. Second, use of custom single/multiple-layer MOM capacitors and a transformer with interleaved routing has reduced parasitic capacitance and mismatch, thus obtaining a better Q factor, as shown in Fig. 2(c)(d). Third, the DCO circuitry undergoes a large signal operation. A current *richer* (due to higher g_m) in harmonics is generated in the g_m -devices (M_1 and M_2). The 3rd harmonic (H3) current in the 26 GHz DCO is reused for implicit frequency tripling. Leveraging the readily existing harmonic current in the DCO for frequency multiplication improves the power efficiency. In order to preserve the 3rd harmonic inside the oscillator, a transformer-based higher-order LC tank is employed to create an ancillary resonance at H3. To achieve a large H3 voltage swing in the DCO, a relatively small magnetic coupling coefficient (k_m) of 0.6 is applied to achieve large tank impedance at this ancillary resonance.

To further increase the H3 swing, the H3 current is also boosted by enhancing the harmonic mixing effects in the DCO.

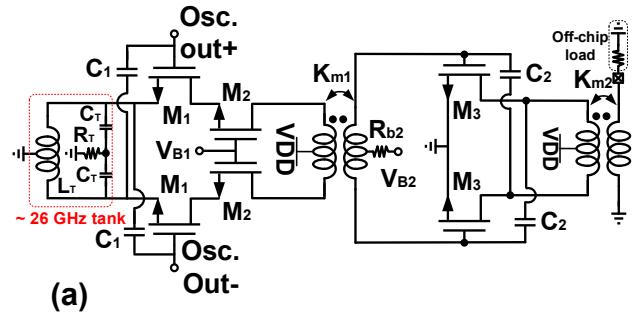


Fig. 4. (a) Schematic of 77/79 GHz buffer with 26 GHz suppression; (b) Concept layout of buffer.

The common-mode (CM) impedance of the LC tank affects the level of H3 current. Fig. 3 shows the dependency of the simulated H3 current on the CM resonant frequency (f_{CM}). As we can see, the H3 current is maximized when f_{CM} equals to the 2nd harmonic (H2) frequency (f_{H2}). Therefore, the CM impedance of the LC tank is tuned to resonate at f_{H2} by properly segmenting the differential and single-ended tank capacitance. In this way, the H2 voltage swing, which is preserved by the H2 resonance, mixes with the fundamental voltage component in the negative g_m -devices of the DCO and delivers more H3 current. This technique can also improve the $1/f^3$ noise corner. Simulations show that the H3 voltage swing is 40% of the fundamental in the oscillator. It relaxes the requirement on the following DCO buffer.

Both the fundamental and H3 components in the DCO are fed forward to the buffer stage. Ideally, the buffer would only react to the H3 component, while discarding the fundamental component. To achieve this goal, a fundamental component cancellation technique is implemented in this design, as shown in Fig. 4. An LC tank is connected to the sources of the input devices (M_1). It exhibits a large impedance at the fundamental by means of parallel resonance at this frequency, while providing a very low impedance at H3. Therefore, the buffer acts as a common-source amplifier at H3, but with heavy degeneration at the fundamental. In other words, M_1 senses only the H3 component between its gate and source (i.e., v_{gs}). The fundamental component is therefore rejected. It also provides more gain to the signal of interest at 77 GHz. It is well known that a large blocker signal can desensitize the low-noise amplifiers (LNAs) in the receivers. The large 26 GHz tone herein could also desensitize the conventional 77 GHz buffers in a similar way. Since the 26 GHz 'blocker' is rejected before reaching the input transistors of the proposed 77 GHz buffer, it will not degrade the 77 GHz signal gain. As

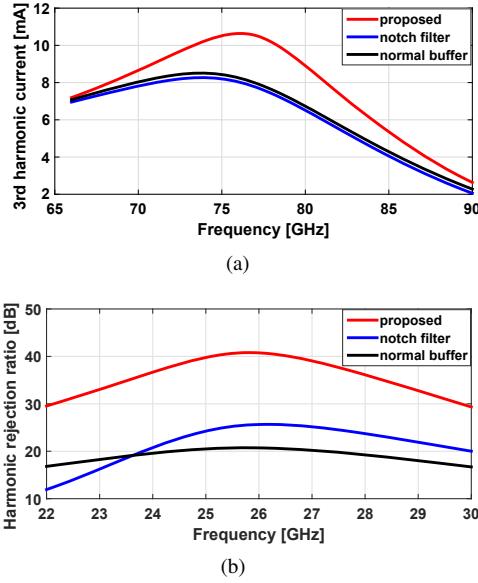


Fig. 5. Comparison of (a) the output current at 77 GHz band and (b) harmonic rejection ratio at 26 GHz band in different buffers.

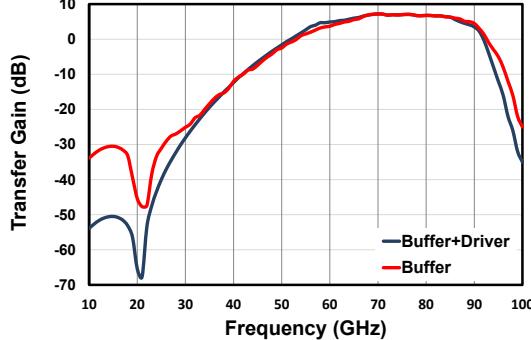


Fig. 6. Simulated transfer curves of the buffer stage and output driver.

shown in Fig. 5, the proposed buffer delivers the largest output current at 77 GHz band and achieves the highest harmonic rejection ratio at 26 GHz when compared to the notch filter and conventional buffers. The reduction of the fundamental component in v_{gs} of M_1 also decreases the H2 component at the buffer output, which can result from the nonlinear distortion of the fundamental tone or harmonic mixing effects. One extra output driver stage is added in this design to drive the external 50Ω load and to deliver sufficient output power. Low k_m coefficient ($k_{m1}=0.25$) is used to achieve wideband interstage matching. Fig. 6 shows the simulated transfer curve of the buffer stage and output driver.

IV. MEASUREMENT RESULTS

The proposed 77/79 GHz frequency generator is prototyped in 16 nm FinFET CMOS. Fig. 10 shows the chip micrograph. It occupies a core area of 0.07 mm^2 . The phase noise (PN) and spectra of the generated E-band carrier are directly probed. 3 GHz outputs of the frequency dividers can also be conveniently monitored.

The 77/79 GHz DCO performance was measured using R&S FSW signal and spectrum analyzers with an external harmonic mixer (up to 90 GHz). The tuning range (TR) of

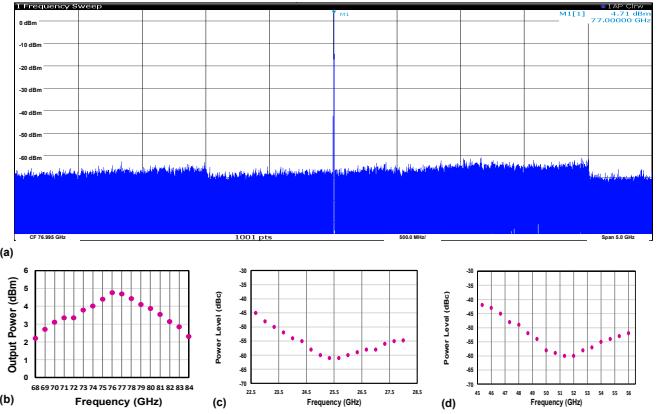


Fig. 7. Measured spectra at: (a)(b) 77 GHz with sweep of the band, (c) 25.6 GHz with the band sweep; and (d) 51.3 GHz with the band sweep.

the DCO is 68–84 GHz (21%), covering all radar channels with sufficient margin. The oscillator core consumes 10 mW from a 0.85 V supply. In this design, the 77/79 GHz buffer and 50Ω load driver stage deliver a maximum of +6 dBm power while consuming 10.2 and 15 mW, respectively. The measured leakage of the ~ 25.6 GHz fundamental is -61 dBc. Due to the common-mode leakage from the oscillator and nonlinearity of the driver, the second harmonic at 51.3 GHz is visible at -60 dBc. The leakage power level of the fundamental and second/third-harmonic tone at the output across the TR varies only 16 dB, 18 dB and 2.57 dB, as shown in Fig. 7. The fundamental and second/third-harmonic power levels satisfy the out-of-band emission mask with sufficient margin.

The PN of the free-running 77/79 GHz DCO are measured after the on-chip $\div 8$ frequency dividers and normalized to the 77 GHz carrier, as shown in Fig. 8. A record-low $1/f^3$ corner of 200 kHz for an automotive radar oscillator is observed. The PN referred to the 77 GHz and 3.2 GHz carriers are -97 dBc/Hz, -125 dBc/Hz at 1 MHz offset, respectively.

Fig. 9 shows the PN at 1 MHz offset and the corresponding FoM across the 21% TR. The PN varies between -96 and -97.5 dBc/Hz. The corresponding FoM changes between 180.4 and 181.8 dBc/Hz across the frequency range. Since the switched capacitors have lower Q-factor in the on-state, the FoM at lower frequencies decreases.

The performance of the proposed LO is summarized and compared to state-of-the-art 77/79 GHz and mm-wave oscillators in Table I. The FoM and FoM_T are 181.6 dB and 188.1 dB at 1 MHz offset, respectively. The FoM is 2dB better than the prior record in [8] [9] with different CMOS process nodes and frequency band.

V. CONCLUSION

We presented a 77/79-GHz frequency generator implemented in 16-nm FinFET CMOS intended for automotive radar applications. It consists of a proposed third-harmonic digitally controlled oscillator (DCO) with a buffer rejecting its fundamental. It further utilizes custom single layer/multi-layer MoM switched-capacitors to achieve good matching, high quality factor and wide tuning range. The DCO and buffer core occupy 0.07 mm^2 , while consuming 20.2 mW from a 0.85-V supply. The DCO satisfies the -97 dBc/Hz PN at 1 MHz offset over the full E-band range.

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART 77/79 GHZ OUTPUT OSCILLATOR SYSTEMS AND OUR PRIOR WORK IN OLDER TECHNOLOGY [8].

| | | This work | JSSC'18 [3] | JSSC'18 [4] | JSSC'18 [5] | TMTT'13 [6] | JSSC'16 [8] |
|-------------------------------------|---------------------------|-----------------|-------------------|----------------------|----------------|-------------------|----------------|
| CMOS Technology | 16nm FinFET | 65nm | 65nm | 130-nm BiCMOS | 65nm | 40nm | |
| Supply Voltage (V) | 0.85 | 1/2.5 | 1 | 1.3-2.7 | 1.2 | 0.7/1 | |
| Type | HM extract & cancellation | Freq. doubler | fundamental | frequency multiplier | fundamental | HM extract | |
| Tuning Range (GHz) | 68-84 (21%) | 77-78.83 (2.3%) | 67.8-81.4 (18.2%) | 75-83 (10.1%) | 75-78 (15.5%) | 48.4-62.5 (25.4%) | |
| PN (dBc/Hz) | 1MHz | -97 | -81.7 | -96 | -97 | -85.1 | -100.1 |
| | 10MHz | -117.2 | NA | -116.5 | -120 | -110** | -122.3 |
| FoM (dBc/Hz) | 1MHz | 181.6 | 165.1 | 179.7 | 168.2 | 170.6 | 179.8 |
| | 10MHz | 181.8 | NA | 180 | 171.2 | 175.5 | 182 |
| FoM_T (dBc/Hz) | 1MHz | 188.1 | 152.4 | 174.5 | 168.3 | 170.7 | 187.9 |
| | 10MHz | 188.3 | NA | 175 | 171.3 | 175.6 | 190.1 |
| Power (mW) | Osc. | 10 | 26.8 | 25 | 470** | 6.8 | 13.5 |
| | Buf. | 10.2 | | | | 9.6 | 22 |
| | Divider | 2.47* | | | | 10.8 | NA |
| Active Area (mm²) | 0.07 | 0.2 | 0.06 | 0.72** | 0.09** | 0.1316 | |

* Power consumption of the ~25 GHz frequency divider. ** graphically estimated.

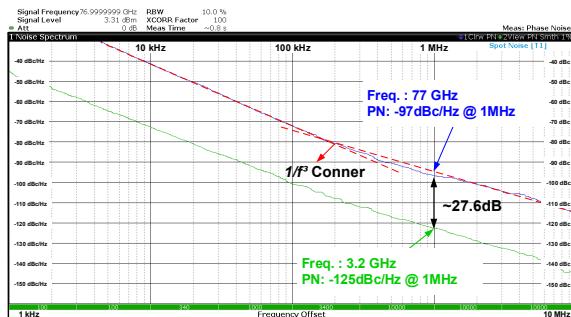


Fig. 8. Measured phase noise plots at 77GHz and 3.2GHz.

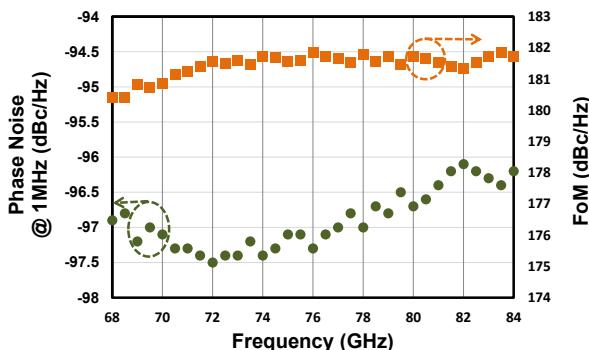


Fig. 9. Phase noise and figure-of-merit (FoM) at 1 MHz offset versus E-band carrier frequency.

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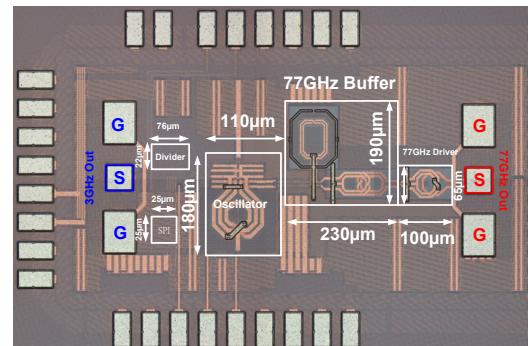


Fig. 10. Chip micrograph of the proposed 77/79 GHz frequency generator.