TU Delft

Delft University of Technology

Document Version
Final published version

Licence
Dutch Copyright Act (Article 25fa)

Citation (APA)
Nagayoshi, K., de Wit, M., Gottardi, L., Taralli, E., Visser, S., Ravensberg, K., Bruijn, M., Vaccaro, D., van der Kuur, J., & Gao, J. R. (2026). Development of a Large-Format X-Ray Microcalorimeter Array Based on a Ti/Au Transition-Edge Sensor. *IEEE Transactions on Applied Superconductivity*, *36*(6), Article 2103006. https://doi.org/10.1109/TASC.2026.3689289

Important note
To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Copyright
In case the licence states “Dutch Copyright Act (Article 25fa)”, this publication was made available Green Open Access via the TU Delft Institutional Repository pursuant to Dutch Copyright Act (Article 25fa, the Taverne amendment). This provision does not affect copyright ownership.
Unless copyright is transferred by contract or statute, it remains with the copyright holder.

Sharing and reuse
Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy
Please contact us and provide details if you believe this document breaches copyrights.
We will remove access to the work immediately and investigate your claim.

*This work is downloaded from Delft University of Technology.*

# Development of a Large-Format X-Ray Microcalorimeter Array Based on a Ti/Au Transition-Edge Sensor

Kenichiro Nagayoshi, Martin de Wit, Luciano Gottardi, *Member, IEEE*, Emanuele Taralli, Sven Visser, Kevin Ravensberg, Marcel Bruijn, Davide Vaccaro, Jan van der Kuur, and Jian-Rong Gao

***Abstract*—We developeda wafer-scale 1504-pixel Ti/Au TES X-ray microcalorimeter array at Space Research Organisation Netherlands (SRON) as a backup technology for the NewAthena X-IFU. The improved fabrication process yields of 99% wiring integrity and uniform absorber thickness within ∼10%, corresponding to minimal performance variation. These results demonstrate a high level of process maturity and support the feasibility of Ti/Au TES arrays for future space-based X-ray spectrometers.**

***Index Terms*—Athena, microcalorimeter, NewAthena, TES, Ti/Au bilayer, X-ray, X-ray integral field unit (X-IFU).**

## I. Introduction

THE stable operation of cryogenic microcalorimeters in orbit on a multiyear timescale has recently been demonstrated with Resolve onboard the X-Ray imaging and spectroscopy mission (XRISM) [1]. Although the XRISM/Resolve focal-plane detector comprises only 36 pixels, the high-resolution spectra obtained from its first light and subsequent astronomical observations have established a new benchmark (e.g., [2] and [3]), clearly distinguishing these spectra from those of traditional X-ray observatories.

Building on the success of XRISM/Resolve, the European Space Agency (ESA) is preparing the Athena mission, which will carry the X-ray integral field unit (X-IFU), an imaging spectrometer designed to achieve significantly higher effective area with improved imaging capability, while enhancing spectral resolution [4]. This performance will be enabled by a large-format transition-edge sensor (TES) [5] microcalorimeter array, which serves as the core technology of the instrument.

The Athena mission has recently undergone a reformulation, primarily driven by the need to reduce mission-end costs to acceptable levels [6]. The redefined focal-plane array for NewAthena is still designed to cover the 0.4–12 keV band, but now with 1504 TES microcalorimeters arranged on a 317 $\mu$m pitch within a hexagon, inscribed in a circle of approximately 15 mm in diameter. The requirement on spectral resolution has been slightly relaxed compared to earlier specifications, now set at 4 eV below 7 keV (corresponding to $\sim$ 2.8 eV for the detector only). Quantum efficiency at 7 keV is maintained around 90%. This requires an X-ray absorptivity of $\approx$95% per pixel, with the remaining difference attributed to the areal fill factor. For the 317 $\mu$m pixel pitch used in this array, achieving this fill factor corresponds to absorber gaps of 6–7 $\mu$m between neighboring pixels, which sets the practical design requirement for the inter-pixel spacing. In addition, the fraction of nonusable science pixels is required to be $<$5% (with a goal of $<$3%).

An X-ray absorber plays an important role in meeting these requirements. Cantilevered absorbers with free ends, consisting of Au and Bi, have emerged as a promising approach, and microcalorimeters based on Mo/Au TESs have been continuously and actively developed at NASA/GSFC, since the pioneering work reported in [7] and [8]. More recently, NASA/GSFC has successfully fabricated large-format arrays covering nearly the entire surface of a 4-in wafer including necessary wiring and connection pads. These arrays have been directly tested at cryogenic temperatures, using dedicated setups, where they demonstrated excellent performance [9], [10].

While the baseline TES array is being developed at NASA/GSFC, Space Research Organisation Netherlands (SRON) is pursuing a fully independent backup array funded by ESA. This effort not only ensures technological redundancy but also provides complementary expertise, thereby enhancing the overall robustness of the mission. At SRON, detectors have consistently demonstrated excellent performance, achieving energy resolutions around 2 eV in smaller array formats, while addressing the evolving requirements of such instruments. In earlier phases, when frequency-domain multiplexing [11] was considered as the baseline readout

Received 26 September 2025; revised 23 March 2026; accepted 26 April 2026. Date of publication 30 April 2026; date of current version 14 May 2026. This work was supported by the European Space Agency through ESA CTP under Grant 4000130346/20/NL/BW/os. *(Corresponding author: Kenichiro Nagayoshi.)*

Kenichiro Nagayoshi, Martin de Wit, Luciano Gottardi, Emanuele Taralli, Sven Visser, Kevin Ravensberg, Marcel Bruijn, and Davide Vaccaro are with NWO-I/SRON Space Research Organisation Netherlands, 2333 CA Leiden, The Netherlands (e-mail: k.nagayoshi@sron.nl).

Jan van der Kuur is with NWO-I/SRON Space Research Organisation Netherlands, 2333 CA Leiden, The Netherlands, and also with NWO-I/SRON Space Research Organisation Netherlands, 9747 AD Groningen, The Netherlands.

Jian-Rong Gao is with NWO-I/SRON Netherlands Space Research Organisation Netherlands, 2333 CA Leiden, The Netherlands, and also with the Optics Research Group, Department of Imaging Physics, Delft University of Technology, 2628CH Delft, The Netherlands.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TASC.2026.3689289.

Digital Object Identifier 10.1109/TASC.2026.3689289

1051-8223 © 2026 IEEE. All rights reserved, including rights for text and data mining, and training of artificial intelligence and similar technologies. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: TU Delft Library. Downloaded on May 26,2026 at 16:14:25 UTC from IEEE Xplore. Restrictions apply.

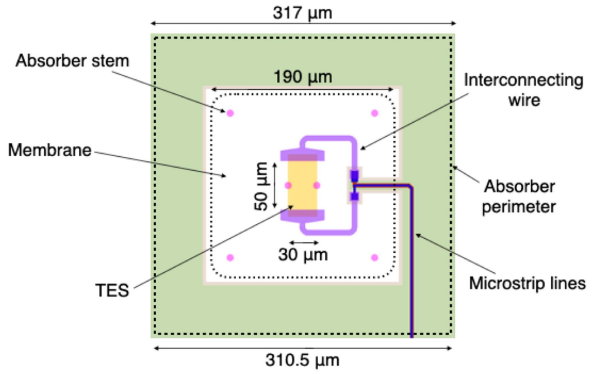



Fig. 1. Schematic of a single TES pixel. Microstriplines enter from the bottom right and split into two branches just before reaching the TES at the center, which is connected to the microstriplines via two interconnecting wires. The square absorber is shown as transparent for clarity, with only its perimeter indicated by a dashed line. The absorber measures 310.5 $\mu$m across, while the pixel pitch is 317 $\mu$m. It is mechanically supported by six stems, two of which are directly connected to the TES to ensure efficient thermal coupling. The green region indicates the Si support frame surrounding the membrane, whose perimeter is shown as a rounded square with sides of 190 $\mu$m and is indicated in the figure by a dashed line of small black dots. Further details are given in the text.

scheme, high-impedance Ti/Au TESs were developed and optimized [12], [13]. Subsequently, as time-division multiplexing [14] was adopted as the mission baseline, SRON shifted its focus to low-impedance TES designs tailored to that architecture [15], [16]. Through these successive developments, SRON has advanced the technological readiness of its fabrication process, and gained valuable insights into the superconducting physics governing TES behavior.

However, these results have so far been obtained mainly with relatively small detector array diced from a wafer. Extending the fabrication process to full wafer-scale arrays introduces additional challenges, particularly in achieving high yield and maintaining uniformity of multilayer structures, such as the X-ray absorbers. Addressing these issues is essential for ensuring reproducibility and reliability in future large-format detector development.

In this work, we present a comprehensive description of the wafer-scale TES fabrication process developed at SRON. Particular emphasis is placed on evaluating the fabrication yield and the thickness uniformity of the absorber layers, identifying dominant failure modes and assessing their impact on large-array reproducibility.

## II. Device Structure and Fabrication Process

The detector architecture and fabrication methods largely follow those reported in [17]. Nevertheless, several steps have undergone minor refinements, and certain details were not previously documented—for example, the Bi X-ray absorber layer, which had not yet been implemented. This section therefore revisits the entire fabrication process, providing a complete description for clarity and reproducibility.

An overview of the detector architecture is shown in Fig. 1. The subsequent subsections describe each fabrication step in detail with reference to this schematic, highlighting both established techniques and the recent modifications introduced at SRON.

### A. Wafer Preparation

The detector is fabricated on a double-side polished 4-in silicon wafer with a thickness of 300 $\mu$m. Both sides of the wafer are first coated with a 350 nm thermally grown silicon dioxide ($SiO_2$) layer, followed by a 500 nm low-stress silicon nitride (SiN) layer deposited by low-pressure chemical vapor deposition. The SiN layer serves as the membrane material, while the $SiO_2$ layer functions as an etch stop during the deep reactive ion etching (Deep-RIE) process from the backside of the wafer. Any residual $SiO_2$ remaining after the Deep-RIE step is subsequently removed by etching in diluted hydrofluoric acid during later stages of the process. In addition, a 280 nm $SiO_2$ film is deposited on the front side and a 3.5 $\mu$m $SiO_2$ film on the backside by plasma-enhanced chemical vapor deposition. The front-side $SiO_2$ layer protects the underlying SiN film during the microstrip line fabrication, while the backside $SiO_2$ layer serves as a hard mask for the Deep-RIE process.

### B. Fabrication of Microstrip Lines

Following wafer preparation, the fabrication proceeds with the formation of the microstrip lines, which define most of the superconducting wiring of the detector array. The microstrip lines are fabricated from sputtered films consisting of a 150 nm Nb layer, 4 $\mu$m wide, a 250 nm $SiO_2$ insulating layer, and a 250 nm Nb layer, 2.8 $\mu$m wide, aligned to the bottom lines. The Nb and $SiO_2$ layers are patterned with tapered profiles by lithography and etched by RIE, using $SF_6$- and $CHF_3$-based recipes, respectively.

In earlier designs, a thin Ta capping layer was employed to suppress Nb oxidation, but this has since been replaced by NbTiN, which provides more robust protection and relaxes process tolerances. The microstrip lines are routed to minimize their total length from the bonding pads to the TESs. The pitch between adjacent lines decreases from 12 $\mu$m near the bonding pads to 4 $\mu$m in the TES region, where the line density is highest. The geometry was chosen to keep the mutual inductance between neighboring lines below the system-level requirement ( 0.5 nH).

### C. TES Fabrication

The TES consists of a bilayer thin film comprising 33.5 nm of Ti and 300 nm of Au, deposited by electron-beam evaporation. The thickness ratio is chosen to yield a superconducting transition temperature in the range of 85–90 mK. The devices are patterned into rectangles with lateral dimensions of 50 $\mu$m $\times$ 30 $\mu$m, a geometry considered promising for X-IFU based on recent studies showing that the sensitivity of TES devices to magnetic fields depends on their width [18], [19], [20]. At cryogenic temperatures, a normal-state resistance of approximately 20 m$\Omega$ is typically observed.

The typical base pressure prior to deposition is $3 \times 10^{-8}$ mbar. The evaporation system is equipped with two independent electron-beam sources, each with a dedicated crucible cassette and shutter. During Ti deposition, the Au source is already melted with its shutter closed, allowing Au deposition to begin

Authorized licensed use limited to: TU Delft Library. Downloaded on May 26,2026 at 16:14:25 UTC from IEEE Xplore. Restrictions apply.

immediately after the Ti layer is completed. The transition between the two depositions is automated, with the shutter system limiting the interval to within 2 s.

The TES bilayer is patterned using a combined dry- and wet-etching process. Most of the Au thickness is first removed by Ar sputter etching in an RIE system. The remaining ∼30 nm of Au is then etched using an iodine-based wet process, ensuring well-defined edges and uniformity across the wafer. Finally, the underlying Ti layer is etched in a 1% HF solution to complete the patterning.

### *D. Dummy Pixel and Interconnecting Wires*

To monitor the gain of the TDM readout, each TDM channel incorporates a low-resistance dummy pixel of approximately 1 mΩ. These pixels are fabricated near the wire-bonding pads, by depositing a 300-nm-thick Au layer with a Ti adhesion layer via electron-beam evaporation, patterned into a short, wide stripe of about 0.1 square using a lift-off process. In the same step, all unoccupied areas on the wafer are coated with the same Au layer.

The dummy pixels and wire-bonding pads are subsequently connected via 450-nm-thick Nb interconnecting wires, also formed using a lift-off process. These interconnects simultaneously establish electrical connections between the TES pixels and the microstriplines.

### *E. X-Ray Absorber Fabrication*

The X-ray absorbers are fabricated using a two-layer photoresist mold. The first resist layer, 4 µm thick, is patterned to define the absorber-supporting stems. Circular openings of 6 µm in diameter are created and subsequently reflow-baked at 135 °C, resulting in smoothly tapered, bell-shaped stem profiles that improve step coverage in later processes and enhance mechanical stability.

Following this, a seed layer is deposited by electron-beam evaporation to enable electroplating. It consists of 120 nm of Au on top of a 5 nm Ti adhesion layer. A second resist layer, 12 $\mu$m thick, is then applied and patterned to define the absorber regions as 310.5 $\mu$m$^2$. The mask design specifies 7.5 $\mu$m gaps between adjacent absorbers, which results in gaps of approximately 6.5 $\mu$m at the top surface of the plated absorbers after processing. The resist mold produces slightly sloped sidewalls (with a sidewall angle of about 88 °), leading to a gradual widening of the gap toward the base, while maintaining good uniformity across the array within typical lithographic tolerances. This resist thickness provides a sufficient margin, to prevent neighboring absorbers from bridging over the mold during plating, as confirmed in Fig. 2.

Electroplating of the Au and Bi absorber layers is carried out in separate baths, each equipped with temperature control and magnetic stirring. The wafer is mounted vertically as the cathode, while a platinized titanium mesh plate serves as the anode. The electrode separation is approximately 30 mm, with the wafer aligned parallel to the anode surface.

For Au deposition, the electrolyte is Techni Gold 25E RTU (Technic Inc.), operated at 56 °C with magnetic agitation at 150 r/min. A constant current density of 1.5 mA/cm$^2$ is applied,

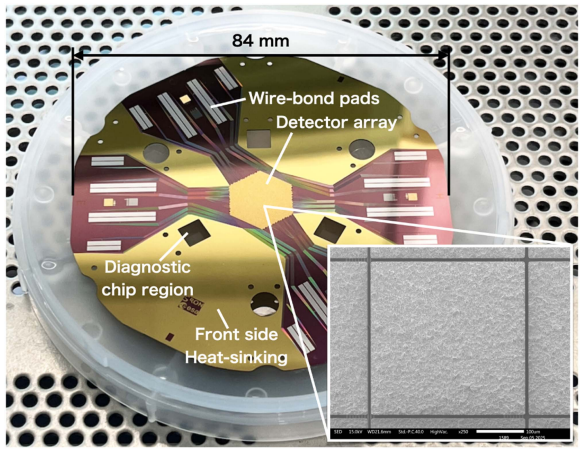



Fig. 2. Photograph of the first complete wafer-scale Ti/Au TES microcalorimeter array fabricated at SRON. The TES array region, wire-bond pads, and one diagnostic chip region are indicated; identical regions are present at the other two corresponding square areas on the wafer. Inset: Top-view SEM image of an Au/Bi X-ray absorber capped with a thin Au layer. The absorber measures 310.5 $\mu$m on a side and is separated from neighboring absorbers by a 6.5 $\mu$m gap. Its surface appears uniformly textured due to the 5–6 $\mu$m Bi grain size while maintaining an overall flat profile. The absorber is mechanically supported by six Bi-backfilled stems that are not visible in the image.

with the plating time adjusted to achieve a target thickness of 0.8 $\mu$m. For Bi deposition, Nb Semiplate 100,[1] a commercial electrolyte co-developed with NB Technologies GmbH is used at 20 °C with agitation at 300 r/min. A constant current density of 0.75 mA/cm$^2$ is applied, and the deposition time is controlled to reach a target thickness of 5.5 $\mu$m. The target thicknesses of 0.8 $\mu$m for Au and 5.5 $\mu$m for Bi were chosen with reference to [23].

After plating, the top resist is stripped with solvent, and a capping layer is deposited by electron-beam evaporation, consisting of 10 nm of Ti followed by 60 nm of Au. This layer serves to prevent oxidation of the Bi surface and to increase reflectivity in the 0.3–20 $\mu$m wavelength range, enhancing the rejection of low-energy radiation as demonstrated in [24].

Finally, the unwanted Au from both the capping and seed layers is removed by Ar sputter etching in an RIE system, with the absorbers protected by a photoresist mask. The absorber fabrication process is thereby completed. Wafer-level visual inspection confirmed, that no visible absorber shorts were present in the main detector array.

### *F. Fabrication of Membrane and Heatsink*

The membrane formation and backside metallization processes follow the procedure reported in [17]. The wafer is temporarily bonded to a carrier wafer using Crystalbond 509, and the deep-RIE process is performed from the backside. Etching is stopped at the $SiO_2$ etch-stop layer prepared during the wafer processing steps described in Section II-A, which is subsequently removed by wet etching in buffered hydrofluoric acid.

[1]https://www.nb-technologies.de/en/products/electroplating-solutions/electroplating-solutions.html

Authorized licensed use limited to: TU Delft Library. Downloaded on May 26,2026 at 16:14:25 UTC from IEEE Xplore. Restrictions apply.

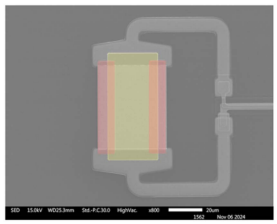


Fig. 3. SEM image of a single TES pixel with Au banks deposited. Each bank is 10 $\mu$m wide (highlighted in red), extending halfway over the Ti/Au bilayer (highlighted in yellow) and halfway onto the SiN membrane layer.

Backside metallization is then carried out by electron-beam evaporation using a shadow deposition technique, which prevents deposition on the membrane backside, while coating the Si pocket sidewalls. This metallization provides a thermal path from the detector chip to the mounting bracket via Au wire bonds, helping to suppress pixel-to-pixel thermal crosstalk and mitigate performance degradation caused by local heating from cosmic-ray interactions. A 10 nm Ti adhesion layer is deposited first, followed by a 2 $\mu$m Cu layer capped with 50 nm of Au. The Cu layer is used here as a cost-effective surrogate to emulate the thermal conduction of a thicker Au layer during process development. In the final detector design, this layer is intended to be replaced by a 3.5 $\mu$m thick Au metallization.

Finally, the detector wafer is released from the carrier. A photoresist remover dissolves the Crystalbond and strips the remaining bottom photoresist from the absorber fabrication procedure, completing the fabrication process as illustrated in Fig. 2.

### G. TES Devices With Au Bank Structures

As shown in Fig. 3, TES devices incorporating Au banks were also fabricated for some pixels located on verification chips as a preliminary experiment. Such structures were first introduced in [21] to improve process robustness and suppress performance degradation in Mo/Au TES fabrication. While not essential in the SRON Ti/Au TES process, the approach was revisited as a means of broadening the options for engineering the TES normal resistance. The fabrication process was integrated into that of the dummy pixels, described in Section II-D: 300 nm of Au was deposited by lift-off into 10 $\mu$m-wide strips placed along the long edges of the TES, half overlapping the TES and half extending onto the surrounding SiN membrane.

Superconducting transition measurements revealed that TES devices with Au banks exhibited approximately a 30% reduction in normal resistance compared to those without, along with a 1 mK decrease in transition temperature. This Tc reduction is consistent with the interpretation that the effective TES width is reduced from 30 to 20 $\mu$m m due to the overlap of the normal-metal Au banks. A detailed study reported in [22] demonstrated that such a width reduction leads to an expected Tc decrease of about 1 mK, in excellent agreement with the present observations. These results therefore confirm that the Au banks function as intended in Ti/Au TES devices. Future work will focus on further optimization of the Au bank geometry, such as adjusting its thickness or coverage, to provide finer control over the TES normal resistance, and enable additional design flexibility.

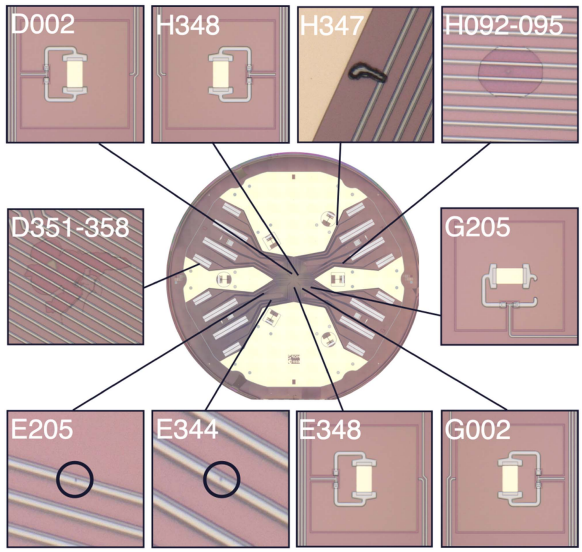



Fig. 4. Optical inspection of the fabricated wafer highlighting representative structures and defects observed across the array. The central image shows the full wafer, with lines indicating the locations of the magnified views. Panels D002, H348, E348, and G002 show representative TES pixels exhibiting design opens (4 pixels). Panel G205 shows a disconnection caused by a patterning error (1 pixel). Particle-related shorts (3 pixels) are observed in E205, E344, and H347; the submicron particles in E205 and E344 are difficult to discern and are therefore indicated by black circles, while H347 shows a larger particle contamination. Panels H092–095 and D351–358 show structural defects associated with poor adhesion of the $SiO_2$ layer, resulting in adhesion perforations (12 pixels).

## III. Fabrication Results

### A. Fabrication Yield of Microstriplines

To assess the reliability of these wiring structures, the room-temperature resistance was measured using an automated probe system (MPI TS2000), which sequentially scanned the wire-bond pads associated with each pixel across the wafer, to verify the continuity of the corresponding wiring loops. For each pixel, 15 measurements were performed, and the mean value was then compared with the nominal resistance. The standard deviation of the accepted pixel resistances relative to the nominal value was found to be about 2%. If the deviation exceeded 5% ($\approx$2.5 standard deviations), the pixel was regarded as potentially defective. To ensure the absence of cross-shorts, the scan program was modified to sequentially probe all neighboring wiring lines, confirming electrical isolation and the absence of low-resistance bridges between adjacent lines.

As a result of the resistance screening, 20 out of a total of 1504 pixels exhibited anomalous values. All of these pixels were subsequently examined using optical microscopy, and the identified causes are presented in Fig. 4.

Among the defective pixels, those labeled D002, E348, G002, and H348 exhibited open-circuit behavior. Further investigation revealed that these cases originated from incomplete connections in the design layout rather than from process-related issues. While unintentional, these instances effectively served as a blind test during resistance screening.

Authorized licensed use limited to: TU Delft Library. Downloaded on May 26,2026 at 16:14:25 UTC from IEEE Xplore. Restrictions apply.

A different type of open-circuit defect was observed in pixel G205, which involves the interconnecting wire rather than the microstrip line. It is clear that one side of the interconnect is disconnected. This failure is most plausibly attributed to a patterning error in the lift-off resist, which unintentionally resulted in part of the interconnect being removed during the lift-off process.

In addition to open-circuit failures, another category of defects observed was short circuits, referring to unintended electrical connections between the lower and upper wiring layers that bypass the TES. A representative example is pixel H347, where the short is most likely caused by a particle deposited during the formation of the lower wiring layer. Although such relatively large-particle contamination is rare, its risk can be further reduced through stricter and more frequent cleaning of the deposition system. On the other hand, shorts induced by submicron-scale particles, as observed in pixels E205 and E344, are of greater concern. While currently limited to only two pixels, further investigation is ongoing to better understand and mitigate this failure mode.

Another category of short defects arises from mechanical failure of the insulating layer. In eight pixels ranging from D351 to D358 and in five pixels from H092 to H095, visible perforations were observed in the $SiO_2$ layer. The morphology of these defects suggests that they are not primarily due to lithographic patterning errors, but rather point to insufficient adhesion of the $SiO_2$ film. To mitigate this issue, greater attention must be paid to wafer cleaning prior to deposition, with a focus on removing organic contaminants completely through chemical cleaning and reassessing the effectiveness of in situ plasma cleaning procedures. Excluding defects originating from design-related issues, the intrinsic process yield is estimated to be approximately 99%, which satisfies the mission requirement on the fraction of nonusable science pixels.

### *B. Thickness Uniformity of X-Ray Absorber Layers*

The thickness uniformity of the X-ray absorber layers was evaluated by depositing and characterizing the Au and Bi films separately on dedicated test wafers. This approach was adopted because it is difficult to measure the thickness of each individual layer with conventional metrology techniques once the full Au/Bi bilayer absorber is fabricated. The test wafers were designed to reproduce the same mold geometry, pattern density, and plating configuration as the device wafers, ensuring comparable deposition conditions.

The thickness of each absorber layer was measured primarily using a 3-D laser confocal microscope (VK-X1000), while a contact-type step profiler (Dektak 150) was also employed as a complementary method when appropriate. For each wafer, 50 sampling points were uniformly distributed across the absorber array to capture both global and local variations. The discrete data were interpolated using a radial basis function algorithm with a thin-plate spline kernel, thereby generating continuous spatial maps suitable for direct visualization and quantitative analysis.

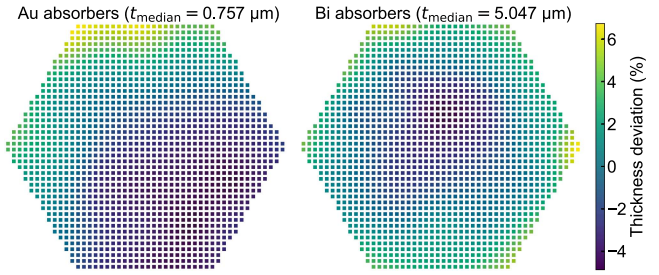



Fig. 5. Deviation in the thickness of electroplated Au (left) and Bi (right) absorber layers across the 1504-pixel array. Each heat map was generated from 50 uniformly distributed measurement points, using radial basis function interpolation with a thin-plate spline kernel.

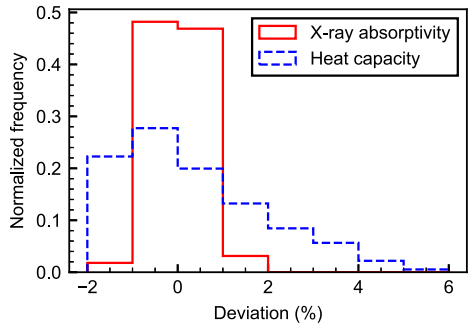



Fig. 6. Step histograms showing the distribution of relative deviations in X-ray absorptivity (solid red line) and heat capacity (dashed blue line) across the absorber array. The distributions are derived from the absorber thickness measurements shown in Fig. 5 and include contributions from the seed layer and the Au capping layer.

Fig. 5 presents the resulting thickness distributions of the Au and Bi layers as 2-D heat maps with color bars, showing deviations from the median thickness at each measurement point. The Au layer exhibited a median thickness of 0.757 $\mu$m with an overall thickness range of approximately 8%, whereas the Bi layer had a median thickness of 5.047 $\mu$m and a range of about 10%. Systematic nonuniformities were evident in both absorber layers, though with distinct spatial profiles. The Bi layer showed a radial pattern, where the thickness gradually increased from the center of the array toward the edges. This is consistent with phenomena commonly observed in electroplating processes, namely current crowding at the pattern boundaries combined with mass-transport limitations. This effect is expected to be further mitigated through optimization of the dummy (sacrificial) plating patterns in future process iterations. By contrast, the Au layer exhibited a vertical gradient: the lower portion of the array was thinner while the upper portion was thicker. This anisotropy is most likely attributable to slight misalignment or nonparallelism between the wafer surface and the plating electrodes during deposition, leading to preferential ion flux and differential deposition rates.

To evaluate the impact of these thickness variations on device-level properties, pixel-by-pixel deviations were translated into corresponding deviations in thermal and absorptive parameters. Fig. 6 shows histograms of the resulting deviations in heat capacity (dashed blue line) and X-ray absorptivity (solid red line). The horizontal axis represents the deviation relative to the

Authorized licensed use limited to: TU Delft Library. Downloaded on May 26,2026 at 16:14:25 UTC from IEEE Xplore. Restrictions apply.

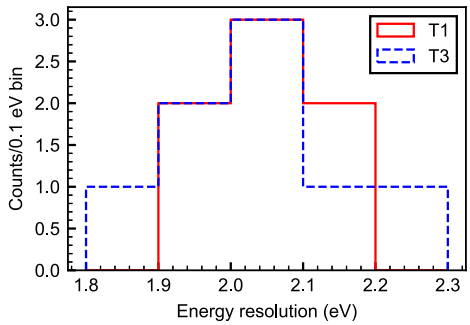



Fig. 7. Stepped histograms of the energy resolution at 5.9 keV for two diagnostic chips. T1 (solid red) and T3 (dashed blue) correspond to the lower-left and lower-right chip locations in Fig. 2. Despite the limited number of pixels measured (7 for T1, 8 for T3), the two chips show consistent performance, suggesting promising device uniformity.

median values, which were estimated to be 0.742 pJ/K at 90 mK for the heat capacity and 87.4% at 7 keV for the absorptivity. The intrinsic contribution of absorber nonuniformity to the TES energy resolution is expected to be relatively small, on the order of 2.8%, since the resolution scales with the square root of the heat capacity. However, other detector characteristics, such as the response function, the decay time constant of the detection pulse, and the linearity of the response scale directly with the heat capacity, making further improvement of absorber uniformity desirable. In particular, because the heat capacity is dominated by the Au layer, enhancements in jig design for the plating setup and further optimization of deposition parameters will be key to achieving better uniformity in the Au films.

On the other hand, the uniformity of X-ray absorptivity across the array is already excellent, with more than 95% of pixels falling within $\pm$ 1% of the median value. It should be noted, however, that the absorptivity reported here for the first time is derived from the average absorber thickness. Therefore, effects associated with absorber surface roughness or the backfilling of absorber stems, as demonstrated in [24], have not yet been incorporated and may require further dedicated evaluation.

## IV. Preliminary Results and Outlook

Initial X-ray measurements on pixels of the diagnostic chips in the same wafer yield an average energy resolution of approximately 2.1 eV at 5.9 keV (Mn K$\alpha$) at a transition temperature of $T_c \sim$76 mK, which presents stepped histograms of the measured energy resolution for the two diagonal chips (see Fig. 7). Despite the limited number of pixels, the consistent behavior between the two chips suggests promising uniformity across the device. The corresponding noise-equivalent power, however, indicates a resolution of roughly 1.7 eV. The origin of this discrepancy is currently under investigation, taking into account both potential improvements to the experimental setup and intrinsic detector properties.

Further characterization is ongoing to fully assess detector performance, including studies of low-energy tails, energy scale calibration, sensitivity to temperature and magnetic fields, reflectance of the Au-capped absorber, and long-term stability relevant to mission lifetime. Feedback from this first fabrication run will inform the upcoming batch production under ESA funding, with the aim of establishing this technology as a fully qualified backup option.

## References

[1] M. Tashiro et al., "X-ray imaging and spectroscopy mission," *Pub. Astron. Soc. Jpn.*, vol. 77, Apr. 2025, Art. no. psaf023.
[2] XRISM Collaboration, "The XRISM first-light observation: Velocity structure and thermal properties of the supernova remnant N 132D," *Pub. Astron. Soc. Jpn.*, vol. 76, no. 6, pp. 1186–1201, Oct. 2024.
[3] XRISM Collaboration, "XRISM spectroscopy of the Fe K$_\alpha$ emission line in the Seyfert active galactic nucleus NGC 4151 reveals the disk, broad-line region, and torus," *Astrophysical J. Lett.*, vol. 973, no. 1 Sep. 2024, Art. no. L25.
[4] D. Barret et al., "The athena X-ray integral field unit: A consolidated design for the system requirement review of the preliminary definition phase," *Exp. Astron.*, vol. 55, no. 2, pp. 373–426, Jan. 2023.
[5] K. D. Irwin and G. C. Hilton, "Transition-edge sensors," *Cryogenic Part. Detection, Topics Appl. Phys.*, vol. 99, pp. 63–150, Jan. 2005.
[6] P. Peille et al., "The X-ray integral field unit at the end of the athena reformulation phase," *Exp. Astron.*, vol. 59, no. 2, Mar. 2025, Art. no. 18.
[7] C. A. Kilbourne et al., "High-density arrays of X-ray microcalorimeters for constellation-X," *Proc. SPIE*, vol. 6266, Jun. 2006, Art. no. 626621.
[8] A.-D. Brown et al., "Absorber materials for transition-edge sensor X-ray microcalorimeters," *J. Low Temp. Phys.*, vol. 151, no. 1–2, pp. 413–417, Jan. 2008.
[9] K. Sakai et al., "Demonstration of a full-scale brassboard TES microcalorimeter array for the athena X-IFU," *IEEE Trans. Appl. Supercond.*, vol. 33, no. 5, Aug. 2023, Art. no. 2100905.
[10] S. J. Smith et al., "Development of the microcalorimeter detector for the athena/X-ray integral field unit," in *Proc. SPIE*, vol. 13093, Aug. 2024, Art. no. 130930V.
[11] H. Akamatsu et al., "Demonstration of MHz frequency domain multiplexing readout of 37 transition edge sensors for high-resolution x-ray imaging spectrometers," *Appl. Phys. Lett.*, vol. 119, no. 18, Nov. 2021, Art. no. 182601.
[12] E. Taralli et al., "Characterization of high aspect-ratio TiAu TES X-ray microcalorimeter array under AC bias," *J. Low Temp. Phys.*, vol. 199, no. 1–2, pp. 80–87, Nov. 2019.
[13] M. de Wit et al., "High aspect ratio transition edge sensors for x-ray spectrometry," *J. Appl. Phys.*, vol. 128, no. 22, Dec. 2020, Art. no. 224501.
[14] W. B. Doriese et al., "Developments in time-division multiplexing of x-ray transition-edge sensors," *J. Low Temp. Phys.*, vol. 184, no. 1–2, pp. 389–395, Jul. 2016.
[15] E. Taralli et al., "Small size transition-edge sensors for future X-ray applications," *J. Low Temp. Phys.*, vol. 209, no. 3–4, pp. 256–262, Mar. 2022.
[16] M. de Wit et al., "Performance of the SRON Ti/Au transition edge sensor x-ray calorimeters," in *Proc. SPIE*, vol. 12181, Aug. 2022, Art. no. 121812B.
[17] K. Nagayoshi et al., "Development of a Ti/Au TES microcalorimeter array as a backup sensor for the Athena/X-IFU instrument," *J. Low Temp. Phys.*, vol. 199, no. 3–4, pp. 943–948, 2020.
[18] D. Vaccaro et al., "Susceptibility study of TES micro-calorimeters for X-ray spectroscopy under FDM readout," *J. Low Temp. Phys.*, vol. 209, no. 3–4, pp. 562–569, Sep. 2022.
[19] M. de Wit et al., "Transition edge sensors for DC operation and low magnetic field sensitivity," *IEEE Trans. Appl. Supercond.*, vol. 35, no. 5, Aug. 2025, Art. no. 2100505.
[20] N. A. Wakeham et al., "Refinement of transition-edge sensor dimensions for the X-ray integral field unit on ATHENA," *IEEE Trans. Appl. Supercond.*, vol. 33, no. 5, Aug. 2023, Art. no. 2100506.
[21] G. C. Hilton et al., "Microfabricated transition-edge X-ray detectors," *IEEE Trans. Appl. Supercond.*, vol. 11, no. 1, pp. 739–742, Mar. 2001.
[22] K. Nagayoshi et al., "Lateral inverse proximity effect in Ti/Au transition edge sensors," *J. Low Temp. Phys.*, vol. 209, no. 3–4, pp. 540–547, Aug. 2022.
[23] E. Wassell et al., "Microcalorimeter absorber optimization for ATHENA and LEM," *J. Low Temp. Phys.*, vol. 216, no. 1–2, pp. 417–426, Jun. 2024.
[24] R. Hummatov et al., "Quantum efficiency study and reflectivity enhancement of Au/Bi absorbers," *J. Low Temp. Phys.*, vol. 199, no. 1–2, pp. 393–400, Mar. 2020.

Authorized licensed use limited to: TU Delft Library. Downloaded on May 26,2026 at 16:14:25 UTC from IEEE Xplore. Restrictions apply.