A High-Resolution, Resistor-Based Smart Temperature Sensor

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Abstract

This thesis focuses on developing a high resolution, energy-efficient smart temperature sensor for wafer stepper temperature monitoring. A resistor-based temperature-sensing structure, Wien Bridge (WB), is chosen as the core of the sensor because it is able to achieve a high resolution in an energy-efficient way. The resolution achieved in previous work based on this structure is limited by the readout noise. Therefore, this work mainly concentrates on developing a low-noise readout which is capable of preserving the inherent resolution of the WB in an energy-efficient way. The design has been fabricated in a standard 180 nm CMOS technology, and the measurement results confirm the expected improvement in the readout performance.

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Chapter 1 Introduction

1.1 Application and Specification

The first working integrated circuit (IC) on semiconductor was demonstrated on 12 September 1958 with planar IC technology [1] [2]. Since then, planar technology, consisting of film deposition, lithography, and etching, has been widely employed to fabricate ICs. Due to the consistent improvement of the planer technology over the years, especially the improvement of the lithography resolution, the feature size of the semiconductor technology has migrated from milimeter-scale to nanometer-scale, and more transistors are integrated in the same area. Just as Gordon E. Moore predicted, "*The number of transistors incorporated in a chip will approximately double every 24 months"* [3], the transistor density on ICs has been increasing exponentially. Correspondingly, the dimensions of a transistor are shrinking about 30% every 18 months [4].

The lithography resolution has been improved by decreasing the wavelength of the exposure light, by increasing the numerical aperture (NA) of the exposure tools (*e.g.* wafer stepper, wafer scanner), and by employing advanced materials and technologies [5].

The highest lithography resolution up to now is achieved by employing a wavelength of 193 nm (ArF) and immersion wafer scanners with 1.35 NA lenses [5]. However, the NA of 193 nm exposure tools cannot be increased further because immersion fluids with higher refractive indices are not available; Meanwhile, smaller exposure wavelengths such as 157 nm cannot be used due to the lack of suitable lens materials or the lack of suitable immersion fluids. Therefore, the industry has to explore new strategies to improve the lithography resolution.

To achieve better lithography resolution while sustaining the planar technology, which is a two-dimensional (2D) technology, multi-patterning can be used [6]. Instead of 2D technology, Intel has deployed a fundamentally different technology for future microprocessor families, three-dimensional (3D) tri-gate transistor. This technology allows the designers to innovate new architectural approaches for 22 nm Intel Atom microarchitecture [7].

In addition to these two, there are also other possible options being researched to achieve a higher resolution. Among all the options, one of the most promising technologies is to employ extreme ultraviolet (EUV) as lithography light source. EUV allows 2D structures and only requires a single exposure. Therefore, the design rule is simplified and the lithography process is simplified as well due to less patterning and less metrology steps, resulting in low cost and potentially better yield [6].

In EUV lithography (EUVL), radiation with a wavelength of 13.5 nm is generated by a EUV source and used to shape the wafer. However, radiation at this wavelength is strongly absorbed by plenty of objects, including wafer steppers. In wafer steppers, thermal expansion is an important error source, thus control loops are required to stabilize the temperature such that the dimensions of the critical mechanical components can be maintained over temperature [33]. Therefore, the temperature of the mechanical elements of the stepper must be accurately measured. In order to achieve high temperature-sensing accuracy, high resolution is required. Since the EUVL process is conducted in the

vacuum environment, self-heating of the temperature sensor should be minimized. Therefore, the power consumed by the temperature sensor should be minimized. In addition to that, since the wafer stepper temperature monitoring would last for a long period, a stability requirement is imposed on the temperature sensors for this application.

This project is to design a temperature sensor in a standard CMOS technology used to sense the temperature inside a wafer stepper. For this application, high resolution, low power consumption and good stability are needed. The goal is to achieve a sub-mK resolution and to exceed the state-of-the-art.

A figure of merit (FOM) has been devised to describe the energy-efficiency of a smart temperature sensor. It is the product of energy/conversion and the square of resolution, which usefully bounds the state-of-the-art.

To date, the highest resolution achieved by an integrated temperature sensor is described in [14]. In that design, the sensor is resistor-based and achieves a temperature-sensing resolution of 100 μK in a 5-Hz bandwidth with a power consumption of 13 mW, leading to a FOM of 12 pJ K^2. However, that sensor is implemented in a micro-electro-mechanical-systems (MEMS) technology instead of a standard CMOS technology.

The design specifications are summarized in Table 1.1.

Table 1.1 Design Specifications of the Temperature Sensor

	Target
Resolution	< 0.2 mK(rms) in a 100-Hz bandwidth
Power consumption	< 100 μW
FOM	< 20 fJ K^2

1.2 Temperature Sensor Comparison

1.2.1 Performance of Temperature Sensors in Literature

Numerous temperature-sensing devices have been designed for different applications. According to the temperature-sensing principle, temperature sensors can be divided into four categories: BJT (bipolar junction transistor)-based temperature sensors, MOSFET (metal-oxide-semiconductor field-effect transistor)-based temperature sensors, thermal-diffusivity-based temperature sensors and resistor-based temperature sensors [8].

Comparisons among these four types of temperature sensors are required in order to choose the most suitable sensor type for this project. Since temperature-sensing resolution and energy consumption are the major specifications in this project, the temperature sensor comparison focuses on these two aspects. For the four types of temperature sensors mentioned above, the relation between the energy consumption per conversion and temperature resolution is summarized in Figure 1.1.

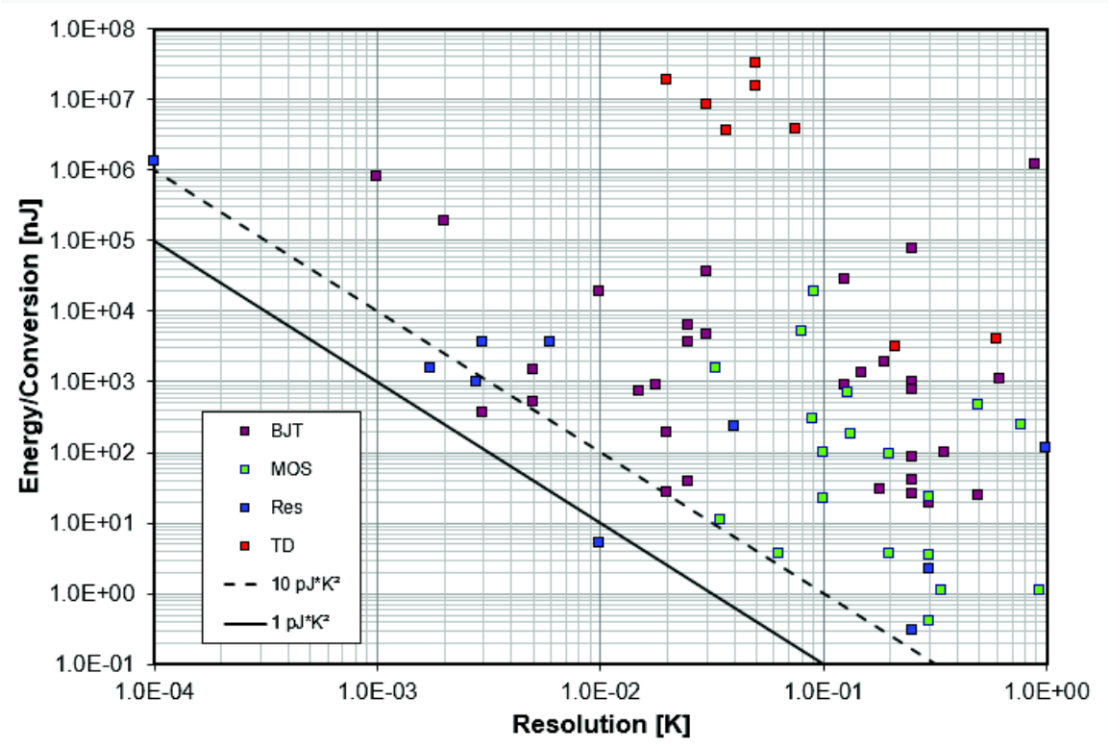

Figure 1.1 Smart temperature sensor performance: energy per conversion versus resolution [16]

According to Figure 1.1, BJT-based temperature sensors and resistor-based temperature sensors are much more energy-efficient (can achieve lower FOM) than the other two types of temperature sensors. Both of them can achieve a FOM better than 10 pJ K^2 [17] [35].

Literature study shows that the resolution of a temperature sensor is always limited by the noise from the readout. Even in those state-of-the-art temperature sensors, this is still the case. For instance, the temperature sensor proposed in [14] has an inherent temperature-sensing resolution of 16 μK (rms) in a 100-ms conversion time; however, due to the readout noise, a resolution of 100 μK (rms) is achieved in the same conversion time.

1.2.2 BJT-Based Temperature Sensors versus Resistor-based Temperature Sensors

To make a proper choice between a BJT-based temperature sensor and a resistor-based temperature sensor, their inherent resolution at the same current consumption is calculated. Assume that the signal band is 50 Hz, and that both of them consume 10 μA current.

The resistor-based temperature sensing technique is shown in Figure 1.2 [14]. The temperature dependent signal is derived from a resistive divider, consisting of one temperature-dependent resistor R(T) and one reference resistor R_0, which is temperature-independent in an ideal case. R(T) is expressed as Equation 1.3, where α is the temperature coefficient (TC) of R(T).

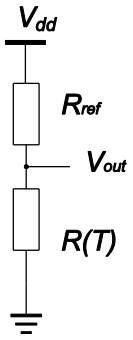

Figure 1.2 Resistor-based temperature-sensing technique

$$R(T) = R_0 + \alpha(T - T_0)R_0 \tag{1.3}$$

Set $R_0 = R_{ref}$, and assume $V_{dd} = 1.8\,V$. Since 10 µA current is consumed, $R_0 = R_{ref} = 90\,k\Omega$. The output noise spectral density is given in Equation 1.4.

$$\overline{v_{n,out}^2} = 4kT(R_{ref} || R_0) \tag{1.4}$$

The voltage-to-temperature sensitivity can be calculated using Equation 1.5.

$$S_T^V = \frac{dV_{out}}{dT} = V_{dd}\frac{R(T)}{R(T) + R_0} - \frac{V_{dd}}{2} \approx \frac{V_{dd}}{4}\alpha \tag{1.5}$$

Assume $\alpha = 0.28\%/℃$, then by combining Equation 1.4 and 1.5, a temperature-sensing resolution of 150.6 µK in a 50-Hz bandwidth can be achieved by a resistor-based temperature sensor with 10 µA current consumption. Assuming the readout consumes 90 µA current, a FOM of 41 fJ·K^2 can be achieved. This is 10× below the current state-of-the-art [46], which achieves a FOM of 0.65 pJ·K^2.

The temperature-sensing resolution of a BJT-based temperature sensor proposed in [47] can be calculated by Equation 1.6.

$$dT = \frac{A}{V_{REF}}\,\alpha\sqrt{\frac{2kT(1 - \mu)}{g_m t_{conv}}} \tag{1.6}$$

As mentioned before, assume the signal bandwidth is 50 Hz, corresponding to a conversion time of 10 ms; and also assume that the current consumption is 10 µA, leading to a g_m of 385 µS. The typical values for the coefficients in Equation 1.6 are: A = 600, V_{REF} = 1.2 V, and μ=0.5. Assume α = 20, then the temperature-sensing resolution of the BJT-based temperature sensor is 326.8 µK. Assuming the readout consumes 90 µA current, a FOM of 192 fJ·K^2 can be achieved.

Assuming the temperature-sensing resolution is determined by the noise from the temperature-sensing component itself, with the same current consumption, a resistor-based temperature sensor can achieve more than twice higher resolution, thus more than four times better FOM than a BJT-based temperature sensor. Therefore, a resistor-based temperature sensor is chosen in this project.

1.3 Literature Review

Resistor-based temperature sensors consist of temperature dependent resistors and temperature independent references. As discussed in Section 1.2, compared with a BJT-based temperature sensor, a resistor-based temperature sensor can achieve a higher temperature-sensing resolution when the same amount of power is consumed. However, the temperature dependency of the resistor-based temperature sensors is less linear than that of other types of temperature sensors. In order to achieve a high accuracy, multiple-point calibration is usually required in resistor-based temperature sensors.

In [14], the temperature sensor core is a voltage divider consisting of a temperature-dependent MEMS resistor and a tunable reference resistor. The tunable reference resistor is implemented by a switched capacitor, of which the resistance can be controlled by the switching frequency. A feedback loop balances the voltage divider by adjusting the switching frequency via a voltage-controlled-oscillator (VCO)-based quantizer and a fractional-N divider. The resulting division factor is a representative of temperature. This design achieves a state-of-the-art resolution of 100 μK in a 100 ms conversion time with a power consumption of 13 mW, leading to a FOM of 13 pJ·K^2. After 6-point calibration, its temperature-sensing inaccuracy is ±0.015 ℃ (min/max) over the temperature range from -40 ℃ to 85 ℃. In that design, the resolution is limited by the readout noise.

In [15], the temperature sensor core is a passive-RC bandpass filter, consisting of temperature-dependent resistors and almost temperature-independent capacitors. When driven by a square wave with fixed frequency, the phase shift of the filter output is temperature-dependent, and is digitized by a phase-domain delta-sigma analog-to-digital converter (ADC). A resolution of 6 mK in a conversion time of 100 ms is achieved with a power consumption of 36 μW, leading to a FOM of 130 pJ·K^2. After batch calibration and a 3-point calibration, it achieves ±0.15 ℃ (3σ) inaccuracy over the temperature range from -40 ℃ to 85 ℃. In that design, the resolution is limited by the thermal noise of the current buffer, which is part of the readout.

In [46], temperature-dependent resistors are embedded in a 2nd order 1-bit continuous time delta-sigma modulator (CTDSM). A resolution of 10 mK in a single conversion time of 100 μs is achieved with 64.5 μW power consumption, leading to a FOM of 0.65 pJ·K^2. After 2-point calibration, it achieves an inaccuracy of ±0.4 ℃ (min/max) over the temperature range from -45 ℃ to 125 ℃.

In [49], temperature-dependent resistors are used to generate a temperature-dependent voltage. Then the difference between the temperature-dependent voltage and the reference voltage is converted into a time interval, which is digitized by a time-to-digital converter. That design achieves a resolution of 250 mK in a conversion time of 10 ms, leading to a FOM of 7.4 nJ·K^2. After 2-point calibration, it achieves an inaccuracy of -0.6℃/0.8℃ over the temperature range from -40℃ to 125℃. The resolution is mainly limited by the noise from the readout.

In [35], the temperature sensor core is the same as the one used in [15]. To digitize the temperature information, the sensor core is embedded in a frequency-locked loop (FLL). It achieves a resolution of 2.8 mK in a conversion time of 32 ms with a power consumption of 31 μW, leading to a FOM of 8

pJ·K^2. After a 3-point calibration, it achieves an inaccuracy of ±0.12 ℃ (min/max) over the temperature range from -40 ℃ to 85 ℃. In that design, the resolution is limited by the thermal noise of the current buffer in the readout.

Literature study indicates that resistor-based temperature sensors do achieve high temperature-sensing resolution in an energy-efficient way; the resolution, however, can be further improved by noting that the state-of-the-art resolution is limited by the readout noise.

1.4 Thesis Organization

The thesis is organized as follows. In Chapter 2, different architectures of resistor-based temperature sensors are discussed, and the reason why the architecture of a passive-RC filter is the most suitable candidate in this project is presented. Chapter 3 elaborates on the design of the temperature sensing block, a passive-RC filter, which is targeted at sub-mK resolution. In Chapter 4, the readout circuit for the temperature sensing block implemented in Chapter 3 is presented. In Chapter 5, the measurement results are presented and analysed. This thesis work is concluded in Chapter 6; also future work which can improve the sensor performance is presented in the same chapter.

Chapter 2 Temperature-Sensing Components and Structures

As discussed in Chapter 1, since a resistor-based temperature sensor can achieve a high resolution in an energy-efficient way, it is chosen in this project. In this chapter, first, based on literature, different types of resistors which are used as temperature-sensing components are discussed. Afterwards, two main configurations of resistor-based temperature sensors are discussed.

2.1 Resistor Choosing

2.1.1 Temperature Dependency of Resistors

In a standard CMOS process, n-well resistors, diffusion resistors, poly-silicon resistor without silicide, and poly-silicon resistor with silicide are available. According to [15] and [49], n-well resistors and poly-silicon resistors with silicide have a relatively higher temperature coefficient (TC) compared with other types of resistors. According to Equation 1.5, a high TC leads to a high sensitivity, resulting in a superior resolution. Therefore, in this project the temperature-dependent resistors required in the sensor should be chosen between n-well resistors and poly resistors with silicide.

2.1.2 N-well Resistor versus Poly Resistor with Silicide

As presented in Section 2.1.1, n-well resistors and poly resistors with silicide have a relatively high temperature coefficient compared with other available resistors in a standard CMOS technology. Therefore, further comparison is conducted between n-well resistors and poly resistors with silicide in order to find the most suitable temperature-sensing components for this application.

A typical n-well resistor in a CMOS process is fabricated by diffusion or ion implantation. The dopant concentration of the resistor and the thickness of the diffusion layer are determined by the technology. As shown in Figure 2.4, the n-well resistor is capacitively isolated from the substrate by forming inverse-biased PN junctions, resulting in a voltage-dependent parasitic capacitance to the substrate.

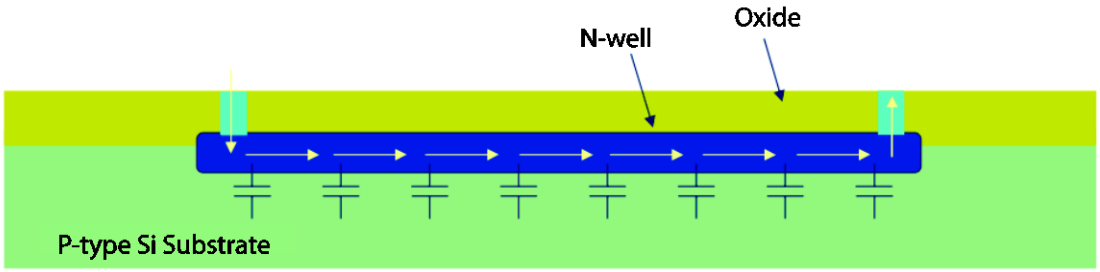

Figure 2.4 A typical n-well resistor (cross section) [18]

Instead of forming resistors on top of silicon material directly, poly resistors are built by depositing poly silicon films on top of silicon oxide [18], as shown in Figure 2.5. Since poly resistors are far away

from silicon material, they have a lower parasitic capacitance compared with diffusion resistors, thus a lower voltage-dependency.

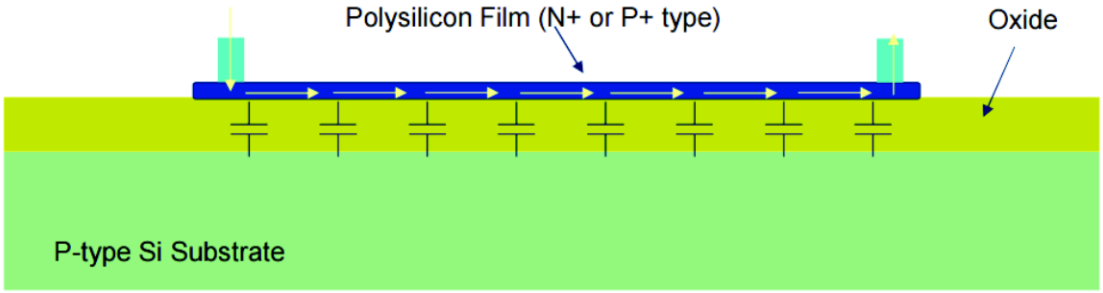

Figure 2.5 A typical poly resistor (cross section) [18]

In addition to parasitic capacitance and voltage-dependency, n-well resistors are inferior to poly resistors when it comes to the process variation. According to the spice model data, the process variation suffered by the n-well resistors is almost two times larger than that suffered by the poly resistors with silicide. Therefore, poly resistors with silicide are preferred as the temperature-sensing components in this project.

2.1.3 Flicker Noise Issue in Poly Resistor with Silicide

As presented in Section 2.1.1 and Section 2.1.2, both poly resistors with silicide and n-well resistors have higher TCs compared with other available resistors in a standard CMOS technology. However, when it comes to parasitic capacitance, voltage-dependency and process variation, poly resistors with silicide are superior to n-well resistors.

In addition to these properties, the temperature-sensing resistors' flicker noise also needs to be considered. It is important to note that in a resistor, flicker noise will increase as the current increases [44].

In this project, the flicker noise should be as low as possible, because the signal in this application is near DC. If the flicker noise corner frequency is higher than the signal band, the temperature-sensing resolution would be limited by flicker noise, which is difficult to suppress during the design phase. Besides, due to high flicker noise the sensor would suffer from fast drift and tend to be less stable. Either from the resolution aspect or from the stability aspect, the temperature-sensing component should have sufficiently low flicker noise.

As presented in [22][24][25], poly resistors demonstrate high flicker noise; however, no literature elaborating the flicker noise of poly resistors with silicide is found; flicker noise of this type of resistors is not modelled in the technology either. Meanwhile, the flicker noise of poly resistors is modelled.

In [32], it is suggested that in poly resistors, flicker noise is proportional to the sheet resistance. Based on this relation and the poly resistor model in the technology, the flicker noise of poly resistors with

silicide was estimated, which was considered acceptable in this project.

Based on the estimation above, poly resistors with silicide were chosen as the temperature-sensing components in this project. However, measurements show that this is not the best choice. More details about this will be discussed in Chapter 5.

2.2 Sensor Structure Choosing

In the previous section, silicided poly resistors were chosen as the temperature-sensing resistors. During temperature measurement, references are also needed to cooperate with the resistors to perform the temperature measurement. In the literature, two kinds of references have been proposed. One is to use resistors with lower TC compared with silicided poly resistor or resistors with opposite TC polarity. The other is to use capacitors and a precision clock frequency as reference impedance. Structures employing these two kinds of references are discussed below.

2.2.1 Temperature Sensor Configured in Wheatstone Bridge

To implement resistor-based temperature-sensing, one way is to configure the temperature sensing resistor in a Wheatstone bridge structure, as shown in Figure 2.6. In this structure, another type of resistor is employed as reference. At room temperature, the four resistors in the bridge have the same resistance, thus the output is zero. As the temperature changes, the resistance of temperature-dependent resistors changes, hence the output is a function of temperature.

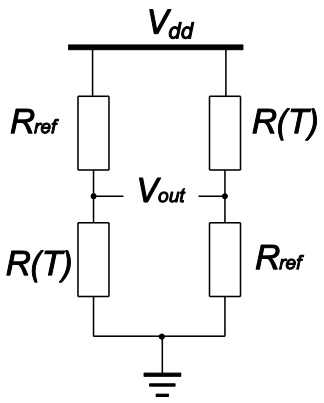

Figure 2.6 A temperature sensor configured in Wheatstone bridge

In [33], a smart temperature sensor consisting of an off-chip Wheatstone bridge and a readout IC is proposed. The Wheatstone bridge consists of two temperature-dependent resistors with negative TC and two metal foil resistors. The diagram of the proposed smart temperature sensor is shown in Figure 2.7. In that design, 0.7 μK (rms) temperature-sensing resolution at a conversion time of 250 ms is achieved at a current consumption of 379 μA (Wheatstone bridge 109 μA, readout-IC 270 μA) from a 5 V supply, leading to a FOM of 0.2 fJ K^2.

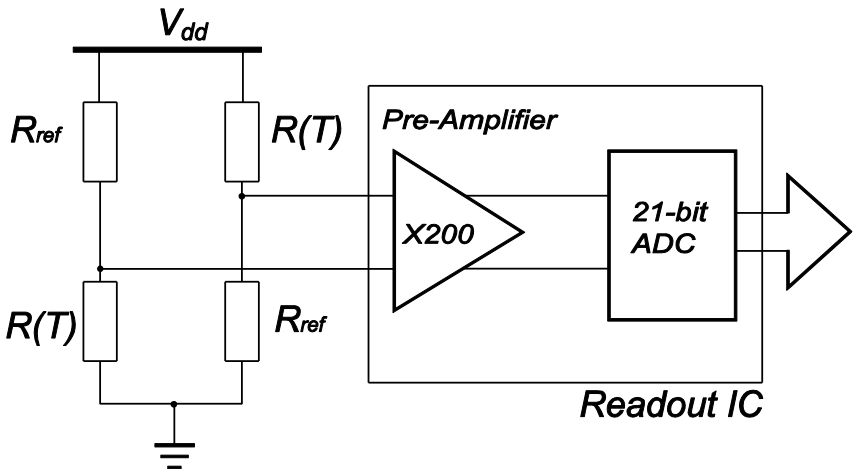

Figure 2.7 Block Diagram of Wheatstone Bridge-based smart temperature sensor [33]

The signal in [33] is digitized by a 21-bit delta-sigma ADC. Since the amplitude of the bridge output is at millivolt level, the bridge output is amplified by an ultra-low-noise precision instrumentation pre-amplifier before being digitized. Because the Wheatstone bridge and readout-IC are not integrated in the same chip, a cable is required to connect the bridge output to the readout-IC. The cable must be well shielded from environmental interference due to the low amplitude of the bridge output.

If the bridge can be directly connected to the ADC without cables or pre-amplifiers, less power consumption is required to achieve a high resolution, which is the main goal of this project. Considering that the resolution specification of this project is relaxed compared with the one achieved in [33], the resolution target is accessible by integrating the Wheatstone bridge and readout in the same chip while getting rid of the pre-amplifier. Since the output of the bridge is at millivolt level, a delta-sigma ADC based on power-efficient Gm-C integrators is intrinsically suitable to handle a signal swing at such a level.

Based on the discussion above, the Wheatstone bridge is a potential candidate for this project, thus further investigation has been done on this structure.

2.2.1.1 Voltage Output versus Current Output

The output of the Wheatstone bridge can be either voltage or current, as expressed in Equation 2.1 and Equation 2.2, respectively.

$$V_{diff} = V_{dd}\left(\frac{\Delta R + R}{2R + \Delta R} - \frac{\Delta R}{2R + \Delta R}\right) = V_{dd}\frac{\frac{\Delta R}{2R}}{1 + \frac{\Delta R}{2R}} \approx V_{dd}\frac{\Delta R}{2R}\left(1 - \frac{\Delta R}{2R}\right) \tag{2.1}$$

$$I_{diff} = \frac{V_{dd}}{2}\left(\frac{1}{R + \Delta R} - \frac{1}{R}\right) \times 2 = \frac{V_{dd}}{R} \cdot \frac{\frac{\Delta R}{R}}{1 + \frac{\Delta R}{R}} \approx V_{dd}\frac{\Delta R}{R^2}\left(1 - \frac{\Delta R}{R}\right) \tag{2.2}$$

ΔR in Equation 2.1 and Equation 2.2 can be expressed as Equation 2.3.

$$\Delta R = \Delta R_{temperature} + \Delta R_{mismatch} \tag{2.3}$$

In Equation 2.3, $\Delta R_{temperature}$ is caused by temperature variation, which is desired and can be expressed by Equation 2.4; whereas, $\Delta R_{mismatch}$ is caused by process variation, which is undesired; in an ideal case, $\Delta R_{mismatch}$ is zero.

$$\Delta R_{temperature} = \alpha \cdot R_0 \cdot \Delta T \tag{2.4}$$

In Equation 2.4, α is the TC of the silicided poly resistor in the Wheatstone bridge, R is the nominal resistance of the silicided polysilicon resistor at the reference temperature, which is usually the room temperature.

Combining Equation 2.1 and Equation 2.3, Equation 2.2 and Equation 2.3, respectively, it can be seen that the nonlinearity of the current-out bridge is two times worse than that of the voltage-out bridge. Therefore, voltage-readout is preferred to current-readout.

2.2.1.2 Temperature-Sensing Resolution

As presented in Section 2.2.1.1, current-readout is inferior to voltage-readout in terms of linearity, hence only the resolution of voltage-readout is elaborated in this section. The structure of a voltage-readout bridge is shown in Figure 2.6. Its output-referred noise is given by Equation 2.5.

$$\overline{v_n^2} = 4kT\,(R_{ref} \,||\, R(T)) \times 2 \tag{2.5}$$

By combining Equation 2.1 and Equation 2.4, the output voltage-to-temperature sensitivity can be calculated, as given in Equation 2.6.

$$S_T^V = \frac{dV_{out}}{dT} = \alpha \frac{V_{dd}}{2} \tag{2.6}$$

Hence the bridge sensitivity is 2.25 mV/℃.

Based on Equation 2.5 and Equation 2.6, the temperature-sensing resolution is calculated by Equation 2.7.

$$dT = \frac{\sqrt{\overline{v_n^2} \times BW}}{S_T^V} \tag{2.7}$$

Based on Equation 2.7, to achieve <200 μK resolution in a 100-Hz bandwidth, the resistance value of the resistors in the bridge should be no larger than 32 kΩ.

2.2.1.3 Challenges

As discussed in Section 2.2.1.2, a resistor-based temperature sensor configured in a Wheatstone bridge structure can achieve a resolution of 200 μK as long as a proper resistance value is chosen. However, there are at least two challenges in implementing an on-chip Wheatstone bridge.

The first challenge is, due to the process variation, the output of the bridge would always have a random initial output, which is process variation dependent. Resistors fabricated in a CMOS technology suffer a typical process spread of ±40%. The significant process spread involved in the passive components would degrade the temperature-sensing accuracy. To achieve a high accuracy, resistive trimming digital-to-analog converters (DACs) are required in a Wheatstone bridge.

The second challenge is to choose a proper type of resistor as the reference. To achieve a high sensitivity, the TC difference between the reference resistors and the poly resistors with silicide should be maximized. Poly resistors without silicide are the best candidates in terms of sensitivity, which have negative TC. However, as presented in Section 2.1, the poly resistors without silicide have a relatively high flicker noise compared with poly resistors with silicide, which would cause a stability issue. In addition to this, the signal is around DC, so it is necessary to minimize the noise around DC in order to achieve a high temperature-sensing resolution. A typical way to reduce flicker noise is to chop the flicker noise source to modulate the flicker noise out of the signal band. However, in the Wheatstone bridge structure, the flicker noise from the poly resistor is always with the signal. If the bridge is chopped, both the flicker noise and the signal are modulated. Thus, chopping the bridge cannot separate the signal from the flicker noise. Alternatively, diffusion resistors which suffer lower flicker noise may be employed as the reference resistors. However, the TC difference between silicided poly resistor and diffusion resistor is relatively small, thus the corresponding bridge sensitivity would be reduced, leading to an inferior resolution.

Although the significant process spread in the bridge resistors can be tackled by trimming DACs, either a stability problem or a poor sensitivity issue would arise when choosing the reference resistors in the Wheatstone bridge. Therefore, the Wheatstone bridge structure is not the most suitable candidate for this project.

2.2.2 Temperature Sensor Configured in Passive-RC Filter

The impedance of a capacitor can also be used as a reference in a resistor-based temperature sensor. In this case, a well-defined frequency is required. In [15], such a reference is employed to construct a resistor-based temperature sensor, as shown in Figure 2.8.

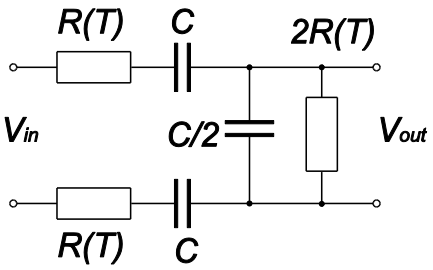

Figure 2.8 A resistor-based temperature sensor with capacitors and a clock as reference [15]

Essentially, the sensor is a passive-RC filter. R(T) is temperature dependent, and C as well as the input signal rarely depend on temperature, leading to an almost temperature-independent reference impedance $\frac{1}{j\omega C}$. When driven by a signal with a certain frequency, the phase shift of the output is temperature-dependent, which is mainly determined by the resistor temperature-dependency. The temperature-dependent phase shift is digitized by a phase-domain delta-sigma modulator.

In the sensor structure configured as a passive-RC filter, the low jitter input and the almost temperature-independent capacitors work together as the reference. Thus the reference is not a flicker noise source any more, unlike the unsilicided polysilicon resistor in the Wheatstone bridge. As elaborated in Chapter 3, the resolution and accuracy of a resistor-based temperature sensor configured as a passive-RC filter can meet the specification of this project in a power efficient way. In addition to that, the process variation of the passive components in the passive-RC filter can be compensated by tuning the driving frequency; no physical trimming DACs are required, which makes the design less complicated and more robust. Therefore, a passive-RC filter is chosen as the sensor structure in this project.

2.3 Summary

In this chapter, available resistors in the technology are investigated in terms of TC, linearity, voltage-dependency and process variation. Based on this, the polysilicon resistor with silicide is chosen as the temperature-sensing component. Afterwards, two resistor-based temperature-sensing structures have been discussed. Due to the flicker issue in the Wheatstone bridge structure, the structure of a passive-RC filter is chosen. In Chapter 3, the design of the temperature-sensing block, the passive-RC filter, is elaborated.

Chapter 3 Wien Bridge Temperature Sensor

As presented in Chapter 2, the reference of a resistor-based temperature sensor configured in a passive-RC filter is flicker noise free; and the significant passive component spread in such a structure can be compensated by tuning the driving frequency. Therefore, a passive-RC filter is chosen as the temperature-sensing structure. In this chapter, the design of the temperature-sensing block is presented. Four main topics are discussed. First, different passive-RC filters are discussed in order to choose the most suitable structure for this project. Second, the type and value of the components in the passive filter are discussed. Third, the jitter requirement of the driving signal is discussed considering the target resolution. Fourth, the driving circuit of the passive filter is discussed considering the stability requirement of this project.

3.1 Sensor Structure

Generally, there are three types of passive RC filters: low-pass, band-pass and high-pass. The low-pass and band-pass filter impose an inherent bandwidth limitation on the thermal noise of the resistors, while the high-pass filter doesn't, so further investigation focuses on the low-pass and band-pass passive filter.

Compared with a low-pass filter, a band-pass filter has a larger phase shift over the industrial temperature range, leading to a higher temperature-sensing sensitivity, thus better resolution. In addition to that, a band-pass filter has a better linearity [15]. With respect to the sensitivity and linearity, the band-pass filter is superior to the low pass filter. Therefore, a band-pass filter is chosen as the sensor structure. This structure is also called Wien Bridge (WB) [15]. It is shown in Figure 3.1.

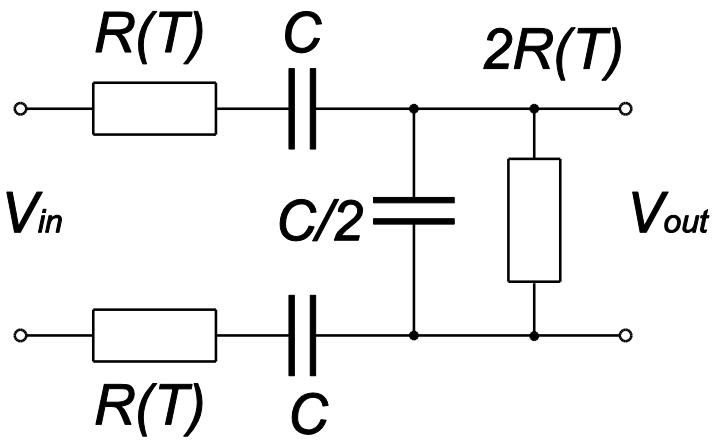

Figure 3.1 Wien Bridge

The transfer function of the Wien bridge filter is given in Equation 3.1 and its phase response can be described by Equation 3.2.

$$H(\omega) = \frac{j\omega RC}{(1 - \omega^2R^2C^2) + 3j\omega RC} = \frac{\omega RC\sqrt{1 + 7\omega^2R^2C^2 + \omega^4R^4C^4}}{1 + 7\omega^2R^2C^2 + \omega^4R^4C^4} \angle - \tan^{-1}\frac{\omega^2R^2C^2 - 1}{3\omega RC} \quad (3.1)$$

$$\varphi_{WB}(\omega) = -\tan^{-1}\frac{\omega^2 R^2 C^2 - 1}{3\omega RC} \tag{3.2}$$

Figure 3.2 shows the bode plot of the Wien bridge. When driven by a sinusoid with $\omega = 1/RC$, the output phase shift of the Wien Bridge is 0 °. And $f_0 = 1/(2\pi RC)$ is called the center frequency of the WB.

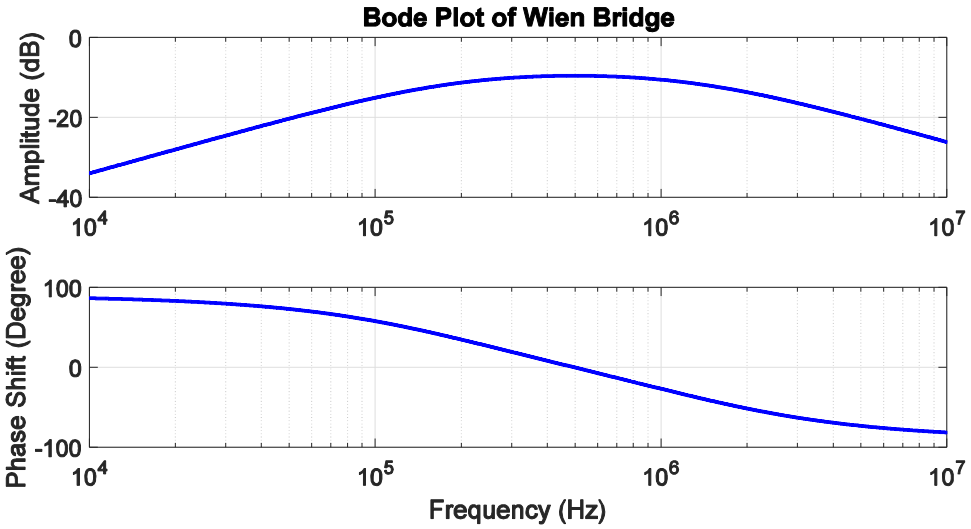

Figure 3.2 Bode plot of the Wien Bridge with $f_0 = 500\ kHz$

According to the phase response given in Equation 3.2, the driving frequency and the resistance in the bridge have identical contribution to the output phase shift in a WB. Therefore, when driven by a fixed frequency, the output phase shift is a function of the resistor value, which is temperature-dependent. According to the bode plot given in Figure 3.2, when driven by a frequency of $1/(2\pi RC)$, the bridge amplitude response is maximized. According to Equation 3.8, Equation 3.12 and Equation 3.14, a high bridge amplitude response leads to a high sensitivity, thus a high temperature-sensing resolution. In addition to that, the phase response at $1/(2\pi RC)$ is steep, which also results in a high sensitivity. Therefore, $1/(2\pi RC)$ is chosen as the bridge driving frequency.

When driven by a sinusoid with a frequency of $1/(2\pi RC)$, the output phase shift of the WB over the industrial temperature range is shown in Figure 3.3. It indicates that over the industrial temperature range, the Wien Bridge has a phase shift of around 14.0 °.

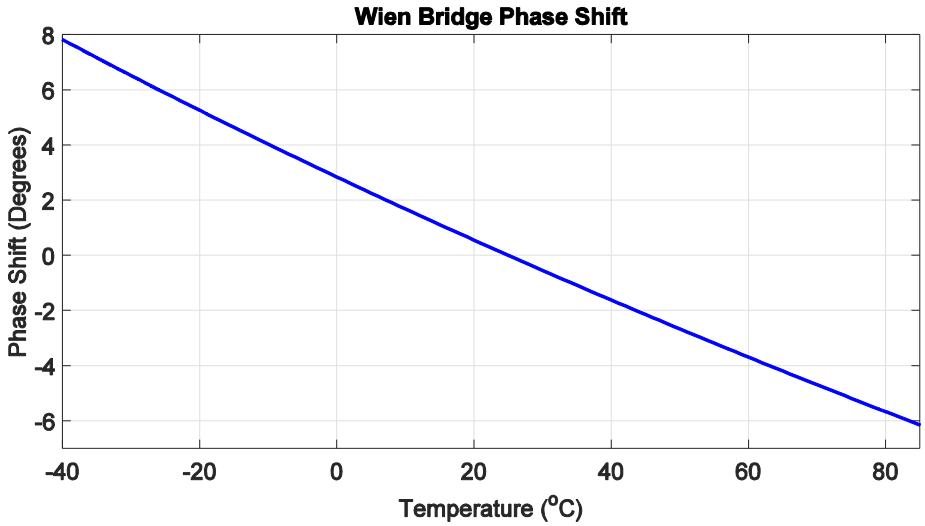

Figure 3.3 The phase shift over the industrial temperature range

When the WB works as a temperature sensor, the residual temperature error after a 2nd order polynomial fitting is plotted in Matlab to estimate its linearity. Its residual error is shown in Figure 3.4. Over the industrial temperature range, the residual error of the Wien Bridge is 0.09 °.

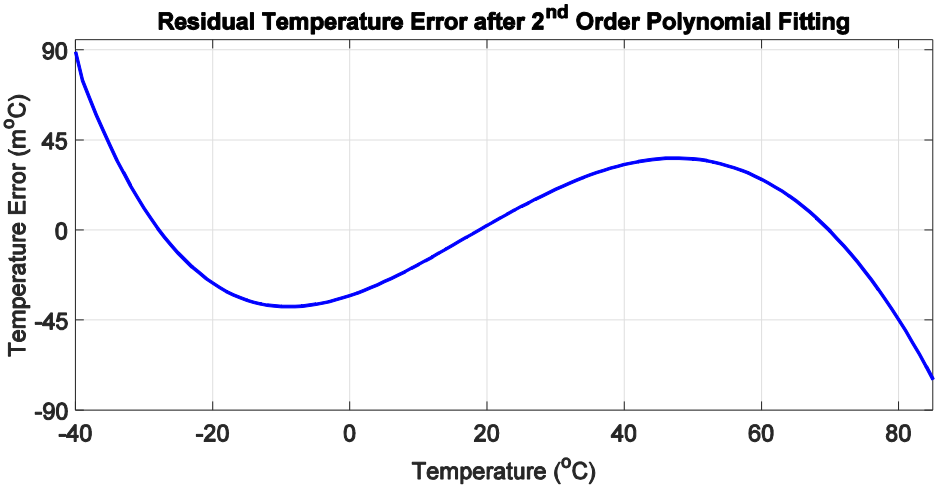

Figure 3.4 The residual temperature error after a 2nd order polynomial fitting

For the Wien Bridge structure, there are two different configurations which implement the same transfer function, as is shown in Figure 3.5. In the structure on the right, the driving circuit needs to drive larger parasitic capacitance, thus the rise/fall time of the driving signal would increase. This leads to extra jitter, which would degrade the performance severely, as will be discussed in Section 3.3. Therefore, the structure on the left is chosen.

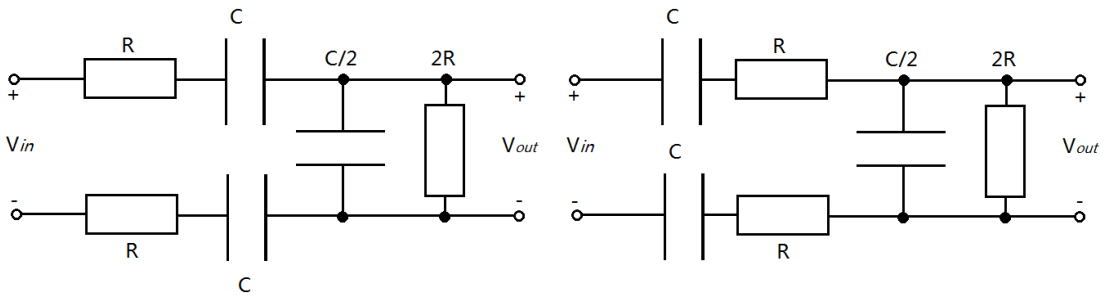

Figure 3.5 Two structures of the Wien Bridge

3.2 Components Used in the Sensor

As presented in Section 3.1, the Wien Bridge structure is chosen as the temperature-sensing structure in this project. The Wien Bridge consists of resistors with a high TC and capacitors with a low TC.

3.2.1 Resistor Type

Based on the reasoning given in Section 2.1, silicided poly resistors are chosen as the bridge resistors. In the technology, there are two types of silicided poly resistors, P+ silicided poly resistor and N+ silicided poly resistor. According to the technology data sheet, their sheet resistances are close to each other, and the TC of an N+ silicided poly resistor is slightly higher than that of a P+ silicided poly resistor. However, the voltage dependency of a P+ silicided poly resistor is much less than that of an N+ silicided poly resistor. In addition to this, the width offset suffered by a P+ silicided poly resistor is less than half of the width offset suffered by an N+ silicided poly resistor. Therefore, a P+ silicided poly resistor rather than a N+ silicided poly resistor is chosen in this application.

3.2.2 Capacitor Type

Two typical types of capacitors prevail in a CMOS process. One is the MOS capacitor, and the other is the metal-insulator-metal (MIM) capacitor. Both of them are available in the technology. Hence, a comparison between these two types of capacitors is needed.

The main difference between these two types of capacitors is the dielectric in the capacitors. For a MOS capacitor, the dielectric is the gate silicon oxide; for the MIM capacitor, the dielectric is the field silicon oxide. The capacitance per unit area can be defined as Equation 3.3, which is inversely proportional to the distance between the two plates of the capacitor. Gate silicon oxide is thinner than the field silicon oxide, thus, the MOS capacitor is denser than the MIM capacitor. Assuming that the MOS capacitor and the MIM capacitor suffer from the same dimension variation, the MOS capacitor presents a larger capacitance variation than the MIM capacitor, *i.e.* the MIM capacitor is more accurate.

$$C = \frac{\varepsilon}{d} \tag{3.3}$$

Another important reason why the MIM capacitors should be used in this project instead of the MOS capacitors is that the temperature dependence of the MIM capacitor is weaker than that of the MOS capacitor in the technology. The weaker temperature-dependency makes the MIM capacitor a good reference in the Wien Bridge temperature sensor.

In addition to that, the two plates in the MIM capacitor are constituted by the top metal layer and the second metal layer counting from top, resulting in less parasitic capacitance. Compared to the MOS capacitor, the MIM capacitor is less voltage dependent. Besides, it should be noted that one of the MOS capacitor plates couples to the substrate. Such coupling would capture noise from the substrate, which is undesired in the low noise design.

Therefore, MIM capacitors are chosen in this project.

3.2.3 Resistor Value

In Chapter 2, the calculation has shown that a resistance of 32 kΩ or less should be used in the Wheatstone bridge to achieve the target resolution. Although a Wien Bridge instead of a Wheatstone bridge is chosen in the end, the resistors with a resistance of 32 kΩ still can provide a resolution of less than 200 μK in a 100-Hz bandwidth, as will be shown below.

The real part of the bridge output impedance at the driving frequency $f_0 = 1/(2\pi RC)$ is given in Equation 3.4.

$$Z_{re} = \frac{2R}{3} \tag{3.4}$$

Therefore, the noise power spectral density of the bridge is given in Equation 3.5.

$$\overline{v_n{}^2} = 4kT\frac{2R}{3} \tag{3.5}$$

To convert the noise voltage to temperature-sensing resolution, the sensitivity of the bridge is required, which can be calculated by Equation 3.6.

$$S_T^V = \frac{dV}{dT} \tag{3.6}$$

where V is the DC voltage acquired by the bridge output being chopped by another square wave. Since V contains the phase shift information caused by the temperature change, introduce the phase shift as the medial variant in Equation 3.6, then the sensitivity can be calculated by Equation 3.7. φ_{WB} in Equation 3.7 is the phase shift when the signal transfers from the input to the output in the Wien Bridge.

$$S_T^V = \frac{dV}{d\varphi_{WB}} \cdot \frac{d\varphi_{WB}}{dT} \tag{3.7}$$

$$V = H_{LPF} \times V_{sq,WB} \times V_{sq,ref} \tag{3.8}$$

In Equation 3.8, H_{LPF} is the transfer function of a low pass filter, of which the -3dB frequency is significantly lower than the center frequency of the Wien Bridge. $V_{sq,WB}$ is the output of the Wien Bridge, and $V_{sq,ref}$ is the phase reference with which the phase shift in the bridge can be defined.

Both the bridge input and the reference are square waves with an amplitude of A and an angular frequency of $\omega_0 = 1/(RC)$. $V_{sq,WB}$ can be expressed as Equation 3.9.

$$V_{sq,WB} = H(\omega) \cdot \frac{4A}{\pi} \sum_{k=1}^{\infty} \frac{\sin[(2k-1)\omega_0 t]}{2k-1} = \frac{4A}{\pi}\left[H(\omega_0)\sin(\omega_0 t) + \frac{H(3\omega_0)}{3}\sin(3\omega_0 t) + \cdots\right] \tag{3.9}$$

$V_{sq,ref}$ is the reference square wave with a phase reference of φ_r, which is calculated by Equation 3.10.

$$V_{sq,ref} = \frac{4A}{\pi} \sum_{k=1}^{\infty} \frac{\sin[(2k-1)\omega_0 t + \varphi_r]}{2k-1} \tag{3.10}$$

By combining Equation 3.2, Equation 3.8, Equation 3.9 and Equation 3.10, V can be expressed as Equation 3.11.

$$V = \frac{8A}{3\pi^2} \cdot \cos(\varphi_{WB} - \varphi_r) \tag{3.11}$$

Therefore, the DC voltage-to-phase sensitivity can be expressed as Equation 3.12.

$$S_\varphi^V = \frac{dV}{d\varphi_{WB}} = -\frac{8A}{3\pi^2} \cdot \sin(\varphi_{WB} - \varphi_r) \xrightarrow{\omega = \omega_0} \frac{8A}{3\pi^2} \cdot \sin\varphi_r \tag{3.12}$$

By combining Equation 2.4 and Equation 3.2, the phase-to-temperature sensitivity can be obtained:

$$S_T^\varphi = \frac{d\varphi_{WB}}{dT} = \frac{d\varphi_{WB}}{dR} \cdot \frac{dR}{dT} = -\frac{2\alpha}{3} \tag{3.13}$$

By combining Equation 3.7, Equation 3.12 and Equation 3.13, the Wien Bridge sensitivity can be expressed as Equation 3.14.

$$S_T^V = -\frac{16A\alpha}{9\pi^2} \sin\varphi_r \tag{3.14}$$

By combining Equation 3.5, Equation 3.6 and Equation 3.14, the temperature-sensing resolution of the Wien Bridge is given in Equation 3.15.

$$dT = \frac{\sqrt{\overline{v_n^2} \cdot BW}}{S_T^V} = -\frac{\sqrt{4kT\frac{2R}{3} \cdot BW}}{\frac{16A\alpha}{9\pi^2}\sin\varphi_r} \tag{3.15}$$

Substituting T = 298 K, R = 32 kΩ, BW = 100 Hz, A = 1.8 V, α = 0.28%/℃, and φ_r = 67.5 °(or 112.5 °) in Equation 3.15, dT = 123 μK, which meets the resolution specification in this project. Hence, R = 32 kΩ is chosen, just the same value as the one used in the Wheatstone bridge.

3.2.4 Capacitor Value

According to Figure 3.3, when the Wien Bridge is driven its center frequency, the phase shift of the output is zero degree, while the amplitude of the output is maximized. When the driving frequency suffers a small offset from the center frequency, the phase shift of the output will present a relatively linear change. The transfer function of the Wien Bridge given in Equation 3.2 indicates that R and ω affect the input signal transfer in an identical way. Thus, when keeping the driving frequency the same, a small resistance change will result in a relatively linear phase shift change, just as when the driving frequency changes while keeping R constant. In other words, the driving signal together with the MIM capacitors works as the reference in the Wien Bridge temperature sensor. As discussed in Section 3.1, the Wien Bridge should be driven by a sinusoid with $f = 1/(2\pi RC)$. However, it is practical to choose a square wave instead of a sinusoid, hence the Wien Bridge will be driven by a square wave with $f = 1/(2\pi RC)$.

Expect the value of R, the value of C needs to be considered. The center frequency f_0 of the Wien Bridge is determined by Equation 3.16.

$$f_0 = \frac{1}{2\pi RC} \tag{3.16}$$

On the one hand, if C is too small, the driving frequency, which is the same as the center frequency, would be relatively high, leading to a severe jitter requirement for the input signal, as will be discussed in Section 3.4. On the other hand, a large C results in large area. To obtain a proper trade-off between the jitter requirement and the area, 500 kHz is chosen as the center frequency of the Wien Bridge. Correspondingly, 10 pF is chosen as the value of C.

3.3 Temperature-Sensing Accuracy

Either voltage or current can be sensed at the output of the WB. In Cadence simulations, when the bridge is driven by an ideal square wave with a period of 2 μs and an amplitude of 1.8 V, the peak value of the output voltage is approximately 700 mV, while the peak value of the output current is approximately 11 μA. Since the output voltage of the WB is too large to be handled linearly by a

normal G_m input stage, its output current is sensed instead.

To estimate the WB temperature-sensing accuracy, an ideal readout is employed to extract the temperature information from the phase shift of the WB output. Implement the WB configuration described above in Cadence, store the corresponding output waveforms, and demodulate the output current into DC value in Matlab. The DC value represents the corresponding temperature. Then employ a 2nd order polynomial to fit the DC value over temperature. The residual temperature error over the industrial temperature range for nominal, fast and slow process corners is shown in Figure 3.6. In the nominal process corner, the residual temperature error is less than ±0.05 ℃. The worst case is located in slow process corner, where the residual error is 0.40 ℃.

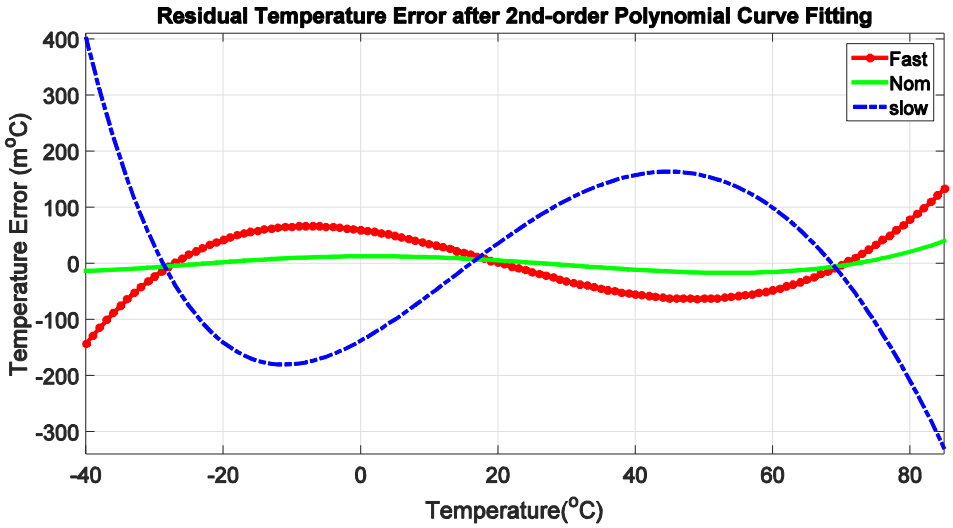

Figure 3.6 Residual temperature error after 2nd order polynomial curve fitting (WB + ideal readout)

3.4 Jitter Requirement for the Master Clock

As discussed before, the square wave together with the MIM capacitors act as the reference in the Wien Bridge. The temperature information is represented by the phase shift caused by the variation of the resistor value over temperature. Therefore, except for the resistor value, all the other components in the WB should be stable; especially the components which would cause a phase error before the signal is demodulated. However, jitter always appears in the driving square wave and the demodulation square wave, which is derived from a master clock.

In order to investigate the jitter requirement for the master clock, a model, including the major jitter sources before the signal being demodulated, is built as shown in Figure 3.7. A master clock generates an 8-MHz square wave. Then the square wave is divided by 16, resulting in a 500-kHz square wave. Several D-flip flops clocked by the 8-MHz master clock delay the 500-kHz square wave, to create its phase-shifted versions at a step of 22.5 °. The output of one D-flip flop acts as the differential input signal of the Wien Bridge, after being buffered and inverted respectively. The outputs of another two D-flip flops work as the chopping signal, which have well-defined phase shifts with respect to the input of the Wien Bridge.

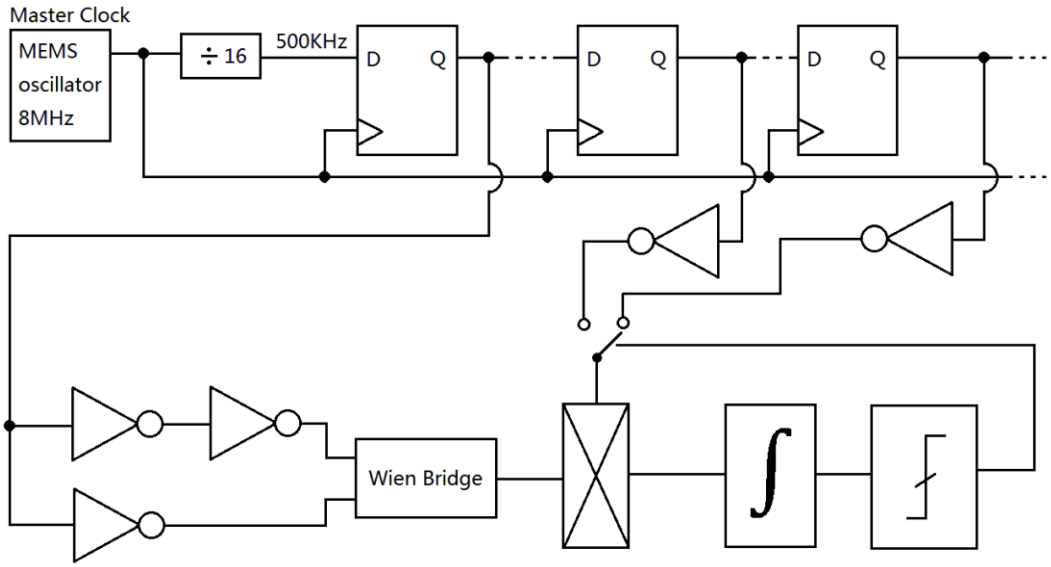

Figure 3.7 Block diagram to model the major jitter sources before chopping

The jitter appearing at the output of the Wien Bridge can be expressed as Equation 3.17.

$$\sigma_{WB}^2 = \sigma_{master}^2 + \sigma_{DFF}^2 + \sigma_{inv}^2 \tag{3.17}$$

The jitter contained in the chopping signal can be expressed as Equation 3.18.

$$\sigma_{CH}^2 = \sigma_{master}^2 + \sigma_{DFF}^2 + \sigma_{inv}^2 \tag{3.18}$$

Therefore, the total jitter involved in the signal path before chopping can be expressed as Equation 3.19.

$$\sigma_{tot}^2 = \sigma_{WB}^2 + \sigma_{CH}^2 \tag{3.19}$$

In order to maintain a temperature sensing resolution of 200 μK in a 100-Hz bandwidth, the temperature sensing error caused by jitter should be much less than 200 μK. To ensure that the jitter does not degrade the resolution, the temperature-sensing error introduced by jitter is constrained to be below 30 μK. Referring to the graph in Figure 3.3, a phase shift of 0.112 ° corresponds to 1 ℃ temperature change in the WB. Thus 30-μK temperature change corresponds to 3.36-μ ° phase shift. Due to the oversampling effect of the phase-domain delta-sigma modulator, the jitter spans a wide bandwidth, thus the phase error before chopping which can be tolerated to maintain the target resolution can be calculated as Equation 3.20.

$$\frac{\frac{\sigma_{max}}{\sqrt{OSR}}}{2us} = \frac{3.36\,u°}{360°} \tag{3.20}$$

To maintain the target resolution, the jitter involved before chopping should be smaller than σ_{max}, as given in Equation 3.21.

$$\sigma_{tot}^2 \leq \sigma_{max}^2 \tag{3.21}$$

Assume that the jitter from a D-flip flop is 30% of that from the master clock, and the jitter from the inverter is 10% of that from the master clock. Combining Equation 3.17 ~ Equation 3.21, it can be calculated that the jitter from the master clock should be no larger than 1 ps. Although this is a tough requirement, it can be met by a commercially available XTAL (crystal) oscillator or a MEMS-based oscillator, *e.g.* the Ultra Performance LVCMOS Oscillator from SiTime [50]. Therefore, the targeted temperature-sensing resolution can be maintained given the phase error caused by the master clock.

3.5 Design of the Bridge Driving Circuit

The bridge is directly driven by CMOS inverters. However, MOSFETs typically suffer from significant flicker noise. Such flicker noise can be reduced by increasing the dimensions of the transistor. Since the drift in this application should be less than 1 m℃/week, the flicker noise corner frequency should be less than 1 mHz.

To determine the width of the transistors in the inverters so that they can deliver the required flicker noise performance, simulations were conducted in Cadence. The result shows that when the width of the NMOS in the driving inverters is 30 μm or larger, the flicker noise corner frequency drops below 1 mHz. A too large width would take up unnecessary area, and load the previous circuit heavily, hence 30 μm is chosen as the width of the NMOSFETs in the driving inverters, and 75 μm is chosen as the width of the PMOSFETs in these inverters.

3.6 Summary

In this chapter, the design of the temperature-sensing block, Wien Bridge, is presented. The components involved in the bridge are discussed, including the resistors, the capacitors and the driving clock. Afterwards, the temperature-sensing accuracy of the Wien Bridge is estimated with an ideal readout. In the end, the design of the bridge driving circuitry is presented. In Chapter 4, the design of the readout circuit for the Wien Bridge is discussed, from system level to transistor level.

Chapter 4 Readout Electronics

In this chapter, the readout circuit for the WB is implemented, which aims to preserve the temperature-sensing resolution provided by the WB in a power-efficient way. First, the system-level design is discussed. Second, the circuit-level design is elaborated.

4.1 System Design

4.1.1 System Architecture

The output of the bridge is phase shifted with respect to the input, and the phase shift represents temperature. A proper readout topology is required to digitize the phase shift.

4.1.1.1 Readout Strategies

A straightforward way to digitize the phase shift is to employ a time-to-digital converter as readout. Since the target resolution is less than 200 μK at T_{conv} = 5 ms, and in the WB 1 ℃ temperature change leads to 0.112 ° phase shift, the required resolution of the time-to-digital converter is around 110 fs, which is difficult to implement according to literature study [51].

Alternatively, the temperature-related phase shift can be first converted into voltage/current domain, and then digitized by a conventional analog-to-digital converter. To convert the phase shift of a square wave into voltage/current domain, multiplication operation is required. One robust and simple way to multiply two signals is by using chopping. In [35], the output of the WB is chopped, and then integrated on a capacitor. The integrated signal is used to control the output frequency of a voltage-controlled oscillator (VCO). Thus the phase shift is first converted into frequency domain, and then digitized by an on-chip counter. To suppress quantization noise, the VCO's output frequency is multiplied by a factor of 9. Essentially, this is over-sampling. But its over-sampling rate is severely limited by the phase noise. In [36], a phase-domain delta-sigma modulator (DSM) is proposed to digitize time information. In [15], such time-to-digital converting strategy is employed. In that literature the output current of a WB is digitized by a 1st order phase-domain DSM.

4.1.1.2 Phase-Domain Delta-Sigma Modulator

The working principle of a phase-domain DSM is the same as that of a conventional DSM. The main difference is that, in a phase-domain DSM, the delta operation is done in the phase domain, which can be easily implemented by a chopper; correspondingly, the feedback digital-to-analog converter (DAC) in a phase-domain DSM should provide a phase reference chosen by the output bit(s) of the quantizer.

4.1.1.2.1 Delta-Sigma Modulator

Benefitting from the advanced CMOS process, a DSM is able to implement a high resolution by trading off speed for resolution. Since the signal bandwidth in this application is a few Hz near DC, even using the modest frequency as sampling frequency would lead to a high over-sampling rate. In other words, high resolution is accessible with a phase-domain DSM in this application. Given that achieving a high temperature-sensing resolution is the main challenge in this project, a phase-domain DSM is chosen as the readout.

The block diagram of a delta-sigma ADC is shown in Figure 4.1. It consists of a loop filter, a low-resolution ADC and a feedback DAC. The embedded ADC works at a much higher frequency than the Nyquist sampling frequency, which is called oversampling. The output of a delta-sigma ADC is generated by utilizing its preceding input values, which indicates that such data converter requires memory elements in its structure, *i.e.* the loop filters in the forward path of the loop. Thus the digital output contains a delayed, but unchanged replica of the input signal, as well as a high-pass filtered version of the quantization noise, which is called noise shaping [37].

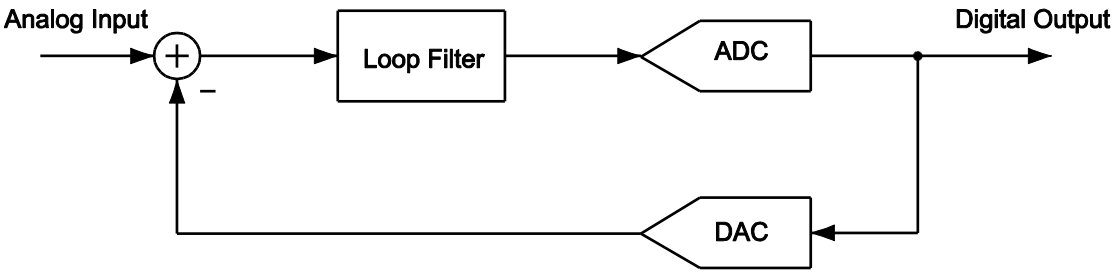

Figure 4.1 Block diagram of a delta-sigma ADC

4.1.1.2.1.1 Loop Filter

In general, there are two kinds of loop filter implementations. One is to implement the loop filters with switched-capacitor (SC) circuits; the other is with continuous-time (CT) circuits. The equations that describe an SC circuit are independent of the clock frequency, so the transfer function of an SC circuit scales naturally with different clock frequency. In contrast, the time constant of a CT filter does not track the clock frequency [37].

Despite the clock frequency dependency of their transfer functions, CT delta-sigma ADCs have two significant advantages. First, a CT modulator is inherently anti-aliasing. The alias is suppressed at the same degree as that of quantization noise. Compared with SC loop filters, CT loop filters postpone the sampling operation till the output of the loop filters. Consequently, the unfavourable effects of sampling, like noise folding, occur at the less sensitive point of the loop [37]. Therefore, no anti-aliasing filters are needed in CT modulators, which makes them more power efficient compared with their SC counterparts. Second, in a CT modulator, the theoretical limitation on the sampling frequency is imposed by the regeneration time of the quantizer and the update time of the feedback DAC [37]; whereas, in an SC modulator, the sampling frequency is limited by the unity-gain frequency of the Op-Amps in the loop. Hence, a CT modulator with slower Op-Amps suffers the same amount of

error caused by a finite bandwidth as an SC modulator with relatively faster Op-Amps. This indicates that less power is required in a CT modulator given the trade-off between power and speed. Since this project targets at low power consumption, a CT delta-sigma ADC is chosen rather than its SC counterpart.

4.1.1.2.1.2 Quantizer

As long as the loop filters have a high gain in the signal band, the in-band quantization noise would be strongly attenuated. The embedded ADC is not necessary to be accurate, because any non-ideality from the embedded ADC will be suppressed in the signal band, just as the quantization noise. The nonlinear distortion from the feedback DAC, however, appears at the output without shaping. Therefore, the linearity of the feedback DAC is one major limitation on the converting performance. To address this problem, single-bit quantization is chosen in the project. Because single-bit quantization requires a sing-bit DAC, of which the transfer characteristics only contains two points, leading to an inherently linear DAC operation [37].

4.1.1.2.1.3 Modulator Order

Based on the noise shaping capability, DSMs with different orders are defined. 1st order DSMs are simple, robust and stable. However, the dead zones appearing in 1st order DSMs severely limit the attainable resolution and the leaky behaviour of the integrator degrades the theoretical noise shaping process [15]. Both the dead zones and the integrator leaky behaviour are caused by the finite Op-Amp DC gain in the integrator. Thus they can be suppressed by increasing the loop filter DC gain. In a 1st order DSM only one integrator is employed. In order to increase the DC gain of the Op-Amp, multi-stage or gain-boosting technique can be used. However, given the loop stability, the speed of the Op-Amp does matter except its DC gain. It is difficult to implement one Op-Amp which is able to provide high DC gain and high speed at the same time with relatively low power consumption.

Alternatively, a 2nd order DSM is chosen in this project. The signal transfer function (STF) of a 2nd order DSM is identical to that of a 1st order DSM at the signal band, which is usually 1; whereas its noise transfer function (NTF) is the squared version of the NTF of a 1st order DSM. Hence, the slope of the NTF at low frequency is 40 dB/decade for a 2nd order DSM while it is 20 dB/decade for a 1st order DSM. This indicates that an increased attenuation of quantization noise at low frequency can be expected from a 2nd order DSM. It should be noted that since the NTF gain of a 2nd order DSM at high frequency is larger than that of a 1st order DSM, the total power of the quantization noise at the output of a 2nd order DSM is higher than that of a 1st order DSM [37].

4.1.1.2.1.4 Compensation in a 2nd Order Delta-Sigma Modulator

The tolerance for a finite Op-Amp DC gain in a 2nd order DSM is increased because the cascade of two integrators squares one Op-Amp's DC gain. However, a 2nd order DSM tends to be less stable. Compensations are required to keep a 2nd order DSM stable. Feedback compensated structure and

feedforward compensated structure are proposed in literature, as shown in Figure 4.2. Assuming that these two structures have the same NTF, the STF of the feedback compensated structure has a flat response which is able to provide more filtering to interference; whereas, in the feedforward compensated structure, the feedforward branch adds a zero to its STF [38], which reduces the interference filtering capability by one order and creates a small peak around the cut-off frequency of its STF. Although at relatively high frequency the interference filtering capability of a feedforward structure is degraded by a zero, since the signal band in this application is only 100 Hz, such a high frequency STF peak (out-of-band peak) barely affects the modulator's low frequency performance. Moreover, feedforward path C_1 in Figure 4.2 b) helps reduce the signal swing at the output of the 1st integrator, thus less power consumption is required in a feedforward structure than in a feedback structure. In order to minimize the power consumption while maintaining the readout performance, a feedforward compensated structure is chosen in this project.

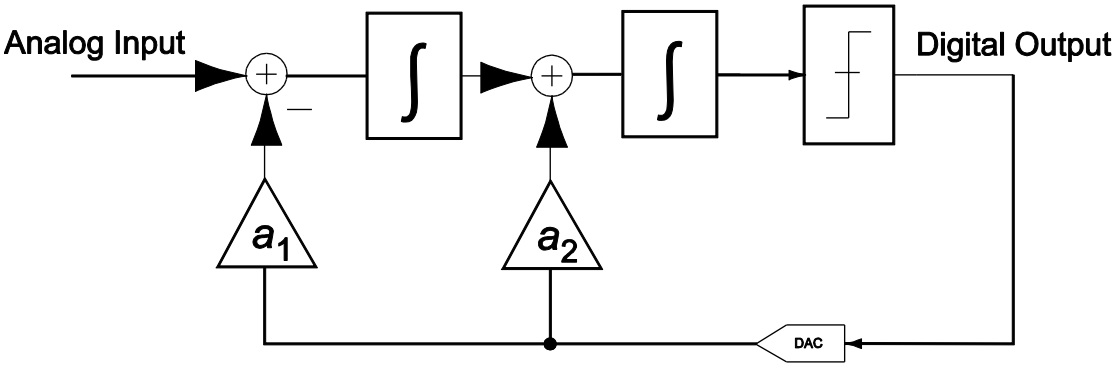

Figure 4.2 a) Feedback 2nd order CT DSM [37]

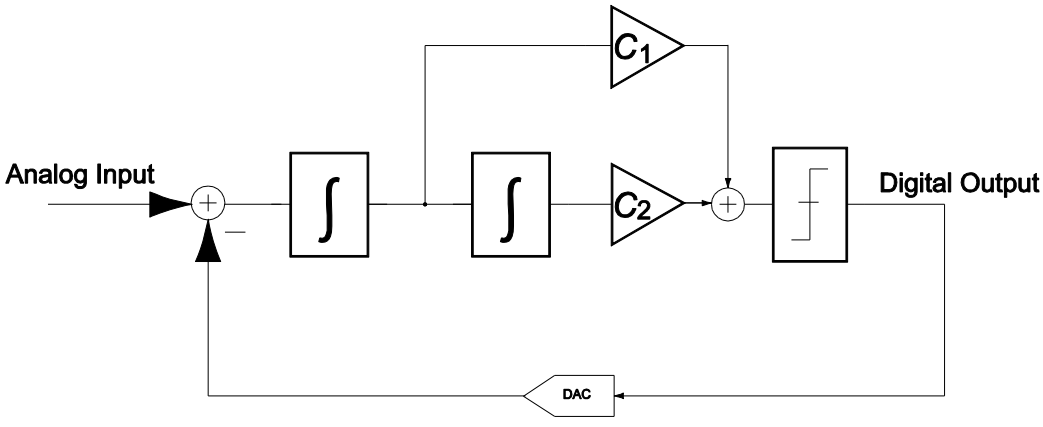

Figure 4.2 b) Feedforward 2nd order CT DSM [37]

4.1.1.2.2 Phase-Domain 2nd Order 1-Bit Feedforward Delta-Sigma Modulator

Since the temperature information to be digitized is in phase domain, the delta node in the conventional DSM structure needs to be modified to implement phase subtraction. For a square wave, multiplication combined with filtering can implement phase subtraction; in the DSM, however, there are subsequent loop filters already, hence only the multiplication operation is required before the loop filters. The

phase-domain DSM used as the readout in this project is shown in Figure 4.3.

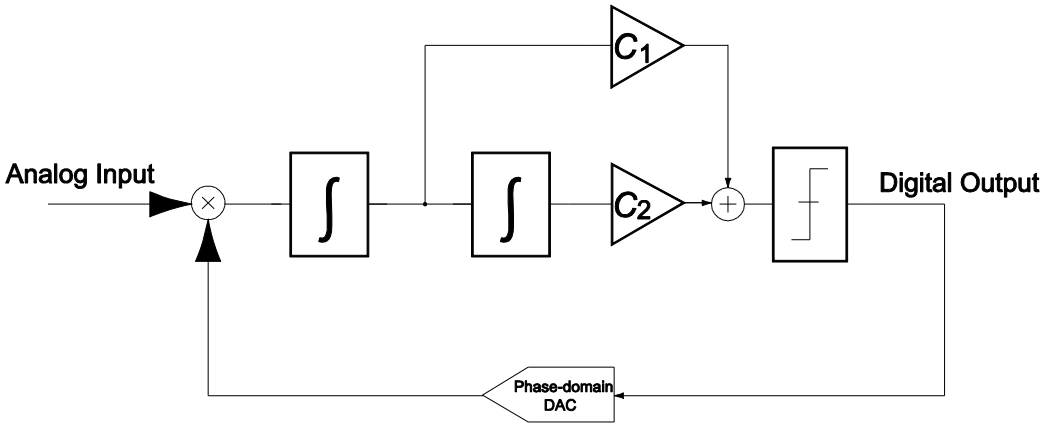

Figure 4.3 Phase-domain feedforward 2nd order CT DSM

Two integrators are incorporated in the readout. Since the linearity of the first integrator is more important than that of the 2nd integrator, an active-RC integrator is chosen as the 1st integrator; meanwhile, a G_m-C integrator is used as the 2nd integrator, which is faster although less linear compared with an active-RC integrator. The 1-bit quantizer is implemented by a comparator. Its sampling frequency is chosen to be equal to the WB driving frequency, *i.e.*, 500 kHz. The available data-acquisition board (DAQ) is able to capture bit-streams at such rate; hence no physical decimation filters are required in the readout circuits.

4.1.1.3 Low Frequency Noise Modulation

In the readout, system-level chopping is employed to modulate the low frequency noise in the readout, *e.g.* flicker noise and offset, out of the signal band. The modulator should start from an initial state of zero at each of the system-level chopping phases, thus reset switches should be added at the outputs of the two integrators.

4.1.1.4 Ambient Temperature Fluctuation Suppression

Considering that the targeted resolution is sub-mK, the ambient temperature should be sufficiently stable. In order to suppress the ambient temperature fluctuation, two identical sensors are placed in proximity in one chip [52]. By sensing the difference of their outputs, the ambient temperature fluctuation can be suppressed as a common-mode variation.

4.1.2 Digital Output Interpretation

The readout will generate a sequence of bit-stream at the rate of 500 kHz, and the average of the bit-stream captured within the conversion time is a representation of the temperature. In this section, the quantitative relation between the bit-stream average and the measured temperature is discussed.

The block diagram of the entire smart sensor system is shown in Figure 4.4. A clock generating block is implemented to provide the WB driving signal and the two phase references in the phase-domain DAC. All of them are square waves and have the same frequency, *i.e.* the center frequency of WB at room temperature, but different phase shifts. The function *f* in the clock generating block in Figure 4.4 is the square wave function.

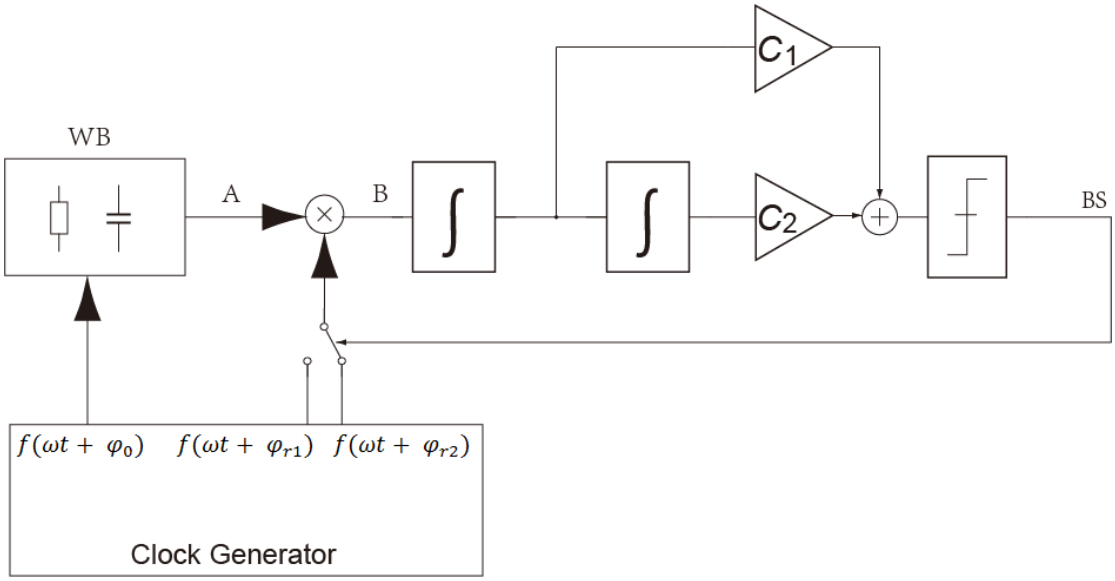

Figure 4.4 Block diagram of the smart sensor system

Driven by the square wave $f(\omega t + \varphi_0)$, the WB outputs a band-pass filtered version of the square wave, *i.e.* $h(\omega t + \varphi_0 + \varphi_{WB})$. According to the WB Bode plot in Figure 3.3, although $f(\omega t + \varphi_0)$ contains components with radian frequencies of $\omega, 3\omega, 5\omega, \cdots$, after filtered by the WB, the amplitude of the harmonic components is highly suppressed. Hence it is fair to express the signal at Point A in Figure 4.4 as $A' \sin(\omega t + \varphi_0 + \varphi_{WB})$ approximately. The signal at Point A will be multiplied by one of the phase references determined by the output of the comparator. The waveform at Point B in Figure 4.4 can be expressed as Equation 4.1, where R is a constant resulting from the Taylor expansion of the reference square wave.

$$i_B = A' \sin(\omega t + \varphi_0 + \varphi_{WB}) \cdot R \sum_{k=1}^{\infty} \frac{sin[(2k-1)\omega t + \varphi_{ri}]}{2k-1} \tag{4.1}$$

Due to the low-pass characteristic of the loop filters, the charge accumulated by the loop filters in one sampling cycle can be expressed as Equation 4.2, where C is a constant.

$$q_{T_s} = C \cdot \cos(\varphi_0 + \varphi_{WB} - \varphi_{ri}) \tag{4.2}$$

The feedback loop in the DSM is to balance the total charge accumulated by the loop filters. The average charge accumulated on the loop filters within the conversion time should be zero, which can be

expressed as Equation 4.3.

$$\mu \cdot C \cdot \cos(\varphi_0 + \varphi_{WB} - \varphi_{r1}) + (1 - \mu) \cdot C \cdot \cos(\varphi_0 + \varphi_{WB} - \varphi_{r2}) \approx 0 \qquad (4.3)$$

Where μ is a rational number which is greater than 0 and less than 1. It equals to the average of the bit-stream sequence captured within the desired conversion time, assuming the two output states of the quantizer is 0 and 1. Equation 4.3 indicates that the phase shift caused by the WB, φ_{WB}, is the weighted average of the two phase references, φ_{r1} and φ_{r2}, and the weight is a function of μ. Therefore, μ can be a representative of φ_{WB}, as shown in Equation 4.4. Meanwhile, φ_{WB} is a representative of temperature; hence, μ is a representative of the temperature to be measured.

$$\mu \approx \frac{\cos(\varphi_0 + \varphi_{WB} - \varphi_{r2})}{\cos(\varphi_0 + \varphi_{WB} - \varphi_{r2}) - \cos(\varphi_0 + \varphi_{WB} - \varphi_{r1})} \qquad (4.4)$$

When the variable closes to 90 °, cosine function can be linearized. Then a linear relation between μ and φ_{WB} can be obtained, as shown in Equation 4.5.

$$\mu \approx \frac{\varphi_{WB} + \varphi_0 - (\varphi_{r2} + 90°)}{\varphi_{r1} - \varphi_{r2}} \quad when \quad \varphi_{WB} + \varphi_0 - \varphi_{ri} \; close\; to\; 90°, \qquad i = 1,2 \qquad (4.5)$$

Over the industrial temperature range, φ_{WB} is between -7 ° to 8 ° at the nominal process corner according to the simulation. Hence the phase shift relation between the bridge driving signal and the references in the phase-domain DAC should meet Inequality 4.6 and Inequality 4.7.

$$\varphi_{r1} - \varphi_0 < 82° \qquad (4.6)$$

$$\varphi_{r2} - \varphi_0 < 97° \qquad (4.7)$$

Driven by a rail-to-rail square wave (±1.8 V), the amplitude of the Wien Bridge output voltage is approximately 0.35 V, which is too large to be linearly handled by a conservative integrator. Therefore, the output current of the Wien Bridge is sensed instead of the output voltage.

4.1.3 Noise Budget

The total noise in the system determines the temperature-sensing resolution. Both the WB and the readout generate noise. In order to preserve the resolution provided by the WB, the noise from the readout should be less than that from the WB. Given the power efficiency target, the noise in the readout should be dominant by the thermal noise rather than the quantization noise. Because to suppress the thermal noise requires more power consumption than to suppress the quantization noise, and employing a 2nd order DSM helps suppress the quantization noise.

The noise from the WB is expressed as Equation 3.5, and the equivalent temperature-sensing resolution is calculated by Equation 3.15, which is 123 μK. Hence in the readout, the temperature-sensing resolution should be less than 123 μK. According to Equation 3.13, 1 ℃ temperature change

corresponds to 0.112 °phase shift caused by the WB. To preserve the resolution of 123 μK, the readout should provide a dynamic range (DR) of 130dB. Thus the thermal noise floor of the readout should be below -130 dB, and the quantization noise should be lower than the thermal noise. For an L^{th} order DSM with a B-bit quantizer, the signal-to-quantization-noise ratio (SQNR) can be calculated by Equation 4.8 [37].

$$SQNR = 10log_{10}\left[\frac{3\pi}{2}(2^B - 1)^2 \cdot (2L+1) \cdot \left(\frac{OSR}{\pi}\right)^{2L+1}\right] \quad (4.8)$$

With B = 1 and L = 2, a SQNR of higher than 130dB can be achieved. Therefore, the readout noise will be dominated by the thermal noise. Since the voltage noise spectral density of the WB is 18.5 $nV/\sqrt{Hz}$ (rms) according to Equation 3.5, the thermal noise spectral density of the readout should be less than this value. Since the noise performance of the first stage in the readout dominates the noise performance of the entire readout, the input-referred noise of the first readout stage should be less than 18.5 $nV/\sqrt{Hz}$ (rms).

4.2 Circuit Design

4.2.1 Demodulator Design

The temperature information sensed by the WB is presented as its output phase shift. To convert the phase shift into current, a chopper is employed. A chopper with ideal switches is shown in Figure 4.5. Signal polarity is switching constantly, which is controlled by the chopping clock.

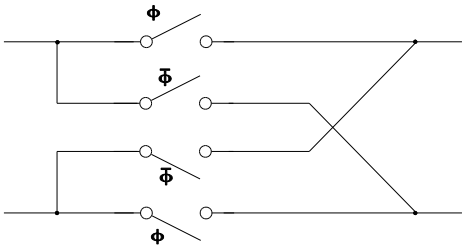

Figure 4.5 A chopper with ideal switches

Compared with ideal switches, switches implemented by MOSFETs suffer from non-zero on-resistance and finite off-resistance. In addition to that, when the MOSFETs are switching, charge injection occurs. This is caused by clock feed-through and channel charge redistribution.

To minimize the unfavourable behaviours during the chopping operation, CMOS switches are used, *i.e.*, switches implemented by PMOSFETs and NMOSFETs in parallel. The on-resistance of a CMOS switch is reduced. Moreover, both clock-feedthrough and channel charge distribution can be reduced. Since PMOSFETs and NMOSFETs require the inverse clock phases when they are in the same state (on/off), clock-feedthrough will induce charge with opposite polarities both at their source and drain. The charge with opposite polarities can be partially cancelled with each other. In addition to this, when a CMOS switch is switched off, the distributed charges from the PMOSFET and from the NMOSFET

are with opposite polarities. They also will be partially cancelled with each other.

The charge injection cannot be totally eliminated; hence certain inaccuracy is added to the demodulated WB output due to the chopping behaviour. Such inaccuracy can be reduced by the multiple-point trimming during data processing.

4.2.2 First Integrator Design

As discussed in previous section, since the output voltage of the WB is too large to be linearly handled by a conventional operational transconductance amplifier (OTA), the output current is sensed by the readout circuits.

4.2.2.1 Integrator Topology Choosing

In [15], a 1st order phase-domain DSM is employed to digitize the WB output. To minimize the readout power dissipation, a passive integrator which consists of a current buffer and an integrating capacitor is used, as shown in Figure 4.6. The dominant noise source in [15] is the quantization noise caused by the leaky behaviour of the passive integrator. Besides, the thermal noise of the current-buffer is 3.5 times larger than the thermal noise of the Wien Bridge.

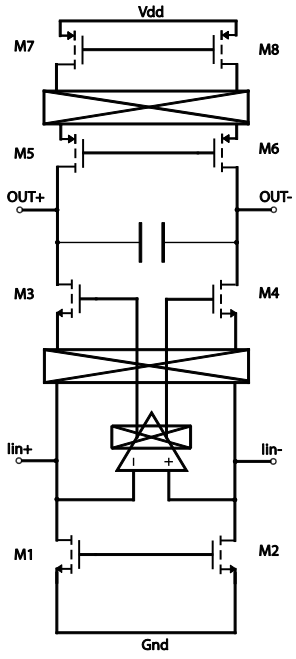

Figure 4.6 Passive integrator [15]

In the passive integrator used in [15], the top and bottom current sources are the dominant noise sources, and the noise from the gain-boosting can be neglected. Hence its input-referred current noise power density can be expressed as Equation 4.9, assuming that the half-circuit is considered. In the equation, g_{mi} is the transconductance of M_i, and γ is determined by process.

$$\overline{i_n^2} = 4kT\frac{\gamma}{g_{m1,2}}{g_{m1,2}}^2 + 4kT\frac{\gamma}{g_{m7,8}}{g_{m7,8}}^2 = 4kT\gamma\cdot(g_{m1,2} + g_{m7,8}) \quad (4.9)$$

Since the transconductance of a MOSFET increases when its source-drain current increases, Equation 4.9 indicates that the input-referred noise of the current buffer will increase as the current increases. In order to ensure that the noise from the readout circuit is no more than that from the bridge itself, the current in one branch of such integrator should be less than 1.4 μA; however, the simulated output current of one branch of the WB at the nominal process corner is 22 μA (peak-to-peak), which sets the minimal current in one branch of the current buffer in order to remain the top and bottom current sources in saturation region.

If a similar passive integrator is used in this design, on the one hand, in order to handle the bridge current, the bias current for each branch in the current buffer should be at least 22 μA; on the other hand, to reduce the thermal noise from this integrator, the bias current in the current buffer needs to be reduced. Therefore, either non-linearity or thermal noise issue would arise if a similar integrator structure is employed.

To keep the noise from the current buffer lower than that from the bridge while ensure that the bias current is able to handle the bridge output, resistors can be added at the source terminals of the transistors which work as current sources in the current buffer [35]. The source resistors help form a negative feedback loop to suppress the noise from the current source. However, they will reduce the integrator output voltage headroom.

To avoid the contradiction between linearity and noise, a passive integrator should not be used in this project. Hence, active integrators are investigated. There are mainly two types of active integrators, active RC-integrators and G_m-C integrators. Compared with G_m-C integrators, active RC integrators are much more linear because they convert voltage into current by resistors; whereas, G_m-C integrators convert voltage into current by transistors. Since any non-linearity introduced by the first stage in a DSM cannot be suppressed by the loop, an active-RC integrator is chosen as the first stage in this design due to its better linearity.

In order to extract the temperature information stored in phase domain, the current from the WB needs to be multiplied by one of the phase reference selected by the quantizer output before being integrated. In this design, the multiplication operation is implemented simply by chopping. The chopper to perform the chopping function is described in Section 4.2.1.

In the active-RC integrator, there are two positions where a chopper may be located. One is between the bridge output resistor and the virtual ground of the OTA, and the other position is between the virtual ground of the OTA and the integrating capacitor. Since the WB also needs the virtual ground to convert the output voltage into the output current, and the former option would disturb the virtual ground of the WB, the latter position is chosen. The bridge resistors are re-used as the resistors in the active-RC integrator. The structure of the first integrator with an inserted chopper is shown in Figure 4.7.

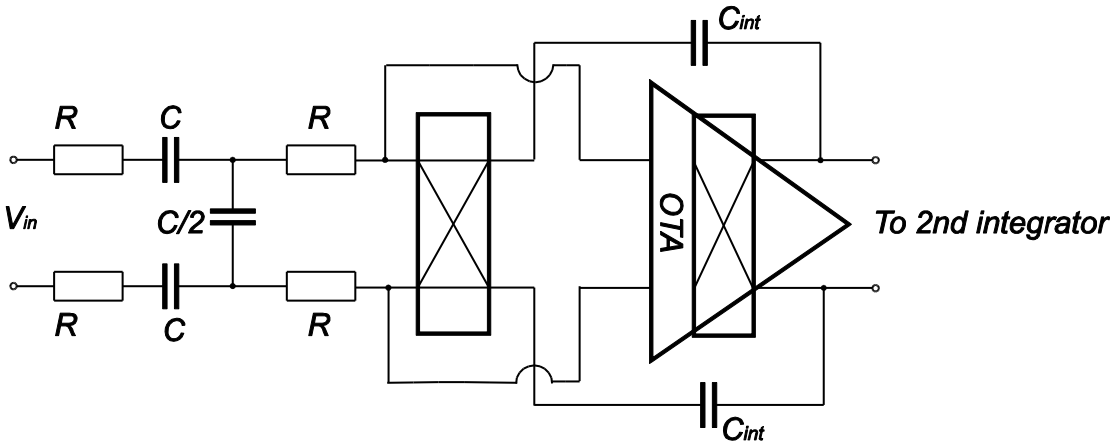

Figure 4.7 First stage in the readout with demodulators inserted

In order to maintain the feedback polarity, except the demodulator which demodulates the temperature information from driving frequency to DC, another demodulator is required in the signal path of the OTA.

4.2.2.2 Active-RC Integrator Characteristic

The transfer function of an active-RC integrator with an ideal OTA is given in Equation 4.10.

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{1}{sRC} \equiv \frac{\omega_u}{s} \quad , \quad \omega_u = \frac{1}{RC} \tag{4.10}$$

Where ω_u is defined as the unity-gain frequency of the integrator.

However, in an active-RC integrator with a practical OTA, a right-half plane zero appears. The transfer function of an active-RC integrator with a practical OTA is given in Equation 4.11.

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{-sC + 2g_m}{sC(1 + 2g_m R)} \approx \frac{\omega_u}{s}\left(1 - \frac{sC}{2g_m}\right) \tag{4.11}$$

The right-half plane zero is located at $s_z = +2\,g_m/C$, as shown in Figure 4.8 A right-half plane zero causes the gain magnitude rising at 20 dB/decade above the zero frequency with an associated phase lag of 90 °, which may cause instability in the feedback loop.

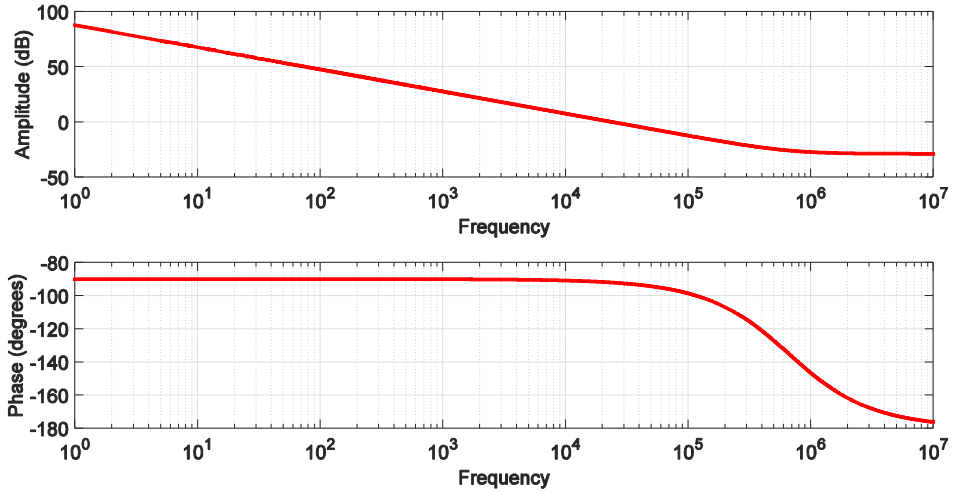

Figure 4.8 Bode plot of an active-RC integrator with real OTA

In order to cancel the right-half plane zero, an extra resistor is placed in series with the integrating capacitor in the feedback path of the active-RC integrator. Then the transfer function can be expressed as Equation 4.12.

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{sC(2R_z g_m - 1) + 2g_m}{sC(1 + 2Rg_m)} \approx \frac{\omega_u}{s}\left[1 + sC\left(R_z - \frac{1}{2g_m}\right)\right] \qquad (4.12)$$

Therefore, in theory, the right-half plane zero can be cancelled by placing a resistor with a resistance of $1/(2g_m)$ in series with the integrating capacitor. The Bode plot after the right-half plane zero cancellation is shown in Figure 4.9. However, due to mismatch, it is possible that the right-half plane zero would be moved to a high frequency instead of being total cancelled. As long as the right-half plane zero is out of the signal band, it is benign.

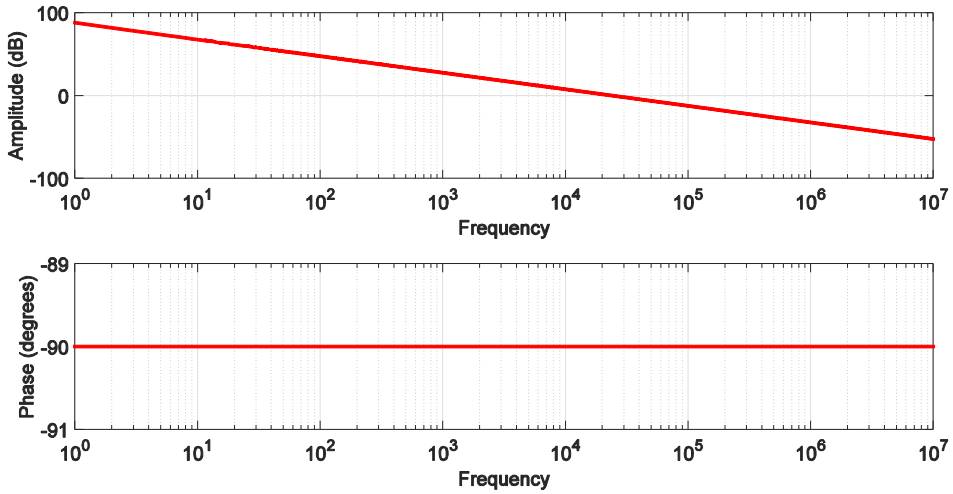

Figure 4.9 Bode plot of an active-RC integrator with real OTA after right-half plane zero cancellation

4.2.2.3 OTA Design

4.2.2.3.1 OTA Structure Choosing

The thermal noise from the readout should be lower than that from the WB, so the WB's inherent temperature-sensing resolution can be preserved. In a 2nd order DSM, the noise from the first integrator will not be suppressed by the loop, hence choosing a proper OTA structure for the first integrator which is able to provide the best noise performance in a power efficient way is essential.

The structure of the OTA in the first integrator is chosen based on the required current level of different OTA structures when their input-referred noise is no more than that of the WB. Three basic structures of Op-Amp are given in Figure 4.10. And the input-referred noise of the telescopic Op-Amp is given in Equation 4.13, the input-referred noise of the folded-cascode Op-Amp is given in Equation 4.14, and the input-referred noise of the two-stage Op-Amp is given in Equation 4.15.

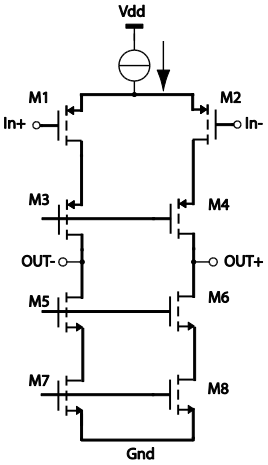

Figure 4.10 a) Telescopic Op-Amp

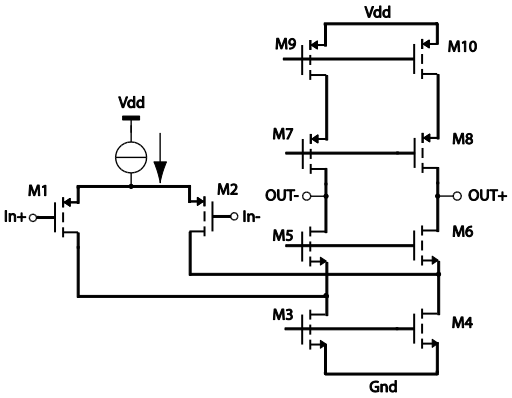

Figure 4.10 b) Folded-cascade Op-Amp

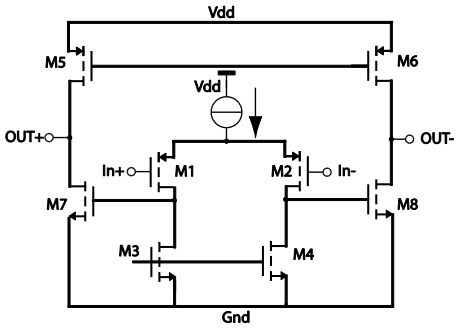

Figure 4.10 c) Two-stage Op-Amp

Figure 4.10 Three basic structures of Op-Amp

$$\overline{v_{n,tele}^2} = 2 \cdot 4kT\gamma \left(\frac{1}{g_{m1,2}} + \frac{g_{m7,8}}{g_{m1,2}^2} \right) \tag{4.13}$$

$$\overline{v_{n,fold}^2} = 2 \cdot 4kT\gamma \left(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}}{g_{m1,2}^2} + \frac{g_{m9,10}}{g_{m1,2}^2} \right) \tag{4.14}$$

$$\overline{v_{n,twoStage}^2} = 8kT\gamma \left(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}}{g_{m1,2}^2} + \frac{\frac{1}{g_{m7,8}} + \frac{g_{m5,6}}{{g_{m7,8}}^2}}{g_{m1,2}^2 \left(r_{o1,2} \,||\, r_{o3,4} \right)^2} \right) \approx 8kT\gamma \left(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}}{g_{m1,2}^2} \right) \tag{4.15}$$

The noise of the WB can be expressed as Equation 3.5. To preserve the temperature-sensing resolution of the WB, the thermal noise from the first OTA in the readout should be lower than that from the WB, which can be described mathematically as Equation 4.16. To minimize the power consumption of the readout, the most favourable state given the noise-power trade-off is that the noise from the readout equals to that from the WB, described by Equation 4.17.

$$\overline{v_{n,OTA1}^2} \leq \overline{v_{n,WB}^2} \tag{4.16}$$

$$\overline{v_{n,OTA1}^2} = \overline{v_{n,WB}^2} \tag{4.17}$$

To meet the condition described by Equation 4.16, the minimum current consumption of the telescopic Op-Amp is 18.8 μA. Comparing Equation 4.14 with Equation 4.13, it is apparent that to achieve the same noise performance, a folded-cascode Op-Amp requires at least twice of the current consumed by a telescopic Op-Amp; Comparing Equation 4.15 with Equation 4.13, it shows that if the first stage in a two-stage Op-Amp is driven by the same amount of current as used in a telescopic Op-Amp, it is able to achieve the same noise performance as a telescopic Op-Amp. However, even though the noise from the second stage is less significant in a two-stage Op-Amp, extra current is demanded in this stage. Hence the total current consumption of a two-stage Op-Amp is higher than that of a telescopic Op-Amp.

Based on these three basic Op-Amp structures, gain-boosting can be introduced. The extra noise generated by a gain-booster depends on its structure. In general, the noise from a gain-booster would be attenuated by the high source-drain impedance of MOSFETs, thus the dominant noise source is in the basic structure rather than in the gain-booster. However, gain-booster demands extra current, which is not favourable in this application where power consumption is one of the major concerns.

With respect to the noise-power trade-off, the telescopic Op-Amp is superior to the other two candidates. However, due to the use of cascode transistors in both PMOS and NMOS sides, the output swing of a telescopic Op-Amp is limited, which can be calculated by Equation 4.18, where $V_{OD,i}$ is the overdrive voltage of MOSFET *i* in Figure 4.10 a), and $V_{OD,CS}$ is the overdrive voltage of the current source.

$$V_{sw} = 2 \times \left[V_{dd} - \left(V_{OD,1,2} + V_{OD,3,4} + V_{OD,5,6} + V_{OD,7,8} + V_{OD,CS} \right) \right] \tag{4.18}$$

For an Op-Amp used in an active RC integrator, its output swing not only depends on the implementation of the Op-Amp, but also depends on the integrating capacitance in the integrator. To

squeeze the output swing of the Op-Amp within the linear range, the transistors in the Op-Amp need to be carefully sized; meanwhile, the integrating capacitance is chosen such that the Op-Amp output is not too large to be distorted.

It is worth to note that the feedforward path in the DSM will also help reduce the output swing of the first integrator.

Except the limited output swing, a telescopic Op-Amp has another drawback, which is the difficulty in shorting its output and input. However, the output and the input of the Op-Amp used in the active-RC integrator will not be shorted. Hence this drawback of a telescopic Op-Amp is not a concern in this application.

Based on the reasoning presented above, a telescopic Op-Amp is used in the first integrator.

4.2.2.3.2 Current Budget

According to Equation 4.13 and 4.17, to remain the temperature-sensing resolution of the WB, the minimum current consumption of the telescopic OTA is 18.8 μA. Given that the output peak current of the WB at each terminal is 11 μA at the typical process corner in simulation, 20 μA current is allocated to each branch in the telescopic OTA to ensure that the OTA can linearly handle the current from the WB over the process corners. 2.5 μA current is allocated to each biasing branch.

Since the current allocated to the OTA is larger than the minimum amount that demanded to supress its thermal noise to the same level as the thermal noise of the WB, the thermal noise from the OTA is actually smaller than that from the WB.

4.2.2.3.3 Front-End Loading Effect

The readout front-end (FE) loads the WB, which will add spread to the WB temperature dependency. The interface between the WB and FE is shown in Figure 4.11, where *k* is the ratio between the FE equivalent input impedance and the resistance of one resistor in the WB.

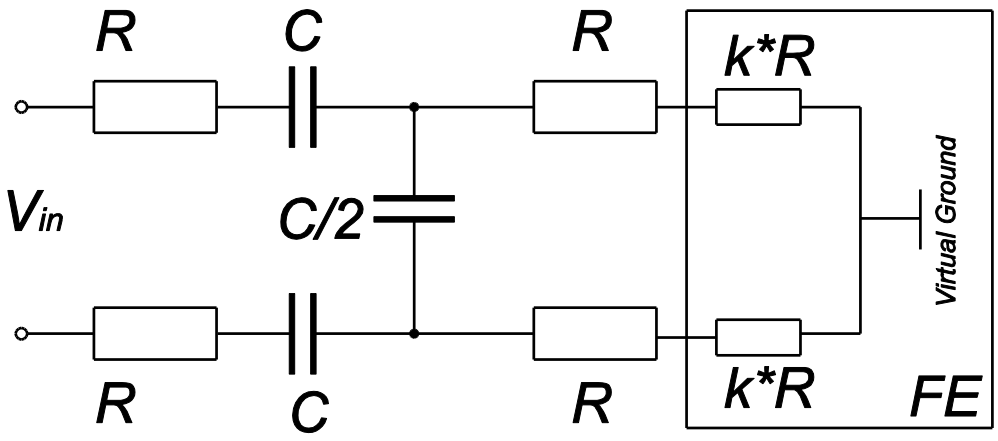

Figure 4.11 Interface between the WB and the readout FE

The transfer function of the WB loaded by the FE is given in Equation 4.19, and its phase shift is given in Equation 4.20.

$$H(\omega) = \frac{j\omega \cdot (1+k)R \cdot C}{[1 - (1+k)\omega^2 R^2 C^2] + j(2 + \frac{1}{1+k})\omega \cdot (1+k)R \cdot C} \tag{4.19}$$

$$\varphi_{WB} = -arctan\frac{(1+k) \cdot \omega^2 R^2 C^2 - 1}{(3+2k) \cdot \omega RC} \tag{4.20}$$

In order to avoid readout FE adding spread to the WB temperature dependency, there are two solutions. One solution is to minimize the FE input impedance, *i.e.* $k << 1$, and then the temperature dependency of the sensed-current is totally determined by the WB. In this case, the FE creates a virtual ground so that the TC of the incoming current is completely determined by the WB, which is the best condition for accurate chopping. However, to implement $k << 1$, extra power consumption is required. The other solution is to ensure that the FE input impedance has the same TC as the resistors in the WB, and the equivalent input impedance of the FE can be the same order as the resistors in the WB, *i.e.* $k \sim 1$.

Considering minimizing power consumption is one of the major goals in this project, the second solution is used. To ensure the input impedance of the FE has the same TC as the resistors in the WB, the bias current of the OTA should be derived from a replica of the same type of the resistors used in the WB, which is discussed in Section 4.2.9.

Once the OTA biasing has the same temperature dependency as the resistors in the bridge, the FE input impedance can be regarded as part of the WB. To degenerate the transfer function of the WB loaded by the FE, as shown in Equation 4.19, back to its ideal transfer function, as given in Equation 3.2, reduce the resistance of the two resistors located at the output side of the WB such that the sum of them and the FE equivalent impedance remains as 32 kΩ.

Since the equivalent input impedance of the FE is a function of frequency, phase offset is introduced when the FE loads the WB, which is temperature-dependant, as shown in Figure 4.12.

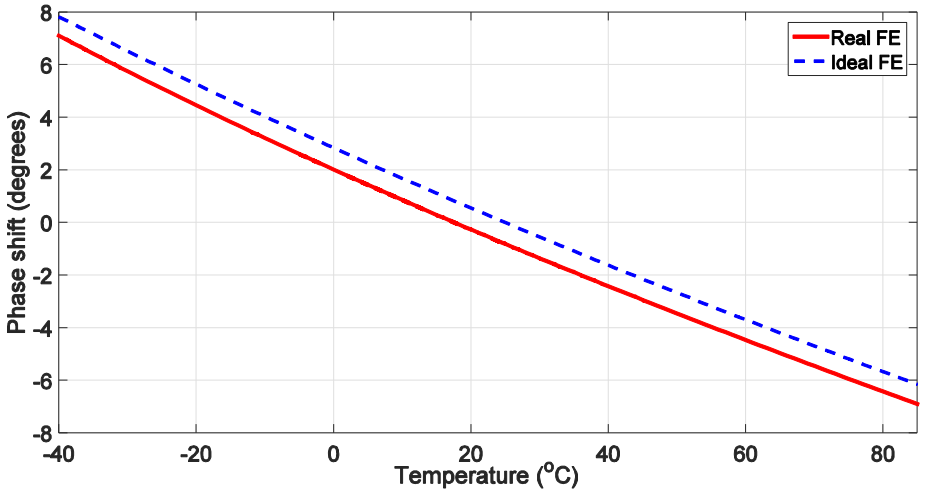

Figure 4.12 WB phase shift over temperature with and without FE loading

The phase offset caused by the FE loading effect will be absorbed by a 3-point calibration. The residual errors after applying a 1st order and a 2nd order polynomial fitting are given in Figure 4.13 and Figure 4.14, respectively. After a 1st order polynomial fitting, the FE loading leads to 1 ℃ more temperature-sensing inaccuracy compared with the ideal case. However, when a 2nd order polynomial fitting is applied, the phase offset caused by the FE input impedance is absorbed. Therefore, in order to prevent the FE input impedance from degrading the temperature-sensing accuracy, a calibration with at least three points is demanded.

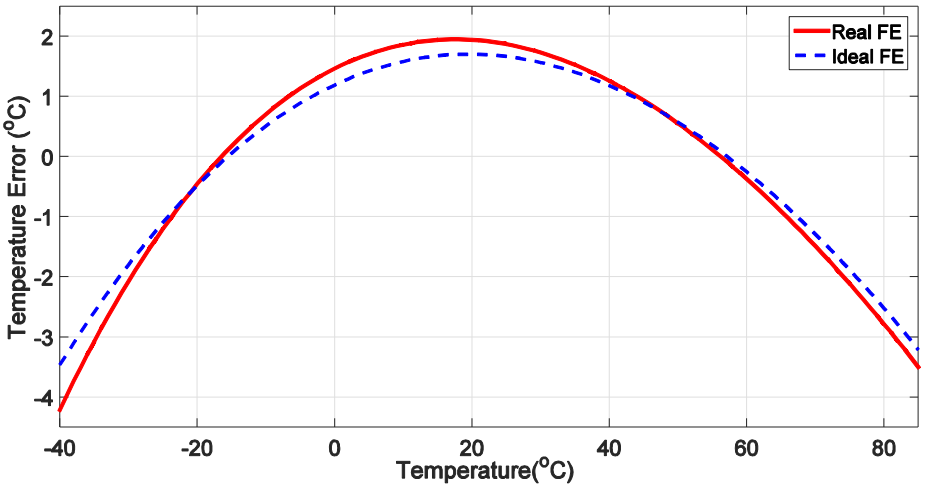

Figure 4.13 Residual error after a 1st order polynomial fitting of the sensor with/without FE loading

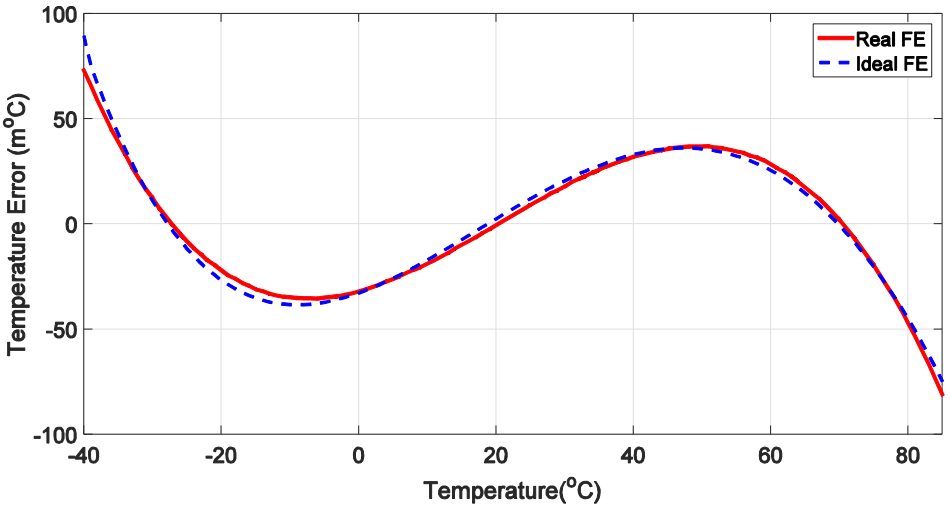

Figure 4.14 Residual error after a 2nd order polynomial fitting of the sensor with/without FE loading

4.2.2.3.4 Transistor-Level Design

As discussed in Section 4.2.2.3.1, the telescopic structure is chosen to implement the OTA in the first integrator of the DSM. Its transistor-level implementation with biasing is shown in Figure 4.15.

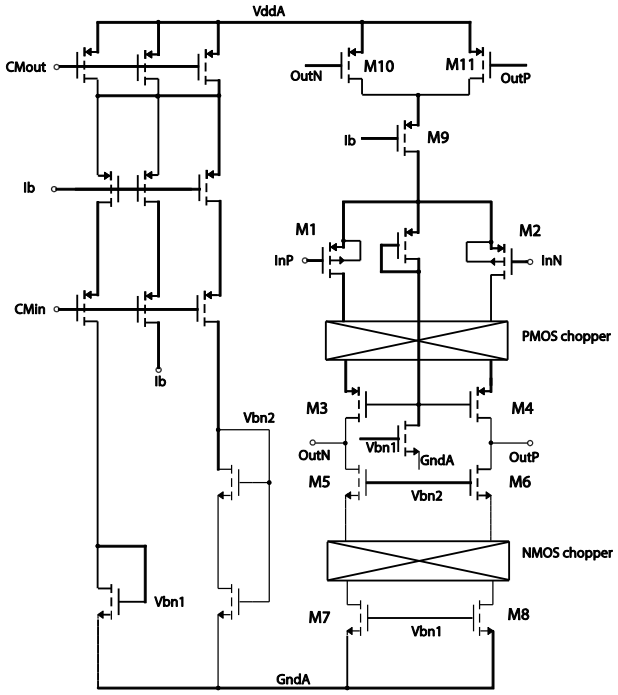

Figure 4.15 Telescopic OTA structure (with biasing)

Choose PMOSFETs as the input pair, because a PMOSFET generates less flicker noise compared with its counterpart, NMOSFET. Besides, it is easier to connect the source and the bulk together for a PMOSFET since the substrate is lightly p-doped. To implement a supply-independent biasing circuit with well-defined temperature dependency as presented in Section 4.2.9, it is necessary to connect the sources and the bulks of the input pair together.

Since the input current of the active-RC filter is chopped before being integrated, to remain the feedback negative, synchronized chopping is demanded in the signal path of the OTA, which is located in the PMOSFET side. The additional function of chopping operation is to modulate the flicker noise and offset to chopping frequency, which is out of the signal band. To modulate the flicker noise and offset of the two NMOSFETs at the bottom out of the signal band, another chopper is placed at the NMOSFET side. Both the choppers are controlled by the same clock as the one used to demodulate the WB output current.

The common-mode feedback (CMFB) in the telescopic OTA is implemented by M_9 ~ M_{11}. The output common-mode (CM) voltage is sensed by the identical transistors M_{10} and M_{11}. Both of them operate in deep triode region, introducing a resistance R between the supply rail and the source of M_9, which is given by Equation 4.21.

$$R = R_{on,10} \,||\, R_{on,11} = \frac{1}{\mu_p C_{ox} \frac{W}{L} \left(V_{outN} + V_{outP} - 2V_{TH,10,11}\right)} \tag{4.21}$$

R is a function of the output CM voltage and independent of the output differential voltage. The output CM level sets R such that I_{D1} and I_{D2} exactly balance I_{D7} and $I_{D8,}$ respectively [43].

Since the output CM voltage is directly converted to resistance, instead of comparing with a reference voltage, a reference voltage is set by the gate voltage of M_9. The output CM level set by this CMFB can be expressed as Equation 4.22.

$$V_{CM,output} = \frac{I_D}{\mu_p C_{ox} \left(\frac{W}{L}\right)_{10,11} (V_{dd} + V_{GS9} - V_{Ib})} + V_{TH} \tag{4.22}$$

Equation 4.22 indicates that the value of the output CM level set by this CMFB network is a function of the device parameters, and it is sensitive to the mismatch between M_{10} and $M_{11.}$ Hence relatively large dimensions are chosen for M_{10} and $M_{11.}$

Cadence simulation shows that the OTA has a DC gain of 87 dB, and a unity-gain frequency of 20MHz. Although there are two poles in this OTA, the 2nd pole is benign because it is located at the frequency higher than the unity-gain frequency.

The calculated input-referred voltage noise of the OTA is $12.45\ nV/\sqrt{Hz}$, and the simulated value is $12.3\ nV/\sqrt{Hz}$. Both values are lower than the thermal noise of the WB, which is $18.5\ nV/\sqrt{Hz}$.

4.2.3 Second Integrator Design

For the second stage in the phase-domain delta-sigma ADC, noise and linearity is not as important as the first stage. To reduce the power consumption, a Gm-C integrator is chosen as the second stage in

the readout.

The OTA in the second stage is also implemented by a telescopic structure, due to its power efficiency and high speed. Since the output common mode (CM) level of the first stage is 750 mV, which is also the input CM level of the second stage, a NMOS pair is chosen as the differential input. CMFB in the second stage is implemented by the same structure used in the first stage.

The noise in the second stage is less significant compared with the first stage, because it will be suppressed by the gain of the first stage. Thus allocate one twelfths of current consumed by the first stage to the second stage.

The linear input range of a Gm-C integrator is small. However, over the process corners and the industry temperature range (from -40 ℃ to 85 ℃), the maximum output amplitude of the first stage is approximately 150 mV, which is too large to be linearly handled by a Gm-C integrator. So in the transconductor of the second integrator, degeneration technique is employed. It is implemented by the source degeneration resistors of the input transistors.

The telescopic OTA used in the second stage is shown in Figure 4.16.

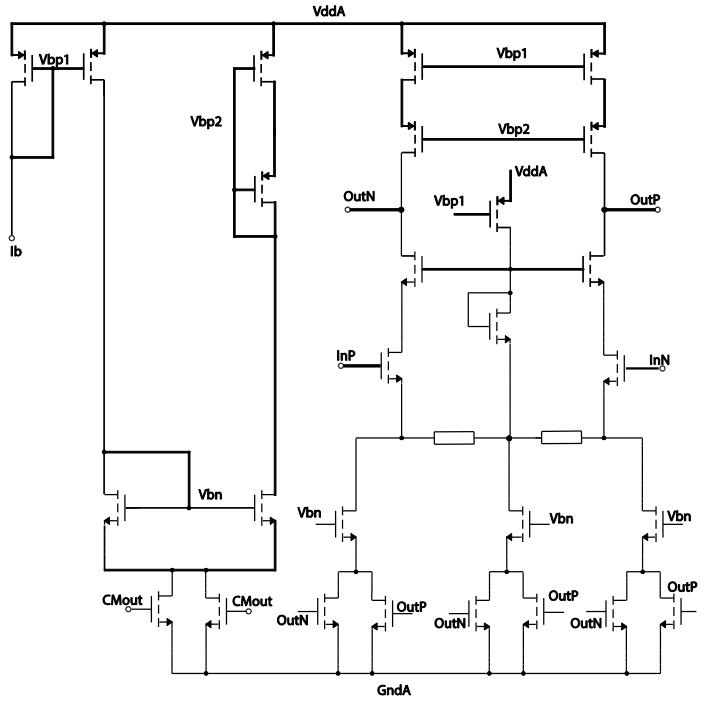

Figure 4.16 OTA structure used in the second integrator (with biasing)

The source degeneration greatly increases the linear input range. The transconductance of the OTA with and without source degeneration is shown in Figure 4.17. With the source degeneration, the linear input voltage can be as large as ±300 mV, which is sufficiently large to liearly handle the output of the first integrator over the temperature and the process corners.

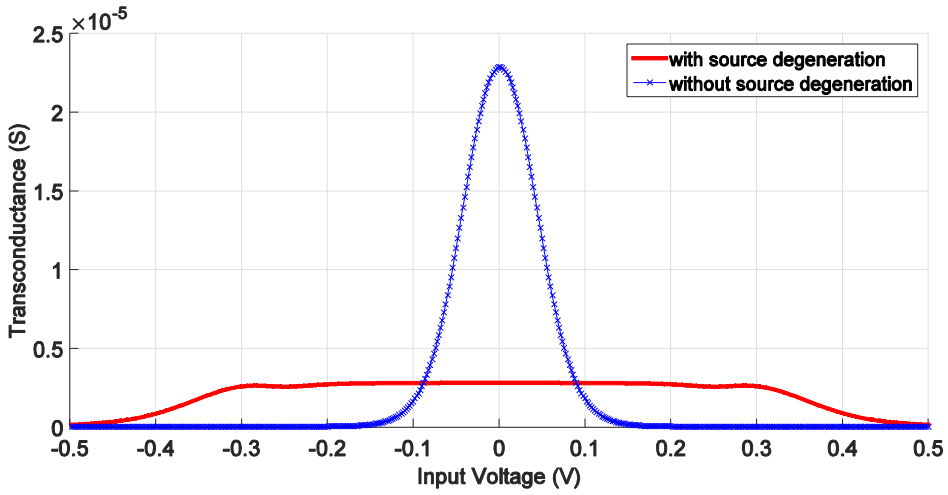

Figure 4.17 Transcondutance with and without source degeneration

The power and linearity trade-off manifests itself when degeneration technique is employed. With this technique, wider linear input range can be achieved at the cost of more power consumption. Now the equvalent transconductance of the OTA is determined by the reciprocal of the source degenration resistance, which is much smaller than the intrinsic transocnductance of the input transistors. With the same power consumption, the intrinsic transconductance of a NMOSFET can be 10 times larger than the one achived by the source degeneration, however, only in a narrow input range.

Cadence simulation shows that the OTA in the second integrator has a DC gain of 78 dB, and a unity-gain frequency of 0.6 MHz.

The transfer function of the 2nd integrator is given in Equation 4.23, where C is the value of the integrating capacitor, and g_m is the equvalent transocndutance of the OTA.

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{g_m}{sC} = \frac{\omega_u}{s} = \frac{3.5 \times 10^5}{s} \qquad (4.23)$$

According to Equation 4.23, the unity-gain frequency of the integrator is set by the transconductance. There is no parasitic poles due to the load capacitance, so the type of integrator is fast. In this design, the unity-gain frequency of the $g_m - C$ integrator is 2.2 MHz.

4.2.4 Feedforward Implementation

To remain a 2nd order DSM stable, compensation structure is demanded. As explained in Section 4.1.1, feedforwad strcucture is chosen in this design.

The feedforward is implemented by feeding the output of the first integrator to the input of the comparator, as shown in Figure 4.18.

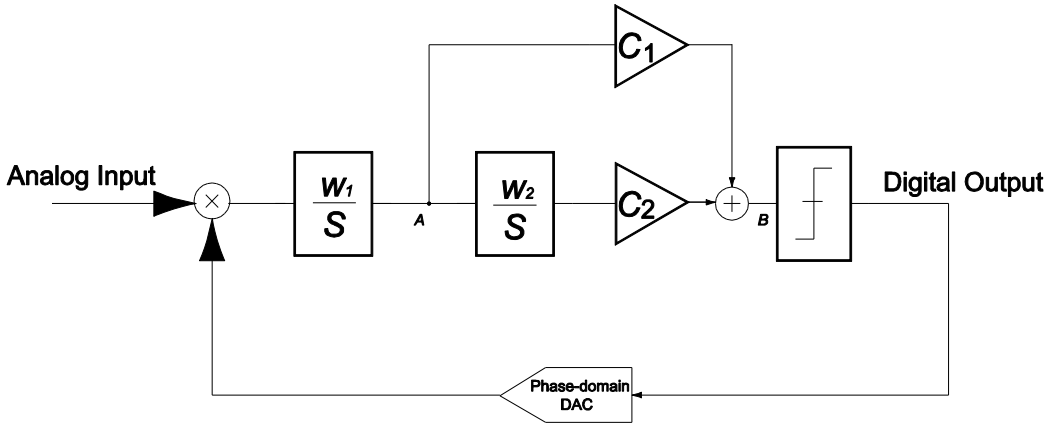

Figure 4.18 Feedforward implementation in the readout

The transfer function from A to B in Figure 4.18 is given in Equation 4.24.

$$H(s)_{A\to B} = \frac{V_B}{V_A} = c_1 + c_2 \cdot \frac{\omega_2}{s} \qquad (4.24)$$

To optimize the NTF of the DSM, choose $c_1 = \frac{2 \cdot \omega_2}{f_s}$ and $c_2 = 1$ [37]. Substituting the value of c_1 and c_2 as well as Equation 4.23 into Equation 4.24, Equation 4.25 can be acquired.

$$H(s)_{A\to B} = \frac{V_B}{V_A} = g_m \left(\frac{2}{C \cdot f_s} + \frac{1}{sC}\right) \qquad (4.25)$$

To implement the transfer function given in Equation 4.25, another structure instead of the one shown in Figure 4.18 can be used, as shown in Figure 4.19. Its transfer function can be expressed as Equation 4.26.

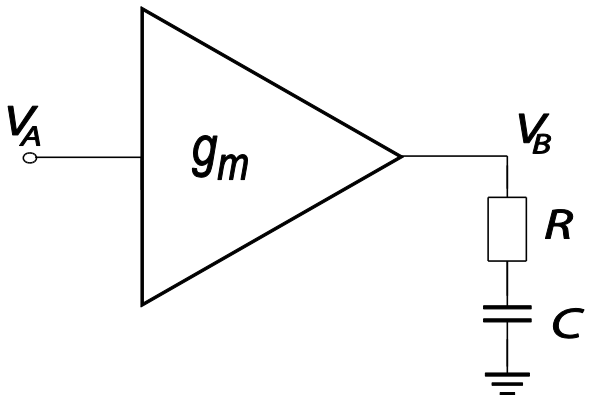

Figure 4.19 Another implementation of Equation 4.25

$$H(s)_{A\to B} = \frac{V_B}{V_A} = g_m \left(R + \frac{1}{sC}\right) \qquad (4.26)$$

In this design, the feedforward is implemented by the structure given in Figure 4.19 instead of the one in Figure 4.18. Because if the conventional feedforward structure shown in Figure 4.18 is employed, a transconductor is required to implement the feedforward coefficient c_1, which would consume extra power; however, energy-efficiency is one of the major goals in this design, so the feedforward is simply implemented by a resistor which is in series with the integrating capacitor in the $G_m - C$ integrator, as shown in Figure 4.19.

The resistor value R can be calculated by combining Equation 4.25 and Equation 4.26,

$$R = \frac{2}{C \cdot f_s} \tag{4.27}$$

As elaborated in previous sections, in single-ended equivalent circuit, C = 16 pF and f_s = 500 kHz, hence R = 250 kΩ.

4.2.5 Comparator Design

The comparator in the readout is implemented by a two-stage pre-amplifier followed by a dynamic latch [39], as shown in Figure 4.20.

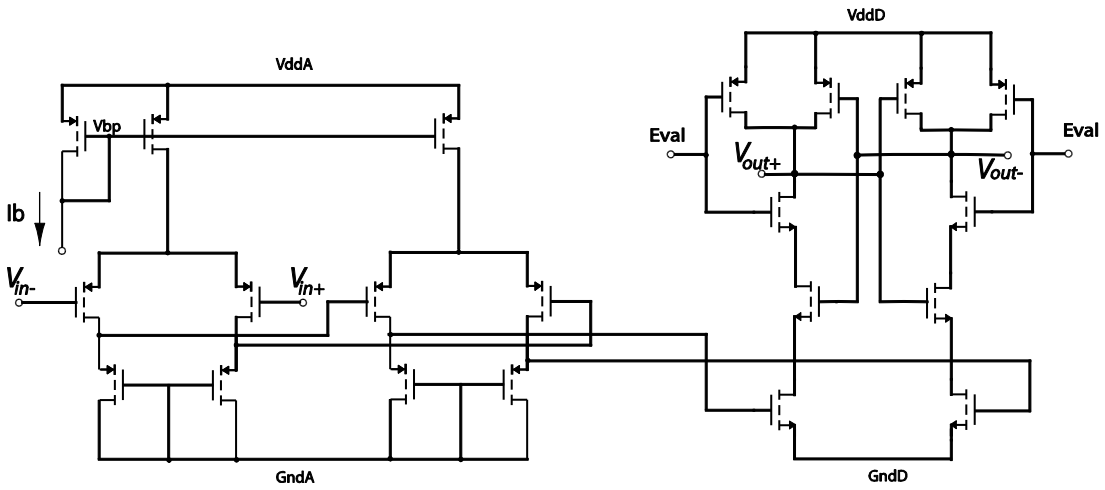

Figure 4.20 Comparator implementation

There are two main functions to employ the pre-amplifier. First, a pre-amplifier can speed up the following latch forming a digital signal. One crucial observation is that the time a latch needs to form a digital decision depends on the initial overdrive voltage [40]. Large input helps reduce the time that the latch needs to make a decision. Second, a pre-amplifier can reduce the charge kick-back. During the decision process in the latch, the relevant transistors go through all of the operation modes of the devices. At the same time, the charges containing in these devices experience a considerable variation, which have to be provided and dumped preferably by the power supply rails. However, parts of these charges are kicked back to the latch input via parasitic capacitance. A pre-amplifier can suppress the charge kick-back effect on the input of the comparator.

The drawback of a pre-amplifier is that it will create an extra delay. In the design, each stage of the pre-amplifier consists of a pair of PMOS input transistors and a pair of diode-connected PMOS loads. Each differential pair consumes 200 nA while provide a DC gain of 3.3 and a unity-gain bandwidth of 10.7 MHz. The delay caused by the pre-amplification stage is less than 5% of the sampling period, which is acceptable given the loop stability.

The sample-and-hold process is fulfilled by the dynamic latch. The latch contains a positive feedback loop. When the control signal *Eval* goes from low to high, the positive feedback starts functioning, and the latch output increases exponentially with respect to time, which makes such latch a fast decision element. The rising edge of *Eval* samples the analog signal and the positive feedback loop regenerates the signal into its digital representation. The positive feedback loop is actually formed by two inverters. The output of one inverter is connected to the input of the other inverter. During *Eval* is high, the decision made by the regenerative process is being stored by the positive feedback loop. When *Eval* goes from high to low, the positive feedback loop is broken, and the latch output is reset by connected to supply rails via PMOS switches thus all state information is being removed actively. Ideally, the two latch outputs should share the same DC level at the reset mode; however, inequality always exists due to the process variation even though they are designed to have the identical following stages, resulting in inaccuracy.

It is should be noted that at the moment that *Eval* goes from low to high, the regeneration starts, but the digital decision isn't made immediately. Regeneration requires certain amount of time. Therefore, each output terminal of the comparator is followed by a D-flip flop (DFF), clocked by the rising edge of *phi_latch*. With respect to *Eval*, *phi_latch* has certain delay. The DFFs capture digital decision made by comparator when it is totally ready. They also help buffer the output of the comparator and send it to DAQ. Meanwhile, the falling edge of *phi_latch* is used as the trigger signal to capture the DSM output bit-stream.

Inaccuracy issue exists in every analog circuit, and is one of the significant considerations during the comparator design. The inaccuracy sources could be the random mismatch of a transistor pair, the mismatch of the load, thermal noise, flicker noise and/or the asymmetry of the layout. All of the contributions can be referred back to an equivalent input-referred random mismatch. To evaluate the input-referred random mismatch of the comparator in this design, the dynamic input range of the comparator is determined by performing Monte Carlo analysis from -40 ℃ to 85 ℃ over the process corners. The simulation indicates that the comparator can make a right decision as long as the input differential voltage is larger than 2 mV. If the input is smaller than 2 mV, wrong decisions occur occasionally. However, since the comparator is inserted in a DSM loop, even if wrong decision is being made, the loop can self-rectified after several cycles.

4.2.6 Feedback DAC

A feedback DAC in the phase domain outputs a phase reference determined by its input digital signal. In this design, one-bit quantizer is employed, hence there are two state of the input of the feedback DAC, either 0 or 1. According to the quantizer output, either phase reference φ_{r1} or φ_{r2} is chosen to

control the chopper which demodulates the temperature information stored in the WB output from phase domain to DC current.

A multiplexer is used to choose one phase reference out of two. It is implemented by the two-stage NAND gates, as shown in Figure 4.21.

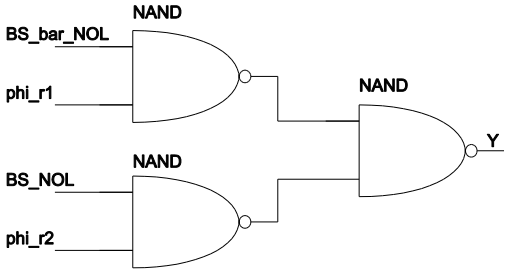

Figure 4.21 Multiplexer used in the phase-domain feedback DAC

The logic between the output and the input of the multiplexer can be described by Equation 4.28, where BS is the output of the quantizer, and φ_{r1} and φ_{r2} are two phase references. When BS is 0, φ_{r1} is chosen; when BS is 1, φ_{r2} is chosen.

$$Y = \overline{BS} \cdot \varphi_{r1} + BS \cdot \varphi_{r2} \qquad (4.28)$$

It is important to make sure that only one of these two phase references is being chosen, thus a circuit to ensure the multiplexer control signal always non-overlapping is employed preceding the multiplexer. The circuit is shown in Figure 4.22 [41]. The non-overlap period is determined by the sum of propagation delay of one NOR gate and two inverters.

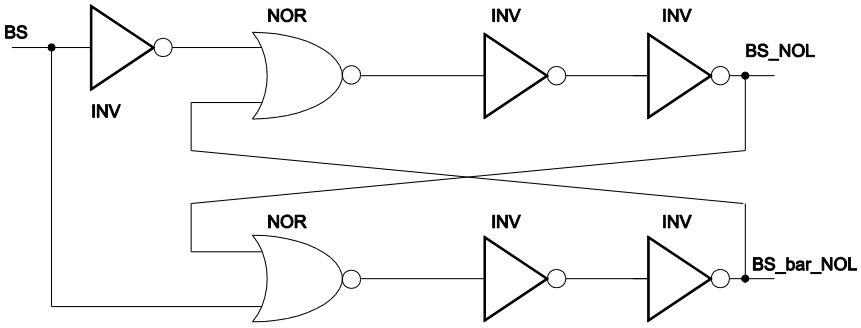

Figure 4.22 Non-overlapping clock generator [41]

Since the chopper which is used to demodulate the WB output is implemented in the T-gate form, both the phase reference and its inverse version are required.

The block diagram of the feedback DAC is given in Figure 4.23.

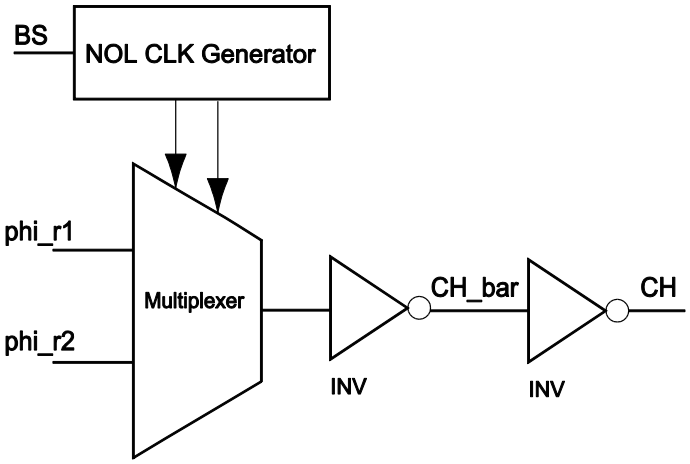

Figure 4.23 Block diagram of the feedback DAC

4.2.7 System-Level Chopping

The signal bandwidth is 100 Hz. In this frequency range, offset and flicker noise will manifest themselves. In order to prevent non-ideal components from degrading the readout resolution, system-level chopping is employed in the readout.

The system-level chopping is implemented by switching the WB driving signal polarity and the quantizer output at the same time, as shown in Figure 4.24. *CHL* is the system-level chopping signal, which is larger than the signal bandwidth, while much smaller than the sampling frequency of the DSM. XOR gates are employed to perform the system-level chopping.

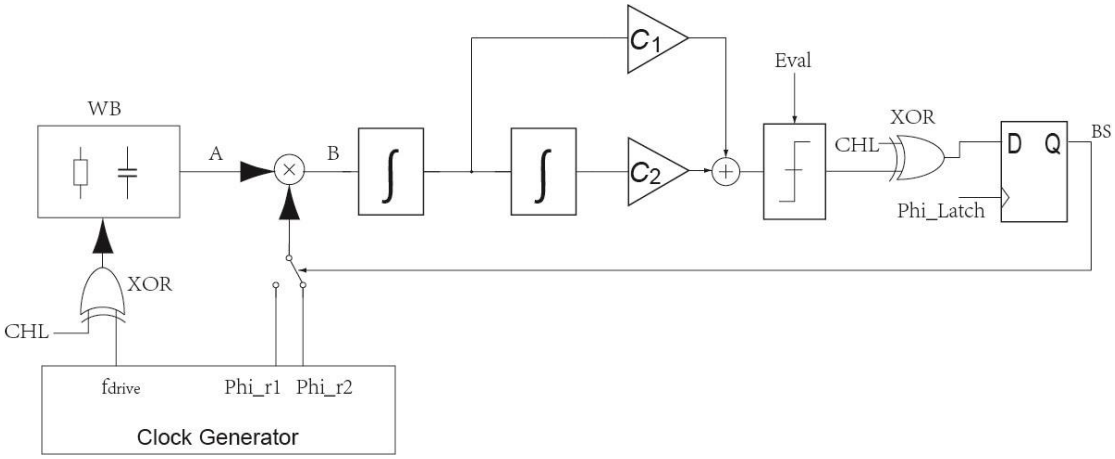

Figure 4.24 System-level chopping implementation

Based on Equation 4.2, the charge will be integrated by the loop filters can be expressed as Equation 4.29.

$$q_{T_s}{}' = CHL \cdot C \cdot \cos(\varphi_0 + \varphi_{WB} - \varphi_{ri}) \quad (4.29)$$

To keep the loop stable, another polarity switching operation is required in the loop. To avoid adding extra delay in the loop due to the system-level chopping, the second polarity switching operation is located at the output of the comparator, before the latch, which is used to buffer the comparator output.

The phase difference between *Eval* and *phi_Latch* is set to be larger than one XOR gate propagation delay.

4.2.8 Clock Generation Circuit

As elaborated in Chapter 3, the center frequency of WB at room temperature is chosen as its driving frequency, which is 500 kHz. In order to utilize the most linear range of cosine function, the two references in the phase-domain DAC are desired to have a phase shift close to 90 ° with respect to WB driving frequency. One of them should have a phase shift slightly smaller than 90 ° and the other should have a phase shift slightly larger than 90 °. Assuming that no mismatch appears, *i.e.* the driving frequency equals to the WB center frequency, at the typical process corner the phase shift of the WB over the industrial temperature is 14 °. Considering the process variation and overloading effect in a DSM, the full-scale of the DSM have to be larger than 14 °. Given the way the phase shift being creating, which will be discussed in Section 4.2.9.2, 67.5 ° and 112.5 ° are chosen as the two phase references in the DAC. Since a phase shift step of 22.5 ° is required, 8 MHz is chosen as the master clock frequency. In case of severe process variation occurs, four square waves with phase shifts of 45 °, 67.5 °, 90 ° and 112.5 ° respectively are available to work as φ_{r1} and another four square waves with phase shifts of 67.5 °, 90 °, 112.5 ° and 135 ° respectively are available to work as φ_{r2}. The selection is done by the control signal from a shift-register.

4.2.8.1 Frequency Division

The 8-MHz master clock needs to be divided by 16 to obtain the desired WB driving frequency. The clock frequency division is implemented by the circuit given in Figure 4.25

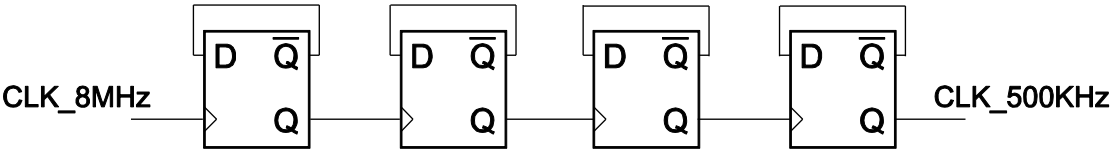

Figure 4.25 clock frequency dividing implementation

4.2.8.2 Phase Shifting

As discussed before, square waves with phase shifts of 45 °, 67.5 °, 90 °, 112.5 ° and 135 ° with respect to the WB driving square wave are required. To obtain these phase shifts, the circuit in Figure 4.26 is employed. Instead of using 8 MHz master clock as the clocks of the D-FFs, 4 MHz and its inverse version are used to implement a phase shift step of 22.5 °. Because the 8 MHz master clock is used to synchronize the WB driving signal and the two phase references, as discussed in next section, its load should be minimized in order to preserve its ultra-low jitter performance.

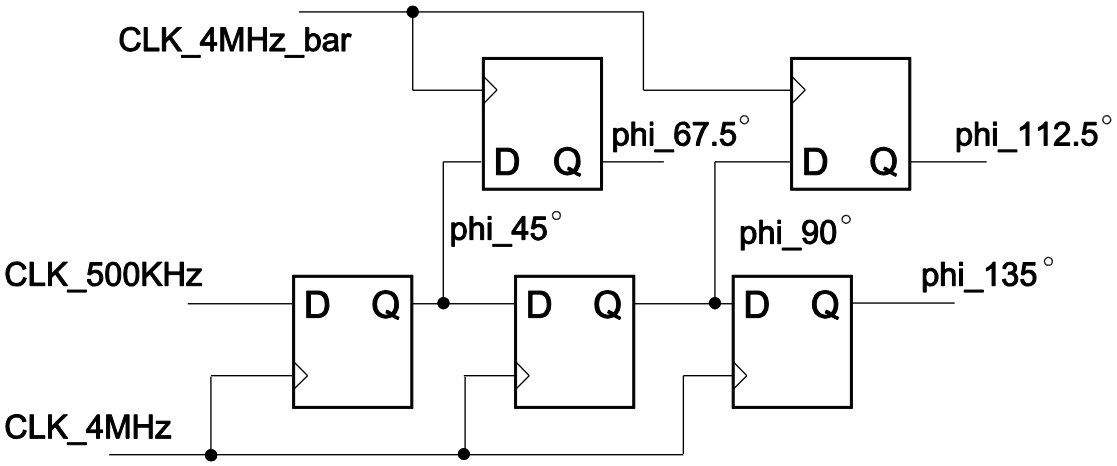

Figure 4.26 Phase Shift Implementation

4.2.8.3 Jitter Consideration

To prevent the phase error from degrading the WB inherent temperature-sensing resolution, a requirement for ultra-low jitter is imposed on the WB driving square wave and the two phase references, as discussed in Section 3.3. Although the 8-MHz master clock frequency has ultra-low jitter performance initially, after being divided and phase-shifted, its jitter performance degrades exponentially [42]. To handle this problem, these jitter-sensitive signals are synchronized by the 8 MHz superior master clock [42]. In this way, the jitter which could cause phase error before demodulating is limited by the 8-MHz master clock jitter performance, which will not degrade the WB inherent temperature-sensing resolution, as calculated in Section 3.3.

4.2.8.4 Timing

The timing diagram of the clock generating block is shown in Figure 4.27. The WB driving signal $f_{driving}$, two phase references φ_{r1} and φ_{r2}, comparator regeneration control signal *Eval*, comparator output capturing signal *phi_Latch* are 500 kHz, and CHL is for system-level chopping control, of which the frequency is larger than the signal bandwidth while much lower than 500 kHz. To indicate the timing relation, in Figure 4.27 CHL period is scaled. φ_{r1} has a phase shift of 67.5 °with respect to $f_{driving}$, and φ_{r2} has a phase shift of 112.5 °with respect to $f_{driving}$. *Eval* has a 11.25 °phase lag with respect to φ_{r2}. Phi_Latch always has a phase lag of larger than 22.5 °with respect to *Eval* either CHL = 0 or CHL = 1. CHL is designed that $f_{driving}$ is switching at the middle of its half-period. In this way, the relative timing relation between $f_{driving}/\overline{f_{driving}}$ and φ_{r1}, φ_{r2}, *Eval*, *phi_Latch* can be maintained at both phases of CHL.

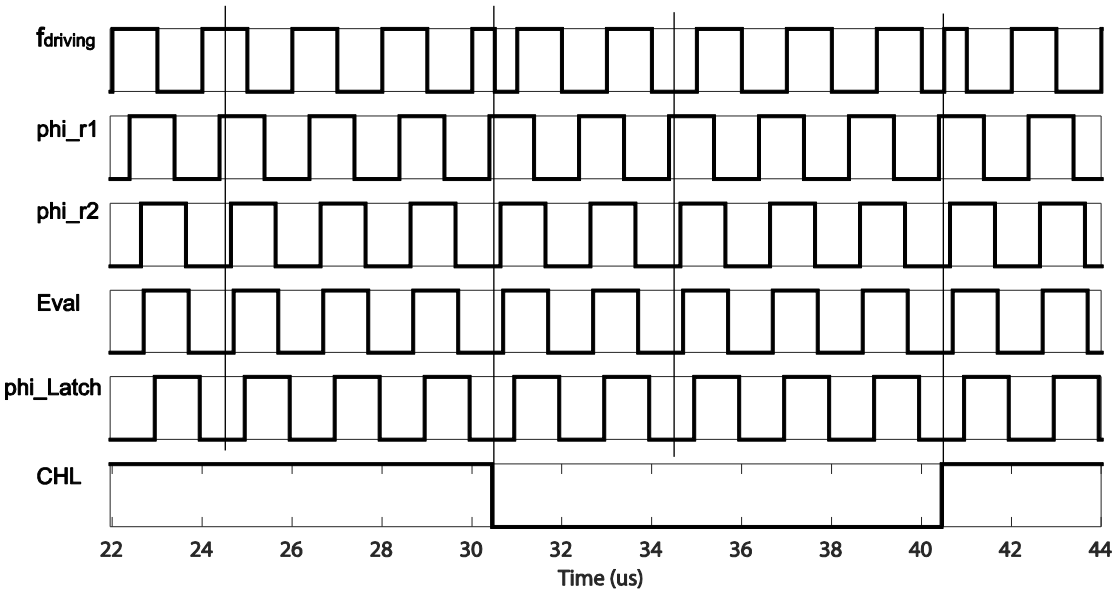

Figure 4.27 timing diagram of the clock generating block

4.2.9 Biasing Circuit

4.2.9.1 Basic Principle

The objective of a biasing circuit is to establish a DC current reference, which is independent of supply and process, and has a well-defined temperature dependency. In this design, as discussed in Section 4.2.2, the biasing current should have the same temperature dependency as that of the silicided resistors used in the WB to avoid the readout FE adding temperature spread to the WB. The basic structure of the biasing circuit to meet these requirements is given in Figure 4.28. R is used to define the current, and it is the same type as the resistors in the WB. Hence the biasing current has the same temperature dependency as that of the WB, so does the readout FE impedance. The source and the bulk of M_3 are connected together in order to eliminate the body effect and ensure the threshold voltage of M_3 and M_4 equal.

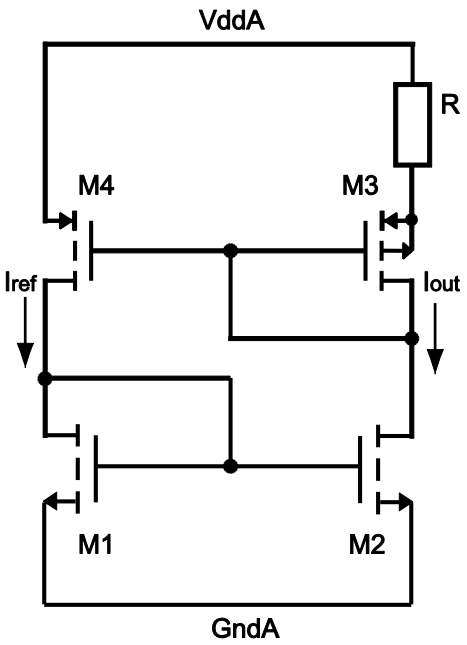

Figure 4.28 supply-independent biasing with well-defined TC

According to Kirchhoff's Voltage Law,

$$-V_{GS4} = -V_{GS3} + I_{out}R \tag{4.30}$$

All the MOSFETs should operate in the saturation region; the $I_D - V_{GS}$ relation for a MOSFET operating in the saturation region can be expressed as Equation 4.31, where the drain current I_D is defined to flow from the drain to the source. In Equation 4.31, channel-length modulation is neglected.

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{4.31}$$

Assuming that M_1 and M_2 have identical dimensions, Equation 4.32 can be obtained.

$$I_{out} = I_{ref} \tag{4.32}$$

Combining Equation 4.30, 4.31, and 4.32, while defining $\left(\frac{W}{L}\right)_3 = K \cdot \left(\frac{W}{L}\right)_4$, Equation 4.33 can be derived.

$$\sqrt{\frac{2I_{out}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_4}}\left(1 - \frac{1}{\sqrt{K}}\right) = I_{out}R \tag{4.33}$$

There are two solutions for Equation 4.33,

$$I_{out,1} = 0 \tag{4.34}$$

$$I_{out,2} = \frac{1}{R^2} \cdot \frac{2}{\mu_P C_{ox} \left(\frac{W}{L}\right)_4} \cdot \left(1 - \frac{1}{\sqrt{K}}\right)^2 \tag{4.35}$$

$I_{out,1}$ indicates that this biasing circuit may settle in the state where both of the braches support zero current, which should be eliminated, as discussed in Section 4.2.8.2.

$I_{out,2}$ indicates that the biasing current is independent of the supply voltage if ignoring the channel-length modulation. And its temperature dependency is precisely defined by R. However, it still suffers from the process variation.

To minimize the process variation suffered by the biasing current, M_4 in Figure 4.28 should be the same type of MOSFET as the input pair of the OTA in the first integrator, *i.e.* PMOSFET with the same length and scaled width. Therefore, the transconductance of the input pairs in the OTA of the first integrator can be expressed as Equation 4.36, where H is the dimension ratio between the input transistor of the OTA in the first integrator and M_4 in the biasing circuit.

$$g_{m,in} = \frac{2}{R} \sqrt{H} \left(1 - \frac{1}{\sqrt{K}}\right) \tag{4.36}$$

Hence the readout FE equivalent input impedance can be expressed as Equation 4.37, which will load the WB.

$$R_{FE} = \frac{1}{g_{m,in}} = \frac{R}{2} \cdot \frac{1}{\sqrt{H}\left(1 - \frac{1}{\sqrt{K}}\right)} \tag{4.37}$$

Equation 4.37 indicates that the readout FE input impedance which loads the WB is independent of the process variation. Although mismatch still plays a significant role, it can be minimized by careful layout. The most important information given by Equation 4.37 is that R_{FE} has the same temperature dependency as that of the resistors in the WB, hence the readout FE will not add temperature spread to the WB theoretically, and no effort is needed to reduce the FE input impedance to a ultra-low level, leading to an energy-efficient interface.

4.2.9.2 Supply-Dependency Improvement

The analysis in previous section exhibits that the biasing circuit given in Figure 4.28 is supply independent if the channel-length modulation is negligible. Hence long-channel devices are used in the biasing circuit. However, the channel-length modulation only can be reduced instead of entirely eliminated. To estimate the change in I_{out} for a small change in the supply voltage V_{dd}, the biasing circuit given in Figure 4.28 is simplified as Figure 4.29.

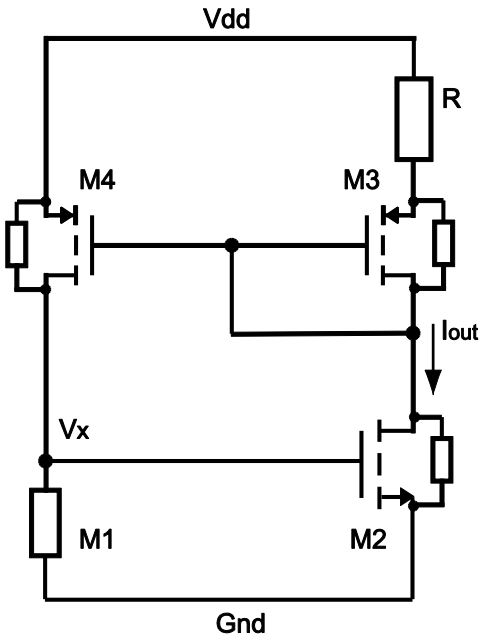

Figure 4.29 Equivalent circuit of the one in Figure 4.28 to analysis its supply dependency

Applying Kirchhoff's Current Law at Node Vx, Equation 4.38 can be obtained.

$$\frac{V_X}{R_1} = \frac{V_{dd} - V_X}{r_{o4}} + g_{m4} I_{out} R_3 \qquad (4.38)$$

r_{oi} is the source-drain resistance of M_i, and g_{mi} is the inherent transconductance of M_i. R_1 and R_3 can be expressed as Equation 4.39 and 4.40.

$$R_1 = \frac{1}{g_{m1}} \,||\, r_{o1} \qquad (4.39)$$

$$R_3 = \frac{r_{o3} + R}{g_{m3} r_{o3} + 1} \qquad (4.40)$$

Denoting the equivalent transconductance of M_2 by G_{m2}, Equation 4.41 can be obtained.

$$I_{out} = V_X G_{m2} \qquad (4.41)$$

Combining Equation 4.38 and Equation 4.41, $I_{out} - V_{dd}$ relation can be obtained as shown in Equation 4.42.

$$I_{out} = V_{dd} \cdot \frac{1}{r_{o4}} \cdot \left[\frac{1}{g_{m2}\left(r_{o4} \,||\, \frac{1}{g_{m1}} \,||\, r_{o1}\right)} - g_{m4} \cdot \frac{r_{o3} + R}{g_{m3} r_{o3} + 1} \right]^{-1} \qquad (4.42)$$

To further reduce the supply voltage dependency of I_{out}, a gain stage with a gain of A can be inserted

between the drain and the gate of M_1, as is shown in Figure 4.30. In this way, the supply voltage dependency of I_{out} can be further reduced by the order of A, as indicated by Equation 4.43.

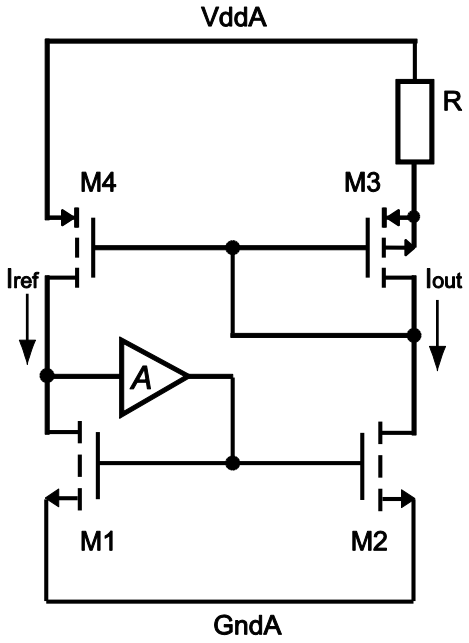

Figure 4.30 Biasing with improved supply-independency

$$I_{out} = V_{dd} \cdot \frac{1}{r_{o4}} \cdot \left[\frac{1}{g_{m2}\left(r_{o4} \,||\, \frac{1}{A \cdot g_{m1}} \,||\, r_{o1}\right)} - g_{m4} \cdot \frac{r_{o3} + R}{g_{m3} r_{o3} + 1} \right]^{-1} \qquad (4.43)$$

A common-source PMOS transistor is used to implement the gain-stage.

Indicated by Equation 4.43, it will help further reduce the supply dependency of I_{out} if the channel-length modulation effect of each transistor can be reduced. Therefore, on the PMOS-side, another cascode PMOSFET is introduced in each branch; while on the NMOS-side, NMOSFETs with long channel length are employed instead of using cascode technique. Because the biasing current is transported to external blocks by NMOS current mirrors, the NMOS-side should preserve sufficient voltage headroom to interface external blocks. The biasing circuit used in this design is shown in Figure 4.31.

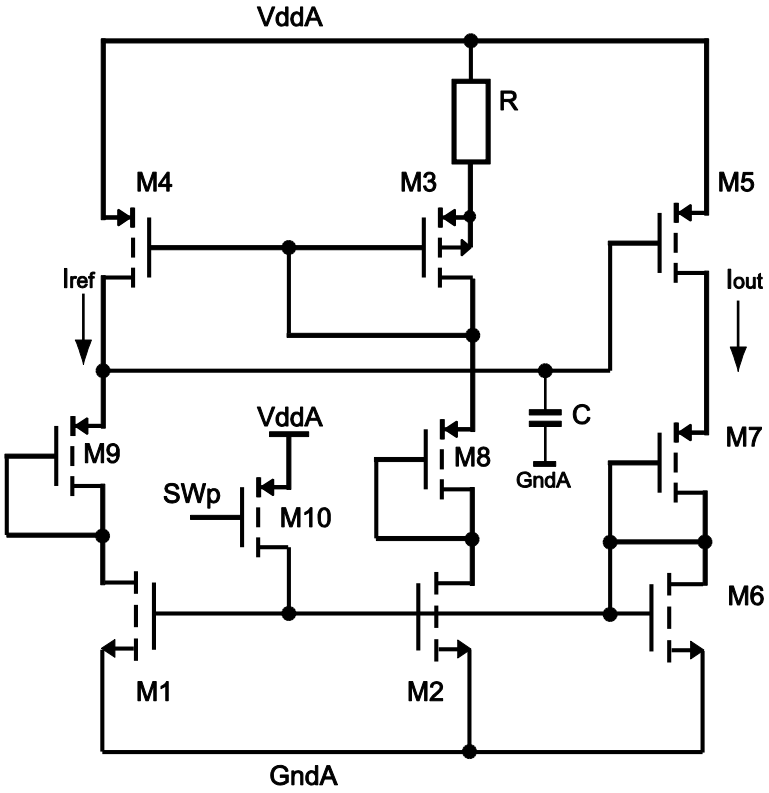

Figure 4.31 Biasing implementation

With the amplification stage inserted in the biasing circuit, the voltage dependency of the transconductance of the first OTA is further compressed compared with the structure shown in Figure 4.28. Cadence simulations have been done for both of these structures, and the simulation result is shown in Figure 4.32. The fluctuation is calculated with the value at 1.8 V as the reference. When ±0.2 V supply variation occurs with respect to the nominal value 1.8 V, the transconductance fluctuation of the OTA in the first integrator biased by the structure with the amplification stage is only 15.4% of the transconductance fluctuation of the OTA in the first integrator biased by the structure without any amplification stage.

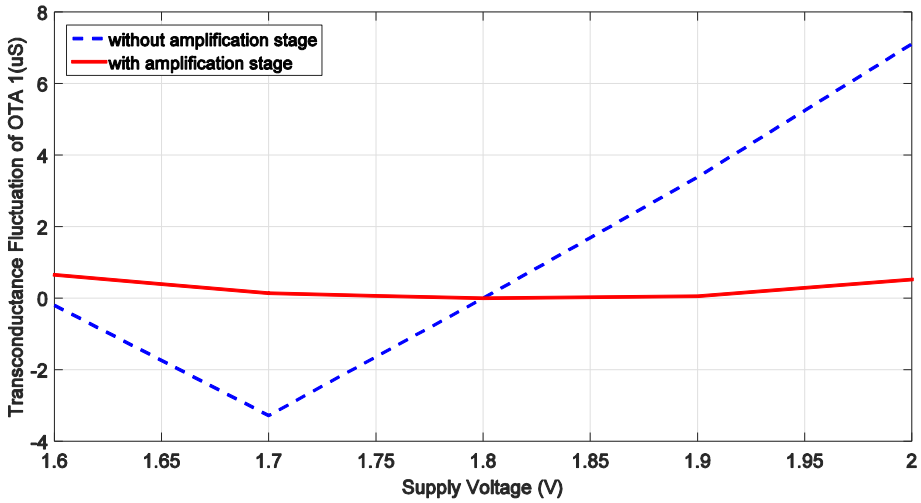

Figure 4.32 Transconductance fluctuation of OTA 1 as supply voltage changes

With Equation 4.20, the transconductance fluctuation of the OTA in the first integrator can be converted to phase shift fluctuation of the WB given that the FE loads the WB. Such fluctuation is plotted in Figure 4.33. As the supply voltage varies from 1.6V to 2.0V, the WB phase shift fluctuation due to the FE loading effect is 0.034 ° if the OTA in the first integrator is biased by the structure in Figure 4.28; once the biasing includes the amplification stage, the phase shift fluctuation is dramatically reduced to 0.002 °, which is 6.3% of the fluctuation in the former situation.

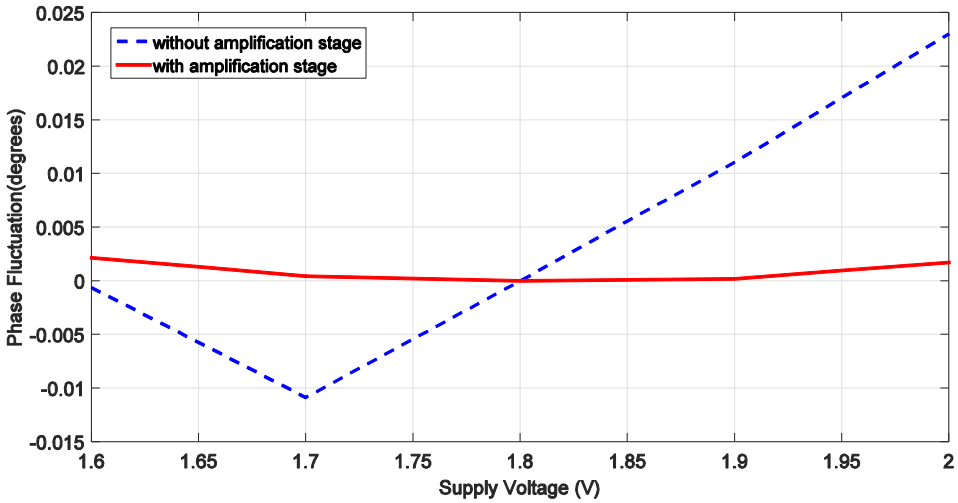

Figure 4.33 Phase shift fluctuation over supply voltage

Correspondingly, the temperature sensed by the WB is less sensitive to the supply variation once the amplification stage is incorporated in the biasing circuit, as shown in Figure 4.34. After adding the amplification stage in the biasing circuit, the temperature fluctuation is reduced from 0.30 ℃ to 0.02 ℃ as the supply voltage suffers ±0.2 V variation with respect to 1.8 V.

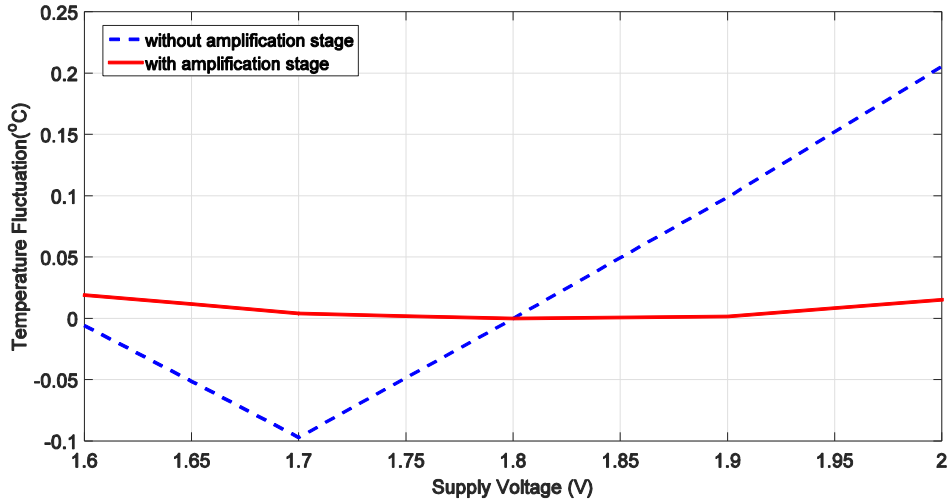

Figure 4.34 Temperature fluctuation over supply voltage

4.2.9.3 Start-Up Issue

An important issue in the biasing circuit shown in Figure 4.28 is the existence of the degenerate bias points, as is shown in Equation 4.34. When the supply voltage is switched on, if all the transistors carry zero current, they may remain this state since the loop allows zero current in both of the two branches indefinitely. This problem is called start-up issue.

To tackle this problem, a switch implemented by a PMOSFET is added in the biasing circuit, as is shown in Figure 4.31. When this switch M_{10} is on, a current path from the supply through M5 and M1 to the ground is created, driving the circuit out of the degenerate bias point. The switch is controlled by Signal SW_p, which is provided by an on-chip shift-register.

4.2.9.4 Stability Consideration

To stabilize the self-biasing loop in the biasing circuit, a capacitor C is added at one of the high impedance nodes in the loop, as is shown in Figure 4.31. This capacitor will dump the high frequency components in the loop to the ground in case that oscillating occurs due to the insufficient phase margin of the high frequency components.

4.3 Summary

In this chapter, the readout circuits for the temperature-sensing block, Wien Bridge, is implemented. The goal of the readout design is to preserve the inherent temperature-sensing resolution of the bridge in an energy-efficient way. To achieve this goal, a phase-domain 2^{nd} order 1-bit continuous-time delta-sigma ADC with the feedforward compensation is employed to digitize the bridge output. In the readout, the first stage is implemented by an active-RC integrator with demodulators inserted, of which the input-referred noise is lower than the noise of the bridge. A Gm-C integrator is employed as the second integrator. The quantizer is simply implemented by a comparator. The phase-domain DAC is implemented by a multiplexer. A biasing circuit which is capable of suppressing the supply fluctuation and providing biasing current with well-defined temperature dependency is designed. In Chapter 5, the chip performance measurement results are given and analysed.

Chapter 5 Measurement

The chip was fabricated in a TSMC180 nm CMOS process. Its photomicrograph is shown in Figure 5.1. The area of the chip is 1.5 × 1.5 mm, which is occupied by two sensors. It is packaged in a 24-pin dual in-line (DIL) ceramic package. For one sensor, the bridge consumes 9 μA current from a 1.8 V supply, while the readout electronics consume 52 μA current from a 1.8 V supply. In Cadence simulations, the bridge consumes 11 μA current from a 1.8 V supply, while the readout consumes 65 μA current. The measured power consumptions are slightly lower than the simulated values.

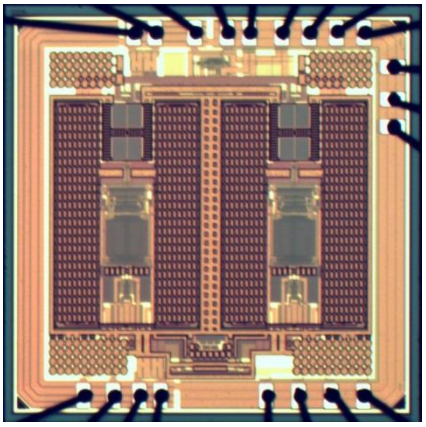

Figure 5.1 Chip photomicrograph (two identical sensors are incorporated in one chip.)

5.1 Measurement Setup

During the measurement, the chip is put in the oven. A PT-100 temperature sensor is also placed in the oven and its resistance is measured by a Keithley 2002 precision multimeter, to provide the temperature reference.

In order to stabilize the ambient temperature, an aluminium block with a volume of 2750 cm^3 (length = 27.5 cm, width = 20 cm, height = 5 cm) is placed in the oven, and the printed circuit board (PCB) is mounted tightly to the top of the aluminium block. Because the thermal conductivity of aluminium is much smaller than that of the air, the aluminium metal block acts as a thermal low-pass filter, which further stabilize the sensor's temperature during measurements. To ensure the chip has a reliable thermal contact with the aluminium block, and also to relieve the stress that the chip suffers, a thermal rubber is placed between the chip and the aluminium block surface. A PT-100 temperature sensor, which provides the temperature reference, is placed in a hole of the aluminium block near its one surface where the PCB is mounted. The measurement setup is shown in Figure 5.2.

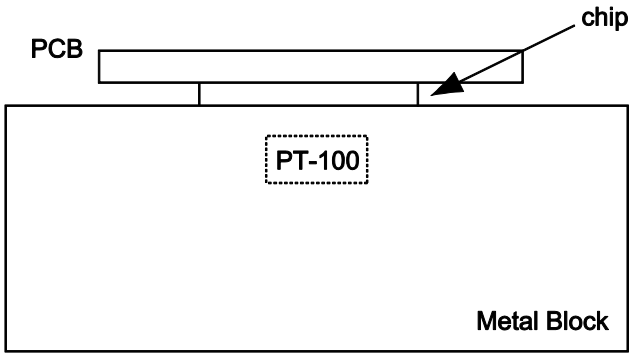

Figure 5.2 Measurement setup

Since the expected resolution is less than 1 mK, the ambient temperature fluctuation in the block is investigated first. Several experiments have been carried out. During these experiments, a PT-100 located in a hole in the aluminium block is used to provide the ambient temperature information. The ambient temperature stability is estimated at 10 ℃ and 40 ℃. Results show that the resolution of the measured temperature is 2 mK (rms).

Since the resistance of the PT-100 is readout by the Keithley, further experiments have been conducted to investigate if the measured temperature variation mainly comes from the ambient temperature fluctuation. Two extra experiments have been done. One experiment is using a Keithley 2002 with the same configuration to readout the resistance of a 100 Ω resistor which has a TC smaller than 10ppm. The other experiment is shorting this low-TC resistor to observe the readout of the Keithley. It turns out that in the total noise corresponding to 2 mK (rms) measured resolution, about 89% (noise power) comes from the combination of the PT-100's resistance and the input-referred noise of the Keithley.

According to the experiment data and analysis, it is fair to say that the ambient temperature fluctuation is not an obstacle to measuring sub-mK resolution.

To further suppress the effect of ambient temperature fluctuations during measurement, two sensors are placed in one chip, as proposed in [52]. In that design, with this measurement setup, a resolution of 0.16 mK in a 1-s conversion time was achieved. Since these two sensors are close to each other, they experience similar ambient temperature fluctuations. By sensing the difference of these two sensors' outputs, the ambient temperature fluctuations can be suppressed, because they will act as common-mode variations.

5.2 Measurement Results

5.2.1 Resolution

The power spectral density (PSD) of two sensors in one chip at 25 ℃ is shown in Fig. 5.3. The large DC term is the signal. A noise shaping behavior with a slope of 40 dB/decade is clearly observed in the PSD, which confirms that the order of the delta-sigma ADC is two.

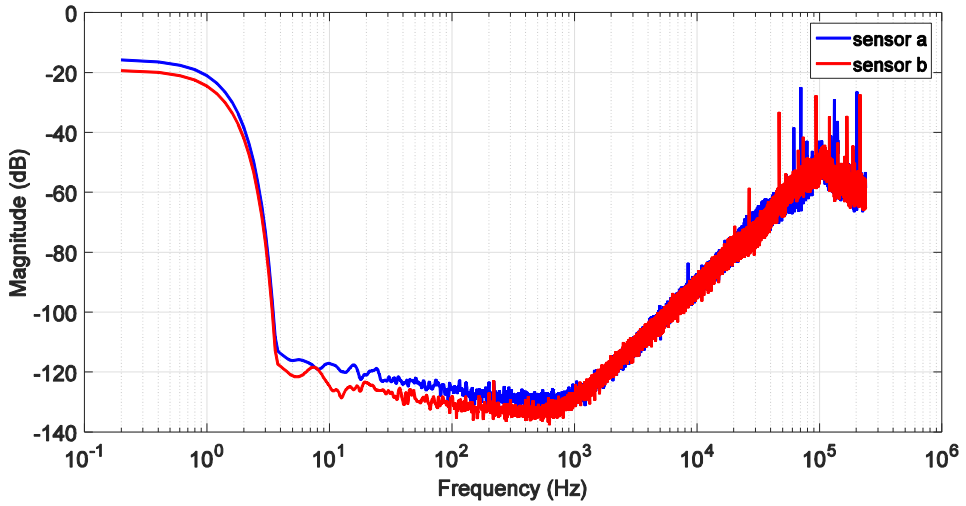

Figure 5.3 Power spectral density of two sensors in one chip (T = 30 ℃; frequency resolution = 0.4Hz)

The resolution in a 5 ms conversion time is 2.2 mK (rms) at 30 ℃, obtained from the differential output of the two sensors in one chip. The measured resolution is 10 times worse than the calculated value. It is essential to find out the reason for such a large difference.

Observing the PSD in Figure 5.3, the noise has a slope of 10 dB/decade at low frequency until around 650 Hz where noise shaping starts working. Apparently, flicker noise manifests itself within a relatively wide bandwidth. In order to confirm this conclusion, the relation between resolution (rms) and conversion time T_{conv} was investigated. To obtain the resolution for a conversion time of T_{conv}, 2000 successive conversions were taken; For each conversion, $f_s \times T_{conv}$ samples were logged and then decimated by a FIR filter. After multiplied by the decimated value-to-temperature sensitivity, the decimated values were converted into temperature values. To suppress the ambient temperature fluctuation, the output difference between the two sensors in one chip was taken and scaled by a factor of $\sqrt{2}$ [35] [52]. The standard deviation of the 2000 differential temperature values represents the resolution (rms) for a conversion time of T_{conv}.

The relation between resolution (rms) and conversion time T_{conv} is given in Figure 5.4. The solid curve represents resolution (rms), and the three dashed curves are three asymptotes which indicate the resolution-T_{conv} relations at different regions. When the conversion time is less than 1 ms, the temperature-sensing resolution decreases with respect to $1/T_{conv}^2$, indicating quantization noise is the dominant noise source in this region. Since 2nd order DSM is employed, resolution is improved at the rate of $1/T_{conv}^2$ in this region [37]. In a very short time-interval around 1 ms, resolution decreases with $1/\sqrt{T_{conv}}$. It indicates that within this short time-interval, thermal noise dominates. When the conversion time is larger than 2 ms, flicker noise takes over from thermal noise, in which case the resolution-T_{conv} relation can be expressed as Equation 5.1 [Appendix A].

$$dT = \sqrt{A \cdot ln\left(1 + \frac{B}{T_{conv}}\right) + \frac{C}{T_{conv}}} \tag{5.1}$$

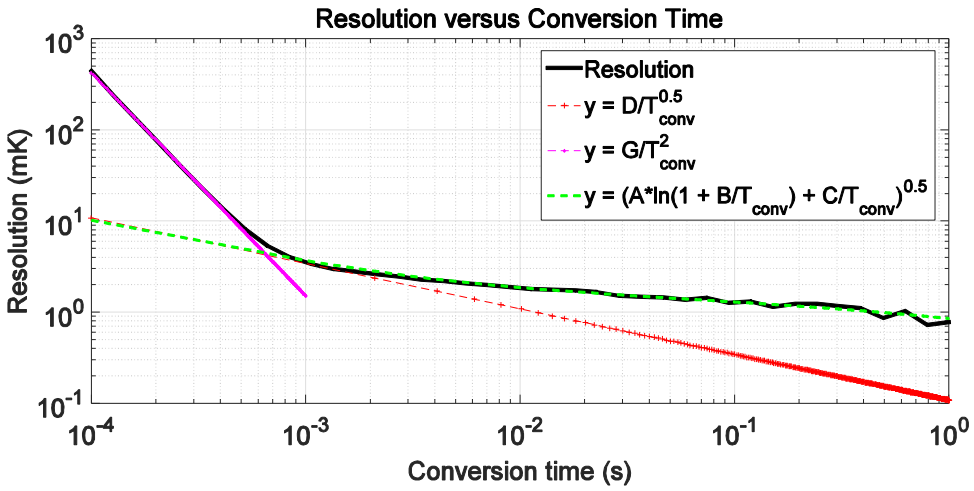

Figure 5.4 Resolution versus conversion time (T = 30 ℃)

The analysis above has shown that this design suffers from flicker noise, which is unexpected. Since the signal frequency is around DC, special attention has been paid to reduce flicker noise during design phase. However, the flicker noise corner frequency turns out to be much larger than expected, which degrades the temperature-sensing resolution significantly.

Investigation is required to find out the major flicker noise source in the design. The significant flicker noise is either from the Wien Bridge or from the readout circuitry, or even from both of them. As elaborated in Chapter 4, system-level chopping has been implemented to modulate the flicker noise of the readout out of signal band. However, no matter whether the system-level chopping is applied or not, the magnitude of the PSD at the low frequency band doesn't change significantly. If the major flicker noise comes from the readout, once the proper chopping frequency is applied, the noise magnitude of the PSD at signal band should be reduced compared with the magnitude when no system-level chopping is applied. However, if the major flicker noise comes from the bridge, system-level chopping doesn't help at all because the flicker noise from the bridge always mixes with the signal, system-level chopping in the readout cannot separate it from the signal.

There is a high possibility that the significant flicker noise comes from the bridge. Considering that the bridge is driven by the inverters, the resolution should degrade if increasing the inverter supply voltage. Because larger inverter supply means larger current going through the bridge, and flicker noise would increase as the current increases [44]. Figure 5.5 shows the resolution variation with respect to the driving inverter supply. The resolution of two sensors in one chip is shown, as well as the resolution obtained from these two sensors differentially. As the inverter supply increases from 0.7 V to 2.1 V, the resolution first reduces then keeps increasing. When the inverter supply increases from 0.7 V to 0.9 V, the resolution exhibits an opposite tendency compared with the tendency when the supply is higher than 0.9 V. This can be explained as follows: when the supply is too low, the electrostatic discharge (ESD) protection starts working. In this circumstance, the current going through the bridge is not proportional to the supply. When the inverter supply increases from 0.9 V to 2.1 V, the resolution keeps getting worse. This phenomenon can be explained as follows: as current going through the bridge increases, flicker noise in the bridge is getting higher.

There is no evidence indicating that the significant flicker noise is from the bridge driving inverters. Although the bridge is driven by CMOS inverters, and MOSFETs contribute flicker noise, Cadence simulation shows that the flicker noise corner frequency of these specially-sized CMOS inverters is lower than 1 mHz, as elaborated in Section 3.4. The flicker noise in MOSFETs is well-modeled; hence the simulation result should be reliable.

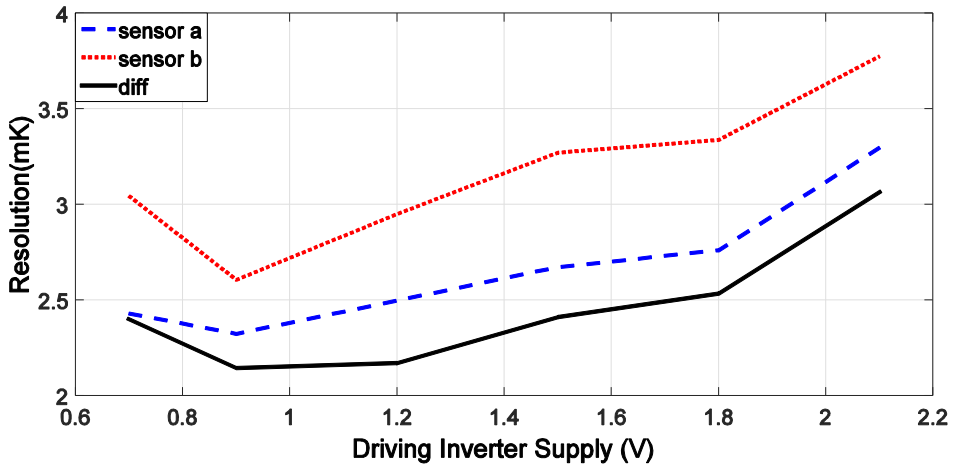

Figure 5.5 Resolution versus bridge driving inverter supply

Based on the analysis above, a conclusion can be made that the significant flicker noise comes from the bridge. The bridge consists of silicided poly resistors and MIM capacitors. The only possibility is that the significant flicker noise comes from the silicided poly resistors. In [32] and [44], it is suggested that flicker noise is proportional to the sheet resistance. So even though the flicker noise of silicided poly resistor is not modeled, considering that the sheet resistance of silicided poly resistors is much smaller than that of poly resistors, silicided poly resistors were used in the bridge. But if investigating into [32] and [44], both of them suggest that the flicker noise-sheet resistance relation applies to polysilicon resistors, and the mechanism of this relation is that the grain dimension in the polysilicon affects its sheet resistance; meanwhile, grain dimension is related to the flicker noise performance of polysilicon. In this sense, such flicker noise-sheet resistance relation should not be applied to the silicided poly resistor.

Referring to the smart temperature sensor proposed in [49], where silicided poly resistors are used as the temperature-sensing components, it also suffers from flicker noise. However, no further analysis on the origin of the flicker noise is given. Since there is the possibility that the dominant flicker noise in that design originates from the readout, no special concern arose when choosing silicided poly resistors as the temperature-sensing components in this project.

The flicker noise mechanism in silicided poly resistors is not modeled. Furthermore, no literature discussing the flicker noise of silicided polysilicon was found, literature on the origin of flicker noise has been studied, and there are at least two reasons that the silicided poly resistors would generate significant flicker noise.

The first reason is shown as following: during silicide formation process, metal ions from the silicide

target are being sputtered to the poly silicon surface, which will create plenty of incomplete bonds on the polysilicon surface, forming electron traps [53]. Although the silicided polysilicon will be subjected to further thermal processing to complete the silicon atom structure, certain amounts of traps are left on the interface between silicide and silicon, depending on the thermal process temperature and the lasting time. The trapping-detrapping process on the interfacial layer makes an important contribution to the flicker noise formation. The existence of such an interface state is the first reason why silicided polysilicon shows significant flicker noise.

The second reason is that the flicker noise in the polysilicon could still appear in a silicided poly resistor. The flicker noise in the polysilicon is mainly caused by the grain boundaries [22] [28], and in the polysilicon part of a silicided poly resistor, such boundaries still exist. There is a portion of current going through this polysilicon part, and this part of current could suffer from the flicker noise caused by the grain boundaries in the polysilicon.

5.2.2 Temperature-Sensing Accuracy

To estimate the inaccuracy of the temperature sensor, measurements have been done from -45 ℃ to 85 ℃ in steps of 10 ℃. For each temperature point, 500,000 points of the sensor output (corresponding to a conversion time of 1 s, and a resolution of 1.5 mK) are logged then averaged.

At each measurement temperature point, the bit stream capture will not start until the difference between two successive readouts of PT-100 is less than 1 m℃, when the ambient temperature is considered to be sufficiently stable with respect to the resolution of the sensor. This is important because during the inaccuracy measurement the ambient temperature fluctuation cannot be suppressed by the differential output of the two sensors in one chip.

Since the effect of process spread on the accuracy of a temperature sensor is random, a large number of samples need to be measured to obtain reliable estimation of the inaccuracy. Assuming the process spread has a Gaussian distribution, the standard deviation estimated from measurements on N samples will have a standard deviation of $1/\sqrt{2N}$ [8]. In this project, 12 chips have been characterized in a temperature-controlled oven from -45 ℃ to 85 ℃. Since in each chip, there are two identical sensors, 24 sensors have been measured in total. Therefore, the standard deviation estimated from the measurement on 24 sensors has a standard deviation of 14.4%.

The decimated values of the 24 sensors over temperature are shown in Figure 5.6. The corresponding phase shift is calculated and plotted in Figure 5.7. The output variation of these 24 sensors is 21.2%. And their average phase shift over the temperature range from -45 ℃ to 85 ℃ is 14.64°. Combined with Equation 3.13, the TC of silicided poly resistors can be estimated, which is 0.29%/℃. This is close to the value given in the technology data sheet.

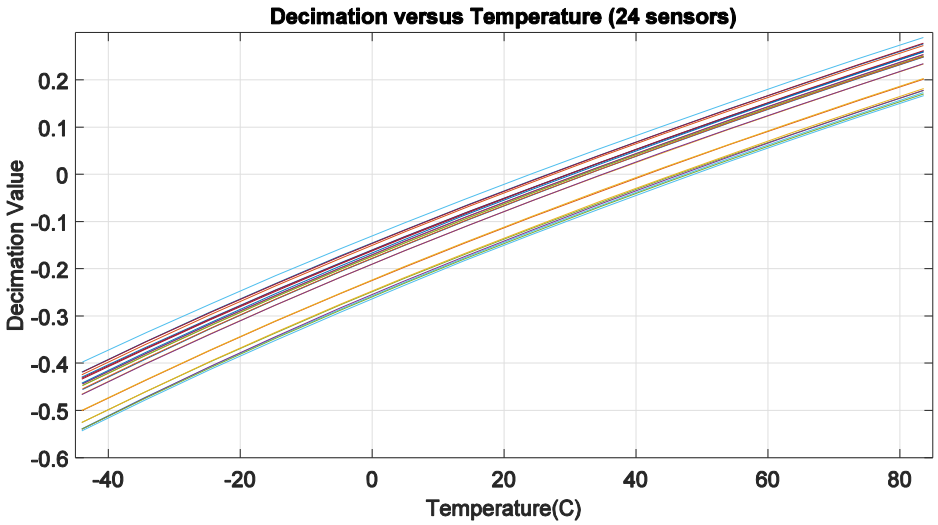

Figure 5.6 Decimated values over temperature

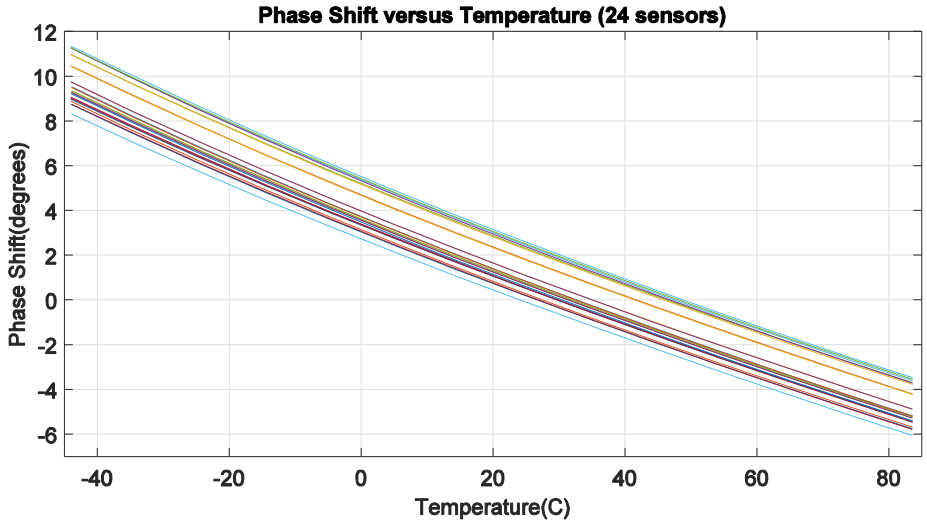

Figure 5.7 Phase shift over temperature

Based on all the measurement data, one optimum polynomial (in a least-squares sense) can be assigned to each sensor. After individual 1st and 2nd order optimum polynomial fitting, the temperature-sensing residual error is given in Figure 5.8 a) and Figure 5.9 a). After being fitted by an n^{th} order polynomial, $(n+1)^{th}$-order error dominates, which can be removed as systematic error. The error after 1st and 2nd optimum polynomial fitting and systematic error removing is shown in Figure 5.8 b) and Figure 5.9 b), respectively.

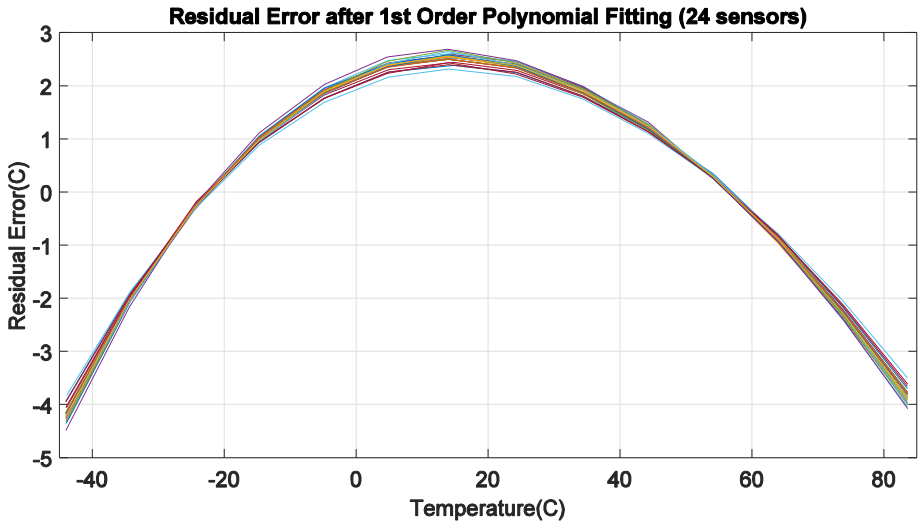

Figure 5.8 a) Residual error after a 1st order optimum polynomial fitting

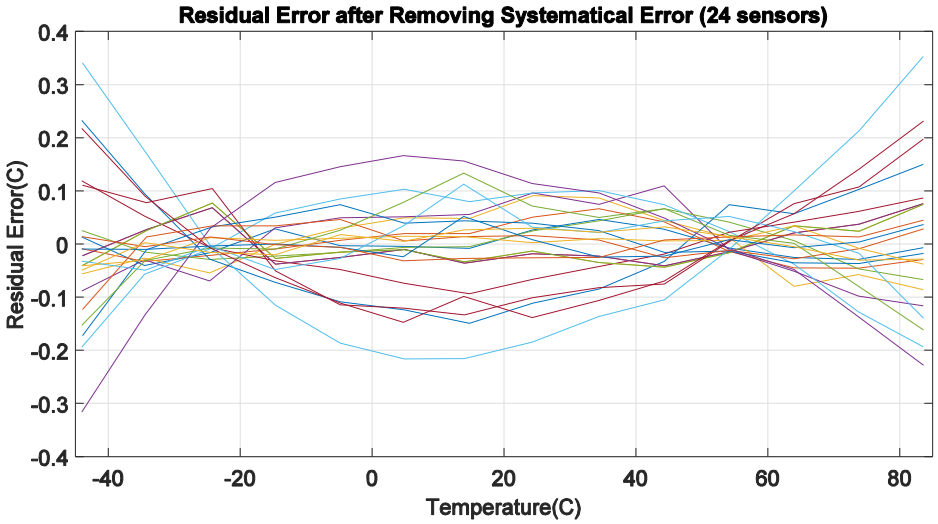

Figure 5.8 b) Residual error after a 1st order optimum polynomial fitting and systematic error removing

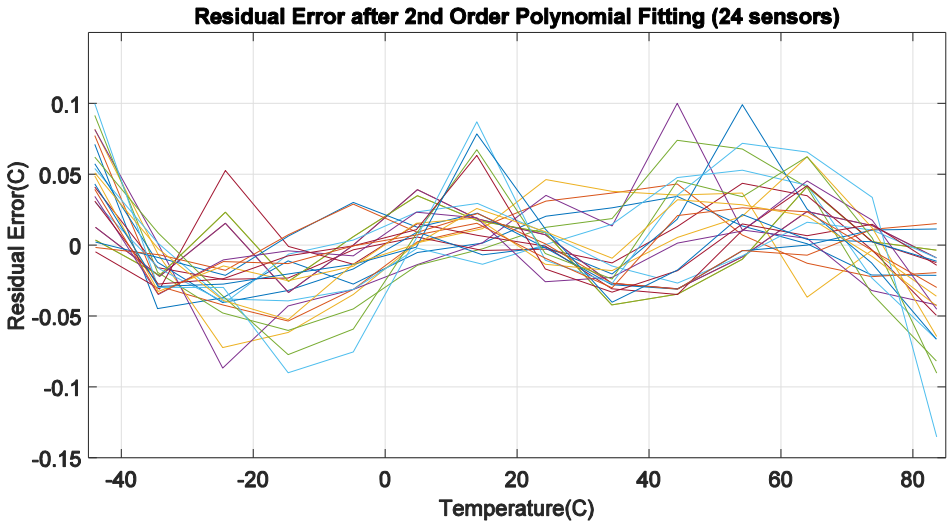

Figure 5.9 a) Residual error after a 2nd order optimum polynomial fitting

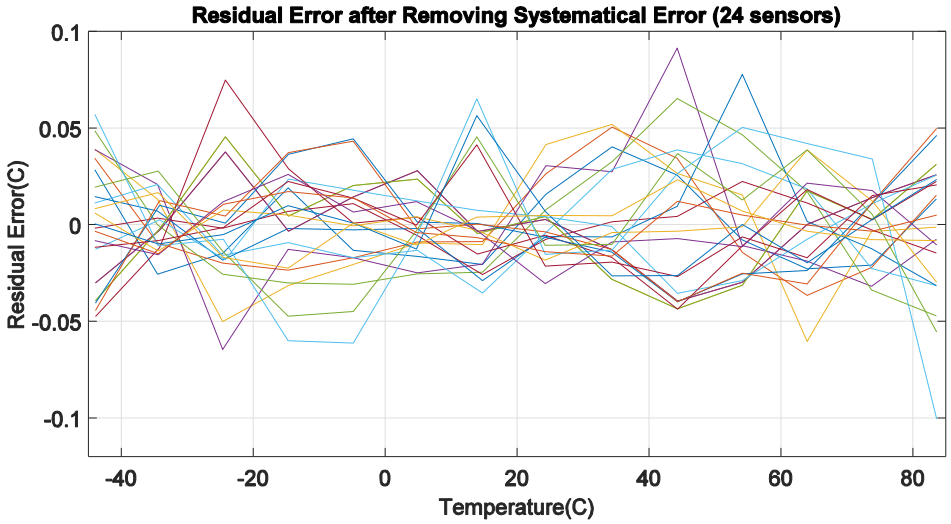

Figure 5.9 b) Residual error after a 2nd order optimum polynomial fitting and systematic error removing

Compared with Cadence simulation results, the residual error after the 2nd order optimum polynomial fitting, as shown in Figure 5.9 a), is slightly larger than the simulation results in the nominal process corner, and smaller than that in the fast and slow process corners.

It is noted that to obtain the optimum x^{th}-order polynomial for each sensor requires more than $(x+1)$ data points, which is costly. Therefore, another more practical approach has been performed to analyze the measurement data.

This approach is to apply individual x^{th}-order polynomial to each sensor, and the polynomial is obtained by measuring $(x+1)$ temperature points.

To obtain a 1st order polynomial for each sensor, the decimated values at -45 ℃ and 85 ℃ are used. With applying the 1st order polynomial, the temperature-sensing residual error for the 24 sensors is

given in Figure 5.10 a). And the residual after removing systematic error is given in Figure 5.10 b).

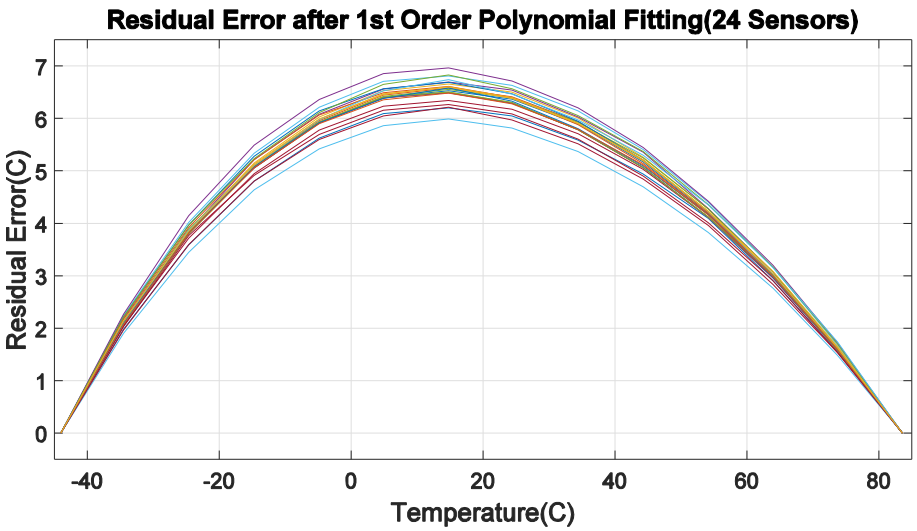

Figure 5.10 a) Residual error after a 1st order polynomial fitting

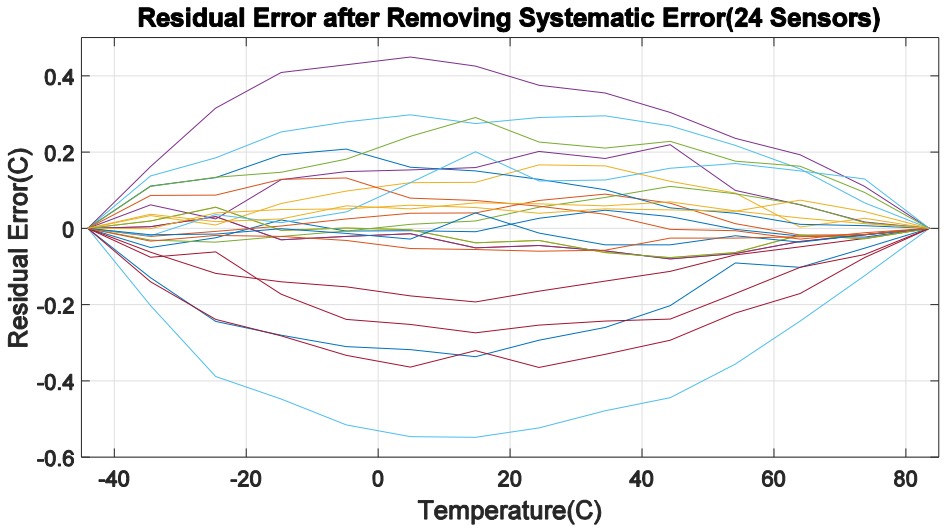

Figure 5.10 b) Residual error after a 1st order optimum polynomial fitting and systematic error removing

In a similar way, three decimated values at -45 ℃, 25 ℃ and 85 ℃ are used to obtain a 2nd order polynomial for each sensor. The residual error after applying polynomial fitting is given in Figure 5.11 a). And the residual after removing systemic error is given in Figure 5.11 b).

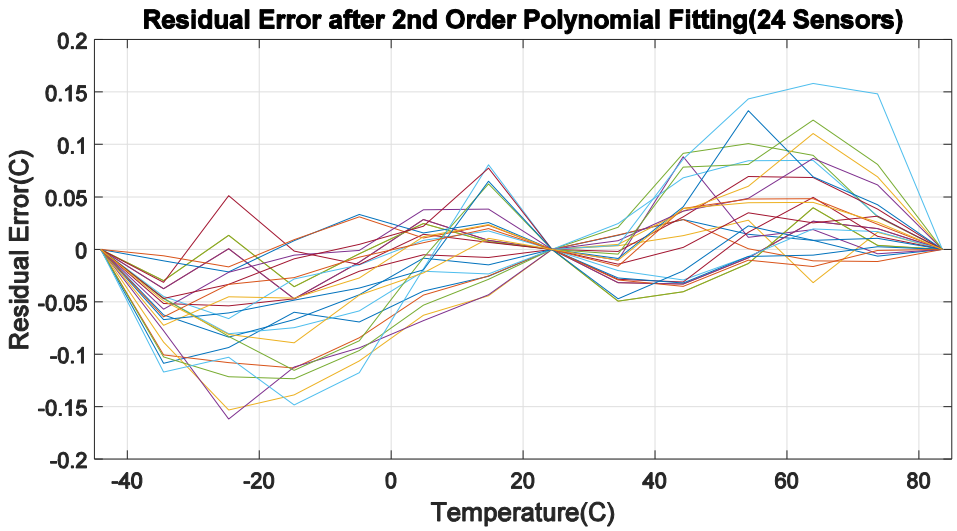

Figure 5.11 a) Residual error after a 2nd order polynomial fitting

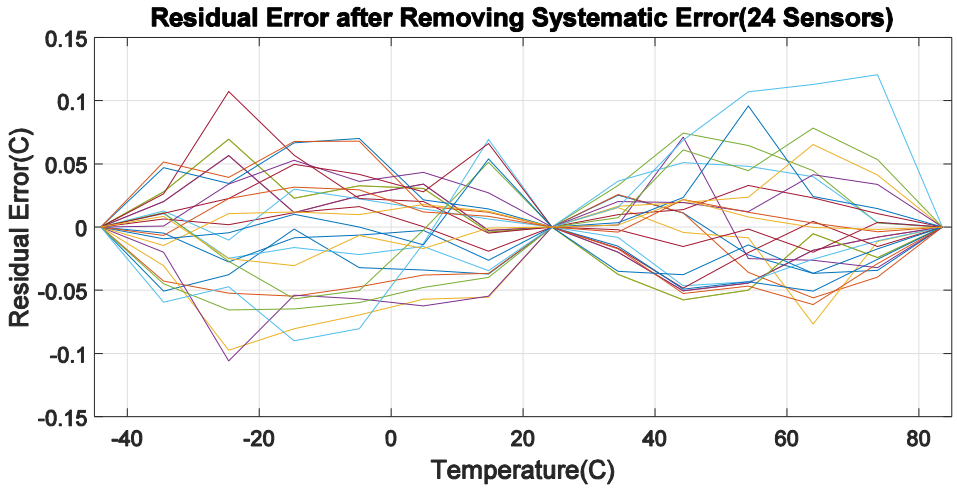

Figure 5.11 b) Residual error after a 2nd order optimum polynomial fitting and systematic error removing

With an optimized 2nd order individual polynomial fitting (least-squares fitting), the temperature-sensing inaccuracy is less than 0.1 ℃ (min-max) over temperature range from -45 ℃ to 85 ℃ for the 24 samples; However, if the 2nd order individual polynomial is obtained from the minimum number of data points (three), which is less optimum, the temperature-sensing inaccuracy increases to ±0.12 ℃ (min-max).

5.2.3 Voltage Dependency

The sensor is designed to achieve high temperature-sensing resolution and high accuracy, thus any interference should be tackled gingerly. In analog circuitry, the supply is one of the interference contributors. During the design phase, an amplification stage is added to the biasing circuit to reduce the readout supply dependency, especially supply dependency of the FE. The actual supply dependency of the sensor should be evaluated by measurement. Apart from the analog part, the WB driving

inverters are supplied separately. Therefore, the total supply dependency, the analog supply dependency and the WB driver supply dependency are measured respectively. The temperature fluctuation of the sensor due to supply variation is given in Figure 5.12. It can be seen that the total supply dependency is 1.2 ℃/V, the analog supply dependency is -0.85 ℃/V, and the driver supply dependency is 2 ℃/V in the worst case. Referring to Figure 4.34, the simulated analog supply dependency is less than 0.05 ℃/V. However, in that simulation, only the supply dependency of the transconductance of the first OTA is considered; in fact, the supply fluctuation manifests itself via many ways, *e.g.* via the common-mode voltages of the OTAs in the two integrators. But in a Delta-Sigma ADC, it takes long to simulate these kinds of effects, so simulations were not performed regarding these effects.

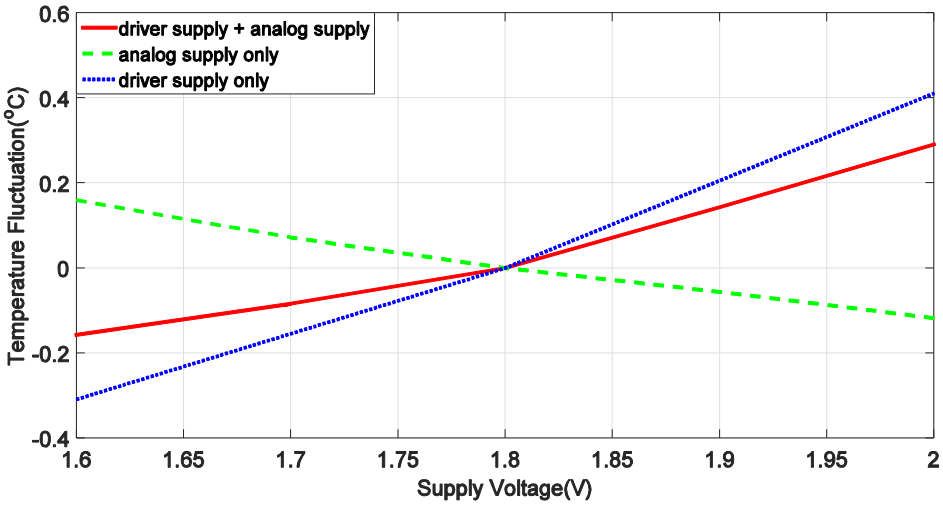

Figure 5.12 Sensor supply dependency

The measurement shows that the sensor's output is highly sensitive to the WB driving supply variation. This can be explained as follows: when the PMOSFETs in the driving inverters are switched on, the WB sees the supply rail directly. Any fluctuation in the supply rail would manifest itself as amplitude noise in the WB driving square wave. After demodulating, such amplitude noise converts to charge error being integrated by the first integrator, leading to a temperature-sensing error. When the PMOSFETs are switched off, the supply fluctuation still affects the amplitude of the driving square wave due to the large dimension of the driving inverters. As elaborated in Section 3.4, large dimension is chosen to reduce the flicker noise corner frequency of the driving inverters. However, large transistor size leads to large parasitic capacitance, and low off-resistance, resulting in a poor supply noise rejection performance in this particular part.

In Figure 5.12 it is worth to note that the temperature fluctuation with respect to analog supply variation has an opposite tendency compared with the fluctuation with respect to WB driving supply variation. Therefore, to minimize the supply dependency of the sensor during measurement, the WB driver and the analog part are supplied by the same source.

5.3 Summary

The performance of the temperature sensor is listed in Table 5.1, and comparisons with the target

specifications as well as with the previous work are given in Table 5.1 a) and Table 5.1 b), respectively.

Table 5.1 a) Performance Comparison between target value and measured value

	Target	Measurement result
resolution	< 0.2 mK (rms) in a 100-Hz BW	2.2 mK (rms) in a 100-Hz BW
Power consumption	< 100 μW	110 μW
FOM* (pJ·K^2)	< 0.02	2.7

* $FOM = energy\ per\ conversion \times (temperature\ resolution)^2$ [8]

Table 5.1 b) Performance comparisons with previous work

	This Work	JSSC [14]	ESSCIRC [15]	JSSC [35]	ASSC [46]
Sensor type	Resistor	Resistor	Resistor	Resistor	Resistor
Technology(μm)	0.18	0.18	0.18	0.18	0.18
Area(mm^2)	1.13	0.18	0.35	0.09	0.43
Resolution(mK) (conversion time)	2.2 (5 ms)	0.1 (100 ms)	6 (100 ms)	2.8 (32 ms)	10 (0.1 ms)
Inaccuracy(℃) (Cali. points)	±0.12 (3)	±0.015 (6)	±0.15	±0.12 (3)	±0.4 (2)
Temperature range	-45℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃	-45℃ to 125℃
Power(μW)	110*	13000	36	31	77.4
FOM (pJ·K^2)	2.7	13	130	8	0.65

*Two sensors are incorporated in one chip; this value is for one sensor.

Table 5.1 a) indicates that the achieved resolution is more than 10 times worse than the target, mainly due to the un-modeled significant flicker noise from the WB resistors. The power consumption is 10% higher than the target value.

Although no specification reaches the target, this design is still comparable with the state-of-the-art temperature sensors, as shown in Table 5.1 b).

Chapter 6 Conclusion and Future Work

6.1 Conclusion

A resistor-based smart temperature sensor has been designed. To implement high temperature-sensing resolution, a WB is employed, where silicided-polysilicon resistors work as the temperature-sensing components and a low-jitter clock together with low-temperature-dependent MIM capacitors work as the reference. To preserve the inherent high resolution of the WB, noise from the readout electronics has been designed to be lower than the noise from the WB itself. To achieve a high energy-efficiency, a 2^{nd} order 1-bit CT DSM is employed as the readout. In the readout, the first integrator is implemented by an active-RC filter, and the second integrator is implemented by a Gm-C integrator. To maintain the loop stability, a novel feedforward structure is employed to simplify the compensation path in an energy-efficient way.

A temperature-sensing resolution of 2.2 mK (rms) in a 5-ms conversion time is achieved, leading to a FOM of 2.7 pJ K^2. 24 sensors have been measured to evaluate the temperature-sensing accuracy over the temperature range from -45 ℃ to 85 ℃. With a 3-point calibration, a temperature-sensing inaccuracy of ±0.12 ℃ (min-max) is achieved for the 24 samples.

Although the sensor suffers from significant flicker noise, limiting its resolution to 2.2 mK (rms) in a 5-ms conversion time, its performance is comparable with other state-of-the-art temperature sensors.

6.2 Future Work

The temperature-sensing resolution in this work is limited by the flicker noise from the WB resistors, which are silicided-polysilicon resistors. Although no literature, which describes the flicker noise characteristics of such resistors, was found; and no flicker noise model was available in the chosen technology, either. Based on the flicker noise mechanism and the tests conducted during measurement as is shown in Section 5.2.1.2, silicided-polysilicon resistors in the technology generate significant flicker noise, which is unacceptable in the applications where the signal band is near DC. Even though silicided-polysilicon resistors have high TC and relatively high linearity, it is not suitable for the application. Instead, N-well resistors could be better candidates due to their high TC and low flicker noise [15]. However, the voltage-dependency of N-well resistors should be investigated.

The temperature-sensing accuracy highly depends on the supply variation, especially the supply variation of the WB driver. To reduce this, a voltage regulator can be employed.

The sensor has a relatively large area compared with other resistor-based temperature sensors. The major area in the sensor is occupied by the integrating capacitors in the first integrator. The reason that large integrating capacitors are used in the first integrator is to reduce the output swing of the first OTA, which is implemented by a telescopic structure. To reduce the integrating capacitance, the telescopic OTA used in the first stage could be replaced by other OTA structures. The new OTA should have a high output swing and be able to maintain the noise, gain and power performance of a telescopic OTA.

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Bibliography

[1] Kilby, J. S. "Miniaturized electronic circuits [US Patent No. 3,138, 743]." *Solid-State Circuits Society Newsletter, IEEE* 12.2 (2007): 44-54.

[2] *The Chip that Jack Built*, (c. 2008), (HTML), Texas Instruments, Retrieved 29 May 2008.

[3] http://www.intel.com/content/www/us/en/history/museum-gordon-moore-law.html

[4] https://www.cymer.com/moore-s-law

[5] "International Technology Roadmap for Semiconductors, Lithography Summary", 2013 version

[6] http://www.asml.com.tw/doclib/investor/asml_3_Investor_Day-Many_ways_to_shrink_MvdBrink1.pdf

[7] http://www.intel.com/content/www/us/en/silicon-innovations/intel-22nm-technology.html

[8] K.A.A. Makinwa. "Smart temperature sensors in standard CMOS." *Procedia Engineering* 5 (2010): 930-939.

[9] Pertijs, Michiel AP, K.A.A. Makinwa, and Johan H. Huijsing. "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1 °C from -55 °C to 125 °C." *Solid-State Circuits, IEEE Journal of* 40.12 (2005): 2805-2815.

[10] Ueno, Ken, Tetsuya Asai, and Yoshihito Amemiya. "Temperature-to-frequency converter consisting of subthreshold MOSFET circuits for smart temperature-sensor LSIs." *Solid-State Sensors, Actuators and Microsystems Conference, 2009. TRANSDUCERS 2009. International*. IEEE, 2009.

[11] Türkes, P. "An ion-implanted resistor as thermal transient sensor for the determination of the thermal diffusivity in silicon." *physica status solidi (a)* 75.2 (1983): 519-523.

[12] Kashmiri, Sayyed Mahdi. "Thermal-Diffusivity-Based Frequency References in Standard CMOS." PhD diss., TU Delft, Delft University of Technology, 2012.

[13] van Vroonhoven, Caspar PL, Dan d'Aquino, and K.A.A. Makinwa. "A thermal-diffusivity-based temperature sensor with an untrimmed inaccuracy of ±0.2 °C (3σ) from 55 °C to 125 °C." In *2010 IEEE International Solid-State Circuits Conference-(ISSCC)*. 2010.

[14] Perrott, Michael H., Jim C. Salvia, Fred S. Lee, Aaron Partridge, Sayan Mukherjee, Carl Arft, Jintae Kim et al. "A Temperature-to-Digital Converter for a MEMS-Based Programmable Oscillator With Frequency Stability and Integrated Jitter." *Solid-State Circuits, IEEE Journal of* 48, no. 1 (2013): 276-291.

[15] Shahmohammadi, Mina, Kianoush Souri, and K.A.A. Makinwa. "A resistor-based temperature sensor for MEMS frequency references." In *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, pp. 225-228. IEEE, 2013.

[16] K.A.A. Makinwa, "Smart Temperature Sensor Survey", [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

[17] Heidary, Ali, Guijie Wang, K.A.A. Makinwa, and Gerard Meijer. "12.8 A BJT-based CMOS temperature sensor with a 3.6 pJ· K^2-resolution FoM." In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, pp. 224-225. IEEE, 2014.

[18] A. Niknejad, B. E. Boser, “Lecture 7: IC Resistors and Capacitors”, *EECS 105, Microelectronic Devices and Circuits,* pp. 13. University of California, Berkeley, 2003.

[19] Deen, M. Jamal, S. L. Rumyantsev, and M. Schroter. "On the origin of 1/f noise in polysilicon emitter bipolar transistors." *Journal of applied physics* 85, no. 2 (1999): 1192.

[20] Seto, John YW. "The electrical properties of polycrystalline silicon films." *Journal of Applied Physics* 46, no. 12 (1975): 5247-5254.

[21] El-Kareh, Badih. "Silicon Devices and Process Integration." *New York: Springer. doi* 10, no. 1007 (2009): 978-0.

[22] Chen, X. Y., J. A. Johansen, C. Salm, and A. D. van Rheenen. "On low-frequency noise of polycrystalline Ge x Si 1− x for sub-micron CMOS technologies." *Solid-State Electronics* 45, no. 11 (2001): 1967-1971.

[23] Cowher, M. E., and T. O. Sedgwick. "Chemical vapor deposited polycrystalline silicon." *Journal of the Electrochemical Society* 119, no. 11 (1972): 1565-1570.

[24] Fripp, A. L. "Dependence of resistivity on the doping level of polycrystalline silicon." *Journal of Applied Physics* 46, no. 3 (1975): 1240-1244.

[25] Seto, John YW. "The electrical properties of polycrystalline silicon films." *Journal of Applied Physics* 46, no. 12 (1975): 5247-5254.

[26] Kamins, T. I. "Hall mobility in chemically deposited polycrystalline silicon." *Journal of applied physics* 42, no. 11 (1971): 4357-4365.

[27] Rai-Choudhury, P., and P. L. Hower. "Growth and characterization of polycrystalline silicon." *Journal of the Electrochemical Society* 120.12 (1973): 1761-1766.

[28] Madenach, Armin J., and Jürgen H. Werner. "Noise spectroscopy of silicon grain boundaries." *Physical Review B* 38, no. 18 (1988): 13150.

[29] Dimitriadis, C. A., J. Brini, and G. Kamarinos. "Low frequency noise in intrinsic low pressure chemical vapour deposited polysilicon resistors." *The European Physical Journal Applied Physics* 3, no. 03 (1998): 283-285.

[30] De Graaff, H. C., and M. T. M. Huybers. "1/f noise in polycrystalline silicon resistors." *Journal of Applied Physics* 54, no. 5 (1983): 2504-2507.

[31] Luo, Min-Yih, and Gijs Bosman. "An analytical model for 1/f noise in polycrystalline silicon thin films." *Electron Devices, IEEE Transactions on* 37, no. 3 (1990): 768-774.

[32] Vandamme, L. K. J., and H. J. Casier. "The 1/f noise versus sheet resistance in poly-Si is similar to poly-SiGe resistors and Au-layers." In *Solid-State Device Research conference, 2004. ESSDERC 2004. Proceeding of the 34th European*, pp. 365-368. IEEE, 2004.

[33] Wu, Rong. *Precision Instrumentation Amplifiers and a Read-Out IC for Sensor Interfacing*. TU Delft, Delft University of Technology, 2011.

[34] Wu, Rong, K.A.A. Makinwa, and Johan H. Huijsing. "A chopper current-feedback instrumentation amplifier with a 1 mHz noise corner and an AC-coupled ripple reduction loop." *Solid-State Circuits, IEEE Journal of* 44, no. 12 (2009): 3232-3243.

[35] P. Park, D. Ruffieux, and K. A. A. Makinwa, “A thermistor-based temperature sensor for a real-time clock with ±2 ppm frequency stability,” *IEEE J. of Solid-State Circuits*, vol. 50, no. 7, pp. 1571-1580, Jul. 2015.

[36] Young, Brian, Sunwoo Kwon, Amr Elshazly, and Pavan Kumar Hanumolu. "A 2.4 ps resolution 2.1 mW second-order noise-shaped time-to-digital converter with 3.2 ns range in 1MHz bandwidth." In *Custom Integrated Circuits Conference (CICC), 2010 IEEE*, pp. 1-4. IEEE, 2010.

[37] Schreier, Richard, and Gabor C. Temes. *Understanding delta-sigma data converters*. Vol. 74. Piscataway, NJ: IEEE press, 2005.

[38] Munoz, F., K. Philips, and A. Torralba. "A 4.7 mW 89.5 dB DR CT complex Delta Sigma ADC with built-in LPF." In *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.* 2005.

[39] Cho, Thomas Byunghak, and Paul R. Gray. "A 10 b, 20 M sample/s, 35 mW pipeline A/D converter." *Solid-State Circuits, IEEE Journal of* 30, no. 3 (1995): 166-172.

[40] Pelgrom, Marcel JM. *Analog-to-digital Conversion*. Springer Netherlands, 2010.

[41] Rabaey, Jan M., Anantha P. Chandrakasan, and Borivoje Nikolic. *Digital integrated circuits*. Vol. 2. Englewood Cliffs: Prentice hall, 2002.

[42] Romano, L., S. Levantino, S. Pellerano, C. Samori, and A. Lacaita. "Low jitter design of a 0.35 μm-CMOS frequency divider operating up to 3GHz." In *Solid-State Circuits Conference, 2002. ESSCIRC 2002. Proceedings of the 28th European*, pp. 611-614. IEEE, 2002.

[43] Behzad, R. A. Z. A. V. I. "Design of analog CMOS integrated circuits." *International Edition. The McGraw-Hill Companies, Inc.–2001* (2001).

[44] Buisson, Dit, O. Roux, and G. Morin. "Flicker noise characterization of polysilicon resistors in submicron BiCMOS technologies." In *Microelectronic Test Structures, 1997. ICMTS 1997. Proceedings. IEEE International Conference on*, pp. 49-51. IEEE, 1997.

[45] Vandamme, L. K. J. "Noise as a diagnostic tool for quality and reliability of electronic devices." *Electron Devices, IEEE Transactions on* 41, no. 11 (1994): 2176-2187.

[46] Weng, Chan-Hsiang, Chun-Kuan Wu, and Tsung-Hsien Lin. "A CMOS thermistor-embedded continuous-time delta-sigma temperature sensor with a resolution of 0.01° C." In *Solid-State Circuits Conference (A-SSCC), 2014 IEEE Asian*, pp. 149-152. IEEE, 2014.

[47] Wu, Rong, Johan H. Huijsing, and K.A.A. Makinwa. "A 21b±40mv range read-out ic for bridge transducers." In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, pp. 110-112. IEEE, 2011.

[48] K. Souri and K.A.A. Makinwa, “A 0.12mm2 7.4μW Micropower Temperature Sensor with an Inaccuracy of ±0.2 °C (3σ) from -30 °C to 125 °C,” JSSC, vol. 46, No. 7, pp. 1693-1700, July 2011.

[49] X. Tang, W. T. Ng, K. P. Pun, “A Resistor-Based Sub-1-V CMOS Smart Temperature Sensor for VLSI Thermal Management”, VLSI System, vol. 23, No. 9, pp. 1651-1660, September, 2014.

[50] http://www.sitime.com/products/oscillators/sit8208#magictabs_Qz100_1

[51] http://www.ko4bb.com/~bruce/TDC.html

[52] Ng, Eldwin J., Hyung Kyu Lee, Chae Hyuck Ahn, Renata Melamud, and Thomas W. Kenny. "Stability measurements of silicon MEMS resonant thermometers." In *Sensors, 2011 IEEE*, pp. 1257-1260. IEEE, 2011.

[53] Krishna Saraswat, “EE311: Advanced Integrated Circuit Fabrication Technology, Interconnections: Silicides”, *Lecture notes 11*, Stanford university, 2006.

Appendix A

The Relation between Resolution and Conversion Time in the Flicker Noise Dominant Region

As introduced in Chapter 5, to obtain the resolution for a conversion time of T_{conv}, 2000 successive conversions were taken; For each conversion, $f_s \times T_{conv}$ samples were logged and then decimated by a FIR filter.

To find out the relation between the resolution and the conversion time T_{conv} in the region where flicker noise dominates, first the relation between the filtered noise and the bandwidth (BW) is investigated. Since it is difficult to express flicker noise in the time domain, the calculation is conducted in the frequency domain.

The noise power spectral density is given in Figure A.1, where f_c is the flicker noise corner frequency, and $\overline{v_{n,th}{}^2}$ is the thermal noise power spectral density.

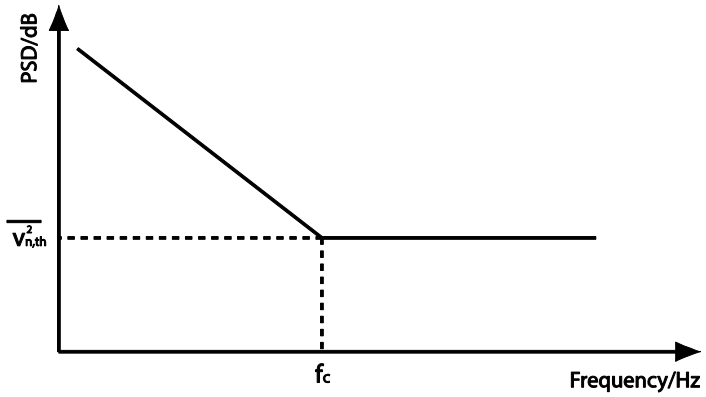

Figure A.1. Noise power spectral density

The noise power spectral density in the region where flicker noise dominates can be expressed as Equation A.1.

$$S_v(f) = \overline{v_{n,th}{}^2}\left(1 + \frac{f_c}{f}\right) \qquad (A.1)$$

As mentioned before, the noise is filtered by a FIR filter with a length of $f_s \times T_{conv}$. Given that the sampling frequency is relatively high compared with the signal bandwidth in this design, it is fair to approximate the FIR filter to a brick-wall filter. Assuming that the transfer function of the brick-wall filter in the passband is H_0, the filtered noise can be expressed as Equation A.2.

$$S_{v,filtered}(f) = S_v(f)|_{f=0\to BW} \times {H_0}^2 \qquad (A.2)$$

The total noise power in the signal band after being filtered can be expressed as Equation A.3.

$$S_{v,tot} = \left(\int_{f_a}^{f_a+BW} \frac{f_c \times \overline{v_{n,th}^2}}{f} \, df + \overline{v_{n,th}^2} \times BW \right) \times {H_0}^2 \qquad (A.3)$$

In Equation A.3, f_a is the starting frequency from which the flicker noise is considered.

According to Equation 3.15, the resolution corresponding to a noise power $S_{v,tot}$ can be expressed as Equation A.4.

$$dT = \frac{\sqrt{S_{v,tot}}}{S_T^V} = \sqrt{A \cdot ln\left(1 + \frac{BW}{f_a}\right) + N \cdot BW} \qquad (A.4)$$

In Equation A.4, S_T^V is the WB sensitivity, given by Equation 3.14; A and N are coefficients which are independent of BW. Equation A.5 gives the relation between the conversion time and the bandwidth. By combining Equation A.4 and Equation A.5, the relation between the resolution and the conversion time can be obtained, as given in Equation A.6, where A, B and C are coefficients which are independent of T_{conv}.

$$T_{conv} = \frac{1}{2BW} \qquad (A.5)$$

$$dT = \sqrt{A \cdot ln\left(1 + \frac{B}{T_{conv}}\right) + \frac{C}{T_{conv}}} \qquad (A.6)$$