3D NAND memory as radiation monitor

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SUMMARY

This thesis explores the feasibility of using 3D NAND flash memory as space radiation monitor. Space radiation is composed by ionizing particles such as protons and ions, which can be harmful to electronics. Shielding and Error Correcting Code can be implemented to counteract these effects. Monitoring the space radiation environment is necessary to better understand the space radiation environment and design shielding and ECC according to the exposed dose of a spacecraft during its mission. Following the trend of miniaturization, using 3D NAND flash technology will drive down the cost of a radiation monitor. This allows for space radiation monitors which can be used on small satellites such as a picosatellites.

3D NAND memory uses electrical charge to store information in bits. The amount of charge that is stored depends on the applied threshold voltage. Literature [1] has shown that the stored charge in a memory cell can be affected by radiation, causing bitflips. The threshold voltage of a memory cell can be read by using hardware and software developed at Delft University of Technology. [2] The preliminary design of the space radiation monitor can easily be adapted to work with any 3D NAND memory chip without the need of any proprietary information from the manufacturer. This work focuses on the analysis of the experimental data from a radiation test at CERN [3] and Monte Carlo simulations[4] of radiation on memory cells. A Ultra-High Energy Pb Ion Beam was used for the CERN radiation test. Furthermore, the internal structure of the 3D NAND memory was investigated and a mapping from the logical pages to the physical memory cell location was established.

The 3D NAND flash memory consist of multiple memory blocks. Each memory block has rows of memory cells which are referred to as a memory page. Multiple pages next to each other form a layer in a memory block. The used memory chip in this work has 64 layer. Data is written and read per page. To speed up the read operation of a whole memory block, a binary search was incorporated in the original read-out method.
The improved search method first analyzes 8 layers as a quick scan through a memory block to identify pillars of memory cells affected by radiation. After the quick scan, a more detailed measurement of the threshold voltage is performed around the affected pillars by using the binary search. This search method reduces the read operation from 10 hours to 20 minutes and the required data storage from 3 GB to 50 MB. The binary search method was verified by using a LogicAnalyzer. The signals probed from the 3D NAND memory were checked to follow a binary search sequence.

A data analysis has been performed on three chips which were tested at CERN. The first two chips were irradiated at a perpendicular angle and the third chip was irradiated with a 30° angle. The data was filtered to only account for threshold voltages that deviate more than two times the standard deviation from the mean. From the filtered data, tracks of the particles could be found in affected pillars for the first two chips and a 30° angle was observed in the third memory chip. The track of the pillars also verify the proposed internal mapping of the memory cells relative to each other.

Monte Carlo simulation were performed to analyze the effect on a pillar of memory cells. The test environment was simulated with a monochromatic Pb-208 33 TeV beam. A total of 1 million events were simulated. The result of the simulation show that memory cells subjected to Ultra High Energy Pb ions (>10 TeV) have a large contribution of deposited dose by secondary particles. For lower energy Pb ions (<500 MeV), memory cells closer to the source have less deposited dose, as memory cells further away are more susceptible to a fan-out effect which occurs when neighbouring pillars can scatter to lower layers of other pillars.
Another set of simulations were run to observe the radiation effects of a memory pillar in LEO, GEO and AEO for both proton and Pb-208 irradiation. For the space environment simulation, the particles are initiated with a SPENVIS[5] macro. The macro allows for random distribution of events and energies around the created geometry. Similar results were obtained for all three cases; protons have little im-

pact on the charge in the memory cells and the deposited dose compared to the Pb-208 simulations. A difference was found between the LEO and GEO and AEO simulations. The GEO and AEO simulation cases show a higher deposited dose on average than the LEO simulation.

Finally, a conceptual design is proposed as radiation monitor payload. A trade-off has been performed to select the FPGA and memory chip for data storage. The Virtex-4QV was chosen as space graded FPGA and the RTIMS space graded memory for data storage. A radiation tolerance voltage regulator is selected to provide the required 1.8 V for signals to and from the 3D NAND memory. The B17A chip is chosen as sensitive volume of the radiation monitor. The sized dimensions are 80mmx68mmx28mm and the weight is estimated to be 89.8 grams. The operating voltage of the radiation monitor is 3.3 V with a power consumption of 965 mW. The operating temperature is limited by the 3D NAND memory which has a operating temperature range of 0° Celsius and 70° Celsius.

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Lists of Abbreviations

Abbreviation	Description
AEO	Areosynchronous Equatorial Orbit
ALE	Address Latch Enable
BGA	Ball Grid Array
BiCS	Bit Cost Scaling
BLS	Bit Line Selector
CD	Critical Dimension
CERN	Conseil Européen pour la Recherche Nucléaire (European Organization for Nuclear Research)
CG	Control Gate
CLE	Command Latch Enable
CME	Coronal Mass Ejections
CMOS	Complementary Metal-Oxide-Semiconductor
COTS	Commercial Of The Shelf
CT	Charge Trap
CuA	CMOS under Array
ECC	Error Correcting Code
ESA	European Space Agency
FG	Floating Gate
FPGA	Field-Programmable Gate Array
FSM	Finite State Machine
GCR	Galactic Cosmic Rays
GEO	Geosynchronous Equatorial Orbit
LDO	Low-Dropout
LEO	Low Earth Orbit
LET	Linear Energy Transfer
LUN	Logical Unit
MCM	Multi-Chip Module
MEOP	Monolithic Even Odd rows of Pillars
MLC	Multi Level Cell

Abbreviation	Description
MRM	Miniature Radiation Monitor
NDA	Non Disclosure Agreement
ONFI	Open NAND Flash Interface
Pb	Lead
PCB	Printed Circuit Board
PE	Program-erase
QLC	Quad Level Cell
R/B#	Read/Busy
RE#	Read Enable
RREACT	Reliability and Radiation Effects on Advanced CMOS Technologies
RTIMS	Radiation Tolerant and Intelligent Memory Stack
SAA	South Atlantic Anomaly
SD	Standard Deviation
SEE	Single Event Effects
SEL	Single Event Latchup
SEU	Single Event Upset
SLC	Single Level Cell
SLS	Source Line Selector
SPENVIS	SPace ENVironment Information System
SSD	Solid State Drive
TID	Total Ionizing Dose
TLC	Triple Level Cell
UART	Universal Asynchronous Receiver Transmitter
VHDL	Very High Speed Integrated Circuit Hardware Description Language
V-NAND	Vertical-NAND
WD	Western Digital
WE#	Write Enable
YMTC	Yangtze Memory Technologies Co.

1
INTRODUCTION

To make spaceflight more affordable, engineers have turned to Commercial Of The Shelf (COTS) components and miniaturization to reduce costs. Micro-propulsion, attitude determination, control systems and space instruments have made the step toward miniaturization over the years. The aggressive down scaling of semiconductors in the past few years makes flash memory an interesting component for a space radiation monitor. This Chapter will provide background information on the NAND flash memory and space radiation. Furthermore, the research questions and objectives are discussed, as well as the scope of the thesis. Finally, the structure of this report is given in Section 1.5.

1.1. NAND FLASH MEMORY

There are two types of flash memories, NOR and NAND. NOR flash memory has faster read speed but is slower in writing and erasing than NAND.[6] The NAND flash memory will be the focus of this project. NAND flash memories are non-volatile memories, which retains the stored information even when they are not powered. This is achieved by using a floating gate transistor. The floating gate is separated from the control gate by dielectric material. For a Single Level Cell (SLC) the float gate can either have a negative charge or no charge. These two charge states allow for one bit per floating gate transistor. Multi Level Cells (MLC) use multiple charge states and allow multiple bits per floating gate. MLC has a smaller error margin as the charge states are closer to each other. The charge state can be read by applying a voltage to the transistor and measuring the current. Each logic level has a corresponding threshold voltage, i.e. the voltage which results in a current readout. [7]

NAND flash memory is used in a wide variety of products, such as computers, smartphones and USBs. This led to a decrease in price and size of the NAND memories. The architecture of the planar NAND memories shrank to the size that it reached its physical limits. This caused the introduction of 3D NAND memory. It follows the same principle of planar NAND memory, but differs in layout. In 3D NAND memory, the channels are stacked into a pillar which increases the bit density of the memory cell. [8]

Radiation effects the threshold voltage leading to bit errors. Ionizing particles can interact with the charge state of the transistor and lower its threshold voltage. This leads to faulty readouts by the system. This property of voltage threshold shifting shows potential use of the 3D NAND memory as radiation monitor. Extensive research has been done by RREACT research group on the radiation effects on flash memory.[1] [9] [10]

Recently, a prototype has been developed at Delft University of Technology, which is capable of reading the threshold voltages in a 3D NAND flash memory cell. This includes the required hardware and software. The prototype is used to read the threshold voltages in a radiation test. [2]

1.2. SPACE RADIATION

Space is known to be a hostile environment. Next to the absence of an atmosphere and widely varying temperatures, radiation is considered a show stopper for space exploration. Electronics that are exposed to radiation for an extended period of time can be permanently damaged. Different types of radiation cause different effects. In this Section the three main sources of radiation in space are discussed, together with the radiation effects on electronics.

1.2.1. Different sources of radiation

The first source of space radiation are trapped particles. Particles are accumulated and trapped in the magnetic field around a planet. This effect causes radiation belts. The best known radiation belts are the Van Allen belts around Earth. The Van Allen belts are split up into two toroidal belts. The inner belt ranges from 1000 km to 6000 km altitude and consists of high energy protons. The outer belt consists of high energy electrons and ranges from 13 000 km to 60 000 km altitude. The South Atlantic Anomaly is a special region where the Earth's magnetic field dips in intensity. This leads to the inner Van Allen belt coming as close as 200 km altitude. Low-Earth orbit spacecraft that travel through the SAA are exposed to increased flux of energetic particles.[11] Outside the Van Allen belts, other types of radiation are more prominent.

The second source of space radiation are solar particles. This type of radiation is caused by the Sun. Two phenomena that can cause solar particles are Coronal Mass Ejections and Solar Flares. During a Solar Flare, the Sun emits large amount of energy which can be seen as flashes on the Sun surface. The Coronal Mass Ejections are slower than the Solar Flares and release plasma and electromagnetic radiation into space. Since both of these events are connected to the Sun's activity, there has been attempts to predict these events. The Sun goes through an 11-year cycle, which consist of four years of low activity, known as solar minimum and seven years of high activity (solar maximum). During a solar minimum, the Sun experiences a CME every five days, while during a solar maximum, the Sun can have up to three CMEs per day. This variation in activity can be decisive for the launch window of a mission. The occurrence of a Solar Flare is harder to predict. Solar Flares cannot be predicted by studying the solar cycle but are studied by finding a relation between the intensity of a Solar Flare and the parameters of the shock and plasma. [12]

The third type of radiation in space are the Galactic Cosmic Rays. This type of radiation originates from outside the Solar System and are highly energetic particles. The Galactic Cosmic Rays are generally the most energetic types of radiation. The high energy of the particles allow them to penetrate and deposit dose to the material they encounter. These particles mainly consist of protons and alpha particles and are referred to as primary cosmic rays. These primary cosmic rays can interact with a atmosphere and decay into other particles. These are known as secondary cosmic rays. These secondary cosmic rays consist mostly of neutrons, with a smaller amount of muons, positrons and pions. A small portion of the GCR consist of heavy-ions (~ 1%) while the majority of the GCR is dominated by protons. GCR are most dominant during a Solar minimum of the 11-year cycle of the Sun. During a Solar maximum, the Sun's activity gives some protection against the GCR.[13]

1.2.2. Radiation effects on electronics

Radiation can cause three different effects on electronics: Total Ionizing Dose, Displacement Damage and Single Event Effects.
There are three particle groups, Electrons, Protons and Heavy-ions. Electrons have electronic interactions with electronics and impact the Total Ionizing Dose or in some cases can cause Displacement Damage. The electronic interactions affect the charge in the transistor.[14]

The Total Ionizing Dose is a long term effect that occurs after prolonged exposure to radiation. Total Ionizing Dose is caused by ionizing radiation that affect the oxide (insulating) layer. The ionizing radiation creates electrons and hole pairs in the oxide layer. The electrons have a higher potential energy and fall back to the gate. The holes however, remain in the oxide and accumulate at the silicon interface, which creates defects and charge traps.[15] This causes interference with the normal operation of the transistor and can cause failures over time. The effect on the silicon-oxide layer is shown in Figure 1.1. It should also be noted that the Total Ionizing dose effect increases with the electrical field applied in the transistor.[16]
Protons can also cause Total Ionizing Dose effects as well as displacement damage due to electronic interactions and nuclear interactions.
Displacement Damage is a cumulative effect similar to Total Ionizing Dose. The material can be permanently damage due to electronic interactions or nuclear interactions. The nuclear interaction takes place at the nucleus of the atom. This can only be achieved by protons as they are the only radiation particle

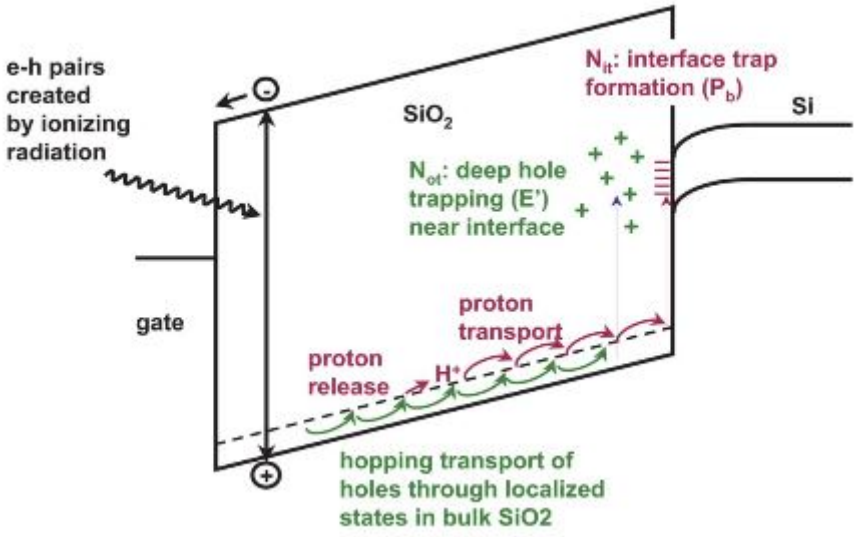


Figure 1.1: Total Ionizing Dose mechanism on oxides.[16]

that have enough energy to overcome the electrical bond between the electrons and the nucleus. The crystalline structure of the atoms can be changed due to radiation. This change has consequences for the properties of the material, for example, current paths can be created that were not present before the radiation exposure or making conduction more difficult. The longer a device is exposed to radiation the more apparent the effects become. [14]

Heavy-ions can cause displacement damage as well as Single Event Effects by depositing their energy. Single Event Effects is a collection for effects that occur due to a single particle. The most common effects are the single event upset and single event latchup. A single event upset describes the change of logic state for a digital circuit. The single event latchup has as consequence that the device switches to a high current state which has destructive results. [17]

1.3. Research question, aims and objectives

The research question, aim and objectives are presented in this Section. The main research objective is to contribute to the development of 3D NAND flash memory as radiation monitor by analyzing the effect of radiation on the threshold voltage in the memory cells. The goal of this research is to analyse the capabilities of the 3D NAND flash memory as radiation monitor.
The main research question is formulated as:

Can the space radiation environment be monitored by the changes in threshold voltage in a 3D NAND Flash memory?

The following sub-questions are raised to get an insight in what the capabilities of the radiation monitor will be:

- How can the radiation monitor distinguish different types of radiation?
- What are the effects of radiation on 3D NAND memory?
- What is the accuracy of the dose measured by the radiation monitor?
- How can the track of the radiation particle be visualized?

Several sub-objective are presented to support the main research objective:

- Identify type of radiation particle.

- Measure single event and cumulative effects in the memory chip.
- Determine the accuracy of a 3D NAND based radiation monitor.
- Reconstruct the particle track.

The first sub-objective is to understand the different types of radiation the 3D NAND memory can identify as radiation monitor. This defines what the radiation monitor is able to do and define its functionality. Next to determining the source of the radiation, monitoring the effects, single events and cumulative, are valuable to measure. Another sub-objective is to investigate the accuracy of the 3D NAND flash memory as radiation monitor. This is required to get an idea of the performance of the device. The final sub-objective is reconstructing the track of the radiation particle. Determining the track of the radiation particle gives more insight in the radiation environment.

1.4. Thesis scope

This thesis focuses on the data analysis of a 3D NAND memory chip tested at CERN.[3] The hardware and software used were developed at Delft University of Technology [2] and improvements have been made to increase the effectiveness of the read-out method. Simulations are performed for two different particles (protons and Pb-208) and a preliminary design is proposed.

1.5. Report structure

Chapter 2 gives an in-depth analysis of 3D NAND memory as a radiation monitor. This includes the transition from planar NAND devices to 3D NAND memory, the internal structure of a 3D NAND memory chip, a market analysis of the prominent 3D NAND manufacturers and a prototype radiation monitor based on 3D NAND. The read-out method for the test-setup was extended by implementing a binary search. The updated read operation can be found in Chapter 3, together with a verification of the read-out method. The data analysis of the results from a Ultra High Energy Pb ion beam radiation test performed at CERN is presented in Chapter 4. Monte Carlo simulations are shown in Chapter 5 and a preliminary design for the radiation monitor is proposed in Chapter 6. Finally, the conclusions and recommendations can be found in Chapter 7.

2

3D NAND MEMORY AS RADIATION MONITOR

This Chapter elaborates on the functionality of 3D NAND memory and transition from planar NAND devices to the 3D NAND memory. Furthermore, the vertical pillar structure which is a key feature of 3D NAND memory, is explained in this Chapter together with a proposed physical architecture. A market analysis is presented to better understand the trend of shrinking chips and predict the memory capacity in the coming years. This Chapter is concluded with a prototype developed at Delft University of Technology.

2.1. NAND MEMORY: FROM 2D TO 3D

The technological advancements on semiconductors over the past decade has led to the shrinking of flash memory chips. Manufacturers were able to produce planar flash memory devices with a feature size of less than 50 nm. The smaller feature size put a higher stress on the reliability of the chips. With the introduction of 3D NAND, the chips were able to continue the shrinking trend while maintaining the reliability. [18] The internal layout of the transistors in the NAND memory will be discussed in this Section, along with function and properties of the 3D NAND memory.

2.1.1. PLANAR NAND MEMORY ARCHITECTURE

The NAND flash memory can be based on the Charge Trap device or Floating Gate device. Both devices have a semiconducting Phosphorous-doped Silicon (P-Subtrate) layer as base which insulates a Source on one side and Drain on the other side. The Floating Gate devices have a Floating Gate on top of the P-Substrate layer which is separated by an insulating (Tunnel Oxide) layer. Another insulating (Interpoly Oxide) layer separates the Floating Gate from the Control Gate. The Floating Gate is used to store electrons. These electrons are trapped since both ends of the Floating Gate are insulated.[19] The amount of electrons stored in the Floating Gate is used to assign a bit value to the device. The Control Gate is used for reading and writing bits assigned to a device.
The Charge Trap device have a similar structure. In the Charge Trap devices, the Floating Gate layer is replaced by a Nitride Storage layer and the Interpoly Oxide layer is replaced by a Blocking Oxide layer. An overview of the Charge Trap and Floating Gate devices is given in Figure 2.1.

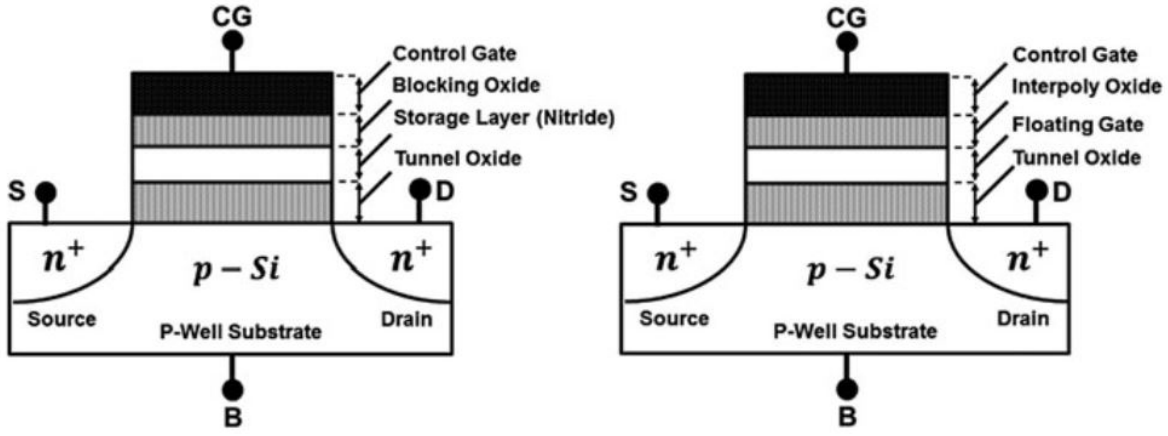


Figure 2.1: The architecture of a Charge Trap device (left) and a Floating Gate (right) device. [19]

The conventional NAND flash memories have strings of memory cells aligned in a line. 3D NAND flash memories have the floating gates stacked upon each other to create a vertical structure. This has as benefit that it reduces the used surface area. Figure 2.2 shows an overview of the internal structure of 3D NAND flash memory.

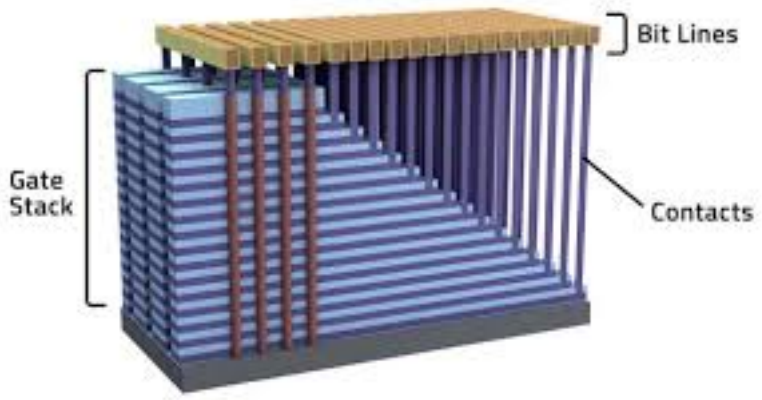


Figure 2.2: Schematic overview of internal 3D NAND memory architecture. [20]

The transistors are the cell level of the NAND flash memory. Multiple cells are connected in series to form strings. The Drain of one cell is the Source of the following cell, to ensure that the current is flowing in one direction. Selection transistors are placed at the Source and Drain end of the string. These transistors allows switching the string "on" or "off". By switching specific strings "on", memory cells can be selected. The Source end of the string is connected to the Source Line, which is shared with other strings. The Drain end of each string is connected with one another through the bitline. The control gate of each floating gate cell is connected to a wordline. Cells that have the same wordline produce a page, i.e. all the cells that are connected to wordline 0 form one page. A schematic overview of the line connections with the cells is given in Figure 2.3.
The block level is formed by a collection of pages and multiple blocks form a plane. A NAND flash memory can have one or two planes and are combined to form the top level of the NAND flash memory, known as die.

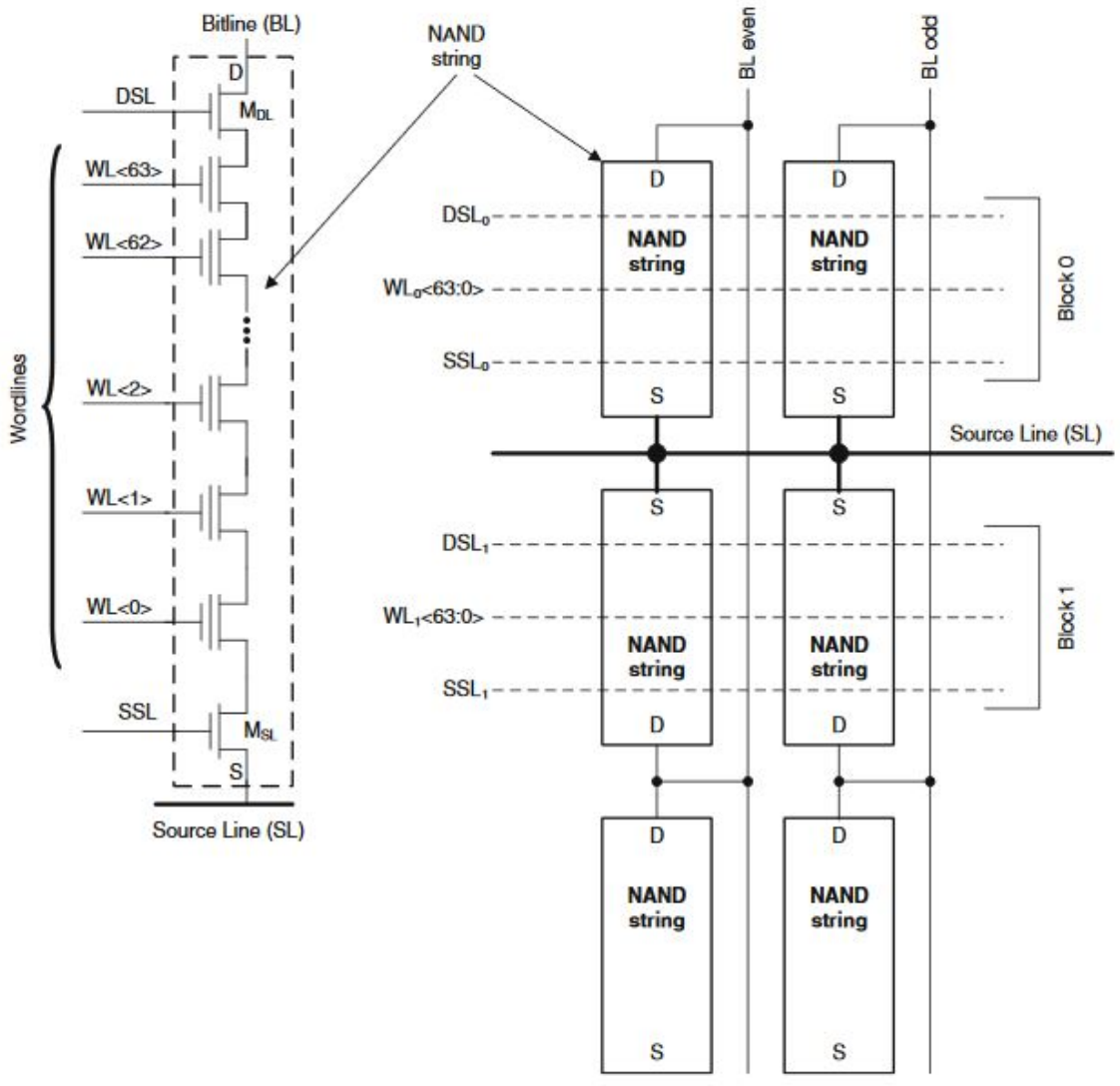


Figure 2.3: Layout of cells connected in series to from strings (left) and connection between strings within an array (right). [19]

2.1.2. Reading and writing NAND flash memory

In this subsection the read and write procedures for the Floating Gate devices are described. The Charge Trap devices follow the same principle, with the Nitride Storage layer fulfilling the same purpose as the Floating Gate layer.

The Floating Gate is separated from the control gate by a dielectric material, which allows the cell to store electrons in the Floating Gate layer. For a Single Level Cell (SLC) the float gate can either have a negative charge or no charge. These two charge states allow for one bit per floating gate transistor. Multi Level Cells (MLC) use two bits and allow four charge states per floating gate. Triple Levels Cells (TLC) and Quad Level Cells (QLC) use three and four bits and allows for eight and sixteen charge states, respectively. Every charge states corresponds to a logic level. Starting at L0 up to Ln with n being the number of charge states for a cell minus one. In Figure 2.4 the different distribution of logic levels for SLC, MLC, TLC and QLC are plotted against the threshold voltage. The threshold voltage is the minimum voltage that needs to be applied to the cell to make the P-Substrate conducting and cause a current readout between the Source and Drain of the cell.

The vertical lines in the graphs of Figure 2.4 represent the voltage that is applied to determine the charge state of the cell. For the SLC, there are two logic levels L0 which corresponds to a bit value of

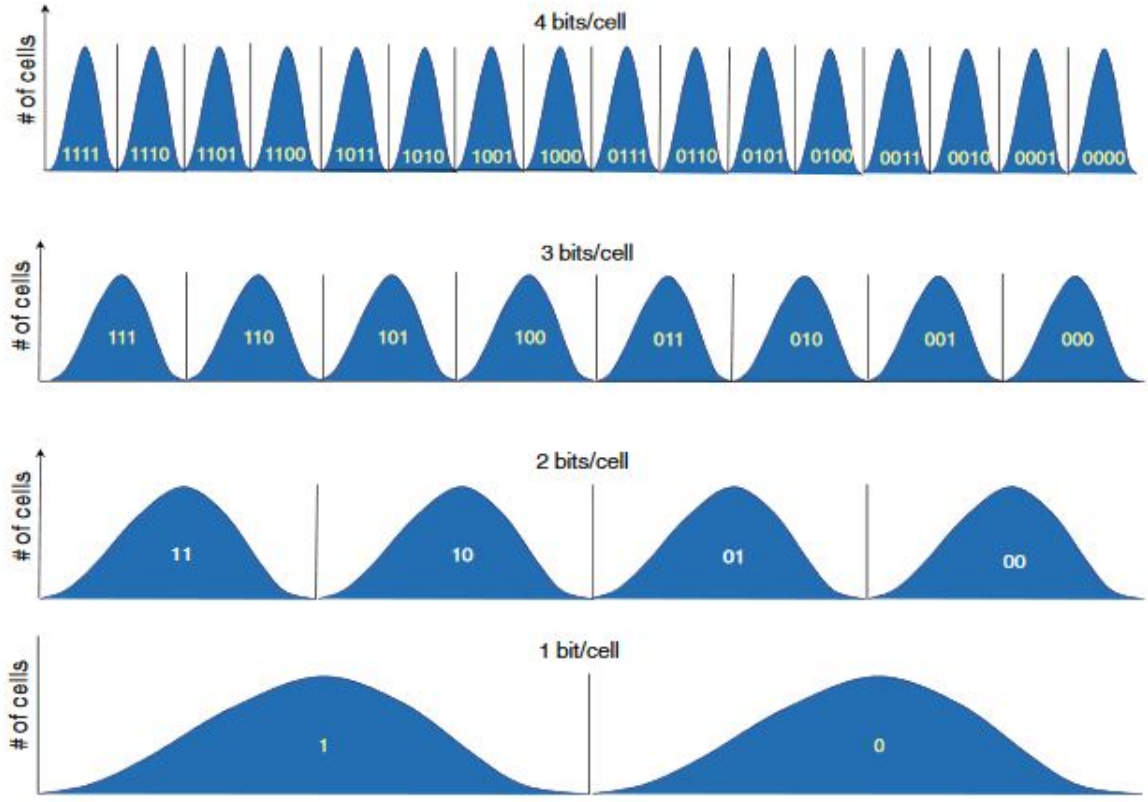


Figure 2.4: The distribution of logic levels for QLC, TLC, MLC and SLC (from top to bottom) [19]

"1" and L1 which corresponds to bit value of "0". An intermediate voltage is applied, represented by the vertical line. If there is no current measured, the cell has a bitvalue of "0", as a higher voltage is needed. If there is a current readout, the cell has a bitvalue of "1". Reading MLC, TLC and QLC bitvalues works similar but with multiple intermediate voltages to find the corresponding bitvalue of the cell. Each logic level has a corresponding threshold voltage, i.e. the voltage which results in a current readout. Memory cells which are programmed to the same logic level can have a different threshold voltage as the logic levels as normally distributed. Using multiple logic levels per cells allows for a higher storage density as more information can be stored per cell, but also lowers the margin of error of the cells since the charge states are closer to each other in terms of threshold voltages.[7]

Writing information onto a NAND memory cell, requires manipulation of the electrons in the Floating Gate. The Floating Gate is completely surrounded by insulating layers, to make sure that information is stored for a long time and keep the information even when the device is powered off.
Electrons are able to pass through the insulation layers by using quantum tunneling. By applying a high positive voltage to the control gate, the insulating oxide layer deforms and allow electrons to be transported from the Floating Gate to the Control Gate through the quantum tunneling effect. This effectively increases the charge of the Floating Gate. The opposite can be done to draw electrons from the Control Gate to the Floating gate. Applying a high negative voltage will draw electrons from the Control Gate to the Floating Gate. The voltages applied for writing are higher than the voltages used for reading, which over time damages the oxide layer and leads to a maximum write cycles.

2.1.3. Transition from planar to 3D NAND memory

The 3D NAND memory has been developed as a result of the planar NAND memory reaching its physical limitations to operate consistently. The linear orientation of the planar NAND memory is tilted 90 degrees to form pillars for the 3D NAND memory. These pillars are radially symmetric, as the pillars have different layers from the center to the edge of the pillar. In 3D NAND memory, Charge Trap devices are commonly used over Floating Gate devices. The 3D structure of both the Charge Trap and Floating Gate are presented in Figure 2.5.

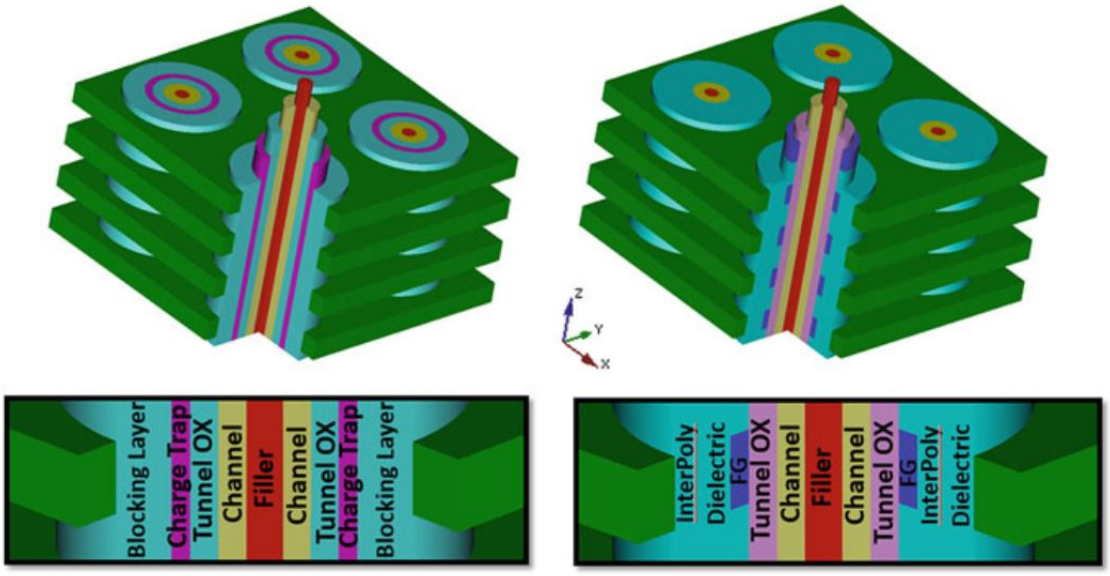


Figure 2.5: Schematic overview of Charge Trap (left) and Floating Gate (right) devices in 3D structure.[19]

Within the Charge Trap (CT) and Floating Gate (FG) categories, there are a number of variations with respect to the orientation, placement of the cells, Source Line Selector (SLS) and Bit Line Selector (BLS). One of such configurations that can be applied to both CT and FT is staggered pillars. Conventional pillars have cells in the XY plane spaced evenly in both X and Y direction. The staggered pillar approach shift a row of cells in the X direction while keeping the distance between the cells the same, which results in a reduction of Y distance between the cells. This effectively doubles the number of bit lines in the staggered pillars as opposed to the conventional pillar configuration. For this configuration, the BLS decoding is simplified, as the odd pillars can be connected to odd bit lines and even pillars to even bit lines. An odd bit line and even bit line can be paired by one BLS. This reduces the amount of BLS required by a factor of two, compared to the conventional pillar structure. The difference between conventional pillars and staggered pillars is shown in Figure 2.6.

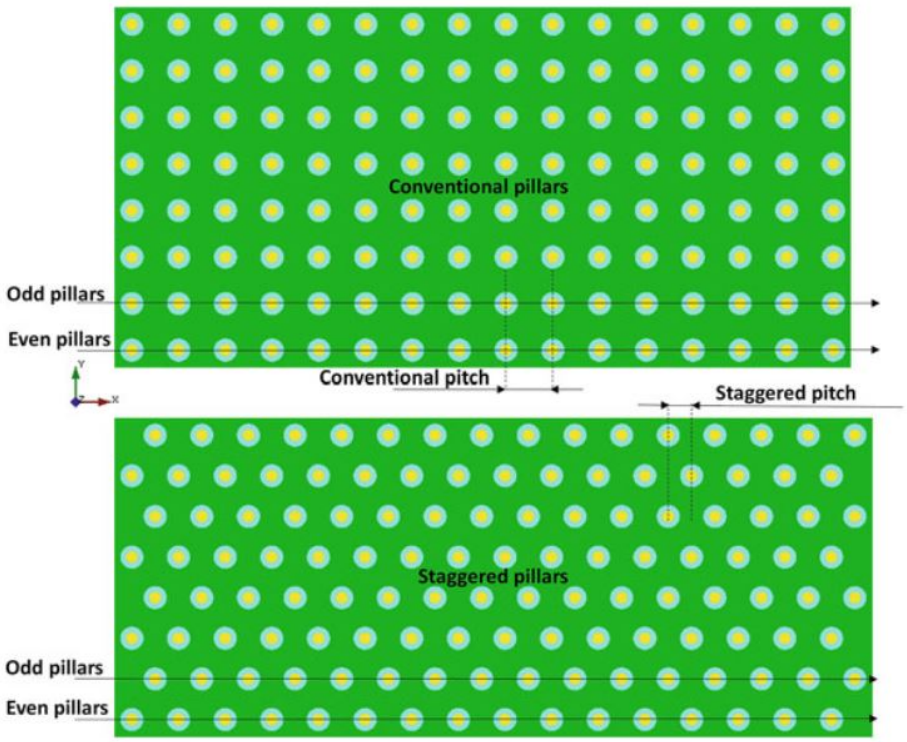


Figure 2.6: Conventional pillar structure vs staggered pillar structure. [19]

The staggered pillar structure can be further optimised for read and write operations by introducing Monolithic Even Odd rows of Pillars (MEOP). This architecture adds a slit between each pair of odd and even rows that connects to the source line. By introducing these silts, there are more contact point with the source line and thus simplifies the SLS decoding. The MEOP architecture is shown in Figure 2.7.

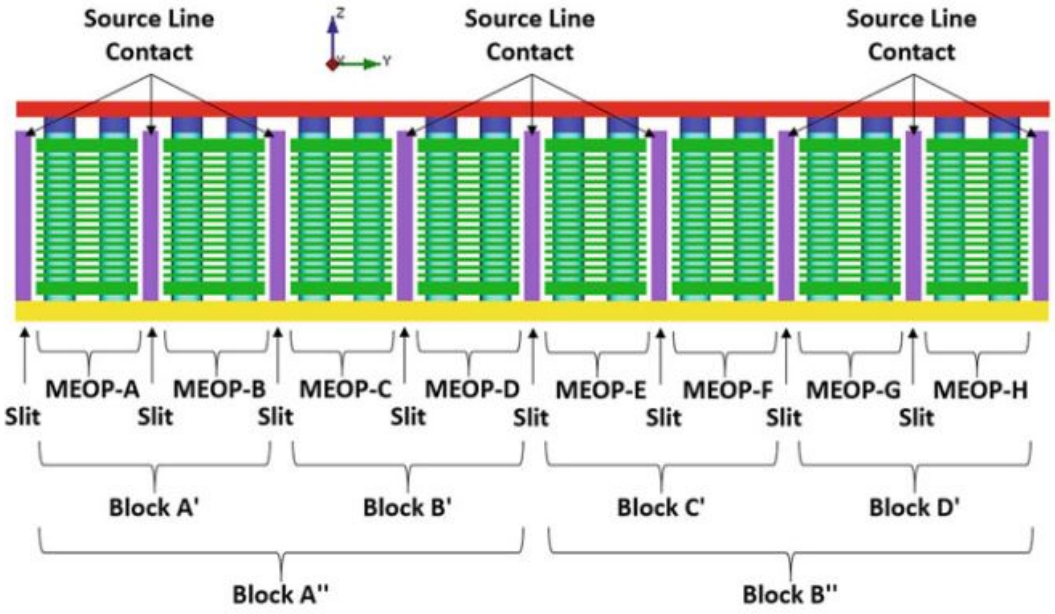


Figure 2.7: Placement of slits between the odd and even row pairs to create the MEOP structure. [19]

The most advanced version of 3D NAND memory architecture expands the MEOP structure by doubling the amount of bit lines. This is referred to as bit line staggering. Figure 2.8 shows the concept of staggered bit lines. In this architecture, two bit lines are arranged per column of pillars. Every pillar is then connected to one of the two staggered bit line contacts. The main advantage of this architecture is that this further increases the bit density of the memory block. Compared to the conventional pillar architecture, the staggered bit line architecture has a four times higher bit density.

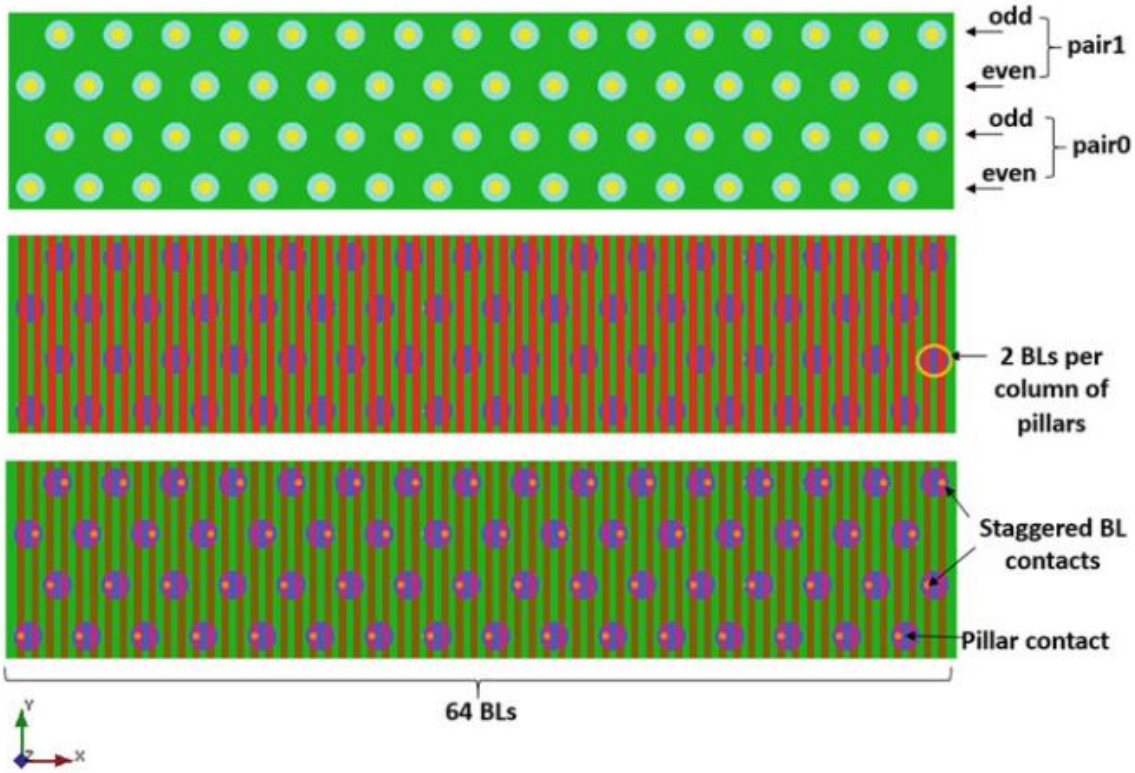


Figure 2.8: Overview of bit line staggered memory block.[19]

2.2. Market analysis

In this section, the current market of 3D NAND memory is discussed. 3D NAND memory is widely used in storage devices such as SSDs, smartphones and tablets. This causes a technology push, which drives the industry to make the chips smaller and faster with increasing storage capacity. Large companies such as Micron, Samsung , Toshiba and SK Hynix invest in the newest technologies with more layers and lower accessing times. A relative new player in the market is China. In 2018 the NAND flash market peaked at 57 billion dollars, with China accounting for 32%. The most prominent company from China to step into the NAND flash market is Yangtze Memory Technologies Co. (YMTC). [21] The 3D NAND flash market has seen a decline in demand in 2019. The industry is developing and producing the newest technologies while the demand for these new chips is lagging behind. [22] Experts in the field forecast an over supply of 3D NAND memory in 2020, thanks to the massive investments from the largest manufacturers. The price of 3D NAND chip are expected to decrease less for the coming years compared to the trend of the past decade. The slowdown of price reduction might lead to a stabilization of the chip price and over time show an increase in 3D NAND memory. If the manufacturers produce more chips than the market demands, there will be an overshoot in products. This will lead to a market loss and to reduce the market loss, the companies could increase the unit price of the chip. However, it remains a risk to increase the memory chip price, since it will give the other competitors an edge.[23] Another option for the manufacturers is to reduce the production of the 3D NAND chips. This will prevent oversupplying the market, but could increase the production cost of the chips. SK Hynix and Micron have already announced that they will reduce their wafer output to address the oversupply. [24]

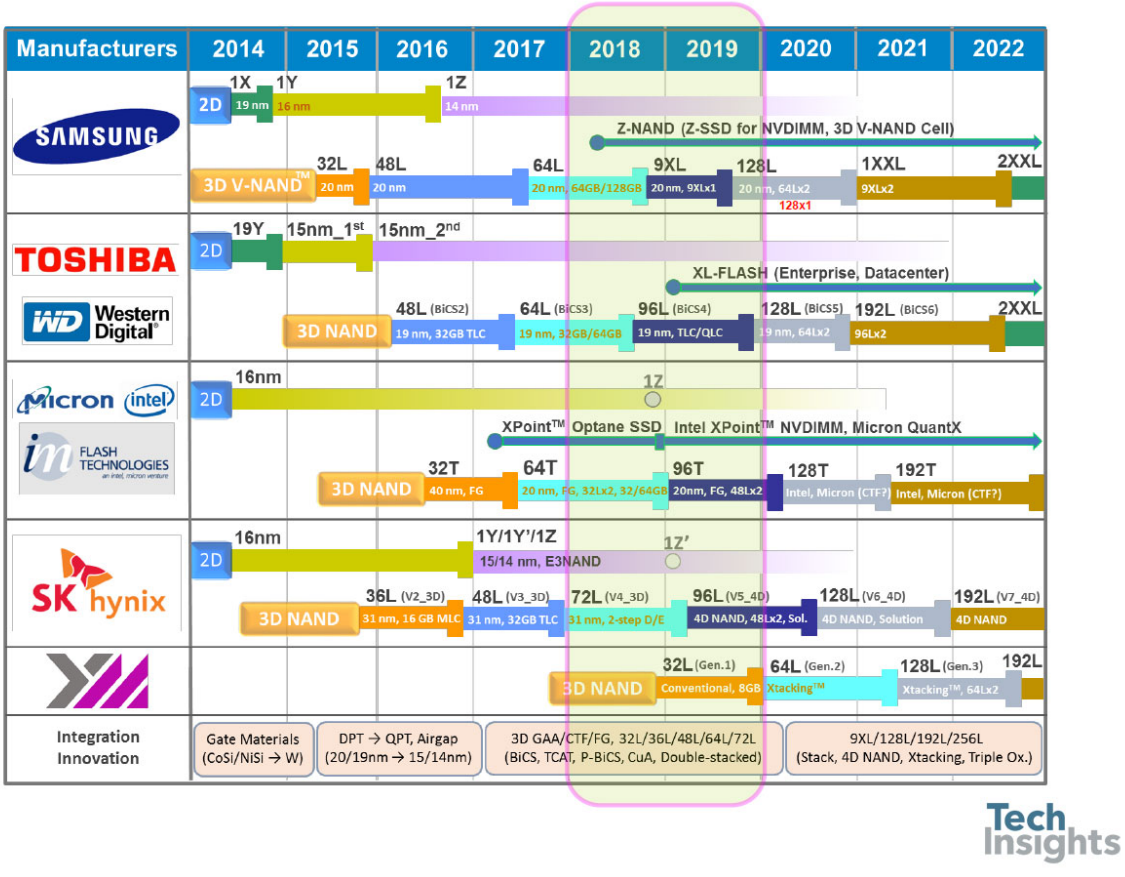


Figure 2.9: Technology development of NAND memory for different manufacturers. [25]

Figure 2.9 shows the technology development for the most relevant NAND memory manufacturers. [25] In recent years, the 3D NAND memory technology is taking over the planar NAND memory market. 3D NAND memory technology continues to grow rapidly with increasing layers. The increase in layers allows for a higher storage capacity per area, effectively reducing the cost per bit. The most recent

developments and available chips from the main manufacturers will be elaborated on in the following subsections.

2.2.1. SAMSUNG

The limitations of the planar NAND flash memory pushed Samsung to the development of 3D NAND flash memory. As early as 2003, Samsung started with a three-step development process to successfully introduce 3D NAND flash memory. The first step includes a material innovation. Charge Trap technology was chosen over Floating Gate technology, with a silicon nitride layer that temporary traps electrons. By adapting the material to a three-dimensional form, cylinders could be made from the silicon nitride. This led to the next step, which is a structural innovation. Samsung uses a Chanel Hole Technology, which connects the memory cells to each other vertically. The holes are created by an etching process. Etching introduces several production challenges which will be addressed later. The final step of the Samsung's 3D Flash NAND memory development process, is the integration innovation. This step entails the seamlessly integration of the modified memory cells with the cylindrical structure and the vertical etched holes. [26] Samsung brands their 3D NAND memory as V-NAND (Vertical-NAND) memory. Figure 2.10 shows the development process of the V-NAND technology.

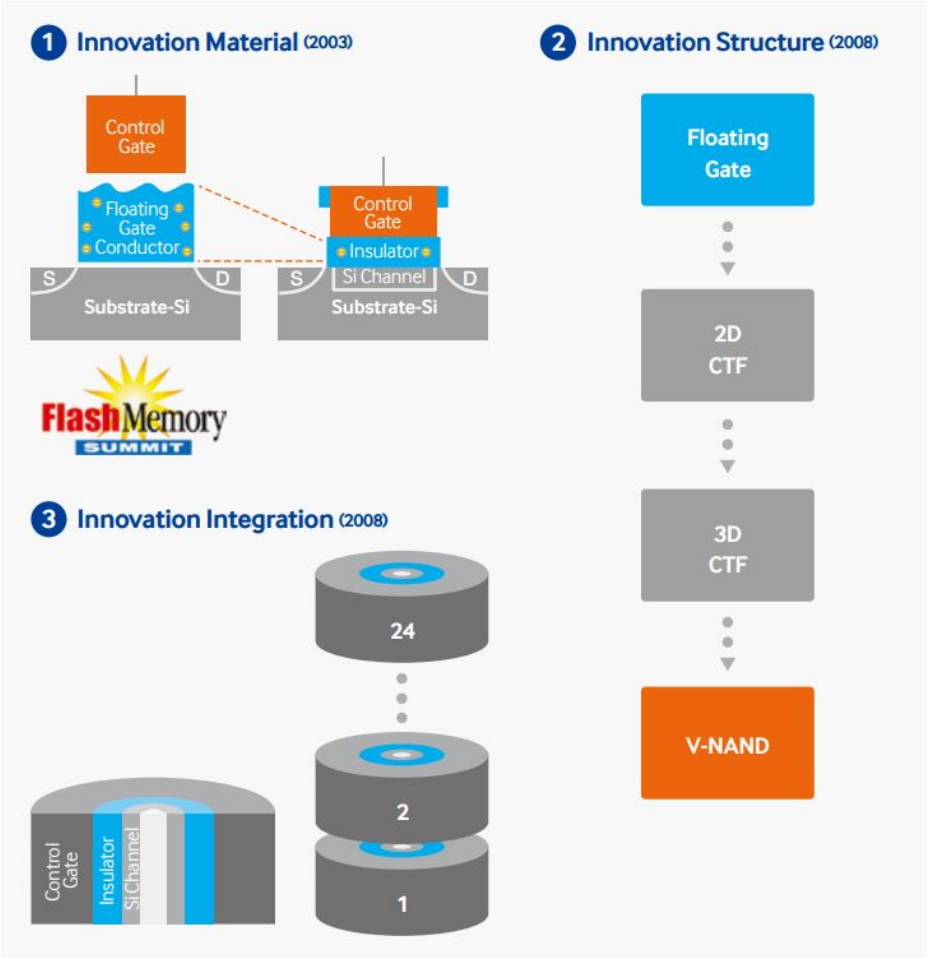


Figure 2.10: Three-step development process of V-NAND.[26]

The development of V-NAND took roughly ten years and let to the first commercial V-NAND product in 2013, which featured 24 layers and used MLC technology. In August 2019, Samsung announced the sixth generation V-NAND with 136 layers and TLC technology. [27] A single die can hold 512 Gbits of data and the chip has a read latency of 45 μs and a write latency of 450 μs.[28] Although the sixth generation chips have been announced, they are not yet available on the market. Samsung's

fifth generation V-NAND memory chip came commercially available in January 2019. The 970 EVO Plus SSD featured the chip in 250GB, 500GB, 1TB and 2TB. The chip contained a 9x-layer structure (ranges from 90 to 99 layers, depending on storage capacity) and 3-bit (TLC) storage.[29] Samsung's roadmap aims to release a new V-NAND generation every year. The V7 generation is projected to release with 200+ layer technology in September 2020. V8, V9 and V10 will debut in 2021, 2022 and 2023 respectively. The V10 generation will have a promising 500+ layer architecture. This is at least a year ahead of the competition, as SK Hynix aims to release 5xx technology chips in 2025. [28]

2.2.2. Toshiba and WD

Toshiba and Western Digital have worked together on 3D NAND memory chip and heavily invested in the developing memory chips based on the BiCS structure (see Chapter 2.4). Similar to Samsung, the chips rely on the charge trap technology rather than the floating gate technology. In May 2019, Toshiba presented their newest 128-layer BiCS-5 chip. The die uses CuA (circuitury under array) which means that all the logic circuitry is placed in a layer under the actual memory array. An example of BiCS structure is given in Figure 2.11.

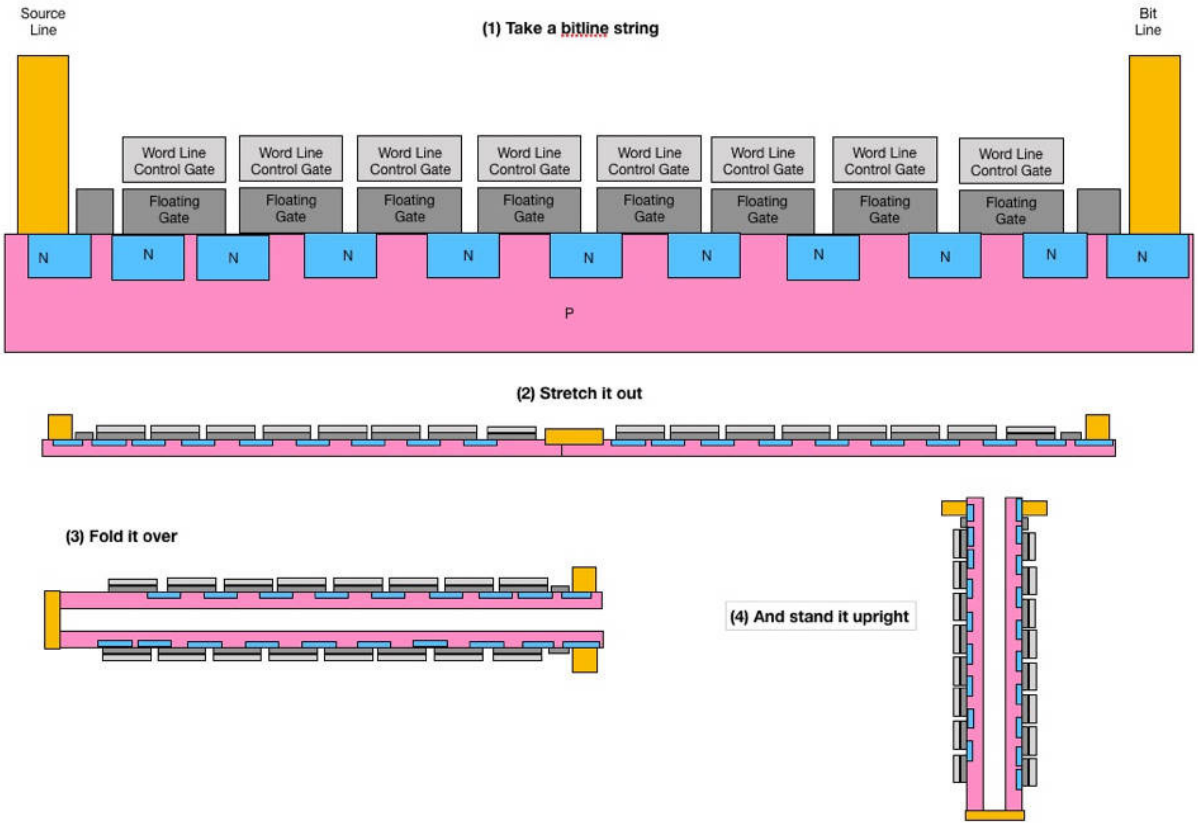


Figure 2.11: Example of planar to BiCS structure. (Note: Toshiba uses charge trap devices as apposed to floating gates as shown in the figure.) [30]

The latest commercially available chip from Toshiba and WD is the BG4 chip. It comes in a 128 GB, 256GB 512GB and 1TB version, which all use the TLC technology for storage.
According to the roadmap of WD, the BICS-5 chips will debut in 2020, featuring 128 layers. To create the BICS-5 chip, WD has two options. Either adding 32 layers to the existing 96 layered BICS-4 die or stacking two 64 layered dies together using a method called string-stacking. String stacking connects the strings from one die to the die on top of it. [31]

2.2.3. SK Hynix

SK Hynix is a semiconductor manufacturer based in South-Korea with a promising roadmap for 3D NAND techonologies. At the Flash Memory Summit in August 2019, SK Hynix announced that they will bring 128 layered dies in 2019, 176 layered dies in 2020 and 800+ layered dies in 2030. [31] This shows a huge increase in memory capacity for the coming ten years. SK Hynix have not released any details yet on how they will achieve this. However, looking at the current generation of their 3D NAND memory chips, it can be seen that SK Hynix uses a folded structure similar to Toshiba and WD. Figure 2.12 shows the internal structure of a 72-layer chip from SK Hynix.

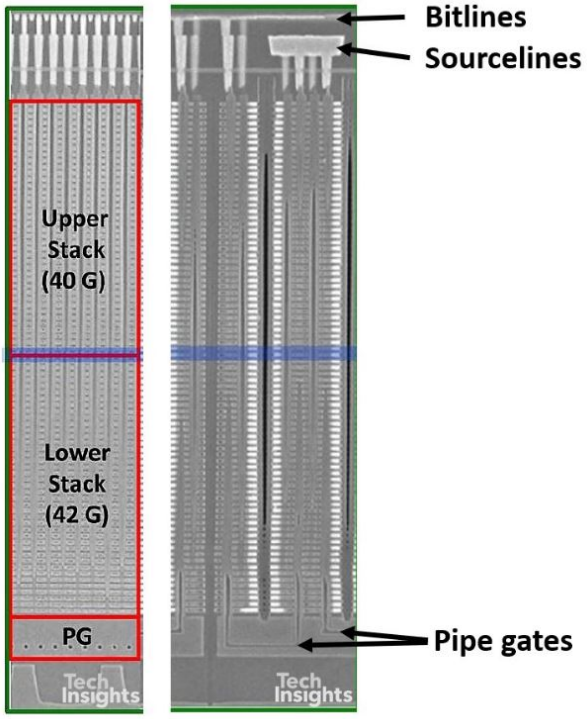


Figure 2.12: Overview of internal 72-layer SK Hynix chip structure.[25]

The die consists of two stacks, one 40 layer stack and one 42 layer stack, making the die a total of 82-layers. The highlighted blue area shows the lower layer of the upper stack and the upper layer of the lower stack. The 82 layer die has 72- active wordlines. The unused 10 wordlines are used as dummies and/or unusable due to manufacturing processes. On the bottom of the die, pipe gates can be identified. These pipegates, connect neighbouring channels with each other effectively creating longer wordlines. The chips from SK Hynix undergo a two step etching process, in which holes needs to made in two steps to achieve the desired result. The two-stage etching process contained the following sequence [25]:

- Pipe gate mold formation
- Channel etching (lower stack)
- Sacrificial layer filling into holes
- Mold formation (upper stack)
- Channel etching (upper stack)
- Sacrificial layer removal
- Channel formation

2.2.4. MICRON

Micron differs from the other manufacturer, as they use the Floating Gate technology as opposed to the charge trap technology the other companies are using. Although Micron uses a different approach to store the charge in the memory cells, they have shown to be able to keep up with their competitors when it comes down to expanding the number of layers in a die. In June 2019, Micron has announced that they will introduce 96-layer TLC dies and even has plans to introduce dies with QLC. QLC tend to be less popular than TLC since they currently have a lower endurance than TLC. In QLC, the read offset voltages are closer to each other which requires more precise read operations than TLC. Figure 2.13 shows the benefits of QLC as opposed to older generation technologies.

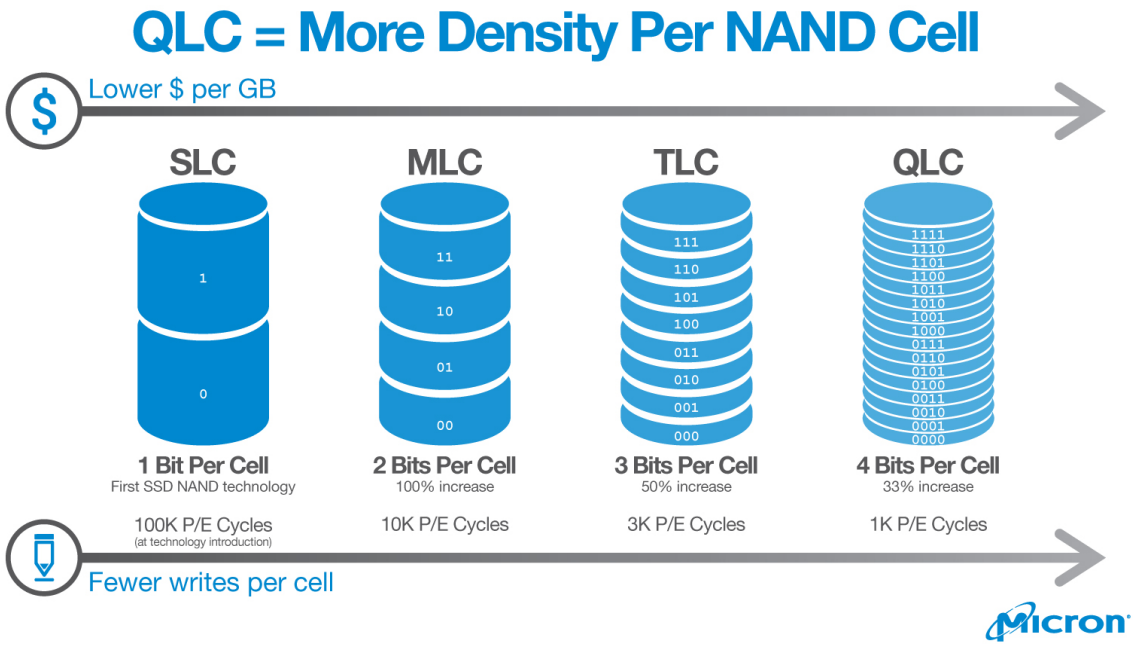


Figure 2.13: Micron's QLC technology leads to reduction of cell size and cost per bit.[32]

By introducing an advanced ECC mechanism, the number of PE cycles can be extended, increasing the endurance of the device. [33] In August 2019, Micron has opened its third facility in Singapore, which will focus on the production of the 96-layer chips. This is the third generation of 3D NAND memory chip from Micron and the last generation in which Intel will collaborate. After the 96-layers, Micron announced that they will use the charge trap technology for their devices, following their competitors. [34]

2.2.5. YMTC

YMTC is relatively new to the 3D NAND market compared to its competitors. Yangtze Memory Technologies Co. was established in July 2019 and based in China. YMTC focuses on the demands of the Chinese market. As of 2019, YMTC is slowly decreasing their production of 32-layer chips and ramping up their production of 64-layer chips. An interesting move by YMTC is to skip the intermediate step of 96-layers and proceeds to develop 128-chips, which are scheduled to go into production in 2020. [35] Another interesting feat that YMTC introduces is their Xtacking technology, in which the CMOS is placed on top of the memory cell array (on the upper part of the staircase structure), instead of underneath. This is the opposite of what Micron's CuA (CMOS under Array), in which the control logic is placed underneath the array.

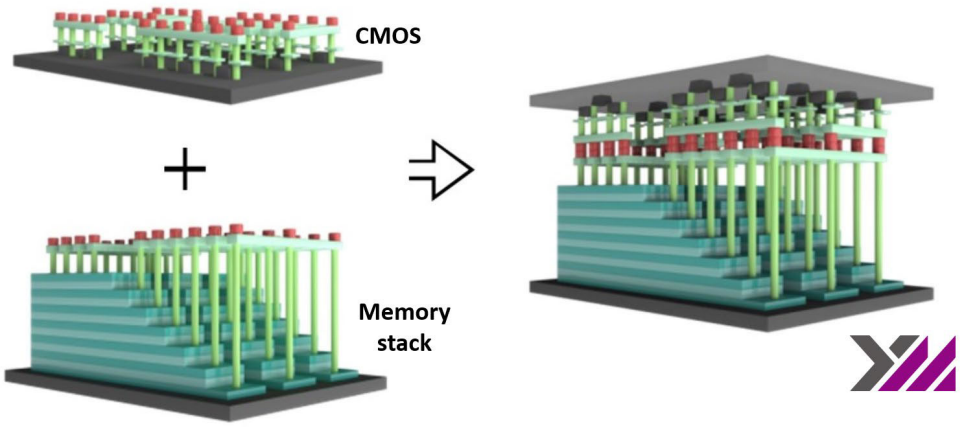


Figure 2.14: Xtacking technology from YMTC, placing the CMOS on top of the memory cell array.[25]

2.3. Scaling limitations

The trend of cramping more layers into a die will continue in the coming decade. One of the major scaling limitations are the manufacturing process. Since the memory cells are getting smaller and closer to each other, the tolerances are getting tighter. Small impurities or deviations can cause faulty chips. Figure 2.15 shows possible types of deviations occurring during the manufacturing process.

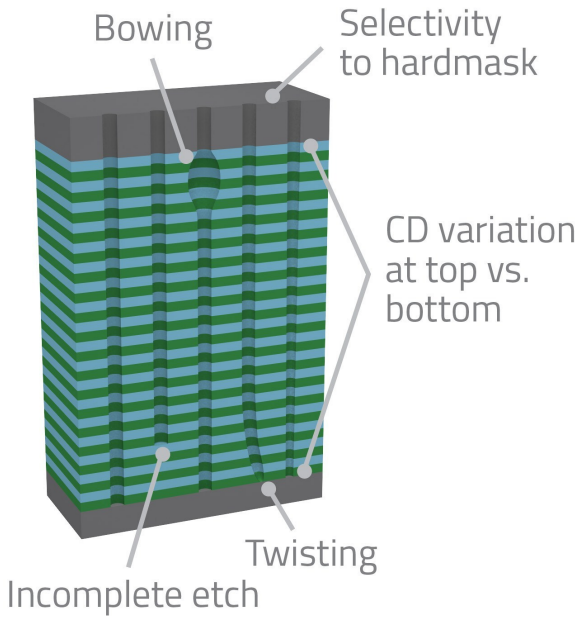


Figure 2.15: Example of impurities and deviations in 3D NAND manufacturing process.[36]

Bowing is an effect that results in the etched hole widening the material, not only effecting the bowed cell, but also neighbouring memory cells. An incomplete etch results in the bitlines not reaching the bottom of the array and therefore causes a failure of a whole column of memory cells. Twisting is an undesired property during manufacturing with curves in the etched holes as result. The critical dimension (CD) refers to the feature width of the memory cells. A CD variation can be created during production, creating unevenly sized memory cells.

Another challenge that the manufacturers face when expanding the amount of layers within a die is the staircase structure within. As the number of layers grow, so does the amount of steps of the staircase. This leads to an increase in size of the required area in the xy-plane.

2.4. 3D NAND MEMORY ARCHITECTURE AND STRUCTURE

The 3D NAND memory structure is represented by a logical architecture and physical architecture. The logical architecture is what is presented to the user. This allows the user to specifically address memory cells within the Logical Unit (LUN) array. The physical architecture of the 3D NAND memory is an intellectual property of the manufacturer and can only be obtained by making assumptions and closely analyzing the datasheets. [37]

2.4.1. LOGICAL MEMORY

Read and write operations on the 3D NAND memory can be performed by given command sequences. These sequences are 6 cycles long, with each cycle containing one byte. The six cycles together contain specific instructions for the memory. These bytes are processed by the control logic, which is not part of the physical memory die. The control logic sends the instructions to the I/O controller, which interacts with the LUN array. A functional block diagram of the memory operation is shown in Figure 2.16.

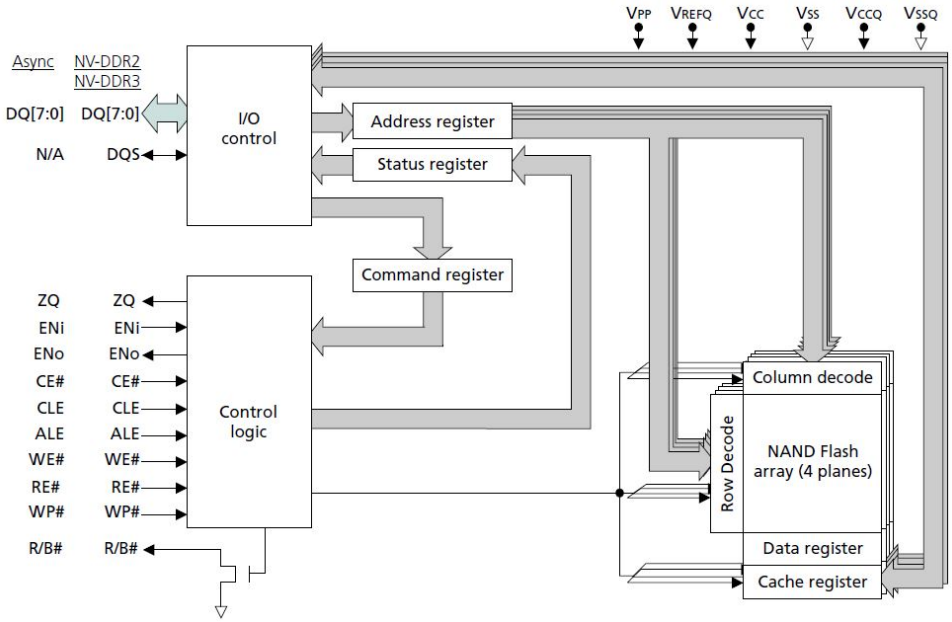


Figure 2.16: Functional Block Diagram of NAND memory operation.[37]

The Asynchronous and NV-DDR2 and NV-DDR3 operations take slightly different commands. In general, DDR2 and DDR3 operations are faster than the Asynchronous operations.
A physical memory die can have up to four Logical Unit, depending on the model. A LUN consists of pages, blocks and planes. The smallest addressable unit in a LUN is a page. The page can be seen as a row in the LUN array. One page contains 18 592 bytes. For NAND memory in TLC configuration, 2208 pages form one block. A total of 504 blocks are stacked per plane. Finally, one LUN contains four planes, or 2016 blocks.
The array organization per LUN is shown in Figure 2.17.
A memory controller can access memory cells by addressing the LUN, block, page and finally the column. Each column addresses one byte thus returns eight bits of data.

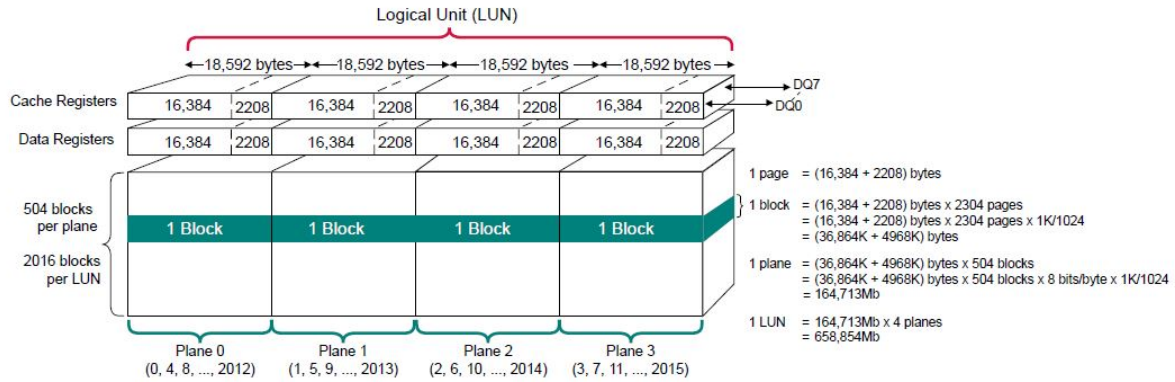


Figure 2.17: Logical Unit for TLC operations.[37]

Shared Pages

Shared pages play a key role in the organization of the logical memory. For memory cells that are programmed in TLC, each memory cell holds three bit values. With three bits, the memory cells can be programmed to eight different logic levels (L0-L7). For the Micron B17A, the logic levels are obtained by programming the memory cells to different logic levels and reading the pages with a threshold voltage offset. Figure 2.18 shows the bit values that correspond to the logic levels for the Micron B17A memory chip.

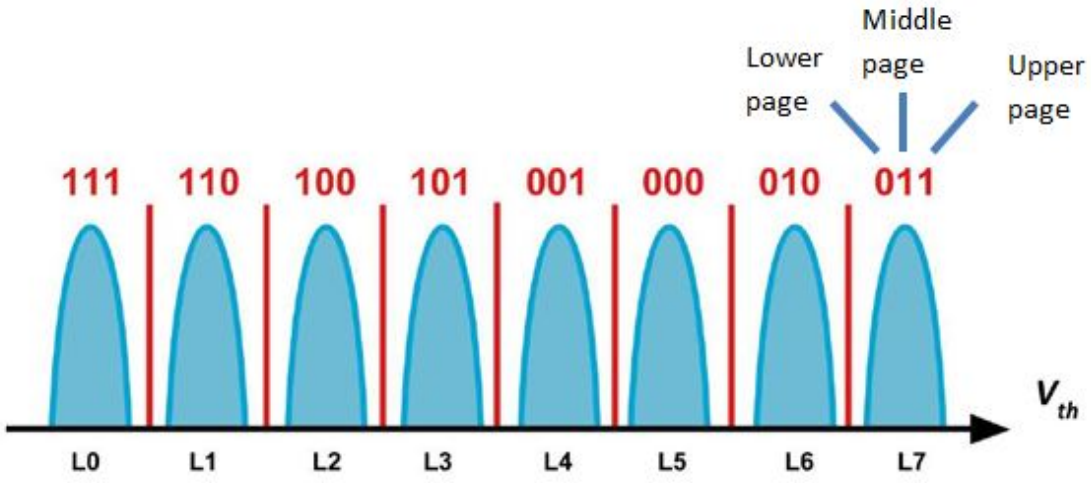


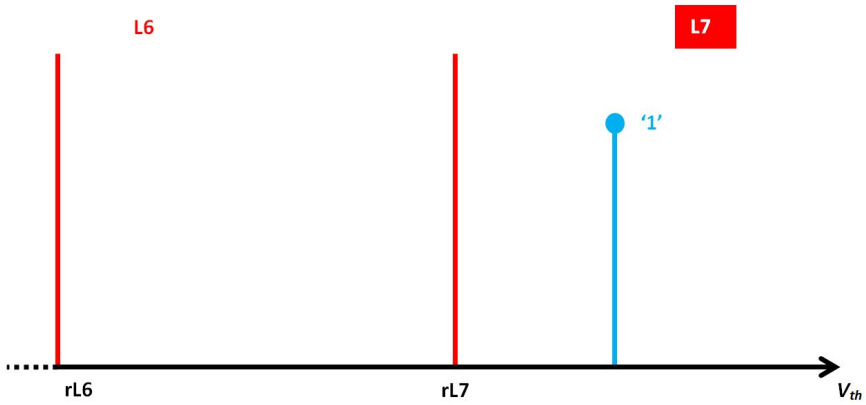
Figure 2.18: Schematic overview of logic levels and corresponding bit values for Micron B17A chip.[2]

A page in the logical memory is split into three for TLC operations. The first bit of each memory cell is stored in the lower page and is shared among all the memory cells of a page. The middle page contains the second bit values of the memory cells and the upper page contains the last bit of each memory cell.

Bit value of a memory cell

The bit value of a memory cell ('0' or '1') is determined by the threshold voltage stored in the memory cell. If the threshold voltage of the memory cell is lower than the read offset voltage, the logical memory will be read with a bit value of '0'. If the threshold voltage is higher than the read offset voltage, the bit value will be read as '1' by the memory. An example of reading a memory cell located at the upper page at read offset rL7 is depicted in Figure 2.19. The vertical red lines represent the read offset levels and the boundaries between the logic levels. The vertical blue line indicates the threshold voltage (V_{th}) of a memory cell. Figure 2.19a shows the case where the threshold voltage of the memory cell is lower than the read offset voltage. This results in a bit value of '0' when the memory cell is read.
Another case is shown in Figure 2.19b. The threshold voltage of the memory cell is higher than the read offset voltage. The memory cell is identified as logic level L7 and therefore read as '1'.

(a) Threshold voltage of the memory cell is lower than the read offset voltage rL7. The memory cell is therefore located in logic level L6 and read as '0'.



(b) Threshold voltage of the memory cell is higher than the read offset voltage rL7. The memory cell is therefore located in logic level L7 and read as '1'.

Figure 2.19: Bit value of a memory cells is determined by the threshold voltage relative to the read offset voltage.[2]

When programming a memory cell, the memory cell will have a threshold voltage which is higher than the corresponding read offset voltage. The exact threshold voltage however, is not assigned, but follows a normal distribution. Figure 2.20 shows data from a memory cell before radiation exposure and a Gaussian fit with a mean of 291mV and variance 91.7mV^2. [2]

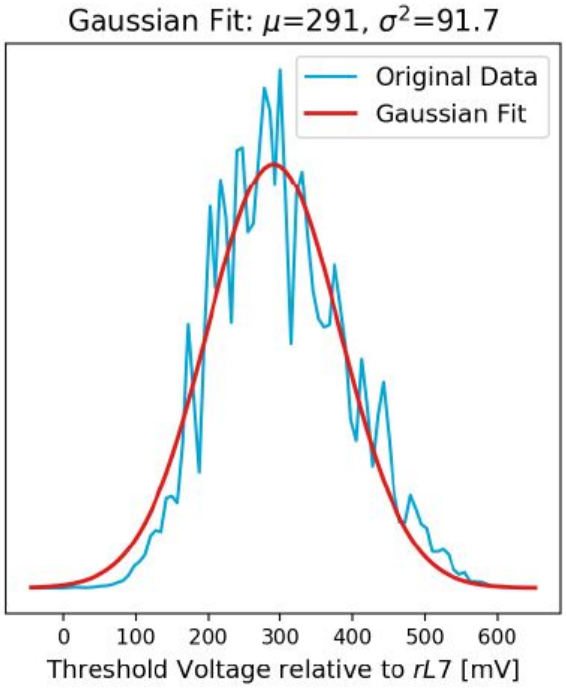


Figure 2.20: Gaussian threshold voltage distribution for cells programmed to L7.[2]

2.4.2. PHYSICAL MEMORY

Memory cells are physically stacked upon each other to create pillars. The height of a pillar is limited to the number of layers (Z-direction). Pillars are put next to each other to form rows (Y-direction) and columns (X-direction). A single memory block contains 110 659 584 memory cells in total. The column of a block is 37 184 memory cells long and 48 memory cells form a row of a block. The B17A die is a 64 layer chip, however, the upper layer and lower layer are not used in TLC mode. These layers are reserved for Error Correction Code (ECC), which results in effectively 62 layers of memory that can be used.

The memory block is 62 memory cells in height, 48 memory cells in width and 37 184 memory cells in length. [2] A coordinate system is introduced with the length as column direction (x), width as row direction (y) and the layer direction (z) corresponds to the height. Figure 2.21 illustrates the memory block orientation with coordinates.

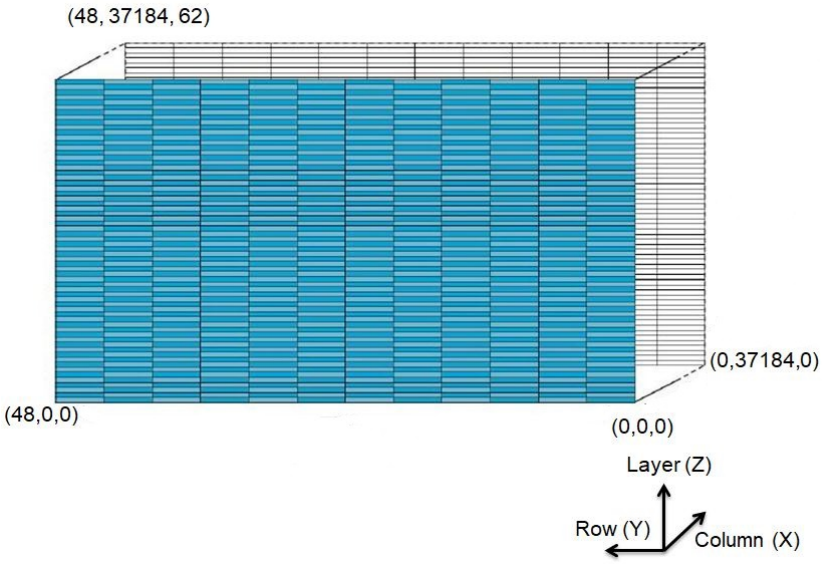


Figure 2.21: Physical block memory with coordinate system.

The exact mapping of the logical pages within a logical block to the physical pages in a physical block is not available in the datasheet provided by Micron.
The data read from the memory chip is obtained from the logical pages and presented to the user per byte. A single byte of the memory page holds the data of eight memory cells, which are assumed to be next to each other. It is assumed that one logical block is translated into one physical memory block. A 3D NAND memory block consist of long strings of memory cells which form a page. The memory pages are placed next to each other to create a layer. The layers of memory pages are then stacked upon each other to create the memory block. The following mapping method is used to make sure that all the memory cells in a logical block fit into a physical memory block:

- Every logical page of 148 736 memory cells is stretched over a row.
- Once a row of 37 184 memory cells have been filled, the adjacent row is filled. For one logical page, four rows are filled.
- After one logical page, the next logical page fills the next four rows.
- When 12 logical pages have filled all the 48 rows, the next logical page will fill the layer above.
- The mapping scheme continues until the complete memory block is filled.

Figure 2.22 shows the memory cell allocation for every memory cell in a logical page to the physical location in a layer.

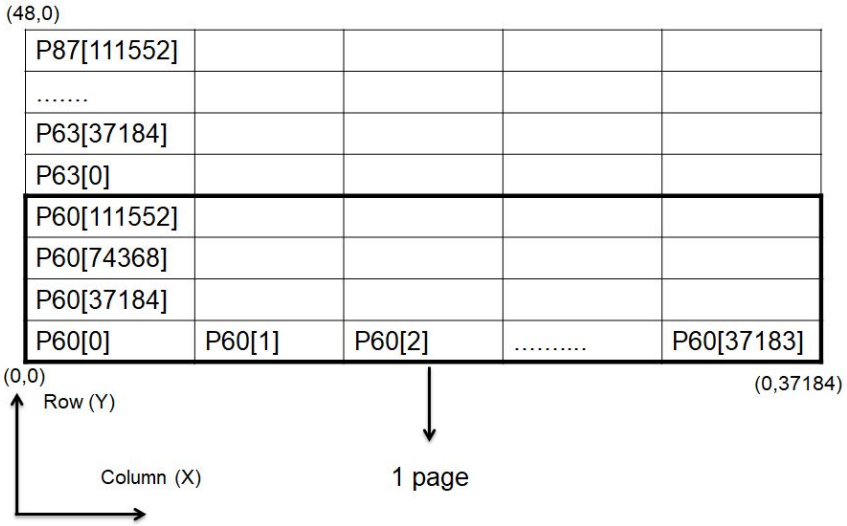


Figure 2.22: Memory cell allocation from logical page to physical page.

The pages are denoted with a 'P' and the memory cells are numbered in square brackets. The physical pages are split into three for the logical pages. The memory cell that is located at P60[0] also holds the information of P61[0] and P62[0], which are stored in the lower and middle page P61 and P62. The next upper page according to the Micron datasheet is P63.
An overview of the complete memory block is given in Figure 2.23.

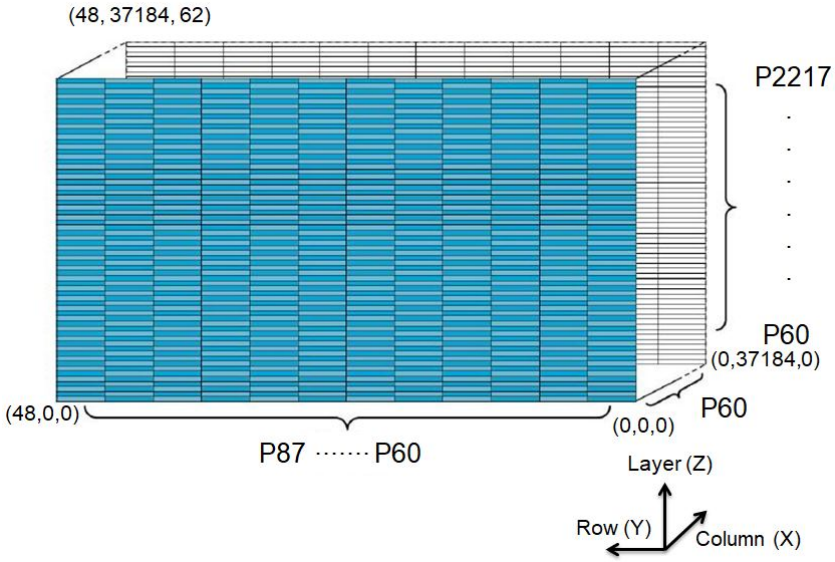


Figure 2.23: Overview of mapped logical pages to the physical memory block.

2.5. Radiation monitor prototype

In this Section the hardware and software that accompanies the 3D NAND memory to function as a space radiation monitor is presented. The prototype has been developed at Delft University of Technology and further improved on by implementing a binary search.

2.5.1. Hardware: ZedBoard

The Zynq-7000 FPGA is programmed to functions as a memory controller. A custom PCB is required to connect the 3D rawNAND memory to the ZedBoard. [2] Communication with an external computer for post-processing is established by using a Pmod module. A LogicAnalyzer can be connected to verify and check the signals from the 3D NAND memory chip. The LogicAnalyzer is further elaborated on in Chapter 3.5.

ZedBoard

The ZedBoard is a FPGA development board which allows users to create unique and powerful designs. The variety of interfaces and functions makes the ZedBoard a suitable candidate for the development of a memory controller. An overview of the functional block diagram of the ZedBoard is given in Figure 2.24. From the many interfaces that are highlighted, the Pmod connections are primarily used. A total of 32 Pmod connections are available on the ZedBoard as Programmable Logic. Four of the Pmod pins are used for the UART Pmod which establishes a connection with the external computer. Furthermore, 16 of the 32 Pmod pins are used to communicate with the rawNAND memory chip though the custom PCB. Eight of these channels allow input and output signals between the FPGA and the rawNAND memory. Input from the FPGA to the memory chip include commands and target addresses, while output from the memory chip to the FPGA contains data. These data signals are denoted as DQ(0-7). With DQ0 being the least significant bit and DQ7 representing the most significant bit.[38]

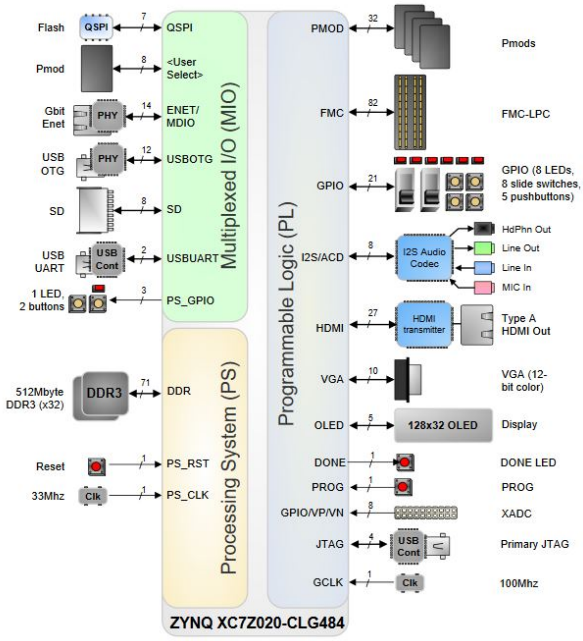


Figure 2.24: Functional block diagram of the ZedBoard development board.[38]

Custom PCB

The custom PCB houses a BGA-152 socket which is also capable of housing rawNAND memory with a BGA-132 configuration. The 3D NAND memory can easily be removed thanks to the clamp design of the socket.

A voltage of 1.8 V is provided to the 3D rawNAND memory, while the signals received from and sent to the ZedBoard have an operating voltage of 3.3 V. The PCB accounts for this voltage difference with linear voltage regulators. The memory in the socket is protected from overvoltage by a Zener diode.

Furthermore, the PCB includes test points which can be probed to test and verify signals during operations.

The 3D rawNAND attached on the PCB takes commands from the memory controller in hexadecimals. The operations of the row and column decoder are not accessible as it is intellectual property of the manufacturer. Hence, the operations that are performed inside the 3D rawNAND memory cannot be changed.

A number of tweaks have been made for an updated version of the custom PCB. First of all, ground pins were added for the LogicAnalyzer. Although, only one ground connection from the LogicAnalyzer to the ground of the board is required, the cables that come with the LogicAnalyzer have a ground wire for every signal wire. To make the wiring more neat while probing the 3D NAND memory chip signals, the ground pins for the LogicAnalyzer were added next to the signal pins. This leads to a change from a 4x1 pin header to a 4x2 pin header. One of the 3.3 V LEDs was replaced by a 1.8 V LED. Another change that has been made is driving the unused lines from the voltage converter to the ground with a 10k Ohm in between. It is not specified in the datasheet from Texas Instruments that this is required for unused pins [39], however, the PCB made by van de Poel experienced unusual behaviour and unstable readouts when the signals were not driven to the ground. This led to a post-production fix, which required external wires that connect to the ground pins of the board. Finally, the lines of the PCB are drawn slightly wider to ensure a stable connection and reduce losses. The updated design is shows in Figure 2.25.

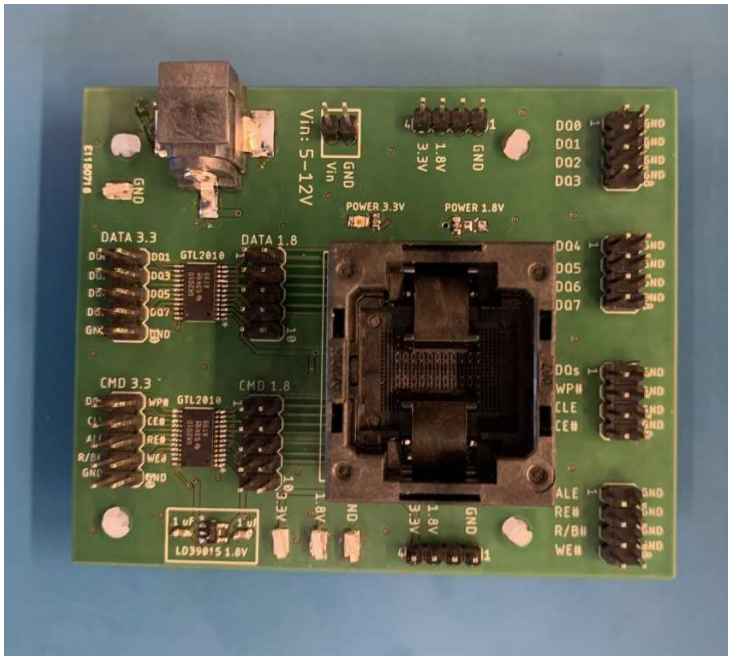


Figure 2.25: The updated design of the PCB.

UART Pmod

The UART Pmod module is an extension of the ZedBoard and transfers the output signals from the ZedBoard to an external computer. The UART Pmod module is used to make the integration with Python scripts easier. The Pmod module sends data from the ZedBoard to an external computer using a serial code with a start and stop bit. A baudrate of 921 600 bit/s is chosen to allow a fast data transfer.

2.5.2. SOFTWARE: FSM

The software used to for the memory controller is written in VHDL. The VHDL code gives a description of the behaviour of the memory controller as well as the physical interaction with the peripherals (custom PCB and UART Pmod). The physical wiring and pin connections are also defined in the VHDL code.

The memory controller is programmed as a finite state machine (FSM). Different states are called sequentially such that the memory controller performs actions in the correct order. The memory controller handles one FSM for the Pmod UART connection and one FSM for the NAND memory operations to ensure proper signal timings. The different states of the memory controller are invoked by a Python script. The states available in the FSM are divided into two categories: the main states and the substates. The main states include the current mode of the memory controller. This includes operations, such as reading, writing and erasing. The substates are defined within each main state and describe the operations that are performed within a read, write or erase procedure. The address cycles and commands that need to be executed and send to the memory are described in the substates.
Figure 2.26 shows the most used states and their substates from the FPGA.

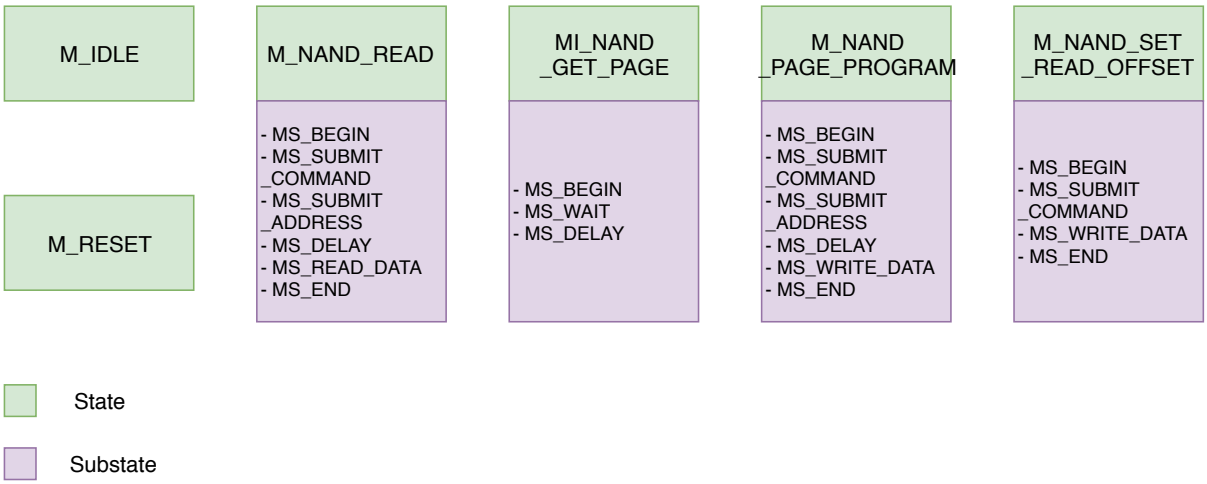


Figure 2.26: Overview of states and substates available in the FSM

The states and their substates are briefly explained:

- **M_IDLE**: The idle state of the Finite State Machine. While the FPGA is in this state, it is able to receive commands.
- **M_RESET**: Resets the variables of the FPGA and clears the cache memory of the rawNAND memory chip. This command should be performed at startup of the memory controller.
- **M_NAND_READ**: Used to read one page of a memory block.
  - **MS_BEGIN**: Prepares the memory chip for read procedure.
  - **MS_SUBMIT_COMMAND**: Sends the read command (00h-30h) to the memory chip.
  - **MS_SUBMIT_ADDRESS**: Writes the address onto the memory chip. The address consist of six address cycles, which include the selected LUN, block, page and column to read.
  - **MS_DELAY**: Sets the FSM into a waiting state until the chip is ready to be read.
  - **MS_READ_DATA**: Copies the memory data from the rawNAND cache memory to the FPGA.
  - **MS_END**: Marks the end of the read operation and performs clean up of used variables.
- **MI_NAND_GET_PAGE**: Transfers the read data from **M_NAND_READ** from the FPGA to the external computer.
  - **MS_BEGIN**: Initiate transfer of page data per byte.
  - **MS_WAIT**: Wait until the transfer of one byte is complete.

  - **MS_DELAY**: Delay state which the controller is set to when the transfer of a byte is has not yet been completed.

- **M_NAND_PAGE_PROGRAM**: Used to program a page of a memory block.
  - **MS_BEGIN**: Prepares the memory chip for program procedure.
  - **MS_SUBMIT_COMMAND**: Sends the program command (80h) to the memory chip.
  - **MS_SUBMIT_ADDRESS**: Writes the address onto the memory chip. The address consist of six address cycles, which include the selected LUN, block, page to program.
  - **MS_DELAY**: Sets the FSM into a waiting state until the chip is ready to be programmed.
  - **MS_READ_WRITE**: Writes the value '1'(FFh) or '0'(00h) onto the page.
  - **MS_END**: Marks the end of the program operation and performs clean up of used variables.
- **M_NAND_SET_READ_OFFSET**: Used set the read offset voltage.
  - **MS_BEGIN**: Prepares the memory chip to change the read offset voltage to the desired value.
  - **MS_SUBMIT_COMMAND**: Sends the set read offset command (EFh-ABh) to the memory chip.
  - **MS_WRITE_DATA**: Writes the read offset voltage values onto the memory chip in four write cycles. Only the first cycle determines the read offset voltage. The other three bytes are '00000000'(00h).
  - **MS_END**: Marks the end of the set read offset operation and performs clean up of used variables.

3

3D NAND DATA PROCESSING

An initial read out method was developed for the space radiation monitor prototype. This Chapter explains elaborates on that particular read-out method and presents an updated read-out scheme with a binary search. The differences between the read-out methods is discussed by addressing the advantages and disadvantages of each method. The Chapter is concluded with a verification process of the used signals in the read-out scheme.

3.1. PAGE BY PAGE READ

The initial prototype reads every page of a block at different read offset voltages. The read offset voltage can be modified to determine the threshold voltage of a memory cell. Figure 3.1 shows how a memory cell is read.

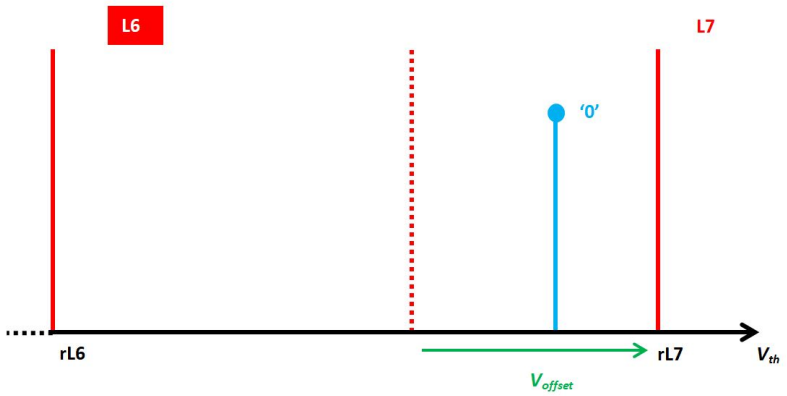


Figure 3.1: Read procedure to determine the threshold voltage of a memory cell.

The procedure of reading a complete block is given in Figure 3.2. The page by page read starts with selecting a page address. To determine the threshold voltage for cells programmed to L7 only the last bit needs to be checked of a TLC memory cell. The last bit of a TLC memory cell is stored in the upper pages of the shared pages.
After the address has been selected, the read offset voltage can be selected. The read offset voltage can be chosen between -960 mV and 960 mV with a 7.5 mV interval. The rawNAND memory will then read the data from the selected page and copies the data on the cache memory of the rawNAND memory. The cache memory of the rawNAND memory can be obtained by the ZedBoard and is stored on the ZedBoard memory. Once the whole page has been copied from the rawNAND to the ZedBoard, the ZedBoard allows a serial communication with an external computer to send the data.
Finally the bit values of the complete page at the chosen read offset voltages is saved on the external computer.
The next read offset is set and the rawNAND memory is read again. This process continues until the page has been read at all the chosen read offset voltages, after which the next page address is chosen and read at the different read offset voltages. Once all the pages has been read, post processing is required to obtain the threshold voltages of each memory cell. The data stored contains the binary data (either a '0' or '1') for each memory cell at each read offset voltage. The measurement data is then processed using Python to identify the readout voltages at which a bitflip occurs and is saved as the threshold voltages of a memory cell.

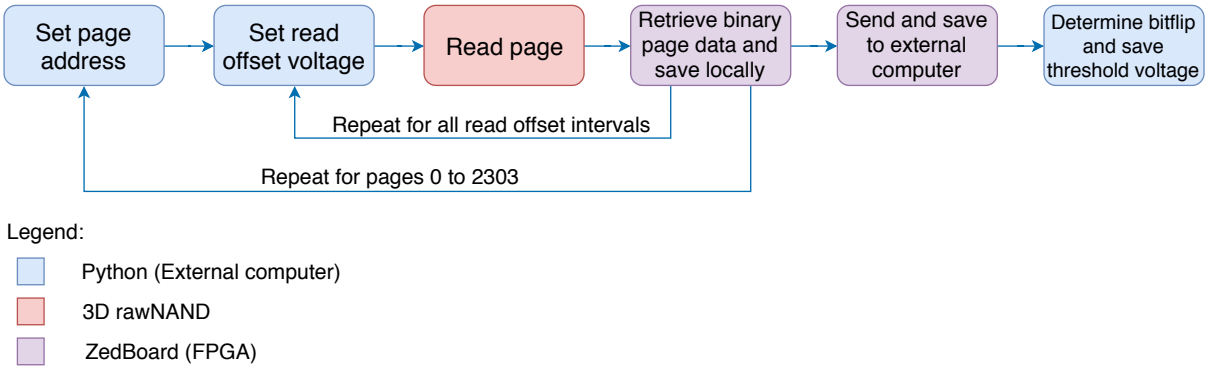


Figure 3.2: Flow diagram of reading a block page by page. The colors indicate which hardware and/or software is involved.

3.2. Binary search

The page by page read method requires a large amount of storage capacity on the external computer to save all the data. The bit value of every memory cell is stored on the external computer to determine the threshold voltage in the memory cells. To reduce the amount of storage required, another method is used which analyses the bit values of the memory cells on the ZedBoard (FPGA) and only sends the actual threshold voltages of the memory cells as an integer represented by eight bits. The FPGA has a limited amount of storage and processing power. It is therefore decided to evaluate the threshold voltages per memory cell, as larger array computations deemed to be too complicated.

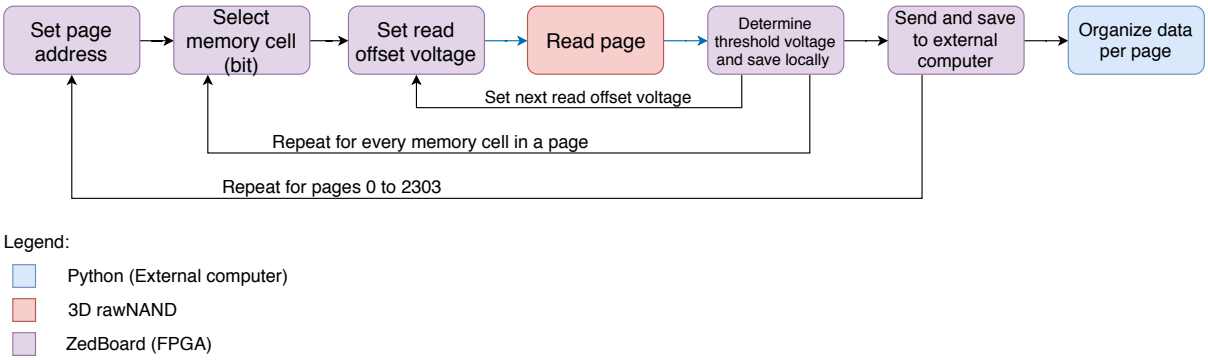
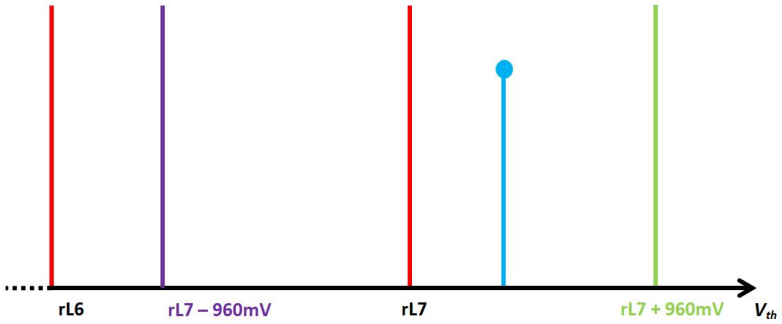


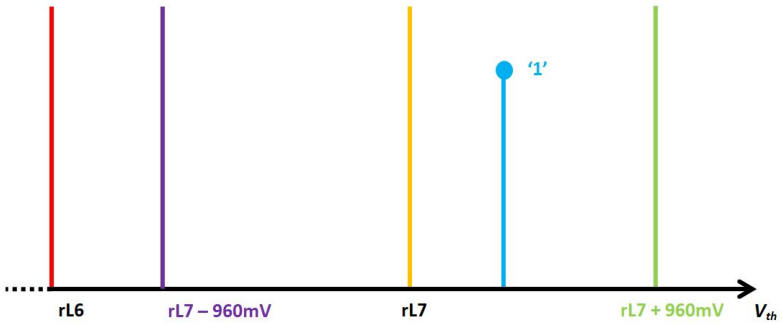
Figure 3.3: Flow diagram of reading a block with a binary search. The colors indicate which hardware and/or software is involved.

Figure 3.3 shows procedure to read and analyse a memory block per memory cell. The FPGA handles most of the operations, such as selecting the page addresses and the read offset voltages.
With the selected page address and the read offset voltage, the page is read. The FPGA only stores the bit value of the memory cell it is evaluating. To determine the threshold voltage of a memory cell, the bit value of the memory cell at the lowest (-960 mV) and highest (+960 mV) read offset voltage. For cells that are programmed to L7, the last bit is '1'. The logic level L6, has as last bit value '0'.
Figure 3.4 shows a schematic representation of the iterative process to find the threshold voltage in a memory cell. First, the the memory cell is read at the upper boundary and lower boundary. The threshold voltage of the memory needs to be within the lower and upper boundary to ensure that the threshold voltage can be found. When reading the at the lower boundary, which is -960 mV relative to the read offset level, the memory cell should be read as '0' for rL7. If it is read as a '1' instead, the FPGA will stop reading the memory cell, the threshold voltage is located below rL7-960 mV.
A similar approach is taken for the upper boundary, which is located at +960 mV relative to rL7. For the upper bound, the memory cell should be read as a '1' to fall within the binary search range. When the memory cell is identified as a '0', the FPGA identifies this cell as faulty as it is threshold voltage exceeds the read-out range. If the memory cell has passed the check for the upper bound and lower bound,

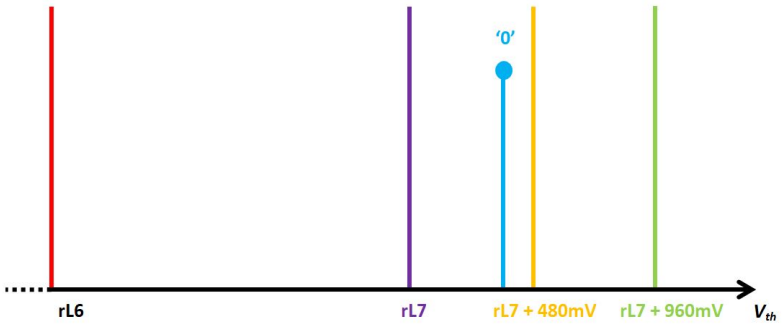
the FPGA will perform a binary search to find the threshold voltage of that memory cell. An example of the binary search method is shown in Figure 3.4. The first read is performed at rL7. In this particular example, the threshold voltage of the memory cell is located between rL7 and rL7+960 mV. When the memory cell is being read at rL7, the memory will return a bitvalue of '1'. The FPGA now knows that the threshold voltage is higher than read offset voltage rL7 but lower than rL7+960 mV. Therefore, the FPGA sets rL7 as the lower bound for the next read operation.
The next read operation is performed, again at the read offset voltage in the middle of the upper and lower bound. Since the lower bound has been shifted to rL7, the second read operation is performed at rL7+ 480 mV. In this example, the threshold voltage is lower than rL7+480 mV and therefore the memory returns a bitvalue of '0'. The FPGA can now sets rL7+480 mV as the new upper bound can continue to read the cell until the threshold voltage of the memory cell has been found. Once the upper bound and lower bound are 7.5 mV apart, which is the minimum step size of the read offset voltage, the FPGA saves the average of the upper bound and lower bound as threshold voltage of the cell. The read offset voltages can be selected from -960mV up until +960 mV. With a step size of 7.5 mV, 256 different read offset voltages can be selected. The 256 read offset voltages are linked to an 8-bit integer value. The threshold voltages are stored as an 8-bit integer, ranging from 0 until 255.
The threshold voltage is thus saved as one byte, whereas, in the page sweep read operations, one byte contains information of eight memory cell. Due to the limited amount of available memory on the FPGA, for the binary search, a page is split up into eight parts. The FPGA sends the information to an external computer through a serial connection. The serial data can be captured by Python and the 8-bit integers can then be translated to the corresponding threshold voltages.



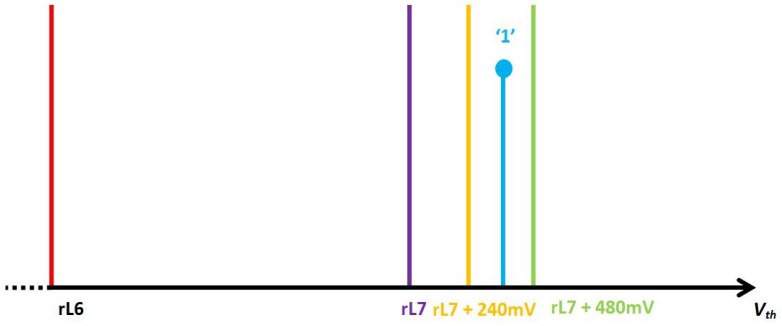
(a) The first lower bound is set to -960 mV and the first upper bound is set to 960 mV.



(b) First measurement at rL7.



(c) Second measurement at rL7+480 mV.



(d) Third measurement at rL7+240 mV.

Figure 3.4: Determining the threshold voltage of a memory cell. Upper bound (green), lower bound(purple) current read offset voltage (orange).

3.3. COMBINED READ-OUT SCHEME

While the page by page read is a systematic approach on reading the memory cells, the large number of serial communication between the FPGA and the external computer slows down the process significantly. On the other hand, the binary search method increases the readout speed significantly for targeting single memory cells as it is not required to fully read a page from the rawNAND memory cache onto the FPGA. Reading a large number of cells however, makes the binary search inefficient.
A third read-out scheme is developed to benefit from both previously mentioned read-out schemes. The combined read-out scheme first uses the page by page read to obtain the threshold voltages from memory cells in 8 layers, spaced evenly among the memory block.
The threshold voltages are sent to the external computer and analysed. Pillars that are affected by radiation are isolated by using a filter. All the threshold voltages that fall within 2 times the standard deviation from the mean are discarded. Furthermore, a pillars is identified if at least 5 of the 8 layers falls outside 2 times the standard deviation of the mean. Figure 3.5 shows the function of the combined read-out method.

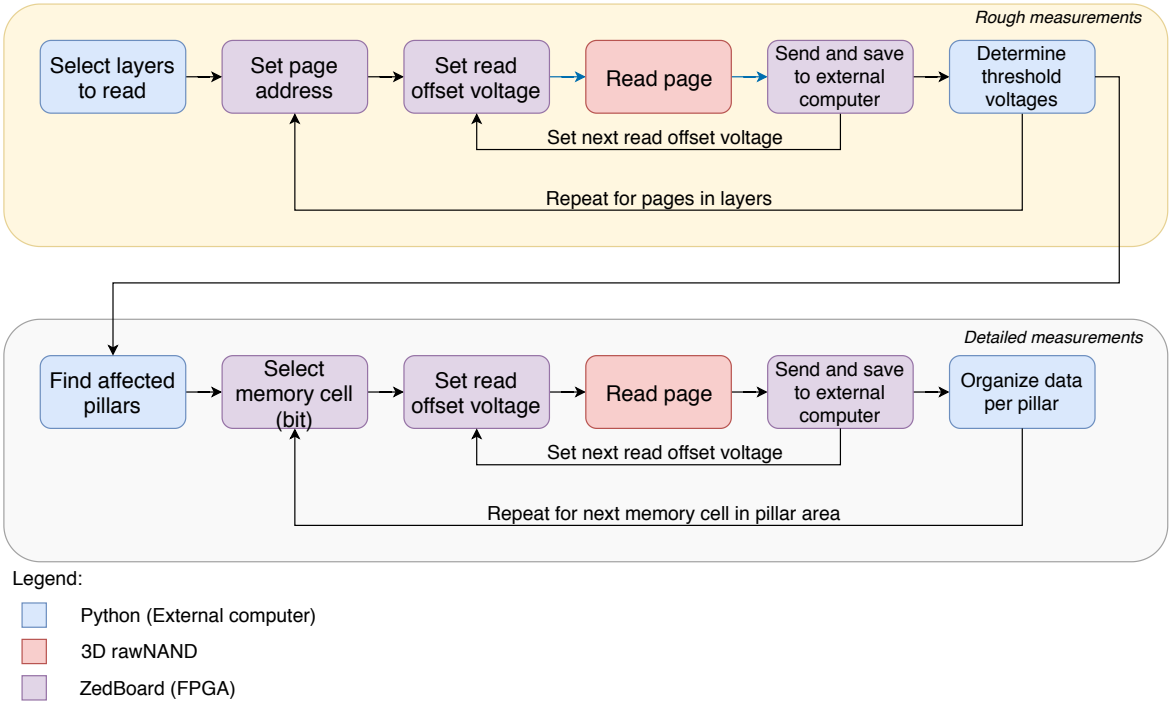


Figure 3.5: Flow diagram of the combined read-out scheme.

The combined read-out scheme can be separated into two parts, a rough measurement where the memory block is read for a couple of layers to find pillar affected by radiation. Those affected pillars are then further analyzed by using a more accurate readout method with the binary search.

3.4. Comparison of the read-out methods

To conclude the methods of reading the memory block, a comparison is made on the different read-out techniques. For all three cases, a block is read and the performance of each is method is recorded and shown in Table 3.1.

Table 3.1: Performance characteristics of the tested measurement methods used to read one block.

	Page by page	Binary search	Combined
Read size	Page	Memory cell (bit)	Page and memory cell (bit)
Required storage	3 GB	900 MB	50 MB
Measurement time	9.4 hours	10 hours	20 minutes

From Table 3.1, it can be seen that the combined reading method has several benefits over the other read-out method. The main advantages are the reduction in measurement time and data needed to store the measurement results. Both of these advantages make the use of the 3D NAND memory chip as a low-cost space radiation monitor more feasible. To achieve this performance, less data is read from the memory block, which makes it easier to miss affected pillars. Moreover, this method is useful for pillars that are irradiated by a beam without an incidence angle. For a radiation beam that affects the memory block with an incidence angle, another method might be more applicable, or the number of analyzed layers needs to be tweaked, as not all memory cells in a pillar will be identified as affected with the proposed read-out scheme.

3.5. Signal verification

In this Section, the signals from the memory chip are verified using a LogicAnalyzer. The LogicAnalyzer used is the Saleae Logic Pro 16. The signal schematics from the raw3D NAND memory are obatined from the Micron datasheet. [37]

3.5.1. Probed signals

The memory chip sends a total of 16 signals to the FPGA which can be probed. Eight of the signals (DQ0-DQ7) are used for data input and output. The other signals are control signals used for write and read instructions, which also includes signals which enable the chip and protect the chip from being read. An overview of the probed signals is given in Table 3.2.

Table 3.2: Signals from and to the raw3D NAND chip

Signal	Description	Type
DQ (0-7)	8-bit Data signal: bidirectional data input/output.	Input/Output
ALE	Address Latch Enable: Loads an address from the data signal to the address register.	Input
CE#	Chip enable: Used to select the LUN to perform the operations on.	Input
CLE	Command Latch Enable: : Loads an command from the data signal to the address register.	Input
RE#	Read Enable: Transfers serial data from NAND flash to the host system when active.	Input
WE#	Write Enable: Transfers command, address and serial data from host to NAND flash.	Input
WP#	Write Protect: Enables or disables PROGRAM and ERASE operations.	Input
R/B#	Read/busy: An open-drain active low output. Requires external pull-up resistor. Signal indicates target array activity.	Output

3.5.2. ADDRESS SIGNALS

To perform a read operation on the memory, a address needs to be issued by the memory controller, in this case, the FPGA. Figure 3.6 shows the signal diagram provided by the data sheet from Micron. The signal diagram shows which signals are pulled high and low and the different timings.

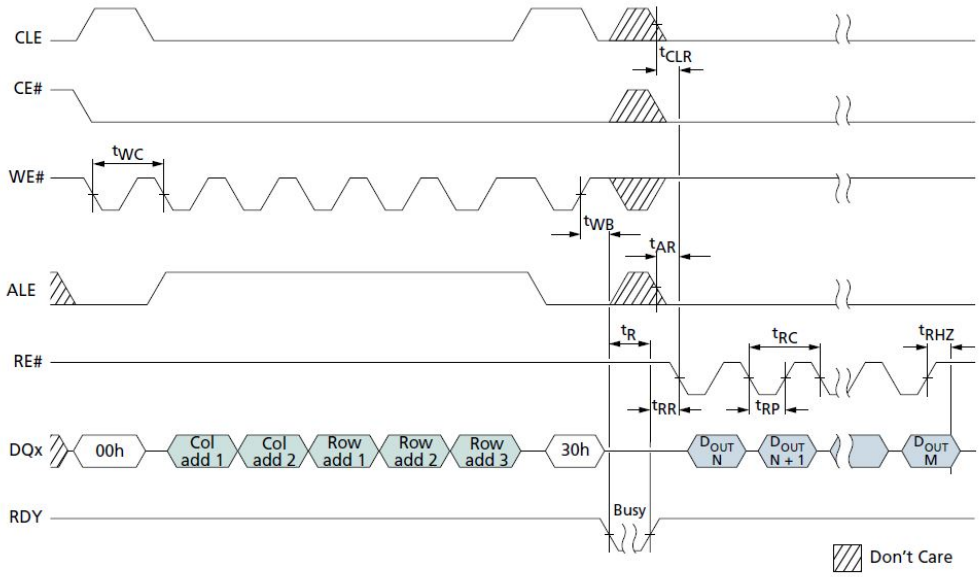


Figure 3.6: Memory chip address signals and timings. [37]

The commands issued in the signal diagrams are shown in hexadecimal, in practice, the memory controller translates the hexadecimal value to an 8-bit binary value. Reading a page starts with issuing command '00h'. The CLE signal is pulled low as well as WE# signal, this indicates that a command is loaded into the memory chip. After the command has been selected, the address can be latched into the memory. The address cycle consist of five bytes. This is split up into two column addresses and three row addresses. The DQ signals are used as input for the address cycle. During this operation, the ALE signal is pulled high as well as the WE# pulling low and high during the process. The difference in low and high of the WE# signal separates the address bytes.
After successfully inputting the address cycle, the '30h' command is raised, which tells the memory to read the selected page from the address cycle. CLE is pulled high again to indicate a command being issued. After read command latched onto the memory, the memory will perform the read and sets it self into a busy state. The R/B# signal is pulled low, indicating that the memory chip is busy. During this stage the chip does not care about the other signals and ignores incoming signals until it is done reading. Once the chip is done, the memory can send the data to the FPGA. the memory sends the data one byte at a time. The bytes are separated by the RE# signal being pulled high and low.

The signals during a read operation are captured using a Logic Analyzer.[40] A screenshot of the result is given in Figure 3.7. The relevant signals are shown in rows, including the eight data signals (DQ0-DQ7), CLE, ALE, RE#, R/B# and WE#. A timescale is provided to indicate the timings between the signals. The input signals (DQ0-DQ7) are decoded into their corresponding bitvalue for better visibility. The bytes that contain the commands are colored in blue and the address bytes are colored red.

The signals shown in Figure 3.7 are probed from the custom PCB and are the signals that are directly issued to the memory. These diagrams are used t verify whether the issued commands and addresses correspond to what the micro-controller is supposed to do.
Starting with the first command, it is issued when CLE signal is high and WE# signal is low. The command to latch an address onto the memory is '00h' in hexdecimal, translates to '00000000' in binary.

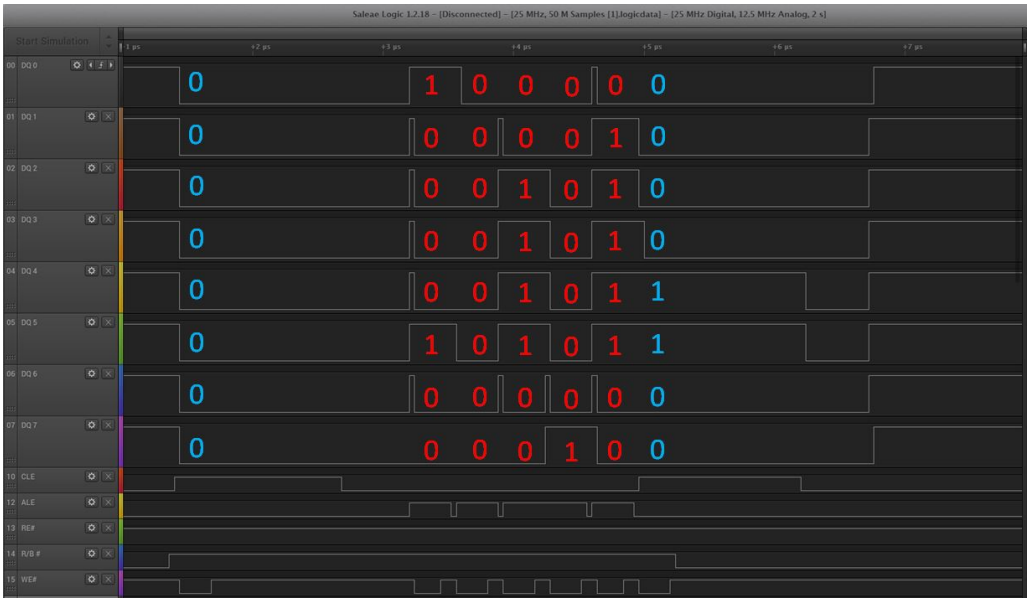


Figure 3.7: Address signals probed by the LogicAnalyzer.

3.5.3. SETTING THE READ OFFSET VOLTAGE

The read offset voltage can be set by invoking the 'SET FEATURE' command on the memory chip. The timing diagram of this operation is shown in Figure 3.8.

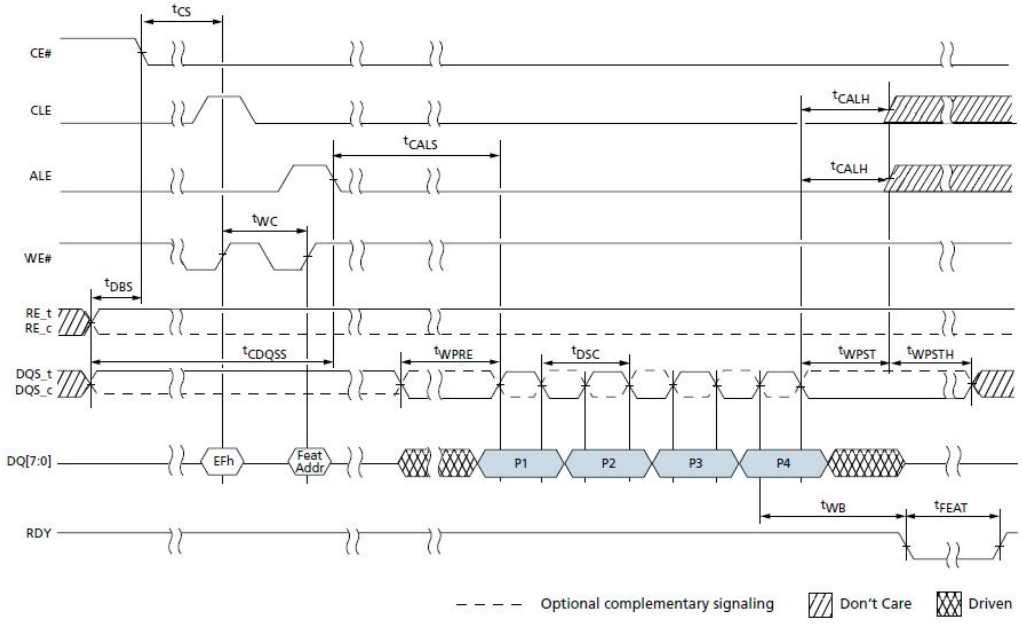


Figure 3.8: Signals and timings to set read offset voltage. [37]

To call the command, EFh is latched onto the command latch unit and the CLE signal is pulled high. After the SET FEATURE operation has been issued, the memory chips awaits the feature address and pulls the ALE signal high. The feature address selects which read offset voltage is changed. The feature address for read offset level (rL7) is ABh. Four subfeatures (P1-P4) are requested by the chip once the feature address had been set. The read offset voltage can be selected ranging from -960 mV to +960 mV with respect to the read offset level and at intervals of 7.5 mV. Only the first subfeature (P1) is used for setting the read offset voltage, the other three subfeatures are set to a value of 00h. Table 3.3 shows the values of P1 and their respective offset voltage.

Table 3.3: P1 Subfeature Values and Corresponding Offset Voltage

P1 Subfeature Value (DQ7-DQ0)	Offset Voltage (7.5 mV resolution)
00h	0
01h	7.5mV
02h	15mV
...	...
7Dh	937.5 mV
7Eh	945 mV
7Fh	952.5 mV
80h	-960 mV
81h	-952.5 mV
82h	-945 mV
...	... mV
FDh	-22.5 mV
FEh	-15 mV
FFh	-7.5 mV

With a resolution of 7.5 mV and a range of -960 mV and +960 mV, P1 has up to 256 different values, which are all captured in the first subfeature byte (P1). When using the binary search to find the threshold voltage, a mapping is required that sets the lowest index to the lowest threshold voltage (-960 mV) and the highest index to the highest threshold voltage (+960 mV) and an increasing threshold voltage with increasing index number. From Table 3.3 it can observed that the first value 00h (0 in decimals) marks the mean of the available offset voltages, while the value 7Fh (127) in decimals), refers to a offset voltage of +952.5 mV. The negative offset voltages take values from 80h (128) for -960 mV to FFh (255) for -7.5 mV.
Table 3.4 shows a re-arranged order of the P1 subfeature values with an index identifier to select the read offset voltage more convenient.

Table 3.4: Rearranged P1 Values with index identifier.

Index	P1 Subfeature Value (DQ7-DQ0)	Offset Voltage (7.5mV resolution)
0	80h	-960 mV
1	81h	-952.5 mV
2	82h	-945 mV
..	...	... mV
125	FDh	-22.5 mV
126	FEh	-15 mV
127	FFh	-7.5 mV
128	00h	0
129	01h	7.5mV
130	02h	15 mV
...	...	...
253	7Dh	937.5 mV
254	7Eh	945 mV
255	7Fh	952.5 mV

After the subfeatures have been set, the R/B# signal is pulled low, which gives the chip time to adjust the read offset voltage to the value given by the subfeatures.
Setting the correct read offset voltages is essential for determining the threshold voltage of a memory cell. The signals during the 'Set read offset voltage' operation were probed with the Logic Analyzer. The probed signals are shown in Figure 3.9.

Figure 3.9: Probed signals for setting an offset voltage at index 31

Similar to the address signals verification, the command signals and address signals, which are highlighted in blue and red respectively The byte read during the read operation is shown in green and the subfeatures signals are shown in yellow. The probed signals show that the CLE is pulled high for a command byte and ALE is pulled high for a address byte. The RE signals is pulled low when a page byte is read by the memory. Finally, the WE# is pulled low when data needs to be written to the memory. To verify that the correct command, address and subfeature values are latched onto the memory, the hexdecimal values of the commands and addresses are translated to binary. The command EFh, which is used to start the SET FEATURE operation, is equivalent to '11101111' in binary. The probed command signal in blue match the binary value. The address signal to change the read offset voltage of rL7 is ABh, which is '10101011' in binary. The red address signal from the LogicAnalyzer shows the same binary sequence. To ensure that the binary search method is correctly programmed onto the memory controller, the next read offset voltage operation in a binary search is probed. The signals are shown in Figure 3.10.

Figure 3.10: Probed signals after setting the readoffset voltage to index 47

The signals from Figure 3.10 are very similar to the signals from Figure 3.9. A difference can be seen in the read data byte. The second readout shows that all the memory cells have a bit value of '1', where as the first readout showed a bit value of '0' except for the third bit of that byte. The difference in readout byte is a result of reading at difference read offset voltages. The first subfeature is also different for the second readout. During the first readout, the P1 value is '00011111' and for the second readout the P1 value is '00101111'. '00011111'is equivalent to 31 in decimal and '00101111' corresponds to 47 in decimal. To verify that the binary search method is working as intended, the signal before the operation shown in Figure 3.9 are probed. Figure 3.11 shows the probed signals before the the P1 value of 31.

Figure 3.11: Setting the read offset voltage to index 64

The P1 value of Figure 3.11 is '11111100' which is 64 in decimals. The sequence in which the subfeature P1 is set is 64,31,47. This is in compliance with the binary search method as the index identifier 47 is in the middle of 64 and 31.

4

DATA ANALYSIS

In this Chapter, the gathered data is analysed from an Ultra High Energy Pb Heavy Ion radiation test at CERN. The performed operations and methods required to perform the data analysis are discussed. The threshold voltage shift as a result of radiation exposure is presented. A comparison between the found test results and measurement data from literature concludes this Chapter.

4.1. DATA ACQUISITION

Three memory chips were exposed to radiation at CERN. CHIP1 and CHIP2 were irradiated without incidence angle, while CHIP3 was irradiate with a 30° angle. From each chip two memory blocks are read, block 1000 (B1000) and block 1001 (B1001). A 33 TeV Pb beam was used for all three CHIPs. An overview of the test conditions is shown in Table 4.1.

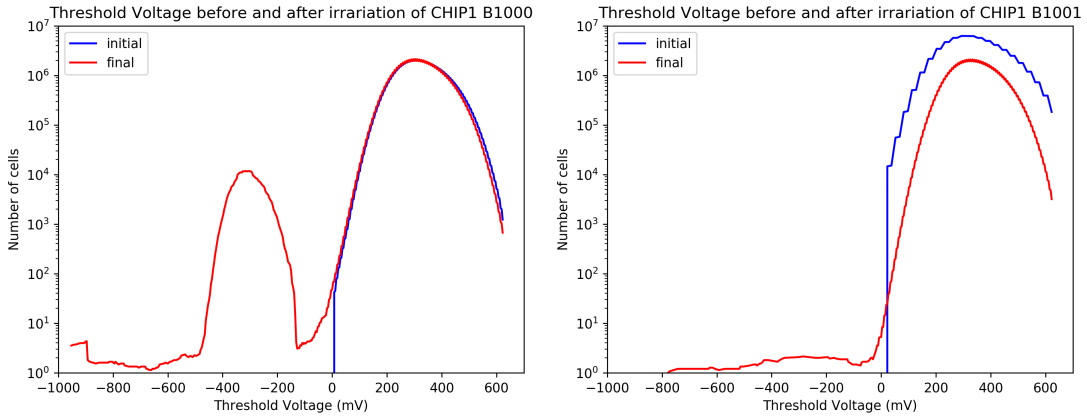
Table 4.1: Test condition of Ultra-High Energy Pb beam at CERN.

	Exposure duration	Incidence angle
CHIP1	1 hour	0 °
CHIP2	6 hours and 45 minutes	0 °
CHIP3	10+ hours	30 °

Threshold voltage measurements were taken before and after radiation. In total twelve measurement operations were performed. For every memory cell, the three bits stored are split into three different logical/virtual pages. Memory cells in the same page have their split bits stored in shared (logical) pages. For the data analysis, only the last bit of the TLC is of interest, as this is the bit that flips when the memory cell changes from L7 to L6. The obtained data only contain the threshold voltages from the shared pages that correspond to the last bit of the read memory cell. This measurement technique only accounts for memory cells that are read as L6 after irradiation, as lower logic levels have bitflips in the first or second bit of the memory cell. A total of 744 shared pages are collected for each measurement. Every shared page contains the threshold voltages of the memory cells in the corresponding physical page. One shared pages contains 148 736 memory cells. The shared page data is stored as a pickle file to easily access the data.

4.2. THRESHOLD VOLTAGE SHIFT

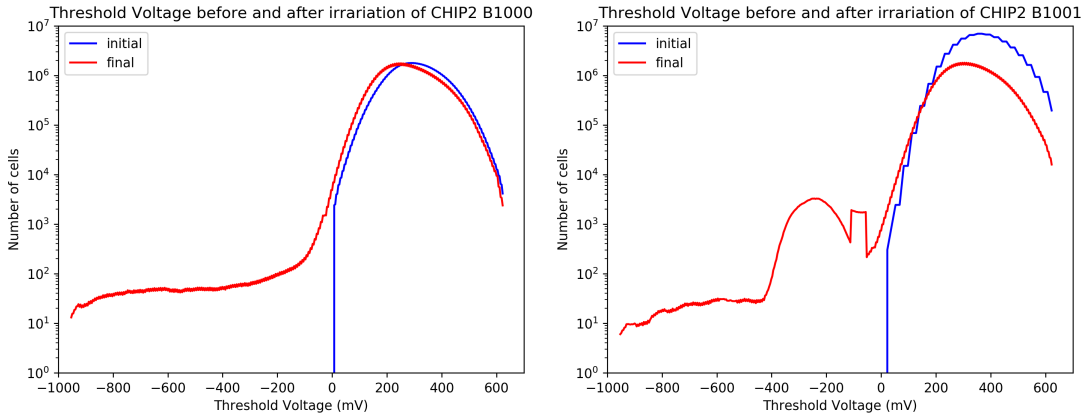
The threshold voltage of the memory cells in all six blocks are measured. The threshold voltage before irradiation and after irradiation is measured to calculate the threshold voltage shift of every memory cell. The threshold voltage is calculated by subtracting the initial threshold voltage from the final (after irradiation) threshold voltage. The distribution of the threshold voltages before and after irradiation are plotted for every block. Since the block contains over 100 million data points, a log scale is used for the number of cells. The threshold voltage distribution for CHIP1 in B1000 are plotted in Figure 4.1a.



(a) Block 1000 (b) Block 1001

Figure 4.1: Threshold voltage distribution before and after irradiation for CHIP1

The threshold voltage relative to read offset level rL7 is plotted on the x-axis and the number of cells with the corresponding threshold voltage is plotted on the y-axis. The threshold voltage distribution before irradiation shows a clear normal distribution with a mean around 300 mV.
For the threshold voltage distribution after irradiation however, a second peak can be observed around -350 mV. This second peak is smaller in terms of amplitude and width. For this block, there are a number of cells that show very negative threshold voltages after irradiation, in the range if -800 mV and -1000 mV.
The other block read from CHIP1 is B1001. The threshold voltage distribution of this block is shown in Figure 4.1b
The threshold voltage distribution for B1001 in CHIP1 follows the voltage distribution before irradiation. A small bump is visible between -400 mV and -200 mV for the voltage distribution after irradiation. This is in the same range as shown in B1000. The threshold voltage after irradiation in B1001 does not go below -800 mV, which is in contrary with B1000 from the same chip.
Moving on to CHIP2, the threshold voltage distribution for B1000 and B1001 is shown in Figure 4.2a and 4.2b, respectively.

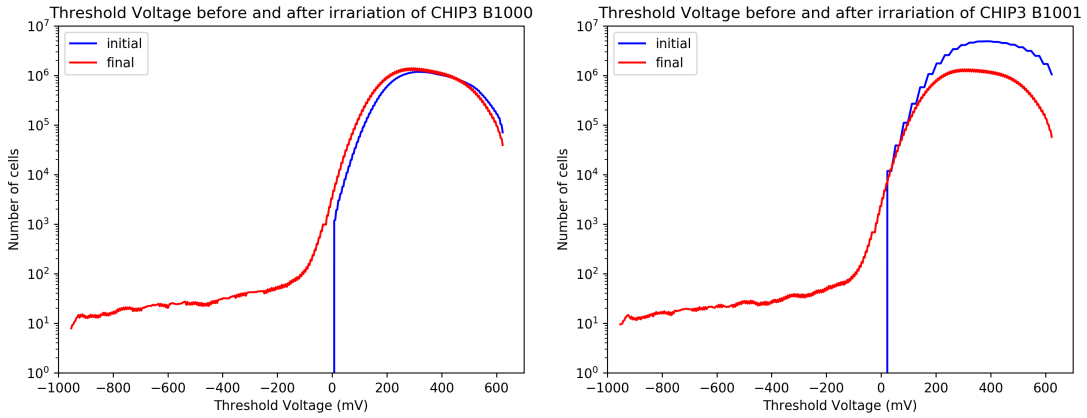


(a) Block 1000 (b) Block 1001

Figure 4.2: Threshold voltage distribution before and after irradiation for CHIP2.

Both blocks in CHIP2 show a slight shift of the main peak around 300 mV and a tail on the negative threshold voltages after irradiation. A difference after irradiation can be seen in the blocks around -300 mV, where B1001 shows a prominent peak with around 1000+ cells having their threshold voltage shifted to this value.

For CHIP3, Figure 4.3a shows the voltage distribution for B1000 and Figure 4.3b shows the threshold voltage distribution for B1001.

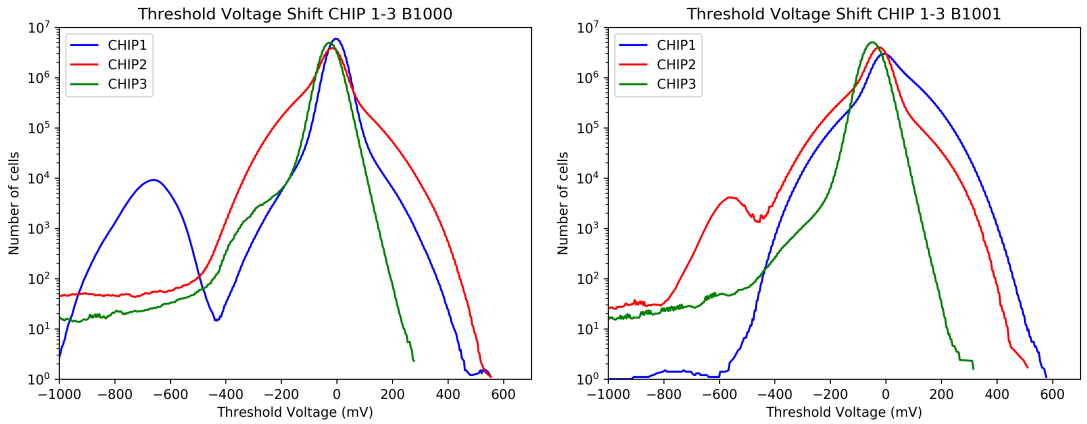


(a) Block 1000 (b) Block 1001

Figure 4.3: Threshold voltage distribution before and after irradiation for CHIP3.

The threshold voltage distribution after irradiation shows similar results for both blocks. A tail on the distribution is seen in the negative threshold voltage range. CHIP3 shows no clear peak in the threshold voltage distribution other than the initial normal distribution from the programmed logic level. The extra peak as observed in CHIP1 and CHIP2 could be the result of irradiating the pillar from top to bottom without incidence angle.

The difference in threshold shifts between the three chips is shown in Figure 4.4a and 4.4b for B1000 and B1001 respectively.



(a) Block 1000 (b) Block 1001

Figure 4.4: Threshold voltage Shift for CHIP1-3

Both threshold shift figures show a normal distribution around 0mV, which could relate to the memory cells that are not or affected very little by the radiation. Furthermore, both distributions show that a large number of cells have a negative threshold voltage shift. Two types of shifts can be observed from these distributions. The first type is the introduction peak due to a normal distribution at a lower threshold voltage. This is the case for CHIP1 B1000 and CHIP2 B1001. The other type of threshold voltage shift is a gradual tail, where the number of affected cells decreases with decreasing threshold voltage shift and no peak is observed.

4.3. DATA FILTERING

Slices can be made in the yz-plane of the memory block to observe the effects on pillars. The threshold voltages for such a slice is plotted with the layers on the y-axis and the columns on the x-axis. Figure 4.5 shows the threshold voltage shifts for memory cells in CHIP2 block 1000 in row 14. The black lines indicate the memory cells from which the threshold voltage could not be determined. A possible explanation could be permanent displacement damage due to radiation on the memory's bitline which causes a part of the row to be unreadable.

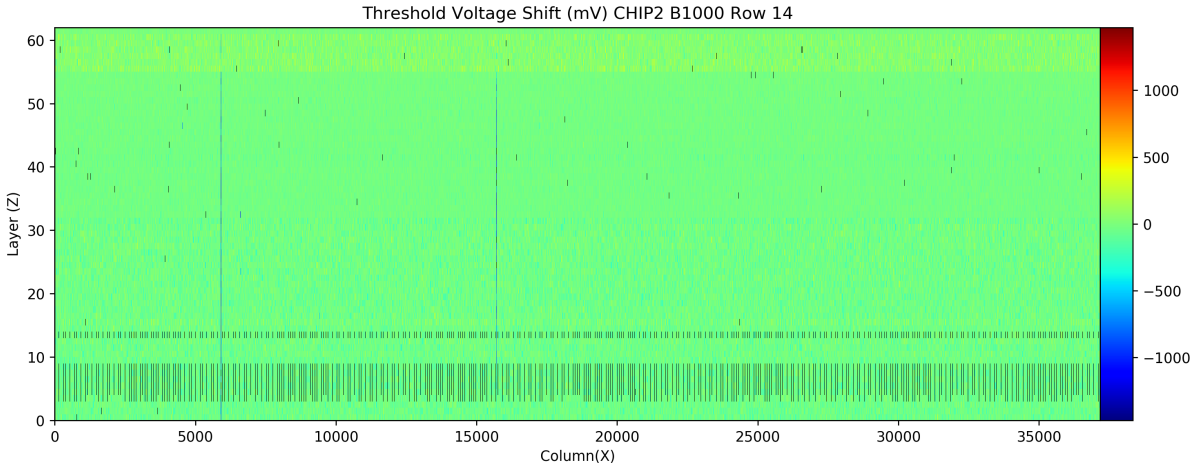


Figure 4.5: Unfiltered data of memory cells in row 14 of CHIP2 B1000

In this rows, two affected pillars can be seen, one around column number 5500 and one at 16000. The large number of memory cells per slice however, makes it harder to detect less pronounced pillars and other effects.
A filter is applied which depends on the mean and standard deviation of the dataset. From Figure 4.5, it can be seen that the majority of the data is around 0mV (colored green). These are the memory cells that have no to little threshold voltage shifts after irradiation. This can either be small effects of radiation or readout inaccuracies. To only capture the memory cells that have larger threshold voltage shift and therefore are heavily affected by radiation, the data is filtered on one, two or three times the standard deviation. For a standard deviation filter of one, the data that falls within one standard deviation of the mean is discarded, which is roughly 68% of the data. For the two times standard deviation filter, 95% is discarded and for the three times standard deviation filter 99.7 % of the data is discarded. When using the three times standard deviation filter, 0.3% of the data is considered for pillar detection, which are 331.978 memory cells. The mean is calculated with Equation 4.1.

$$\mu = \frac{\Sigma x}{n} \tag{4.1}$$

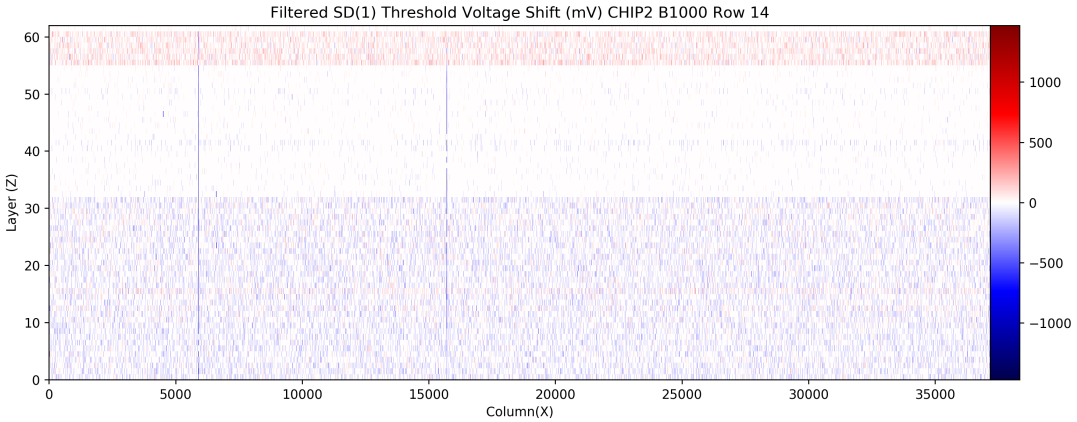
Where μ is the mean of the dataset, x is a value of the dataset and n is the number of values in the dataset. With the mean, the standard deviation can be calculated. The equation to compute the standard deviation is shown in Equation 4.2. [41]

$$\sigma = \sqrt{\frac{\Sigma \left(x_i - \mu\right)^2}{n-1}} \tag{4.2}$$

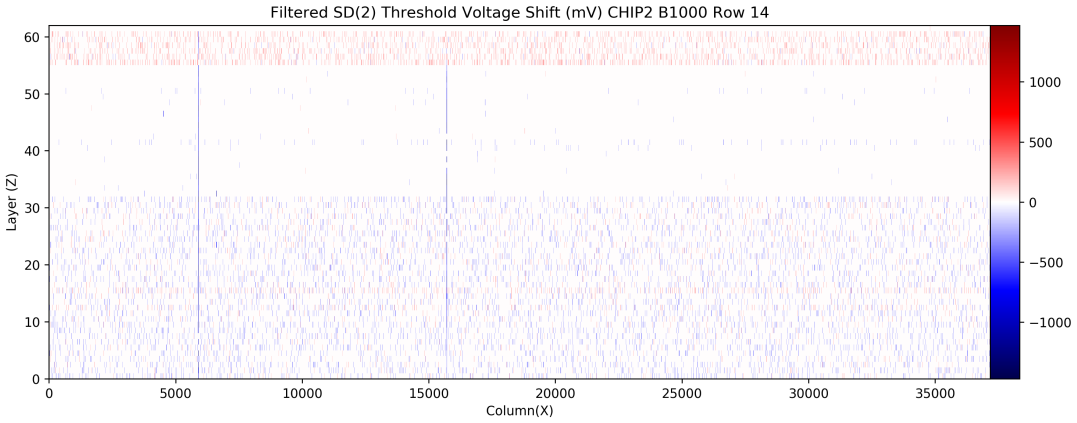
Where σ is the standard deviation and x_i is the value of the dataset iterated over i for every point of the dataset.
The mean and standard deviation for the analyzed memory blocks is shown in Table 4.2.
Figure 4.6 shows the data from Row 14 after all three filters for comparison.
The different filters show how the dataset is reduced as the standard deviation increases. The two affected pillars are visible for all three filters, however, the other affected cells for SD3 filter become very faint. It is therefore preferred to use the SD1 or SD2 filter, to keep as many relevant data points as possible. Another reason to filter the dataset is to reduce the computation time.

Table 4.2: Statistical analysis of threshold voltage shift in analyzed memory blocks.

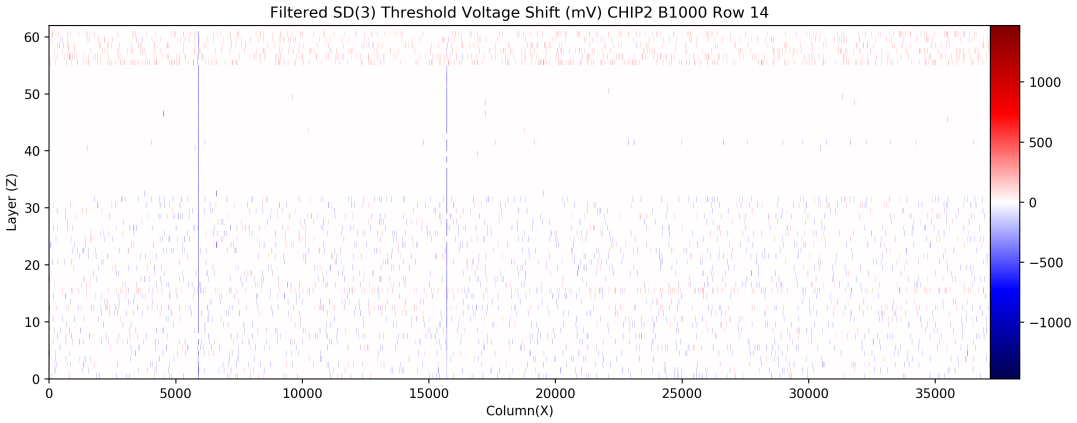
	CHIP1		CHIP2		CHIP3	
Block	1000	1001	1000	1001	1000	1001
Mean μ	-6.6 mV	12.8 mV	-27 mV	-40 mV	-28 mV	-49 mV
Standard deviation σ	50 mV	81 mV	70 mV	71 mV	32 mV	34 mV
Min.	-1571 mV	-1268 mV	-1470 mV	-1493 mV	-1538 mV	-1575 mV
Max.	551 mV	578 mV	555 mV	510 mV	277 mV	315 mV



(a) SD1 filter



(b) SD2 filter

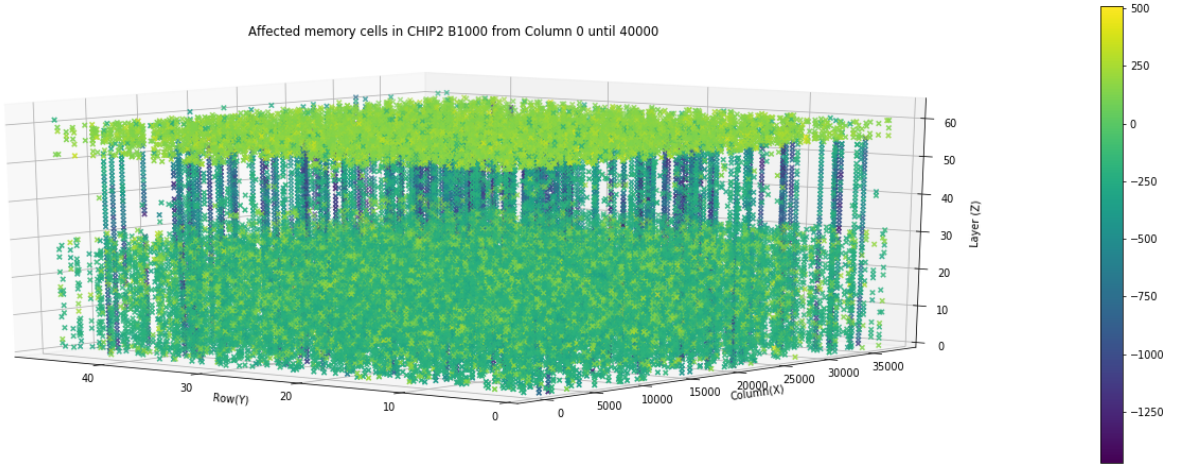


(c) SD3 filter

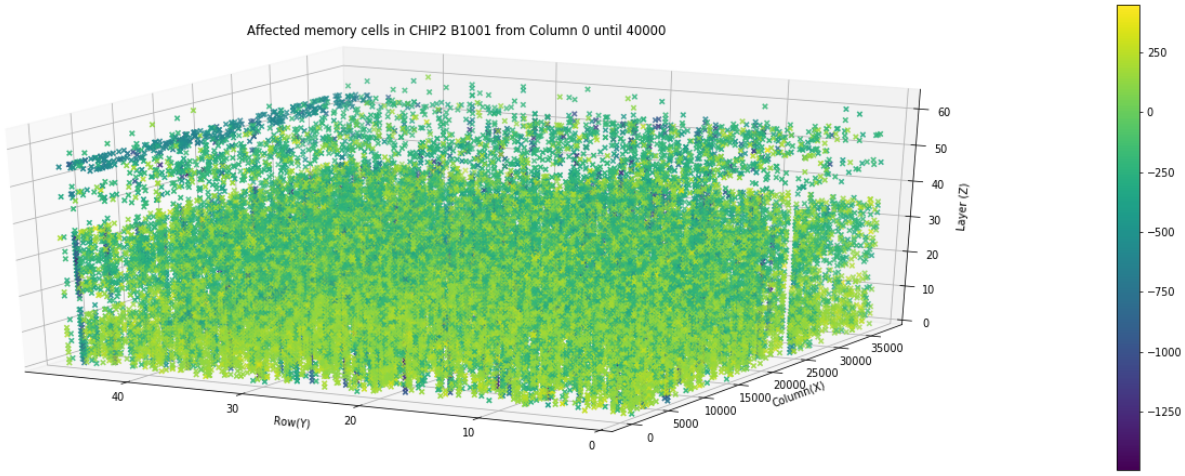
Figure 4.6: Filtered data of CHIP2 B1000 Row14 with different SD filters

4.4. AFFECTED PILLARS

By using the filtered data, the affected pillars within a memory block can be highlighted. Figure 4.7a shows the affected pillars and their threshold voltage shift for block B1000. From the pillar analysis, it can be observed that the upper layers (around layer 60) show a positive threshold voltage shift. To determine the direction of irradiation, block B1001 is shown in Figure 4.7b. For block B1001, the memory cells with a positive threshold voltage shift are located in the lower layers (around layer 5).



(a) Block 1000



(b) Block 1001

Figure 4.7: Affected pillars in memory CHIP2

Block B1000 and block 1001 are placed next to each other, but show distributions of threshold voltage shift which are mirrored in the xy-plane. An explanation for this phenomenon can be found in the physical architecture of the memory block and the evolution from planar to 3D memory devices. Figure 4.8 shows the evolution of planar NAND memory to 3D NAND memory.

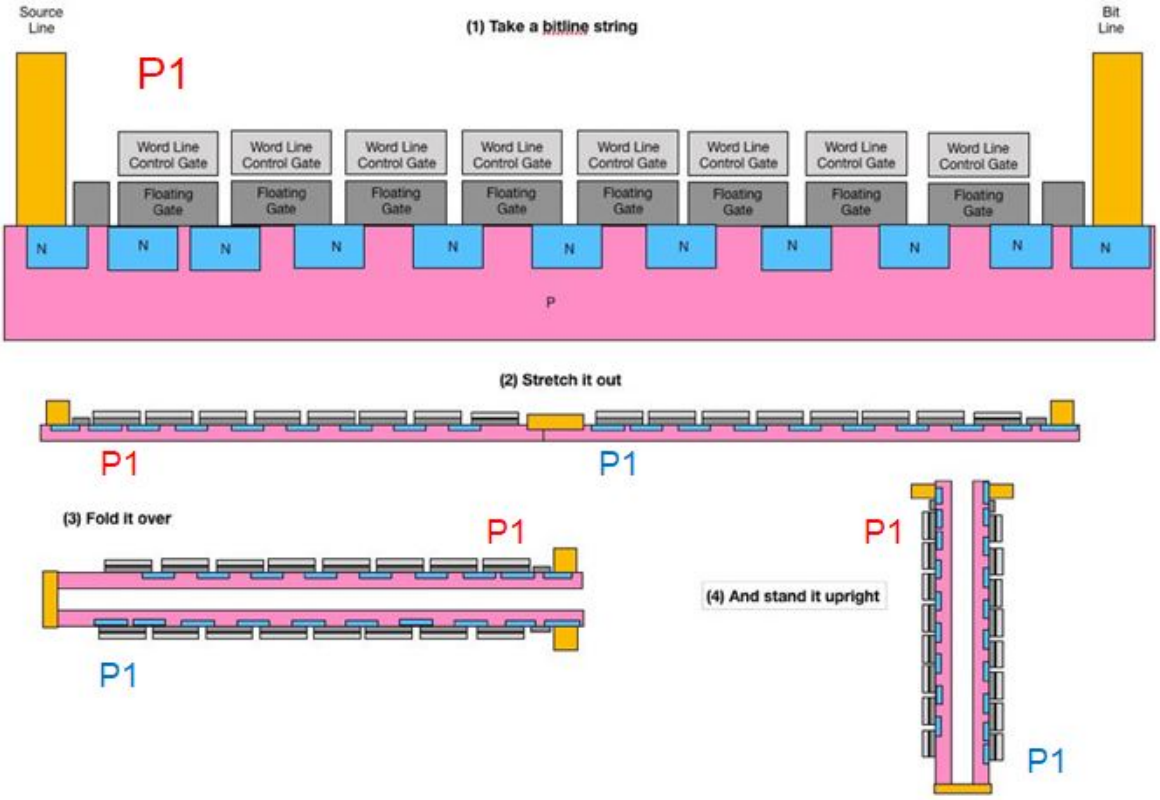


Figure 4.8: Explanation of mirrored structure from evolution into 3D NAND memory

Suppose the first page of memory block B1000 is shows in red and the first page from memory block B1001 is shown in blue. In a planar memory structure the blocks are next to each other with a repetitive pattern of page allocation. However, after the evolution into the 3D memory structure, the cells are folded into a U-shape. If the page order remains through this evolution, then the first page of block B1000 is on top while the first page of block B1001 is on the bottom of the U-shape. This could explain the mirrored pillar distribution as shown in Figure 4.7.

4.5. Comparison with literature

The Reliability and Radiation Effects on Advanced CMOS Technologies (RREACT) group has analyzed the effect of different heavy-ions on 3D NAND memory. In [1], Bagatin shows radiation results of the predecessor of the B17A chip. The test beam energies used were 109 MeV, 157 MeV, 220 MeV and 266 MeV for oxygen, silicon, nickel and silver ions respectively. The results from Bagatin's paper are compared with the results from this Chapter. Figure 4.9 shows the Threshold voltage distribution before and after nickel irradiation ans shows similarities with the previously presented threshold voltage distributions.

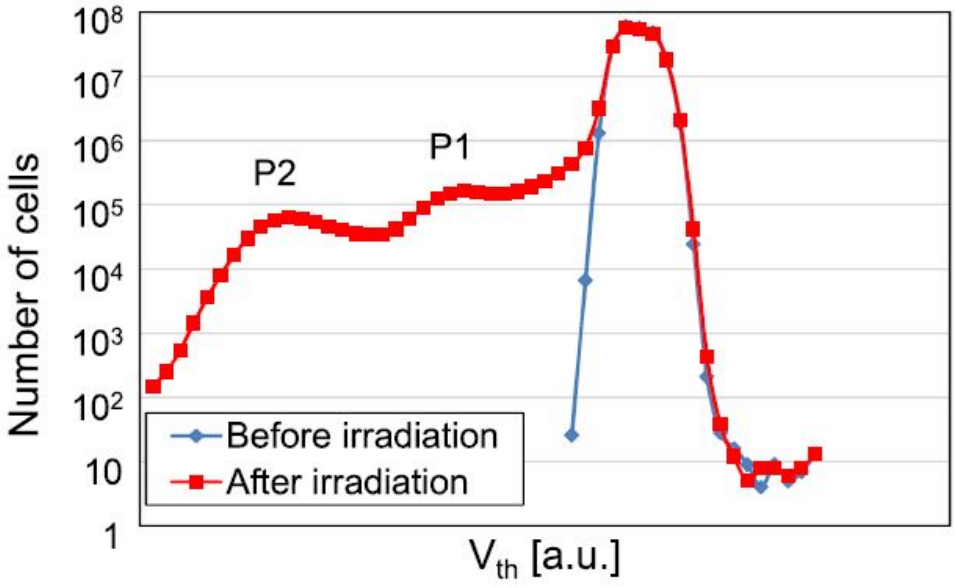
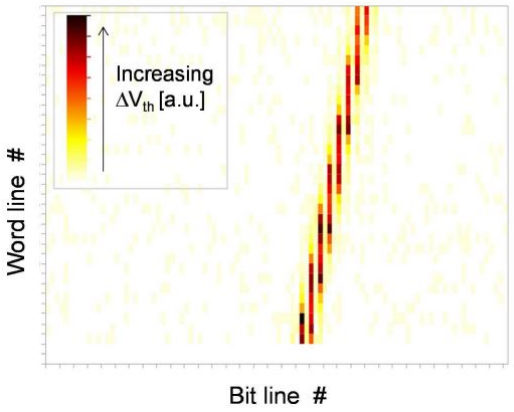


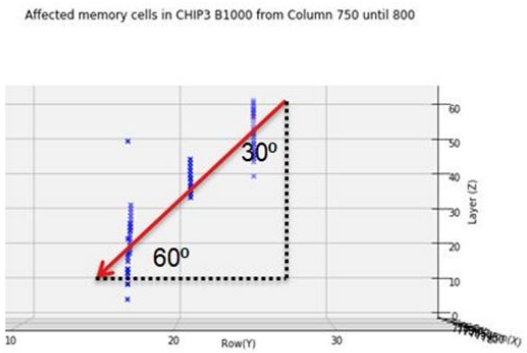
Figure 4.9: Distribution of threshold voltages after Nickel-ion irradiation.[1]

A tail and peak is present in both threshold voltage distributions, however, Bagatin presents two distinctive peaks, denoted by P1 and P2. The threshold voltage distribution from the B17A chip only shows one distinct peak and for some blocks a graduate tail distribution. Since Bagatin's voltage distribution shows no numerical values for the voltages, it is not possible to determine whether the B17A chip's peak is closer to P1 or P2. It should be noted that the B17A chip was programmed to L7 while the chips used by Bagatin were programmed to L5.[1]

Another comparison can be made on the physical mapping of the memory block. In the paper by Bagatin, a chip was irradiated with an incidence angle of 30°. The memory cells that are affected by radiation under a 30° as presented in the paper of Bagatin is shown in Figure 4.10a. CHIP3 which was also subjected to a radiation beam under a 30° angle has its affected memory cells shown in 4.10b.



(a) Bagatin [1]



(b) B17A CHIP3

Figure 4.10: 30 ° track comparison between [1] and tested B17A CHIP3.

Similarities can be seen between both Figures, with a clear track of the radiation particles in the memory cells. The main difference is the gaps shown in the B17A mapping of CHIP3. Since the mapping to the physical layout from the logical pages was done using an assumed structure, the actual memory cells could offset by a couple of rows.

5
Monte Carlo Simulations

In this Chapter, the Monte Carlo simulations are presented. The effect of radiation on electronics is a rather analytically unpredictable process, as the interaction between radiation particles and materials is stochastic. Monte Carlo methods give an insight of the effects by simulating a large number of events and estimate the effects with statistics.

5.1. Geant4: A simulation toolkit

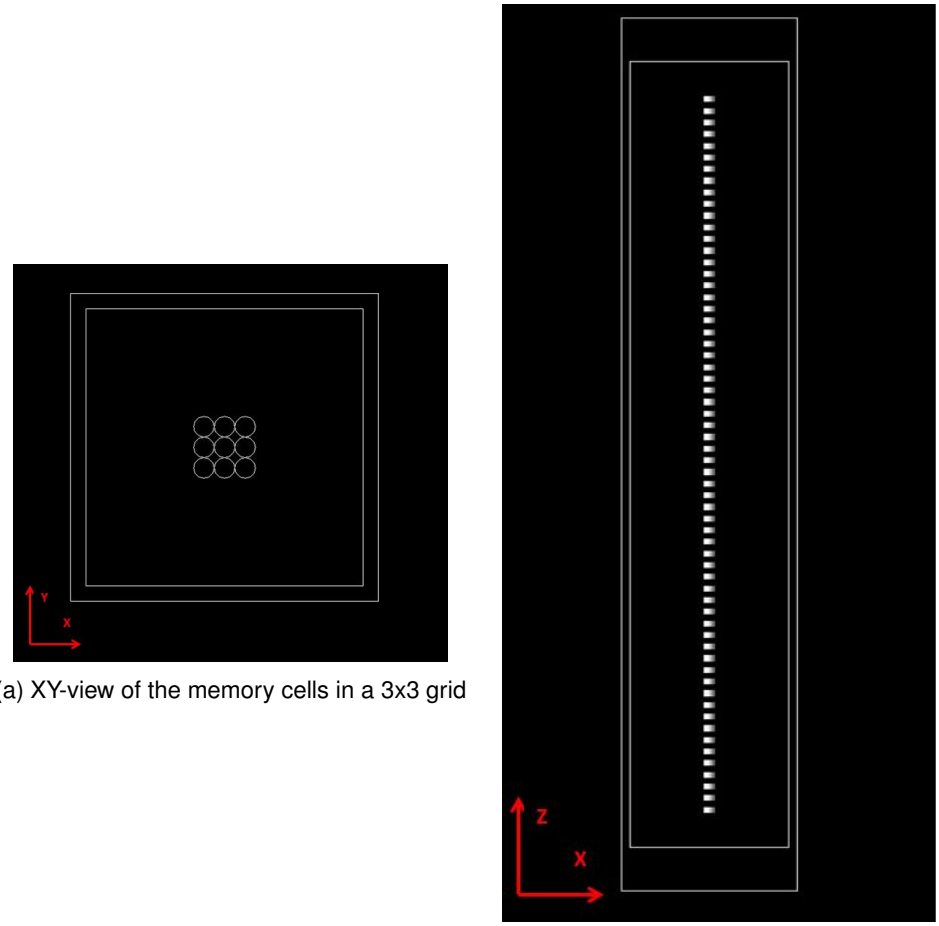
Geant4 [4] is an open-source toolkit programmed in C++. The toolkit finds its application in nuclear, high energy and accelerator physics as well as space and medical science.

Within the Geant4 toolkit multiple variables need to be specified to run a simulation. A section of the memory block is created in the geometry class of the toolkit. A detailed description of the created geometry is discussed in Subsection 5.1.1. The physical interaction an processes between the material and the particles are defined in physics list. For the discussed simulation in this Chapter, the electromagnetic and hadronic processes are used for particle interaction.
Different terms are defined within a simulation. For clarity the units are explained below:

- **Run**: A Run is the largest unit of the simulation and consist of multiple events. The events within a run are simulated with identical conditions, ie. the geometry nor the physical interactions cannot be changed in between events.
- **Event**: An Event starts by placing a particle at a starting point and its trajectory and interaction with matter is tracked. The starting point can be different for every Event in a Run.
- **Track**: The Track unit is a snapshot of the particle as it moves to the simulated geometry. The Tracks of the simulated particles can be saved in a list with trajectories and visualized.
- **Step**: A step is the smallest unit in the simulation. It consist of a pre-step and post-step point. It contains particle information as well as the volume and material information.

5.1.1. Geometry

The geometry of the memory cells is made from scratch in Geant4. Figure 5.1 shows the geometry from the XY-(topview) and XZ-plane (sideview).
To create a geometry in Geant4, a Logical Volume as well as a Physical Volume needs to be defined. The Logical Volume describes the dimensions, shape and density of the geometry, while the Physical Volume controls the location and rotation.
For the memory chip a World Volume is created which is a Physical Volume with dimensions $3\mu m$ x $3\mu m$ x $15\mu m$. In this World Volume, an envelope is placed which helps confine the memory cells into pillars. The envelope volume has a width, depth and height of $2.7\mu m$ x $2.7\mu m$ x $13.5\mu m$, respectively.
The memory cells are placed within the Envelope Volume and a total of nine pillars are created in a 3x3 grid, each with 62 layers of memory cells. One memory cell is a radius of $0.098\mu m$ and a height of $0.1\mu m$. The spacing between two memory cells in width and depth is $0.005\mu m$ and the spacing in height is $0.1\mu m$. These values are estimated from [2].
Although the memory cells have multiple layers of different material in the radial direction, the exact composition and dimension are not available as it is the intellectual property of the manufacturer. For the sake of these simulations the memory cell is simulated to consist of silicon dioxide only, as this is a commonly used material for semiconductors. Figure 5.1a shows the XY-view of the memory cell geometry created in Geant4. The World Volume can be seen as the outer square. The square larger



(a) XY-view of the memory cells in a 3x3 grid

(b) XZ-view of memory cells in a pillar

Figure 5.1: Memory cell geometry in Geant4

than the 3x3 memory grid but smaller than the World Volume is the Envelope. A pillar with its 62 memory cells can be seen in a XZ-view and is shown in Figure 5.1b. Only one pillar of the total nine pillars is shown for clarity.

5.1.2. SCORING VOLUMES

All memory cells and pillars contribute to interactions between material, however, a sensitive volume or scoring volume needs to be identified for which the effects are saved. For these simulation, the center pillar is chosen as sensitive volume, as this pillar will also be affected by neighbouring pillars which will be the case during an actual test. A scoring mesh in the shape of a cylinder is created. The mesh is divided into equal slices to match the number of memory cells in the pillars, such that one slice of the mesh matches exactly one memory cell. Next to defining what the scoring volume is, it should also be defined which quantities are being scored. Table 5.1 shows the quantity names and a short description of scored values.

Table 5.1: Scored quantities

Quantity name	Description	Unit
cCharge	Change in charge in a memory cell	[e+]
dDep	Deposited dose on a memory cell	[Gy]
nCol	Number of collisions within a memory cell	[-]
nSecond	Number of generated secondary particles in a memory cell	[-]

5.2. Simulation scenarios

The simulations were divided into two scenarios: test beam and space environment. The simulations with the test beam as input are performed to mimic the conditions at the CERN radiation test. The space environment simulations are performed to get an insight of the effects on the 3D NAND memory when it is subjected to the space radiation environment.

5.2.1. Monochromatic Pb-208 beam: unidirectional

The test beam simulations were performed with a monochromatic unidirectional Pb-208 beam and an energy of 33 TeV. A total of 1 million events were sampled. The radiation direction was along the z-axis and from layer 62 down to layer 0. The starting point in the xy-plane was randomized. Figure 5.2 shows a snapshot of the simulation with 10 events drawn, with the tracks and hits shown.

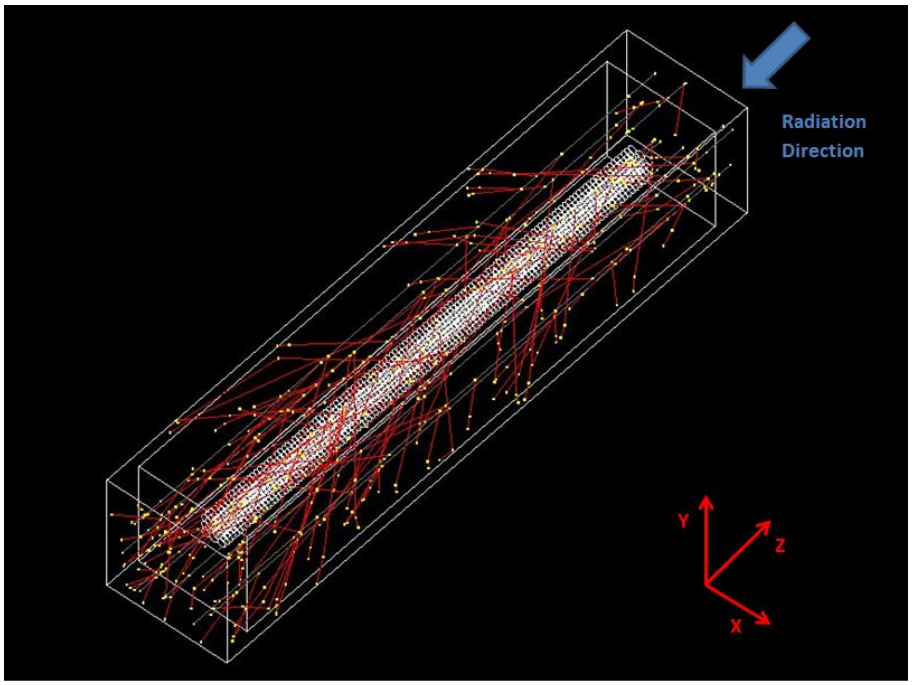
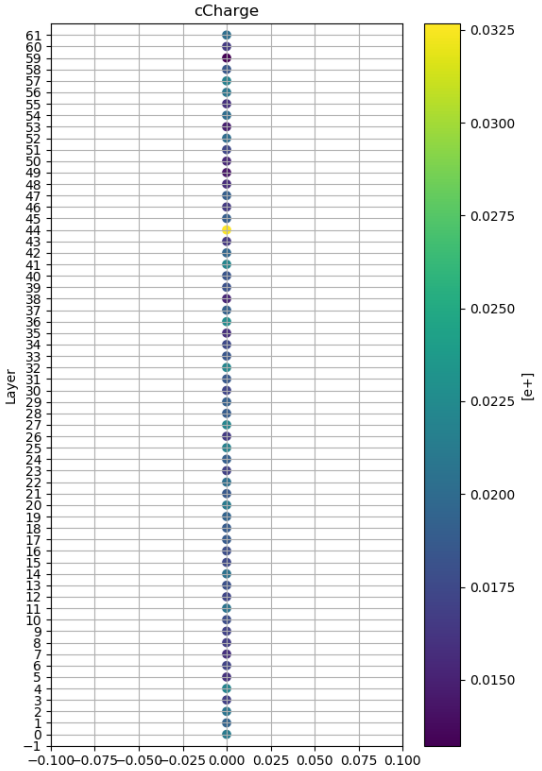
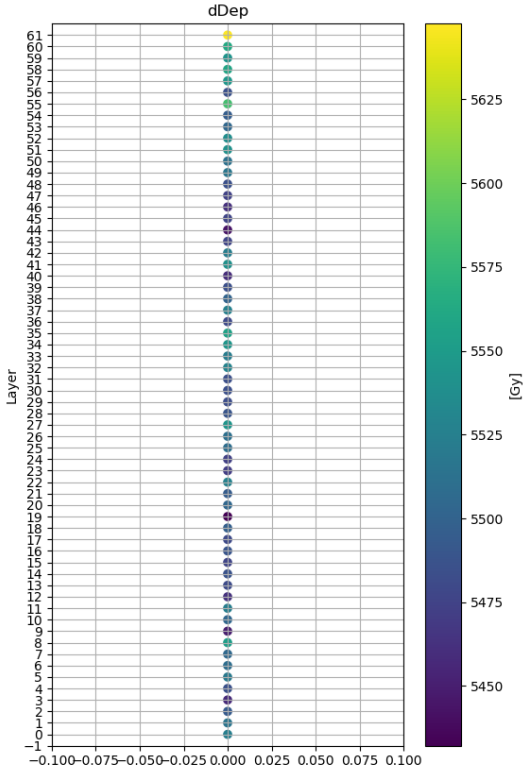


Figure 5.2: Unidirectional beam (Pb-208, 33 TeV) with 10 events simulated

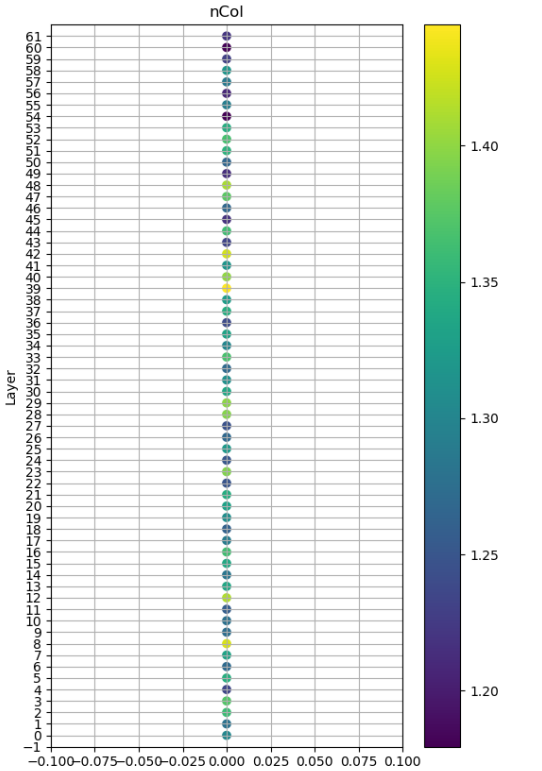
The scored quantities are accumulated over the number of events and stored by Geant4. The results are normalized by dividing the accumulated scored values by the number of particles that enter the corresponding memory cell. This leads to average values per memory cell in all the 62 layers. The average charge, deposited dose, number of collisions and number of generated secondary particles are shown in Figures 5.3a, 5.3b, 5.3c and 5.3d.



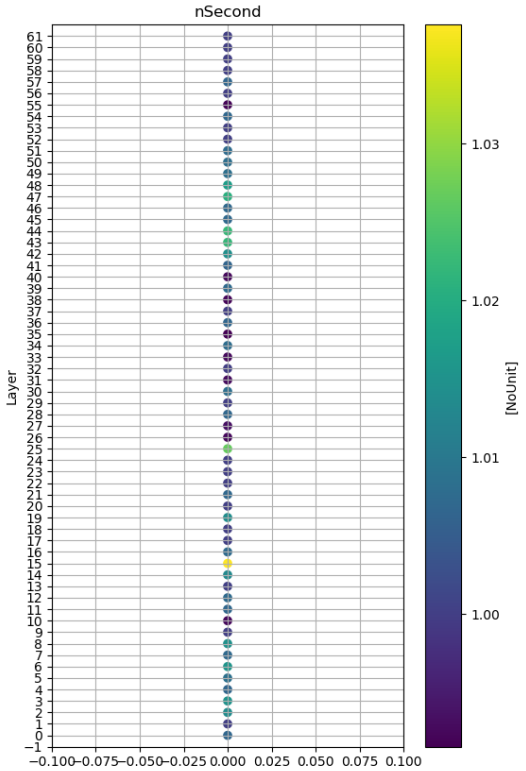
(a) Charge per memory cell



(b) Deposited dose per memory cell



(c) Number of collisions within a memory cell

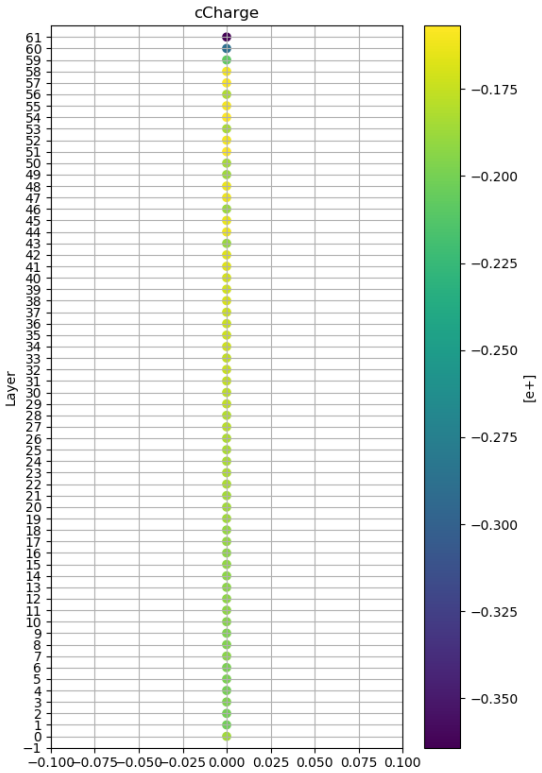


(d) Number of generated secondary particles per cell

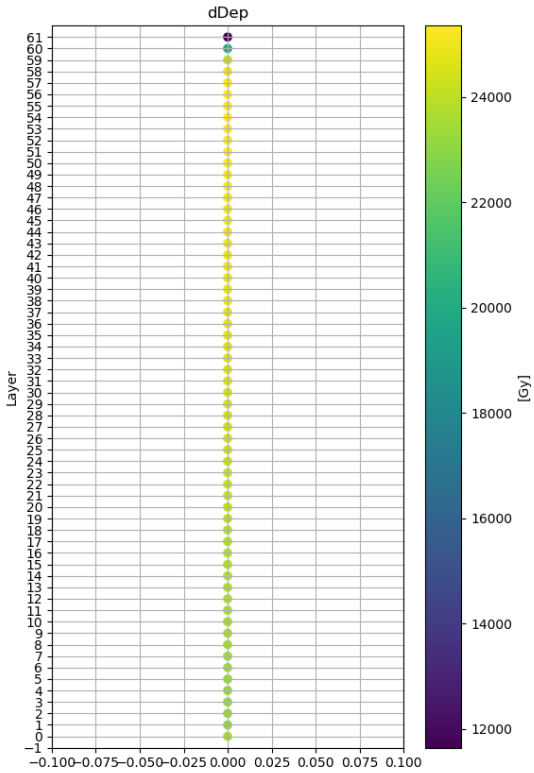
Figure 5.3: Normalized scored quantities for memory stack at test condition subjected to Pb-208 33 TeV

The average charge deposition in the memory pillar for 33 TeV beam is normally distributed. The deposited dose is highest for the first cell hit (5650 Gy), and remains relatively high for the first 5 layers hit. As the particle propagates though lower layers, the deposited dose tend to drop as low as 5450 Gy.
No clear pattern can be seen in either the number of collisions in the memory pillar nor from the number of generated secondary particles. Overall, secondary particles are created along the memory pillar without any bias for the highest number of created secondary particles.
The result of this effect might be that the created secondary particles cause the pillar to be irradiated from the inside. This would explain the normal distributed deposited dose along the memory pillar.

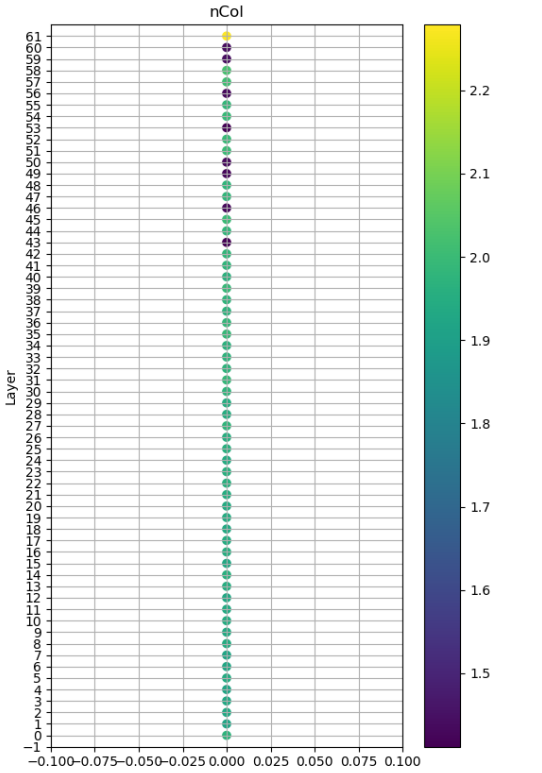
The same simulation was run a second time with a lower beam energy of 210 MeV, to get an insight in the varying energies affecting the memory cells. The results for a memory stack subjected to Pb-208 with 210 MeV are shown in Figures 5.4a, 5.4b, 5.4c and 5.4d.
The deposited dose and charge distribution for the 210 MeV beam show a similar pattern. The lowest value for the first layer(62), high values in the middle layers(20-50) and middle/high values for the lowest layers(0-10). This can be related to the neighbouring pillars. On first contact with a pillar, the particle can scatter though underlying layers, even from other pillars.
The simulations with two different monochromatic beams, show the difference in deposited dose in the memory cells. For Ultra High energies, in the order of TeV, the memory stack shows that the upper layer (first memory cell affected) shows the largest dose deposition, while for lower beam energies it is vice-versa. For low energy beams, the first hit layer shows the least deposited dose of the memory stack. This is likely the cause of secondary particles being the primary factor of the deposited dose. This is also verified by the number of secondary particles created, which is the highest for the first hit memory cell. For the Ultra High Energy beams, the secondary particles have a small contribution to the deposited dose. The generation of secondary particles for Ultra High Energies is also normally distributed along the memory pillar.



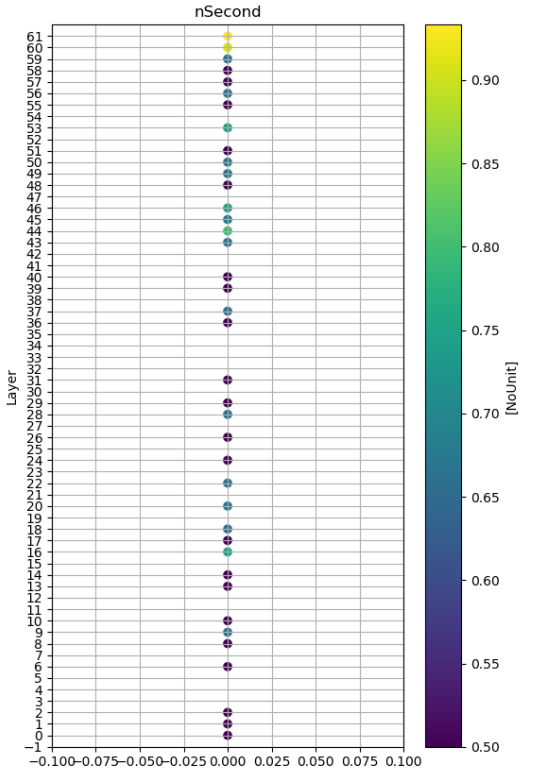
(a) Charge per memory cell



(b) Deposited dose per memory cell



(c) Number of collisions within a memory cell



(d) Number of generated secondary particles per cell

Figure 5.4: Normalized scored quantities for memory stack at test condition subjected to Pb-208 210 MeV

5.2.2. Space Environment: omnidirectional

The main difference between the space environment and the test environment lies in the initial particle initialization. For the space environment, the particles are created randomly around the pillars for every event. For the space environment protons and lead (Pb-208) ions are the used particles for the simulations. Protons are the most dominant particle in GCR and Pb-208 is chosen as heavy-ion to compare with the radiation test results. For the space environment simulations, GCR are the only source of radiation. Three different space environment are simulated. A LEO, GEO and Mars mission (Areosynchronous equatorial orbit) scenario are considered. The LEO and GEO missions are more suitable for small satellites, while the Mars simulation explores the possibility of using the space radiation monitor for interplanetary environments. To simulate the different mission parameters in Geant4, a General Particle Source(GPS) macro file needs to be created. The GPS files are created using SPENVIS[5], an online tool created by ESA for orbit analysis and supporting programs such as Geant4. Several inputs are required by SPENVIS to create the orbit. The following parameters are the same for all three mission profiles:

- **Mission duration**: 1 year
- **Solar radiation pressure**: 0 $m^2 kg^{-1}$
- **Orbit start**: 01-01-2020
- **Eccentricity**: 0
- **Inclination** : 0 deg
- **right ascension of the ascending node**: 0 deg
- **Argument of periareion**: 0 deg
- **True anomaly**: 0 deg

The parameter which varies for the three missions is the semi-major axis. Table 5.2 shows the semi-major axis used for the orbit generation in SPENVIS.

Table 5.2: Semi-major axis of the selected orbits

Orbit	Semi-major axis
LEO	6708 km
GEO	42.164 km
AEO	20.428 km

For the space environment simulation, 1 million particles are simulated for each run. After every run, the scored quantities are saved. The scored quantities output the accumulated results of the 1 million events. To compare the data with the test environment simulation, the data is normalized by dividing the accumulated values in each memory cell by the number of times a track has passed though that memory cell. Figure 5.5 shows the memory pillar subjected to omnidirectional radiation.

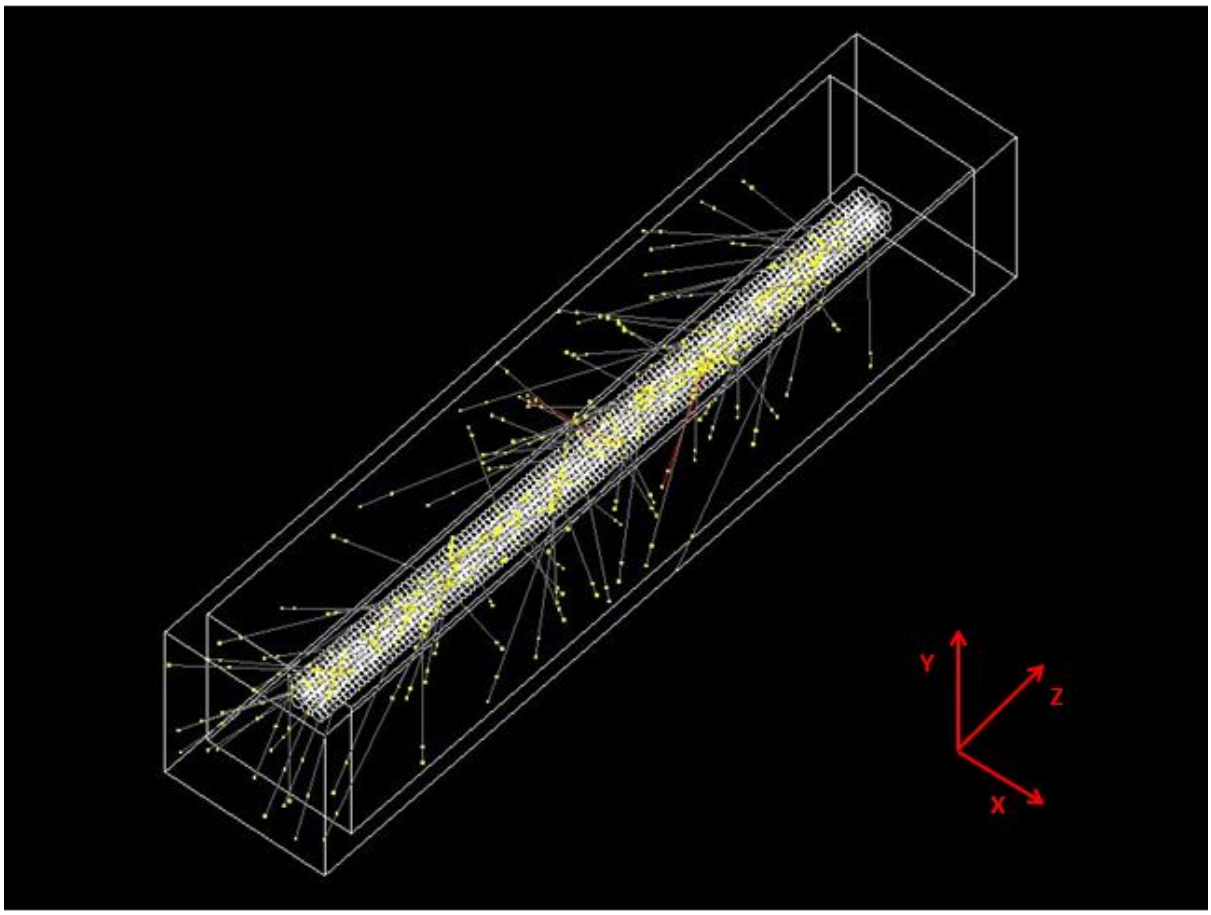
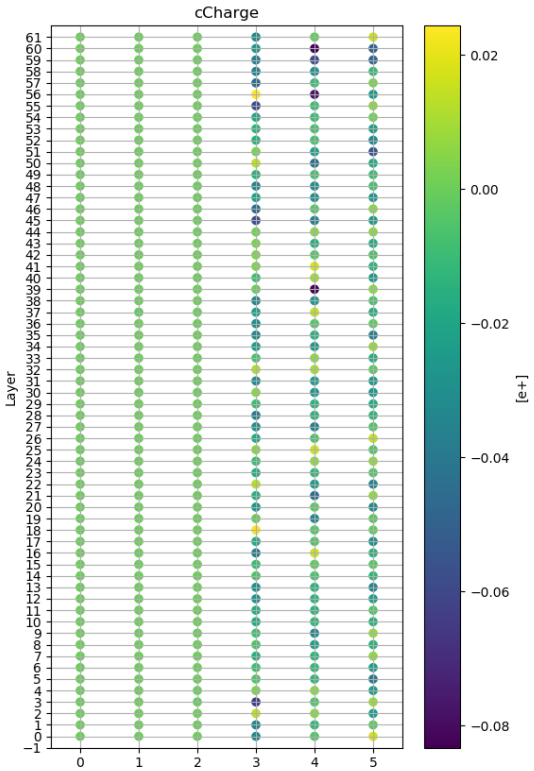


Figure 5.5: Geant4 simulation on memory stack with omnidirectional radiation.

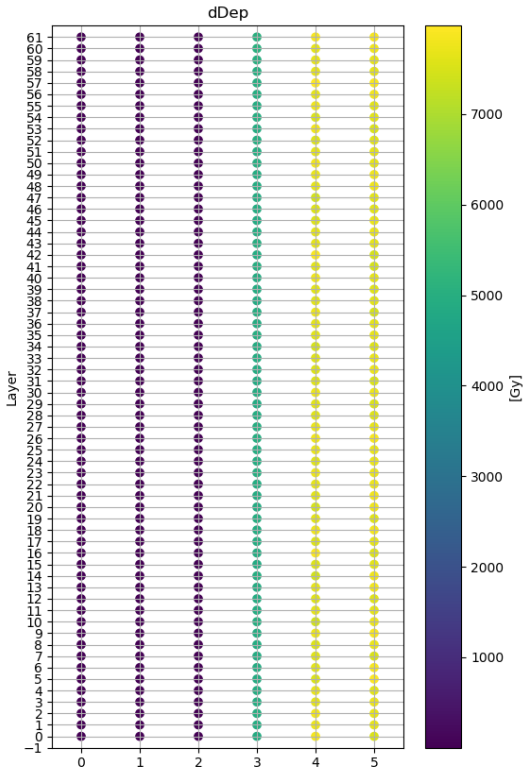
The results of the simulations are summarized in Figure 5.6. Every index of Figure 5.6, refer to a different orbit and particle combination. Table 5.3 shows the indices with their corresponding simulation parameters.

Table 5.3: Simulation conditions for every index.

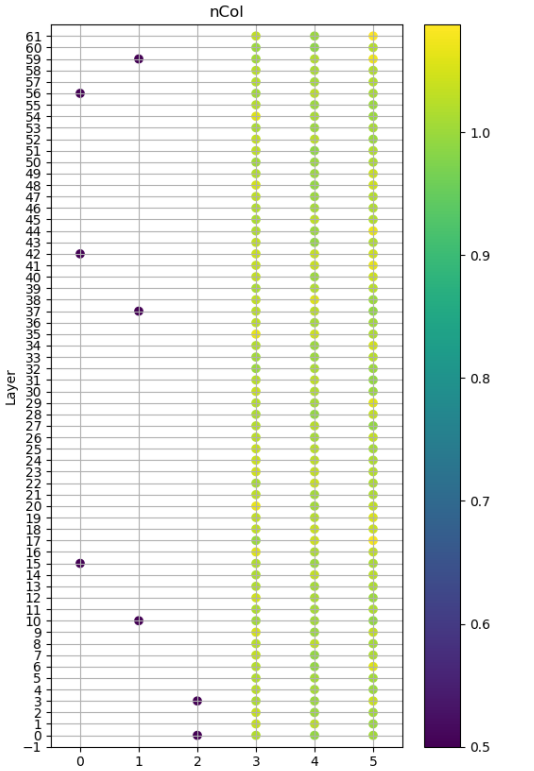
Index	Orbit	Particle
0	LEO	Proton
1	GEO	Proton
2	AEO	Proton
3	LEO	Pb-208
4	GEO	Pb-208
5	AEO	Pb-208



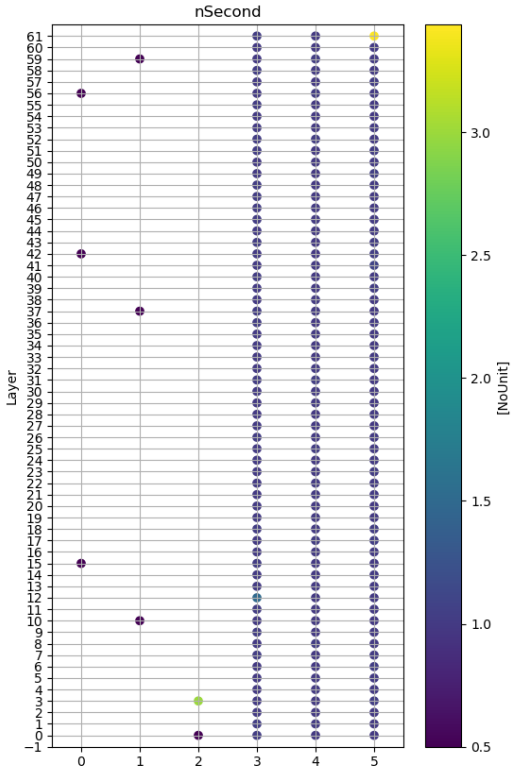
(a) Charge per memory cell



(b) Deposited dose per memory cell



(c) Number of collisions within a memory cell



(d) Number of generated secondary particles per cell

Figure 5.6: Normalized scored quantities for memory stack at space conditions subjected to protons and Pb-208.

The Figures of 5.6 shows the normalized scored quantities, with the layers on the y-axis and the indices on the x-axis. The first three pillars present the result of proton irradiation for LEO, GEO and AEO. Pillars 3 to 5 show the results of Pb-208 irradiation at LEO, GEO and AEO.
The differences between proton and Pb-208 irradiation are clearly visible. Proton irradiation show less little to no change in the charge of the memory cells and lower deposited dose on the memory cells.
This makes the space radiation more useful as radiation monitor for heavy-ions than protons. The proton irradiation also show very little collisions within memory cells and almost no creation of secondary particles in the memory cells.
When observing the difference between the orbits, it can be seen that the LEO orbit shows deposited dose in the range of 4000 Gy to 6000 Gy, while the deposited dose for GEO and AEO are around 7000 Gy. This difference is as expected as spacecrafts in LEO are more subjected to trapped particles in the Van Allen belts. More detailed results of the simulations per orbit can be found in Appendix B.

6

PRELIMINARY DESIGN OF A RADIATION MONITOR BASED ON 3D NAND

In this Chapter, the preliminary design of a 3D NAND flash memory as space radiation monitor is presented. This includes an initial mass and dimension sizing as well as a power budget.

6.1. FUNCTIONAL ANALYSIS

The functions of a low-cost space radiation monitor are shown in the Function Flow Diagram in Figure 6.1. The space radiation monitors function start with a memory chip affected by radiation. At a certain

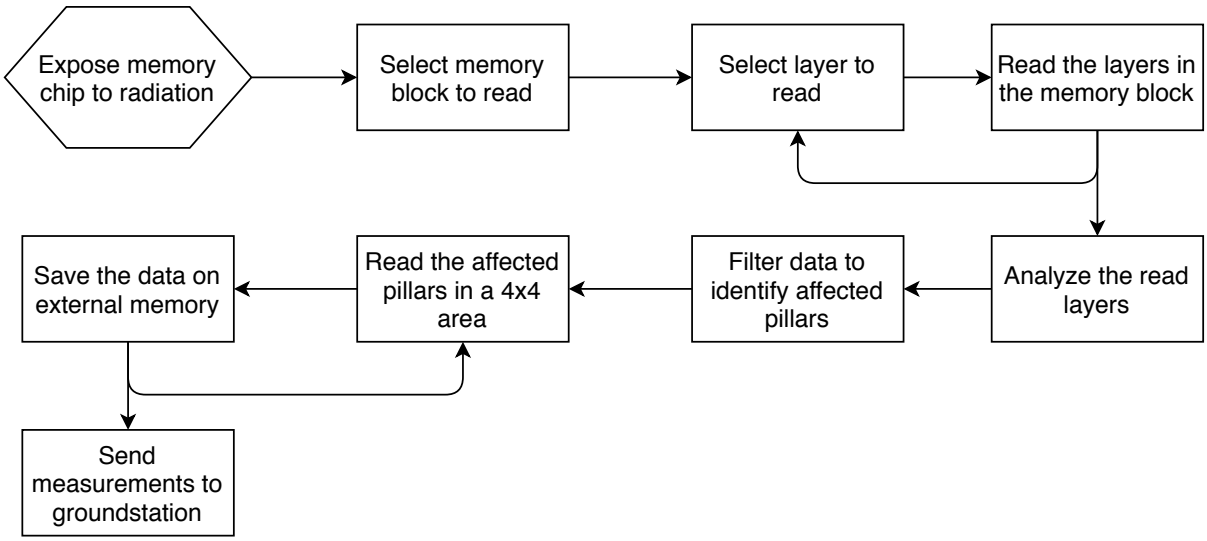


Figure 6.1: The Functional Flow Diagram of the space radiation monitor.

time interval, the measurement procedure can start. The chosen measurement method is the combined page by page read and binary search method. First the FPGA selects a memory block to read. Then a couple of layers are read to obtain a general overview of the affected memory block. The read layers are analyzed by the processing logic of the FPGA and filter to obtain the affected pillars. Then a more detailed scan around the pillars is performed to get an accurate measurement of the threshold shift in the pillars. The overall scan of the layers and the detailed scan of the pillars is saved on an external memory and send to a groundstation when possible for further analysis.

6.2. REQUIREMENTS

For the preliminary design of the radiation monitor, several initial requirements were posed. The requirements are based on the performances of the Miniature Radiation Monitor (MRM) from ESA[42], since the radiation monitor based on 3D NAND should have comparable or even better specifications than existing space radiation monitors. The requirements are used in this Chapter for the trade-off of different components. The initial requirements for the space radiation monitor are given in Table 6.1, during the detailed design of the space radiation monitor the requirements can be adjusted according to the demands of the stakeholders.

Table 6.1: System requirements of the radiation monitor

Requirement identifier	Requirement description
RAD-MAS-01	The mass of the radiation monitor system shall not be greater than 100 grams.
RAD-VOL-01	The volume of the radiation monitor shall not exceed 30 cm^3.
RAD-POW-01	The power consumption of the radiation monitor shall not exceed 100 mW.
RAD-COS-01	The total costs of the radiation monitor shall be less than 30 kEuros.
RAD-HAR-01	The non-sensitive volumes of the radiation monitor shall be radiation hardened up to a TID of 100 krad(Si).

6.3. Proposed components

To accommodate the function from Figure 6.1, the following components are required:

- **FPGA**: Used to perform the operations and data processing.
- **3D NAND memory chip**: Used as sensitive volume. This memory chip will be exposed to radiation and changes in threshold voltages will be measured.
- **Voltage regulators**: Used to apply to prescribed voltages to the 3D NAND memory chip and the FPGA from the satellites main power system.
- **External memory**: Used as data storage for measurement results.
- **PCB**: A custom Printed Circuit Board is required on which the components are soldered on.

For the FPGA and the external memory, multiple components are considered. A trade-off is performed to determine the components of the conceptual design.

FPGA

For the FPGA, three different components are considered. The first chip is the Zynq-7000 which is used in the ZedBoard. The second chip is the Virtex-4QV, which is made from the same manufacturer as the Zynq-7000. The third chip considered is the RTG4 Radiation-Tolerant FPGA made by Microsemi. The following criteria have been selected for the FPGA trade-off based on the requirements:

- **Mass**: The mass of the component.
- **Size**: The size of the component.
- **Power**: The estimated power consumption of the component.
- **Software development cost**: Cost to develop the required software to program the FPGA as memory controller.
- **Radiation Hardness**: The amount of total ionizing dose the component can absorb for guaranteed operations.

The cost of the Virtex-4QV and RTG-4 are not publicly available, instead the software development cost are considered. Adjusting the software to another FPGA will increase the cost and risk of the component. The criteria are all weighted equally. A trade-off is performed with a graphical trade-off table shown in Table 6.2, with the width of the columns representing the weight of the criterion.

Table 6.2: FPGA trade-off table. Green[++]:Excellent, exceeds requirements. Blue[+]: Good, meets requirements. Yellow[-]: Correctable deficiencies. Red[- -]: Unacceptable.

		Criterion				
		Mass	**Size**	**Power**	**Software development cost**	**Radiation Hardness**
Option	**Zynq-7000**	11.6 grams [++]	0.36 cm^3 [++]	2760 mW [1] [- -]	Software has already been developed for the ZedBoard [+]	TID 0 krad(Si) [- -]
	Virtex-4QV	34 grams [+]	7.84 cm^3 [+]	955 mW [2] [- -]	Software needs to be adjusted from the ZedBoard [-]	TID 300 krad(Si) [++]
	RTG-4	32 grams [+]	5.2 cm^3 [+]	1285 mW [3] [- -]	Different manufacturer, different software required [- -]	TID 100 krad(Si) [+]

From the trade-off table it can be seen that the Zynq-7000 outperforms the other two FPGAs on most criteria. However, the Zynq-7000 is not radiation tolerant and has a huge estimated power consumption. To estimate the power usage of the Zynq-7000, the voltage over pins J21 of the ZedBoard is measured during the read-out procedure. The pins J21 is connected to a 10mOhm resistor. The measured voltage on the pins is 2.3mV,which results in a current of 230mA. The input voltage of the ZedBoard is 12V, multiplying with the current of 230mA results in a power consumption by the ZedBoard of 2.76W. The power consumption from the other two FPGAs have estimated by using the a power estimator tool from their respective manufacturer. All three FPGAs have acceptable mass and size properties. The memory controller on the ZedBoard is written for Zynq-7000.
The Virtex-4QV is made by the same manufacturer and uses the same software to program the FPGA. Small adjustments are likely required to program the Virtex-4QV as a memory controller. The RTG-4 is from Microsemi and thus uses a different software to program their FPGAs. This will add to the software development cost when this FPGA is selected as the already developed software for the ZedBoard needs to be heavily modified or rewritten. Unfortunately, none of the FPGAs satisfy the power requirement. For this conceptual design the Virtex-4QV is chosen as it has the lowest estimated power consumption. Depending on the mission and stakeholders, the power requirement might be negotiable. Another options to reduce the power consumption is to optimize the FPGA as memory controller.
The Virtex-4QV from Xilinx is the chosen FPGA for the space radiation monitor. [43] Since both FPGA are from Xilinx, there is no need to rewrite the software of the readout scheme. Table 6.3 shows the

[1] Measured from ZedBoard
[2] Estimated using the power estimation tool from Xilinx (https://www.xilinx.com/products/silicon-devices/fpga/virtex-4qv.html)
[3] Estimated using the power calculator from Microsemi (https://www.microsemi.com/product-directory/design-resources/1748-power-calculator)

difference in specs between the chips.

Table 6.3: Comparison between Development Board FPGA (Zynq-7000) and proposed FPGA (Virtex-4QV).

	Zynq-7000	Virtex-4QV
Partnumber	XC7Z020	XQR4VFX140
Block RAM	4.9Mb	9.9Mb
Logic Cells	85K	142K
Clock speed	866MHz	400MHz
Size	15mmx15mm	40mmx40mm

The characteristics of the radiation tolerance of the Virtex-4QV chip are shown in Table 6.4. The chip is guaranteed to be radiation tolerant for a Total Ionizing Dose of atleast 300krad(Si). The chip is immune to Single-event Latchups for at least 100 $MeV - cm^2/mg$. The estimated Single Event Functional Interrupts are estimated to be 1.5E-6 upsets per device per day.

Table 6.4: Radiation tolerance characteristics of Virtex-4QV chip

Symbol	Description	Min	Typical
TID	Total Ionizing Dose, dose rate 50 rad(Si)/sec	300 krad(Si)	-
SEL	Single-event latch-up immunity, Heavy ion linear energy transfer (LET)	100 LET $MeV - cm^2/mg$	-
SEFI	Single-event functional interrupt, GEO 36000 km typical day	-	1.5E-6 Upsets/device/day

Another advantage of using the Virtex chip is the ability to reconfigure the FPGA at no cost during the design cycle. Figure 6.2 shows the interaction with re-programmable logic to accommodate change in during the design cycle.

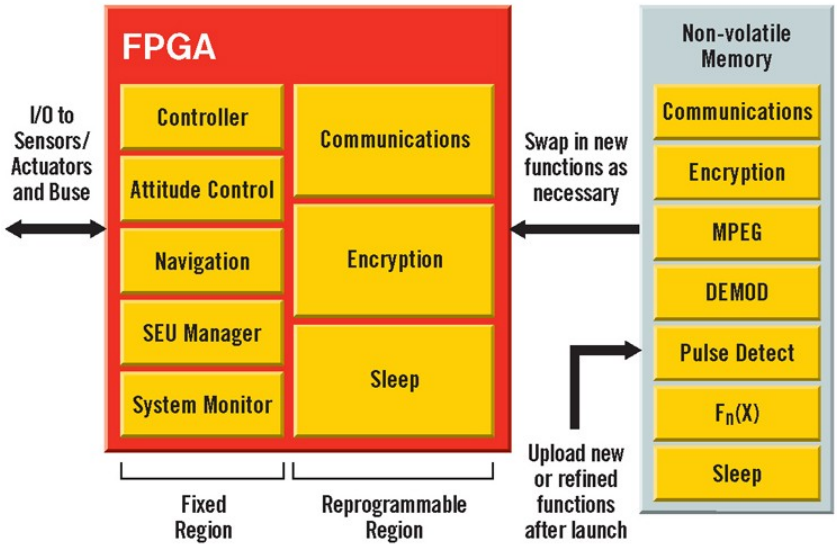


Figure 6.2: Functional block diagram of the re-programmable Virtex-4QV

The FPGA holds a set of fixed functions which cannot be altered. However, there is a region within the FPGA which can be re-programmed if necessary. Functions can even be added after launch, by uploading functions to a non-volatile memory and swapping or updating existing functions on the FPGA. This functionality of the FPGA is a benefit for the risk and cost of the system.

3D NAND CHIP

The proposed 3D NAND chip to use as sensitive volume and thus as monitor, is the B17A from Micron. The chip is chosen, since it is the same chip that has been used in the development of the space monitor. For this chip, the datasheet is available and the readout schemes are tested and verified. A collaboration with the manufacturer is recommended to get better insight in the actual physical properties of the chip. This can lead to more accurate Monte Carlo simulations, as the geometry can be modeled more accurately.

Other chips can also be considered. The B17A is a rather old chip in the fast growing market of 3D NAND flash memory. The chip might be obsolete when the space radiation monitor is ready for launch or newer chips might outperform the B17A. The trend of squeezing more memory in smaller dies continues while the number of layers also continue to grow. By the time the space monitor is ready for deployment, chips could be available with 200+ layers. The newer chips should be taken into consideration as they have more sensitive volumes allowing for more measurements. The increase in memory cells to measure can also increase the processing time.

VOLTAGE REGULATOR

The voltage regulator is needed to provide the correct voltages to the FPGA and the memory chip. The FPGA allows for an input voltage of 3.3V while the memory chip needs a supply voltage of 1.8V. It is assumed that the satellite provides a voltage between 1.5V and 7V for the space radiation monitor and Only a 3.3V power output is available from the satellite main power system to the space radiation monitor The chosen voltage regulator is the TPS7H1101A-SP Radiation-Hardened LDO Regulator from Texas Instruments.[44] An overview of specs of the LDO is shown in Table 6.5.

Table 6.5: TPS7H1101A-SP LDO specs

Parameter	Value
V_{in}	1.5-7 V
V_{out}	0.8-6.65 V
Max Current output	3 A
Radiation Hardness Assurance	Up to TID 100 krad (Si)
Single Event Latchup (SEL) Immunity	Up to 85 $MeV - cm^2/mg$
Operating temperature range	-55 ° Celsius to 165 ° Celsius

EXTERNAL MEMORY

The amount of memory required to save the data from one read memory block is 50MB. The memory where the measurement data is stored needs to be radiation tolerant, as it is not desired to have bitflips in the measurement data. This can be achieved by choosing for a radiation tolerant memory chip by design or using a commercially available memory chip with an advanced fault tolerance mechanism and error correction code. Three chips are considered; The Radiation Tolerant Intelligent Memory Stack (RTIMS) by 3D Plus, B17A 3D NAND memory chip by Micron and the Multi-Chip Module (MCM) by Honeywell.

The memory chips are traded-of on the following criteria:

- **Mass**: The mass of the memory chip.
- **Size**: The size of the memory chip.
- **Storage capacity**: The amount of available storage of the chip.
- **Cost**: The cost of the memory chip.
- **Radiation Hardness**: The amount of total ionizing dose the memory chip can absorb for guaranteed operations.

Table 6.6: External memory trade-off table. Green[++]:Excellent, exceeds requirements. Blue[+]: Good, meets requirements. Yellow[-]: Correctable deficiencies. Red[- -]: Unacceptable.

		Criterion				
		Mass	**Size**	**Storage capacity**	**Cost**	**Radiation Hard-ness**
Option	**RTIMS**	16 grams [+]	0.36 cm^3 [++]	4Gb [+]	10 000 Euros [-]	TID 100 rad(Si) [+]
	B17A	1 gram [++]	0.1 cm^3[++]	512Gb [++]	16.50 Euros [4] [++]	TID 0 krad(Si) [- -]
	MCM	Unknown	6.5 cm^3 [+]	64Mb [- -]	Unknown	TID 300 krad(Si) [++]

The properties of the RTIMS chip are obtained from the datasheet. [45] The RTIMS memory chip has acceptable properties, but the price is rather high. A cheaper option is the B17A 3D NAND memory chip from Micron. This chip is also used as sensitive volume for radiation monitoring. Its low weight, cost and volume makes it an interesting candidate. The main drawback is no radiation hardness. The external memory will save the measurement data and should therefore not be corrupted by radiation. The last option is the MCM MRAM from Honeywell. This memory chip stores information using magnetic storage elements instead of charge. The volume, storage capacity and radiation hardness are obtained from the datasheet. [42] The price and mass could not be obtained from the manufacturer website. The available storage on the MRM is quite limited. 64 Gb is equal to 8 MB, which is not enough to store the data from one memory block measurement(50 GB).
The Radiation Tolerant Intelligent Memory Stack by 3D Plus is the memory of choice for the space radiation monitor. The memory is based on SLC NAND Flash technology. The benefit of using NAND Flash as external memory is the ability to use the ONFI[46] commands which are already programmed in the FPGA to read the memory chip affected by radiation.

PCB

The PCB used can be very similar to the PCB from the development test-setup. The main difference with the custom PCB from the development board is that for the conceptual design of the space radiation monitor, it is desired to make the PCB as small as possible. The size of the PCB will mostly be driven by the largest component. Furthermore, it would not be necessary to have the probing and test pins on the board for the final product. The socket from the development PCB can be removed and instead solder the raw3D NAND chip directly onto the PCB, as changing the memory after launch is not possible.

6.4. Dimensions

For the low-cost space radiation monitor, it is desired to have small dimensions, as it promotes miniaturization. Smaller instruments usually lead to lower masses, which reduces the overall cost of the device. The dimensions of the components are obtained from their respective datasheet and the PCB is sized accordingly to make sure that the components fit on the PCB. The estimated dimensions for the components of the conceptual design are shown in Table 6.7.

Table 6.7: Estimated dimensions of the preliminary design

Component	**Dimensions** (LxWxH)
Virtex-4QV (FPGA)	40 mmx40 mmx7.15 mm
B17A chip (3D NAND)	13.9 mmx7.95 mmx0.86 mm
TPS7H1101A-SP (LDO)	25.14 mmx11.26 mmx2.33 mm
RTIMS	31 mmx28 mmx11.2 mm

[4] Quote from Mouser: https://nl.mouser.com/ProductDetail/Micron/MT29F512G08EBHAFJ4-3RA?qs=sGAEpiMZZMsIA2dzklOPMze%252BFs5z9XFVTk9NxO%2F%252B1IAesy8lcqSFqg%3D%3D on 7-11-2019

The PCB is sized to have a length of 80mm, a width of 68mm and a height of 1.4mm. These dimensions allow for all the components to be soldered onto one side with a clearance offset of 5mm from the edge of the PCB to account for mounting options. This is the same size as the custom PCB from the development test setup. Figure 6.3 shows a mock-up of a possible arrangement of components for the low-cost space radiation monitor made in CATIA.[47] The red rectangles represent the 3D NAND memory chips, which will be used as sensitive volumes. The large grey square is the Virtex-4QV FPGA. The orange block is the LDO regulator and the yellow block represents the RTIMS memory storage. Smaller components such as resistors and capacitors are not drawn onto the preliminary design. The final dimensions of the low-cost space radiation monitor measure: 80 mmx68 mmx28 mm

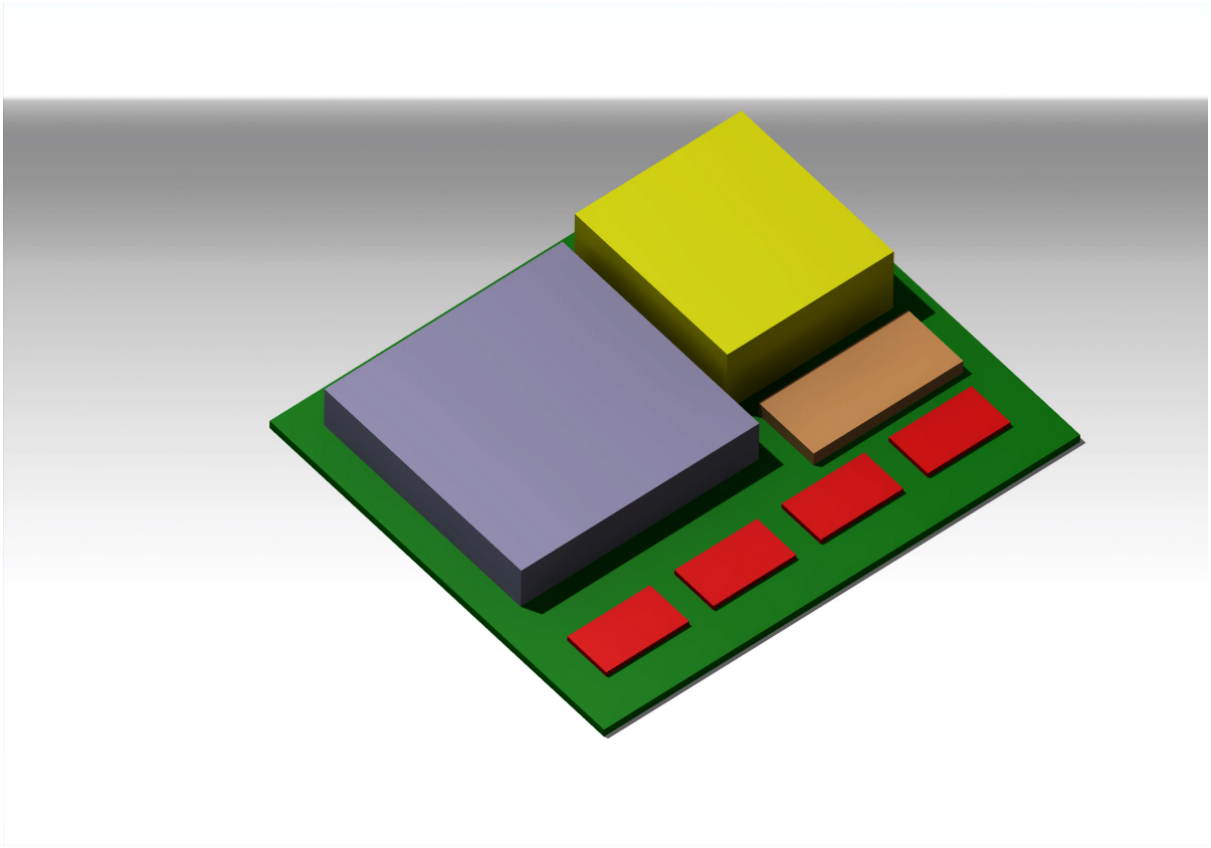


Figure 6.3: Preliminary design of space radiation monitor.

6.5. Mass

The mass is one of the design parameters for any space instrument. By using very small components, the space radiation monitor it designed to have a low mass. The mass of the components are extracted from the datasheet from their respective manufacturer. The weight of the PCB is estimated by weighing the PCB of the development setup, as they have the same dimensions. The 3D NAND memory and PCB were weighted in the workshop. The mass balance of the components and the total mass are displayed in Table 6.8

Table 6.8: Mass budget

Component	Mass
FPGA	34 grams
3D NAND memory	4*1 gram
LDO	15.8 grams
RTIMS	16 grams
PCB	20 grams
Total:	89.8 grams

6.6. Power

The components used for the conceptual design of the space radiation monitor operate on three different voltages. The 3D NAND memory chip which will be exposed to radiation operates at a voltage of 1.8 V. The memory chip that is used as external data storage and FPGA operate both at 3.3 V. The different operating voltages require a voltage regulator. A power diagram is shown in Figure 6.4, which shows how the voltages are is distributed. In this configuration, the system only requires a 3.3 V input voltage from the satellite main power system.

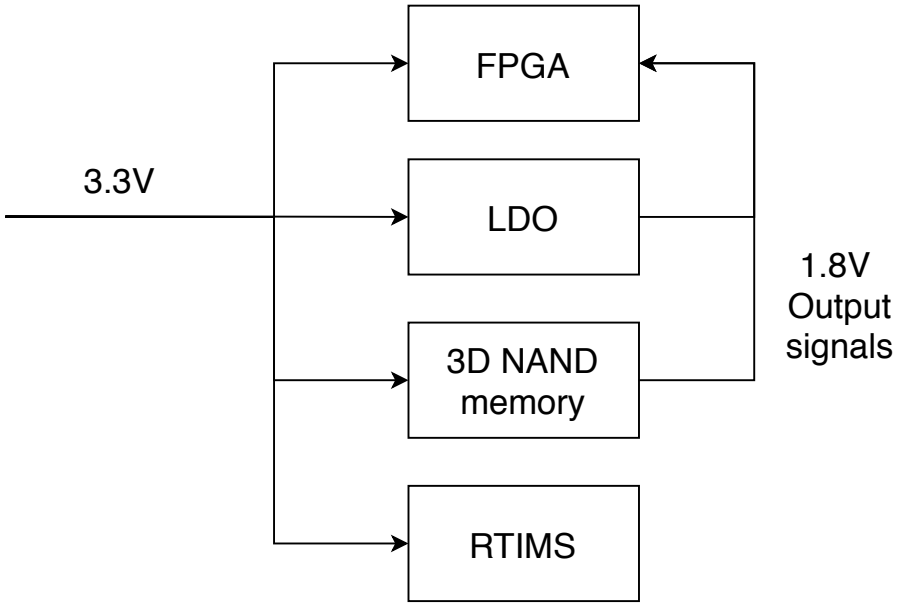


Figure 6.4: Applied voltages to the components on the PCB.

The power consumption of the Virtex-4QV is estimated the power estimation tool form Xilinx.The estimated power is 955 mW. A summary of the estimated power characteristics can be found in Appendix C. The custom PCB is connected to a 5 V power supply. During the read-out operation, the current was measured at 0.002 A. The power consumed by the PCB is 10 mW. The total power consumption is thus estimated to be 965 mW. It should be noted that the ZedBoard is a development board that houses more components than is used for the space radiation monitor. The final power usage is expected to be lower.

6.7. Overview

An overview of the main parameters of the space radiation monitor is given in Table 6.9.

Table 6.9: Overview of the conceptual design specs

Parameter	Value
Mass	89.8 grams
Dimensions (LxWxH)	80 mmx68 mmx28 mm
Power	965mW
Operating voltage	3.3 V
Processing time	20 minutes
Operating temperature	0° Celsius to 70° Celsius
Radiation characteristics	
Radiation Hardness Assurance	TID 100 krad (Si)
SEL Immunity	Up to 85 $MeV - cm^2/mg$

The conceptual design of the space radiation monitor has an estimated mass of 89.8 grams, which includes all the aforementioned components and the PCB. The outer dimensions are 80mmx68mmx28mm, assuming all component are housed on one side of the PCB. Furthermore, the estimated power consumption is 965mW. This has been estimated from the Virtex-4QV power estimation tool and the power consumption of the B17A 3D NAND memory chip as measured during operation. The total time to read memory cells and process the measurements to a threshold voltages is 20 minutes per memory block. The operating temperature is limited by the operating temperature of the B17A chip as prescribed by the manufacturer. The radiation tolerance characteristics are estimated from the lowest values of the selected radiation tolerant components. The LDO and the RTIMS memory have a radiation hardness for TID of 100 krad(Si). The single event latchup immunity of the LDO regulator is the limiting factor, which is 85 $MeV - cm^2/mg$.

7

Conclusions and Recommendations

In this Chapter the conclusions are given in Section 7.1 and the Recommendations are given in Section 7.2.

7.1. Conclusions

A data analysis was performed on three memory chips which were exposed to a Ultra-High energy Pb beam at CERN. Moreover, Monte Carlo simulations have been carried out for different environments and for two different particles. The results of the radiation test and the Monte Carlo simulations will be used to answer the posed research questions at the beginning of the thesis:

- How can the radiation monitor distinguish different types of radiation?
- What are the effects of radiation on 3D NAND memory?
- What is the accuracy of the dose measured by the radiation monitor?
- How can the track of the radiation particle be visualized?

Although only one particle type (Pb-208) was tested at CERN, the Monte Carlo simulations were used to get an idea of a difference in particle interaction within the 3D NAND memory stack. From the simulations, it can be concluded that Pb-208 and the proton irradiation show different dose and charge characteristics on memory pillars. Heavy-ions also create more secondary particles and collisions in a memory pillar than protons. Heavy-ions deposit a higher dose on the memory cells than protons.
Moreover, the monochromatic simulations showed a different deposited dose pattern for different energies. The Ultra-High energy beam (33 TeV) resulted in memory cells closest to the radiation source having the largest deposited dose. On the contrary, the memory pillars irradiated by a 210 MeV beam showed the lowest deposited dose in the cells closest to the radiation source. The large number of secondary particles created for the Ultra-High energy simulation could be an explanation for this difference.

From the data obtained from the CERN radiation test, it could be concluded that the threshold voltage of a memory cell decreases after being irradiated. The normal distribution of the threshold voltages in a memory cell before irradiation is affected by radiation. This property is used to filter a memory block and quickly identify the affected memory cells. From the simulations, a clear difference is seen for unidirectional and omnidirectional irradiation. The 210 MeV monochromatic simulations show that memory cells closest to the radiation source are less affected in terms of deposited dose and change in charge than the cells further away from the particle source. An explanation for this is the fanout effect. After a particle strikes the first layer it can fan out to other layers and neighbouring pillars. The simulations of the omnidirectional irradiation show that the effects within a pillar of memory cells show a homogeneous distribution regarding the deposited dose and charge.

The measured threshold voltage changed cannot be directly translated in an absorbed dose. The simulations performed did not account for initial charge that is held by a memory cell when programmed to a logic. A qualitative analysis can be made rather than a quantitative analysis based on the test results. CHIP3 for example, which was irradiated for a longer period of time shows a lower average threshold voltage per cell than CHIP1 which was irradiated for the shortest time. A direct relation between the deposited dose and the change in threshold voltage could not be found.

Perpendicular irradiation create tracks in the pillars of a memory block. A method is developed to quickly identify affected pillars in a memory block by using the change in normal distribution of the threshold

voltages. This method also works for irradiation under an angle where multiple pillars are involved. The track of a particle that travels through a memory block in a more random fashion is almost impossible to track. As more particles are involved, it cannot be determined which change in threshold voltage correspond to which particle.

7.2. Recommendations

A number of recommendations are presented in this Section to push the development an research for the low-cost space radiation monitor forward.
The first recommendation would be to expand the complexity of the Monte Carlo Simulations. The Monte Carlo simulations performed were simplified in terms of geometry and physics interaction. Only one layer was modeled for the geometry, while in reality, one pillar consists of different materials. To get a better estimation of the geometry it is recommended to contact the manufacturer for additional information. Possibly a NDA has to be signed as the internal structure of the memory is an intellectual property of the company. From the market analysis, it can be concluded that 3D NAND memory will only increase in the number of layers in their memory blocks. For future simulations the rapid increase in layers should be taken into account.
The simulations can also be extended by incorporating the peripherals and other components of the radiation monitor. The performed simulations only considered nine pillars and no external components. The final design of the radiation monitor will consist other components which can alter the paths of incoming radiation. The final configuration of the radiation monitor can be simulated in Geant4 to investigate the effectiveness of the 3D NAND memory with neighbouring components. The proposed space graded components in the conceptual design can shield the 3D NAND chip against a portion of the radiation, which could a part of the incoming radiation. The actual effects are currently unknown, however, this should be taken into account and possibly be calibrated for.

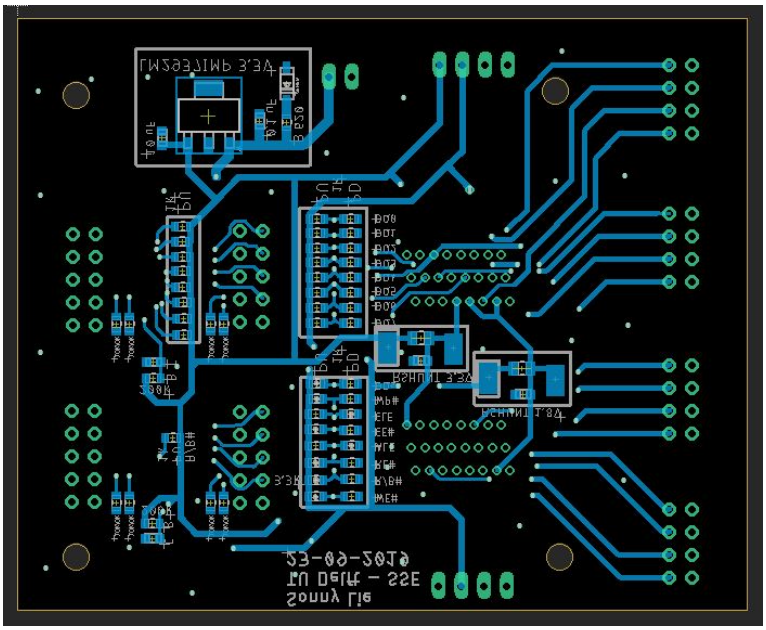
The charge trap devices are interesting to investigate, as most of the 3D NAND memory manufacturers use this technology. Micron, the only floating gate user for 3D NAND memory, also announced that they will switch to charge trap technology in the future. As charge trap devices become the dominant technology, it should be researched whether the developed hardware and software still applies to these devices and how well they perform in comparison with the floating gate devices.
One of the limiting parameters of the conceptual design is the operating temperature of the 3D NAND memory chip. The other components are space graded, which allow usage at a wider temperature range. Since the 3D NAND chip is a commercial product, the operating temperature range is from 0° C to 70° C. To accommodate the required temperature range, a stable thermal environment should be created for the radiation monitor.

In this thesis, a method has been developed to quickly find and visualize a pillar that is affected by radiation. This works well for unidirectional radiation beams without incidence angle. For a memory block that has been irradiated with an angle, it is harder to identify and capture affected pillars, as the pillars are only effected partially. An even more advanced method is required to identify the tracks in a space environment, where the radiation is omnidirectional. Machine learning would be an interesting option for data processing of the measurements. The measurements from the memory chip could be analyzed by an machine learning.

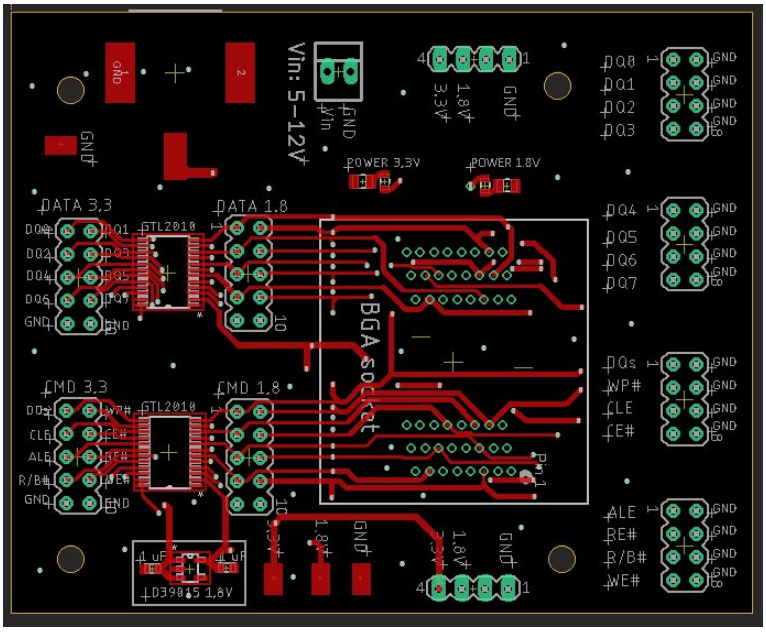
The conceptual design shows a radiation monitor heavily based on space graded components. These are only necessary for long-term missions. For smaller and shorter missions (LEO) it might be sufficient to use an FPGA and voltage regulator which are commercially available. A commercially available flash memory can be used with an advanced ECC to account for SEE due to radiation. These changes can reduce the cost of the radiation monitor significantly. The conceptual design shows the worst case scenario, where radiation tolerance is key. The overall outline of the components on the PCB is still flexible. Depending on the satellite configuration and available volume, the PCB can be changed in dimensions, as long as all the components fit on the chip. Another option could be placing components on both sides of the PCB or using a flex or foldable PCB. These options can save space and decrease the outer dimensions of the radiation monitor. The use of a different PCB layout can increase the cost of the radiation monitor.

A

PCB LAYOUT



(a) Bottom-view of custom PCB

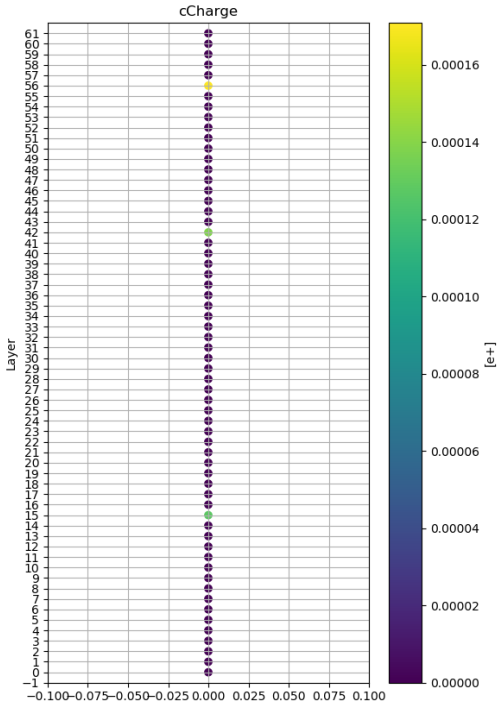


(b) Top-view of custom PCB

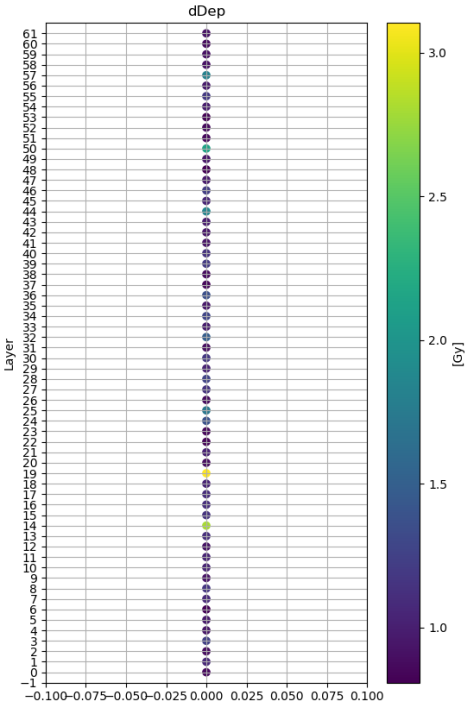
Figure A.1: Overview of top and bottom side of the custom PCB

B

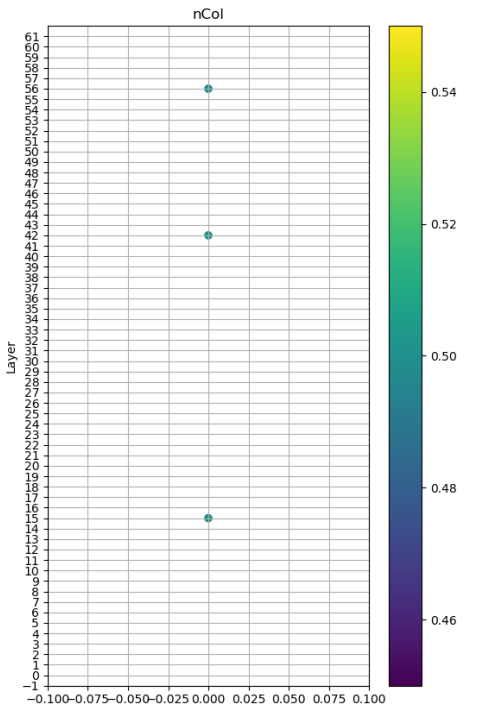
DETAILED SIMULATION RESULTS



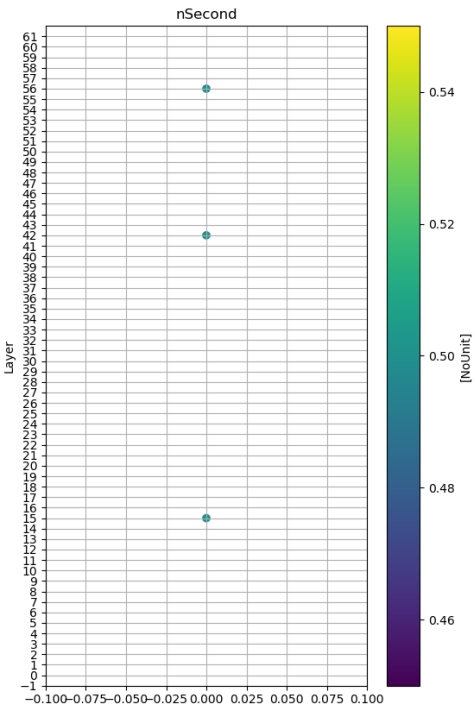
(a) Charge per memory cell



(b) Deposited dose per memory cell

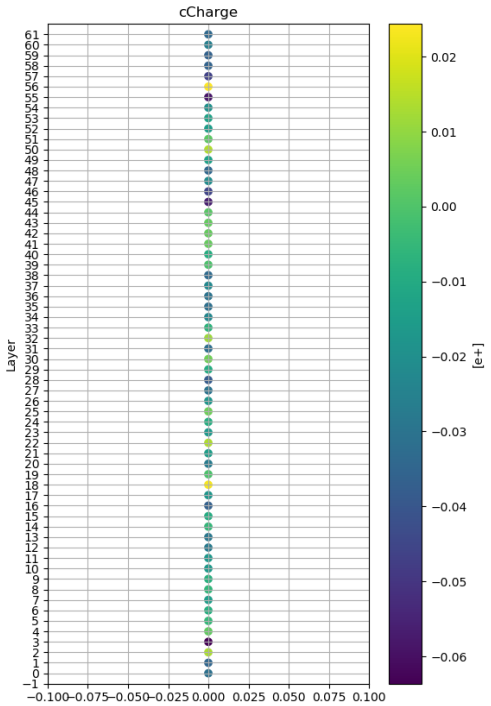


(c) Number of collisions within a memory cell

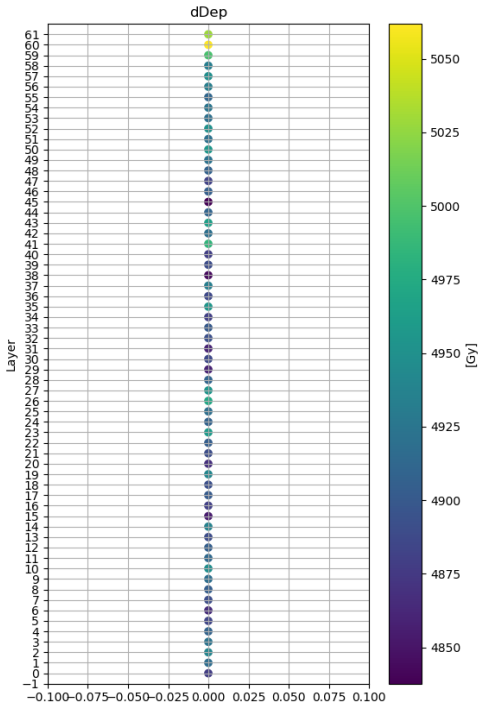


(d) Number of generated secondary particles per cell

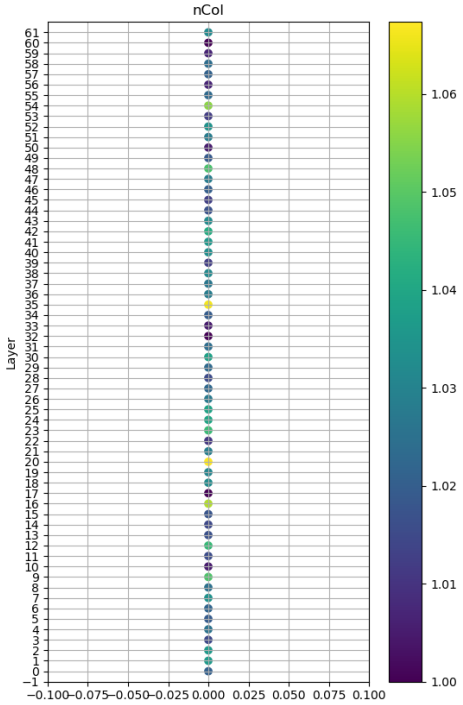
Figure B.1: Normalized scored quantities for memory stack in LEO subjected to protons



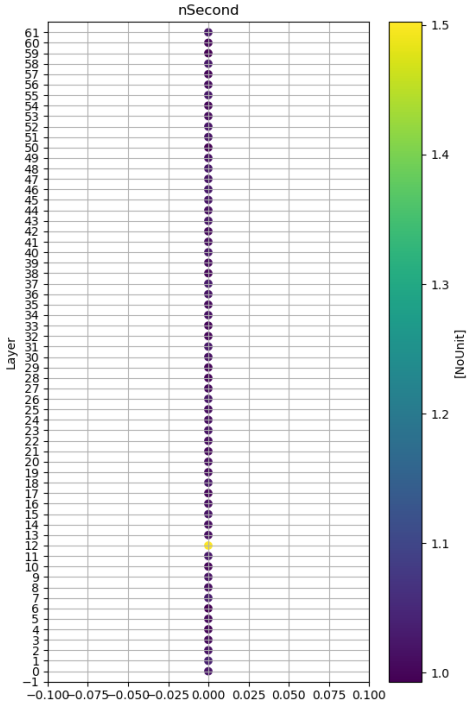
(a) Charge per memory cell



(b) Deposited dose per memory cell

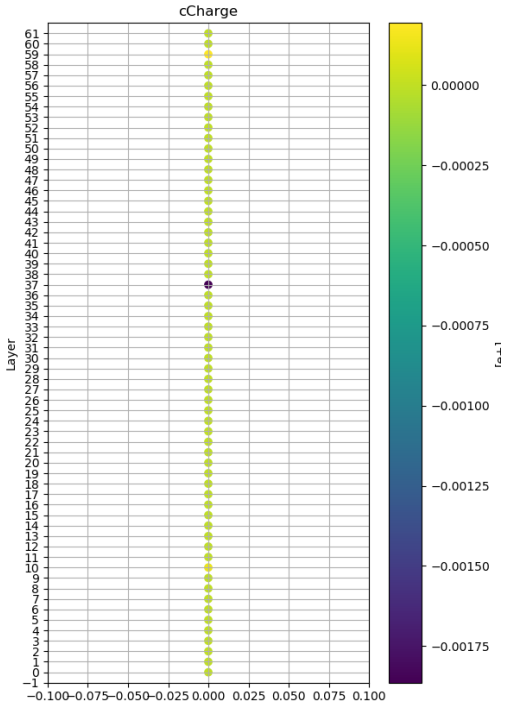


(c) Number of collisions within a memory cell

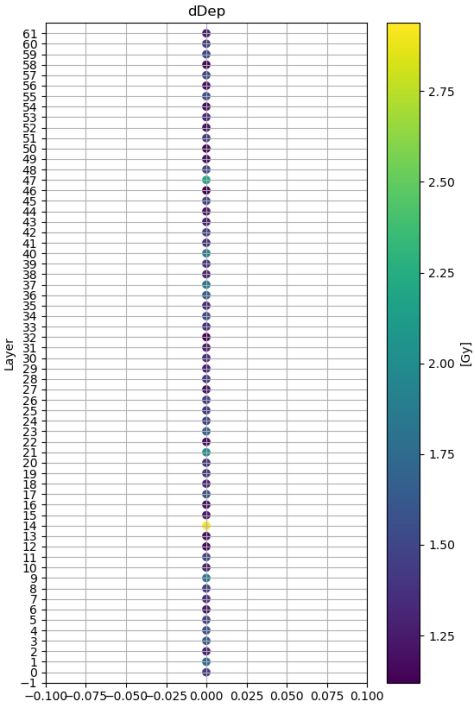


(d) Number of generated secondary particles per cell

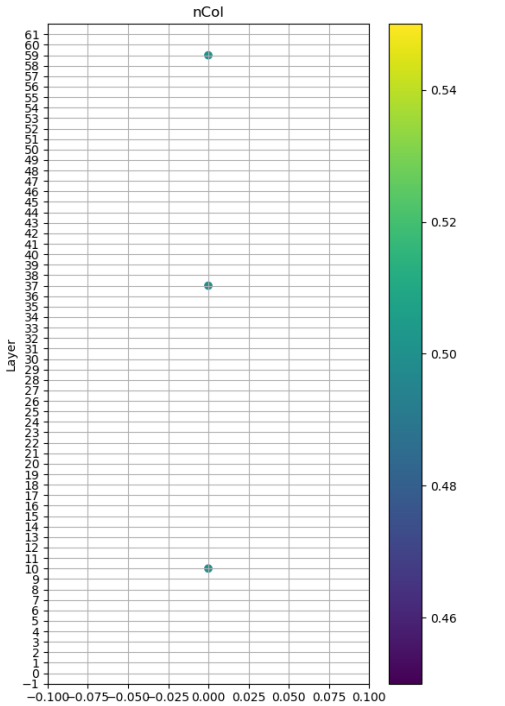
Figure B.2: Normalized scored quantities for memory stack in LEO subjected to Pb-208



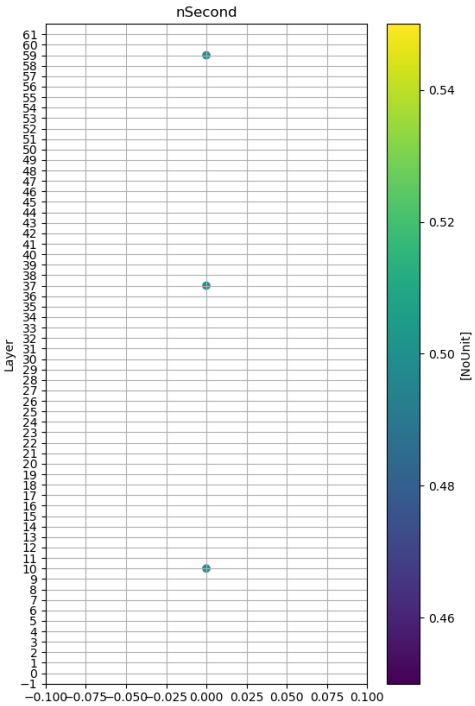
(a) Charge per memory cell



(b) Deposited dose per memory cell

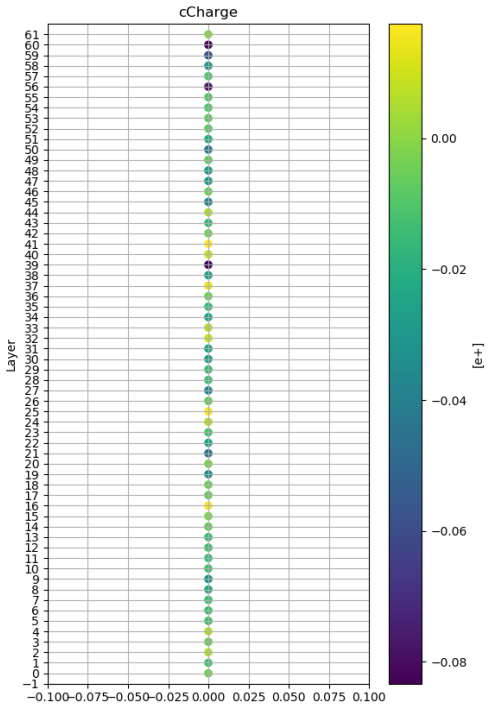


(c) Number of collisions within a memory cell

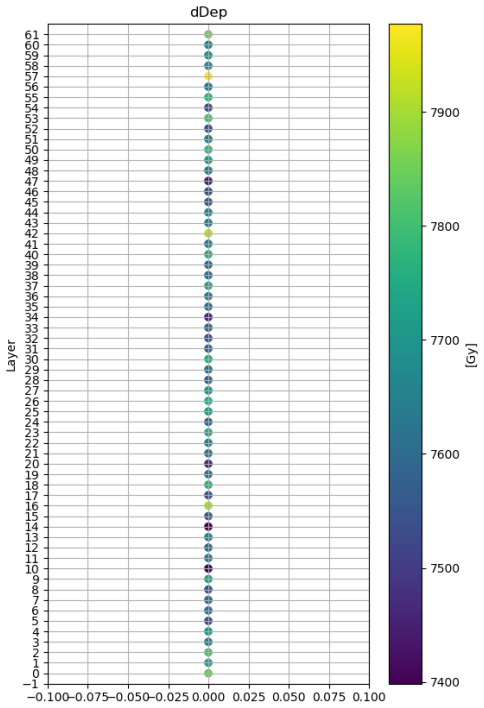


(d) Number of generated secondary particles per cell

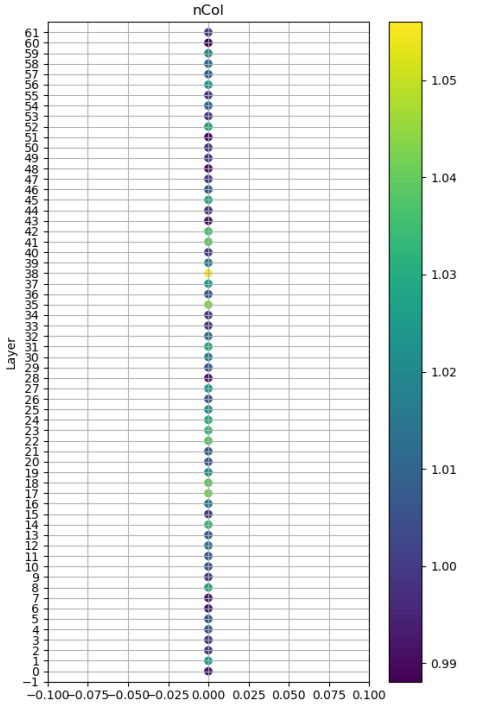
Figure B.3: Normalized scored quantities for memory stack in GEO subjected to protons



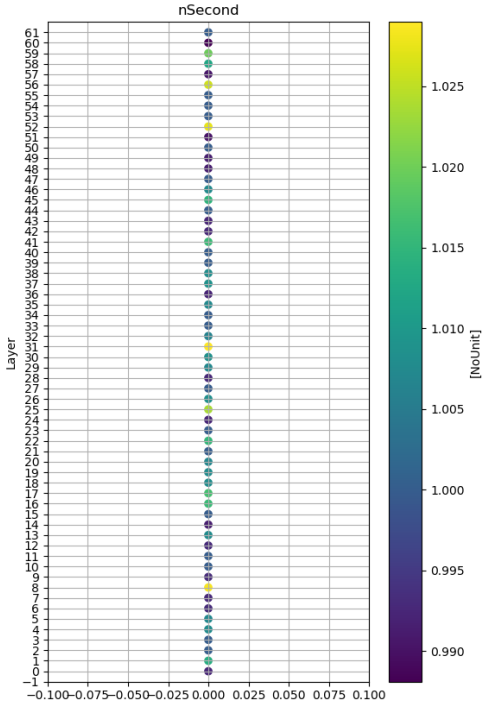
(a) Charge per memory cell



(b) Deposited dose per memory cell

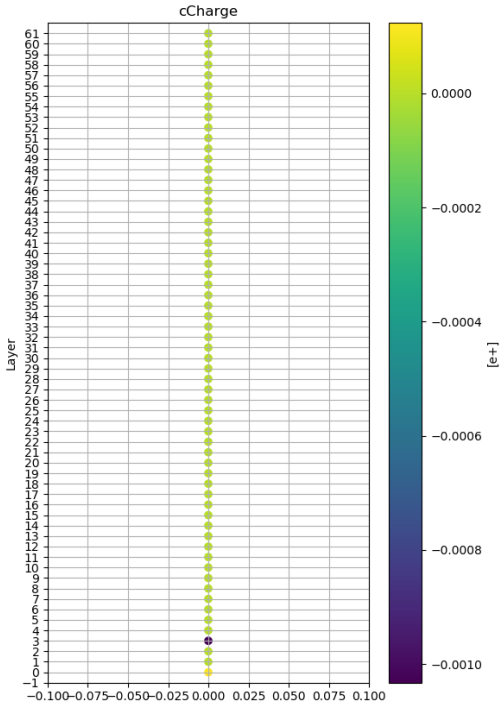


(c) Number of collisions within a memory cell

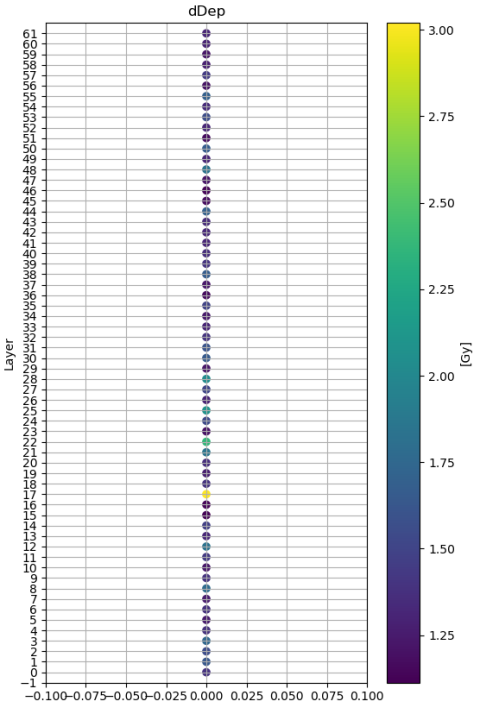


(d) Number of generated secondary particles per cell

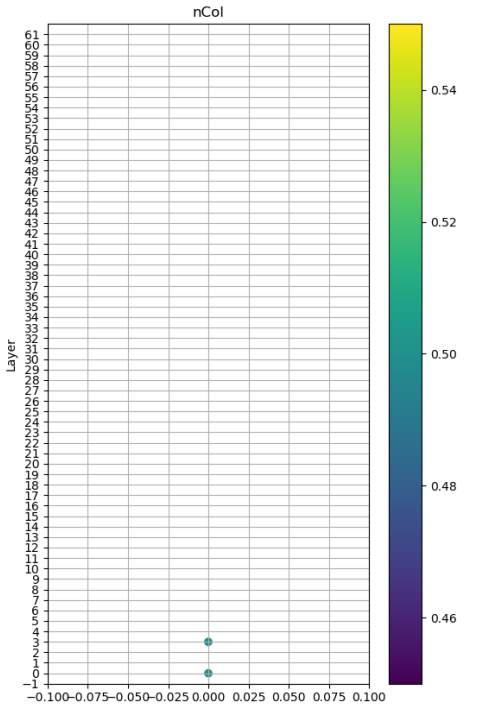
Figure B.4: Normalized scored quantities for memory stack in GEO subjected to Pb-208



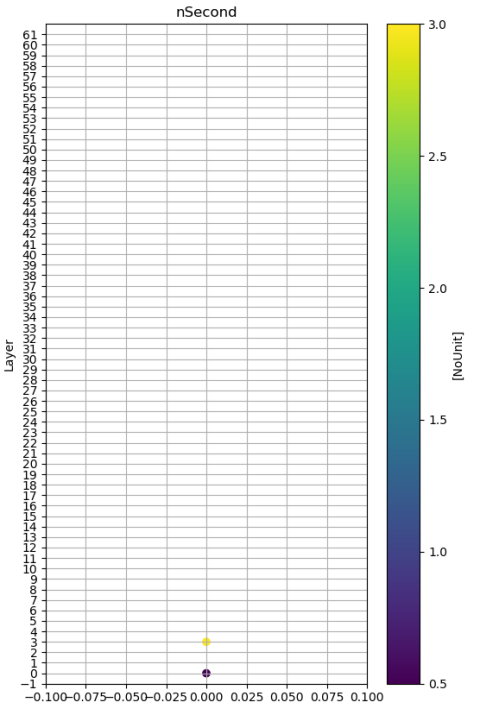
(a) Charge per memory cell



(b) Deposited dose per memory cell

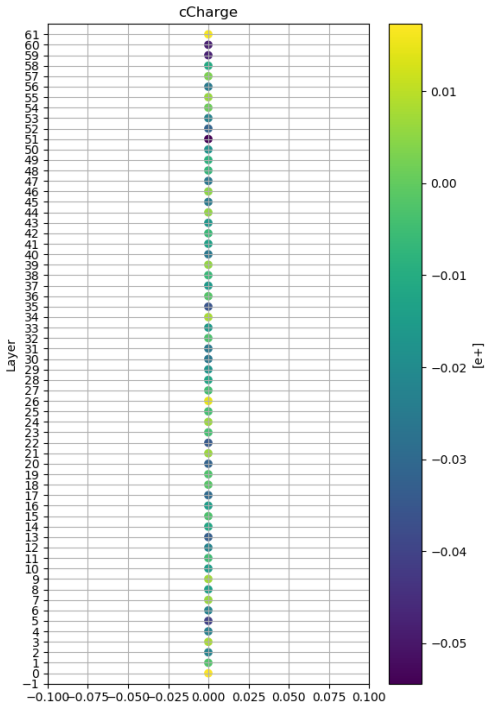


(c) Number of collisions within a memory cell

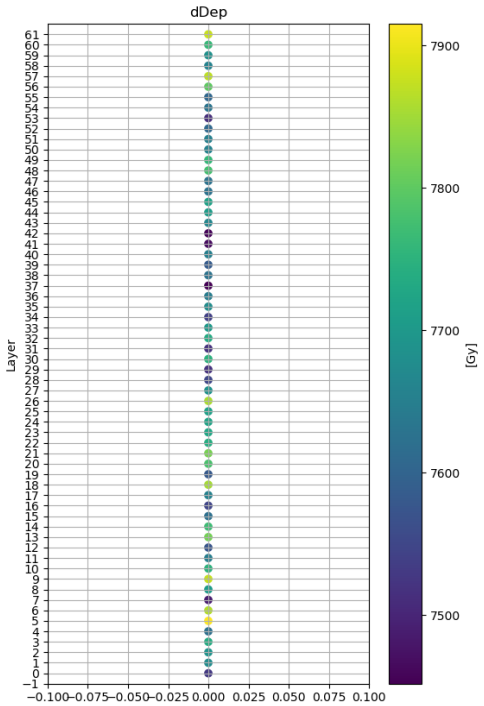


(d) Number of generated secondary particles per cell

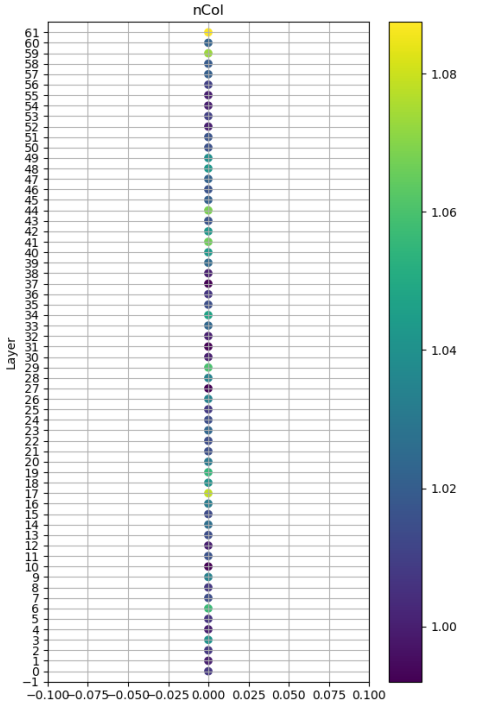
Figure B.5: Normalized scored quantities for memory stack in AEO subjected to protons



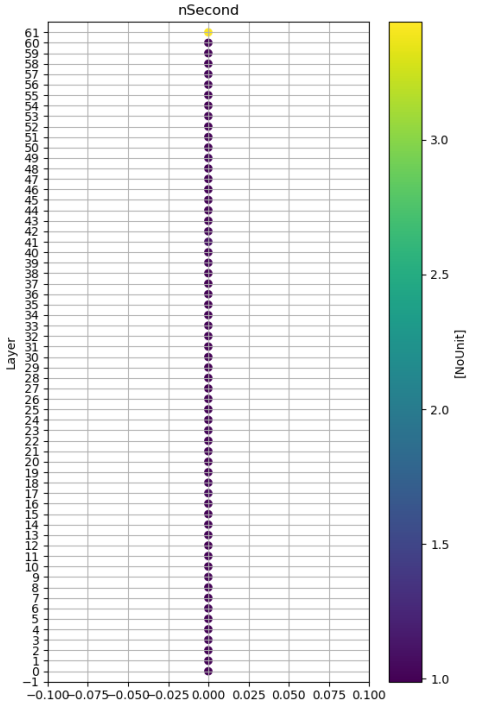
(a) Charge per memory cell



(b) Deposited dose per memory cell



(c) Number of collisions within a memory cell

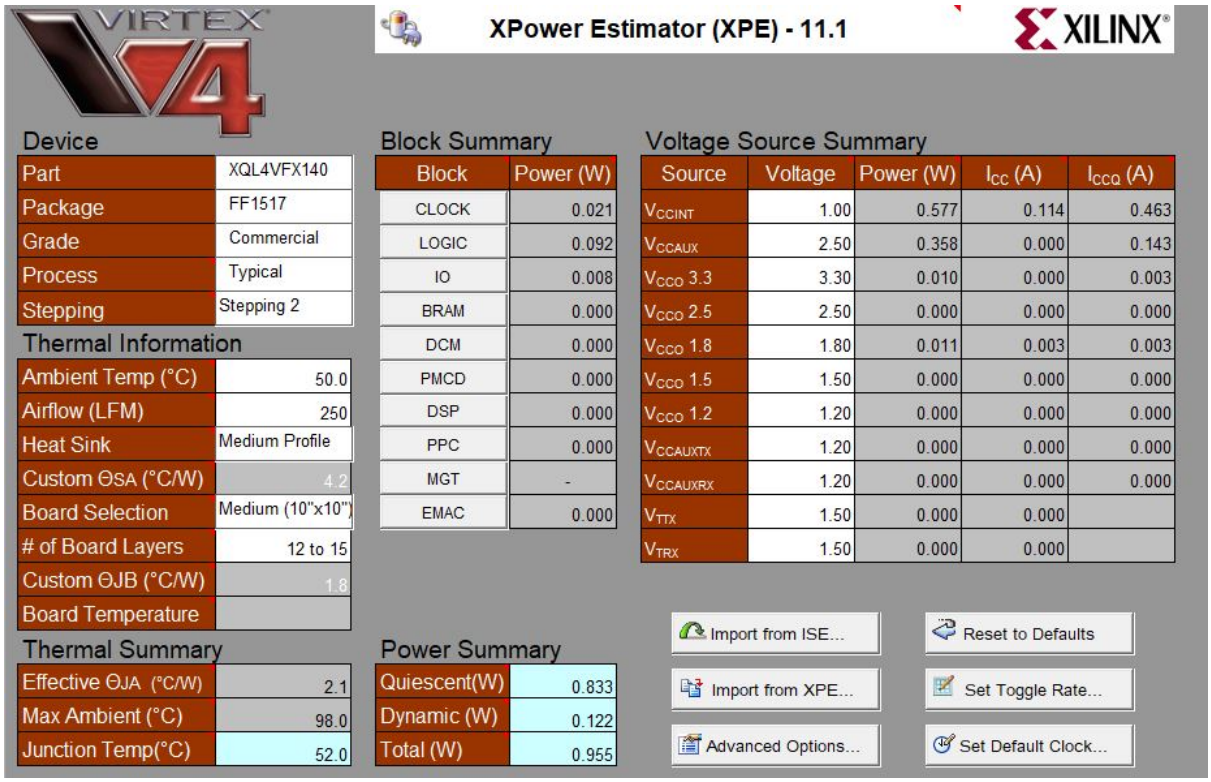


(d) Number of generated secondary particles per cell

Figure B.6: Normalized scored quantities for memory stack in AEO subjected to protons

C

Power Estimation Summary Virtex-4QV



XPower Estimator (XPE) - 11.1

XILINX

Device

Part	XQL4VFX140
Package	FF1517
Grade	Commercial
Process	Typical
Stepping	Stepping 2

Thermal Information

Ambient Temp (°C)	50.0
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom ΘSA (°C/W)	4.2
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom ΘJB (°C/W)	1.8
Board Temperature	

Thermal Summary

Effective ΘJA (°C/W)	2.1
Max Ambient (°C)	98.0
Junction Temp(°C)	52.0

Block Summary

Block	Power (W)
CLOCK	0.021
LOGIC	0.092
IO	0.008
BRAM	0.000
DCM	0.000
PMCD	0.000
DSP	0.000
PPC	0.000
MGT	-
EMAC	0.000

Power Summary

Quiescent(W)	0.833
Dynamic (W)	0.122
Total (W)	0.955

Voltage Source Summary

Source	Voltage	Power (W)	I_{CC} (A)	I_{CCQ} (A)
V_{CCINT}	1.00	0.577	0.114	0.463
V_{CCAUX}	2.50	0.358	0.000	0.143
V_{CCO} 3.3	3.30	0.010	0.000	0.003
V_{CCO} 2.5	2.50	0.000	0.000	0.000
V_{CCO} 1.8	1.80	0.011	0.003	0.003
V_{CCO} 1.5	1.50	0.000	0.000	0.000
V_{CCO} 1.2	1.20	0.000	0.000	0.000
$V_{CCAUXTX}$	1.20	0.000	0.000	0.000
$V_{CCAUXRX}$	1.20	0.000	0.000	0.000
V_{TTX}	1.50	0.000	0.000	
V_{TRX}	1.50	0.000	0.000	

Import from ISE... | Reset to Defaults | Import from XPE... | Set Toggle Rate... | Advanced Options... | Set Default Clock...

Figure C.1: Estimated power summary for the Virtex-4QV FPGA.

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