Thermal Management of High-Current Bidirectional Isolated DC-DC Converters

Yi Wang

Thermal Management of High-Current Bidirectional Isolated DC-DC Converters

Proefschrift

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To my family

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LIST OF SYMBOLS

δ	Vector angle between reactance and impedance of a capacitor	[rad]
δ	Phase shift	[rad]
δ	Skin depth	[m]
δ_{min}	Minimum phase shift	[rad]
δ_{max}	Maximum phase shift	[rad]
δ_{tri_max}	Maximum phase shift in triangular modulation	[rad]
δ_{trap_min}	Minimum phase shift in trapezoidal modulation	[rad]
δ_{null}	Null time duration	[rad]
ε	Permittivity	[F/m]
η	System efficiency	[%]
σ	Electrical conductivity	[S/m]
μ_n	Electron mobility	[m^2/(V s)]
ρ	Electrical resistivity	[Ω m]
ΔB	Flux density peak-to-peak value	[T]
ΔI	Magnitude of current ripple	[A]
a	Steinmetz constant	
a_f	Fill factor	
A_c	Core cross-section area	[m^2]
A_{cu}	Copper area	[m^2]
A_{drift}	Area of the drift region in a semiconductor	[m^2]
A_w	Winding window area	[m^2]
b	Steinmetz constant	
B_{pk}	Peak flux density	[T]
C_d	Core depth	[m]
C_{in}	Input capacitors	[F]
C_m	Steinmetz constant	
C_n	Material-related constant of core hysteresis loss	
d	Ratio between the input voltage and referred output voltage V_o'	

D	Duty Ratio	
D_c	Ratio between the conduction time and the switching period	
D_o	Duty Ratio	
E_c	Field breakdown strength of a semiconductor material	[V/m]
f_r	Resonant frequency	[Hz]
f_{sw}	Switching frequency	[Hz]
F_{prx}	Normalized skin-effect loss factor	
F_{sk}	Normalized proximity-effect loss factor	
h	Height of the secondary winding of transformer	[m]
I_{AVG}	Average Current	[A]
$I_{eq\_35\mu m}$	Equivalent current in 35μ m thick PCB trace	[A]
I_{rms}	Root-mean-square value of a current	[A]
I_f	Forward flowing current	[A]
i_{pri}	Current in the primary winding	[A]
I_{rr}	Peak of the reverse recovery current	[A]
J	Current density	[A/m^2]
k_{ce}	Material- and waveform-related constant of classical eddy current loss	
k_{ex}	Material- and waveform-related constant of excess eddy current loss	
k_h	Material-related constant of core hysteresis loss	
K_{rr}	Material-related constant of diode reverse recovery loss	
L_{bst}	Inductor in a boost converter	[H]
L_{lk}	Leakage inductance	[H]
L_r	Resonant inductor	[H]
M	Number of winding layers	
M	Distance from trace left/right edge to board left/right edge	[m]
N	Number of turns per winding layer	
N	Transformer turns ratio	
N_t	Number of winding turns	
N_{sw}	Number of semiconductors in parallel	
N_u	Number of identical converter units in parallel	

P_b	Base power in the per-unit system	[W]
P_{cap}	Capacitor loss	[W]
P_{ce}	Classical eddy current loss	[W]
P_{cond}	Conduction loss	[W]
P_{dr}	Loss in semiconductor driver	[W]
P_{ex}	Excess eddy current loss	[W]
P_h	Hysteresis loss in magnetic cores	[W]
P_{layer}	Power loss in each layer	[W]
P_{max}	Maximum power	[W]
P_{mag}	Loss in magnetic components	[W]
P_o	Output power	[W]
P_{on}	Turn-on loss	[W]
P_{off}	Turn-off loss	[W]
$P_{rec\_max\_pu}$	Maximum power of rectangular modulation in per-unit system	[W]
P_{rr}	Diode reverse recovery loss	[W]
P_{prx}	Winding loss due to proximity effect	[W]
P_{semi}	Semiconductor loss	[W]
P_{sw}	Switching loss	[W]
P_{sk}	Winding loss due to skin effect	[W]
P_{trap_max}	Maximum power of trapezoidal modulation	[W]
$P_{trap\_max\_pu}$	Maximum power of trapezoidal modulation in per-unit system	[W]
P_{trap_min}	Minimum power of trapezoidal modulation	[W]
$P_{trap\_min\_pu}$	Minimum power of trapezoidal modulation in per-unit system	[W]
P_{tri}	Power transferred by triangular modulation	[W]
P_{tri_max}	Maximum power of triangular modulation	[W]
$P_{tri\_max\_pu}$	Maximum power of triangular modulation in per-unit system	[W]
P_w	Winding loss	[W]
$Q_{g.tot}$	Gate charge of a MOSFET	[C]
Q_{rr}	Reverse recovery charge	[C]
R_{ac}	AC resistance	[Ω]
R_c	Resistor representing the magnetic core loss	[Ω]
R_d	Diode on-state resistance	[Ω]

R_{dc}	DC resistance	[Ω]
R_{ESR}	Equivalent series resistor	[Ω]
R_{fuse}	Fuse resistance	[Ω]
R_g	Gate drive resistor	[Ω]
R_{lk}	Leakage resistance	[Ω]
R_{on}	On-state resistance	[Ω]
$R_{on.sp}$	Specific on-resistance	[Ω]
R_{rr}	Resistor representing the reverse recovery loss of power diodes	[Ω]
R_p	Winding resistance due to the proximity effect	[Ω]
R_s	Winding resistance due to the skin effect	[Ω]
R_{shunt}	Shunt resistance	[Ω]
R_{sw}	Resistor representing the switching loss of power semiconductors	[Ω]
$R_{th.j\_PCB}$	Thermal resistance from junction to PCB	[K/W]
R_{th_jc}	Thermal resistance from junction to case	[K/W]
$R_{th.j\_top}$	Thermal resistance from junction to case top	[K/W]
R_{th_layer}	Thermal resistance of each lamination layer	[K/W]
S_{mod}	Modulation method	
t_{null}	Null time duration	[s]
t_{on}	Turning-on time interval	[s]
t_{off}	Turning-off time interval	[s]
T, T_{sw}	Switching period	[s]
T_c	Case temperature	[^{o}C]
T_{hs}	Heatsink temperature	[^{o}C]
t_{rr}	Reverse recovery time	[s]
t_s	Excitation time	[s]
V_b	Base voltage in the per-unit system	[V]
V_{BD}	breakdown voltage	[V]
V_c	Core volume	[m^3]
V_f	Diode forward voltage	[V]
V_g	Drive voltage of a MOSFET	[V]
V_{in}	Input voltage	[V]
V_i	Input voltage	[V]

v_p	Voltage across the primary winding	[V]
V_{RBD}	Diode reverse breakdown voltage	[V]
V_{tr}	Volume of each copper layer	[m^3]
V_o	Output voltage	[V]
V_o'	Output voltage referred to the primary side of the transformer	[V]
w	Width of the secondary winding of transformer	[m]
w_w	Winding window width	[m]

ACRONYMS

1D	One-Dimensional
2D	Two-Dimensional
3D	Three-Dimensional
AC	Alternating current
CCC	Current-carrying capacity
CCM	Continuous conduction mode
DAB	Dual active bridge
DAB-FB	Dual active bridge - full bridge
DC	Direct current
DCM	Discontinuous conduction mode
DF	Dissipation Factor
DFPR	Die free package resistance
DHB-SC	Dual half bridge with split capacitors
DSCC	Double-sided collective cooling
EMI	Electromagnetic interference
ESR	Equivalent series resistance
GaN	Gallium nitride
GSE	Generalized Steinmetz equation
HC	High current
HF	High efficiency
HPD	High power density
HV	High voltage
iGSE	Improved generalized Steinmetz equation
i^2GSE	Improved improved generalized Steinmetz equation
IGBT	Insulated-gate bipolar transistor
KPI	Key Performance Index
LV	Low voltage
LQC	Load resonant converter

MOSFET	Metal oxide semiconductor field-effect transistor
MLCC	Multi-layer ceramic capacitors
MLT	Mean-length-per-turn
MSE	Modified Steinmetz equation
PCB	Printed circuit board
PCRC	Parallel connected resonant converter
PD	Power density
PE	Power electronic(s)
PRC	Partially Resonant Converter
PWM	Pulse-wide-modulation
QRC	Quasi-resonant converter
RMS	Root mean square
SBD	Schottky barrier diode
SE	Steinmetz equation
SiC	Silicon carbide
SCRC	Series-connected resonant converter
TM	Thermal management
VA	Voltage-ampere
WBG	Wide band gap
ZCS	Zero-current switching
ZVS	Zero-voltage switching
ZVZCS	Zero-voltage and zero-current switching

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Chapter 1

Introduction

Conventional "Thermal Management" (TM) indicates various cooling techniques [1-1]. The goal of TM is to facilitate components operating at or below their maximum operating temperature while enhancing electronic designs that achieve all of the physical, electrical, thermal, and reliability requirements of the end products. In a power electronic converter with High-Power-Density (HPD), loss density in power components tends to increase due to a more compact component and system volume. The traditional thermal management approach would not be adequate for handling the thermal stress caused by the increased loss density within a limited space. *The major contribution of this work is to investigate an extended thermal management approach to effectively managing heat generation and heat removal in PE converters in order to realize HPD*. More specifically, this research will concentrate on the high-current bidirectional isolated DC-DC converters deployed in private marine vehicle applications where space is limited. To assist readers to better understand this work, this chapter introduces the related research background, problem statement, and thesis layout.

1.1 Development of Power Electronics (PE)

PE is an application of solid-state electronics for controlling and converting electrical power with assistance of electronic switching devices [1-2][1-3]. Until now, the development of PE has been driven by both technology push and application pull.

During the 1960s, breakthroughs in power semiconductor technology dramatically improved the voltage- and current- handling capabilities and switching speeds of electronic switching devices [1-4]. This allowed PE to flourish in a broad range of residential, industrial, and military applications such as traction and automotive, heating, lighting, information and telecommunication. Consequently, the continuous advance in technical fields of semiconductor wafer manufacturing, microprocessor design, packaging, and material has promoted PE to a more mature stage.

In addition to technology development, the needs in a wide range of applications have also significantly stimulated the advancement of PE. Some applications demand power supplies

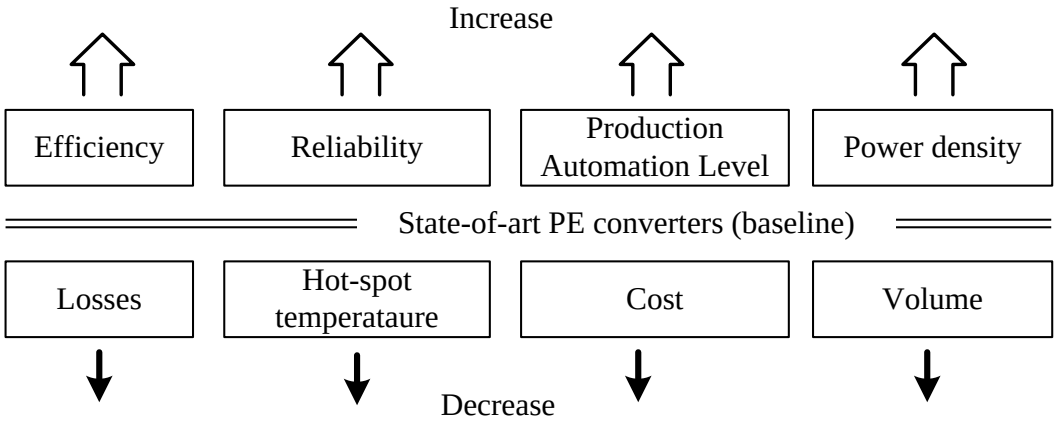
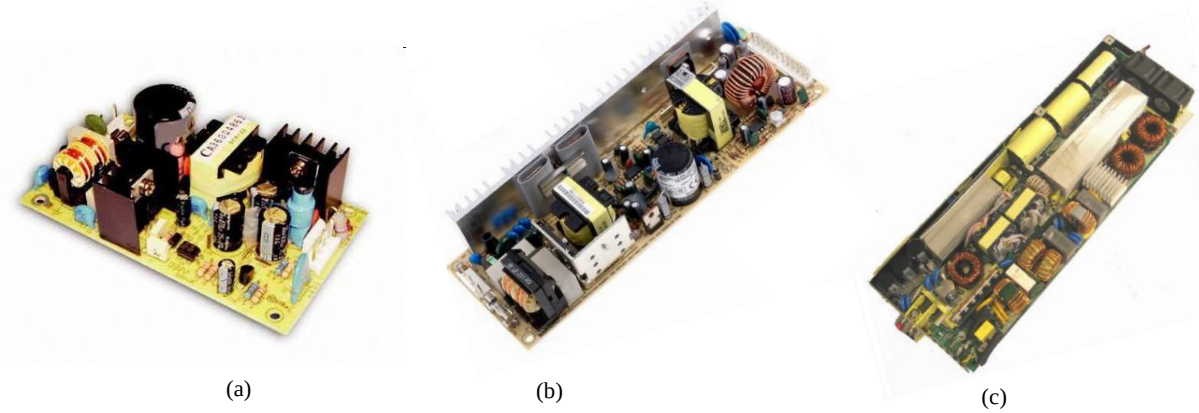


Fig. 1.1 Trends of PE converter requirements

with improved performance. Take power supplies for digital processors for example, the voltage level of microprocessors continuously decreases in response to the trend of smaller size, greater power, and higher transistor density [1-5]. Therefore, their power supplies must have increased stable output voltage and faster dynamic response. Some applications, such as the (hybrid) electric car [1-6] and solid-state lighting [1-7], require more efficient usage of energy where PE converters are employed to drive the loads and control the power flow. In recent decades, the utilization of renewable energy such as solar and wind power has been emphasized due to the depletion of fossil energy sources and the issues concerning the ever-deteriorating environment. As an important technical approach to the conversion and delivery of renewable energy [1-8], PE plays a vital role in the energy harvest industry.

Generally speaking, advancements of PE systems are stimulated by following application requirements: higher energy efficiency, better reliability, higher production automation level, and larger power density (Fig. 1.1).

Higher energy efficiency is a direct result of the generation of lower losses which is not only a response to the energy-saving appeal but also influences whether other requirements such as reliability and power density can be successfully fulfilled. Greater reliability requires the hot-spot temperature in the system to be lower since the temperature-dependent failure is the major cause of malfunction in electronic equipment [1-9]. Higher production automation level increases product yield and reliability, and reduces the end-product cost. The current PE practice has developed into a stage whereby it is difficult to reduce the system cost from a component perspective, but the packaging and assembly are quite costly due to the labor-intensive process [1-10]. Higher power density requires a reduced system volume with the same power processing capability, more power to be handled within the same volume, or more functionality to be integrated in the same space and more spatial design freedom [1-11]. HPD design is important for applications where space is limited such as in portable electronics and IT power supply as well as in automotive, marine and space vehicles. As achieving HPD design is the primary goal of this work, the status of state-of-the-art converters will be introduced briefly below from the power density point of view.



(a) (b) (c)

Fig. 1.2 (a) 25 W AC-DC UPS; (b) 150 W switching mode power supply (SMPS); (c) 3 kW AC/DC telecom power supply (forced air cooling)

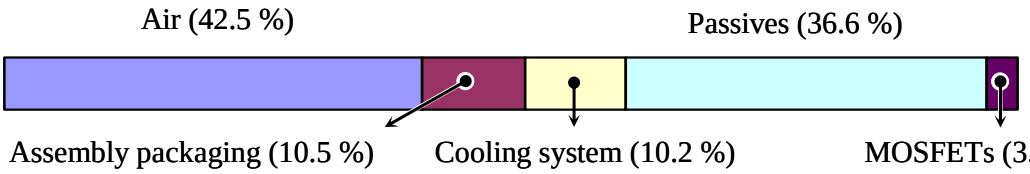


Fig. 1.3 Volume breakdown of an off-line laptop power supply built with the conventional technology [1-13]

The power density of state-of-the-art PE converters remains at a relatively low level. A survey performed on the primary power supply products of four Dutch PE developing companies [1-12] has indicated that the power density of several hundreds of W/L is still the mainstream. Many factors deteriorate the power density of current PE converters and main factors are introduced below.

Large amount of useless air filled in the system

Since component manufacturers employ varied packaging technologies and processes for the different components and even for the components with the same functions [1-13], the diversity and non-uniformity of component shapes and sizes are generated in current PE converters. This results in the fact that an extensive volume of waste air, which is not used for heat removing, fills a conventional PE system. This futile space can be observed in three typical switching-mode power supplies (open-frame) exhibited in Fig. 1.2. A volumetric breakdown of an off-line laptop power supply constructed with traditional technology is shown in Fig. 1.3 and indicates that the air occupies almost half (42.5%) of the system volume.

Inefficient Operation

The losses generated in a PE converter will be dissipated in the form of heat. An overabundance of heat generation increases the internal temperature of components to a level that shortens the component lifetime in the long run or immediately instigates catastrophic damage. To suppress heat generation, considerations can be given to a number of design aspects such as more efficient converter topologies, smarter semiconductor modulation methods, paralleled component units, better magnetic component structures, and more energy-efficient materials.

Inefficient Heat Removal

In PE converters, typical loss density ranges are 1~100 W/cm^2 for semiconductors, 0.1~1 W/cm^2 for magnetic components, and less than 0.1 W/cm^2 for capacitors [1-14]. Despite the minimal volume compared with passive components, high power semiconductors are always equipped with a cooling system much larger than themselves due to their outstanding loss density. If the thermal interface from semiconductors to the cooling system is not carefully designed, the volume of cooling system will be boosted considerably. Often, magnetic components and capacitors handle their heat through convection and radiation over their surfaces. This inefficient self-cooling pattern and their low energy density make the passive components cumbersome. In the case demonstrated in Fig. 1.3, the volume of passive components is the second largest contributor to the system volume.

To design a compact PE converter, this work investigates an effective heat generation management and heat removal management approach. More specifically, high-current bidirectional isolated DC-DC converters in marine vehicle applications will be our research carrier.

1.2 High-Current Isolated DC-DC Converters

A DC-DC converter is a PE system that converts a source of direct current from one voltage level to another. A typical application of high-current isolated DC-DC converters is the interface of Low-Voltage (LV) storage batteries to the High-Voltage (HV) DC bus in vehicle power distribution systems such as yachts illustrated in Fig. 1.4. In this system, the diesel generator is the primary energy source that provides power to the loads and charges the batteries when sailing. As the alternative energy source, the storage batteries power a number of on-board loads when the generator ceases to perform, or provide the transient power to assist the start-up of engines and other electrical machines on board. It is the DC-DC converter (highlighted in Fig. 1.4 with bold lines) that connects the storage batteries to the HV DC bus that distributes the power to loads. The major characteristics of this DC-DC converter are listed below:

- *High-Current*. Since the voltage level of the storage batteries remains at several tens of volts, and the normal continuous power is several kilowatts, the current can increase to several hundreds of amperes at the converter input.
- *Galvanic isolation*. Due to the large difference between batteries and a HV DC bus, a transformer with a substantial turns-ratio is normally employed to scale the voltage level.
- *High transient power*. Batteries power the start-up of engines and other electrical machines on board, so their cascaded DC-DC converters must electrically and thermally handle this large transient power.
- *Bidirectional power flow*. In addition to energy discharge, the batteries must also be charged when their voltage drops below a certain level. This is performed through the generators on-board or the grid plug on-shore when the marine vehicle is idle in har-

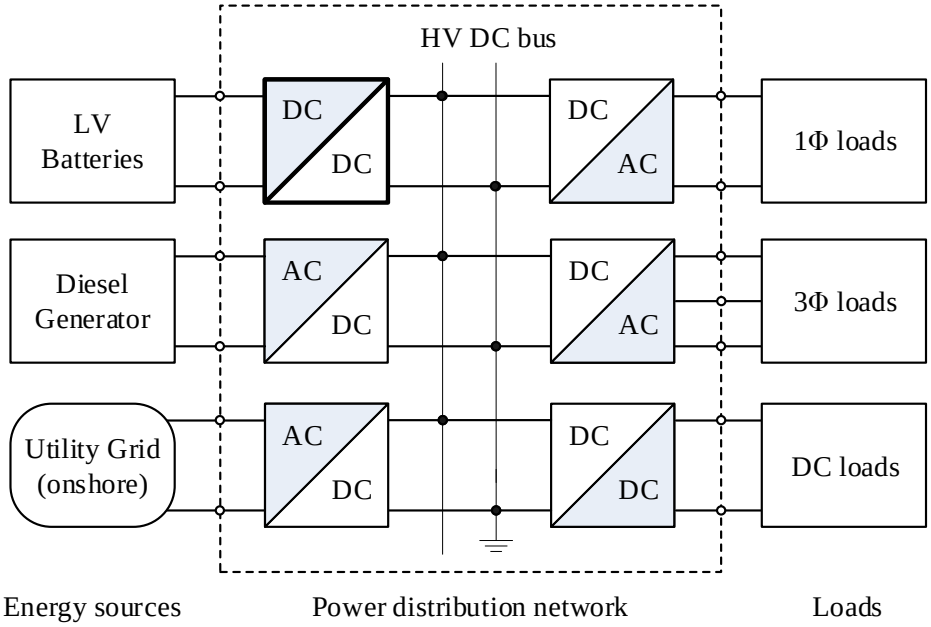


Fig. 1.4 Diagram of a typical power distribution network on a yacht

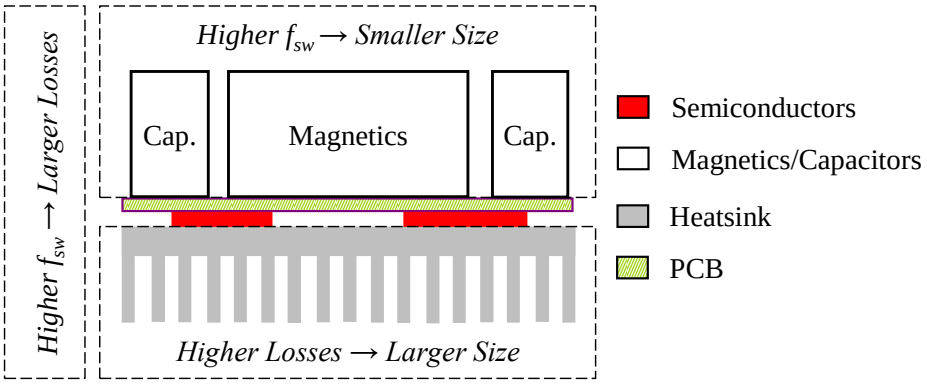


Fig. 1.5 An illustration of an air-cooling PE converter

bors. Therefore, it requires the DC-DC converter to be equipped with bidirectional power flow ability.

- *High power density*. Due to the limited space on marine vehicles like yachts, a HPD design of this type of converters is always preferable.

1.3 Problem Description

At the fixed power level, volume reduction increases the converter power density. In state-of-the-art PE converters, the passive components and cooling system dominate the system volume [1-15], which is conceptually illustrated in Fig. 1.5. Increased switching frequency of semiconductors is able to effectively reduce the volume of magnetics and capacitors [1-11], unless the capacitors are used for line frequency energy storage. However, higher frequency also raises the switching losses of semiconductors and core losses of magnetic components, which subsequently blows up the required volume of the cooling system to keep the temperature of components below a safe level. This undermines the effort of increasing frequency to

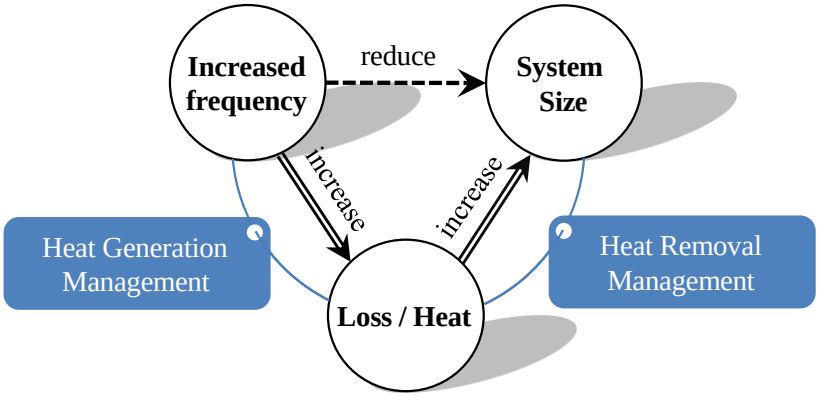


Fig. 1.6 Design dilemma in raising the power density of PE systems

reduce the system volume. This design dilemma (illustrated in Fig. 1.6) is the primary obstacle to improving the power density of PE converters. Effective heat generation management to control the loss generated by the high switching frequency and heat removal management to control the temperature rise would be solutions to this design issue (Fig. 1.6)

The loss characteristics of a PE converter primarily originate in its circuit topology property. Different topologies vary in terms of component stresses, component counts, semiconductor modulation methods, power delivering pattern, and so on. The topology that can intrinsically generate less loss in a specified application facilitates heat generation management. In addition to operation efficiency, many other factors determine whether one topology is appropriate for a HPD design in a certain application. For instance, if capacitors are used to carry the power current, then this topology requires large capacitors to thermally manage the significant loss and is, therefore, inherently not a suitable candidate for high-current HPD design. Therefore, selecting the most suitable topology for given applications is the initial decision to make at the beginning of designing a PE converter.

Once the converter topology has been confirmed and component types have been specified, a number of other design and component parameters must be optimized to obtain the optimal system performances. The design parameters include the switching frequency, inductance value and modulation methods, and so on. Key component parameters encompass the number of units connected in parallel (e.g. semiconductors, capacitors), number of winding turns, and the winding configuration of transformers. The optimal values of these parameters may also change with temperature and converter operating range. If the converter is to be optimized for efficiency, a loss model that can accurately and rapidly estimate the system and component losses with the abovementioned parameters will significantly facilitate the design.

The winding loss of a high-current transformer is extensive. To reduce it, the low-voltage winding must be with the minimum turn count to decrease winding resistance. However, less winding turns increase the flux density of the magnetic cores which tends to increase the tem-

perature of the cores. A larger core can be employed to restrain the flux density increase, but again, the volume of the transformer increases. Therefore, it is helpful to review the high-current transformer design in order to achieve the balance between the loss generation and transformer volume.

Besides heat generation, heat removal is the other aspect of HPD design. Without a careful cooling design, even a minimal loss can accumulate to burn components, not to mention the escalated loss density in the HPD design. Power semiconductors can be easily coupled to any flat cooling surface, however, the bulky passive components, which are considered as volume-heating components, are often decoupled from the cooling force that is engaged at semiconductors. The heat within these passive components has to be released to ambient through their own surfaces. This results in a poor cooling efficiency. Integrating the active and passive components into the same cooling structure will improve the cooling efficiency. However, the bulky size, volume-heating property, and high internal thermal resistance of passive components remain as the challenge to cooling design.

1.4 Objective and Approaches

To solve the aforementioned issues, the primary objective of this thesis is to achieve a high power density design of high-current isolated DC-DC converters. To achieve this goal, a thermal management approach is proposed which extends the traditional thermal management concept to two parts: heat generation management and heat removal management.

Heat generation management

Heat generation management does not signify minimizing losses at any expense but, instead, minimize the losses within affordable cost and limited space such that the subsequent heat removal management is supplied with optimized loss inputs. This part covers three steps:

- Evaluate and select the isolated DC-DC topology that is the most appropriate for the high-current HPD design.
- Develop a loss modeling platform to analyze losses and optimize the converter and component parameters.
- Design optimization of high-current transformers.

Heat removal management

The collective cooling strategy is proposed to limit the component temperature rise in a volumetrically efficient manner. It aims to collect heat from the main power components via different heat interface designs and conduct it to a common heat exchange surface where heat is dissipated in a centralized manner.

1.5 Thesis Layout

The body of this thesis consists of two parts, namely, heat generation management and heat removal management. The thesis layout is illustrated in Fig. 1.7.

Chapter 2 introduces the main loss sources in a PE converter. The loss mechanisms in different components and their calculation methods are presented as well as addressing the solutions to decrease these losses. This chapter provides background and input to the heat generation management chapters that follow.

Heat Generation Management

Chapter 3 evaluates and compares several mainstream isolated DC-DC topologies that are equipped with bidirectional power flow and soft-switching capability. These comparisons are based on the voltage and current stress on components, utilization of transformers, component counts, and whether passive components handle the power currents. Based on these comparisons, the topology that is most suitable for high-current and HPD design is concluded.

Chapter 4 proposes an analytical loss modeling platform which is specifically developed for high-current converters. Based on this loss model, losses in major power components can be calculated rapidly and accurately with various design and component parameters over the entire operating range. The effects of parasitic resistances and temperature are also included.

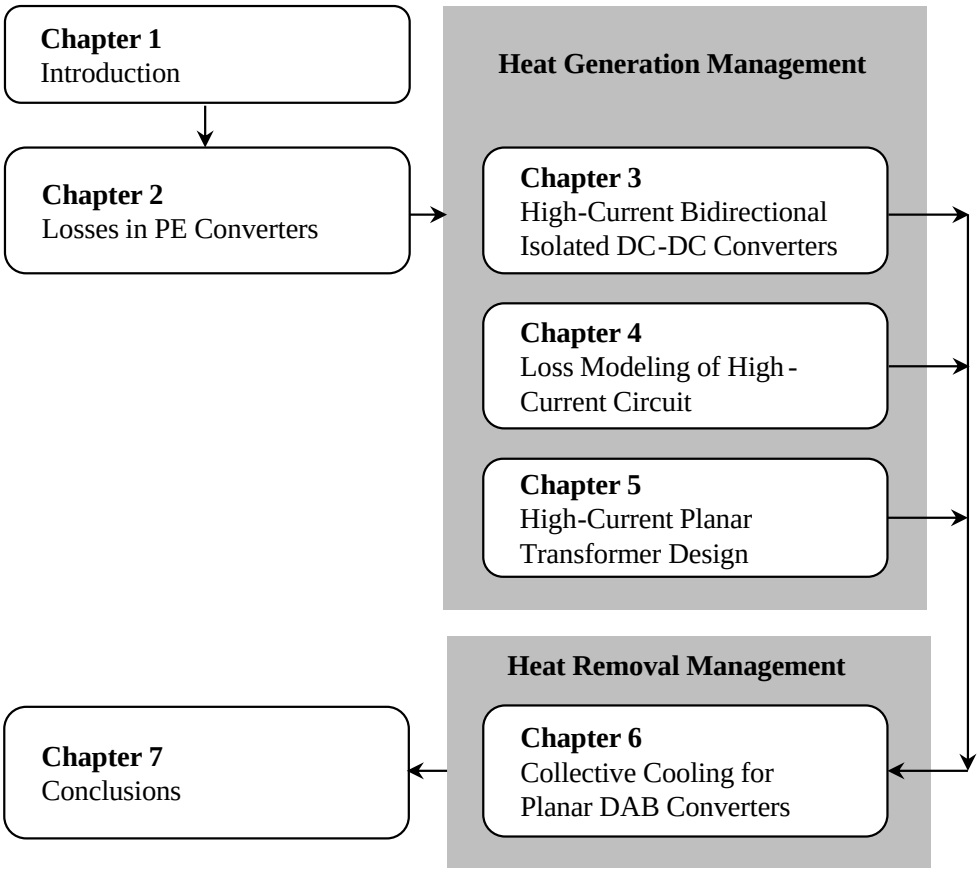


Fig. 1.7 Thesis Layout

The verification methods of this loss model are also presented. This loss model is employed to optimize the converter according to the given specifications.

Chapter 5 reconsiders the design of the planar PCB transformers for high-current applications. The dimensions of the transformer core are optimized for minimum transformer losses, and the configuration of the cores is improved in response to the requirements for improved cooling and specific leakage inductance in dual active bridge topology. The transformers made of ferrite and nano-crystalline core materials are compared.

Heat Removal Management

Chapter 6 proposes the collective cooling strategy for high-current isolated DC-DC converters. This strategy is engaged to obtain an effective and compact cooling system. The concept is demonstrated on a 1 kW dual active bridge converter. A double-sided collective cooling structure is also proposed to fully exploit the surface area of a low-profile converter. A dual active bridge converter with 2 kW nominal power and 10 kW peak power is designed to demonstrate this concept.

This thesis is concluded in Chapter 7 which summarizes the major contributions in this thesis. Re-commendations for future research are also suggested.

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Chapter 2

Losses in Power Electronic Converters

2.1 Introduction

Loss is generated in the form of heat during the electrical power processing and the loss generation is inevitable. With a PE converter, electrical energy is propagated and converted through several major functions [2-1]:

- Conduction
- Switching
- Electromagnetic (EM) transformation
- Filtering and storage

These functions are mainly executed by three categories of power components, including semiconductors, magnetic components (e.g. transformers, inductors) and capacitors. The functions that these components act are illustrated in Fig. 2.1. It can be found that all power components are involved in the conduction function. In the high-current applications, the conduction function will generate considerable loss in all power components. In applications where high switching frequency is required to reduce the size of passive components, high

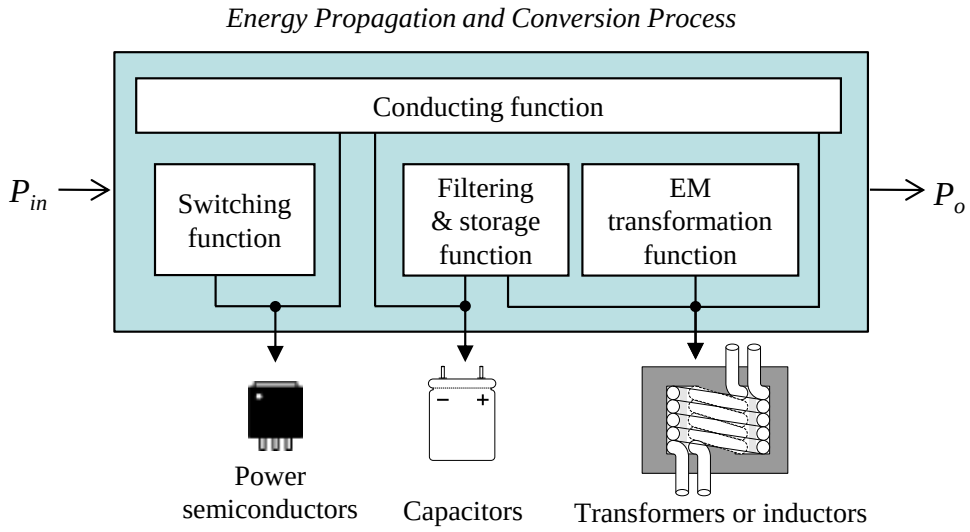


Fig. 2.1 Loss generation by main functional components

loss will be induced in switching and EM transformation functions, which are conducted mainly by power switching semiconductors and magnetic components.

Objectives

The proposed thermal management approach, especially the heat generation management component, requires a thorough understanding of losses. The objectives of this chapter are

- To review loss generation mechanisms in power semiconductors, magnetic components and capacitors.
- To review the loss-related factors and loss calculation of different components.
- To evaluate loss reduction methods.

This chapter provides inputs to the chapters related to heat generation management and allows for 1) the evaluation of whether a topology is suitable for high-current bidirectional isolated DC-DC converters (Chapter 3), 2) the losses generated in different components to be quantified (Chapter 4); 3) Optimization of a high-current transformer design in terms of efficiency (Chapter 5).

In Section 2.2, the typical losses in a PE system based on a boost converter are outlined, and the loss generation mechanisms of key power components, loss-related factors and loss calculation methods are reviewed. The solutions to reduce losses in these components are introduced and evaluated in Section 2.3. Conclusions are presented in Section 2.4, with emphasis on high-current PE converters.

2.2 Component Losses

In this section, an overview of losses in PE converters is presented, with a boost converter (Fig. 2.2) as the carrier. The boost topology contains the basic power components of a PE system: power switching transistor (*S*, here MOSFET used) and its drive circuit, power diode (D_{bst}), magnetic component (inductor, L_{bst}) and capacitors (C_{in}, C_o). The losses in a boost converter are shown in Fig. 2.3, where all power components are assumed lossless, but their losses are represented by equivalent resistors or a voltage source (listed in TABLE 2.1). Most of losses are generated by the conduction functions, however three are generated by non-conduction functions:

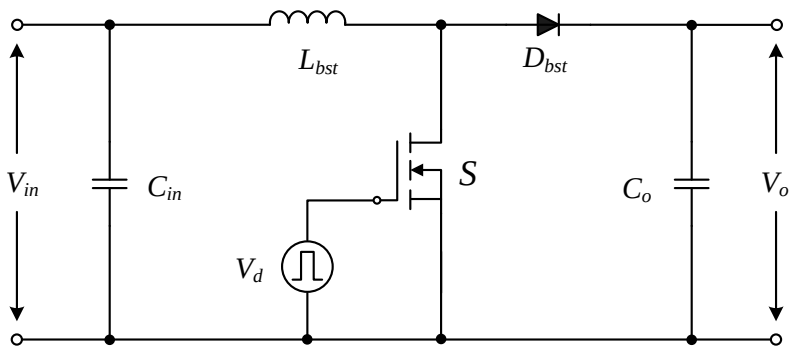


Fig. 2.2 Circuit schematic of a boost converter

TABLE 2.1 LOSSY RESISTORS OR VOLTAGE SOURCE IN FIG. 2.3 AND THEIR REPRESENTED LOSSES

Designators	Resistors	Loss Represented
	Power MOSFET	
R_{on}	On-state resistance	Conduction loss
R_{sw}	Equivalent dependent resistance	Switching loss
R_g	Gate drive resistor	Switching loss
	Diode	
R_d	Diode on-state resistance	Conduction loss
V_f	Diode forward voltage	Conduction loss
R_{rr}	Equivalent dependent resistance	Switching loss (Reverse Recovery)
	Inductor	
R_s	Winding resistance (skin effect)	Conduction loss
R_p	Winding resistance (proximity effect)	Conduction loss
R_c	Equivalent dependent resistance	Core loss from EM transformation and storage functions
	Capacitor	
R_{lk}	Leakage resistance	Dielectric loss from filtering and storage function
R_{ESR}	Equivalent Series Resistor (ESR)	Conduction loss

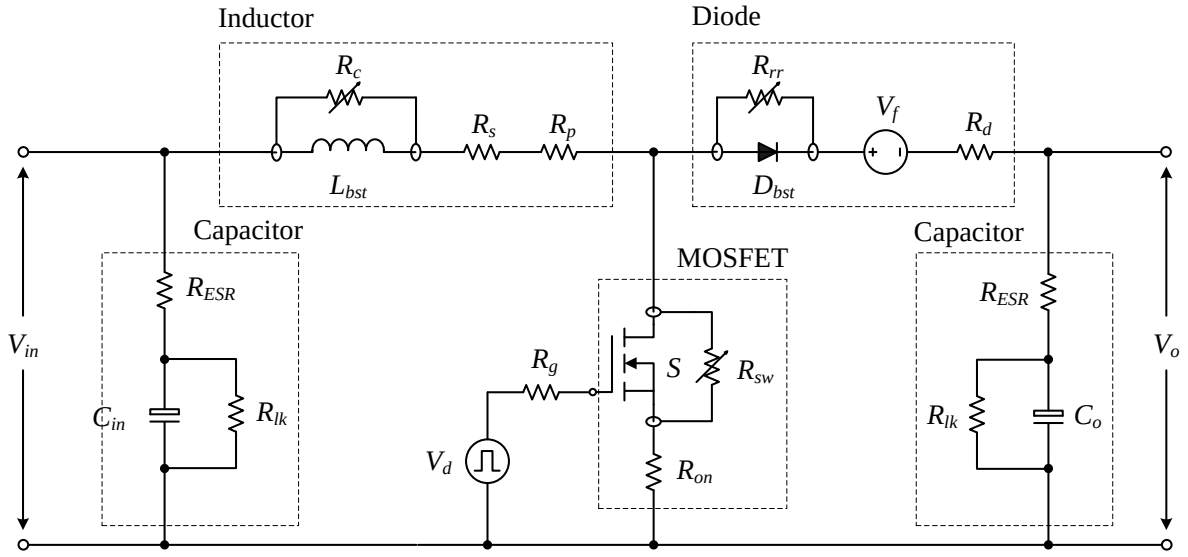


Fig. 2.3 Losses in key power components in a boost converter, where losses resulted from switching, EM transformation and storage functions are represented as equivalent dependent resistors (R_{sw}, R_{rr}, R_c)

- Switching loss of MOSFET (R_{sw}) and diode reverse-recovery loss (R_{rr}). These two are generated by the switching function. Their values depend not only on electrical stress, but also on device properties and parasitic elements.
- Inductor core loss (R_c), which is induced by the EM transformation function. Besides electrical stress, it also depends on core material and switching frequency.

Important losses and their calculation will be reviewed below.

2.2.1 Power Semiconductor Loss

Semiconductor losses include conduction loss and switching loss. The conduction loss is the ohmic loss during the on-state and the switching loss is generated during the turn-on and turn-off transient intervals. Because MOSFET has higher efficiency and a faster switching speed than other power transistors (e.g bipolar transistor and IGBT) in low-voltage and high-current applications, this section concentrates on MOSFET loss.

Conduction Loss

The conduction loss is an ohmic loss. It is generated when electrical current flows through the device channel during the on-state. It is calculated by $R_{on}I_{rms}^2$, where R_{on} is on-state resistance and I_{rms} is the root-mean-square (RMS) value of the flowing current. Defined as proportional to I_{rms}^2, the conduction loss increases dramatically in high-current applications.

On-state resistance can be divided into two parts: die resistance and packaging resistance. The die resistance is determined by the die material, structure and doping density and so on, while the packaging resistance is dependent on the applied interconnection structures.

In the internal structure of power semiconductors, the drift layer determines the device voltage blocking rating and dominates the die resistance to a large extent. For majority carrier devices like MOSFET, the drift layer resistance, also known as specific on-resistance ($R_{on.sp}$), can be estimated as [2-2] follows:

$$R_{on.sp} = \frac{4V_{BD}^2}{\varepsilon \mu_n A_{drift} E_c^3} \tag{2-1}$$

where V_{BD} is the breakdown voltage rating, E_c is the field breakdown strength of applied semiconductor material, A_{drift} is the layer area, μ_n is the electron mobility, and ε is the permittivity. It can be determined from Eq. (2-1) that

- The specific on-resistance rises as the breakdown voltage rating V_{BD} increases. Therefore, the MOSFET voltage rating should be kept low enough for a low die resistance.
- Larger die area results in a smaller die resistance.
- Electron mobility μ_n drops as the die temperature increases, consequently, the die resistance rises with higher temperature. Typically, R_{on} doubles as temperature rises from 25 ^{o}C to 125 ^{o}C [2-3].
- Semiconductor material with high E_c, such as the Wide Band-Gap (WBG) semiconductors SiC and GaN, has lower die resistance than Si-based semiconductors, theoretically [2-4].

The packaging resistance is the resistance generated in the interconnection between the die and external circuit. The bonding-wire or lead-wire is typically deployed as the interconnec-

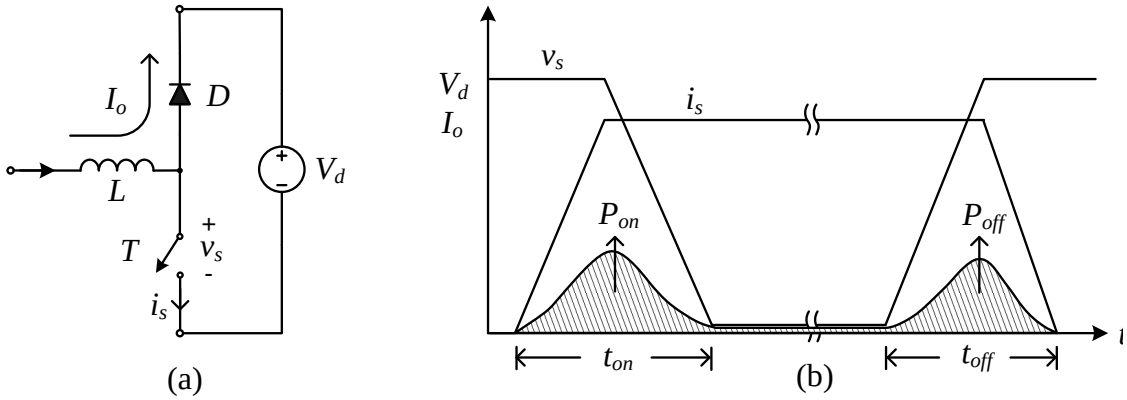


Fig. 2.4 (a) Diode-clamped inductive switching network; (b) switching waveforms at turn-on and -off intervals

tion structure in traditional semiconductor packaging methods. Due to recent advances in die fabrication technology, packaging resistance has replaced die resistance as the bottleneck to further reduction of the on-state resistance in LV MOSFETs [2-5].

Switching Loss

When switched from one state (ON/OFF) to the other (OFF/ON), power semiconductors experience high voltage and high current simultaneously during switching intervals, which results in the so-called switching loss. Fig. 2.4(a) illustrates a representative diode-clamped inductive switching network, which can be found in basic PE converters like buck, boost, buck-boost and inverter circuits. Fig. 2.4(b) shows the voltage and current waveforms of its semiconductor during on/off switching intervals (t_{on}/t_{off}). It can be observed that during switching intervals t_{on} and t_{off}, only when one of the voltage or current rises to the steady state value, the other starts to change. This switching pattern is known as hard- switching. The hard-switching behavior at high frequency results in a considerable switching loss, semiconductor stress and electromagnetic interference (EMI) [2-6]. The hard-switching loss P_{sw} can be estimated as [2-7]:

$$P_{sw} = \frac{1}{2} V_o I_o \left(t_{on} + t_{off} \right) f_{sw} \tag{2-2}$$

where V_o is the voltage across the diode D_d and the semiconductor switch S, and f_{sw} denotes the switching frequency of the switch S. The following can be determined:

- The switching loss is proportional to f_{sw}, which implies that high frequency operation desired by a HPD requirement has to face a high P_{sw} with hard switching. This leads to a soft-switching solution as explained in Section 2.3.1.
- Large switching times t_{on} and t_{off} increase the switching loss.

Switching intervals (t_{on} and t_{off}) are mainly caused by the parasitic capacitances across semiconductor electrodes and the parasitic inductance distributed in the interconnection of semiconductors and the external routing wires [2-8]. A smaller die area enables smaller parasitic capacitances and hence, is able to accelerate the switching speed for a smaller P_{sw}. However,

as aforementioned, a decreased die area will boost the conduction loss. Therefore, an optimal die area exists to achieve the balance between switching loss (parasitic capacitance) and conduction loss (on-state resistance) in a given electrical stress condition. The parasitic inductance will slow down the switching process [2-9] and excite waveform oscillations with the parasitic capacitances of semiconductors during switching transients [2-8][2-10]. Both effects increase the switching loss. As the switching frequency is raised catering to the power density requirement, the switching loss must be handled carefully.

2.2.2 Power Diode Losses

Power diode losses mainly consist of two parts: forward conduction loss and reverse recovery loss. The V-I characteristic of a forward-biased power diode is shown in Fig. 2.5. It implies that when conducting, the power diode, especially a PN diode, is equivalent to a voltage source (with forward voltage V_f) in series with a resistor R_d. Then, its forward conduction loss can be calculated with the following expression:

$$P_{d\_f} = V_f I_f + R_d I_f^2 \tag{2-3}$$

where I_f is the forward flowing current through the diode. The reverse-recovery loss occurs during the turned off process of a silicon PN junction diode. After the current reaches zero, the diode experiences a reverse current in order to sweep out the excess carrier charge stored in the drift region during the conducting state. The representative shape of this reverse recov-

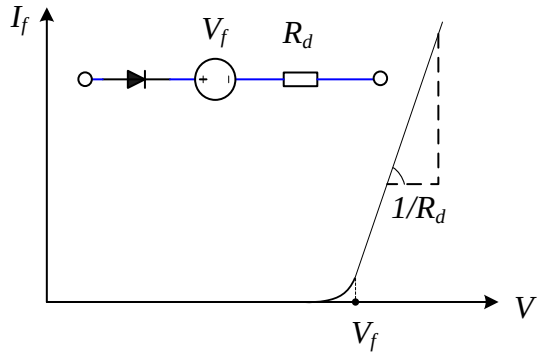


Fig. 2.5 V-I characteristic of a forward-biased power diode

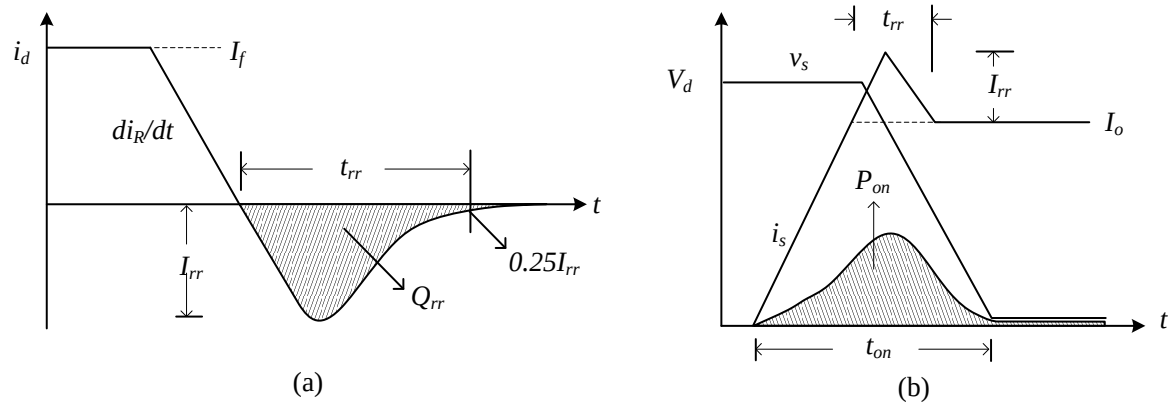


Fig. 2.6 (a) Diode reverse recovery current at turn-off; (b) reverse recovery current added to the switching current in the diode-clamped inductive switching network

ery current at turn-off is illustrated in Fig. 2.6(a). The reverse current with a peak value of I_{rr} during time t_{rr} forms the reverse recovery charge Q_{rr}. The reverse-recovery loss P_{rr} can be approximated as follows:

$$P_{rr} = Q_{rr} V_R f_{sw} \tag{2-4}$$

where V_R is the reverse voltage of diode, and f_{sw} is the switching frequency. Since Q_{rr} is proportional to the square of diode reverse breakdown voltage (V_{RBD}^2), the reverse recovery loss P_{rr} can be calculated as [2-11]:

$$P_{rr} \approx K_{rr} V_{RBD}^2 V_R f_{sw} \tag{2-5}$$

where K_{rr} is a material-related constant, V_R is the reverse voltage on the diode. It follows that a PN junction diode with a high reverse breakdown voltage rating tends to have a bigger reverse-recovery loss.

The diode reverse recovery phenomenon induces losses in other components. A diode-clamped inductive switching network (see Fig. 2.4(a)) is taken as a typical example of this. When the switch *S* is turned on, the diode reverse recovery current starts to flow the switch *S*, as illustrated in Fig. 2.6(b). This lifts the peak current that *S* has to switch on from I_o to $I_o + I_{rr}$ and hence, results in a higher transistor turn-on loss (P_{on}).

2.2.3 Magnetic Components

Losses in magnetic components can be grouped into two major categories: core loss and winding loss. The core loss occurs when the core is under AC excitation and winding loss is the ohmic conduction loss in the windings of magnetic components.

Magnetic Core Loss

The time-varying electromagnetic fields result in the magnetic core losses (P_c), which have three components: hysteresis loss (P_h), and classical and excess eddy current losses (P_{ce} and P_{ex}) [2-12]. Hysteresis loss is the energy lost in the domain wall motions caused by the AC magnetic field, which can be represented by the area enclosed by the B-H curve of the magnetic material. Classical eddy current loss results from eddy currents induced by the AC magnetic field; while excess eddy current loss originates from the inhomogeneous change of the magnetic field due to domain wall motion. Three terms can be calculated as shown below [2-13]:

$$P_h = k_h f_{sw} B_{pk}^{C_n} \quad P_{ce} = k_{ce} \frac{A_c}{\rho} f_{sw}^2 B_{pk}^2 \quad P_{ex} = k_{ex} \left(\frac{A_c}{\rho} \right)^{0.5} f_{sw}^{1.5} B_{pk}^{1.5} \tag{2-6}$$

where k_h, and C_n are material-related constants, k_{ce}, k_{ex} are material- and waveform-related constants, A_c is the cross-section area of the core, ρ is the electrical resistivity of applied core materials, and B_{pk} is the peak flux density. In practice, the total core loss is normally approximated using Steinmetz's equation (SE), given in Eq. (2-7):

$$P_c = P_h + P_{ce} + P_{ex} = C_m f_{sw}^{a} B_{pk}^{b} \ , \tag{2-7}$$

where C_m, a, b are Steinmetz constants, curve-fitted to approximate the summation of P_h, P_{ce} and P_{ex} . Normally, a certain set of C_m, a, b is provided in the material datasheet only for the specific application of the material.

It is should be noted that SE is only applied for sinusoidal excitation. However, in the PE converters and AC motors, non-sinusoidal excitation waveforms are more often seen. To solve this discrepancy, many core loss calculation methods derived from SE have been proposed: the Modified Steinmetz equation (MSE) [2-14] is applied to non-sinusoidal excitation cases, by involving the dependency of the excitation voltage derivative on the core loss., The Generalized Steinmetz equation (GSE) [2-15] overcomes some anomalies in MSE, e.g. in cases where magnetizing current contains large sub-harmonics. Furthermore, the improved GSE (iGSE) [2-16] adds the consideration of minor hysteresis loops of excitation to GSE; while the improved iGSE (i^2GSE) [2-16] further considers the core loss when the magnetic flux is constant. These methods are more widely applicable with higher accuracy than the original equation, but are still limited to a certain frequency range where the Steinmetz constants are characterized. Roshen [2-13] proposed a loss calculation method that can not only be applied to all operating frequencies, but also takes into account the core dimension effect. However, the experimental extraction of many parameters required by this method makes it less practical [2-17].

Winding Loss

The windings in magnetic components are exposed to the time-varying AC magnetic field, which can significantly disturb the homogeneous current distribution across the conductor cross-section area. As a result, it raises the winding loss compared with those present in the DC case.

Two AC effects contribute to the increase of winding losses: skin effect and proximity effect. Skin effect occurs due to the AC magnetic field induced by AC current in the conductor itself, whereas the proximity effect is induced by adjacent conductors. The skin effect tends to push the current in a thin layer of skin depth around the conductor surface, resulting in a shrunken current-flowing cross-section area. Meanwhile, the proximity effect increases the RMS value of extra eddy currents in conductors close to each other, despite maintaining their net current unchanged. Ferreira [2-18] has proved that the losses induced by the skin effect and proximity effect (P_{sk} and P_{prx}) are orthogonal to each other, therefore the winding loss can be described as follows:

$$P_w = P_{sk} + P_{prx} \ . \tag{2-8}$$

Dowell [2-19] has proposed an analytical winding loss calculation method, assuming a one-dimensional (1D) magnetic field distribution between windings. This assumption is realistic for wide and planar windings. In Appendix A, the loss of a planar winding with multiple turns

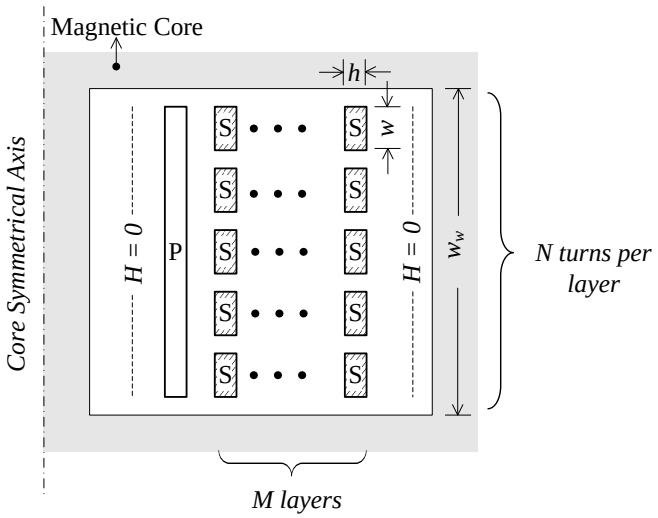


Fig. 2.7 The cross-section view of a transformer core with a 1-turn planar primary winding and an N x M turn planar secondary winding

and layers is derived based on this method. The configuration of this planar winding is illustrated in Fig. 2.7, where the primary winding has one layer and the secondary winding has *M* layers and *N* turns per layer. The conductor height and width of the secondary winding are *h* and *w*, respectively, and the winding window of the core (grey color) has a width of w_w. Note that this configuration can be a section of interleaved winding structure which bears zero magnetic field intensity on both sides. The skin-effect loss and proximity-effect loss of the secondary winding are derived as (see Appendix A):

$$P_{sk} = R_{DC}\frac{\nu}{2}\frac{\sinh\nu+\sin\nu}{\cosh\nu-\cos\nu}\cdot I_{rms}^2 \tag{2-9}$$

$$P_{prx} = \nu R_{DC}\frac{\sinh\nu-\sin\nu}{\cosh\nu+\cos\nu}\cdot\frac{4M^2-1}{6}N\cdot I_{rms}^2 \tag{2-10}$$

where R_{dc} is the DC resistance of this winding, I_{rms} is the RMS value of sinusoidal current, and ν is the normalized conductor height *h* related to skin depth δ ($\nu = h/\delta$). The skin depth δ is expressed as:

$$\delta = \sqrt{\frac{1}{\pi\mu\sigma f_{sw}}} \tag{2-11}$$

where μ is the permeability, σ is the conductor conductivity, and f_{sw} is the frequency of the sinusoidal current. The skin-effect loss and proximity-effect loss can be normalized to DC loss $R_{dc}I_{rms}^2$, then the normalized skin-effect loss and proximity-effect loss factors (F_{sk} and F_{prx}) are:

$$\begin{aligned} F_{sk} &= \frac{\nu}{2}\frac{\sinh\nu+\sin\nu}{\cosh\nu-\cos\nu} \\ F_{prx} &= \nu\frac{\sinh\nu-\sin\nu}{\cosh\nu+\cos\nu}\cdot\frac{4M^2-1}{6}N \end{aligned} \tag{2-12}$$

As is shown, loss from skin effect is only related to the skin depth, while the proximity loss is not only influenced by the skin depth, but more importantly, by the winding configuration, especially the number of winding layers (*M*). Fig. 2.8 illustrates two normalized loss factors as a function of normalized skin depth and number of winding layers. Based on this, the following can be concluded:

- Smaller normalized conductor height will reduce both skin loss and proximity loss.
- Multiple layers will significantly lift proximity loss.
- Assuming the conductor height is constant, higher frequency results in larger normalized conductor height, and hence, causes higher losses.

Capacitor Loss

When the capacitor experiences an AC current, the charges in its dielectric material are displaced from one direction to the other. During this polarization process, a part of electrical energy is absorbed by the dielectric materials, which is known as the dielectric loss. Together

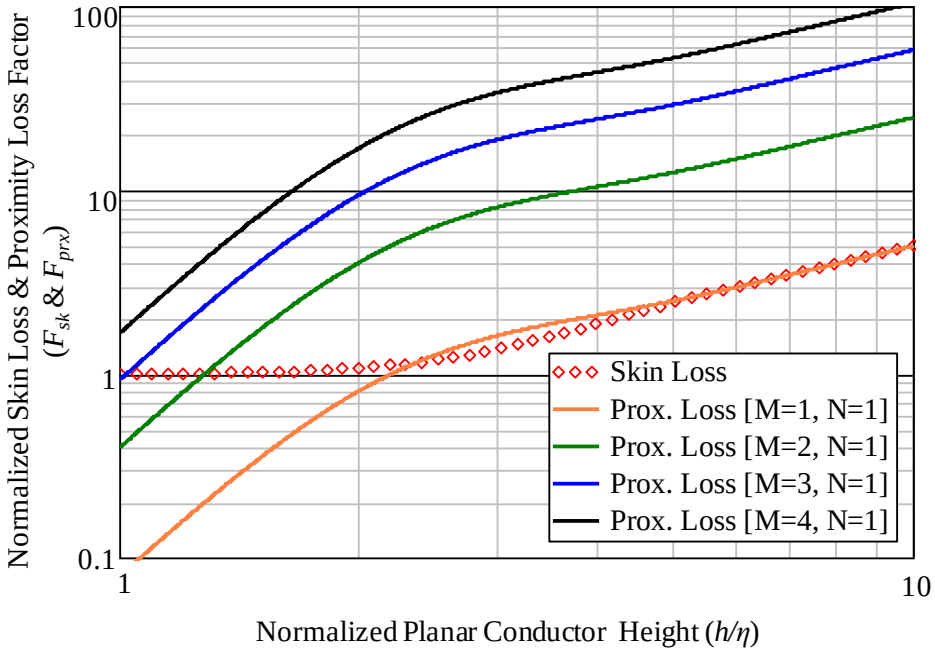


Fig. 2.8 Normalized skin loss and proximity loss as a function of normalized planar conductor height at different number of winding layers (M)

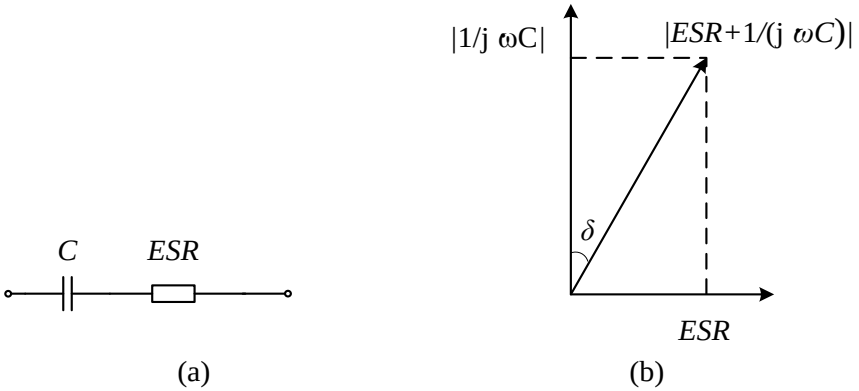


Fig. 2.9 (a) Simplified lumped equivalent capacitor model; (b) capacitor impedance vector

with the ohmic loss in the electrode plates and terminals leads, these two loss sources comprise the capacitor loss. In a lumped capacitor model, these losses can be regarded as an equivalent series resistance (ESR) in series with an ideal capacitor (Fig. 2.9(a)). ESR causes a small angle δ between the capacitor's impedance vector (|ESR+1/j·ωC|) and the reactance vector (|1/ωC|) [2-20], as shown in Fig. 2.9(b). ESR can be estimated by:

$$ESR = \frac{\tan\delta}{2\pi f_{sw} C} \tag{2-13}$$

Then, the loss in the capacitor can be calculated as:

$$P_{cap} = ESR \cdot I_{rms}^2 = \frac{\tan\delta}{2\pi f_{sw} C} \cdot I_{rms}^2 \tag{2-14}$$

where I_{rms} is the RMS value of the AC current flowing through the capacitor. It can be found that the smaller dissipation factor, higher capacitance and current frequency help to reduce the capacitor loss.

The dissipation factor and capacitance values are determined by the capacitor technologies. Examples of mainstream capacitor technologies are electrolytic, metalized film, ceramic, and tantalum. Different technologies offer the capacitors with varied dissipation factor and capacitance ranges, which indicate different loss properties. After an extensive survey on many capacitor manufacturers, the voltage and capacitance range, dissipation factor and maximum energy density of the commercial capacitors are summarized in TABLE 2.2 according to capacitor types.

TABLE 2.2 PROPERTIES OF DIFFERENT CAPACITOR TECHNOLOGIES

Capacitor Type	Manufactures	Dielectric Type	Voltage [V]	Capacitance [μF]	Dissipation Factor	Max. Energy Density [J/cm^3]
Electrolytic Capacitor	Rubycon	Alumina (Liquid)	6.3 ~ 450	0.1μF~68mF	8~35 @ 120 Hz	4.76
	Murata	Polymer (Solid)	2 ~ 16	6.8 μF ~ 470 μF	ESR@100kHz: 6~30 mΩ	0.06
Tantalum Capacitor	AVX	Tantalum (MnO_2)	2.5~125	0.1 μF ~ 1.5 mF	ESR@100kHz: 3~500 mΩ	0.673
Multilayer Ceramic Capacitor (MLCC)	Samsung	Class I (C0G)	6.3~3000	0.2 pF ~ 0.15 μF	0.1 @ 1 kHz	0.06
		Class II (X7R)	6.3~2000	0.1 pF ~ 4.7 μF	2.5 @ 1 kHz	0.44
Film capacitor	EPCOS	Polyester	63~12500	68 nF~220 μF	0.8 @ 1 kHz	0.1
		Polypropylene	160~3000	68 nF~110	0.1 @ 1 kHz	0.27
	Vishay	Polycarbonate	63~400	0.22nF~10	0.3 @ 1 kHz	0.1

Electrolytic capacitors provide the highest capacitance values among popular capacitor technologies. However, due to the relatively large ESR and equivalent series inductance, electrolytic capacitors, especially the ones with liquid electrolyte, normally have slow dynamic response and therefore, are generally utilized for line frequency energy storage and bus voltage stabilization. Additionally, thanks to their superior loss handling capability resulting from their bulky volume, the liquid aluminum electrolytic capacitor is almost the only option to carry the low-frequency power current in PE converters [2-21].

Tantalum capacitors have fairly low ESR and quite a wide capacitance range. However, their use is limited by the low voltage rating, short-circuit failure mode and costs.

Multi-Layer Ceramic Capacitors (MLCC) and metal film capacitors provide low dissipation factor and very wide voltage range. They are always used to filter out high-frequency ripple current due to fast dynamic response. Metal film capacitors outperform MLCC in terms of high voltage handling capability, but MLCC attracts attention due to their better energy density.

2.2.4 Other Losses

In high-frequency converters, the loss in semiconductor drivers cannot be neglected. In high-current converters, the conduction loss of the parasitic resistance is not trivial. They are explained below.

Losses in semiconductor drivers

The gate capacitances of semiconductors, such as MOSFET and IGBT, need to be charged and discharged to switch semiconductors on and off. The flow of these charges generates losses on the drive resistors and the internal resistor of the driver IC, and this loss P_{dr} can be predicted as

$$P_{dr} = Q_{g.tot} V_g f_{sw} \tag{2-15}$$

where $Q_{g.tot}$ is the gate charge and V_g is the applied drive voltage. It can be concluded that higher switching frequency and higher gate charge both cause a proportionally higher driver loss. Gate charge depends on the transistor gate capacitance. Transistors with wider die area, aiming at high-current application, generally cause bigger gate charge and larger drive loss.

Losses in parasitic resistances

Parasitic resistances of the interconnection mechanism exist between components, such as the PCB track, PCB vias, solder, and the contact of connectors. In high-current converters, all of these parasitic resistances generate conduction losses that can decrease efficiency and even harm system reliability [2-22][2-23]. Additionally, the resistance of shunt resistors for current measurement is another possible heat source, so placement of the shunt resistor in the high-current loop should be avoided [2-24].

2.3 Loss Reduction Methods

This section reviews and evaluates loss-reduction methods. Since the losses in semiconductors, magnetics and capacitors dominate the total converter losses, only their loss reduction methods are considered here.

2.3.1 Loss Reduction in Power Transistors

For compact volume PE converters with a voltage below 600V, power MOSFET is generally a better option than power bipolar transistors or Insulated-Gate Bipolar Transistors (IGBT), due to its faster switching speed. Since this work focuses on the HPD design of high current converters, only the loss reduction in power MOSFETs will be discussed below.

Conduction loss

The reduction of conduction loss of power transistors is important to the heat generation management of high-current converters. It can be realized by decreasing the device resistance and RMS current value required to deliver certain power to loads.

Die resistance

The drift layer resistance makes up a large part of MOSFET die resistance. It is given in Eq. (2-1) and is re-written here.

$$R_{on.sp} = \frac{4V_{BD}^2}{\varepsilon \mu_n A_{drift} E_c^3} \tag{2-16}$$

It can be observed that the drift layer resistance can be reduced as follows:

- The breakdown voltage V_{BD} should be kept as low as possible compared with the converter input or output voltages.
- Enlarging the die area of single MOSFET or paralleling multiple MOSFETs reduces the total drift layer resistance in the current flowing path.
- Semiconductor materials with higher E_c, such as wide band gap materials SiC and GaN, decrease channel resistance [2-25].

Parasitic resistances in the interconnection

Numerous efforts have been attempted to reduce parasitic resistance in packaging – the so-called Die Free Package Resistance (DFPR). Fig. 2.10 illustrates the DFPR evolution of high-current MOSFETs from International Rectifier [2-27]. Selecting the packaging with low DFPR always helps to lower the conduction loss.

RMS current

Different DC-DC topologies have various RMS current values when feeding the same load. One can select a topology and its operating mode that generates less RMS current value. Fig. 2.11 represents four typical current waveforms of magnetic components in DC-DC converters. Note that these current are the sums of semiconductor currents in converters.

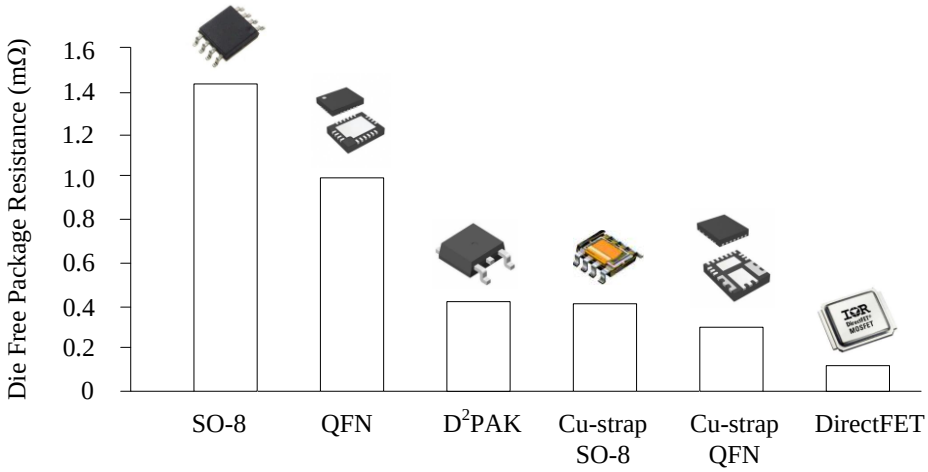


Fig. 2.10 DFPR evolution of high current MOSFETs from IR [2-27]

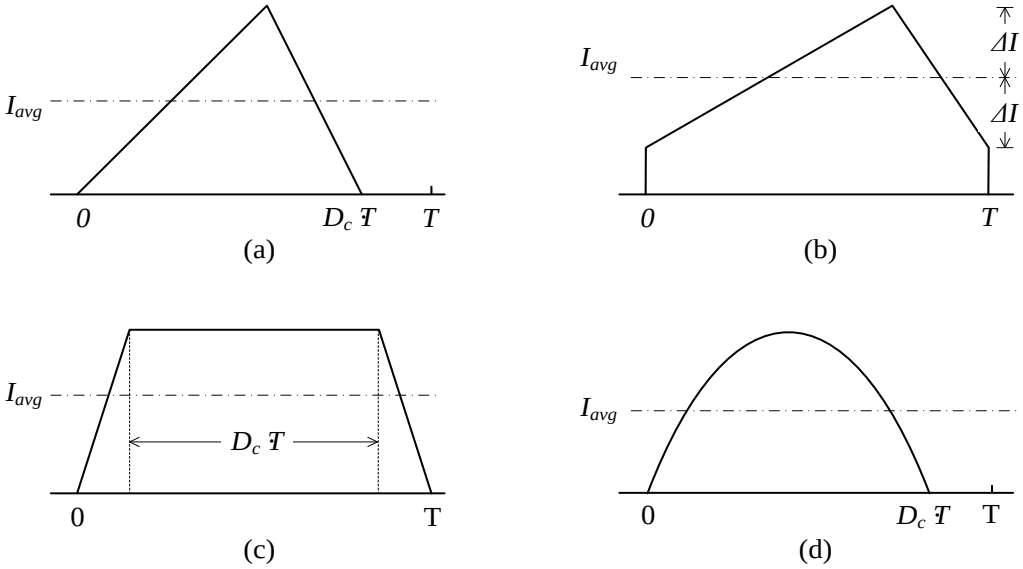


Fig. 2.11 Four typical current waveforms within PE converters

- Fig. 2.11(a) and (b) show the inductor current of Discontinuous and Continuous Conduction Modes (DCM and CCM), in duty-ratio controlled converters, such as buck, boost, buck-boost and flyback; Here, D_c indicates the ratio between the conduction time of the inductor and the switching period (T), ΔI is the magnitude of the current ripple in CCM.
- Fig. 2.11(c) represents a typical transformer current in phase-shift-controlled converters, such as a DAB converter. Here, D_c is the ratio between the conduction time of flat current part and switching period.
- Fig. 2.11(d) illustrates the transformer current in quasi-resonant or load resonant converters. Here, D_c means the ratio between the conduction time of the transformer.

The ratio between the RMS current value (I_{RMS}) and the average current value (I_{AVG}) reflects to a great extent how much the conduction loss can be delivered at the same power. These ratios of four waveforms as a function of D_c are presented in TABLE 2.3. In Fig. 2.12, these ratios are compared for D_c ranging from 0.8 to 1, wherein I_{RMS} / I_{AVG} of CCM triangular wave-

TABLE 2.3 I_{RMS}/I_{AVG} RATIOS OF FOUR TYPICAL CURRENT WAVEFORMS WITHIN PE CONVERTERS

Waveforms	DCM Triangular	CCM Triangular	Trapezoidal	Sinusoidal
I_{RMS} / I_{AVG}	$2\cdot\sqrt{\frac{D_c}{3}}$	$\sqrt{1+\frac{1}{3}\left(\frac{\Delta I}{I_{AVG}}\right)^2}$	$\frac{2}{1+D_c}\sqrt{\frac{1+2D_c}{3}}$	$\frac{\pi}{2}\sqrt{\frac{1}{2D_c}}$

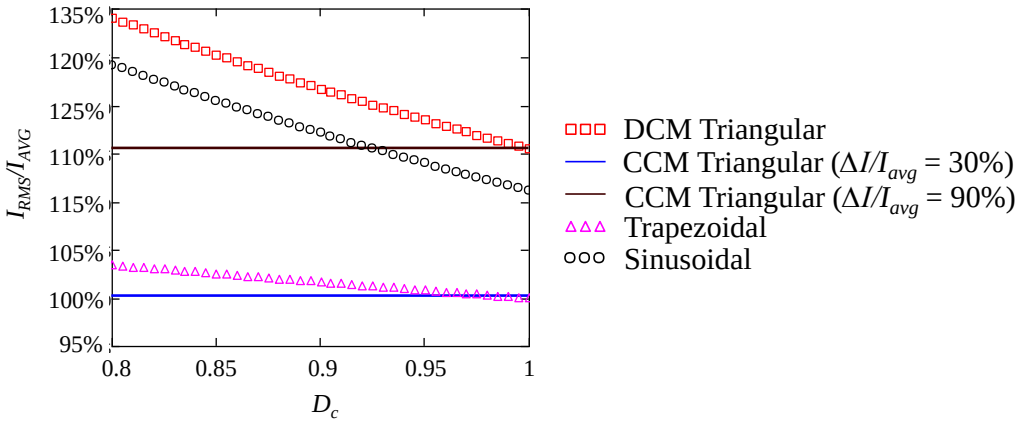


Fig. 2.12 I_{RMS}/I_{AVG} ratios plotted as a function of D_c

forms are illustrated with $\Delta I/I_{AVG}$=50% and 90%, respectively. The following can be concluded:

- Trapezoidal waveforms bear the smallest RMS value of other all other cases for D_c >0.8, so the converters with trapezoidal current waveforms are the preferable options for high-current applications.
- The sinusoidal waveform has a lower RMS current value than a triangular waveform in DCM mode at the same D_c.
- CCM triangular waveform has a lower RMS value as the ripple current ΔI decreases. At $\Delta I/I_{AVG}$ approaches zero by increasing the inductance in the circuit, the RMS value gets closer to the average current.

Multiple semiconductors in parallel can also reduce the conduction loss, in which case the total conduction losses can be calculated as

$$P_{cond} = N \cdot R_{on}\left(\frac{I_{rms}}{N_s}\right)^2 = \frac{R_{on}I_{rms}^2}{N_s} \tag{2-17}$$

where N_s is the number of paralleled semiconductors. In this way, the total conduction loss can be reduced by a factor of N. When semiconductors are paralleled, equal current sharing is very important. MOSFETs, due to their positive temperature coefficient on resistance, are theoretically suitable for paralleling [2-28]. However, more parameters must be taken into account to realize the current balances among MOSFETs at not only at steady state but also at the transient state. These parameters include the threshold voltage, transconductance, internal capacitances, parasitic inductances and temperatures [2-29][2-30][2-31].

Switching loss

The switching loss can be decreased by following aspects: device structure [2-32][2-33][2-34] and packaging [2-37][2-38][2-39][2-40], active drive control [2-35][2-36], auxiliary snubber circuit [2-28][2-41] and soft-switching techniques. Device-level improvements focus on less parasitic inductance and capacitance, while drive control and snubber circuits require extra components and increased costs to achieve low switching loss.

The following discussion is limited to soft-switching techniques, as they are most widely used to reduce the switching loss of semiconductors. Soft-switching is to avoid simultaneous high voltage and high current over semiconductor devices, when the device traverses from conducting to blocking state or otherwise. Taking the turn-off interval as an example, the typical hand and soft turn-off waveforms are shown in Fig. 2.13(a) and (b). Compared with hard-switching, soft-switching has a reduced overlapping area of voltage and current, and causes less switching loss. Soft-switching DC-DC converters can be categorized into three main groups: quasi-resonant converters, load-resonant converters and intermittent resonant converters. All of them create a resonant process for soft-switching.

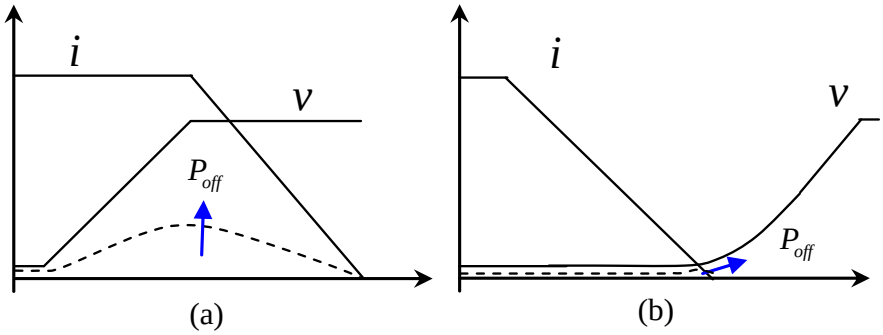


Fig. 2.13 (a) Hard-switching and (b) soft-switching turn-off process

Quasi-Resonant Converters (QRC)

In QRCs, a LC network is built around the switches in basic topologies, like buck, boost, buck-boost, SEPIC, Cuk. The resonance of LC network oscillates the voltage or current of the switch to zero, which creates the possibilities to achieve Zero-Voltage or Zero-Current Switching (ZVS or ZCS). The circuit diagrams of ZCS and ZVS quasi-resonant buck converters and their key waveforms are given in Fig. 2.14(a) and (b). Additional components diode D_1, an inductor L_r and a capacitor C_r are placed around the switch S in a normal buck converter to achieve the desired resonance. During different time intervals, the working states of semiconductors are indicated in the waveforms.

In the ZCS quasi-resonant Buck shown in Fig. 2.14(a), the switch current oscillates to zero at the time instant t_2 and switch S turns off naturally at zero-current. However, although S switched on with current starting at zero (t_0), the energy stored in the drain-source capacitance during off-state is still dissipated in the switch channel at turn-on, which actually causes a lossy turn-on. In the ZVS version Fig. 2.14(b), when the switch voltage oscillates to zero by res-

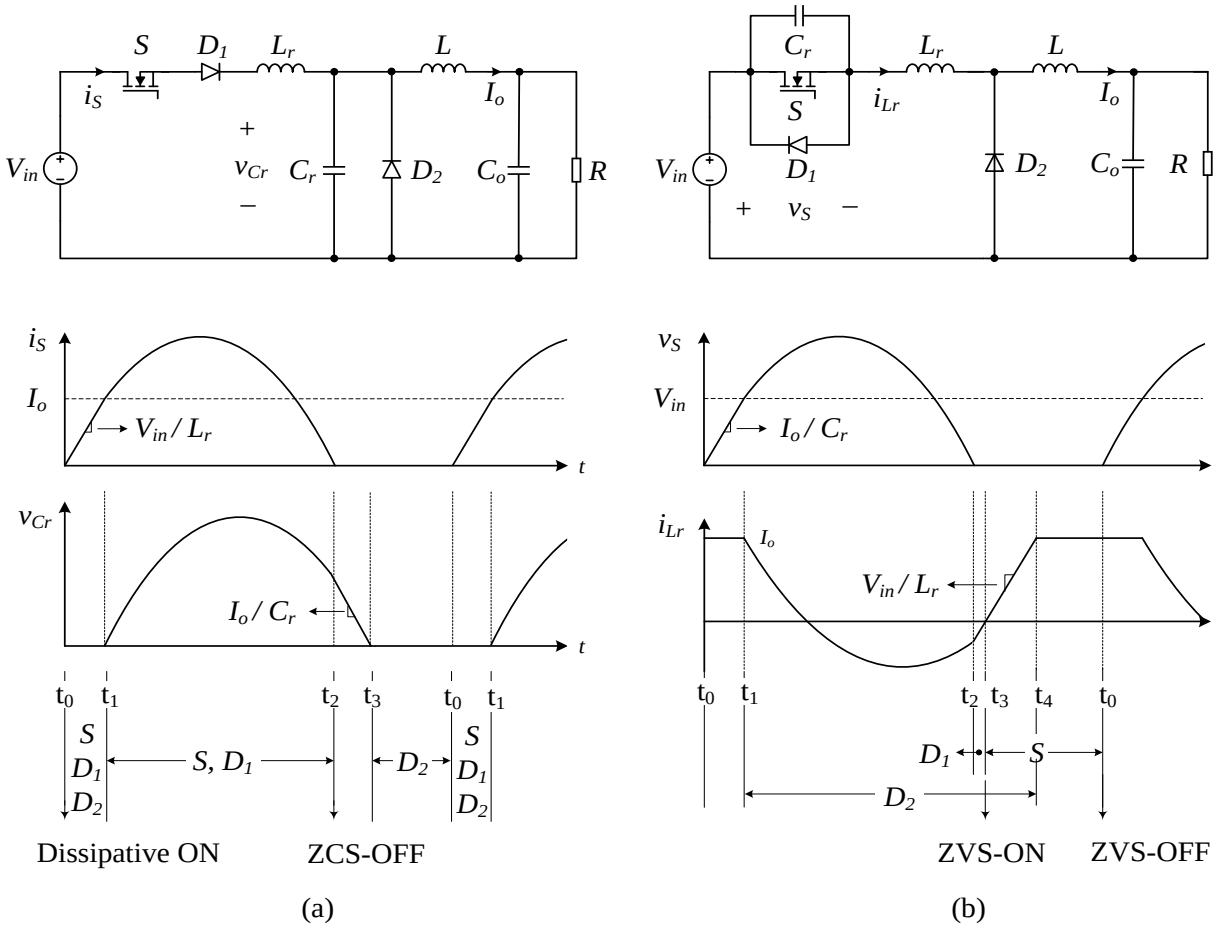


Fig. 2.14 Circuit diagrams and typical waveforms of (a) ZCS and (b) ZVS quasi-resonant Buck converter

onance, the anti-parallel diode D_1 of switch S starts conducting (t_2-t_3). During t_2-t_3, the gate of S is on and when the current in D_1 reaches zero due to freewheeling and then switch S is turned on with zero-voltage (ZVS-ON). When switch S is turned off at t_0, its voltage increases with a defined slope V_{in}/L_r. During the short switching interval, the switch voltage can be regarded as zero, which implies a ZVS-OFF. Comparing ZCS and ZVS quasi-resonant bucks, the switch in ZCS mode bears turn-on loss that equal to the energy in drain-source capacitance stored in off-state, while in ZVS quasi-resonant Buck, the switch barely has any loss.

The switch with its associated resonance LC network is called “resonant switch”. Many variants of these "resonant switches" exist for various purposes [2-42]. It can be found that the ZVS cell has the resonance capacitor in parallel with the switch, while ZCS cells have the resonance inductor in series. Although soft-switching can be realized by these resonance switch cells, this is achieved at the expense of higher switch current or higher switch voltage [2-42]. Higher current induces higher conduction loss and semiconductors with higher voltage rating bear bigger on-resistance, which will further boost the conduction loss. The resultant higher conduction loss compromises the effort to achieve the soft switching in QRCs. Besides, the auxiliary resonance components have to be bulky to thermally handle the high power currents. Therefore, QRCs are not suitable candidates for high-current and HPD converter design.

Load Resonant Converter (LRC)

Soft-switching can be also created by other resonant processes. The name "Load Resonant Converter" refers to the fact that the load is part of the resonant circuit. There are basically two different types of LRCs, Series-Connected and Parallel-Connected Resonant Converters (SCRC/PCRC), whose names indicate the manner in which the load is connected with the resonance tank. Fig. 2.15 shows the equivalent circuits of SCRC and PCRC, where v_{in} is the voltage excitation source, formed by half or full switch bridge, and R_{eq} is the equivalent load referred to the resonant tank (L_rC_r). There are some hybrid variants of SCRC and PCRC, such as LLC [2-43] and LCC [2-44] circuits, mainly focusing on improving the controllability over the wide load variation.

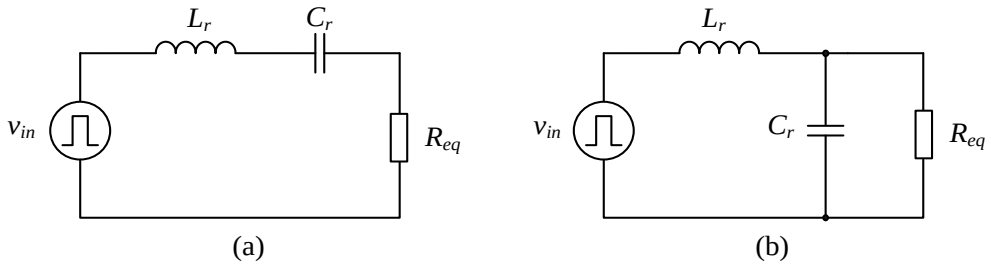


Fig. 2.15 Equivalent circuits of (a) SCRCs and (b) PCRCs

Utilizing the resonance between the LC tank and the load, the switches that form the square voltage excitation can be softly switched. Depending on whether the switching frequency is larger or smaller than LC resonant frequency f_r, the converter can operate in ZVS or ZCS mode. A full-bridge based SCRC and the waveforms of the resonant tanks are shown in Fig. 2.16.

In ZVS mode (Fig. 2.16(b)), switches turn on (t_1, t_3) after the current in their anti-paralleled diodes is freewheeled to zero. At this moment, the voltage across switches is zero and a ZVS turn-on is achieved. By doing so, the diode reverse recovery loss is also largely reduced. To achieve a less lossy turn-off process, a capacitor across the switch needs to be placed, which can be an external capacitor or the body capacitance of the switch. Fig. 2.17 zooms in this turn-off process of S_1 at t_2, during which the inductor current i_L is assumed as a constant current source. When S_1 is gated off, inductor current charges C_1 while discharges C_2 (Fig. 2.17(b)). As the voltage across C_2 (v_b) reaches zero or voltage across switch (v_a) reaches the input voltage V_{in}, the inductor current starts flowing through D_2 (Fig. 2.17(c)). During this process, C_2 releases energy but C_1 stores it, the difference between the stored and released energy is the loss dissipated [2-45], which is very low.

In LRCs, soft-switching conditions are created without additional components in the power stage, like QRCs. However, the resonant capacitors have to handle the full power current. This means that bulky capacitors have to be used to handle the thermal problems in high-current applications, which will increase system volume.

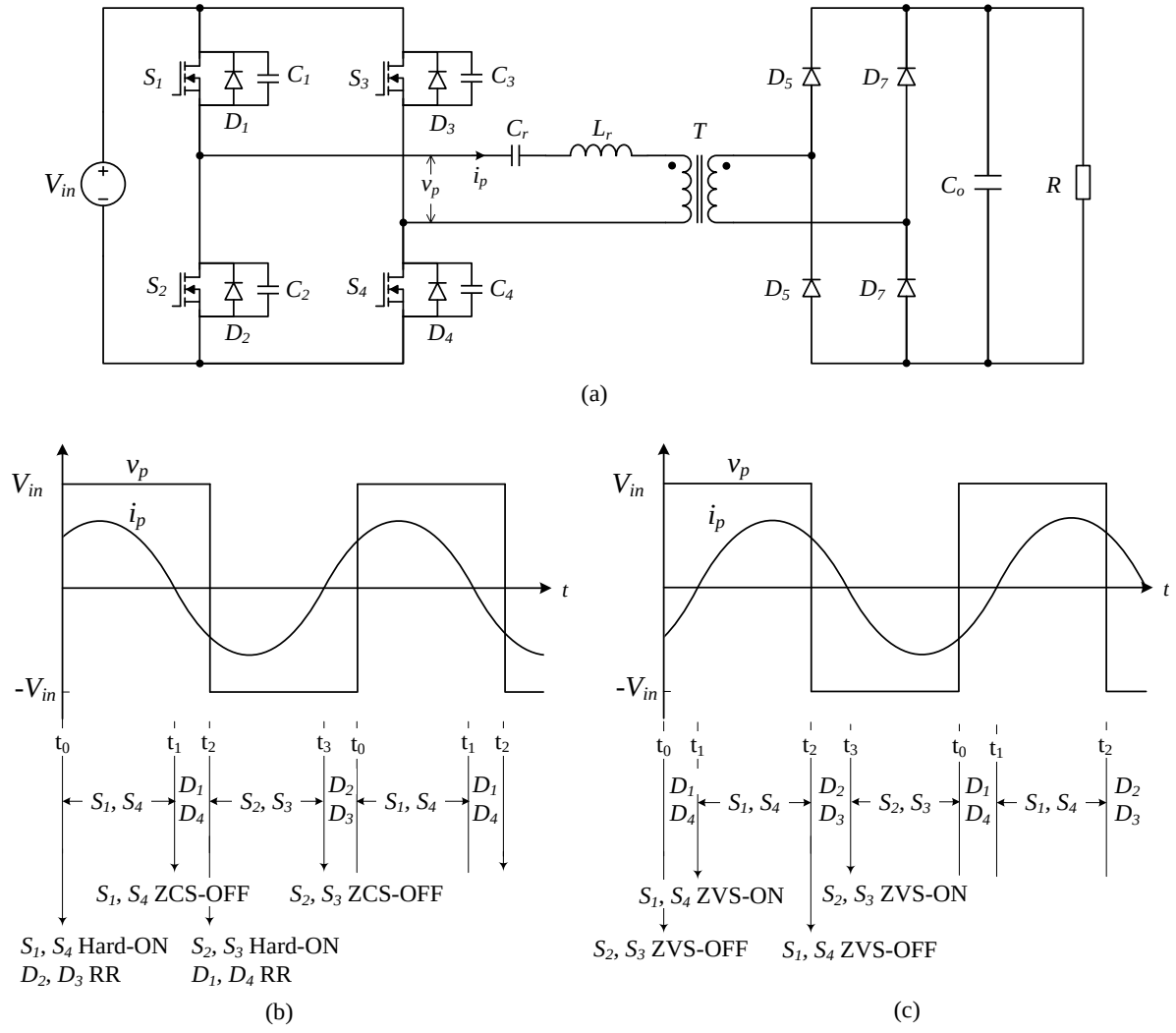


Fig. 2.16 (a) Circuit diagram of a SCRC and the resonant tank waveforms in (b) ZVS and (c) ZCS modes

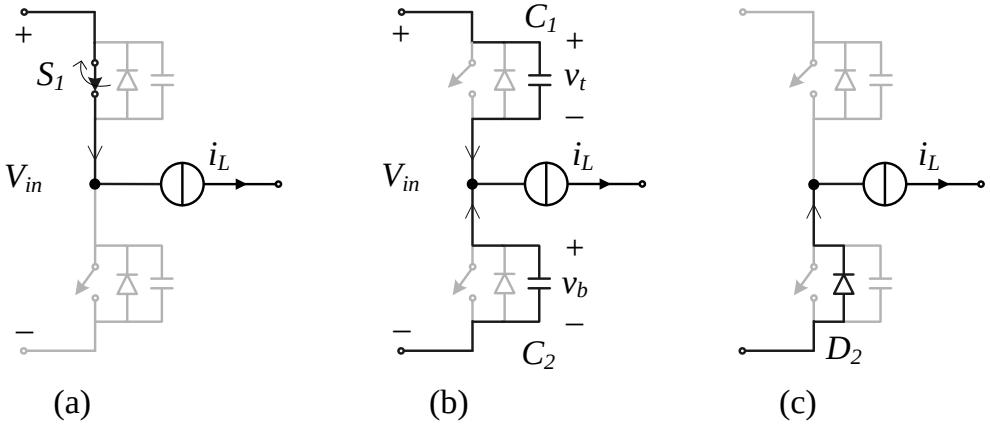


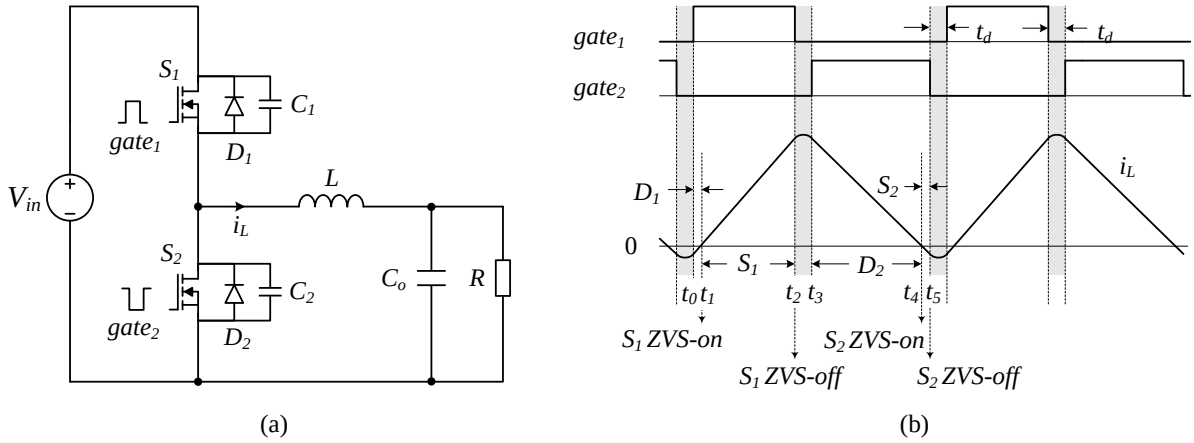
Fig. 2.17 A less lossy turn-off process in the full-bridge configuration with an inductive load

Partially Resonant Converters (PRC)

Some topologies achieve soft-switching only by realizing a resonance only within the switching intervals. They can be referred to as the partially resonant converters. Typical topologies

includes synchronous buck/boost converter [2-46], dual active full/half bridge converter [2-47][2-48].

A synchronous buck converter (Fig. 2.18a) operated in DCM can be taken as an example, with its inductor current and gate voltages shown in Fig. 2.18(b). Before t_0, C_1 resonates with the inductor L and is discharged. When the voltage over C_1 is very low at t_0, switch S_1 is turned on with ZVS. When S_1 turns off at t_2, the inductor charges C_2 and discharges C_2 through the same process described in Fig. 2.17, so S_1 turns off with very low loss.



(a) (b)

Fig. 2.18 Circuit diagram of synchronous buck converter (a) and its DCM waveforms (b)

PRCs are able to achieve the resonance process with the least components compared with QRCs and LRCs. Moreover, PRCs do not have a capacitor that carries the full power current, which eliminates the need for a bulky capacitor to handle the heat. Therefore, PRCs are better soft-switching topologies for high-current applications.

2.3.2 Loss Reduction in Power Diodes

Diode losses can be reduced in several ways:

- Converters should be designed in such a way that the blocking voltage of the diode is close to the converter terminal voltages. This implies that the reverse voltage rating of diodes and the according reverse recovery charges can be minimized, according to Eq. (2-5).

- Diodes with faster reverse recovery speed should be chosen. Table 2.4 [2-49] lists various Si diodes with their reverse breakdown voltage V_{RBR}, forward voltage V_f and reverse recovery time t_{rr}. Here, the Schottky Barrier Diode (SBD) exhibits the lowest V_f and the shortest t_{rr}, which implies the lowest conduction loss and lowest reverse recovery loss. This is a result of its metal-to-semiconductor junction construction. However, the limited reverse voltage blocking capability (<200V) disables the use of Si SBD in high-voltage applications.

TABLE 2.4 REVERSE BREAKDOWN VOLTAGE V_{RBR}, FORWARD VOLTAGE V_F AND REVERSE RECOVERY TIME T_{RR} OF DIFFERENT SI DIODE [2-49]

Type	V_{RBR} (V_{rrm})	V_f	t_{rr}
Si Schottky Barrier Diode	15 V ~ 200 V	0.3V ~ 0.8 V	< 10 ns
Si Supper Fast Diode	50 V ~ 600 V	0.8 V ~ 1.2 V	25 ns ~ 35 ns
Si Ultra-Fast Diode	50 V ~ 1000 V	1.35 V ~ 1.75 V	50 ns ~ 75 ns
Si Fast Recovery (Epitaxial) Diode	50 V ~ 1000 V	1.2 V	100 ns ~ 500 ns
Si Standard Recovery Diode	50 V ~ 1000 V	1.0V	1 μs ~ 2 μs

- DCM operation does not completely remove reverse recovery process, but it does not trigger extra loss in other transistors [2-55].
- The emergence of Wide Band-Gap (WBG) semiconductor material makes the high voltage SBD possible, enabling much higher efficiency of HV rectification [2-50].

2.3.3 Loss Reduction in Magnetic Components

Core Loss

Decreasing excitation frequency or peak flux density reduces magnetic core loss; however, it is difficult to improve the power density of magnetic components. Employing a better transformer structure or magnetic material offers an alternative solution.

Following material property is preferable for small core loss:

- Small coercive force: The hysteresis loss depends on the coercive force of the applied core material [2-12]. By adding addictives to the iron metal such as silicon, materials with a small coercive force can be made to have a very narrow hysteresis loop and hence a low hysteresis loss.
- Increase electrical resistivity: The classical and excess eddy current losses decrease as the material's electrical resistivity increases Eq.(2-6). Since ferrite material bears much higher electrical resistivity than iron-based material, they are preferable for use at high switching frequency ranges

Some magnetic materials have low electrical resistivity, such as amorphous alloys, nanocrystalline and iron-based materials, but their core structures are adapted to reduce their eddy loss at high frequency:

- *Laminated structure*: Such cores are made from stacks of many thin laminations, electrically insulated from each other by a thin insulating coating. For the amorphous alloys and nanocrystalline materials, the lamination thickness can vary within the range of 10-50 μm.

- *Powder structure*: Powdered iron cores consist of tiny iron particles that are resin bonded and are, as such, electrically isolated from each other. The size of the particles is smaller than the skin depth of applied frequency, therefore resulting in a quite high resistivity of the material and leading to low eddy currents.

Ferrite materials outperform most iron-based magnetic materials in high-frequency ranges. Nanocrystalline materials recently exhibit more superior properties, such as higher saturation level (1.2-1.5 T), higher thermal conductivity and higher operating temperature. This part will be discussed in details in Chapter 5.

Paralleling multiple inductors and interleaving their current phase can also reduce the core loss. Integrating these units in one magnetic core allows for a smaller core size [2-51].

Winding Loss

Winding loss reduction in the high-frequency transformers is of great importance for an efficient high-current isolated DC-DC converter design. To reduce winding losses, decreasing the DC resistance of windings and alleviating the AC effect are two feasible approaches.

- *Decrease DC resistance*. The most practical way to decrease DC resistance is to minimize the number of winding turns or increase the winding cross-section area. However, less turns indicate that the peak flux density within the core under the same excitation will be raised, which in turn causes higher core loss. (This will be discussed in detail in Chapter 5.)
- *Decrease AC resistance.*
  - The skin depth effect limits the effective current flowing area. A thin, but wide foil conductor [2-52], Litz wire or even planar Litz wire can be used to extend the effective conductor cross-section area.
  - The proximity effect significantly boosts the winding loss when the number of winding layers is high [2-28]. An interleaved winding structure can effectively mitigate the proximity effect on increasing winding loss (as explained in Appendix A).

2.3.4 Loss Reduction in Capacitors

Assuming the capacitance has been specified in the design and according to the capacitor loss equation (Eq. (2-14)), the dielectric dissipation factor, frequency and current RMS value are considered as three approaches to reducing the capacitor loss. Possible solutions are summarized in Fig. 2.19 with explanations to follow.

Increase the frequency of current ripple

Increasing the frequency of the current ripple results in a decrease of the capacitor ESR. Besides boosting the switching frequency of semiconductors, interleaving converters can also increase the frequency of capacitor current. Instead of a single converter (Fig. 2.20 (a1)), an

interleaved converter (Fig. 2.20 (b1)) connects multiple identical converter units in parallel and shares the same input and output capacitors. The PWM control signals to each unit are equally phase-shifted apart in one switching cycle. The summation of the phase-shifted currents flowing into each unit ($i_{\Phi 1}$+ $i_{\Phi 2}$+ $i_{\Phi 3}$) results in a much higher frequency and smaller magnitude of current ripple (Fig. 2.20(b2)) in common capacitors compared with those in a non-interleaved converter (Fig. 2.20(a2)). This decreased current ripple not only reduces the capacitor losses, but also diminishes the need of large capacitors to limit the voltage ripples at input and output, thus helping to increase efficiency and the power density [2-53][2-54]. The drawback of an interleaved isolated DC-DC converter is that multiple magnetic components are used and core losses are increased.

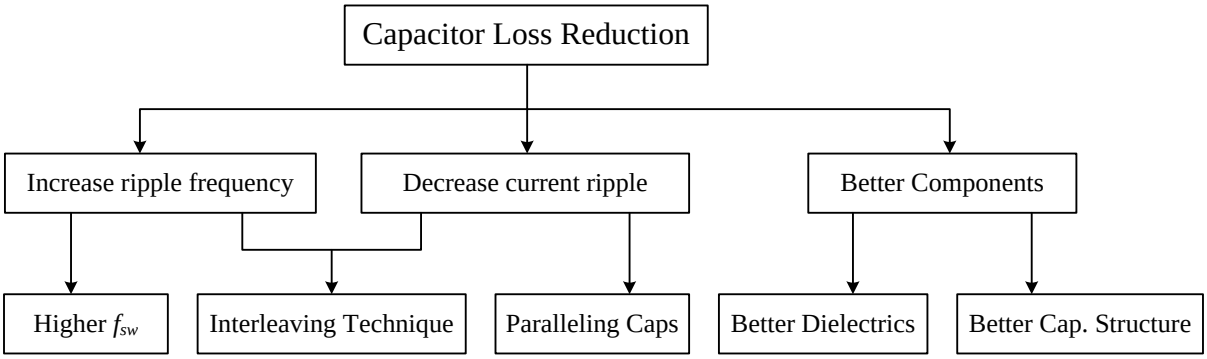


Fig. 2.19 Overview of the capacitor loss reduction methods

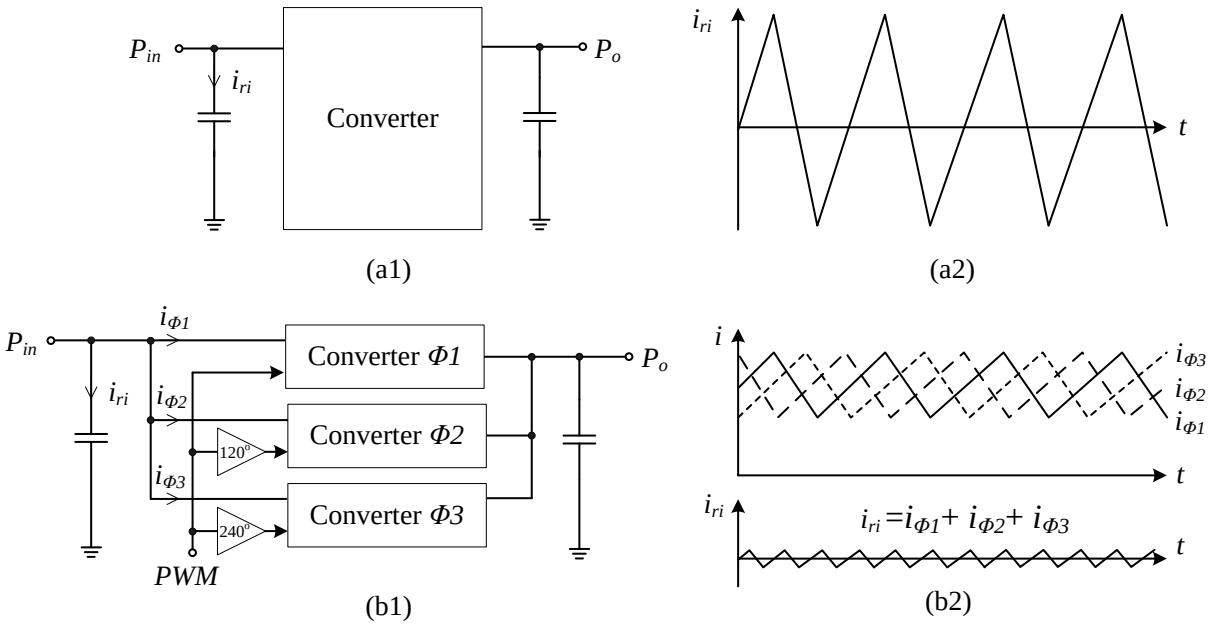


Fig. 2.20 Simplified circuit diagram and input capacitor current waveforms of (a) single unit converter and (b) interleaved converter (3 units)

Decrease the current ripple magnitude

Current ripple magnitude can be decreased by putting multiple capacitors in parallel to share the current, which results in reduce the total loss in the capacitors.

Better component technology can reduce ESR

The capacitor ESR consists of two main parts: dielectric resistance and interconnection resistance. A dielectric material with a lower dissipation factor improves dielectric resistance, while electrode metal with higher electrical conductivity or improved electrode structure helps to reduce interconnection resistance. Solid polymer electrolytic capacitors are famous for their low ESR due to more efficient material and large capacitance density and would be appropriate for use in high-current applications.

When experiencing a larger current ripple or even entire power current flowing through, bulky capacitors like liquid electrolytic capacitors are often deployed to handle the large loss, due to their large volume and surface area. However, these bulky capacitors largely increase the system volume. Therefore, carrying the full power current by an electrolytic capacitor is unwanted for HPD system design.

2.4 Conclusions

Losses generated in PE systems are dissipated in the form of heat, and hence, they are the issue at which the proposed thermal management approach is aimed. Three basic loss-related issues are addressed in this chapter, providing a background to the following heat-generation management chapters:

- Loss generation mechanisms in key power components
- Loss calculation equations
- Loss reduction methods

In high-current applications where compact system volume is also preferred, the conduction and switching functions are found to generate great mount of losses during the power processing. The major power components that deliver these two functions include power semiconductors, magnetic components and capacitors. Their losses can be reduced at the component level, circuit level and system level.

Loss-reduction methods at component level

For power semiconductors

- Devices with low parasitic elements are preferred with both high-current and high-frequency applications.
- Paralleling devices reduce the total on-resistance. However, current balancing among all devices should be treated carefully.
- WBG devices inherently bear lower on-resistance and faster switching speed.

For magnetic components

- Windings with larger cross-section area and interleaved structure help to reduce DC and AC resistance.
- Less winding turns reduce winding resistance but boost core loss at the same time.

- Better core materials reduce the core loss at high frequency, such as ferrites, nanocrystalline and amorphous alloy. For nanocrystalline and amorphous materials, a laminated core structure is required to reduce eddy current loss, which should be considered in core geometry design.

For capacitors

- Capacitor ESR is reduced by higher-frequency, more efficient packaging techniques and better dielectric material with high energy density.
- Paralleling capacitors
- Avoid carrying the full power current in capacitors

Loss-reduction measures at circuit level

- Deploy a circuit topology that generates less RMS current value to deliver the same power to load. It is found that the topologies with quadrilateral or CCM triangular current waveforms are preferred for high-current applications.
- Avoid a circuit topology that requires higher semiconductor voltage rating than terminal voltages.
- Soft-switching is preferred to lower switching loss. PRCs are preferred over QRCs and LRCs because they use less components and avoid carrying high current through capacitors.

Loss-reduction measures at system level

- Paralleling multiple converter units helps to reduce total system resistance. Phase-shifting these units can decrease the volume of decoupling capacitors and inductors.

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Chapter 3

High-Current Bidirectional Isolated DC-DC Topologies

3.1 Introduction

The basic structure of a bidirectional isolated DC-DC converter is illustrated in Fig. 3.1. It is characterized by two power conversion stages (A and B) located at each side of a transformer. When power flows from stage A to stage B, stages A and B behave as an inverter and a rectifier, respectively; in the reverse power flow, the functions of stages A and B are exchanged. The transformer, behaving as the galvanic isolation and AC link between two stages, preferably operates at high frequency so as to realize a compact size.

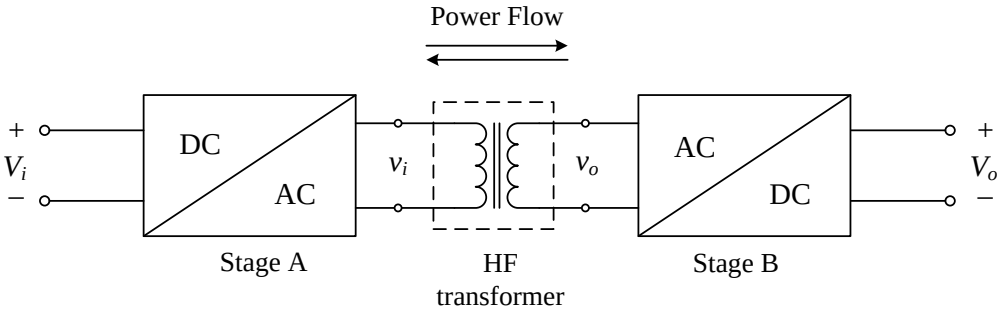


Fig. 3.1 Basic structure of bidirectional isolated DC-DC converter

Numerous topologies have been proposed for bidirectional isolated DC-DC converters. As discussed in Chapter 2, LRC converters are more suitable for high-current applications. An extensive literature study shows that these LRC topologies can be categorized into three basic families according to their major operating principles. They are:

- Flyback-derived.
- Half switch bridge-based.
- Full switch bridge-based.

The characteristic examples of each family will be introduced in subsequent sections, with emphasis on high-current applications. Since low switching loss is essential to achieve high efficiency and high power density, topologies equipped with soft switching capability are considered exclusively.

Objectives

The objectives of this chapter is to

- Find the appropriate topology candidate for high-current and low-voltage current applications, in terms of potential for low loss, high power density and a wide voltage operating range.
- Characterize the selected topology mathematically and prepare for the loss modeling introduced in Chapter 4.

The structure of this chapter is organized as follows: In Section 3.2, typical topologies in three major families are reviewed and compared. The most suitable topology for the high-current and low-voltage applications is selected. Different operating modes of this topology is introduced and quantitatively described in Section 3.3. Finally, conclusions are presented in the last section.

3.2 Topology Review and Evaluation

3.2.1 Flyback-Derived Converters

The conventional flyback converter belongs to the category of the duty-ratio-controlled isolated DC-DC topology. The advantages of a flyback converter are the easy start-up and its low cost due to its low component count. However, because of the hard switching pattern and high electrical stress on the switches [3-1], conventional flyback converters cannot normally reach a high level of efficiency and are only suitable for use in applications up to several hundred watts [3-2]. Much effort has been invested into increasing the efficiency of flyback converters. To reduce the switching loss, passive snubbers [3-3], active clamps [3-2][3-4] or auxiliary winding circuits [3-5][3-6] and dual-switch flyback [3-7] have been proposed.

Bidirectional flyback topologies achieving good efficiency have been reported in [3-8][3-9]. The typical circuit diagram is shown in Fig. 3.2. The active clamping branches (S_3+C_{c1} and S_4+C_{c1}) are paralleled with the flyback transformer windings on both sides. These branches prevent severe voltage oscillation between the leakage inductance of the transformer and the output capacitances of the power switches (S_1, S_2). The resultant clamped voltages $V_{s1.cl}$ and $V_{s2.cl}$ of power switches (S_1, S_2) in CCM can be defined as follows:

$$V_{S1.cl} = \frac{1}{1-D} \cdot V_i$$
$$V_{S2.cl} = \frac{1}{D_0} \cdot V_o \qquad (3\text{-}1)$$

where D is the duty ratio of S_1, S_2, and D_o is the duty ratio of S_3, S_4. Since the duty ratio is smaller than unity, the clamping voltages of S_1, S_2 are higher than the input voltage V_i and output voltage V_o, respectively. This means switches with higher voltage ratings than the terminal voltages have to be deployed, resulting in higher on-resistance.

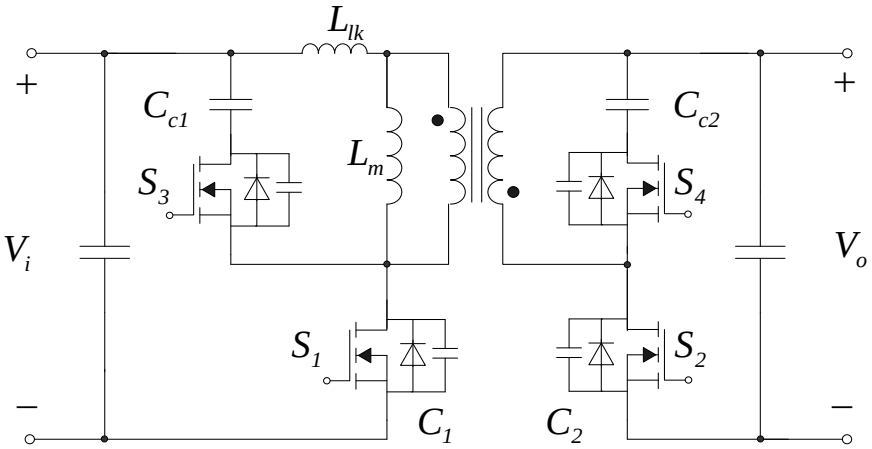


Fig. 3.2 Active clamping bidirectional flyback converter [3-8]

The switch modulation scheme is applied in such a way that 1) during the turn-off process the output capacitance (C_1, C_2) of the power switches is charged slowly and the switch voltage rises slowly to realize zero-voltage switching (ZVS); 2) S_1, S_2 can be turned on with zero-voltage and zero-current switching (ZVZCS) because the leakage energy freewheels through the body diodes of S_1, S_2 before they are turned on.

Because of the triangular current shape, the current stress of the power switch at the output stage remains high, despite soft-switching and limited switch voltage stress. The triangular current shape also implies the need for big capacitors to smooth input and output voltage ripples. Additionally, the unipolar flux swing in flyback transformers results in a magnetic core twice the size of converters with a bipolar flux swing [3-10], which increases the transformer size.

3.2.2 Half-bridge-based Converters

In half-bridge-based converters, switch bridges are located on both sides of a high-frequency transformer. The two bridges generate square voltage waveforms with a 50% duty ratio. The phase shift between two square voltage waveforms determines the power to be transferred. The transformer leakage inductance, loaded with the voltage difference of two square voltage waveforms, is utilized to transfer the power. Two main half-bridge-based DC-DC converters are introduced below, namely, dual half bridge with split capacitors and dual active bridge (DAB) – half bridge.

Dual Half Bridge with Split Capacitors (DHB-SC) [3-11]
In this topology (shown in Fig. 3.3), the input inductor associated with the input half bridge boosts the total voltage over C_1 and C_2 to $2V_i$, with V_i on C_1 and C_2, respectively. This results in a bipolar input voltage of transformer v_p between V_i and $–V_i$. The advantages and disadvantages of this topology are summarized below:

Advantages:

- Input current ripple is relatively small due to the usage of an input inductor that reduces the need for large input capacitance;
- Bipolar flux operation enables a more effective utilization of the magnetic core than the unipolar operation in flyback-based topology;
- The current through the switches and transformer windings is of quadrilateral shapes, which has a lower RMS value when transferring the same power compared with triangular and sinusoidal shapes (see Chapter 2).

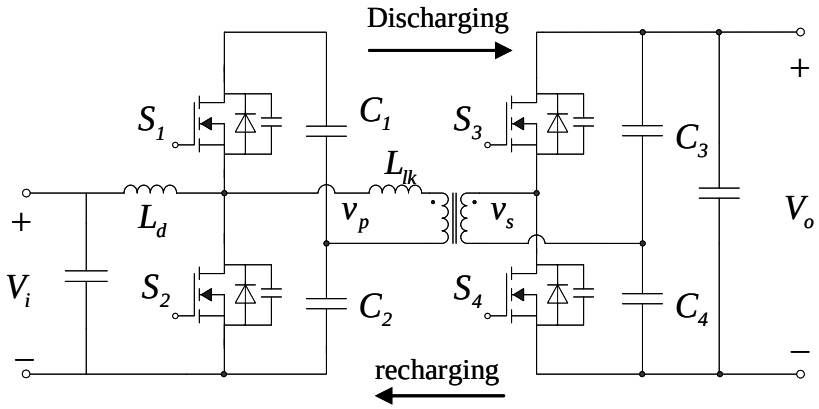


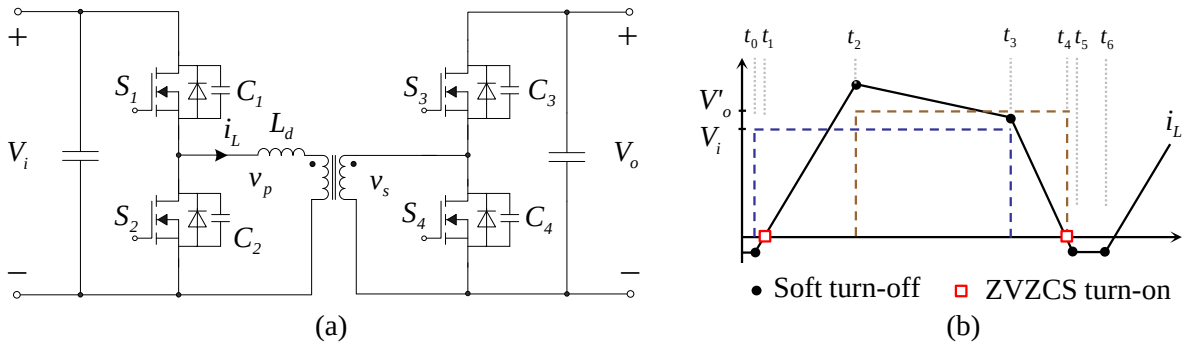
Fig. 3.3 Dual-half-bridge converter with split capacitors [3-11]

Disadvantages

- The voltage across S_1 and S_2 is equal to $2V_i$, which requires semiconductors with an increased voltage rating. This will result in an increased on-resistance of semiconductors and hence higher conduction loss;
- The split capacitors (C_1-C_4) have to handle the full load current. Bulky electrolytic capacitors that can be thermally loaded with high current should be used as C_1-C_4. This will undoubtedly deteriorate the power density of the high-current converter due to the large capacitor volume;
- The loss distribution in S_1 and S_2 is not even due to their different current peaks.

Dual Active Bridge - Half Bridges (DAB-HB) [3-12]

A DAB converter has two actively-switched bridges on both sides of a high frequency transformer (Fig. 3.4(a)). A DAB converter has two forms, namely, DAB with half bridges (DAB-HB) and DAB with full bridges (DAB-FB).



(a) (b)

Fig. 3.4 (a) Dual active bridge converters with half bridges (DAB-HB); (b) Waveforms of a DAB-HB converter ($V_i < V_o'$)

The operation of a DAB-HB converter is described as follows: When the input discharges its energy to the load, the switches S_1, S_4 are first turned on to store energy in the inductor L_d (t_1-t_2 in Fig. 3.4b). Then, S_4 is off and while S_3 is on to transfer the energy directly to the load (t_2-t_3), after that all switches are off and the freewheeling diodes of S_2, S_3 dump the energy left in L_d to the load (t_3-t_4). When the inductor current reaches zero, the switches S_2, S_3 and the freewheeling diodes of S_1, S_4 are turned on to create a negative current flow (during t_0-t_1 *and* t_4-t_6 in one switching cycle as illustrated in Fig. 3.4b) in the transformer winding, which is necessary to accumulate enough energy in L_d to charge and discharge the output capacitance of the switches. This negative current is also used to achieve ZVZCS by freewheeling the body-diodes of switches before the switches are turned on.

Advantages:

- Lower component count to accomplish the filtering, inverting, isolation and rectifying function, compared with DHB-SC.
- The voltage stresses over the switches equal the input or output voltages. Therefore, the on-resistance of MOSFET switches can be selected to be the minimal than otherwise.
- The quadrilateral current waveform (shown in Fig. 3.4b) reduces the current RMS value in switches and transformer windings.
- Immunity to parasitic inductance.
- Wide operating voltage range.

Disadvantages

- Difficult sensing and a complex controller needed to strictly regulate the magnitude and period of the negative current in transformer windings.
- Unipolar flux swing on transformer results in a magnetic core twice the size of those in topologies with bipolar flux swing.
- Large input/output capacitors to lower the terminal voltage ripples.

3.2.3 Full-bridge-based Converters

In full-bridge-based converters, similar to half-bridge-based topologies, square voltage waveforms generated by two full bridges are fed to the input and output of the transformer and the phase shift determines the power transfer. The main difference is that full bridges generate not only two-level but also three-level square voltage waveforms. This modulation flexibility facilitates the soft-switching pattern and simplifies the sensing and control circuit [3-13]. A full-bridge-based topology is considered below.

Dual Active Bridge – Full Bridge (DAB-FB)

DAB-FB (shown in Fig. 3.5) was proposed in the 1980s [3-14]. The leakage inductance of the transformer L_{lk} or an external inductor in series with the transformer is used to transfer power,

and the phase shift between two square-wave voltage sources (two full bridges) determines the power. Details of DAB-FB converter operation is described in Section 3.3. The DAB-FB converter [3-14] has many prominent advantages, but also some drawbacks.

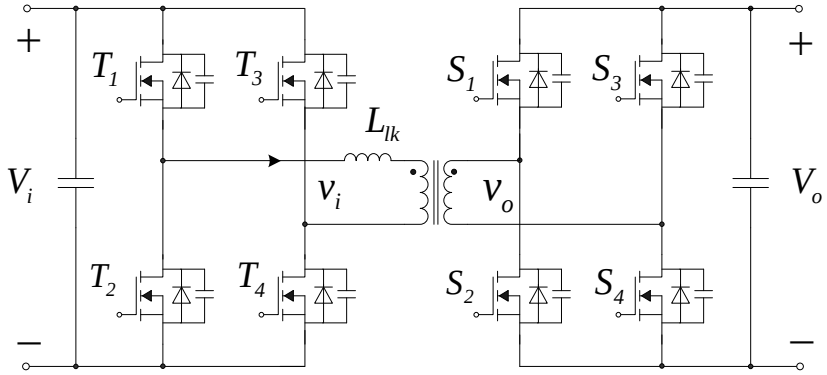


Fig. 3.5 Circuit diagram of dual active bridge – full bridge [3-14]

Advantages:

- Soft-switching capability without any auxiliary circuit.
- Low component count compared with other active full-bridge converters.
- Immunity to parasitic inductance in the transformer and circuit.
- Bipolar flux swing resulting in a smaller transformer.

Disadvantages

- Soft switching is lost at light load for simple phase-shift modulation method [3-15].
- With the simple phase-shift modulation method [3-16], system conduction loss is high due to the reactive power when the input voltage deviates far away from the output voltage referred to the input side.
- Large input/output capacitors are required to lower the terminal voltage ripples.

As controller design advances, more sophisticated current modulation methods have been proposed to improve the soft-switching range [3-16] and to reduce the circulating reactive power [3-17][3-18]. Details of three typical modulation methods are described in Section 3.3. Compared with DAB-HB, DAB-FB has doubled switch count. However, if the average current in the switches are the same, DAB-FB can transfer roughly doubled power to the output. Additionally, DAB-FB does not require such a complex sensing circuit to control the current for soft-switching. Therefore, a DAB-FB configuration is more suitable to deliver higher power than DAB-HB.

3.2.4 Summary

The advantages and disadvantages of three bidirectional isolated LRC topologies are compared in TABLE 3.1. Considering the high-current applications with high power density requirements, a full bridge DAB topology is selected as the converter carrier.

TABLE 3.1 ADVANTAGES AND DISADVANTAGES OF THE TYPICAL TOPOLOGIES IN THREE LRC TOPOLOGY FAMILIES

LRC Topology Family	Advantages	Disadvantages
Flyback-derived	▪ Lower voltage stress than normal flyback	▪ High current stress ▪ Extra components for soft-switching ▪ Larger transformer size due to unipolar flux swing
Half-bridge based (DHB-SC)	▪ Low input current ripple ▪ Quadrilateral current shape ▪ Bipolar flux swing resulting in a small transformer	▪ High voltage stress on semiconductors ▪ Capacitors carrying power current ▪ Input inductor required
Half-bridge based (DAB-Half Bridge)	▪ Low component count ▪ Quadrilateral current shape ▪ Immunity to parasitic inductance ▪ Low voltage stress on semiconductors	▪ Complex current sensing ▪ Larger transformer size due to unipolar flux swing ▪ Large input/output capacitors needed for lower voltage ripple
Full-bridge based (DAB-Full Bridge)	▪ Quadrilateral current shape ▪ Immunity to parasitic inductance ▪ Wide operating voltage range ▪ Bipolar flux swing resulting in a small transformer size ▪ Low voltage stress on semiconductors ▪ More modulation possibility;	▪ Complex controllers ▪ Large input/output capacitors needed for lower voltage ripple

3.3 Three Typical Modulations of Full-Bridge DAB

The circuit diagram of DAB-FB (*hereinafter* DAB) converter is shown again in Fig. 3.6(a). Each switch (S_x in input bridge or T_x in output bridge) is connected in anti-parallel with a diode (D_{Tx} or D_{Sx}) and a snubber capacitor (C_{Tx} or C_{Sx}). The leakage inductance of the high-frequency transformer (T_s) is referred to the primary side and denoted as L_{lk}. Here, the two switch bridges behave as two square-wave voltage sources (v_i and v_o). The voltage sources are shifted in phase δ to deliver power. When power flows from an input bridge to an output bridge, it is called discharging mode while the charging mode refers to the power flowing in the opposite direction. Through the switch modulations, two voltage sources are able to generate three voltage levels - positive and negative terminal voltages (V_i and V_o) and zero. Assuming the magnetizing inductance of transformer T_s is much larger than its leakage inductance, the DAB circuit diagram can be simplified into Fig. 3.6(b), where v_o' is the output voltage referred to the input side of transformer.

Three typical modulation methods are available [3-16]. Each method differs in power transfer capability, voltage operating range, soft-switching range and also system efficiency. This section will describe these modulation methods, namely rectangular, trapezoidal and triangular modulations, according to their transformer current shapes.

3.3.1 Rectangular (Phase-shift) Modulation

Rectangular modulation, also called phase-shift modulation, was first proposed for DAB converters [3-14]. Two voltage sources generate square waveforms with positive and negative terminal voltages (i.e. V_i and V_o). The power is transferred from the leading bridge to the lagging bridge. The power that can be delivered, P_o, is calculated as:

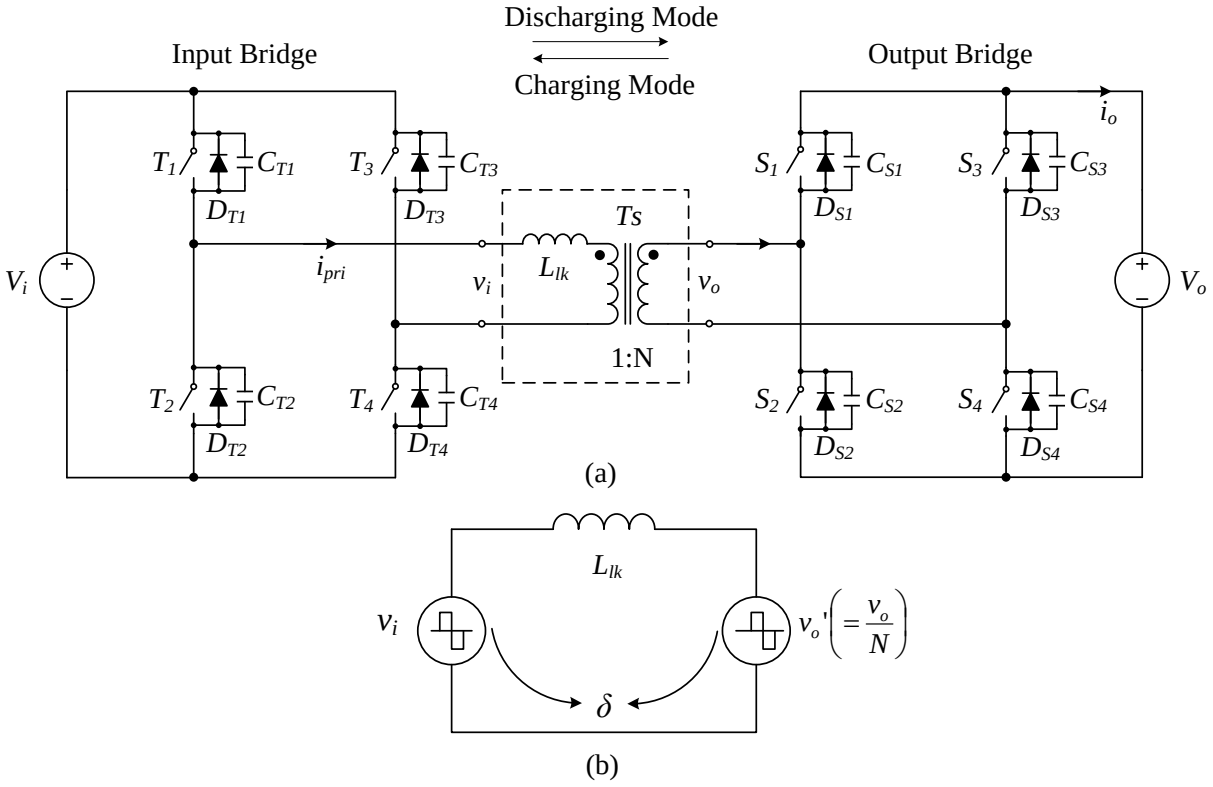


Fig. 3.6 Circuit diagram (a) and equivalent circuit (b) of DAB-FB

$$P_o = \frac{V_i^2}{2\pi f_{sw} L_{lk}} d\delta\left(1-\frac{|\delta|}{\pi}\right) \tag{3-2}$$

where δ is the phase shift in radians, f_{sw} is the switching frequency of the switch, and d is the ratio between the input voltage V_i and the referred output voltage to the input side (V_o'):

$$d = \frac{V_o'}{V_i} \tag{3-3}$$

$$V_o' = \frac{V_o}{N} \tag{3-4}$$

assuming the transformer turn ratio is 1: N. Eq. (3-2) is valid when $-\pi/2 \le \delta \le \pi/2$. It can be determined that the power transfer is zero when $\delta = 0$ and maximal when $\delta = \pi/2$. The maximum power is expressed as follows:

$$P_{max} = \frac{V_i^2 d}{8 f_{sw} L_{lk}} \tag{3-5}$$

if the base voltage V_b and base power P_b are

$$V_b = V_i \tag{3-6}$$

$$P_b = \frac{V_i^2}{2\pi f_{sw} L_{lk}} \tag{3-7}$$

The maximal power in the Per-Unit (PU) system is expressed as follows:

$$P_{rec\_max\_pu} = \frac{\pi d}{4} \tag{3-8}$$

The typical transformer voltage (v_i and v_o') and current (i_{pri}) waveforms are shown in Fig. 3.7(a) and (b) to illustrate the working principle of the rectangular modulation, where Fig. 3.7(c) indicates the conducting devices in different switching intervals.

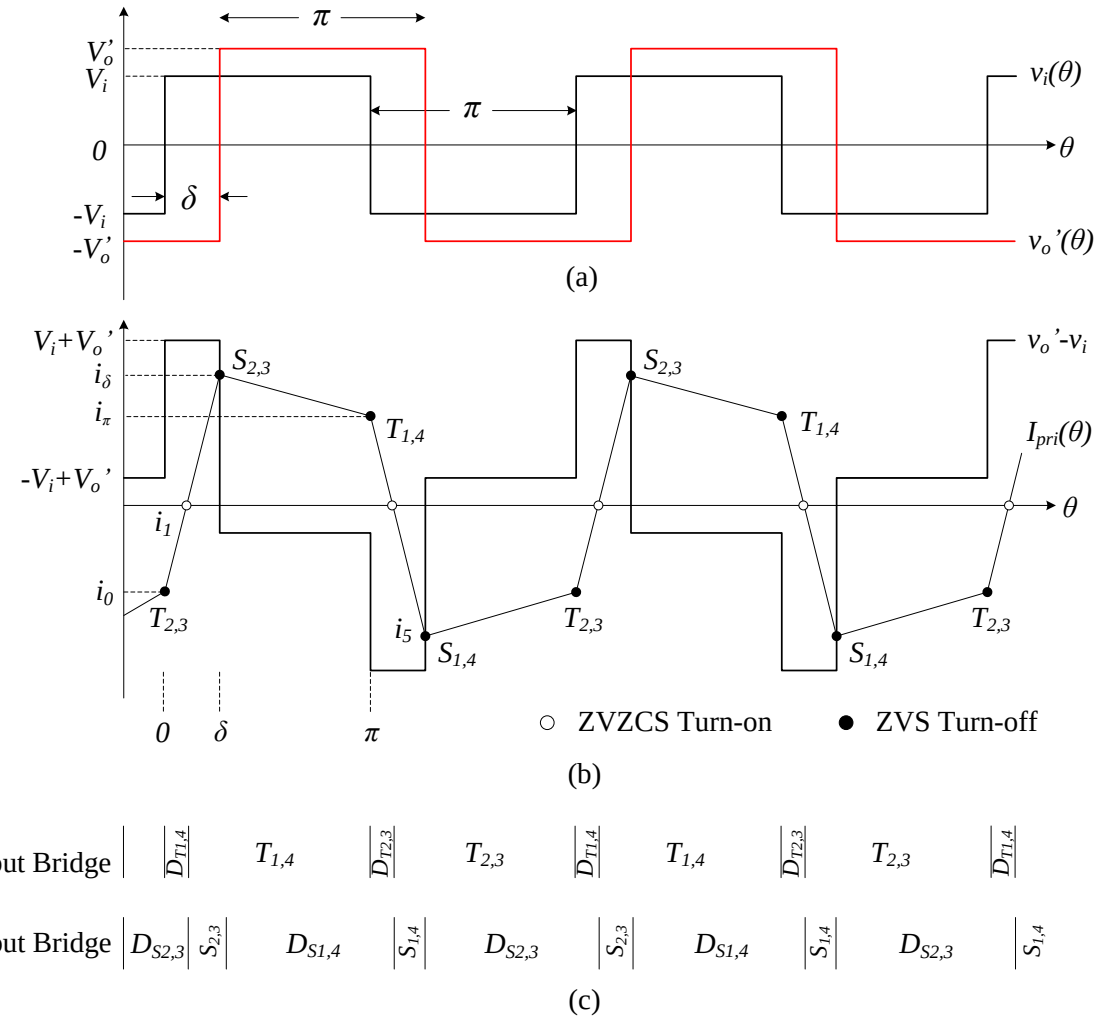


Fig. 3.7 Rectangular modulation - soft-switching mode (a) Transformer input v_i and output voltage v_o' (b) voltage across the transformer leakage inductance and transformer primary current; (c) conducting devices in different switching intervals

It can be determined from Fig. 3.7(b) and (c) that the turn-on of eight switches is initiated while their anti-parallel diodes are conducting. This ensures that the switch naturally takes over as the diode current reverses with ZVZCS. The turn-off of the eight switches is also implemented as a ZVS process, due to the snubber capacitors (C_{Tx} and C_{Sx}), as explained in Sec-

tion 2.3.1. In Fig. 3.7(b), ZVZCS turn-on and ZVS turn-off events are labeled with white dots and black dots, respectively. The transformer current in the primary winding when $\theta = 0$, δ and π can be defined as follows:

$$\begin{aligned} i_{pri}(0) &= \frac{-V_i}{2\pi f_{sw} L_{lk}} \left[d\delta + \frac{\pi(1-d)}{2} \right] \\ i_{pri}(\delta) &= \frac{-V_i}{2\pi f_{sw} L_{lk}} \left[-\delta + \frac{\pi(1-d)}{2} \right] \\ i_{pri}(\pi) &= -i_{pri}(0) \end{aligned} \tag{3-9}$$

Note that when $V_i = V_o/N$, $i_{pri}(\delta) = i_{pri}(\pi)$, it means the current in the transformer has a rectangular shape. According to the Section 2.3.1, this current shape has a lower RMS value than triangular and sinusoidal shapes, and hence a minimal conduction loss. However, the current during intervals 0 and δ is actually circulating between the transformer and switches and not transferred to the load, which decreases the transformer utilization and system efficiency.

Assuming that the converter is lossless, the phase shift can be calculated as:

$$\delta = \frac{\pi}{2} \cdot \frac{V_i - \sqrt{V_i^2 - 8V_i L_{lk} f_{sw} \left| P_o / V_o' \right|}}{V_i} \tag{3-10}$$

where I_o is the output current. The sign of the phase shift is positive in discharging mode and negative in charging mode.

To guarantee the soft-switching condition for both input and output switch bridges, the following conditions should be fulfilled:

$$i_{pri}(\delta) > 0 \quad \& \quad i_{pri}(\delta) > 0 \tag{3-11}$$

which can be translated into the relationship between d and phase shift δ [3-15] as shown here:

$$1 - \frac{2\delta}{\pi} \le d \le \frac{1}{1 - \frac{2\delta}{\pi}} \qquad (0 \le \delta \le \pi) \tag{3-12}$$

When this condition is violated, the soft-switching pattern will be lost, which will cause a great drop in efficiency. The transformer current and voltage waveforms and conducting devices in the hard-switching range are illustrated in Fig. 3.8. Here, the turn-off of switches in the input bridge and turn-on of switches in the output bridge occur with a hard-switching pattern, and all diodes are switched off at high current resulting in reverse recovery losses.

The soft-switching range confined by input and output bridge soft-switching boundaries given in Eq. (3-12) is illustrated in Fig. 3.9. Here, the PU power is related to the phase shift at different ratio d between the input and output voltage ratio. Within the soft-switching range, the power curves are denoted with solid lines. It can be observed that when the input and output

voltage ratio *d* is one, it has soft-switching capability over the whole phase-shift and power range. However, the further *d* deviates from unity, the narrower the soft-switching range becomes.

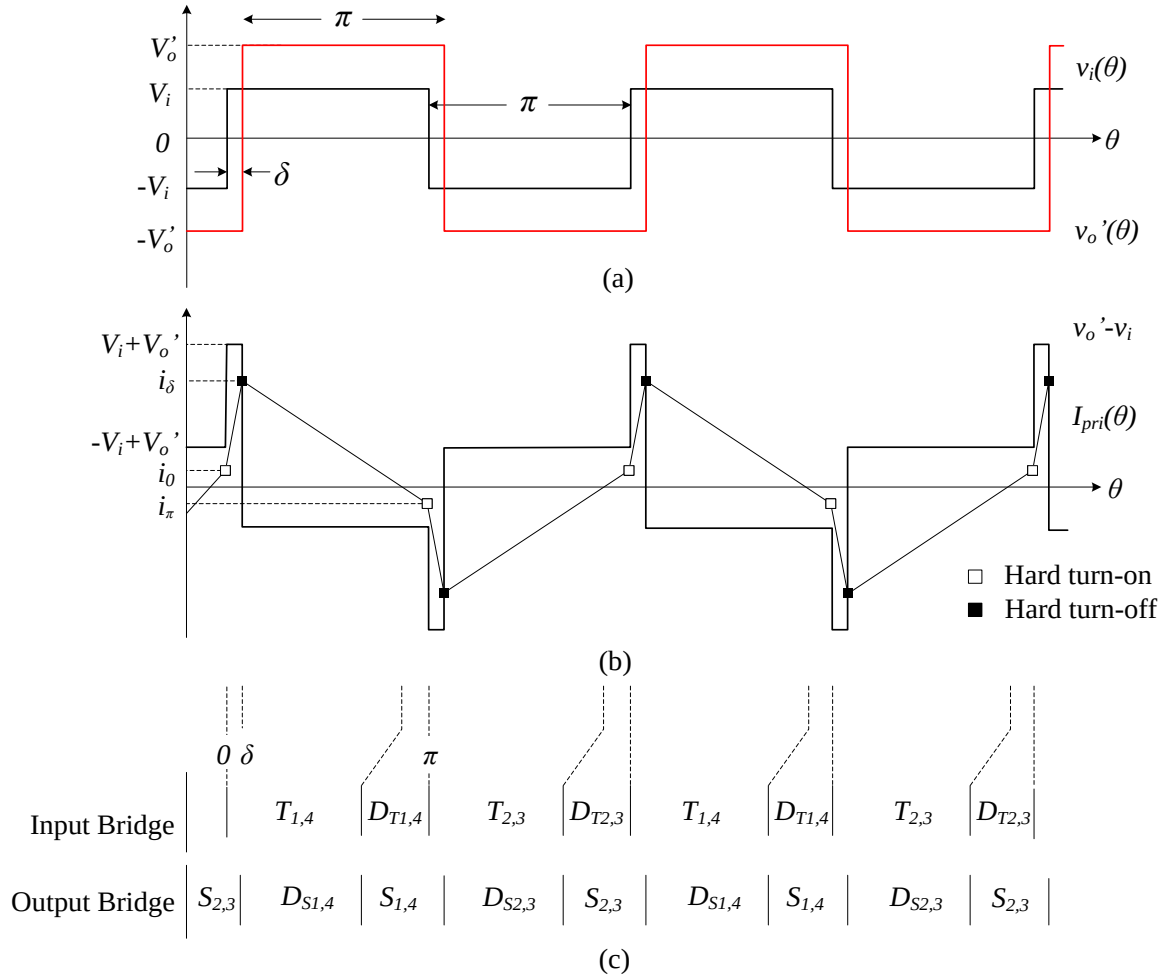


Fig. 3.8 Rectangular modulation - hard-switching mode (a) Transformer input v_i and output voltage v_o' (b) voltage across the transformer leakage inductance and transformer primary current; (c) conducting devices in different switching intervals

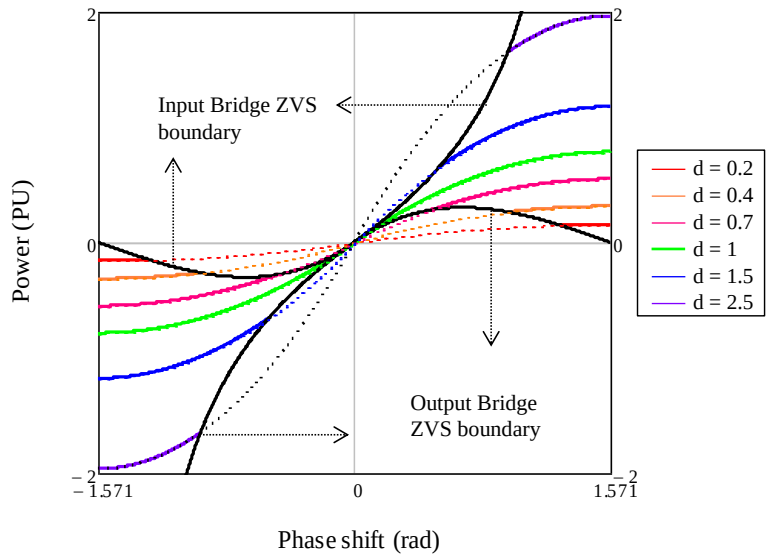


Fig. 3.9 Soft-switching range in PU power system in relation to phase shift and input/output voltage ratio *d*

3.3.2 Trapezoidal Modulation

This modulation method introduces a zero voltage level in two square voltage sources generated by active bridges. This zero level has a length of 4 times Ω_1 and Ω_2 in each cycle, respectively, as shown in Fig. 3.10(a). It makes the transformer current start from and stop at zero in each half of the switching period. The current in the primary winding of the transformer i_{pri} and the voltage across the transformer leakage inductance L_{lk} are shown in Fig. 3.10(b), where ZVZCS turn-on and ZVS turn-off events are labeled with white dots and black dots, respectively. The conducting active devices in two switch bridges in each interval are pointed out in Fig. 3.10(c). The major features of this modulation are that:

- The power circulating between transformer and switches in rectangular modulation are greatly reduced, and the transformer utilization rises.

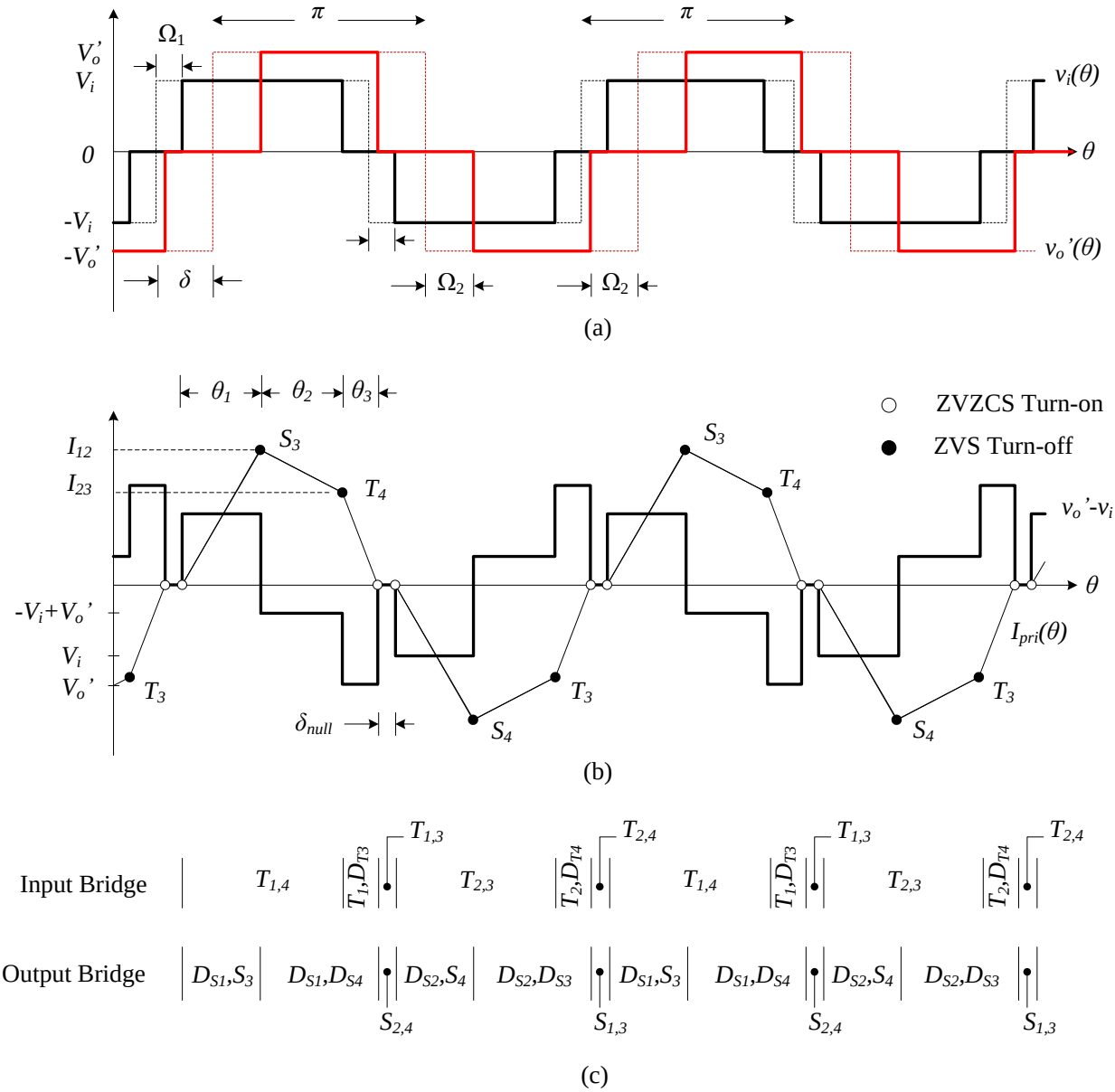


Fig. 3.10 Trapezoidal modulation (a) Transformer input v_i and output voltage v_o' (b) voltage across the transformer leakage inductance and transformer primary current; (c) conducting devices in different switching intervals

- The zero voltage level applied to two voltage sources enables all switches to be turned on with ZVZCS, half of the switches are turned off with ZVS while the other half are turned off with ZVZCS, which means the switching loss is smaller than that of the rectangular modulation.

Mathematical description

- $V_i \le V_o'$

To construct the trapezoidal transformer current waveform, the following relation between Ω_1, Ω_2, δ and given null time δ_{null} in which the voltage across the transformer leakage inductance equal zero should be fulfilled:

$$\begin{aligned}\Omega_1 &= \frac{(1-d)\pi + 2d(\delta + \delta_{null})}{2(d+1)} \\ \Omega_2 &= \delta - \Omega_1 + \delta_{null}\end{aligned} \tag{3-13}$$

Two current-turning points I_{12} and I_{23} in each half-cycle are determined by:

$$\begin{aligned}I_{12} &= \frac{V_i(\delta - \Omega_1 + \Omega_2)}{2\pi L_{lk} f_{sw}} \\ I_{23} &= \frac{V_o'(\delta - \Omega_2 + \Omega_1)}{2\pi L_{lk} f_{sw}}\end{aligned} \tag{3-14}$$

The output power P_o can then be calculated as below:

$$\begin{aligned}P_o &= v_o' i_{pri} = \frac{V_i^2}{2\pi f_{sw} L_{lk}} \frac{\left(d^2\theta_2\theta_3 + d\theta_1\theta_3 + d^2\theta_3^2\right)}{2\pi} \\ &= \frac{V_i^2}{2\pi f_{sw} L_{lk}} \cdot \frac{d^2}{2\pi(d^2+1)} \cdot \left\{ -\left[N(A - 2\delta) - \frac{A}{N} \right]^2 + A^2 \left(\frac{N^2+1}{N^2} \right) \right\}\end{aligned} \tag{3-15}$$

where

$$\begin{aligned}\theta_1 &= \delta + \Omega_2 - \Omega_1 = \frac{Ad - \theta_2}{d+1} \\ \theta_2 &= \pi - \delta - \Omega_2 - \Omega_1 = A - 2\delta \\ \theta_3 &= \delta - \Omega_2 + \Omega_1 = \frac{A - \theta_2 d}{d+1} \\ \delta_{null} &= 2\Omega_1 - \theta_3 = -\delta + \Omega_1 + \Omega_2 \\ A &= \pi - \delta_{null} \\ N &= \sqrt{d + \frac{1}{d} + 1}\end{aligned} \tag{3-16}$$

It can be found from Eq. (3-15) that if one of the input or output voltages approach zero, the power transferred is close to zero as well.

From the equations above, the phase shift δ in trapezoidal modulation can be calculated as follows:

$$\delta = \pi \left[\frac{M_1\left(1-2t_{null}\, f_{sw}\right)}{2M_2} - \frac{\left(V_i + V_o'\right)\sqrt{M_3\left(4 f_{sw}^2 t_{null}{}^2 + 1\right) - 4 f_{sw}\left[\left|\left(P_o / V_o'\right)\right| L_{lk} M_2 + t_{null} M_3\right]}}{2\sqrt{V_i} M_2} \right] \tag{3-17}$$

where

$$\begin{aligned} M_1 &= V_i^2 + V_o'^2 \\ M_2 &= V_i^2 + V_i V_o' + V_o'^2 \\ M_3 &= V_i^2 V_o' \\ t_{null} &= \frac{\delta_{null}}{2\pi f_{sw}} \end{aligned} \tag{3-18}$$

The sign of this phase shift is positive in discharging mode and negative in charging mode. To guarantee the current trapezoidal shape, the transferred power has upper and lower limits. At the lower limit, the phase-shift δ is such that I_{23} equals zero. So, the minimal phase-shift can be calculated using the following expression:

$$\delta_{min} = \frac{\left(\pi - \delta_{null}\right)}{2}\left(1 - \frac{V_i}{V_o'}\right) = \frac{\left(\pi - \delta_{null}\right)}{2}\left(1 - \frac{1}{d}\right) \tag{3-19}$$

Then the minimal transferred power is:

$$P_{trap\_min} = \frac{V_i^2}{4\pi^2 L_{lk} f_{sw}}\left(\pi - \delta_{null}\right)^2\left(1 - \frac{V_i}{V_o'}\right) = \frac{V_i^2}{2\pi L_{lk} f_{sw}}\frac{\left(\pi - \delta_{null}\right)^2}{2\pi}\left(1 - \frac{1}{d}\right) \tag{3-20}$$

It can be seen that a large null time δ_{null} decreases the power transfer capability. The maximal phase-shift can be obtained by differentiating Eq. (3-15) and making it zero, in which case the maximal phase-shift can be expressed as:

$$\delta_{max} = \frac{\pi - \delta_{null}}{2}\left(\frac{\frac{V_i^2}{V_o'^2} + 1}{\frac{V_i^2}{V_o'^2} + \frac{V_i}{V_o'} + 1}\right) = \frac{\pi - \delta_{null}}{2}\frac{d^2 + 1}{d^2 + d + 1} \tag{3-21}$$

The maximal transferred powers by trapezoidal modulation method are defined as

$$P_{trap\_max} = \frac{V_i^2}{4\pi^2 L_{lk} f_{sw}}\left(\pi - \delta_{null}\right)^2 \frac{1}{\frac{V_i^2}{V_o'^2} + \frac{V_i}{V_o'} + 1} = \frac{V_i^2}{2\pi L_{lk} f_{sw}}\frac{\left(\pi - \delta_{null}\right)^2}{2\pi}\left(\frac{d^2}{d^2 + d + 1}\right) \tag{3-22}$$

The minimal and maximal power transfers in PU system are

$$P_{trap\_min\_pu} = \frac{\left(\pi - \delta_{null}\right)^2}{2\pi}\left(1 - \frac{1}{d}\right) \tag{3-23}$$

$$P_{trap\_max\_pu} = \frac{\left(\pi - \delta_{null}\right)^2}{2\pi}\left(\frac{d^2}{d^2 + d + 1}\right) \tag{3-24}$$

- $V_i > V_o'$

In this case, the terminal voltages (V_i and V_o') can be considered to swap in the case of $V_i \leq V_o'$. The trapezoidal current waveform is then constructed by:

$$\Omega_1 = \delta - \Omega_2 + \delta_{null}$$

$$\Omega_2 = \frac{\pi\left(d-1\right) + 2\left(\delta + \delta_{null}\right)}{2\left(d+1\right)} \tag{3-25}$$

The expression of maximal output power P_o and maximal phase shift are the same to case $V_i \leq V_o'$, while the minimal power transfer becomes:

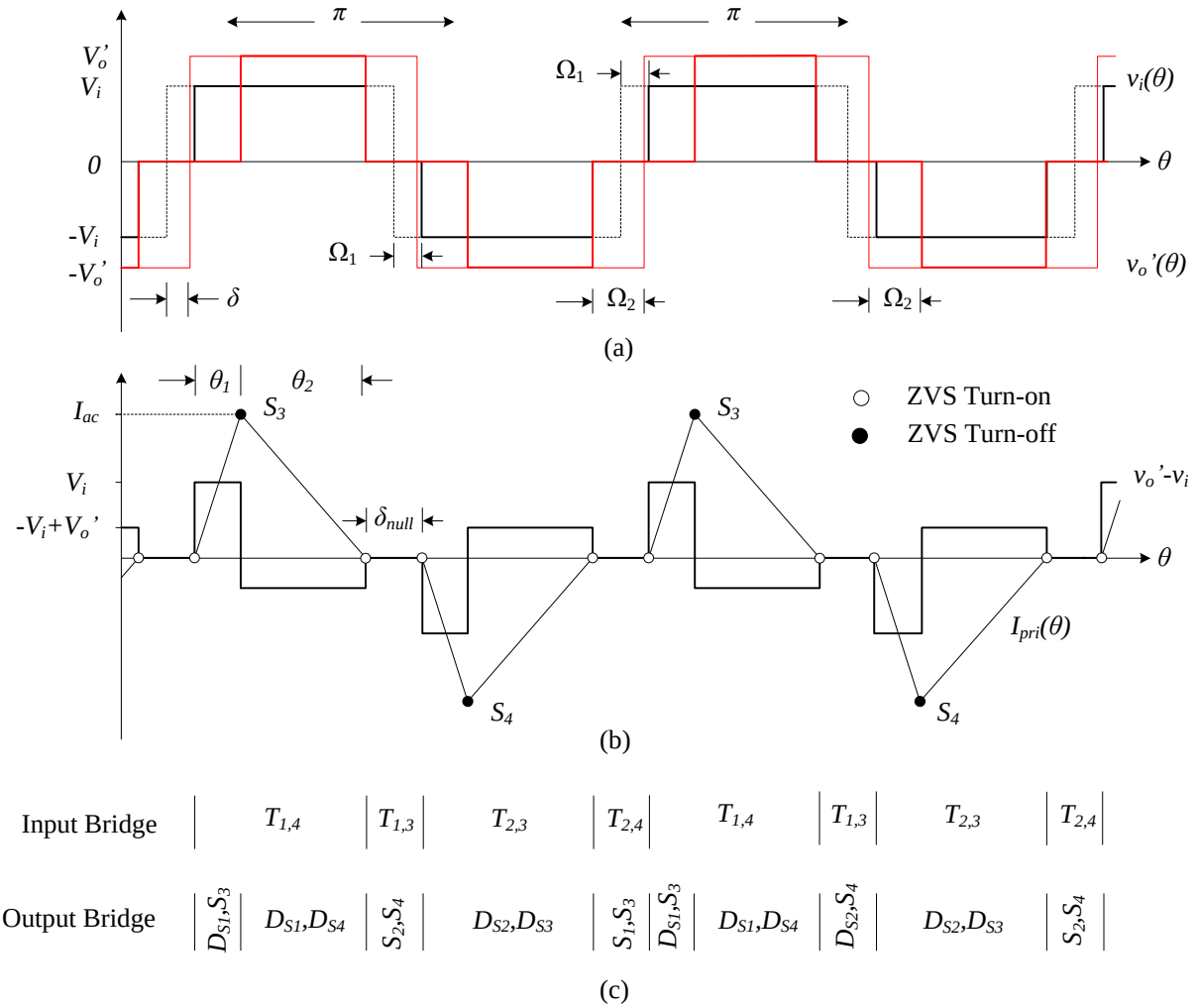


Fig. 3.11 Triangular modulation (a) Transformer input v_i and output voltage v_o' (b) voltage across the transformer leakage inductance and transformer primary current; (c) conducting devices in different switching intervals

$$P_{trap\_min} = \frac{V_i^2}{4\pi^2 L_{lk} f_{sw}} \left(\pi - \delta_{null}\right)^2 \left(1 - \frac{V_o'}{V_i}\right) = \frac{V_i^2}{2\pi L_{lk} f_{sw}} \frac{\left(\pi - \delta_{null}\right)^2}{2\pi} \left(1-d\right) d^2 \quad (3\text{-}26)$$

at

$$\delta_{min} = \frac{\left(\pi - \delta_{null}\right)}{2} \left(1 - \frac{V_o'}{V_i}\right) = \frac{\left(\pi - \delta_{null}\right)}{2} \left(1-d\right) \quad (3\text{-}27)$$

3.3.3 Triangular Modulation

The triangular modulation can be seen as a special case of the trapezoidal method. If I_{23} in trapezoidal modulation is maintained at zero, the transformer current shape becomes triangular. Typical transformer input and output voltage and current waveforms are shown in Fig. 3.11(a) and (b), respectively. The main benefit of this modulation is that all switches are turned on with ZVZCS, while only two switches at the output switch bridge (in the discharging mode) are turned off with ZVS and other switches with ZVZCS. However, to transfer the same power to the load, triangular current shape in general will bear more conduction losses in the transformer and semiconductors than a trapezoidal shape, as explained in section 2.3.1.

Mathematical description

- $V_i \leq V_o'$

The two conducting intervals of the transformers can be described by phase shift as follows:

$$\theta_1 = 2\delta$$
$$\theta_2 = \frac{2\delta}{d-1} \quad (3\text{-}28)$$

The output power of triangular modulation can be calculated as

$$P_{tri} = V_o' i_{pri} = \frac{V_i^2}{2\pi f_{sw} L_{lk}} \cdot \frac{2d\delta^2}{\pi\left(d-1\right)} \quad (3\text{-}29)$$

Eq. (3-29) shows that when the input voltage is equal to the output voltage, or one of them is zero, the triangular modulation cannot transfer any power.

In a PU system, the output power of triangular modulation is

$$P_{tri\_pu} = \frac{2d\delta^2}{\pi\left(d-1\right)} \quad (3\text{-}30)$$

The phase shift can be derived from Eq. (3-29):

$$\delta = \frac{\pi}{V_i} \sqrt{\frac{L_{lk} f_{sw} P_{tri} \left(d-1\right)}{d}} \quad (3\text{-}31)$$

It can be concluded that the output power increases with the phase shift. Therefore, the minimal power transfer is zero at zero phase shift. The maximal power transfer occurs when the interval Ω_1 reaches the half of given null time limit δ_{null}.

$$\delta_{tri\_max} \xrightarrow{2\Omega_1=\delta_{null}} \frac{(\pi-\delta_{null})}{2}\left(1-\frac{1}{d}\right) \tag{3-32}$$

$$P_{tri\_max}\Big|_{\delta_{max}} = \frac{V_i^2}{2\pi f_{sw} L_{lk}} \frac{(\pi-\delta_{null})^2}{2\pi}\left(1-\frac{1}{d}\right) \tag{3-33}$$

In a PU system, the maximal power is:

$$P_{tri\_max\_pu}\Big|_{\delta_{max}} = \frac{(\pi-\delta_{null})^2}{2\pi}\left(1-\frac{1}{d}\right) \tag{3-34}$$

The peak current I_{ac} is defined as

$$I_{ac} = 2\delta \cdot \frac{V_i}{L_{lk}} = \frac{2\pi}{L_{lk}}\sqrt{\frac{L_{lk} f_{sw} P_{tri}(d-1)}{d}} \tag{3-35}$$

- $V_i > V_o'$

Again in this case, the terminal voltages (V_i and V_o') can be considered to swap in the case of $V_i \le V_o'$. The maximal power transfer is defined as

$$P_{tri\_max} = \frac{V_i^2}{2\pi f_{sw} L_{lk}} \frac{(\pi-\delta_{null})^2}{2\pi}(1-d)d^2 \tag{3-36}$$

$$\delta_{tri\_max} \xrightarrow{2\Omega_1=\delta_{null}} \frac{(\pi-\delta_{null})}{2}(1-d) \tag{3-37}$$

3.3.4 Comparison of three DAB modulation methods

Power Range

From the mathematical descriptions above, the minimal and maximal PU power capability of rectangular, trapezoidal and triangular modulations are summarized in the TABLE 3.2. Fig. 3.12 illustrates the power capability range of three modulations in PU system as a function of *d*. It can be seen that the rectangular modulation transfers the most power, and the maximal power of the triangular method is equal to the minimum of the trapezoidal modulation.

Switching Loss

Not only the power ranges of the three modulations are different, but also the switching loss generated. In the three modulation methods, each switch is switched on and off once.

TABLE 3.3 summarizes the number of different switching patterns in one switching cycle. Here, rectangular modulation is assumed to operate in soft-switching range. ZVZCS turn-on and -off barely has any loss, but ZVS turn-off described in Section 2.3.1 has [3-19]. Therefore,

TABLE 3.2 MINIMAL AND MAXIMAL POWER OF THREE DAB MODULATIONS (PU SYSTEM)

Modulation Methods	Minimal Power (PU system)		Maximal Power (PU system)	
	$V_i > V_o'$	$V_i \le V_o'$	$V_i > V_o'$	$V_i \le V_o'$
Rectangular	0		$\frac{\pi d}{4}$	
Trapezoidal	$\frac{(\pi-\delta_{null})^2}{2\pi}(1-d)d^2$	$\frac{(\pi-\delta_{null})^2}{2\pi}\left(1-\frac{1}{d}\right)$	$\frac{(\pi-\delta_{null})^2}{2\pi}\left(\frac{d^2}{d^2+d+1}\right)$	
Triangular	0	0	$\frac{(\pi-\delta_{null})^2}{2\pi}(1-d)d^2$	$\frac{(\pi-\delta_{null})^2}{2\pi}\left(1-\frac{1}{d}\right)$

TABLE 3.3 NUMBER OF ZVZCS AND ZVS TURN-ON AND TURN-OFF IN THREE MODULATIONS

Modulation Methods	Turn-on		Turn-off	
	ZVZCS	ZVS	ZVZCS	ZVS
Rectangular	8	0	0	8
Trapezoidal	8	0	4	4
Triangular	8	0	6	2

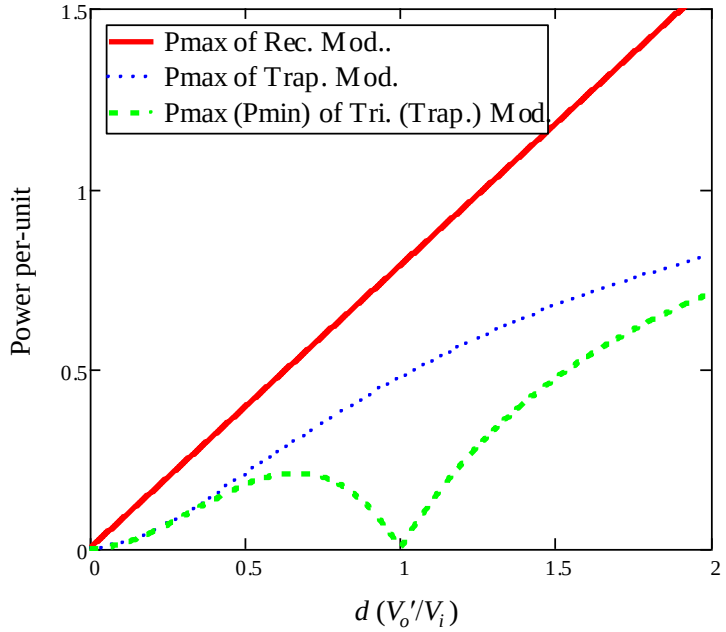


Fig. 3.12 Power capability range of rectangular, trapezoidal and triangular modulations in DAB (PU system)

the varied number of ZVS turn-offs differentiates the switching losses of three modulation methods. The rectangular modulation has more ZVS turn-offs than the other two modulations, and generates even more switching losses if operating in hard-switching range.

Conduction Loss

Fig. 3.13 illustrates the current, input and output voltages of the transformer for the three modulations. The shallow area E_o below the current waveform indicates the actual energy transferred to the output, which is calculated as follows:

$$P_o = \frac{\int_{\theta_0}^{\theta_\pi} v_o' \cdot d\theta \cdot \int_{\theta_0}^{\theta_\pi} i_{pri} \cdot d\theta}{\pi^2} \tag{3-38}$$

It follows that to deliver the same power, rectangular modulation requires some circulating current (in other words, reactive power) during time $\theta_1 \sim \theta_\pi$, while the other two modulations do not. This implies that more conduction loss will occur in the transformer and switches under the rectangular modulation.

In summary, each modulation method outperforms the other two, in terms of power transfer capability, efficiency and operating voltage range, within a different power range. The identification of these operating boundaries between different modulations helps to optimize the DAB system's efficiency over the entire operating range. This can be done using an accurate loss model, which will be introduced in Chapter 4.

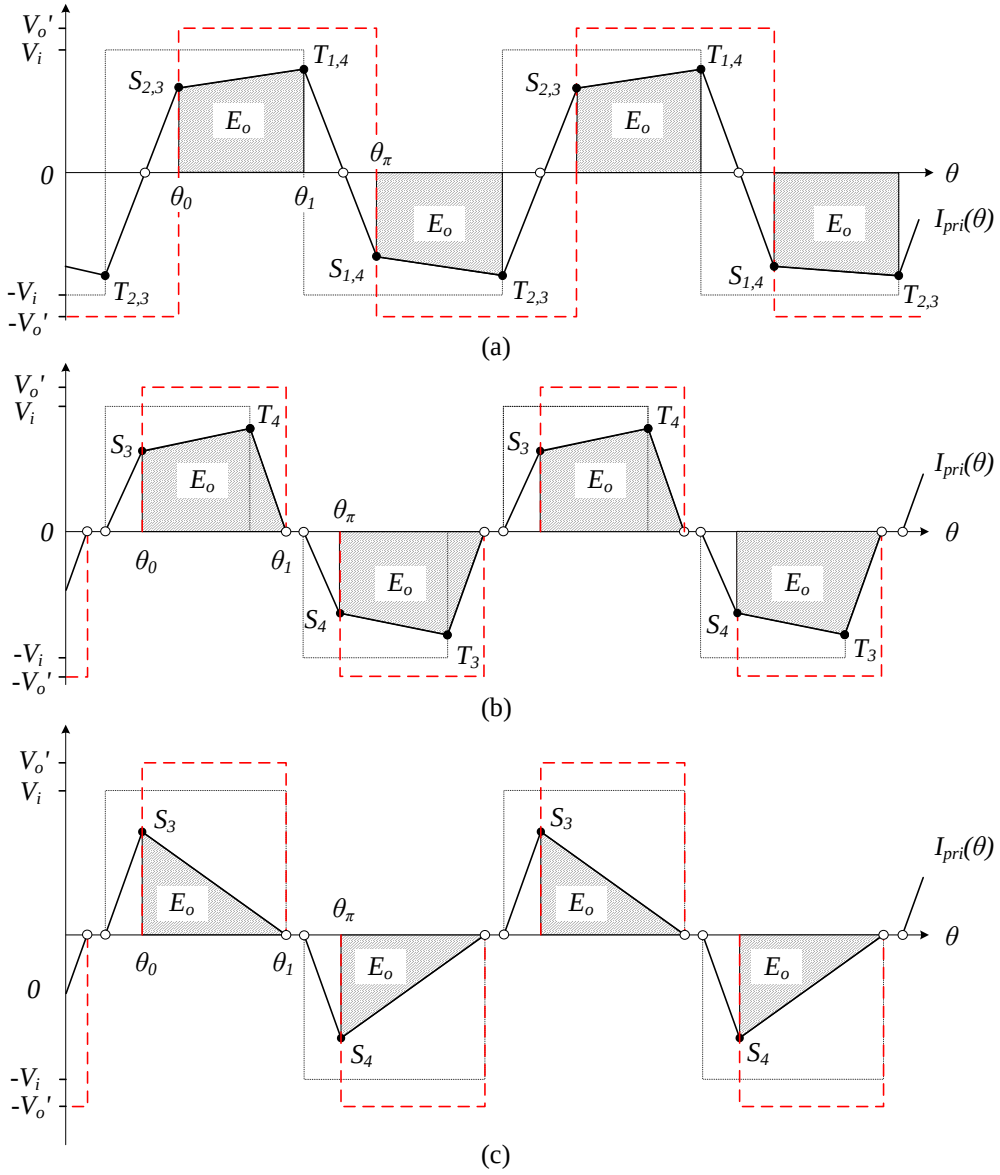


Fig. 3.13 The transformer input voltage (dotted curve), referred output voltage (dashed curve) and current (solid curve) of rectangular (a), trapezoidal (b) and triangular (c) modulations, with shadow area below current indicating the amount of energy transferred to output

3.4 Conclusions

After a comprehensive comparison of typical topologies in three LRC families, the full-bridge DAB topology is found to be the best carrier for high-current bidirectional isolated DC-DC converters, due to its simple circuit structure, low component count, immunity to parasitic inductance, soft-switching ability, and the wide operating range enabled by multiple modulation methods.

Three major modulation methods of DAB-FB topologies, namely, the rectangular, trapezoidal and triangular modulations, are described and compared, including a mathematical description for each modulation method. It has been determined that each of the modulations can outperform the other two, in terms of efficiency, in different power and voltage operating ranges. Identification of these boundaries among modulations can optimize the DAB system efficiency over the full operating range. This requires an accurate loss modeling approach, as a tool for heat generation management. An accurate loss modeling approach for high-current DAB converters will be proposed in Chapter 4.

3.5 References

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Chapter 4

Loss Modeling of High-Current Converters

4.1 Introduction

After the full-bridge DAB topology is selected for the given high-current applications, the details of the converter design should be further established and optimized, including its operating parameters, control parameters and component parameters, to meet the specifications and HPD requirement. To achieve this, a tool is required to calculate, analyze and optimize the losses on the component and system levels. Then, the loss information received as the output of this tool will be passed down to the subsequent heat removal design. This heat generation management tool further requires this loss model with the following Key Performance Indices (KPI):

- Accuracy
- Computational effort
- Multiple-variable analysis possibility
- Full operating range calculation capability

Many loss-modeling methods exist, including analytical calculations [4-1], circuit simulation [4-3] and Finite Element Analysis simulation [4-2], used to estimate component and system losses. A simulation software-based approach is accurate, but time-consuming, and it is difficult to verify the losses over a range of operating points. The analytical methods are powerful to understand and analyze the PE converters quickly, however, most of them perform the loss calculation based on ideal waveforms under the assumption of a lossless circuit, thereby compromising accuracy.

Objectives

This chapter will present an analytical loss modeling approach for high-current DAB converters, which realizes the aforementioned four KPIs. The accuracy of this approach is improved by involving critical non-ideal factors within high-current converters. An experimental verification approach for the developed DAB loss model is proposed and applied to a 12V~350V, 1 kW DAB prototype. This loss model is also utilized to design and optimize a 2 kW high-current DAB converter (discussed in Chapter 6).

The structure of this chapter is presented as follows. Section 0 describes the principle of this loss-modeling approach in depth. Section 4.3 and 4.4 elaborate the two steps of building such a loss model - waveform construction and loss calculation. The involvement of critical non-ideal factors is highlighted. Section 4.5 introduces the experimental verification of the proposed loss model for a 1 kW DAB converter.

4.2 Loss Modeling Approach

The proposed loss modeling approach is aimed at high-current converter design. The following are its main characteristics:

- *Analytical modeling*: This method decreases required calculation time and is able to gain more insights into the designed converter, compared with the circuit simulation software-based methods.
- *Crucial losses are involved* to increase the model's accuracy.
- *Valid in full operating range*: It enables efficiency maximization over full working points.
- *Critical temperature-dependency of losses is built in*. It includes the temperature dependency of semiconductor on-resistance and winding resistance.
- *Multivariable analysis*: The inputs of the proposed loss model include several groups of parameters that have impacts on loss generation: operating points, modulation mode switch, design parameters, loss-related properties of components and temperature information. Fig. 4.1 demonstrates all the model's input variables.

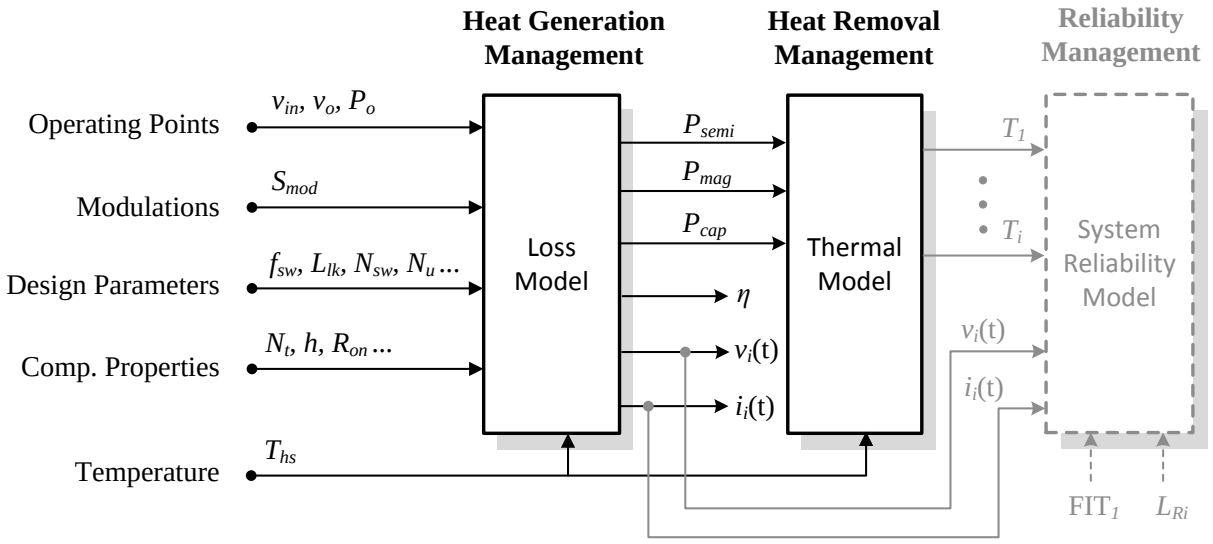


Fig. 4.1 Inputs and outputs of the system loss model and thermal model

The loss model's input variables are introduced here:

- *Operating points*

  These parameters cover the input and output voltage (V_{in}, V_o) and power level (P_o). They define the range in which the converter works.
- *Modulation*

This parameter informs the loss model under which modulation method (S_{mod}) the waveforms will be generated;

- *Design parameters*
  These include component parameters that influence the operating property of the converter, such as switching frequency (f_{sw}), inductance of magnetic components, transformer turn ratio and the count of switches (N_{sw}) or converter units (N_u) in parallel. These parameters present targets to be optimized.
- *Components properties*
  This part contains the key loss-related component parameters to be designed. For high-current converters, these parameters include transformer-turn ratio (N_t), winding configuration (e.g. thickness h) and Steinmetz parameters of the applied core material, semiconductors' on-resistance (R_{on}), and diode forward voltage (V_d). For high-frequency converters, the capacitances of semiconductors are also important to be involved. If some of these parameters have no freedom to vary, they are set as invariable (or fixed) parameters within the loss model instead of variables to be designed.
- *Temperature*
  Electrical resistance varies with temperature (especially the semiconductor on-resistance), so do conduction losses. Taking this temperature-dependency into account is important in loss modeling, especially for high-current converters where modeling accuracy is required over a wide operating range. This temperature can be the cooling surface temperature of the heatsink (T_{hs}). This temperature-dependency will be included in both waveform construction and conduction loss calculation in the loss model.

As illustrated in Fig. 4.1, the outputs of the loss model include the loss and waveform of each power components, and the system efficiency (η). The calculated losses and temperature T_{hs} will be passed down to the system thermal model for heat removal management. The component temperatures generated from the thermal model and the component stress information from the loss model are two important inputs to the system reliability model to check if the specified system lifetime requirement has been met. This reliability management falls outside the scope of this work.

Two steps constitute the proposed loss model: 1) Waveform construction and 2) Loss calculation**.** Waveform construction builds the current and voltage waveforms of main power components over the full operating range, and this information is fed to the subsequent step, loss calculation. The involvement of the input variables in each step is shown in Fig. 4.2. In order to take the non-ideal circuit factors into account for better modeling accuracy, the component properties and temperature information are involved in the waveform construction. These two modeling steps are explained in depth below.

4.3 Waveform Construction

This section first introduces the ideal waveform construction that does not take any loss into account, and then describes how to incorporate non-ideal factors in the high-current converters to increase the waveform modeling accuracy.

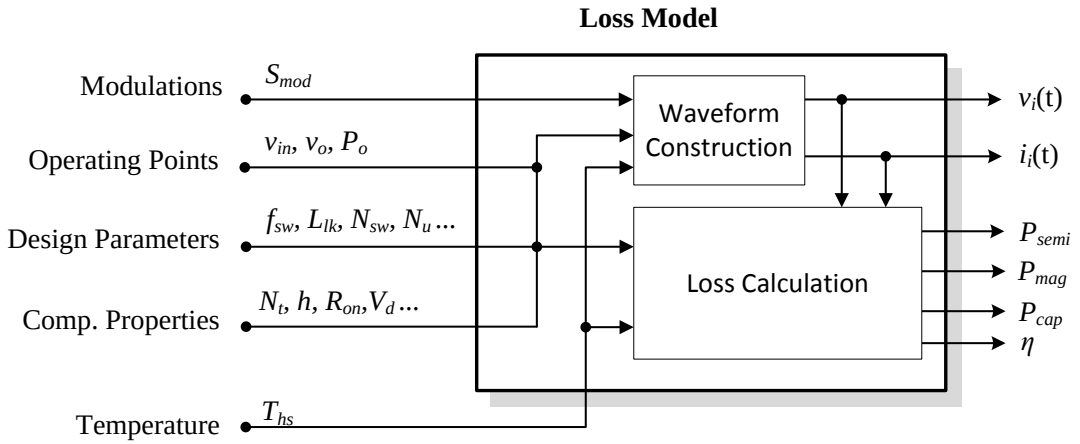


Fig. 4.2 Involvement of all input variables in the waveform construction and loss calculation steps

4.3.1 Ideal Waveform Construction

According to the modulation method deployed, waveforms of components in a lossless circuit can be analytically modeled based on the modulation equations described in Chapter 3. In PE converters like DAB, where the current waveforms of main power components are piece-wise linear, initially, each turning point on the current waveforms and the time intervals between them need to be calculated. Voltage waveforms are built based on the operating input and/or output voltages applied and time intervals related to the modulation method used.

A general form of the ideal waveform function is defined in Fig. 4.3, where the operating points, design parameters, modulation, and key component properties are involved as variables to define the waveform turning points and time intervals. Below, an example of building the transformer winding current waveform in the DAB with rectangular modulation method is shown. This waveform is referred to the input voltage (V_i) side. First, each turning point of the winding current waveform (illustrated in Fig. 4.4) and time interval are defined in Eq. (4-1)

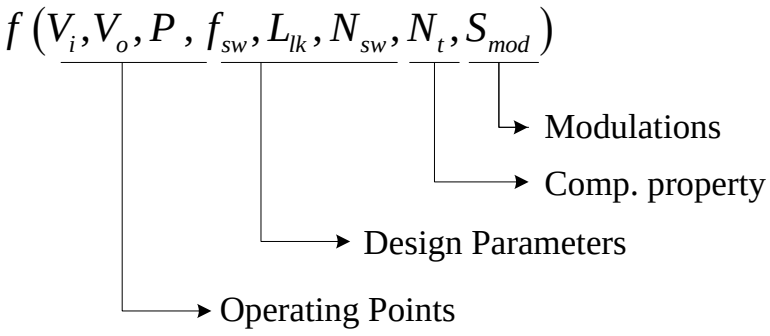


Fig. 4.3 General form of the waveform modeling equations

and Eq. (4-2), respectively.

$$t_0 = 0, \quad t_\pi = \frac{1}{2 f_{sw}}$$
$$t_\delta\left(V_i, V_o, P, f_{sw}, L_{lk}, N_t\right) = \frac{V_i - \sqrt{V_i^2 - 8 V_i L_{lk} f_{sw} \left| P / V_o \right| N_t}}{2 f_{sw} V_i} \tag{4-1}$$

$$i_0\left(V_i, V_o, P, f_{sw}, L_{lk}, N_t\right) = -\frac{1}{L_{lk}}\left[\frac{V_o}{N_t} \cdot t_\delta + \frac{1}{4 f_{sw}}\left(V_i - \frac{V_o}{N_t}\right)\right]$$
$$i_\delta\left(V_i, V_o, P, f_{sw}, L_{lk}, N_t\right) = \frac{1}{L_{lk}}\left[V_i \cdot t_\delta + \frac{1}{4 f_{sw}}\left(V_i - \frac{V_o}{N_t}\right)\right] \tag{4-2}$$
$$i_\pi\left(V_i, V_o, P, f_{sw}, L_{lk}, N_t\right) = i_0\left(V_i, V_o, P_o, f_{sw}, L_{lk}, N_t\right)$$

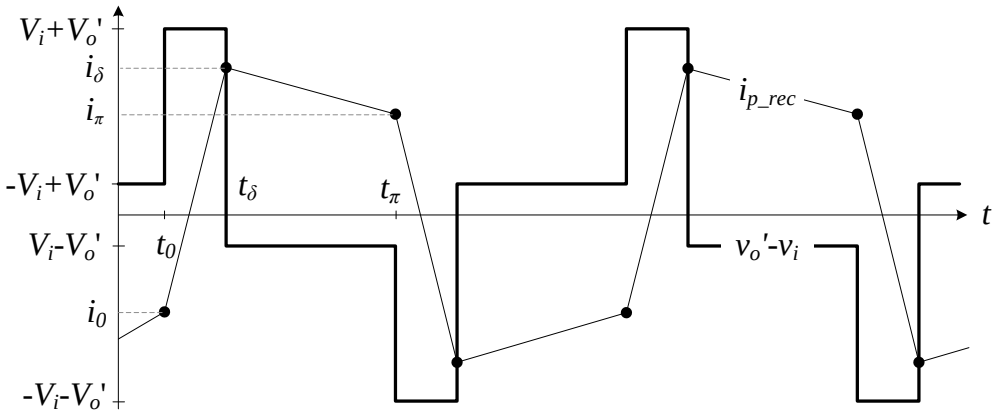


Fig. 4.4 Current and voltage waveforms of the energy transfer inductor in a DAB, referring to the input side

Here, the input and output voltages are considered equal to the excitation voltages across the energy transfer inductance of DAB converters. In this case, the winding current as a function of time during one steady-state switching cycle can be written as follows:

$$i_{p\_rec}\left(V_i, V_o, P, f_{sw}, L_{lk}, N_t, t\right) = \begin{cases} i_0 + \dfrac{V_i + V_o / N_t}{L_{lk}} \cdot t & \left[0 \le t < t_\delta\right] \\ i_\delta + \dfrac{V_i - V_o / N_t}{L_{lk}}\left(t - t_\delta\right) & \left[t_\delta \le t < \dfrac{1}{2 f_{sw}}\right] \end{cases} \tag{4-3}$$

where i_0 and i_δ are defined in Eq. (4-2). The winding current is calculated similarly for other two modulations, then the winding current under three modulation methods are

$$i_p\left(V_i, V_o, P, f_{sw}, L_{lk}, N_t, S_{mod}, t\right) = \begin{cases} i_{p\_rec}\left(V_i, V_o, P, f_{sw}, L_{lk}, N_t, t\right) & if\ S_{mod} = 0 \\ i_{p\_trap}\left(V_i, V_o, P, f_{sw}, L_{lk}, N_t, t\right) & if\ S_{mod} = 1 \\ i_{p\_tri}\left(V_i, V_o, P, f_{sw}, L_{lk}, N_t, t\right) & if\ S_{mod} = 2 \end{cases} \tag{4-4}$$

where S_{mod} is the modulation index, and 0, 1, 2 represent the rectangular, trapezoidal and triangular modulations, respectively.

4.3.2 Inclusion of Non-Ideal Factors

Ideal waveform construction originates from the volt-second balance principle of magnetics or the resonance over the *LC* resonance tanks. For DAB converters, the waveforms are derived on the volt-second balance of the inductance in series with the transformer. To increase the waveform modeling accuracy, the excitation of this energy transfer inductance must be accurately described. Therefore, any non-ideal factors that deviate the inductor excitation voltages away from the input and output voltages should be taken into account. In low-voltage and high-current converters, the critical non-ideal elements include the diode forward voltage, component resistance and circuit parasitic resistances distributed along the current flowing path. These resistances include high-current fuse resistance, semiconductor on-resistance, winding resistance, and PCB track resistance and so on. These resistances and diode-forward voltage represent the great conduction loss generated in high-current applications. Note that the impact of non-conduction losses, such as semiconductor switching loss and magnetic core loss, are neglected in this loss modeling approach because of their relatively lower contribution to the total loss in high-current converters.

These conduction loss contributors are incorporated to update the ideal waveforms generated based on the voltage-second balance of the energy transfer inductance. Fig. 4.5 illustrates the conduction loss contributors in the DAB when the input power is transferred directly to the output. This is an equivalent circuit referred to the low-voltage side. It can be observed that the major errors between the terminal voltages and excitation voltages on both sides of the energy transfer inductor come from the fuse resistance (R_{fuse}), semiconductor on-resistances (R_{on}), winding resistances (R_{pri} and R_{sec}') and the diode forward voltage (V_d') on the HV side. The excitation voltages of the inductor can be updated as:

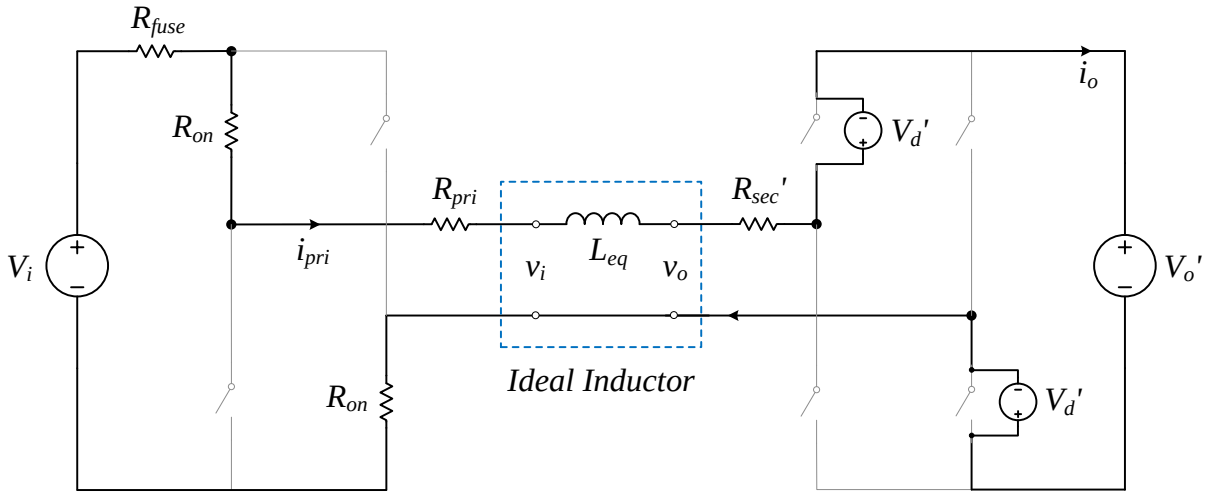


Fig. 4.5 Equivalent circuit of DAB referred to the low-voltage side, when power transferred directly from input to output.

$$v_i\left(V_i,P\right)=V_i-\left(2R_{on}+R_{sen}+R_{pri}\right)\cdot P/V_i$$
$$v_o\left(V_o,P,N_t\right)=\frac{V_o+2V_d}{N_t}+\frac{R_{sec}{}'}{N}\cdot\frac{P}{V_o} \tag{4-5}$$

Note that AC winding resistances are considered (the calculation can be found in Appendix A). Note that the semiconductor on-resistance can be made temperature-dependent, therefore, the temperature can be another variable to both voltages. The time intervals in Eq. (4-1) and current waveforms in Eq. (4-2) are renewed by Eq. (4-4) as Eq. (4-6) and Eq. (4-7):

$$t_0=0,\quad t_\pi=\frac{1}{2f_{sw}}$$
$$t_\delta\left(V_i,V_o,P,f_{sw},L_{lk},N_t\right)=\frac{v_i\left(V_i,P\right)-\sqrt{v_i\left(V_i,P\right)^2-8L_{lk}f_{sw}\left|P/v_o\left(V_o,P,N_t\right)\right|N_t\cdot v_i\left(V_i,P\right)}}{2f_{sw}v_i\left(V_i,P\right)} \tag{4-6}$$

$$i_0\left(V_i,V_o,P,f_{sw},L_{lk},N_t\right)=-\frac{1}{L_{lk}}\left\{\frac{v_o\left(V_o,P,N_t\right)}{N_t}\cdot t_\delta+\frac{1}{4f_{sw}}\left[v_i\left(V_i,P\right)-\frac{v_o\left(V_o,P,N_t\right)}{N_t}\right]\right\}$$
$$i_\delta\left(V_i,V_o,P,f_{sw},L_{lk},N_t\right)=\frac{1}{L_{lk}}\left[v_o\left(V_o,P,N_t\right)\cdot t_\delta+\frac{1}{4f_{sw}}\left[v_i\left(V_i,P\right)-\frac{v_o\left(V_o,P,N_t\right)}{N_t}\right]\right] \tag{4-7}$$
$$i_\pi\left(V_i,V_o,P,f_{sw},L_{lk},N_t\right)=i_0\left(V_i,V_o,P_o,f_{sw},L_{lk},N_t\right)$$

The ideal winding current waveform and the waveform considering the conduction loss are compared in Fig. 4.6 with measured waveform on a 1 kW DAB with 12V input and 347 V output. It can be found that the loss-considered waveform matches the measurement much than the ideal waveform.

4.4 Loss Calculation

Waveform construction provides voltage and current information for the loss calculation step. Besides the waveform information, the loss-related component parameters should also be well known before carrying out the loss calculation. These parameters mainly include the on-state resistance and switching energy of power semiconductors, winding DC resistance and the winding arrangement, magnetic core material and the equivalent series resistances (ESR) of capacitors at the frequency of interest.

Some of these loss-related parameters are temperature and/or voltage dependent. If the design interests cover a wide operating range, the key temperature-dependent and/or voltage-dependent component parameters should be well modeled to guarantee the loss modeling accuracy over the wide operating range. In high-current converters, the semiconductor on-resistances over the wide operating range should be well defined. The approach to model the on-resistance of semiconductors in high-current topology will be discussed later.

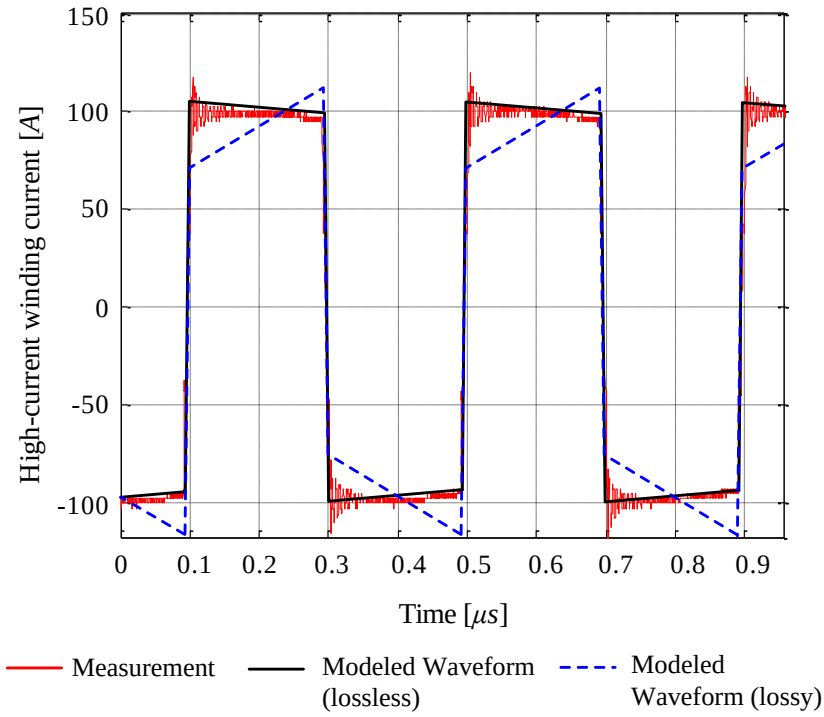


Fig. 4.6 Comparison of the ideal winding current waveform, the loss-considered waveform and the measured waveform, on 1 kW DAB with 12 V input and 347 V output

The analytical loss calculation methods for semiconductors and magnetic components are summarized in Chapter 2. The main outputs of the loss model are component losses and system losses. Because all the loss functions involve waveform functions, they share the same input variables. As an example, the general form of the loss functions is given in Eq. (4-8):

$$P_{loss}\left(V_i, V_o, P, f_{sw}, L_{lk}, N_{sw}, N_t, T_{hs}, S_{mod}\right) \tag{4-8}$$

Heatsink temperature T_{hs} is involved here to consider the temperature-dependency of power semiconductors, which will be introduced below.

4.4.1 Modeling of Critical Resistances

The precise modeling of critical resistances is very important to the loss calculation accuracy for low-voltage and high-current converters. The critical resistances include semiconductor on-resistances and winding AC resistances. The planar winding AC resistance modeling is explained in Appendix A and so, only the semiconductor on-resistance modeling is concerned below. Since MOSFETs are popular in low-voltage applications and therefore the on-resistance of MOSFETs is focused here. The method to model the temperature-dependency is emphasized.

Finding the correct on-resistance at different operating conditions and temperatures is a dynamic process. When the current in semiconductor increases, semiconductor loss rises accordingly. Higher loss raises the junction temperature, which in turn drives the on-resistance even higher. The resulted larger on-resistance again causes more loss. This process will stop until a thermal balance is reached: loss generated equals the power dissipated to the cooling system.

It is expected that modeling on-resistance involves the information of cooling system. Fig. 4.7 shows the thermal network from junction of a MOSFET attached against a heatsink to the air, where the junction temperature T_j is calculated as

$$T_j = P_{MOS\_loss}\left(R_{th\_jc} + R_{th\_ca}\right) + T_a \tag{4-9}$$

where P_{MOS_loss} is the total loss in MOSFET, R_{th_jc} and R_{th_ca} are the thermal resistance from MOSFET junction to its case and from the case to the ambient, respectively. Here, the case temperature T_c is calculated as

$$T_c = P_{MOS\_loss} R_{th\_ca} + T_a \tag{4-10}$$

and junction temperature T_j is

$$T_j = P_{MOS\_loss} R_{th\_jc} + T_c \tag{4-11}$$

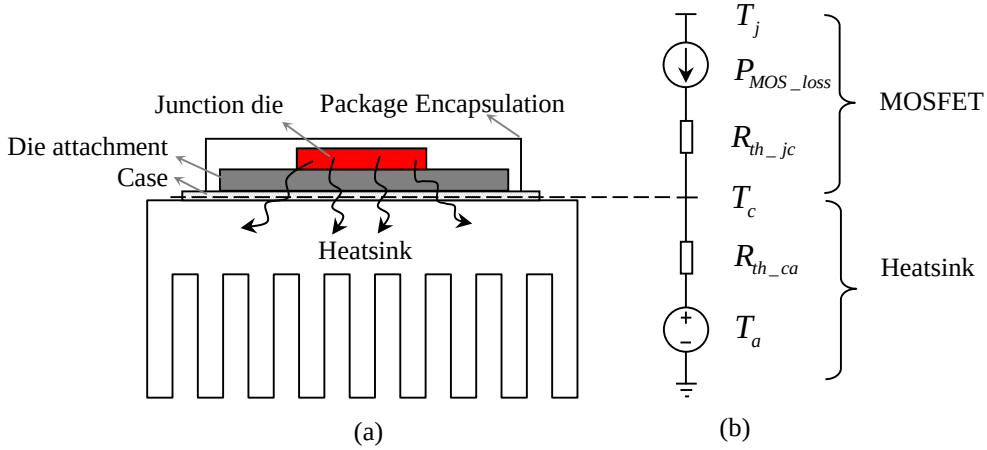


Fig. 4.7 (a) A MOSFET attached with its cooling system and (b) its equivalent thermal network

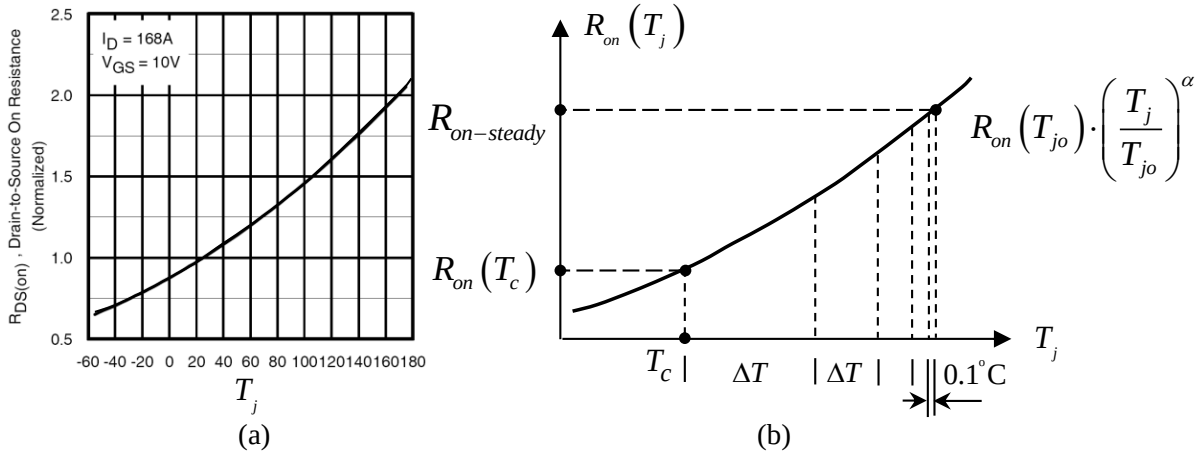


Fig. 4.8 (a) A typical $R_{on}(T_j)$ curve of MOSFETs; (b) iterative process to find the steady-state

The main idea proposed here is to model R_{on} related to heatsink temperature (T_c) and thermal resistance from junction to case (R_{th_jc}), in such a way that both the electrical and thermal systems can be designed with a common heatsink temperature. Here, T_c becomes another input

variable to the loss model. R_{on} is directly related to the junction temperature of MOSFET, however, an iterative calculation process can retrieve R_{on} from T_c, R_{th_jc} and loss generated in the MOSFET.

First, the $R_{on}(T_j)$ function can be extracted from the datasheet of the selected MOSFET. It can be observed from a typical $R_{on}(T_j)$ curve of MOSFETs (Fig. 4.8(a)) that the curve tends to be a part of parabola and $R_{on}(T_j)$ can be structured by curve-fitting techniques in the following form:

$$R_{on}\left(T_j\right) = R_{on}\left(T_{j0}\right) \cdot \left(\frac{T_j}{T_{j0}}\right)^a \tag{4-12}$$

where $R_{on}(T_{j0})$ is the on-resistance at the given tested temperature T_{j0}, normally 298 K (25 ^oC). The temperature value in Eq. (4-12) is expressed in Kelvins. The curve-fit power α normally ranges from 1.5 for low voltage MOSFET (<100V) to 2.5 for medium and high voltage MOSFETs (> 400V).

After determining the value of $R_{on}(T_j)$, the iterative process can be started assuming the junction temperature to be the designed T_c (as an initial guess). Using R_{on} at $T_j = T_c$ to calculate the first conduction loss, together with the calculated switching loss, the total semiconductor loss P_{MOS_loss} and new junction temperature can be obtained via Eq. (4-11). The R_{on} at the new

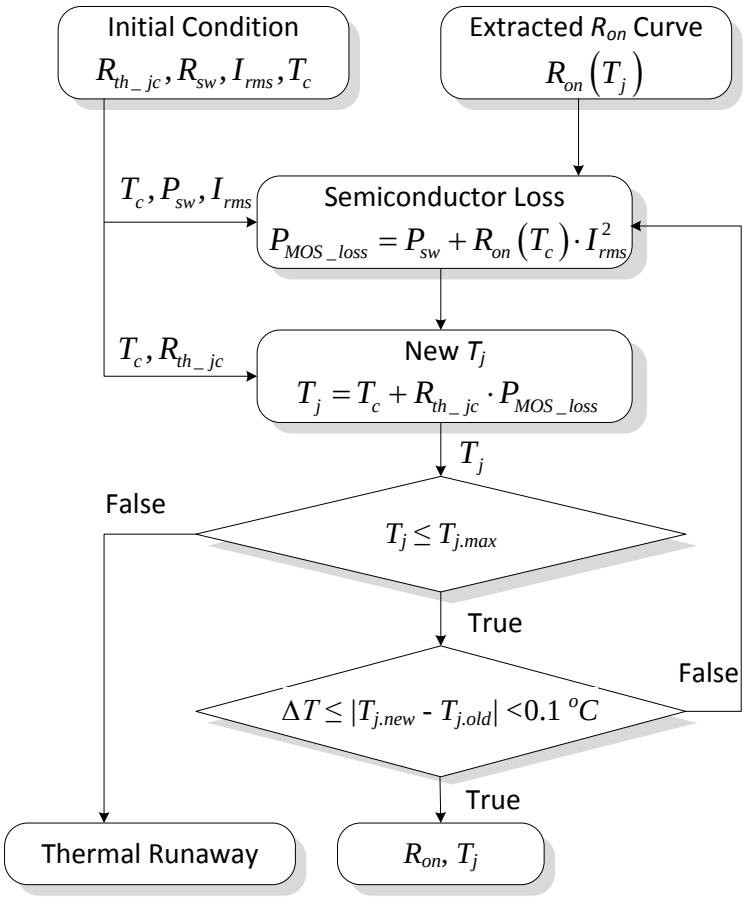


Fig. 4.9 Iterative process to find the R_{on} and T_j at steady-state

junction temperature can be used to calculate the new loss again. This iterative process is continued and when the temperature difference between the new T_j and T_j at the previous iterative step is very small, e.g. less than 0.1 ^{o}C, it can be said that the steady-state is achieved. In this process, if T_j at certain operating conditions is higher than the maximum designed junction temperature, this design indicates a thermal runaway and is considered unacceptable. This iterative process to find the steady-state R_{on} and T_j is illustrated in the flowchart Fig. 4.9. Note that the switching loss should be calculated before this iterative process and has nearly no dependence on temperature. Since $R_{on}(T_j)$ curve given in datasheets is tested at specified gate voltage and higher gate voltage reduces R_{on}, the gate voltage used in designed converters should not be smaller than that used in datasheets.

If the switching loss (P_{sw}) is far smaller than the conduction loss (P_{cond}), in cases of low-frequency, low voltage but high-current applications, the proposed iterative calculation above can be replaced by an experimental procedure can be employed to directly identify the R_{on} at certain given T_c and RMS current.

Experimental extraction of R_{on} when $P_{sw} << P_{cond}$

This section proposes a useful and practical method of correlating R_{on} with the semiconductor heatsink temperature T_c and drain current I_d from experiments when the switching loss P_{sw} is much smaller than the conduction loss P_{cond}. In the experiments with a constant T_c, R_{on} is found to be approximately with a second order dependency on the drain current I_d , then R_{on} can be defined as:

$$R_{on}\left(I_d\right) = A + B \cdot I_d + C \cdot I_d^2 \tag{4-13}$$

A, *B*, *C* represent the curve coefficients at a certain T_c and can be obtained by a 2nd order polynomial curve-fitting from the measured R_{on}–I_d curves. *A*, *B* and *C* are temperature-dependent and should be correlated with T_c. If two case temperatures (T_0, T_1) are sampled, the R_{on}'s dependency on T_c can be linearly modeled. More temperatures sampled result in a higher order of dependency and more accurate results. Linear temperature dependency can be defined as:

$$\begin{aligned} A\left(T_c\right) &= a_o + a_1 \cdot T_c \\ B\left(T_c\right) &= b_o + b_1 \cdot T_c \\ C\left(T_c\right) &= c_o + c_1 \cdot T_c \end{aligned} \tag{4-14}$$

where

$$\begin{aligned} x_0 &= \frac{x_{T_0} \cdot T_1 - x_{T_1} \cdot T_0}{T_0 - T_1} \\ x_1 &= \frac{x_{T_0} - x_{T_1}}{T_0 - T_1} \end{aligned} \tag{4-15}$$

where $x = a, b, c$, respectively. Hence, the function of $R_{on}(T_j, I_d)$ can be calculated as

$$R_{on}(T_c, I_d) = A(T_c) + B(T_c) \cdot I_d + C(T_c) \cdot I_d^2 \tag{4-16}$$

Here the extraction of R_{on} of a MOSFET module is presented as a case study. The case substrate of a MOSFET module is tightly pressed against the temperature plate of Julabo heating circulator (Model: FP50) (Fig. 4.10(a)). The plate temperature is controlled by the heating circulator and is also the module case temperature. All the MOSFETs in the module are turned on with the gate voltage 12 V, which is the same as the gate voltage in the converter in which the module is working. Six MOSFET chips are placed in one module, with three in parallel as one set, and two sets connected in series. Therefore, a common gate causes the module resistance to be 2/3 on-resistance of a single MOSFET chip (Fig. 4.10(b)). The current is injected into the drains of top MOSFETs from DC power supply. For $R_{on}(T_c, I_d)$ calibration, the temperature plate was fixed at 40 ^{o}C and 55 ^{o}C, respectively, and current was increased at a step of 20 A. The current value is observed by measuring the voltage drop on a 0.1 mΩ shunt in series with the module. R_{on} of a single MOSFET chip is then calculated as 1.5 times of the ratio from measured voltage to current. Two $R_{on}(T_c, I_d)$ curves were obtained at 40 ^{o}C and 55 ^{o}C. From these two curves, all the coefficients required in Eq. (3.9) are calculated by curve fitting. To verify the calibrated $R_{on}(T_c, I_d)$, another curve is measured with T_c at 60 ^{o}C and it matches well with the calibrated function (Fig. 4.11).

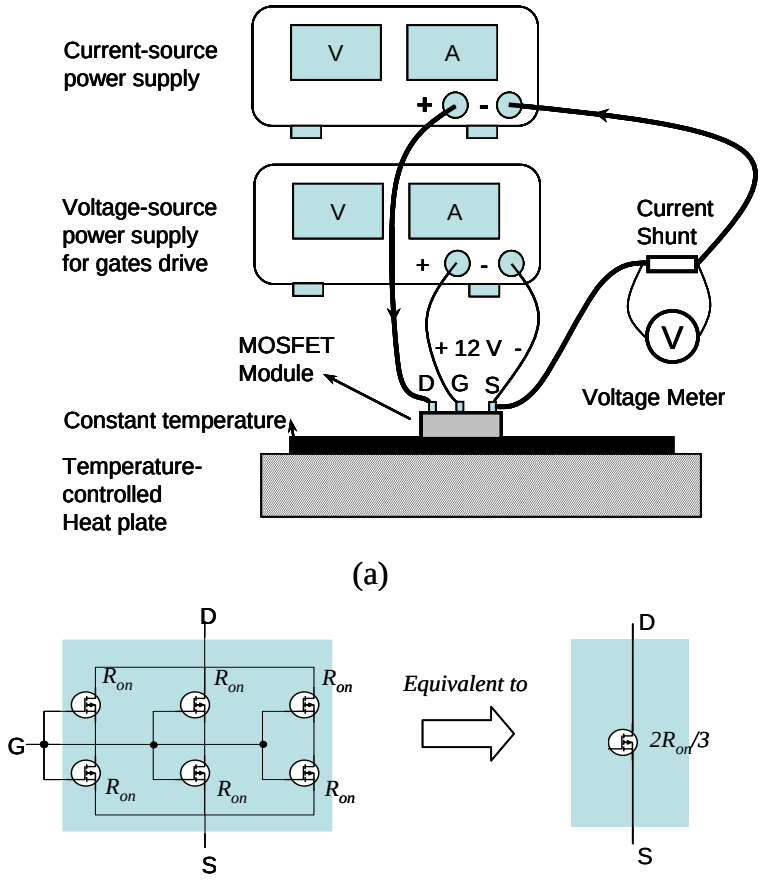


Fig. 4.10 The setup of extracting $R_{on}(T_c, I_d)$ of MOSFET chip; (b) the connection of pins in the MOSFET module during the measurement

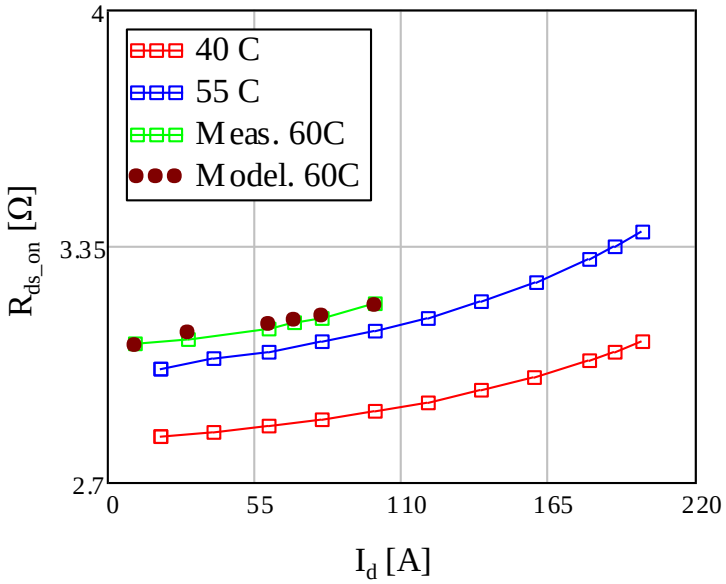


Fig. 4.11 Measured $R_{on}(T_c, I_d)$ curve at T_c = 40 °C and 55 °C, and verification of the modeled $R_{on}(T_c, I_d)$ at T_c = 60 °C

The extracted $R_{on}(T_c, I_d)$ function directly describes the relation between on-resistance, T_c, and current at steady-state. It can be inserted into the loss model to correct the waveform and get the conduction loss without any iterative calculation. This method has advantages of low computation effort and high accuracy, but the experimental setup time is high and it can be used only when the semiconductor types are confirmed.

4.5 Model Verification

The loss model should be validated on the component level and system level before being used to optimize the design.

4.5.1 Semiconductor Losses

Methods using a digital oscilloscope to measure the loss in semiconductors were recorded in literature [4-4][4-5]. They are susceptible to measurement errors and are time-consuming [4-6]. Calorimetric methods are very accurate [4-6], but cannot measure the losses in all components during the converter operation. A practical way to measure the loss in double-sided SMD semiconductors or semiconductor modules is proposed in [4-7]. The basic idea is to place a heatsink system with known thermal resistance to the ambient (R_{th_hk}) beneath the semiconductors, the semiconductor losses P_{tot} can be calculated by measuring the temperature difference between the ambient temperature (T_a) and the temperature of the heatsink surface (T_c). T_c is measured right underneath the semiconductor modules.

$$P_{tot} = \frac{T_c - T_a}{R_{th\_hk}} \tag{4-17}$$

The measured heatsink surface temperature can be used as the input parameter T_c to the loss model and the corresponding modeled semiconductor losses are then compared with the

measured values to verify the loss model. Fig. 4.12 gives an example of the setup to measure the losses of semiconductor modules in a low-profile converter. To validate the model at different T_c, the drive voltage of the fan should be tuned to vary the thermal resistance of the heatsink. However, the thermal resistance of the heatsink at the according fan drive voltages should be measured beforehand.

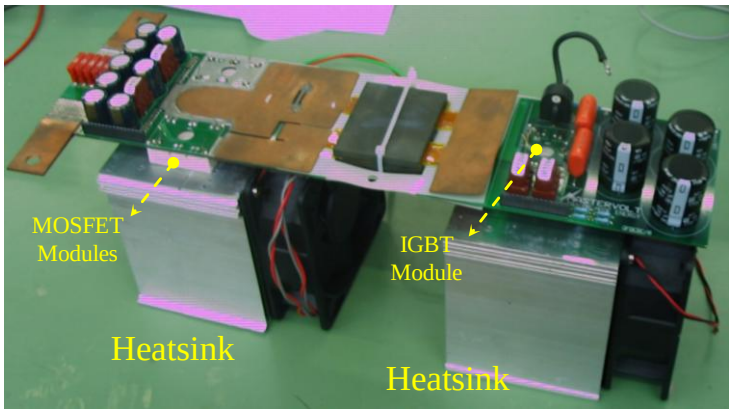


Fig. 4.12 Loss measurement of semiconductor modules in a low-profile DAB converter [4-7]

4.5.2 Transformer Losses

It is difficult to experimentally measure losses in high-frequency transformers when the converter is operating. The following section introduces a practical method by which the transformer loss model can be validated.

Winding loss

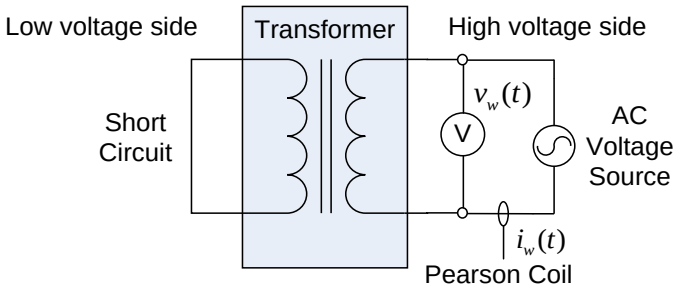
Because the winding losses are calculated by summing the modeled losses in the first tens of current harmonics, calculating accuracy can be guaranteed if the loss model is accurate at certain harmonics. To measure the loss in the transformer winding under certain sinusoidal current excitation, additional tests should be done. The test circuit diagrams are given in Fig. 4.13(a).

The high-current winding is shorted and the low-current side is fed by sinusoidal voltage source under certain frequency. The current and terminal voltage waveforms are recorded by a digital oscilloscope via Pearson coil (model: 2877) and probe. As the core excitation voltage is very low due to the shorted winding, the loss in the core can be neglected and the instantaneous product of measured voltage and current can be integrated over one period to obtain the copper loss power (Eq. (4-18)):

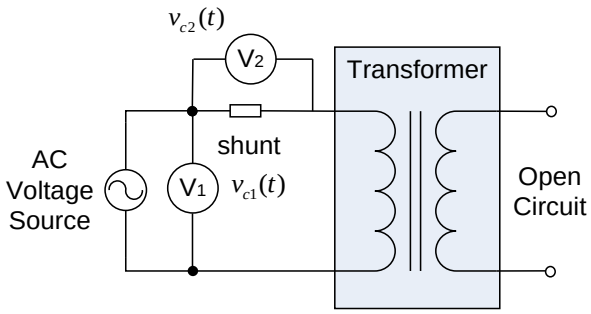
$$P_w = \frac{1}{T}\int_0^T i_w(t)v_w(t)\cdot dt \tag{4-18}$$

Core loss

Calorimetric loss measurement is the most accurate method of loss measurement and is used by many researchers for core loss measurement in well equipped labs. However, the great effort required to implement the calorimetric measurement makes it impractical for engineers.



(a) Copper Loss Measurement



(b) Core Loss Measurement

Fig. 4.13 Circuit diagrams to measure the transformer losses (a) winding loss measurement (b) core loss measurement

A digital oscilloscope is again chosen to measure the core loss. Assuming the accuracy of the modified Steinmetz equation, only the parameters in the original Steinmetz's equation for used core material given in the literature are validated for a range of excitation frequency. The test circuit diagram is shown in Fig. 4.13(b). The high-voltage side is open in such a way that the current flowing through the low-voltage winding is only a result of the core loss. If the shunt resistor R_{shunt} does not exist, the core loss can be calculated by integrating the instantaneous product of the terminal voltage and current in one cycle. Owing to the very small loss, the phase shift between terminal voltage and current of the core are very close to 90^o, which causes the loss calculation to be very sensitive to the sampling delay of the digital oscilloscope and therefore very high error.

To decrease the phase shift and achieve higher calculation accuracy, a well-calibrated shunt resistor should be connected in series with the low-voltage winding of the transformer. The voltage measurement crosses the resistor and transformer winding and the current is indicated by measuring the voltage drop on the shunt resistor. The core loss is calculated as:

$$P_w = \frac{1}{T}\int_0^T \frac{v_{c2}(t)\cdot\left[v_{c1}(t)-v_{c2}(t)\right]}{R_{shunt}}\cdot dt \tag{4-19}$$

System Losses

In the final phase of model verification, the system loss must be validated by including other losses, like capacitor loss. A power analyzer can be used to measure the system loss by subtracting the measured output power from the input power.

4.5.3 Model Verification of a 1 kW DAB Converter

Based on the loss modeling approach proposed above, a loss model is built for a low-voltage, high-current DAB converter (12 V-350 V, 25 kHz and 1 kW). The model is validated on a converter prototype. Based on the verified loss model, the optimal operating ranges of three modulation methods are determined below to maximize the system efficiency over the full operating range.

DAB converter prototype

A high-current DAB converter needs to be built for marine application, to connect the storage battery to the DC power bus. The main given design specifications are 12V-350V, 1kW nominal power and 25 kHz. A converter prototype has been built (Fig. 4.14) in a low-profile PCB-based structure. MOSFETs and IGBTs are used as the switches on the low-voltage and high-voltage sides, respectively. Standard semiconductor module packages are employed and they are mounted on a common heatsink. The transformer has a turn ratio of 1:30, the high-voltage winding in PCB is sandwiched by two paralleled low-voltage windings, which are two copper sheets soldered on the PCB surfaces of both sides. Note that only the rectangular modulation is implemented on this prototype. This prototype is utilized as the verification workbench of the designed DAB loss model, and the validated loss model is in turn used to optimize the DAB topology design.

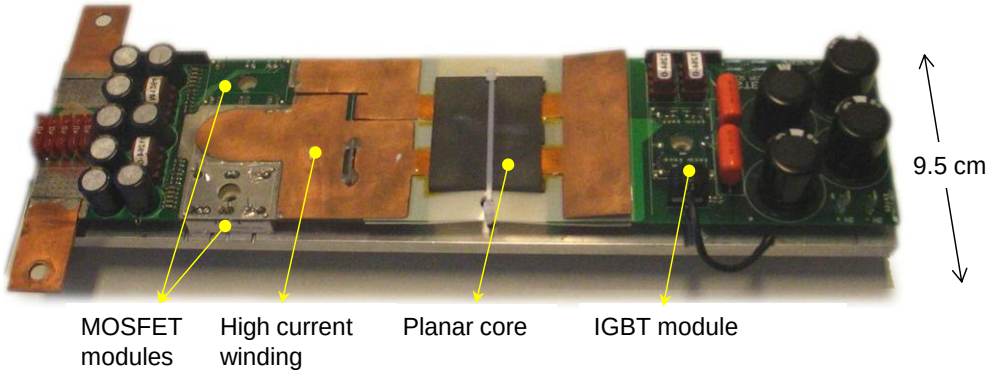


Fig. 4.14 The DAB converter prototype (12V/350V, 1 kW, 25 kHz)

Through a rough calculation, the switching loss is much less than the conduction loss in the MOSFET modules in this low-voltage and low switching frequency DAB converter. Therefore, the proposed method to extract MOSFET R_{on} from experiments is valid and the results have been shown in Fig. 4.11.

Using the semiconductor loss measurement setup illustrated in Fig. 4.12, the losses of the MOSFET and IGBT modules are measured. Fig. 4.15 shows the well-matched results of measured and modeled losses of MOSFET and IGBT modules.

The copper loss model is validated at several sinusoidal frequencies. With low-voltage winding shorted, sinusoidal currents are injected into the high-voltage winding. Consumed power

measured at the high-voltage winding terminals represents the generated copper loss. Fig. 4.16 shows the modeled and measured copper loss at 30 kHz and 40 kHz.

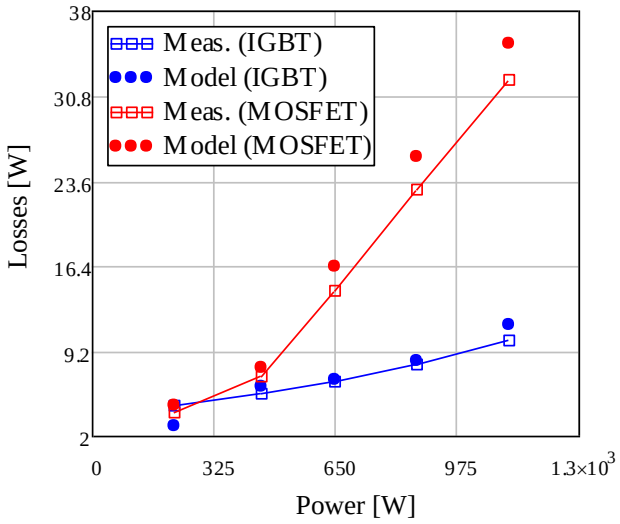


Fig. 4.15 Measured and modeled losses of MOSFET and IGBT modules (T_c = 31 °C and rated input/output voltages)

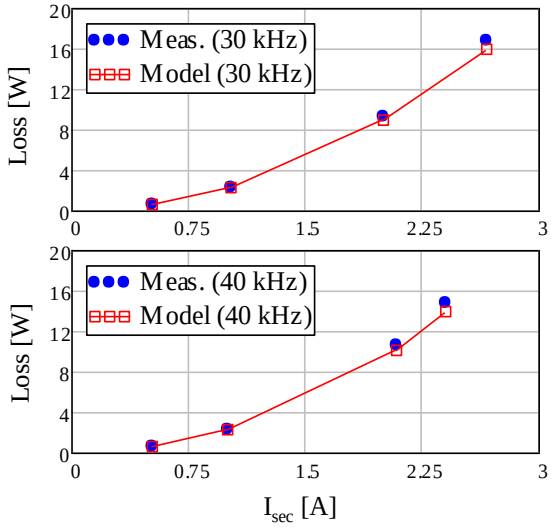


Fig. 4.16 Measured and modeled copper loss at 30 kHz and 40 kHz

The ferrite 3C90 is used as the magnetic core material. Via the proposed core loss measurement, the measured core losses are compared with the loss calculated from Steinmetz's equation at 20 kHz, 35 kHz and 100 kHz (Fig. 4.17). A satisfactory match can be observed except at the excitation voltage points higher than 12 V at 20 kHz curve. This mismatch occurs because the used AC voltage source cannot provide enough reactive power and hence, makes the voltage excitation distorted from sinusoidal form. Nevertheless, the use of given 3C90 Steinmetz's equation parameters in literature can be justified.

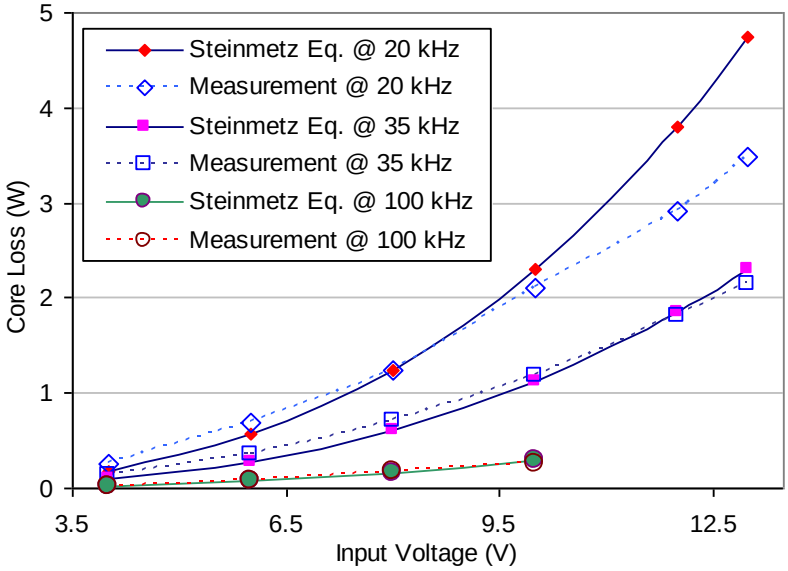


Fig. 4.17 Measured and modeled core losses at 20 kHz, 35 kHz and 100 kHz

As the final phase of the model verification, the system loss needs to be validated to include other losses, like capacitor losses. Power analyzer Delta-PZ4000 is used to measure the sys-

tem loss by subtracting the measured output power from the input power. Note that the MOSFET and IGBT modules are driven by an auxiliary power supply and the loss in drivers are not included in the system loss measurement and calculation. Fig. 4.18 shows the measured and modeled system losses at rated voltage 12V-350V. Considering the possible measurement error, the loss model can be considered accurate. Due to the high current level, the parasitic resistances from input terminals to MOSFETs are measured and the related losses are also included in the loss model.

The modeled loss distribution at the nominal operating condition (1 kW, 12 V~350 V) is given in Fig. 4.19. It can be observed that the transformer winding loss dominates the core loss, in which the loss in the secondary windings (PCB traces) is about two-fold of that in the high-current primary winding, which indicates a huge amount of heat is buried in the PCB. It can also be found that the ohmic loss in the parasitic resistances, including the input fuse resistance, the high-current connector resistance and its contact resistance with PCB, and the PCB trace resistance from the connectors to the MOSFETs, are notably high.

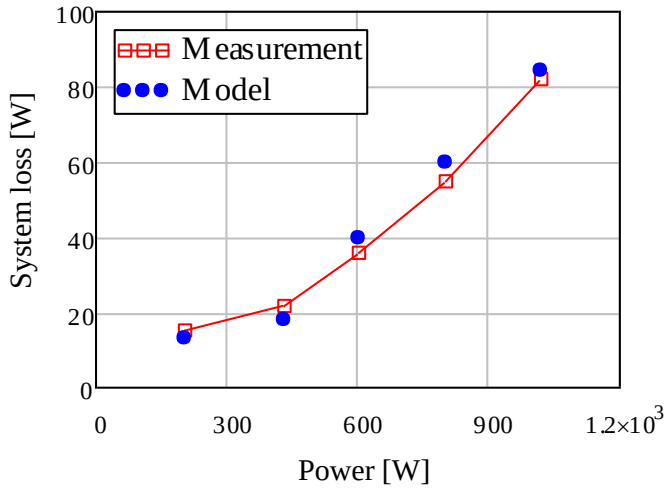


Fig. 4.18 Measured and modeled system loss (12 V ~ 350V, 25 kHz, L_{lk} = 125 μH, T_c = 31 °C)

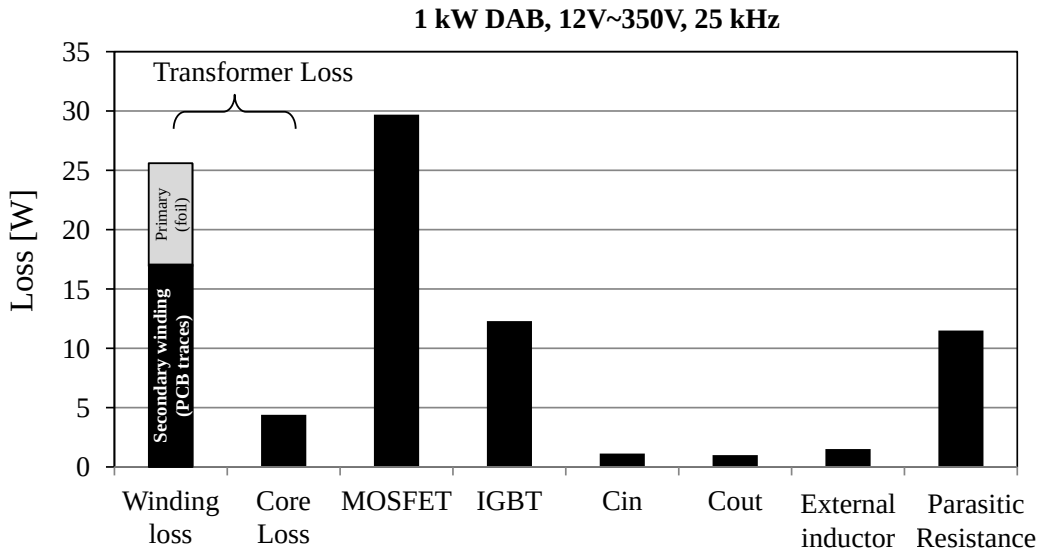


Fig. 4.19 The modeled loss distribution of 1 kW DAB at 12V~350V

4.6 Conclusions

An analytical loss modeling approach is proposed for low-voltage and high-current DAB converters. It fulfills the four KPIs of a loss model: high accuracy, low computation effort, multivariable analysis possibility and calculation capability over full operating range.

To realize the balance between the high accuracy and low computation effort in this loss model, the conduction loss is considered in the waveform modeling. Results show that precisely modeling the voltage-second balance principle of the energy transfer inductance is crucial for high waveform modeling accuracy. This can be conducted by taking into account the impact of critical resistances and voltage on the excitation voltages across the energy transfer inductance. These critical resistances include semiconductor on-resistor, winding resistances, circuit parasitic resistances and diode forward voltage.

Multi-variable analysis is enabled by the analytical functions that describe the operation of DAB converters in three modulation methods. The input variables to the model cover five groups of parameters: the operating points, modulation information, design parameters, component properties, and heatsink temperature. The calculation capability over the full operating range is enabled by the accurate waveform modeling over full range and the inclusion of the temperature-dependency of semiconductor on-resistances.

The loss model built for a 1 kW DAB converter has been validated experimentally. A heatsink-based method is proposed to measure the losses of semiconductor modules when the converter is operating, while the transformer loss model is validated offline. The winding loss model is verified at each of the current harmonics generated by an AC current source, and the core loss model is validated under a sinusoidal voltage source based on a measurement with digital oscilloscope.

This loss model will be utilized in high-current transformer optimization and a 2 kW DAB converter design in Chapters 5 and 6, respectively.

4.7 References

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Chapter 5

High-Current Planar Transformer Design

5.1 Introduction

Transformers provide galvanic isolation and/or voltage matching in isolated DC-DC converters [5-1]. In the autonomous power system of private marine vehicles, the isolated DC-DC converters, usually used to interface low-voltage (LV) back-up batteries with high-voltage (HV) DC bus, are often also characterized with high current on the battery side. Fig. 5.1 illustrates a typical example of marine onboard power network where three power sources can be found: onshore mains, an AC generator and lithium ion batteries. Mains onshore power the electrical apparatus onboard and recharge the batteries when ships are harbored. Usage of the onboard power source related to load profile in the course of sailing is given in Fig. 5.2. It shows that at steady state, LV lithium ion batteries (24V) together with the AC generator output 5 kW in total to load (batteries 2kW and generator 3 kW). However, during start-up, the power is exclusively provided by batteries, to start the generator engine with 10 kW in

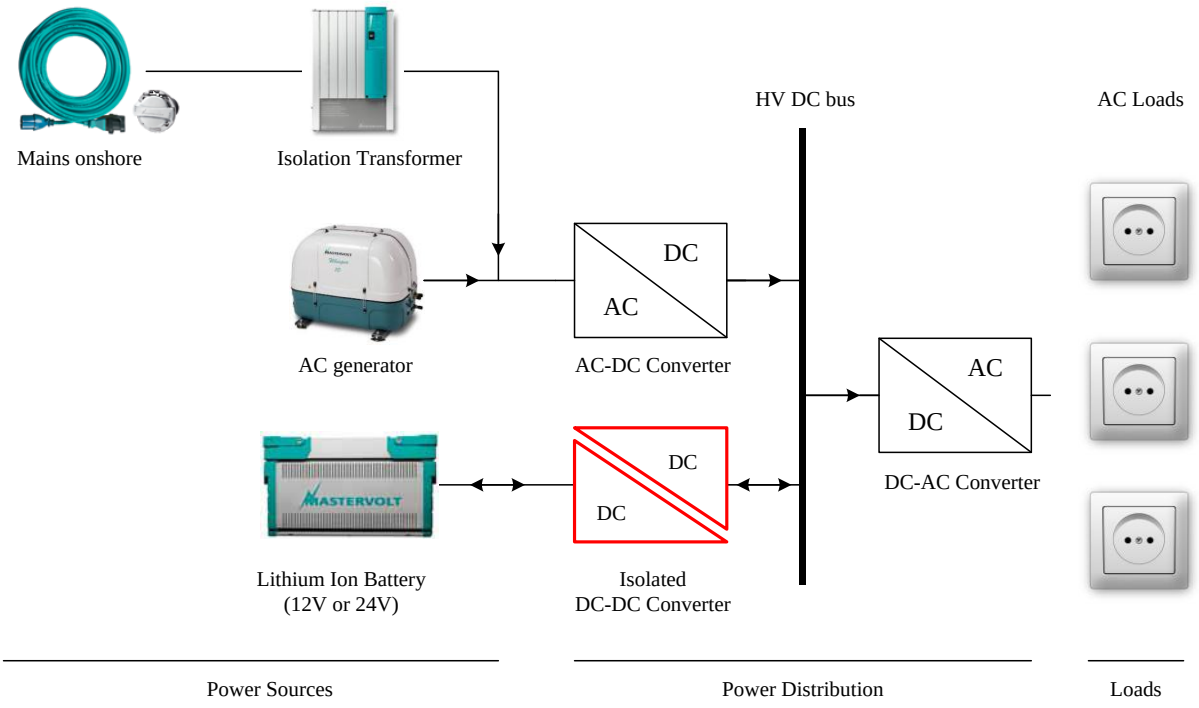


Fig. 5.1 The position of isolated DC-DC converter in marine onboard power network

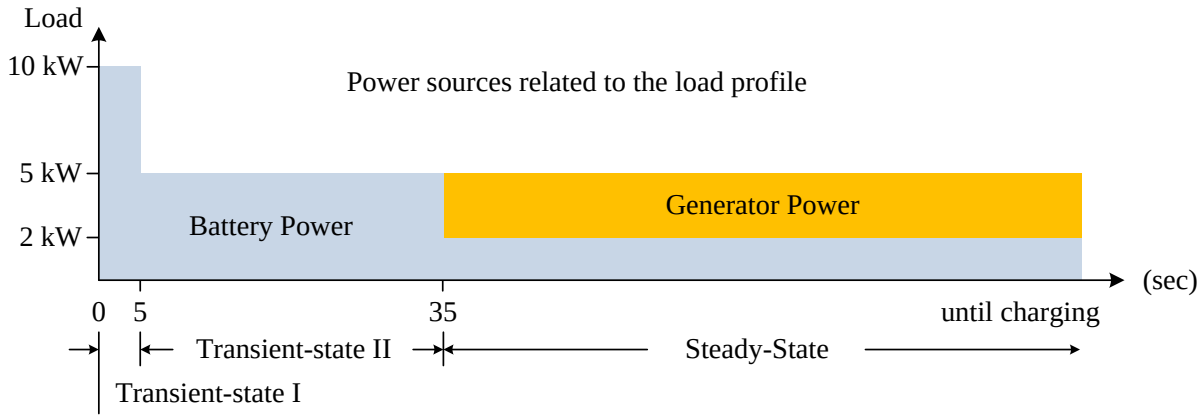


Fig. 5.2 An example of power source usage (24V LV lithium ion battery) related to the load profile onboard

transient-state I and to feed 5 kW load in transient-state II. Here, batteries are discharged and recharged through the isolated DC-DC converters. The power source usage implies a large input current of around 100 A to the isolated DC-DC converter at steady state and much more during transients. Additionally, because of limited space onboard, the isolated DC-DC converters need to be compact. In such applications, the transformers, as the most bulky components in isolated converters need to have the following characteristics:

- High turn ratio to match the voltage difference between LV input and HV DC bus.
- High-current handling capability.
- Compact size due to the limited space onboard.

Unfortunately, the requirements of both high current and compact size causes design difficulties from:

- *Heat generation*
  High current tends to generate a great mount of loss in windings.
- *Heat Conduction Path*
  Because windings are buried in the bulky magnetic core that is not well thermally conductive, the winding loss is difficult to be effectively transported to the cooling medium, easily resulting in a serious hotspot if the loss generated is significant.
- *Cooling Surface*
  Compact size limits the transformer surface area for heat removal.

Planar transformers have great potential to solve these problems and add value to the design, due to their superior thermal performance, a result of large surface-to-volume ratio (due to their low-profile structures), versatile winding types, low leakage inductance, easy winding termination, and manufacturing repeatability [5-2][5-3]. However, high-current (>100A) planar transformer design aiming at high power density is rarely reported in literature. This chapter will investigate this research topic.

TABLE 5.1 OPERATION SPECIFICATIONS OF DAB CONVERTER TO BE DESIGNED

Steady-State	
Input (Battery) voltage V_i	24 V (20 V~32 V)
Output (Bus) voltage V_o	360 V (300 V, 450 V)
Nominal load	2 kW
Transient-State	
Input (Battery voltage) V_i	20 V~24 V
Output voltage V_o	360 V
Transient load in transient state I	10 kW (5 seconds)
Transient load in transient state II	5 kW (30 seconds)

- In Section 5.2, the core and winding structures of planar transformer are reviewed. The heat generation and cooling characteristics of planar transformers are compared with barrel counterpart, to show its great benefits in high-current application.
- In Section 5.3, the necessity and boundary of using single-turn winding for high-current design is analyzed, with 12 V/1 kW DAB as the carrier. Three single-turn transformer designs are compared in terms of loss generation, temperature rise and volume. These transformers are 1) planar transformer with PCB-integrated windings, 2) planar transformer with PCB winding and Litz-wire winding, and 3) barrel transformer with copper foil and Litz wire. All magnetic cores discussed in this section are of ferrite material widely used in industry.
- In Section 5.4, the nanocrystalline-material-based planar transformer with C-shaped cores is proposed for high current application. The advantages of nanocrystalline material over ferrite are highlighted. Then, the core dimension optimization is investigated for a high-current DAB with high transient/nominal power ratio. The operation specifications of this DAB converter are given in TABLE 5.1. Here, a special design effort is engaged to control the leakage inductance to a required level, by manipulating the core and winding structures. Next, this nanocrystalline planar transformer is compared with a ferrite planar transformer, designed to the same specifications.
- PCB trace Current-Carrying Capacity (CCC) is of increasing importance to converter designs with high current, high switching frequency and high power density. The drawbacks of current design guidelines of PCB trace CCC are pointed out in Section 5.5. The methods of making new PCB trace CCC design guideline are also proposed in the same section. The detailed experimental results are attached in Appendix B.

5.2 Planar vs. Barrel Transformers

This section illustrates the benefits of the planar transformer concept by comparing the planar E-core transformers with commonly-used barrel wire-wound E-core transformers, in terms of magnetic core and winding structures, heat generation and heat removal properties.

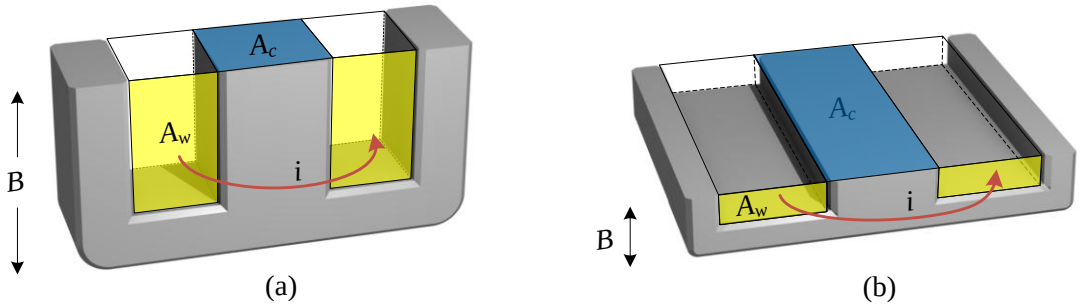


Fig. 5.3 Structure of (a) Barrel E-core and (b) Planar E-core

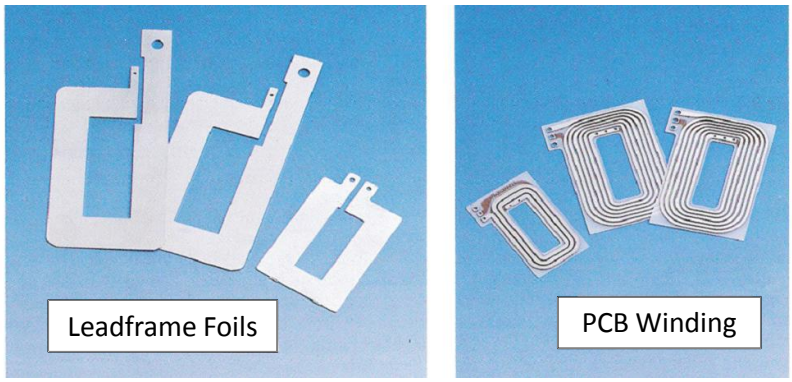


Fig. 5.4 Metal leadframe foil and PCB trace windings

5.2.1 Core and Winding Structures

Core Geometry

E-shaped magnetic cores are commonly used in isolated converters. Fig. 5.3 shows classic barrel E-core (a) and planar E-core (b), where the windings are wound around the center leg, causing magnetic flux to flow perpendicular to the flux area (A_c) and winding current perpendicular to the winding window area (A_w). Planar core has much lower height B than its barrel counterpart, which results in low profile geometry.

Windings

Windings of barrel transformers are normally made of solid wire, Litz wires or copper/aluminum foils, while planar transformers have additional options, such as leadframe foils and PCB traces, as shown in Fig. 5.4. These windings have the advantages of pre-tooling, automatic assembly, accurate positioning, and easy termination [5-4]. Again, these windings are in low profile. All of these windings can be implemented together in planar transformer design.

The exploded view of a planar transformer structure is illustrated in Fig. 5.5, where leadframe foil winding and four-layered PCB winding are combined. Due to high current carrying capacity, the leadframe foils are used as the high-current winding; while PCB traces are employed as the HV winding due to the isolation lamination layers in between copper layers.

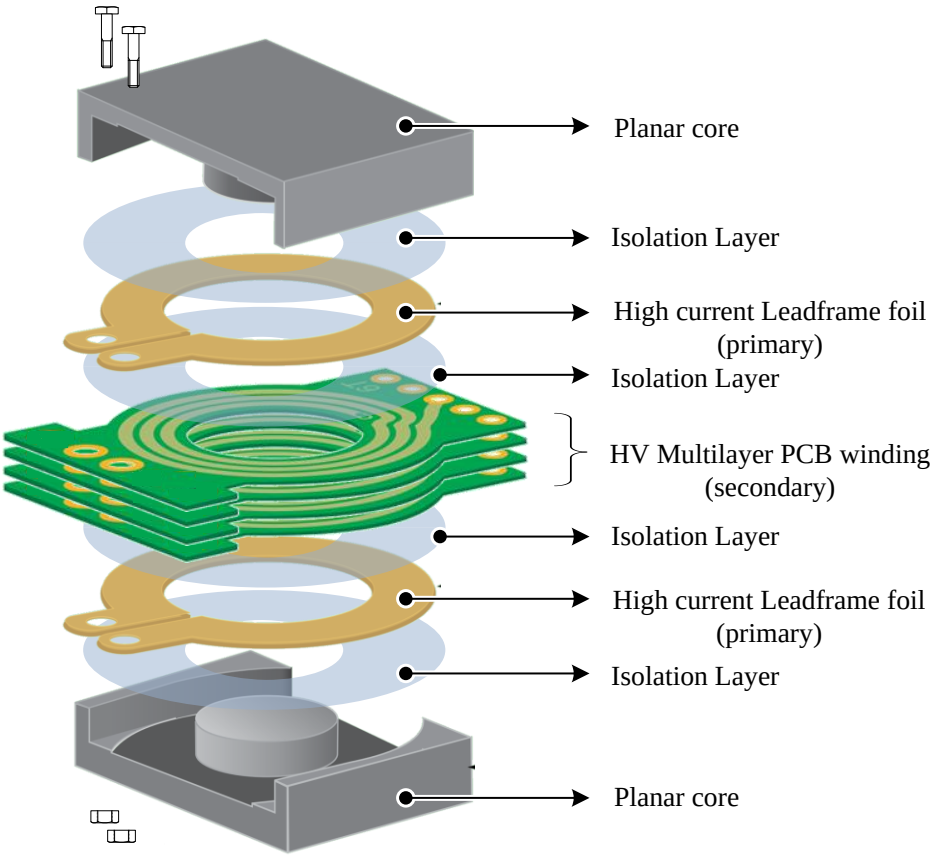


Fig. 5.5 Exploded view of a planar transformer structure, where leadframe foils and PCB traces are used as high current and high voltage winding, respectively.

5.2.2 Heat Generation

The core loss and winding loss depend on the flux density and current density of the core and windings, respectively, which are again impacted by the core geometry. Hence, core geometry influences the heat generation of transformers under a given design specification. Based on the core geometry database from the popular magnetic core vender Ferroxcube [5-5], commercial barrel and planar E-cores are compared in terms of core and winding geometry properties, as presented in Fig. 5.6.

Core loss

At the same voltage excitation level and frequency, the same flux area A_c generates the equal core loss density. This can be observed in Steinmetz equation in Eq. (5-1), assuming a uniform flux distribution within cores and sinusoidal voltage excitation:

$$P_c = C_m f_{sw}^a B_{pk}^b V_c = C_m f_{sw}^a \left(\frac{\int_0^{t_{ex}} v(t)\,dt}{2NA_c} \right)^b V_c \tag{5-1}$$

where N is the number of turns, C_m, a, and b are so-called Steinmetz parameters [5-6] related to magnetic materials, V_c is core volume, $v(t)$ is the transformer terminal voltage in the excitation time t_{ex}. t_{ex} of DAB rectangular modulation is half the switching period:

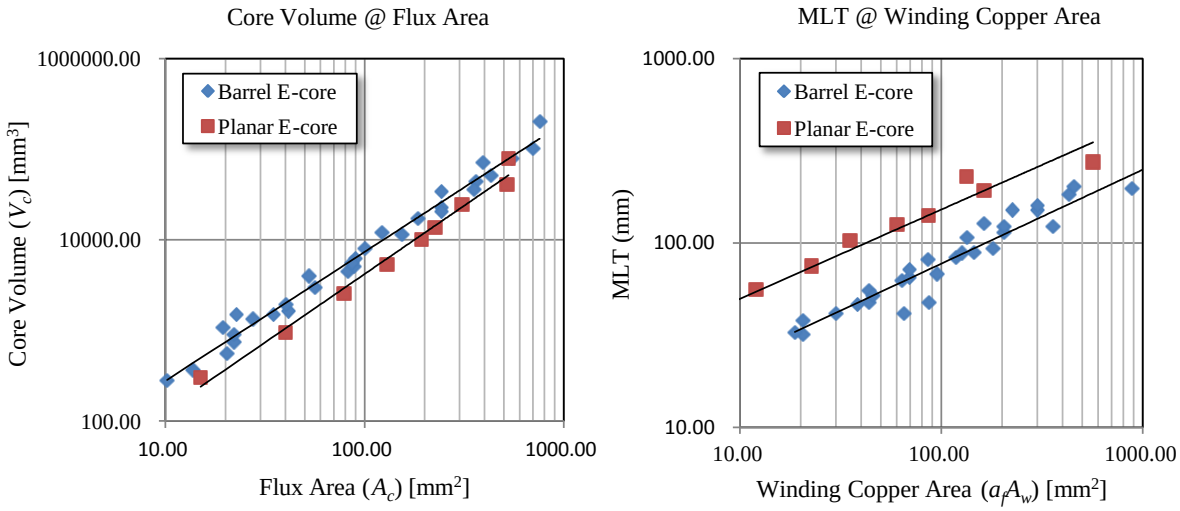


Fig. 5.6 The core volume V_c (a) and Mean Length per Turn (MLT) (b) related to flux area A_c and winding copper area A_{cu} for barrel and planar E cores (Data extracted from Ferroxcube database)

$$t_{ex\_rec} = \frac{T_{sw}}{2} \tag{5-2}$$

The excitation time t_{ex} of trapezoidal and triangular modulations is

$$t_{ex\_trap} = t_{ex\_tri} = \frac{\theta_1 + \theta_2}{2\pi} \cdot T_{sw} \tag{5-3}$$

where θ_1, θ_2 of trapezoidal and triangular modulations are defined in Eq. (3-16) and Eq. (3-28), respectively. It can be concluded from Eq. (5-1) that a larger core volume V_c implies a bigger core loss. Fig. 5.6(a) shows that with the same flux area, commercial planar E-cores generate less core loss.

Winding loss

Assuming the AC effect is absent, the winding loss can be calculated as:

$$P_w = N \cdot R_t I_{rms}^2 \tag{5-4}$$

where N is the number of turns, R_t is the electrical resistance per turn and I_{rms} is the current RMS value. This can be expressed in more detail:

$$P_w = \frac{N I_{rms}^2}{\sigma} \cdot \frac{MLT}{\alpha_f A_w} \tag{5-5}$$

where MLT is mean length per turn, σ is the electrical conductivity of winding wire, A_w is the winding window area and a_f is the fill factor (the ratio between winding window area and net copper area). Fig. 5.6(b) indicates that barrel E-cores have a shorter MLT than planar E-cores at the same winding copper area, assuming a_f = 0.4 for barrel E-core and a_f = 0.3 for PCB-based planar E-cores [5-6]. Here, note that the fill factor of pure PCB-based windings is gen-

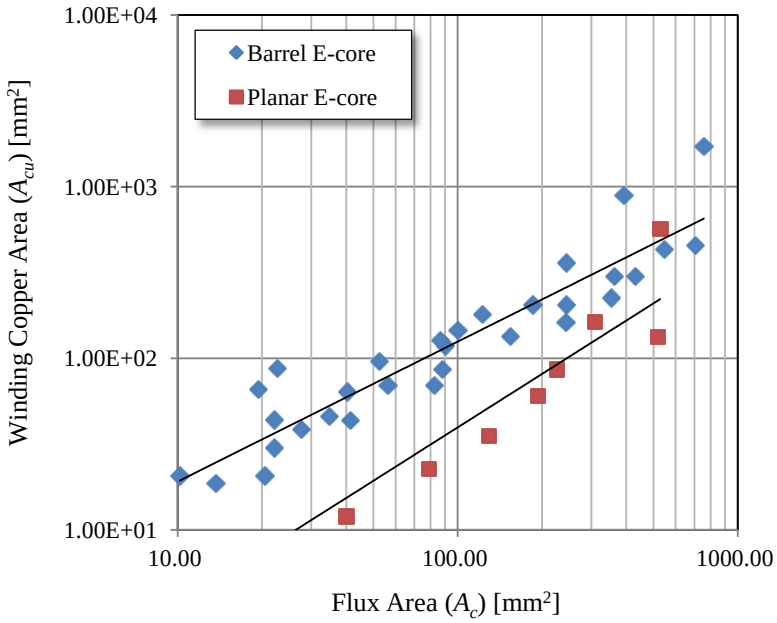


Fig. 5.7 Winding copper area related to core flux area of barrel and planar E cores

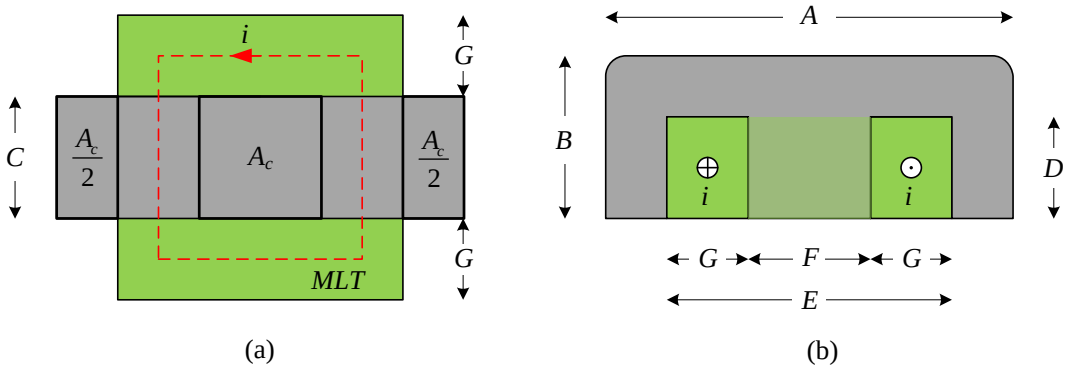


Fig. 5.8 E-core dimensions from (a) core-section view and (b) side view

erally lower than wound wire used in barrel E-core due to PCB lamination material, but this can be improved by combining with other types of windings, like leadframe foils or Litz wires [5-6]. Fig. 5.7 shows that at the same flux area, planar E-core has less winding copper area available. Therefore, it can be concluded that planar E-cores based transformers have generally more winding loss than transformers built with barrel E-cores.

5.2.3 Heat Removal

Cooling surface area

Transformer heat removal capability depends on the cooling surface area. At a constant temperature increase, a larger cooling surface is able to dissipate more power loss, resulting in higher power processing capability and higher power density. Fig. 5.8 illustrates the dimensions of an e-shaped core from the cross-section view (a) and side view (b). The core cooling surface and winding surface area that is extended out of core are defined in TABLE 5.2.

TABLE 5.2 DEFINITION OF CORE AND WINDING COOLING SURFACE AREA BASED ON CORE DIMENSIONS DEFINED IN FIG. 5.8

	Barrel E-core	Planar E-core
Core Surface Area	2ED + 4GD	4EG
Winding Surface Area	AC + 2BC	AC + 2BC

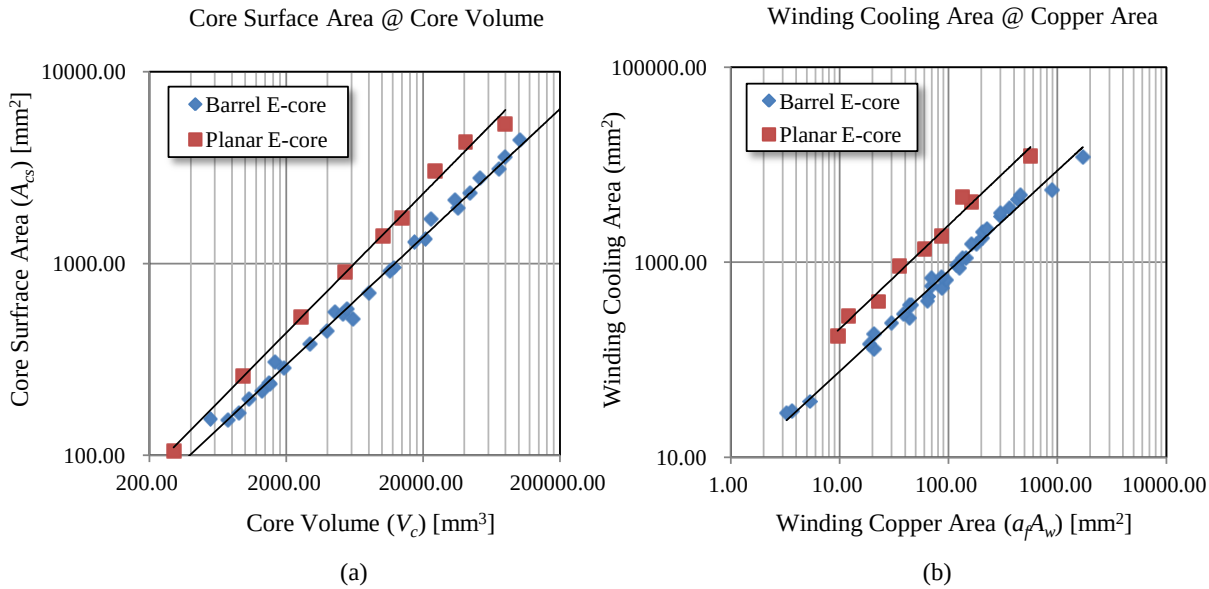


Fig. 5.9 (a) Core cooling surface related to core volume (b) Winding cooling surface related to winding copper area (Data extracted from Ferroxcube database)

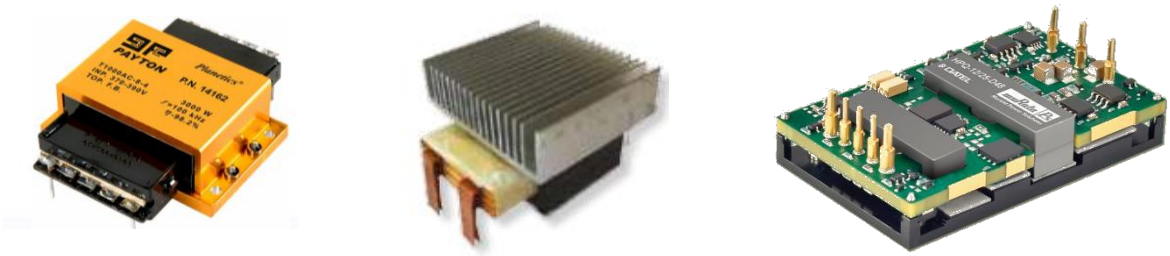


Fig. 5.10 Planar transformers cooled by clamped heatsinks (a) (source [5-9]), (b) and cooling plate (c) (source [5-10])

The cooling surfaces of both commercial barrel and planar E-core are compared in Fig. 5.9(a) according to the database from manufacturer Ferroxcube. The figure shows that at the same core volume, a planar E-core has more cooling surface area than barrel counterparts. Fig. 5.9(b) illustrates at the same copper area, in other words, the same winding current density, planar E-cores have more cooling surface area. In summary, planar transformers are superior in thermal performance.

Cooling Methods

Barrel transformers are usually mounted standalone, cooled by natural or forced convection over its own surface area. Large surface area to volume ratio offered by planar cores makes them ideal for heatsink mounting and forced air-cooling. Fig. 5.10 demonstrates different

mounting methods of planar transformers to other cooling medium. These heat removal methods again improve the thermal performance [5-8] and hence, help to increase the power density of planar transformers.

5.3 Single-Turn Planar Transformer Design

The previous section indicated that commercial planar transformers outperform their barrel counterparts in terms of heat removal and core efficiency, but the winding loss generation is a serious issue. To minimize the transformer loss in high-current applications, transformer design with single-turn high-current winding will be addressed in this section.

5.3.1 Sing-Turn High-Current (HC) Winding

From Eq. (5-1) and Eq. (5-2), it can be found that core loss decreases and winding loss increases as the number of turns (N) rises. The general trends of winding loss, core loss and transformer related to number of turns are described in Fig. 5.11. Therefore, an optimal turns number (N_{opt}) of HC winding should exist to minimize the total transformer losses. Theoretically, the optimal turns number occurs when the absolute derivatives of winding loss and core loss related to N are equal [5-11]. When current rating rises, the winding loss is increased and the optimal turn number decreases. When winding loss overwhelms core loss in HC applications, single-turn HC windings can minimize total transformer losses.

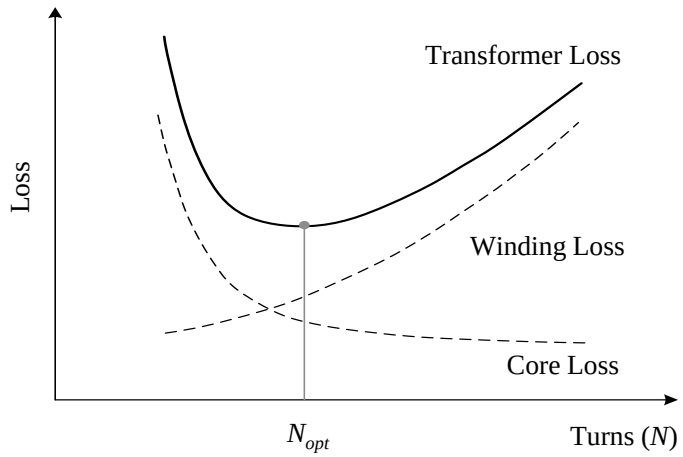


Fig. 5.11 General trends of winding loss, core loss and transformer loss related to number of turns

The operating range in which single-turn HC winding design is more efficient than using multiple-turns is analyzed below. An HC DAB converter is used as the carrier, which is based on rectangular modulation and the planar transformer with EI 64/10/50 ferrite planar cores, a 1:30 turn ratio, and 70 μm thick PCB windings.

Core loss is calculated with Modified Steinmetz Equation (MSE) [5-12] and the winding loss is calculated by assuming a DC current running through the transformer with Eq. (5-5). MSE

involves the changing rate of flux density (dB/dt) into Steinmetz equation so that core loss excited by any arbitrary waveforms can be calculated. MSE is expressed as:

$$P_c = f_{sw} C_m f_{eq}^{a-1} B_{pk}^{b} V_c \tag{5-6}$$

where f_{sw} is the actual switching frequency, f_{eq} is the equivalent frequency defined as follows:

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^{\frac{1}{f_{sw}}} \left(\frac{dB}{dt} \right)^2 dt \tag{5-7}$$

where ΔB is the difference between maximum and minimum flux density (B_{max}, B_{min}), and B_{pk} is half of ΔB. In a DAB converter with rectangular modulation, the excitation voltage to the primary winding is a square voltage waveform with 50% duty ratio. B_{pk} is defined as

$$B_{pk} = \frac{\Delta B}{2} = \frac{\int_0^{\frac{1}{2 f_{sw}}} V dt}{2 N A_c} = \frac{V}{4 N A_c f_{sw}} \tag{5-8}$$

Here, V is the excitation voltage to transformer. dB/dt is defined by:

$$\frac{dB}{dt} = \frac{V}{N A_c} \tag{5-9}$$

Then the core loss calculated by MSE is

$$P_c = f_{sw} C_m \left(\frac{8 f_{sw}}{\pi^2} \right)^{a-1} \left(\frac{V f_{sw}}{4 N A_c} \right)^{b} V_c \tag{5-10}$$

Fig. 5.12 shows how the DAB transformer loss changes with the turns number of high-current windings (N_{HC}) when input voltages (V_{in}) are 12 V and 24 V. It can be observed that when V_{in} = 12 V, the transformer loss is minimum at N_{HC} = 1, when input current is above 60 A and the frequency is above 25 kHz. When V_{in} = 24V, minimal transformer loss occurs with N_{HC} = 1 when the current is above 100 A and the frequency is above 50 kHz. These are the boundaries of single-turn winding design.

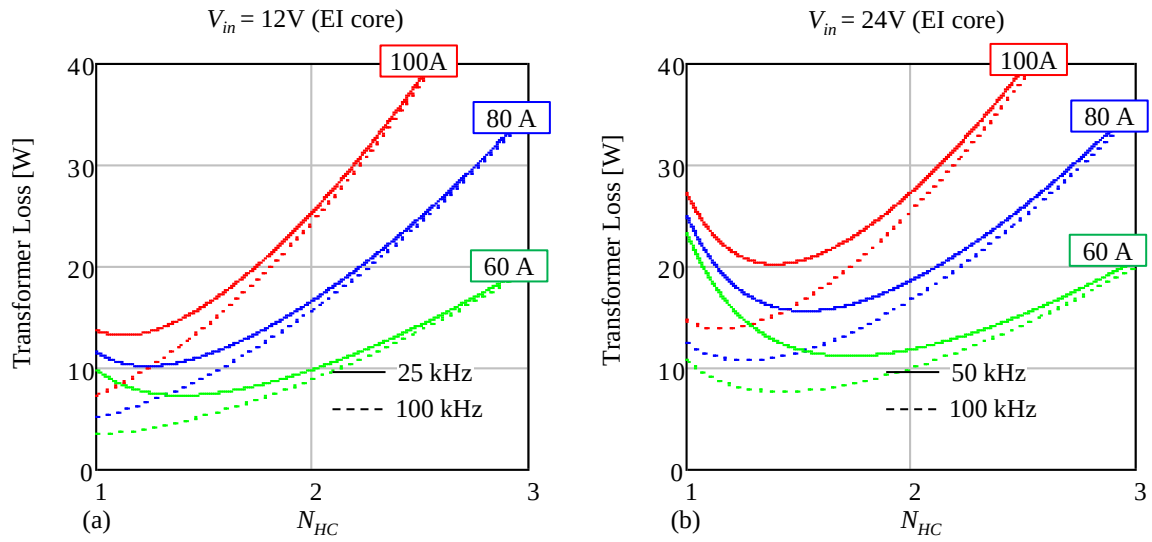


Fig. 5.12 Transformer loss at input current 60 A, 80 A, 100 A with (a) 12 V input voltage, 25 kHz and 100 kHz frequency; (2) 24 V input voltage, 50 kHz and 100 kHz frequency

Note that the calculation done above is only based on DC winding current, and moreover, the resistance of the winding terminations is not included. In reality, AC effect and termination resistance boost the winding losses, which indicates that the single-turn high-current winding design is more justified at the applying boundaries mentioned above.

Optimal turn number < 1

It can be observed in Fig. 5.12 that when current rating continues growing, the optimal turns number will be smaller than one, theoretically. In this case, the winding loss must be reduced to practically reach the minimal transformer loss at a single turn. As indicated by Eq. (5-5), winding loss can be reduced by bigger copper fill factor or wider winding window area. Higher copper fill factor can be realized by deploying different winding types other than PCB traces, such as copper foils or Litz wire. Transformers with various winding types are evaluated in Section 5.3.3. Larger winding window area can be achieved by 1) using a larger standardized core size, 2) custom-designing a special core or 3) using multiple cores in parallel. Another method to reduce winding loss is using the interleaving technique.

5.3.2 Single-Turn Interleaving Techniques

As introduced in Chapter 2, the AC effect (skin effect and proximity effect) will push the current into certain copper area and increase winding loss. This also justifies that single-turn HC winding is necessary in high-current transformer design for increased efficiency, since single-turn is to alleviate the winding loss.

Interleaving the windings can reduce the winding loss caused by AC effect. "Interleaving" denotes that turns of primary and secondary windings are stacked alternatively in space. The result is that the winding window area is divided into multiple sections and the boundary between each section is defined by the point where the total magnetic field intensity becomes zero. Fig. 5.13 shows primary and secondary foil windings segmented into 1 (non-interleaved), 2, 3 sections (n_{sc} = 1, 2, 3) and according magnetic field intensity distribution. An important finding here is that a larger n_{sc} reduces the field intensity.

The winding loss calculation in such an interleaved structure is derived in Appendix A. To explain the loss-reducing effect of the interleaving technique, the ratio between winding AC and DC resistances is re-written below:

$$F_{AC} = \frac{R_{AC}}{R_{DC}} = \frac{\nu}{6}\left[\frac{\sinh\nu - \sin\nu}{\cosh\nu + \cos\nu} N\left(4M^2 - 1\right) + 3\frac{\sinh\nu + \sin\nu}{\cosh\nu - \cos\nu}\right] \tag{5-11}$$

where N is the turns number per layer and M is the number of layers in each winding section. The ratio between the thickness of a layer and the skin depth is represented by ν:

$$\nu = \frac{h}{\delta} \tag{5-12}$$

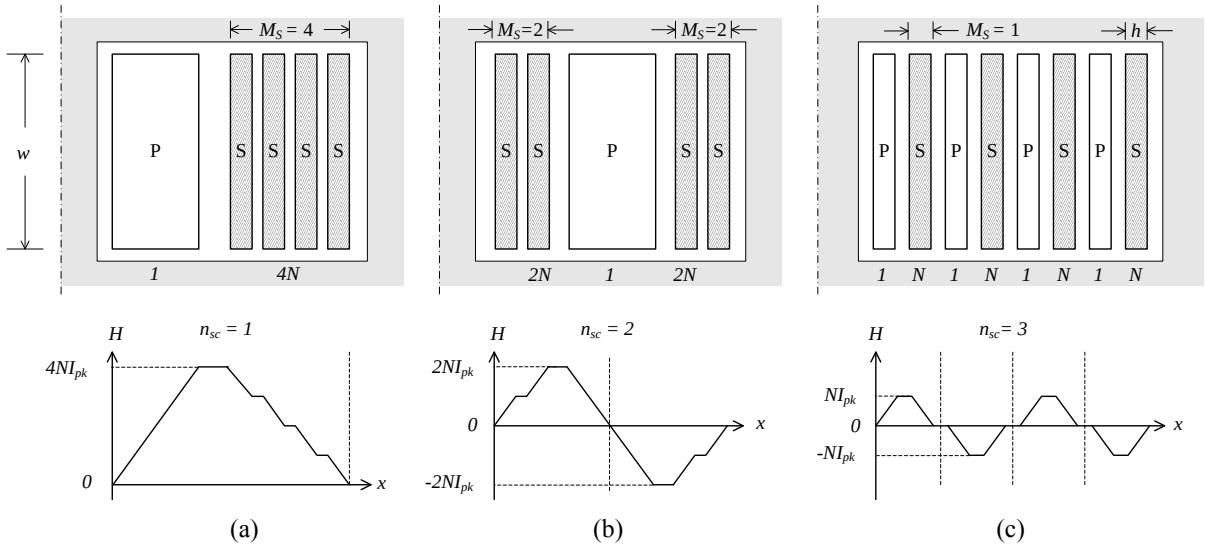


Fig. 5.13 Winding window area, where the primary (P) and secondary (S) windings are interleaved into 1,2,3 sections (a,b,c). The field intensity at each section border is zero.

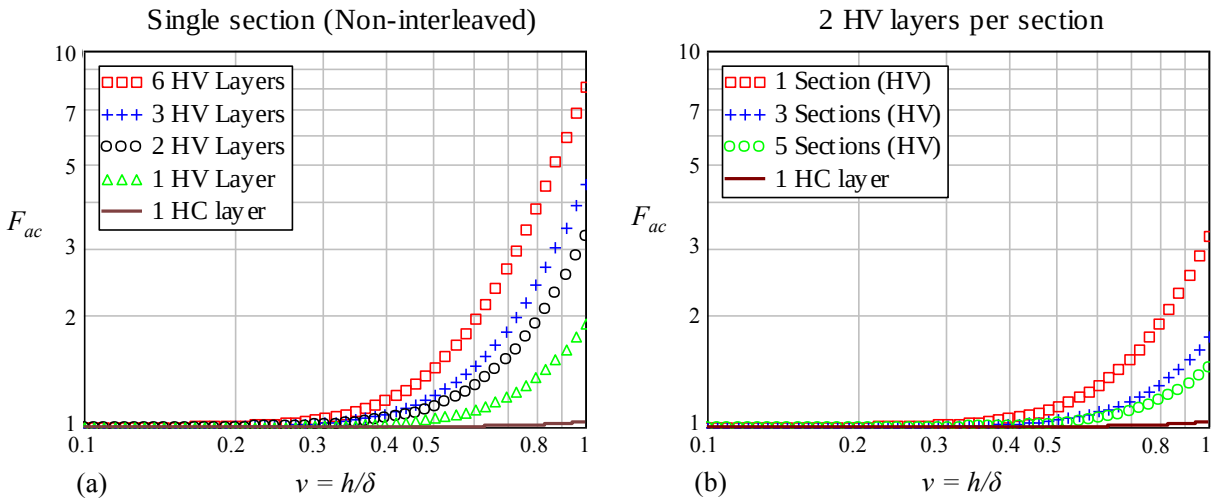


Fig. 5.14 (a) F_{ac} of one winding section (non-interleaved structure) with different layers of HV windings (b) F_{ac} of interleaved winding structure with 2 HV layers of each winding section. (Single-turn HC winding, and 30 turns HV windings that evenly distributed in each layer)

Based on Eq. (5-11), F_{ac} is plotted in Fig. 5.14, for a planar transformer consisting of a single-turn HC foil winding and 30 turns HV foil winding, where HV turns are evenly allocated to each layer. Fig. 5.14(a) shows the non-interleaved case, where it can be found that

- Smaller v gives less AC resistance in general.
- More layers increase AC resistance.

Fig. 5.14 (b) shows the interleaved case where HV winding has two layers per section and all HC windings are connected in parallel. It can be concluded that more winding sections give less winding AC resistance. However, additional sections also complicate the winding design and terminations.

Reducing magnetic field intensity by interleaving technique results not only in smaller resistance of the transformer windings, but also in smaller leakage inductance because of less

magnetic energy stored [5-13]. In some converter topologies, like flyback, low transformer leakage inductance is desired [5-14]. However, in converters like DAB, a certain inductance value is required to transfer the defined power. If the transformer leakage inductance is employed exclusively as the power transfer inductance, it has to be controlled to a specific value rather than aiming for the smallest possible value.

5.3.3 Evaluation of Three Single-Turn Transformers

This section evaluates and compares three single-turn high-current transformers. The transformers are designed for a 12V~350V DAB converter, with a power rating of 1 kW, designed with the rectangular modulation method. The aim is to illustrate how to reduce winding loss and how to control the leakage inductance of planar transformers. In addition, via the comparison between the planar and barrel transformer designs, the benefits of planar transformers are highlighted.

Converter Prototype Structure

The DAB converter prototype consists of three parts: LV-side PCB, HV-side PCB, and a high-frequency transformer placed in between the two. Fig. 5.15 illustrates such a converter structure. On the LV-side PCB, two MOSFET modules (SK300MAA055T) are employed, with each module used for one switch leg and with three MOSFET dies (SUM110N06-04L) in parallel at each switch position. On the HV-side PCB, one IGBT module (SK80MD055 module with SK80MD055IGBT dies packaged inside) is employed for the HV switch bridge. Electrolytic capacitors are used as both input and output capacitors. Control circuitry is placed on a separate board and microcontroller PIC18F4331 is used.

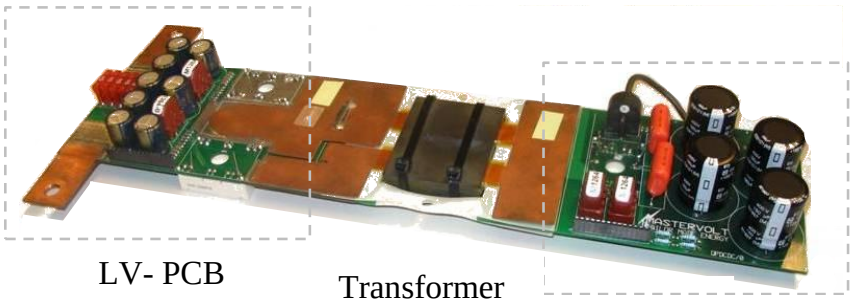


Fig. 5.15 Structure of a 1 kW DAB converter prototype

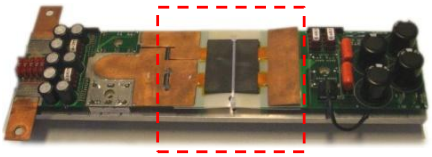
Transformer Structures

Three single-turn high-current transformer prototypes have been developed, two planar transformers and one barrel transformer. Photos of these three transformers are shown in Fig. 5.16. The structure details of these three transformers are described in TABLE 5.3, where highlights are:

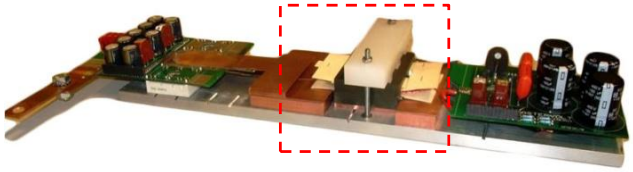
- All transformer cores are 3C90 ferrite and the turns ratio is 1:30.
- The primary windings (HC winding) of all three transformers are made of copper foils to enlarge the current flowing area and keep winding loss low.

TABLE 5.3 STRUCTURE DETAILS OF THREE TRANSFORMER CONCEPTS

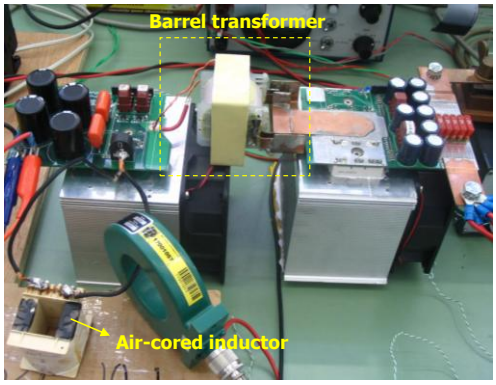
3C90 material 1:30 Turns Ratio	Planar Transformer I	Planar Transformer II	Barrel Transform-er
Core Set	Planar E/PLT 64/10/50	Planar EE64/10/50	EE 65/32/27
Primary winding (HC)	0.5 mm thick/15mm wide copper foil	1 mm thick /18mm wide copper foil	1 mm thick/30 mm wide copper foil
Secondary wind-ing (HV) structure	70 µm /3mm PCB traces placed in 8 lay-ers	0.2mm / 25 strands Litz wire placed in 2 layers	0.2mm/25 strands Litz placed in 2 layers
No. of interleaved Sections	2	Not interleaved	2
Leakage induct-ance (from HV side)	10 µH	76.4 µH	24 µH
Integrated leakage layer?	No	Yes	No
External inductor?	Yes	No	Yes



(a) Planar Transformer I – Copper Foil (HC)+ PCB winding (HV)



(b) Planar Transformer II – Copper Foil (HC) + Litz wire winding (HV)



(c) Barrel Transformer – Copper Foil (HC) + Litz wire winding (HV)

Fig. 5.16 Pictures of three developed transformers (a) Planar Transformer I (b) Planar Transformer II (c) Barrel Transformer

- The secondary winding of planar transformer I is made of 70 µm PCB traces, while Litz wires (25 strands and 0.2 mm diameter per strand) are used in the other two trans-formers.
- Planar transformer I and the barrel transformer have interleaved winding structures to reduce winding losses (see Fig. 5.17(a, b)). However, their leakage inductances (10 µH and 24 µH, respectively, seen from the secondary side) are too low to be the power transfer inductance alone. This is because 1) an unacceptably-high current peak will

TABLE 5.4 GEOMETRIC DATA OF THREE TRANSFORMERS

Geometric data	Planar Transformer I	Planar Transformer II	Barrel Transformer
Flux area (A_c)	500 mm^2	500 mm^2	540 mm^2
Winding window area (A_w)	111.2 mm^2	222.4 mm^2	537.2 mm^2
Copper area (A_{cu})	22 mm^2	41.6 mm^2	41.6 mm^2
Core volume (V_c)	35500 mm^{3*}	40700 mm^3	79000 mm^3
Core height (H_c)	15.3 mm	20.4 mm	65.6 mm
DC current density in primary winding (J_p)	6.2 A/mm^2	6.2 A/mm^2	3.1 A/mm^2
DC current density in secondary winding (J_p)	14.3 A/mm^2	3.7 A/mm^2	3.7 A/mm^2

* The volume of external air-cored inductor is not included

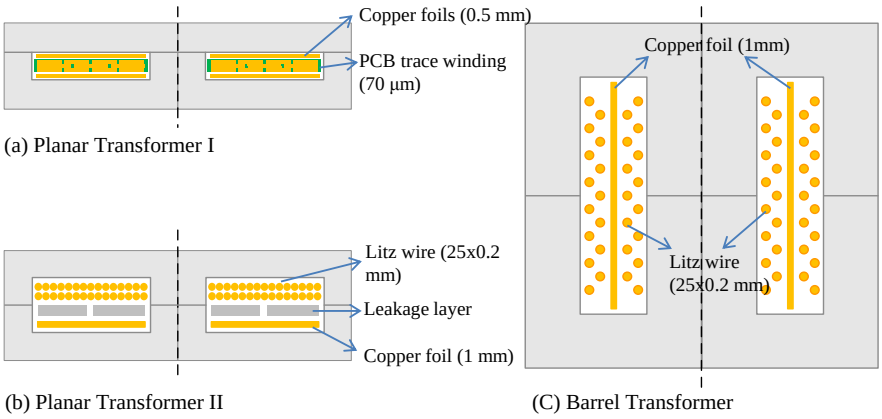


Fig. 5.17 Cross-section view of three transformer designs (a) Planar transformer I, (b) Planar transformer II, (c) Barrel Transformer (Insulation material is omitted here)

occur when the battery voltage drops; 2) the resulted too steep current slopes cannot be caught by the microcontroller with limited PWM phase shift resolution (25 ns). Therefore, external air-cored inductors are connected in series with these two transformers at the HV side (see Fig. 5.16(c)). This implies more converter volume taken and extra loss generated.

- Planar transformer II has a non-interleaved winding structure in order to increase the leakage inductance to a level (76.4 μH) that the converter can operate at without an external inductor. To compensate for the winding loss increased by this non-interleaved structure, it employs double planar E-cores that extend the winding window area, so that the copper foil and Litz wire with larger the copper area than the PCB traces can be accommodated.

- To manipulate the leakage inductance, a leakage layer consisting of some ferrite plates can be placed between two windings in planar transformer II (Fig. 5.17(c)). The principle is that a leakage layer placed inside the winding window enhances the leakage

inductance by increasing the leakage flux in a specific area [5-15]. The leakage inductances are tuned by varying the area through which leakage flux flows.

Performance comparison

Geometric data

The geometric data of three transformers are listed in TABLE 5.4, including winding window area (A_w), copper area (A_{cu}), flux area (A_c), core volume (V_c) and height (H_c), and DC current density in primary and secondary windings (J_p and J_s). Three transformers are built with cores that have similar flux areas and the same ferrite material (3C90), hence, their flux density levels and core loss densities are close. It can be observed from TABLE 5.4 that:

- Planar transformer I has the smallest copper area. This is mainly because of the limited copper fill factor of PCB. The secondary winding, which is made of PCB traces, has a very high DC current density, reaching up to 14.3 A/mm^2 at nominal conditions (12V, 1kW). However, although the magnetic core size and height are also the smallest, the external inductor volume is not taken into account.
- The barrel transformer has the greatest core volume, core height and winding window area. Due to the large winding window area, the copper area can be enlarged with wide copper foil and Litz wire, which results in the smallest current density in both primary and secondary windings compared with the other two transformer designs. Note the core volume here does not include the external inductor required.
- Planar transformer II combines the advantages of planar transformer I and the barrel transformer: not only maintaining quite a low profile (20.4 mm thick) but also extending the winding window/copper area. Additionally, the leakage layer proposed eliminates the need for an external inductor.

The converter efficiency and thermal performance of transformers are evaluated below.

Efficiency and Temperature

The DAB efficiency and transformer temperatures are measured when DAB is operating with rectangular modulation method. The input current is measured through a 1 mΩ sensing resistor and converter efficiency is measured with a PZ4000 power analyzer from Yogokawa. The temperature is measured with type-K thermal couples. The measurement setup is given in Fig. 5.18. It is found that the secondary windings have the highest measured temperature in three transformers (hotspot). The hotspot temperature of three transformers at nominal conditions are compared in Fig. 5.19, together with the according converter efficiency. The efficiency measurement includes the external inductor as well. Here, natural convection cooling is applied and the ambient temperature is 22 ^{o}C.

It can be found that:

- The planar transformer I has the highest secondary winding temperature, soaring up to 124 ^{o}C, more than 100 ^{o}C above the ambient temperature. This is a temperature that will significantly speed up the failure of PCB substrate and any insulation material,

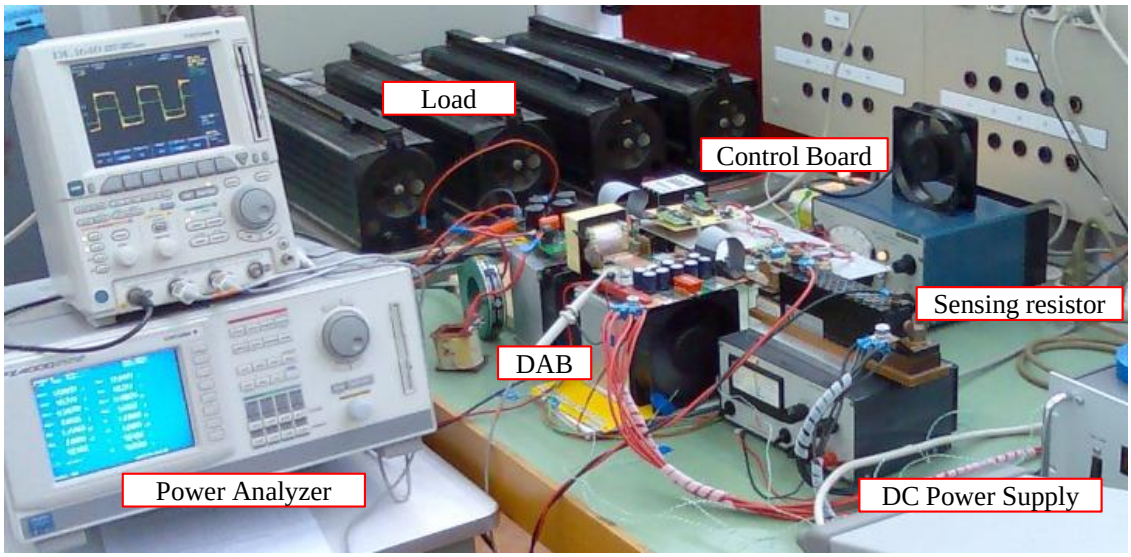


Fig. 5.18 Setup of DAB efficiency and transformer temperature measurements

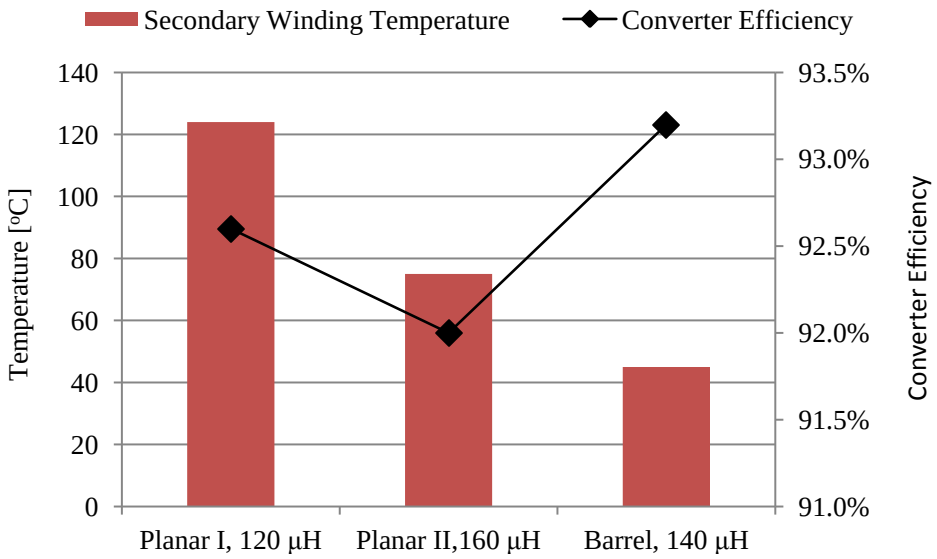


Fig. 5.19 The secondary winding temperature and converter efficiency at three different transformers

will possibly saturate the magnetic cores and even worse, cause thermal runaway of PCB windings at ambient temperature rise. The reasons include 1) too high current density in PCB traces; 2) the winding hotspot is buried deep in the magnetic cores and the thermal resistance to ambient is driven high.

- Planar transformer II has a lower winding temperature than planar transformer I, due to the larger winding copper area as a result of employing bigger winding window area and Litz wire with higher fill factor. Due to the leakage layer inserted between windings, the leakage inductance can be tuned in an integrated manner. Due to the absence of the external inductor, the power density of planar transformer II is higher than that of the other two transformers. However, bigger core volume, non-interleaved winding structure and inserted leakage layer all increase transformer loss and hence, decrease converter efficiency.

- Although achieving the highest efficiency and lowest winding temperature, the barrel transformer has the biggest volume and height. When the too low winding temperature rise (only 20 ^{o}C over ambient) is considered, this transformer is actually an oversized design.

In conclusion, among the three examined transformer designs, planar transformer II is the best in terms of low structure profile, high power density and integrated leakage tuning.

Modularized converter structure

One of the most prominent benefits of a low-profile transformer structure is that it enables a modularized converter structure. By stacking multiple converter units in parallel, a DAB system with more power can be freely configured in a volume compact manner, as illustrated in Fig. 5.20.

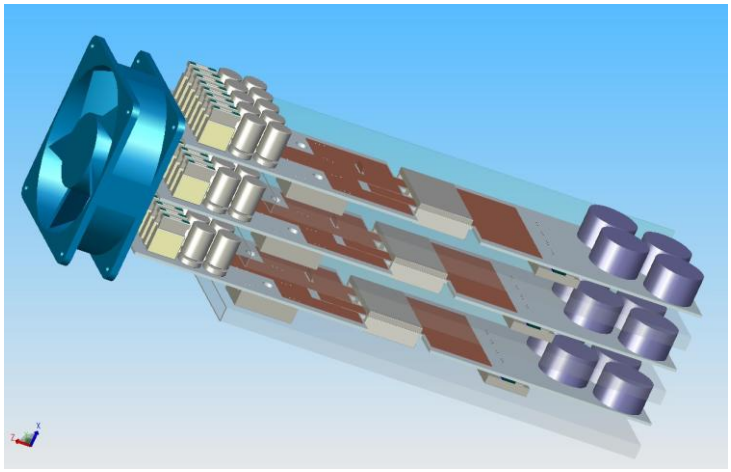
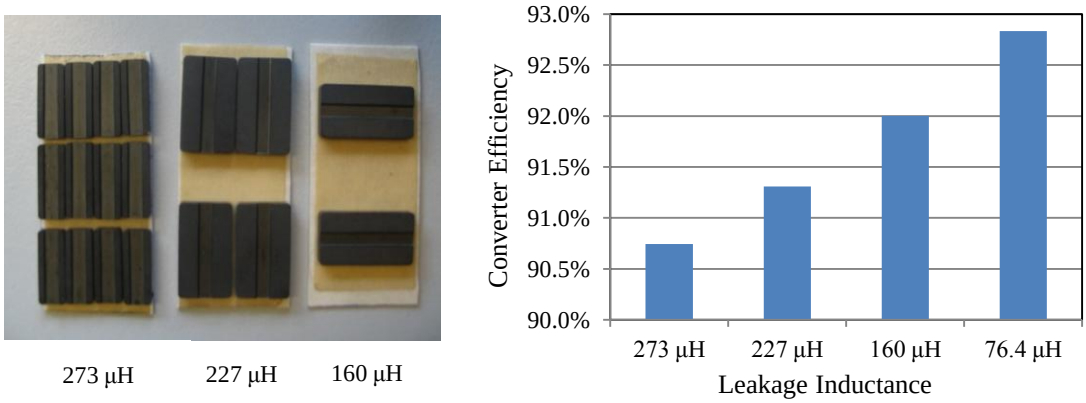


Fig. 5.20 Modularized system structure with three low-profile DAB converters in parallel

5.3.4 Leakage Inductance Tuning

DAB converter requires a specific inductance to transfer power. If the transformer leakage inductance is used as the inductance, an extra inductor is not needed and the power density of DAB converter can increase. Planar transformer II is equipped with an ability to tune the leakage inductance in an integrated way. To tune its leakage inductance, a leakage layer consisting of multiple thin ferrite plates is placed between the primary and the secondary windings of planar transformer II, as illustrated in Fig. 5.17(b). The cross-section area of the leakage layer and distances between ferrite plates can be changed to tune the leakage inductance. Three ferrite plate configurations (Fig. 5.21(a)) provide leakage inductance of 273 μH, 227 μH and 160 μH, respectively, measured in experiments. The converter efficiencies with different leakage inductances are measured and shown in (Fig. 5.21(b)), where 76.4 μH indicates the case without a leakage layer. The measurement setup is described in Fig. 5.18. It can be observed that higher leakage inductance results in lower converter efficiency. The reasons include:



(a) (b)

Fig. 5.21 Three different ferrite plates configurations; (b) Converter efficiency at planar transformer II with different leakage inductances

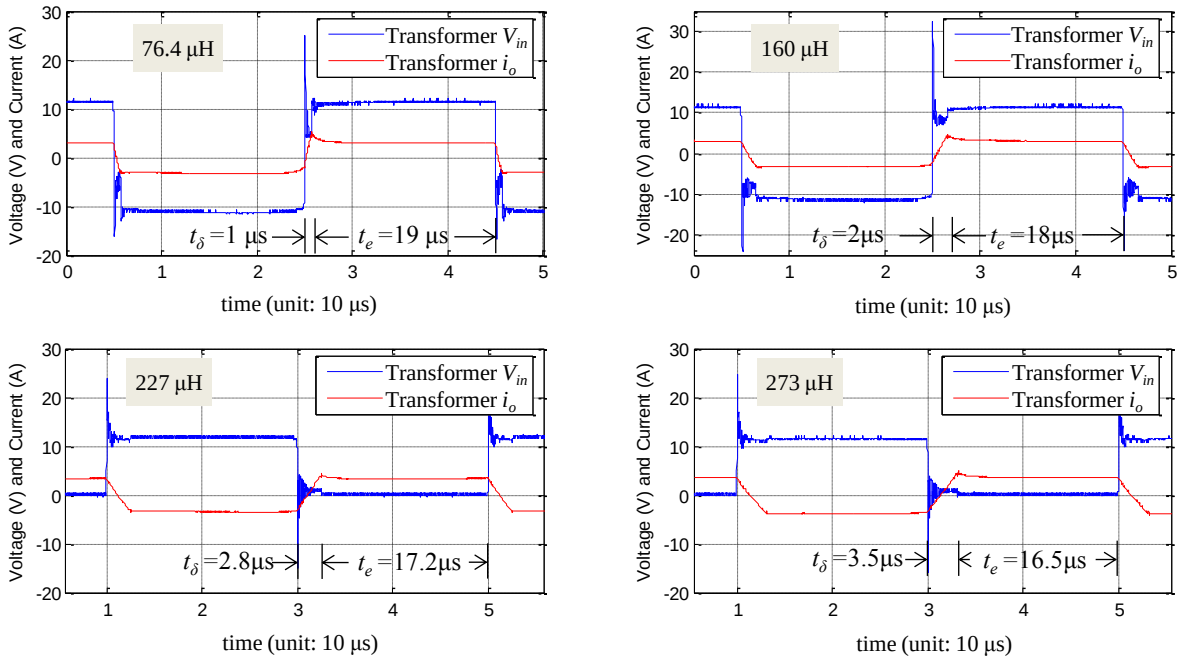


Fig. 5.22 Measured transformer input voltage and output current waveforms at four different leakage inductances

- Loss is generated in the ferrite plates;
- As explained in Chapter 3, to deliver the same power to load, a higher power transfer inductance causes more circulating current (hence a higher RMS current value) in the DAB converter, so more conduction loss in power semiconductors and transformer windings. Fig. 5.22 shows the measured transformer input voltage and output current waveforms at four leakage inductances in nominal condition (12 V, 1 kW). It can be observed that the phase shift time (t_δ) is higher with bigger leakage, also indicating more circulating current. Additionally, the effective time (t_e) to transfer the power to load (half switching period - t_δ) is smaller at higher leakage. With the same load delivered, the current magnitude in the effective time has to be higher, resulting in even more winding loss.

- Owing to the absence of a leakage layer, the 76.4 μH case generates the smallest loss. However, the peak current will be high when the input/output voltage ratio deviates far away from the transformer turns ratio under rectangular modulation, resulting in a high conduction loss. This drawback of lower leakage inductance can be solved by employing trapezoidal and triangular modulation methods, which has been explained in Chapter 4.

Actually, this integrated leakage layer can also be inserted into the interleaved structure. Since the interleaved winding structure reduces winding loss, it will offset the increased loss caused by the leakage layer.

5.3.5 Summary

- In LV HC transformer design with commercial planar cores, it is proved that a single-turn HC winding can minimize the transformer loss. The boundary of using a single-turn HC winding has been analyzed for a DAB converter with 1 kW power rating.
- PCB windings have a relatively low copper fill factor, resulting in relatively high winding loss and temperature. The current density of HV winding in the planar transformer I reaches 14.3 A/mm^2, causing serious thermal problem. This raises the question of what the current-carrying capacity of PCB traces should be. This problem will be investigated in Section 5.5.
- A big copper cross-section area helps to reduce the winding loss. To achieve that, either winding window area or the fill factor should be increased. In planar transformer II, EE core set instead of an EI core set doubles the winding window area, and the employed Litz wire boosts the copper area significantly to a higher value than the 70 μH thick PCB traces used in planar transformer I.
- If a specific high leakage inductance is required, the solutions integrated inside the transformer, like a non-interleaved winding structure and an integrated leakage layer, are proved effective.

5.4 Nanocrystalline Planar Transformer Design Optimization

The previous section has illustrated that a single-turn design is needed for low-voltage high-current (>90A) planar transformer based on commercial ferrite planar cores. However, when the current rating reaches several hundred amperes (with an example given in Table 5.1), the LV planar transformer design based on standard ferrite cores is rarely found in literature and manufacturers' databases. One reason is that the limited ferrite planar core dimensions cannot handle such a high current from perspective of heat generation and removal.

Recently, the potential to push the transformer power density higher has been demonstrated in nanocrystalline magnetic materials, due to their lower loss density, higher saturation level, higher operation temperature and higher thermal conductivity than their ferrite counterparts

[5-16][5-17][5-18]. In addition, the dimensions of nanocrystalline transformers are custom-designed, which opens opportunities for core design optimization according to given converter specifications. These appealing characteristics prompt an investigation of the low-voltage high-current planar transformer design based on this nanocrystalline material. The proposed nanocrystalline planar transformer will be designed for a DAB converter with a load profile as shown in Fig. 5.2. The major operation specifications are listed in TABLE 5.1. The maximum current in the circuit occurs with V_i = 20 V, V_o = 360 V, and a 10 kW load.

The design strategy is to maximize the converter efficiency for the steady state and guarantee that the electrical and thermal stresses over all electronic components during transient states are maintained within component specifications.

5.4.1 Ferrite vs Nanocrystalline Cores

Nanocrystalline soft magnetic material is a rapidly quenched iron-based alloy with a fine crystalline micro-structure, with a typical grain size about only 10 nm [5-19]. The nanocrystalline material FT-3M and the ferrite material 3C90, are compared in TABLE 5.5 in terms of saturation flux density, Curie temperature, relative permeability, densi-

TABLE 5.5 COMPARISONS OF NANOCRYSTALLINE (FT-3M) AND FERRITE (3C90) MATERIALS

Properties	**FT-3M**	**3C90**
Saturation flux density B_s [T] @ 20 °C	1.23	0.47
Curie Temperature T_c [°C]	570	220
Relative Permeability μ_r @ 10 kHz	50,000	≈ 2k
Density [g/cm^3]	7.3	4.8
Thermal conductivity σ_{th} [W/m.K]	≈ 9	≈ 4
Electrical resistivity ρ [Ωm]	1.2x10^{-6}	5

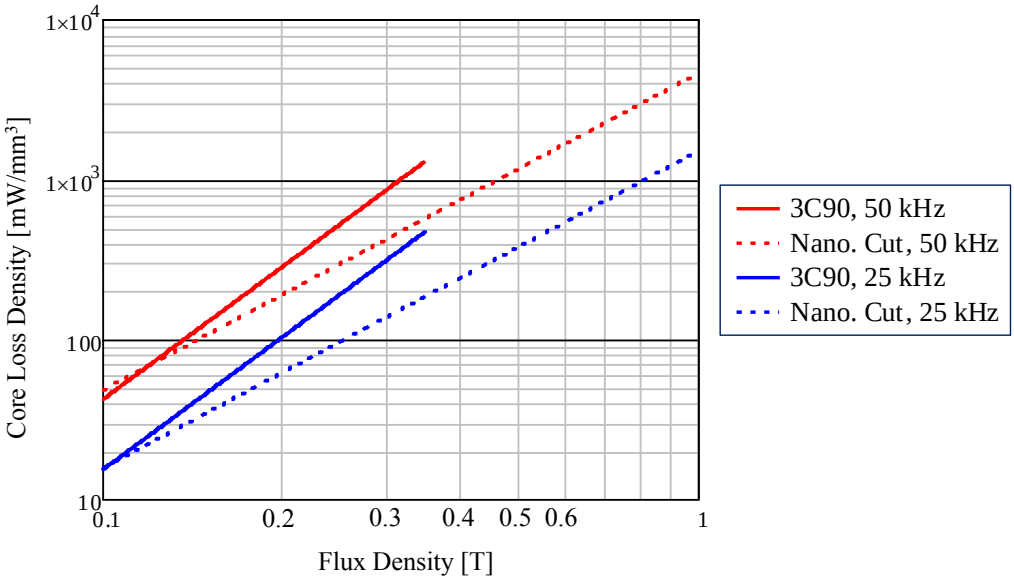


Fig. 5.23 Loss density of 3C90 and FT-3M (cut-core) at 50 kHz and 25 kHz

ty, thermal conductivity, and electrical resistivity. Fig. 5.23 shows the loss density of 3C90 ferrite material and FT-3M cut-core at 25 kHz and 50 kHz. It can be also seen that FT-3M is more efficient than 3C90 at the same flux density. It can be concluded that FT-3M is superior thanks to its larger saturation flux density, higher temperature operation ability, and higher thermal conductivity. For cut-cores, like C- and E-shaped cores, the core preparation effect exists. The core preparation effect [5-16] induces loss in the surface where two cores meet each other and this effect deteriorates nanocrystalline core loss.

Ferrite materials, which are of MnZn- or NiZn-based ceramic compounds, can be molded into desired core shapes, due to their high electrical resistivity and resultant low eddy current loss. On the contrary, due to the low electrical resistivity of nanocrystalline materials, nanocrystalline cores are wound from ultra thin ribbon to suppress of the eddy current at high switching frequency. Because of this laminated structure, most nanocrystalline cores are built for robust mechanical strength. However, as manufacturing techniques advance, the nanocrystalline material can be wound with the minimum stacking thickness of 5 mm, which offers an opportunity to consider a planar transformer with nanocrystalline material.

5.4.2 Key Transformer Parameters Selection

The DAB converter to be designed has a high transient/steady power ratio (10 kW Max / 2 kW Nominal). As explained in Chapter 3, rectangular modulation method with a high power transfer capability is employed for transient state. As already stated, trapezoidal and triangular modulation methods are used for high efficiency at steady state, thanks to their low switching loss and lower RMS current value at the same load. Since the maximum power (10 kW) is much greater than that of the DAB converter designed in Section 5.3 (1 kW), the nanocrystalline transformer parameters have to be redesigned.

This section will explain the selection of key nanocrystalline transformer parameters that are related to the single-turn planar transformer design, where the transformer leakage inductance is employed as the power transfer inductance. The key parameters include the switching frequency, leakage inductance and turns ratio of the transformer.

Leakage inductance and switching frequency

The transformer leakage inductance L_{lk} and switching frequency f_{sw} determines the maximum power that DAB can transfer, as defined in Eq. (3-5). The large value for the product of L_{lk} and f_{sw} is required for the maximum load (10 kW) in transient state I shown in Fig. 5.2. The product of L_{lk} and f_{sw} derived from Eq. (3-5) is:

$$f_{sw}L_{lk} = \frac{V_{i\_min}V_o}{8NP_{max}} \tag{5-13}$$

where N is the turns number of the secondary winding, bearing in mind that the primary (high current) winding has a single turn. It can be observed that higher switching frequency results

in lower leakage inductance. Higher switching frequency helps to shrink the size of passive components, but lower leakage inductance introduces high current peaks and *di/dt* at the low current side. High *di/dt* raises the problem of EMI, and a high current peak stresses power semiconductors and generates high conduction loss.

With the rectangular modulation method, the maximal *di/dt* occurring in phase shift interval δ (shown in Fig. 3.7) and maximal input voltage V_{i_max} is defined as:

$$di/dt\Big|_{rec\_max} = \frac{V_{i\_max} + V_o'}{L_{lk}} = \frac{8P_{max} f_{sw}}{V_o} \frac{NV_{i\_max} + V_o}{V_{i\_min}} \tag{5-14}$$

For trapezoidal and triangular modulations, the maximal *di/dt* occurring in interval θ_1 (shown in Fig. 3.10 and Fig. 3.11) is defined as:

$$di/dt\Big|_{trap\_tri\_max} = \frac{V_{i\_max}}{L_{lk}} = \frac{8P_{max} f_{sw}}{V_o} \frac{NV_{i\_max}}{V_{i\_min}} \tag{5-15}$$

The *di/dt* at three different modulation methods and three different numbers of turns of the secondary winding (N = 12, 14, 16), as a function of switching frequency, is plotted in Fig. 5.24. The following can be observed:

- A higher switching frequency results in higher *di/dt*.
- More secondary winding turns increase *di/dt*.
- Trapezoidal and triangular modulation methods reduce *di/dt* by half, compared with rectangular modulation.

As a trade-off between a mild *di/dt* and high power density, a switching frequency of 50 kHz is selected.

A severe current peak should be avoided as well in the transients. The key current points in rectangular modulation waveforms are defined in Eq. (3-9). The maximum current is calculat-

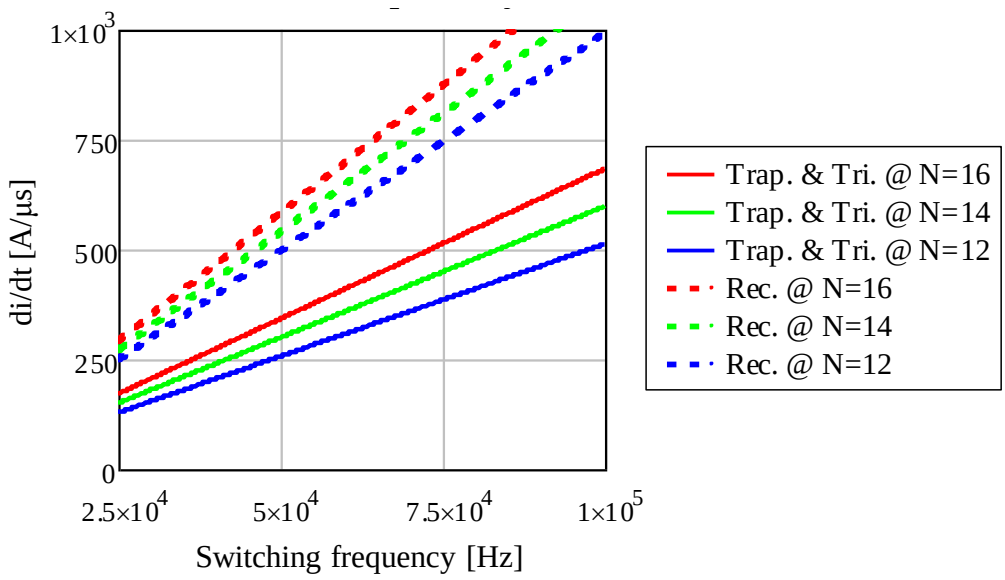


Fig. 5.24 di/dt on the primary side at three different modulation methods and three secondary winding turn numbers, as a function of switching frequency

ed as:

$$i_{pri\_max} = \mathrm{MAX}\left[i_{pri}(0), i_{pri}(\delta) \right] \quad (5\text{-}16)$$

The theoretical peak current at N = 12, 14 and 16 and f_{sw} = 50 kHz is plotted in Fig. 5.25 as a function of leakage inductance. It can be found that

- The maximum leakage inductances required to realize the maximum load at N = 12, 14 and 16 are 17 μH, 20 μH, and 23 μH, respectively.
- The leakage inductance necessary to achieve the minimal peak current at N = 12, 14, 16 is around 15 μH.
- A value of N = 16 generates the lowest peak current than other two winding numbers.

Transformer Turns Ratio (N)

As explained above, single-turn high-current winding minimizes the total transformer loss in high current applications. This section determines the number of HV winding turns N for the DAB to be designed.

First, the influence of turns number on transformer current is investigated. Fig. 5.25 has illustrated that a higher number of secondary winding turns causes lower peak current at transients. Additionally, Fig. 5.26 plots the RMS (a) and peak current value (b) of primary winding at V_o = 360 V and 2 kW load with N = 12, 14 and 16, relating to the entire input voltage range. Current values of three different modulation methods are shown as well. Here, RMS current value is calculated from the waveform built in the loss model proposed in the last chapter, while the peak current of trapezoidal and triangular modulations are calculated in Eq. (3-14) and (3-35), respectively. It can be concluded that:

- N = 16 gives the lowest RMS and peak current values around nominal input voltage 24 V, comparing to N = 12 and 14 and even higher. Lower RMS current value indicates lower conduction loss in the transformer and semiconductors, and smaller peak

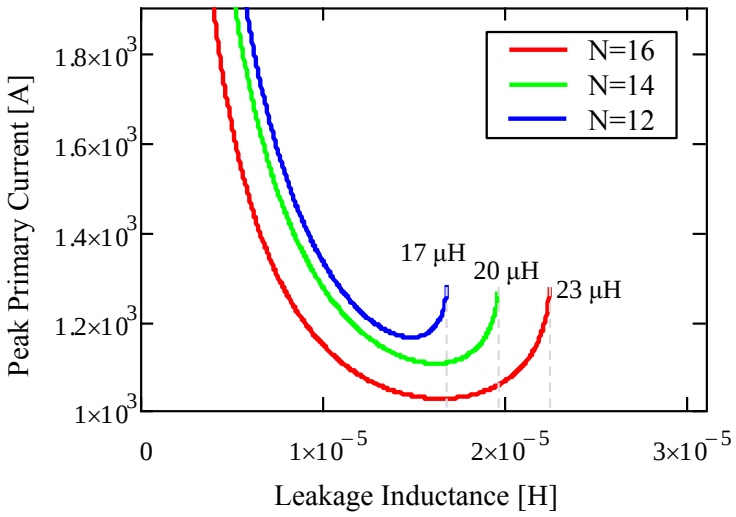


Fig. 5.25 Peak current in primary winding as a function of leakage inductance at three different secondary winding turns number (at 50 kHz)

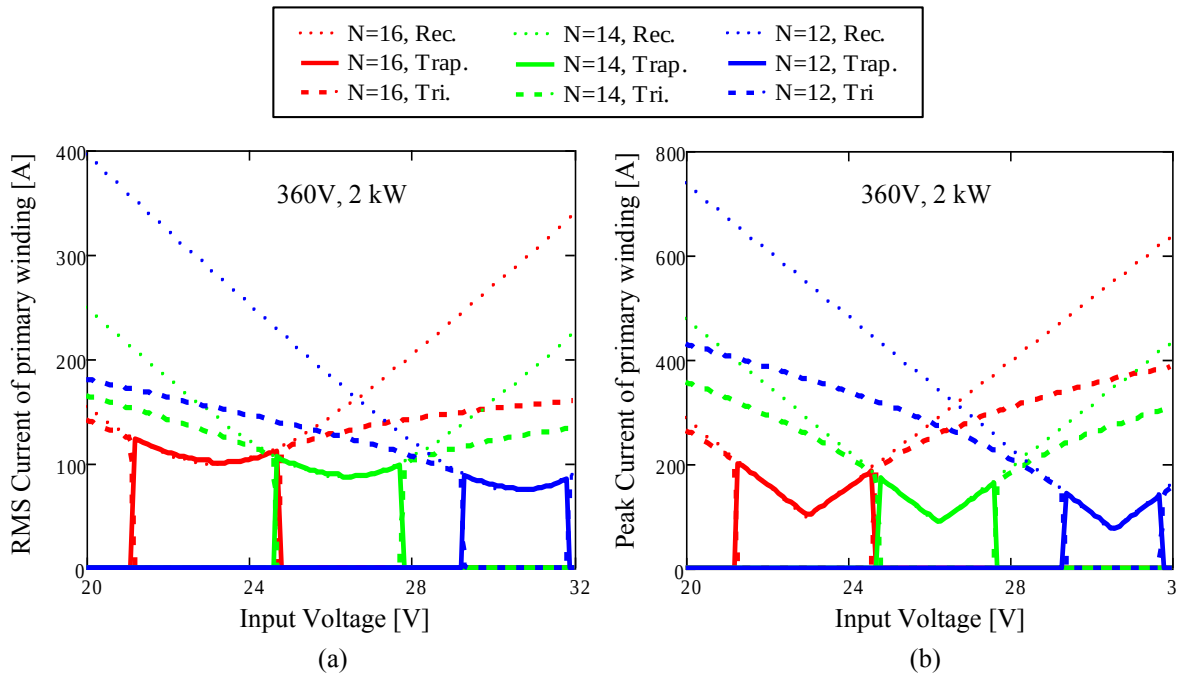


Fig. 5.26 RMS current (a) and peak current (b) of primary winding at 360V, 2 kW as a function of input voltage under rectangular, trapezoidal and triangular modulation methods

current implies released stress on the semiconductors and filtering capacitors.

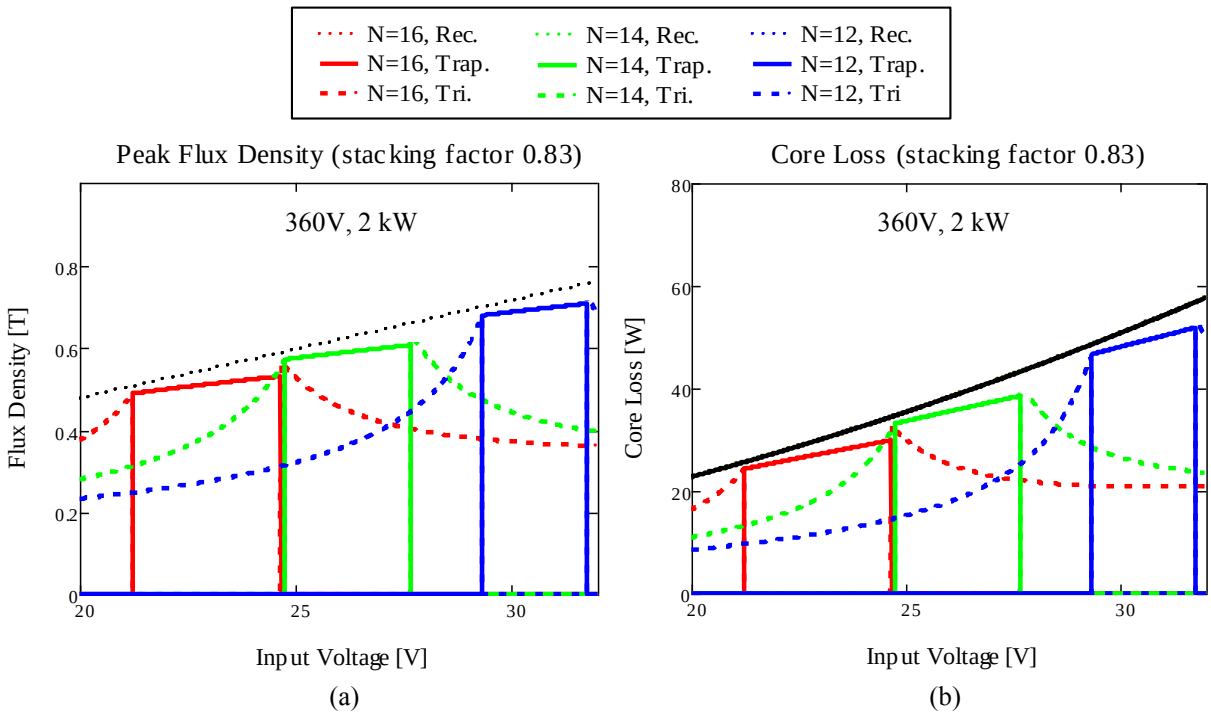
- Here, rectangular and trapezoidal modulations have similar RMS and peak current values around V_i / V_o = 1: N. However, when V_i / V_o deviates far away from 1: N, the peak and RMS current values of rectangular modulation are much bigger than that of triangular modulation. Note the operating range of trapezoidal and triangular methods are complementary (explained in Chapter 3). Hence, the use of trapezoidal and triangular modulations should be combined over the entire operating range.

Second, the influence of turn number N on core loss is analyzed below. Assuming the flux area of the nanocrystalline core is 127 mm^2 and the stacking factor is 0.83 [5-20], the flux density and core loss at N = 12, 14, 16 and three different modulation methods are plotted in Fig. 5.27 relating to the input voltage. It can be observed that:

- Rectangular modulation generates the higher flux density and core loss than the other two modulations. This is because the core excitation time for rectangular modulation is 50% switching period, while it is shorter for other two modulations (defined in Eq. (5-5)).

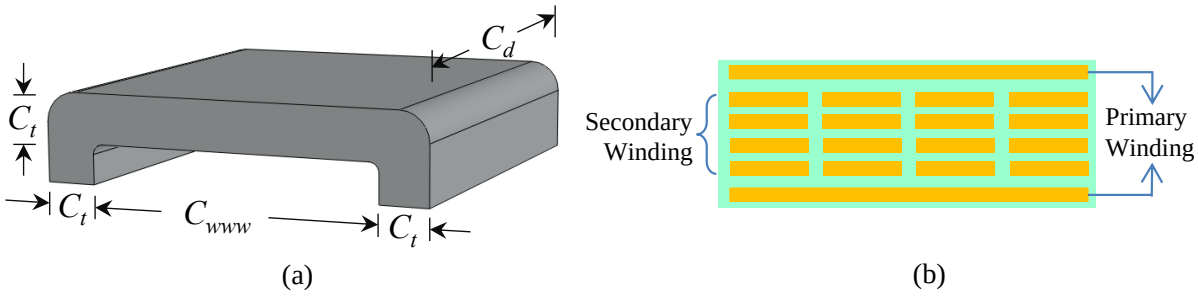
- Triangular modulation has a reduced flux density and core loss when V_i / V_o deviates far away from 1: N.

- N = 12 with triangular modulation generates the least flux density around the nominal input voltage, however, its highest flux density occurring at high end of the input voltage range reaches 0.7 T. Although nanocrystalline core FT-3M will not saturate, a large core loss generated may undermine the applicability of such a high flux density.



(a) (b)

Fig. 5.27 (a) Peak flux density and (b) core loss at 360 V and 2 kW load, at different input voltage and three modulation methods



(a) (b)

Fig. 5.28 Dimensions of C-shaped nanocrystalline cores (b) cross-section view of the PCB winding configuration

- N = 16 with trapezoidal modulation generates the highest flux density around the nominal input voltage. Its flux density at V_i = 24 V is calculated to be 0.52 T, where the loss density of FT-3M is equal to that of 3C90 at 0.35 T and 50 kHz (see Fig. 5.23).

Determination of the turn number of the secondary (HV) winding relies on the overall transformer loss. The turns number (N) that generates the lowest transformer loss at the nominal condition will be selected. It is assumed that 210 μm (6 oz) thick PCB traces are used both as the primary (HC) and secondary windings. All windings are located in 6-layered PCB, where HV windings are evenly allocated into 4 internal layers, and the 2 paralleled HC PCB traces sandwich the HV winding layers on two external layers of the PCB. The PCB winding structure of N = 16 are illustrated in Fig. 5.28(b). The dimensions of the referenced nanocrystalline cores are shown Fig. 5.35. The transformer losses are 360V and 2 kW load are plotted in Fig. 5.29 over the entire input voltage range, with N = 12, 14, 16 respectively. The loss calculation is done using the loss model proposed in Chapter 4.

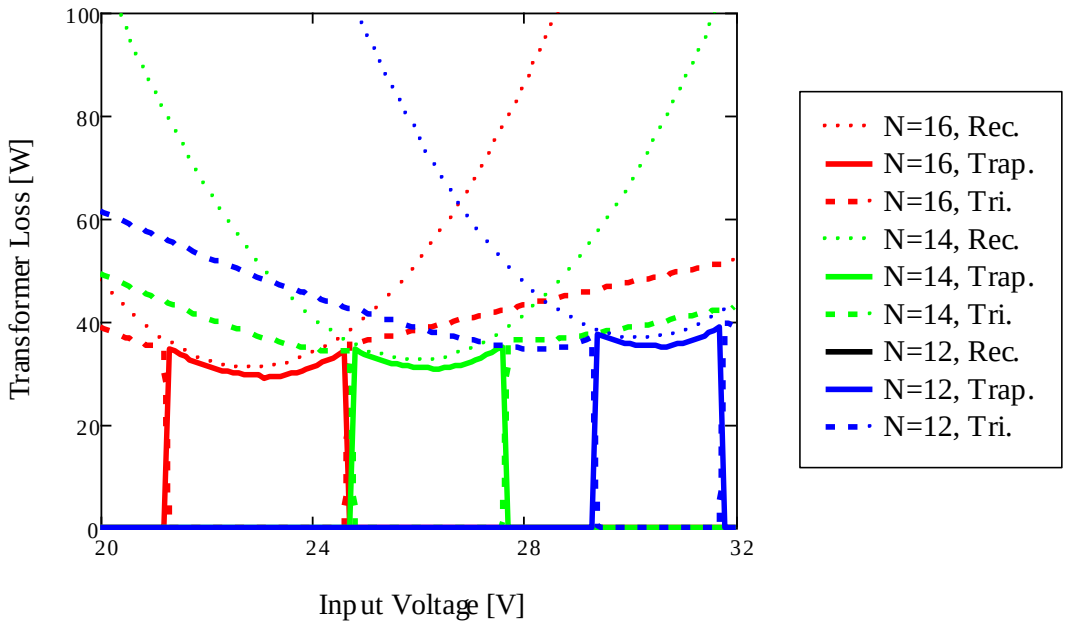


Fig. 5.29 Nanocrystalline transformer loss at 360 V, 2 kW load at varying input voltage and three modulation methods

It can be concluded from Fig. 5.29 that N = 16 with trapezoidal modulation generates the least loss around the nominal input voltage and load. When V_i / V_o far away from 1: N, the triangular modulation is much more efficient than the rectangular one and additionally the current peak is lower. Therefore, N = 16 will be employed in the transformer design, and the combination of trapezoidal and triangular modulation will be employed at steady state. In transient power states, rectangular modulation will be employed.

5.4.3 Optimal Core Dimension Design

The dimensions of all ferrite-based planar magnetic cores have been standardized according to [5-21], which implies that the core shapes are not optimized for low-voltage and high-current applications [5-22]. For optimal performance, a special core has to be custom-designed and manufactured. Since the nanocrystalline core shape and dimensions have not been standardized until now, there is more design freedom to optimize the core dimensions to minimize transformer loss according to the given specifications.

Design boundary

- Due to the special property of nanocrystalline material, low-profile nanocrystalline magnetic core is only available in C-shape. The dimensions of the C-shaped core are shown in Fig. 5.28 (a).
- To guarantee enough mechanical strength, the stacking thickness (C_t shown in Fig. 5.28(a)) of the core is 5 mm minimum specified by core supplier. To realize the thinnest profile, the stacking thickness of the C-shaped core is set at 5 mm.
- Primary (HC) and secondary (HV) windings are integrated in the PCB for a high level of integration. Here, the secondary winding is allocated into 4 layers, with 4 turns per

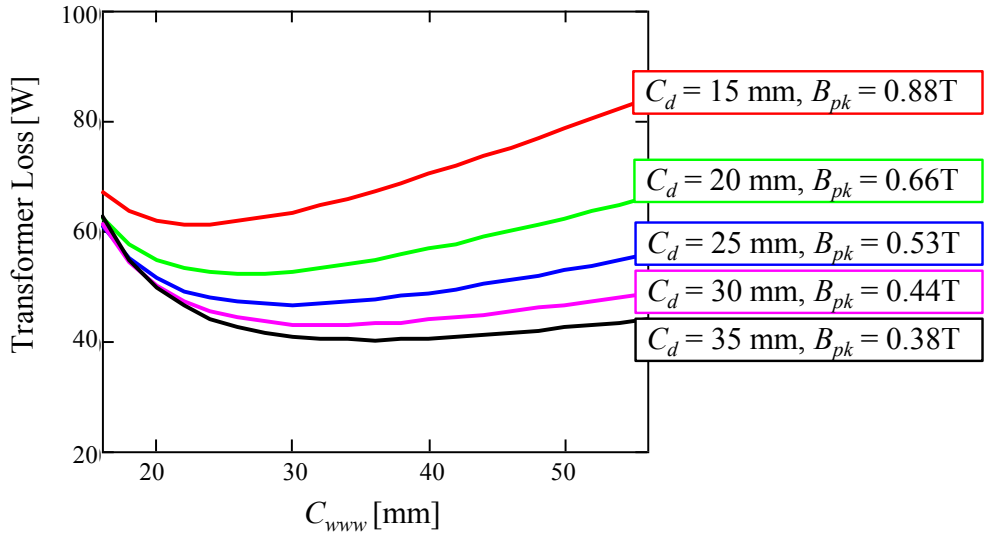


Fig. 5.30 Nanocrystalline transformer loss as a function of C_{www} and C_d at nominal condition (24 V~360 V, 2 kW load) with trapezoidal modulation method

layer. The primary winding has an interleaved structure and two paralleled wide PCB traces sandwich the secondary winding in the middle, as depicted in Fig. 5.28(b). To alleviate the current density in windings, 6 oz (210 μm), PCB trace thickness is selected.

There are two degrees of freedoms left for the design: core depth and core winding window width (C_d and C_{www} in Fig. 5.28a). Bigger C_d decreases flux density and consequently core loss, but also extends the winding conductor length and increases winding loss. Wider C_{www} reduced winding current density and winding loss, however, it also results in a raised core volume and hence higher core loss. Transformer loss as a function of C_{www} is plotted in Fig. 5.30, at different core depths and with the trapezoidal modulation. The operational condition is nominal (24 V~360 V, 2 kW load). The according flux density at different core depths is also denoted on each loss curve. It can be found that:

- There is an optimal C_{www} to obtain a minimal transformer loss for each C_d.
- A longer C_d generally generates a smaller transformer loss, as a result of the lower flux density.

As a tradeoff between power density and efficiency, C_d = 25 mm is selected, which results in a peak flux density 0.52 T at nominal condition. Note that this is a flux level that cannot be provided by ferrite material, indicating a higher power density given by nanocrystalline material. To avoid a high core temperature due to the high core loss density at 0.52 T, a special heat-removal structure is designed. This will be addressed in detail in the next chapter.

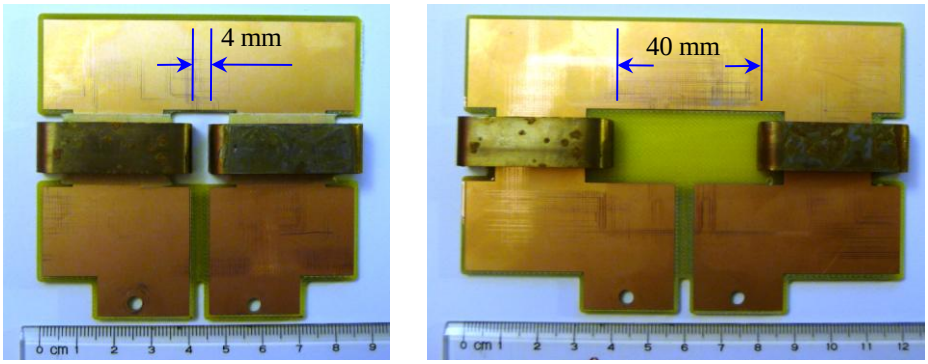
The dimension optimization approach to realizing the minimum transformer loss is applied to ferrite-based transformer design as well. However, the increased manufacturing cost due to the non-standard core shapes needs to be taken into account.

5.4.4 Leakage Inductance Tuning

The required maximum inductance to achieve the required peak transient power is 23 μH, as was derived in the previous section. This is a leakage inductance level that may be realized by manipulating the core and PCB winding structures. The basic principle is to loosen the coupling between windings. In Section 5.3, a leakage layer is inserted between non-interleaved windings to achieve a high leakage. Non-interleaved winding structures also help to raise leakage inductance. However, to keep winding loss low, especially in this high transient load application, interleaved winding structure is maintained for improved efficiency. Another method should be applied to achieve the required leakage inductance. For the C-shaped nanocrystalline transformers with PCB windings, the required leakage inductance is obtained by varying the distance between two C-shaped core sets and the structure of the exposed windings.

Distance between two C core sets

Transformers with C-cores can weaken the winding coupling by setting two core sets apart. Fig. 5.31 shows two nanocrystalline transformers with 4 mm and 40 mm distance between



(a) (b)

Fig. 5.31 Nanocrystalline ransformer prototypes with 4 mm (a) and 40 mm (b) between two C-shaped core sets

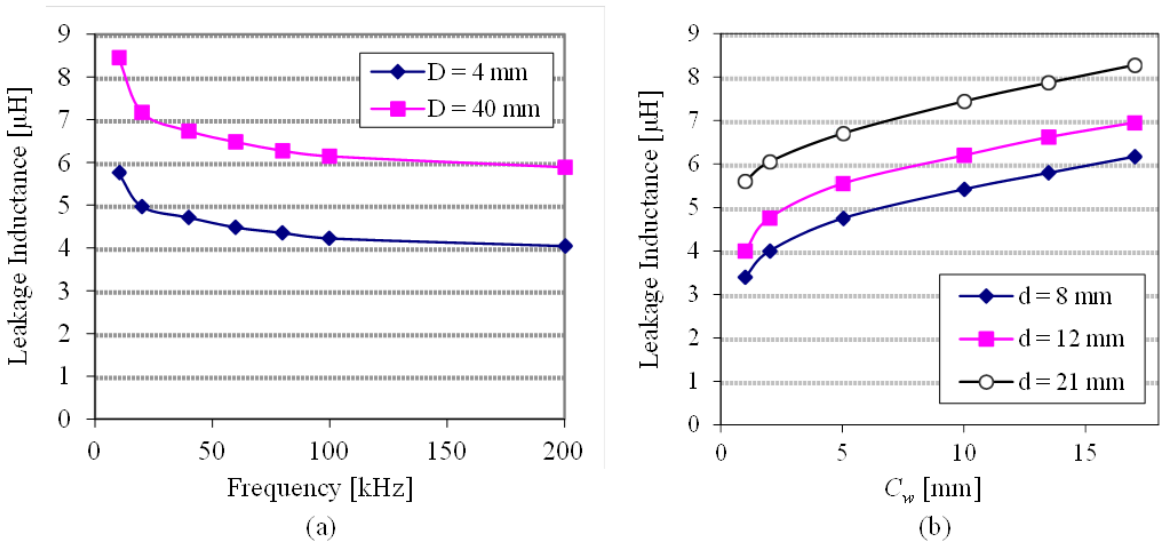


Fig. 5.32 Measured leakage inductance of (a) two C-shaped core sets with 4 mm and 40 mm in between shown in Fig. 5.31; (b) the transformer structure shown in Fig. 5.33(a)

two core sets, where the primary (copper foil) and secondary winding (PCB traces) are located on the top and bottom sides of the PCBs, respectively. Fig. 5.32(a) shows the measured leakage inductances of these two transformers related to switching frequency. It demonstrates that wide separation increases the leakage inductance.

Another benefit of separating C-core sets is that more core surface area is exposed compared with E-cores. This extra area allows more effective cooling of cores. Cooling of planar transformers will be addressed in detail in Chapter 6.

Structure of Exposed Windings

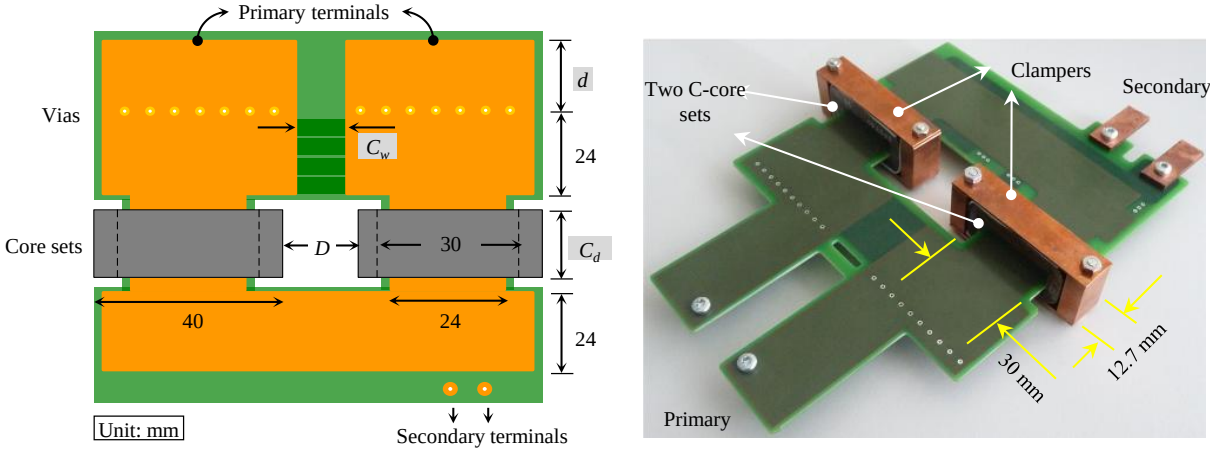
Creating a loosened structure of exposed windings can also increase leakage inductance. Fig. 5.33(a) illustrated a top view of the nanocrystalline transformer design with C-shaped core sets, where C_w is the distance between two primary winding terminals and d is the length of the primary winding that does not cover the secondary winding buried inside the PCB. Fig. 5.32(b) shows the measured leakage inductance related to varying C_w and d, where C_d = 12.7 mm and distance between core sets D = 15 mm. It can be found that larger C_w and d can both boost leakage inductance.

Final Transformer Design

The final transformer design is illustrated in Fig. 5.34. Here C_w = 10 mm, C_d = 25.4 mm, C_{www}=30 mm, D = 15 mm, and d = 35 mm. The measured total transformer leakage inductance is 13.1 μH. Considering the winding terminal stray inductance and semiconductor package inductance, the equivalent leakage inductance is close to 15 μH. In Fig. 5.33(b) and Fig. 5.34, the nanocrystalline cores are clamped with copper bars, for purpose of mechanical support and effective heat removal.

5.4.5 Nanocrystalline vs. Ferrite Transformer Comparisons

This section illustrates the benefits of a nanocrystalline planar transformer, by comparing it on



(a) (b)

Fig. 5.33 (a) Top view of the nanocrystalline transformer with C-shaped core sets (b) a physical prototype

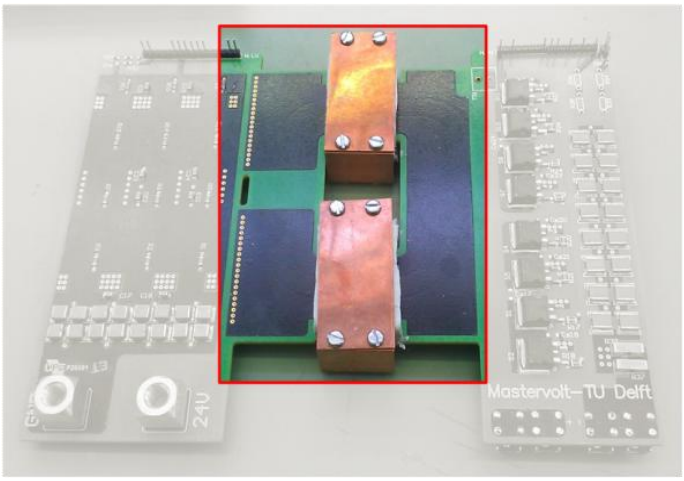
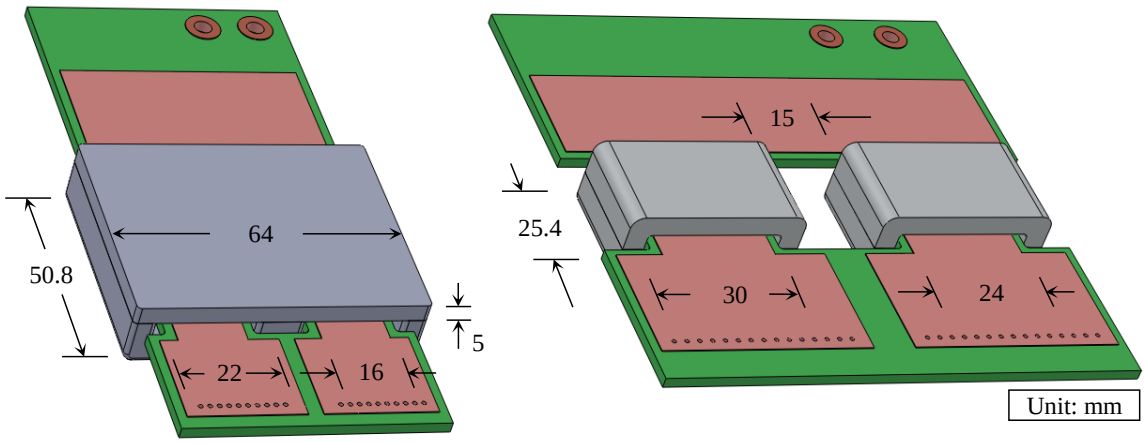


Fig. 5.34 Final nanocrystalline transformer design in a DAB converter prototype



(a) (b)

Fig. 5.35 Dimensions of (a) Ferrite (3C90) transformer with EE64/10/50 core sets and (b) Designed nanocrystalline transformer

a simulation level with a ferrite transformer, both designed for the specifications defined in Table 5.1. Planar EE64/10/50 core sets with 3C90 ferrite material are selected due to their large flux cross-section area and winding window width. The winding structure and PCB trace thickness are the same as that of a nanocrystalline transformer. The core and winding dimensions of the two transformer concepts are illustrated in Fig. 5.35.

The transformer dimensions and loss of the two transformer concepts are compared in TABLE 5.6. It can be found that:

- The nanocrystalline transformer has half the core volume of the ferrite transformer, but the surface area is more than half. This is thanks to the two extra sides resulted from C-shaped core structure. It also indicates the better cooling capability of C-shaped core design.
- The winding loss of nanocrystalline transformer is significantly reduced. This is due to the optimized core winding window width and shortened winding length resulted from a shortened core depth. The lower loss density of the nanocrystalline material and higher saturated flux density enables the shorter core depth.

TABLE 5.6 COMPARISONS OF DESIGNED NANOCRYSTALLINE TRANSFORMERS AND A FERRITE (3C90) TRANSFORMER WITH EE64/10/50 CORE SETS

.

	Transformer Properties and Loss @ 50 kHz	**Ferrite 3C90** EE64/10/50	**Nanocryst. FT-3M** C-Core sets
Core Size Property	Core Surface	88.4 cm^2	61 cm^2
	Core Volume	43 cc	25 cc
Nominal Condition 24V, 360V, 2 kW	Flux density	0.22 T	0.52 T
	Core Loss	13.9 W	29.3 W
	Surface Loss Density /Core	0.16 W/cm^2	0.48 W/cm^2
	Volume Loss Density /Core	0.32 W/ cm^3	1.17 W/cm^3
	Copper Loss	30.5 W	16.9 W
	Total Loss	48.9 W	46.2 W
Worst Condition 20V, 360V, 10 kW	Flux density @ worst condition	0.2 T	0.47 T
	Core Loss @ worst condition	22.2 W	23.1 W
	Copper Loss @ worst condition	1903 W	1043 W
	Total Loss @ worst condition	1925 W	1066 W

- In the worst condition (20V~360V, 10 kW load), the RMS current value of the converter reaches the its maximum. The nanocrystalline transformer generates about 800 W less winding loss than the ferrite transformer, which significantly relaxes the thermal problems of PCB windings. This also implies the much greater peak power processing capacity of this nanocrystalline transformer designed for transient high-current application.
- The nanocrystalline transformer has almost twice the core loss of the ferrite design, due to the high flux density to realize a high power density. To keep the hotspot temperature rise low enough, much cooling effort is required. Due to the higher surface/volume ratio caused by C-shaped cores and higher thermal conductivity of FT-3M material than that of 3C90, heat removal management is intrinsically easier in nanocrystalline transformers. The cooling design will be addressed in Chapter 6.

Moreover, the ferrite planar E-core transformers have a compact winding structure, which means special treatments are required to boost the leakage inductance to required level. These treatments, such as an external inductor, non-interleaved winding structure or integrated leakage layer as mentioned beforehand, introduce extra loss and volume as a side effect.

Summary

The prominent benefits of the designed nanocrystalline transformer are summarized below:

- High power density designed for high-current application.
- Increased effective cooling surface due to the C-shaped core design.
- Freedom to tune the leakage inductance by manipulating the core distance and winding structures.

5.5 Thermal Design Guideline of PCB Traces under DC & AC Current

The thermal issue of PCB winding in planar transformer I as introduced in Section 5.3 triggers a question: what is the PCB trace Current Carrying Capacity (CCC) within an allowed temperature rise. As the converter current rating rises rapidly in many applications, the trace CCC in PCB-based converters becomes an increasingly important topic related to thermal management and system reliability. If the trace temperature climbs up to a level beyond the glass transition temperature of the PCB lamination materials or beyond the maximum allowed temperature of the components close to PCB traces, it could cause permanent damage and operation failure can be predicted. Hence, sizing PCB traces for a certain amount of temperature rise with applied currents should be a basic step of PCB thermal management, especially for high-current applications.

Modern high-current PCB designs are commonly characterized with high current density, high component density, and high operating frequency. Many documents [5-23][5-24][5-25][5-26] present their guidelines and charts for PCB traces' CCC. However, they have been proved to be inaccurate and conservative [5-26][5-27][5-28]. Detailed literature reviews will be provided in Appendix B.1. For achieving higher accuracy and wider applicability in modern power PCB designs, the previous PCB trace thermal design guidelines should be modified and supplemented with consideration of additional CCC-influencing factors, like multi-layers, corners and AC effect.

The objective of this section is to develop thermal design guidelines for traces on PCBs with high-current, high component density and high frequency operation, in order to estimate the trace CCC at defined temperature rise requirements. In Section 5.5.1, the heat conduction impact of trace CCC will be investigated in single-, double- and multi-layered PCBs. In Section 5.5.2, the CCC of wide PCB traces which are usually used in HC applications will be studied under the influence of additional factors such as the AC effect and corner effect. The temperature measurement method and setups are given in Appendix B.3. Some discussion of this work is presented in Section 5.5.3.

Note the following conditions for all PCB boards used in this work:

- Board thickness is 1.5 mm.
- The traces and copper planes are 35 μm thick.
- The boards are placed vertically.
- Standard FR4 material is used. The thermal conductivity parallel with the boards and vertical to the boards are measured to be 1.648 W/(m·K) and 0.38 W/(m·K), respectively. The measurement setup and method are described in Appendix B.2.
- The boards are placed at an ambient temperature of 22 ^{o}C.

5.5.1 Heat Conduction on varied PCB structures

The heat is spread by conduction across the PCB, resulting in a larger effective heat dissipating area, hence lowering the temperature rises of PCB traces. In most PCB CCC design guidelines, PCBs with large spare areas (area with no copper paved) were employed (details seen in appendix B.1). However, in modern high-current PCB designs, the power component density is so high that such an area luxury rarely exists. This means that the heat spread area is limited and the resulting temperature rise is higher than the values provided in previous CCC design guidelines. In this section, the effect of heat conduction area on the trace temperature rises will be experimentally investigated.

Board designs shown in Fig. 5.36 are employed for the test. Here, *w* is the trace width and *M* is the board margin which means the distance from trace left/right edge to board left/right edge. When *M* = 0, an extreme case in high component density PCB designs, the heat is only removed from the surface of the traces. In this case, the clearance distances between traces and traces-to-components are neglected.

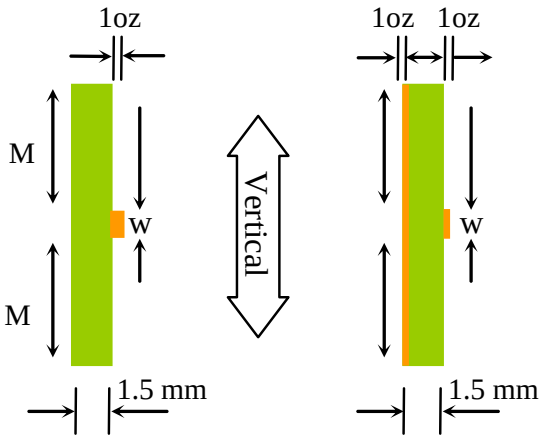


Fig. 5.36 Two PCB structures under test. Left: an external copper trace (1oz/35 μm thick) located in the middle of the board. Right: an extra copper plane (1oz/35 μm thick) at the backside.

Single-sided PCB

First, the temperature rises of the trace on the single-sided board (left figure in Fig. 5.36) with board margin *M* = 0 and 4 cm, respectively, are recorded and compared. The used trace widths are 2 mm, 5 mm, and 10 mm, and the trace thickness is 35 μm (1 oz). The measured results are shown in Fig. 5.37, where solid curves represent the trace temperature rises when the board has a 4 cm board margin to spread out heat, and dashed curves represent the trace temperature rises when the heat can only be dissipated within the trace area. The narrower board margin increases the temperature of the traces due to less heat dissipating area. In a high density PCB design, it is not possible to have a board margin as wide as 4 cm. However, the dashed curves in Fig. 5.37 represent the maximum trace temperature in high density PCBs.

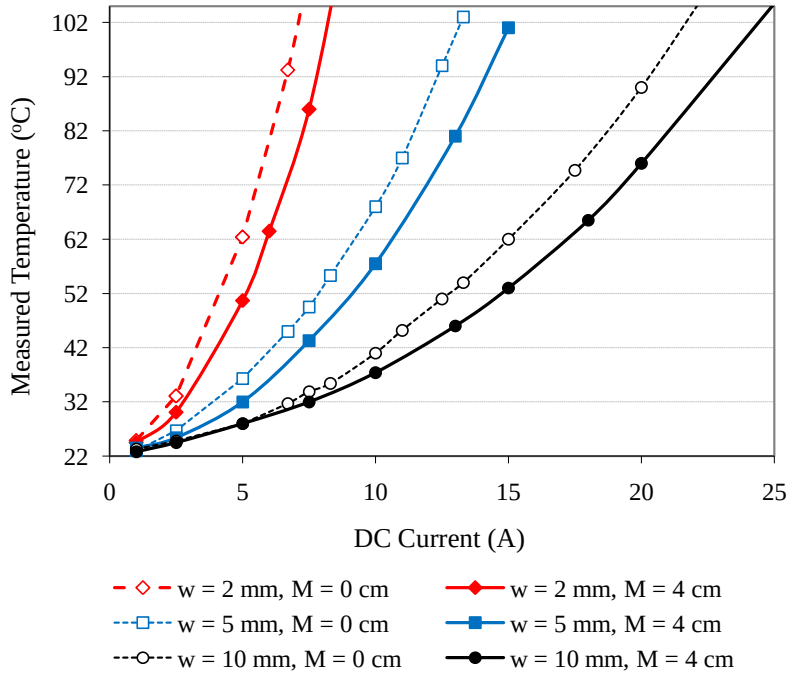


Fig. 5.37 Measured temperature rises of *w* wide the traces with varying DC current

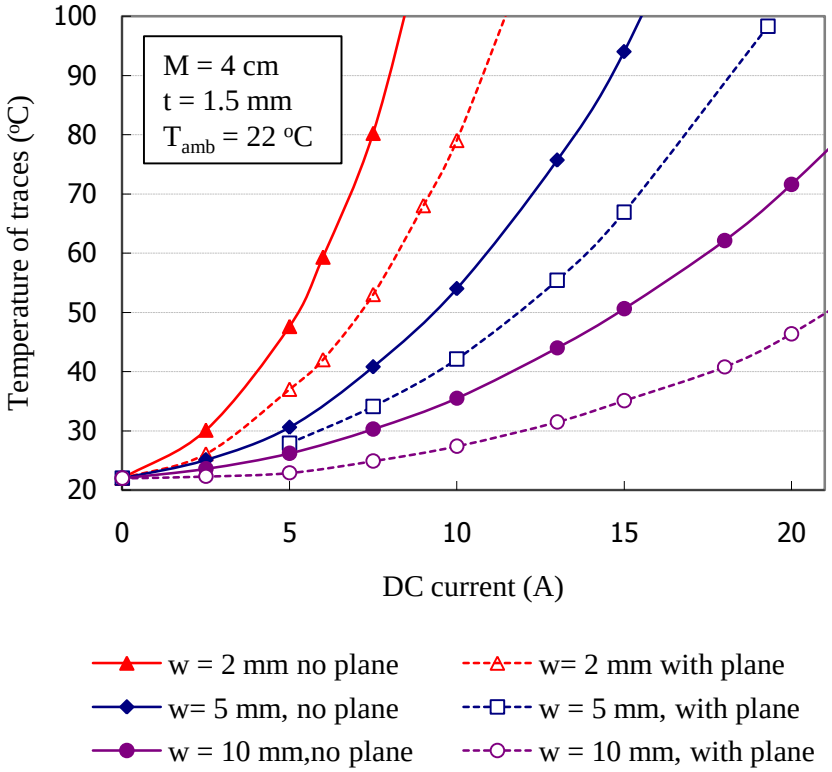


Fig. 5.38 Temperature rises of *w* mm wide the traces with varying DC current (Board margin *M* = 4 cm)

Double-sided PCB

Case 1: *One trace on one side and a copper plane on the other (M = 4 cm)*

Thanks to high thermal conductivity of copper, even 35 µm thick copper plane attached on the other side of PCB will spread the heat effectively across the board. The PCB structure depict-

ed in the right figure of Fig. 5.36 is tested. Its trace temperature rise is measured and compared with that of the same board without a copper plane. The results are plotted in Fig. 5.38. It can be found that the temperature rise of the trace on the board with copper plane at the back side decreases significantly, compared to the board without a copper plane. This PCB pattern is similar to that used in the IPC-2221 chart. However, the employed substrate material in IPC-2221 is phenolic and epoxy which has thermal property that are different from the FR4 material, which is commonly used today. Therefore, this test with FR4 material as substrate is of more value to current PCB design.

Case 2: *Two external traces on both sides of PCB (M = 0)*

Fig. 5.39 shows the measured temperature rises of two, 20 mm-wide external traces on both sides of the PCB with $M = 0$. Since the trace width is more than 10 times larger than the PCB thickness, the heat dissipated on the PCB edges can be neglected. This temperature curve can be also expressed as a function of the current density in each trace, $T_{tr\text{-}0}(J)$. This expression can be used to predict the temperature rise in a multilayer PCB which has the same current density in each layer. This will be explained below.

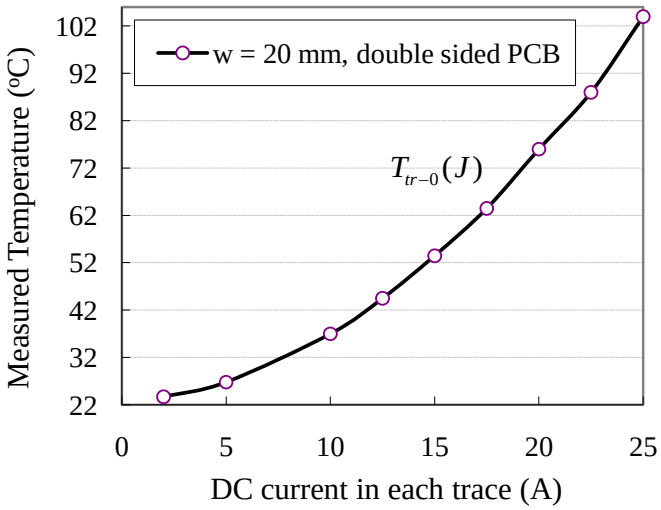


Fig. 5.39 Temperature rise of two 20 mm wide external traces on both sides of PCB

Multi-layered PCB

The left picture in Fig. 5.40 shows the double-layer PCB with current density J in both traces. A loss power P_1 is dissipated into the ambient by convection and radiation. The right picture in Fig. 5.40 shows the multilayer ($2N$ layer) case. If the loss power transferred to the ambient is the same in both cases, the temperature of the external layers should be the same. Assuming the current density in each layer of $2N$ layer PCB is J, the current density in each layer of double layer board should be $\sqrt{N} \cdot J$ ($P \propto J^2$) to obtain the same loss power dissipated to external environment. Then the temperature of the external layers of $2N$ layer PCB can be calculated with $T_{tr-0}(\sqrt{N} \cdot J)$.

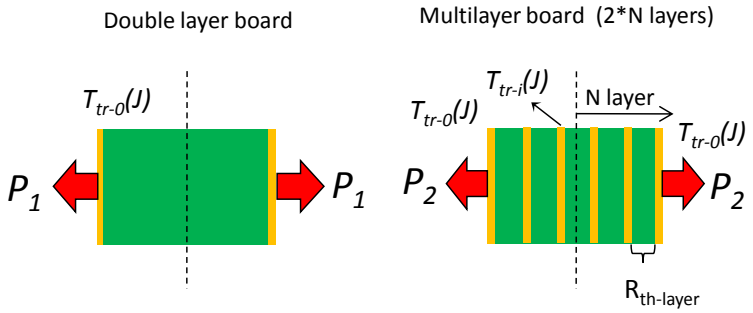


Fig. 5.40 Double layer PCB and 2N layer PCB with M = 0 having current density J in each layer

Fig. 5.41 shows the thermal network of the symmetrical half part of a multilayer (*2N* layer) PCB. The current density in each layer is *J*. The thermal resistance of the substrate material between each two copper layers is $R_{th\text{-}layer}$. The potential at each node in the thermal network represents the temperature on the corresponding layer. As long as the loss power flows vertically to the external layer, the temperature of the external layer can be calculated as $T_{tr-0}(\sqrt{N}\cdot J)$, which corresponds to the top node in the network shown in Fig. 5.41. Knowing the loss power injected in each node in the network and the temperature of the top node, the temperatures at the other nodes can be calculated with thermal resistance $R_{th\text{-}layer.}$ The power in each trace can be expressed as

$$P_{layer} = V_{tr}\cdot\rho_{cu}\cdot J^2 \tag{5-17}$$

where V_{tr} is the volume of each copper layer, ρ_{cu} is the electrical resistivity of copper. The variation of ρ_{cu} in each layer due to temperature difference is neglected. The temperature on the *i*-layer can be derived as

$$T_{tr-i}(J) = T_{tr-0}(\sqrt{N}\cdot J) + \left[N\cdot i - \frac{i(i+1)}{2}\right]\cdot R_{th-layer}\cdot V_{tr}\cdot\rho_{cu}\cdot J^2 \tag{5-18}$$

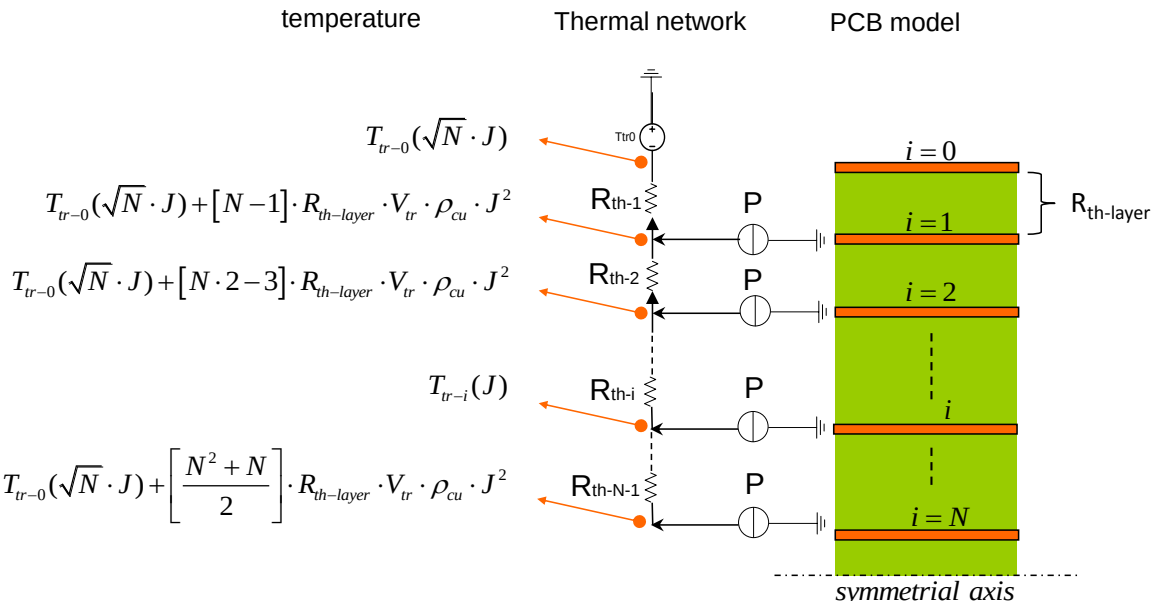


Fig. 5.41 Thermal network of the symmetrical half part of a multilayer (2N) PCB and the temperature on each layer

Keep in mind that Eq. (5-18) is only valid when the PCB is vertically placed and the internal heat is perpendicularly conducted to the external layers. When the layer number is odd, the temperature equation of each can be derived in a similar way and will not be described here.

All the current-carrying copper layers or traces under above tests have a thickness of 35 μm. If a different trace thickness t_{pcb} is used, the applied current I_{other} should be transferred to an equivalent current in the trace of 35 μm thick that generates the same loss power, so that all the measured temperature charts can be applied to check the temperature rises of the designed PCB. The equivalent current $I_{eq\text{-}35\mu m}$ in 35 μm thick traces can be calculated from:

$$I_{eq-35\mu m} = I_{other} \cdot \sqrt{\frac{35\mu m}{t_{pcb}}} \tag{5-19}$$

This section experimentally quantified the effect of heat conduction to reduce the temperature rises of the traces on the FR4 board. Two PCB scenarios are mainly investigated: FR4 boards with 4 cm board margin with and without 35 μm thick copper plane at the back side. The results are compared with the case when the trace width equals the board width ($M = 0$). The conclusion is drawn that both the board margin and the copper plane help spread the heat and reduce thermal stress on the traces. The measured trace temperature charts can be used as a thermal design reference of traces for PCB designers.

5.5.2 CCC of Wide PCB Traces

For high-current applications, wide PCB conductor strips are required. Due to skin effect, the current in foil conductors concentrate on the edges. When PCB tracks are bent, the current will concentrate on the inside of the bend curvature. In addition, adjacent conductor strips will induce currents in each other, causing the so-called proximity effect. This section will experimentally investigate the temperature rise of the traces due to these effects resulting in current concentration. The following layouts will be investigated in the frequency range DC and 20 kHz to 200 kHz:

- Straight trace
- L-shaped corners with various radii
- An isolated conductor on the top of a PCB, first with the return conductor adjacent to it, and then the return conductor as a conducting plane on the second layer
- An investigation of a transposition arrangement (Litz) between the first and second layer to improve the high frequency resistance

High-frequency current generation

To generate the high frequency current to feed the PCB traces, parallel resonant *LC* circuit excited by a half-switching bridge is used. The PCB trace under test at high frequency signal behaves like an inductor and then is utilized as the inductor part in LC parallel resonance circuit. The input of the switching bridge is a 60V-20A DC power supply. Between the switching bridge and the resonance circuit, a capacitor is placed to block the DC current. The circuit

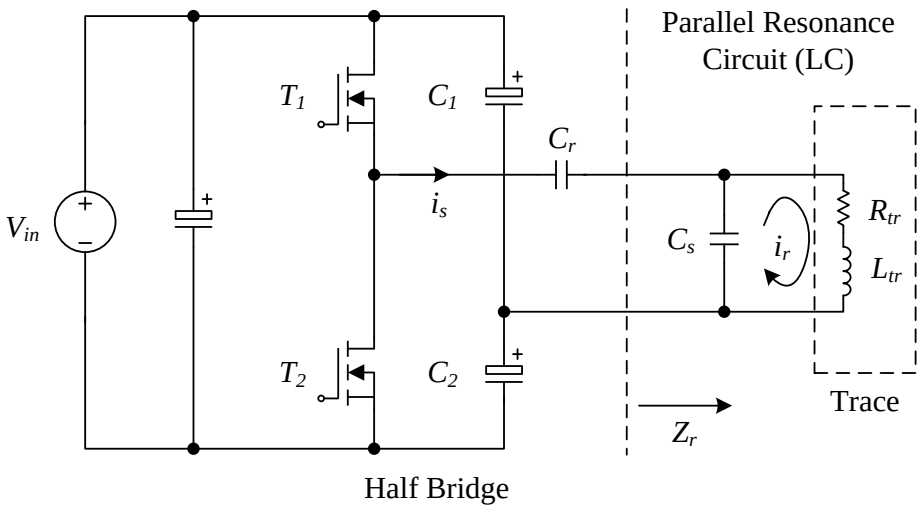


Fig. 5.42 Generation of high frequency current in PCB traces using the parallel resonant circuit

diagram is shown in Fig. 5.42. If the resonance circuit is tuned to resonance frequency, the input impedance of the resonance circuit can be very small, and the current i_r circulating between PCB trace and C_r would be of very high magnitude while the input current to the resonance circuit i_s would be very small compared with i_r. The type of the capacitors used for C_r and C_s is MKS2 WIMA, with values of 0.47 μF and 2.2 μF, respectively. The proper combination of several these capacitors together with PCB trace will obtain the resonance frequency of interest in range from 20 kHz to 200 kHz. The resonance current can have an RMS value up to 40 A.

Wide, straight traces with AC current

The AC effect reshapes the current distribution in conductors, causing the current density of one part to be higher than the others. The resulting temperature rise will be higher than in the DC case, but this AC effect is absent from all PCB trace thermal design guidelines.

First, a 2 cm wide, 19 cm long PCB with a 2 cm wide trace on one side is tested. The frequencies of the injected AC current are 34.5 kHz, 64 kHz, 116 kHz, 152 kHz, and 198 kHz. The measured temperature rises of trace are shown in Fig. 5.43, in which the temperature rise with DC current is included as well. It can be found that the current with higher frequency makes the trace hotter. Although the skin depth at 198 kHz, 147 μm, is about 4 times larger than the trace thickness 35 μm, the ac resistance of the trace is still appreciably larger than the dc case. Converting the x-axis into current density makes this chart also applicable to the trace with a width larger than 2 cm, but overestimates the temperature rise for $w < 2$ cm cases.

Next, the 2 cm-wide, 19 cm-long PCB, fully covered with copper traces on both sides, is tested. AC current is injected into both traces and the same five frequencies are applied as in the test above. The measurement results can be found in Fig. 5.44.

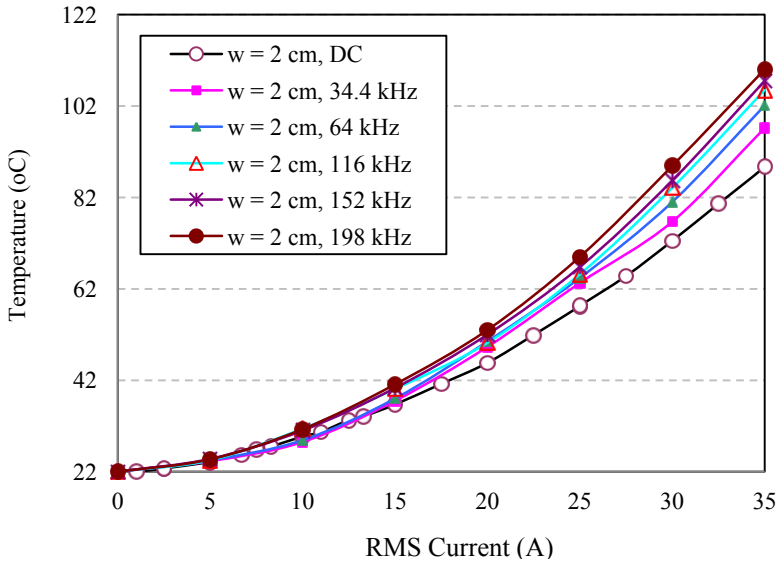


Fig. 5.43 Measured temperature rises of a 2 cm wide trace (M = 0) under AC current with five different frequencies

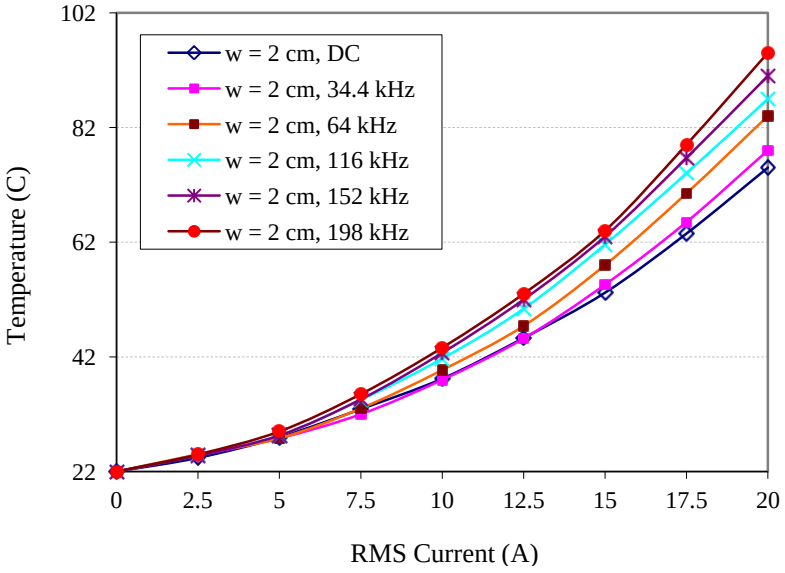


Fig. 5.44 Measured temperature rises of 2 cm wide traces on both sides of PCB (M = 0) under AC current with five different frequencies

In this test, the proximity effect is involved in addition to the skin effect. As expected, the current with higher frequency causes the trace to be hotter. If the loss in the traces is the same in two cases shown in Fig. 5.43 and Fig. 5.44, then the extra rise of trace temperature with the presence of proximity effect is 9 ^{o}C higher at 198 kHz case. This means that the proximity effect does affect the thermal stress on traces. If more current-carrying layers exist in the board, the proximity effect will be more obvious on pushing the temperature high.

L-shaped corners with various radii

If the trace bends, such as transformer windings, the current tends to flow through the path that lowers the impedance, normally on the inner side of the bends. The current is concentrated there, driving the temperature in that part higher. This section examines the temperature rise of the trace corner with various radii under DC and AC current.

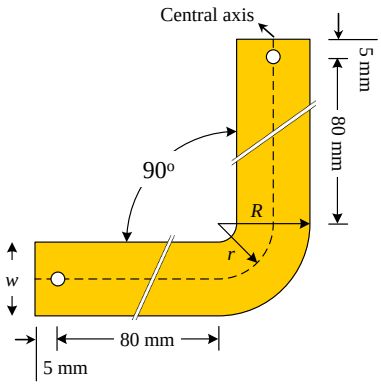


Fig. 5.45 The PCB trace with 90° L-shaped corner

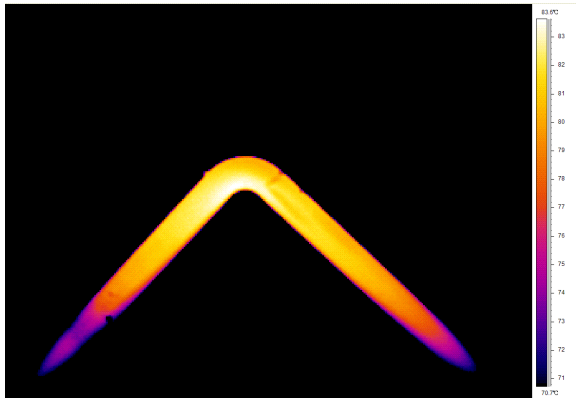


Fig. 5.46 Infrared thermal picture of the 10 cm wide trace (r/R = 0.65, 198 kHz, 16 A rms current, T_{amb} = 22 °C)

The tested trace on the single-sided PCB structure is drawn in Fig. 5.45. This structure is vertically placed. The *w*-cm wide trace bends with right angle, with radius *r* from origin to the middle line of the trace and radius R from origin to the outer edge. L is the length of straight part of the trace. The 35 μm thick trace has the same width as the board. Injected are DC current and AC current with the frequency of 34.4 kHz and 198 kHz. Here we investigate two curve rates of the bends: r/R = 0.5 and 0.65. The ratio r/R = 0.5 represents the R = w, which is a sharp 90° corner. Fig. 5.46 shows the infrared thermal picture of the 10 cm-wide trace with r/R = 0.65 and with the AC current of 198 kHz and 16 A rms. The temperature range is set between 70.7 °C and 83.6 °C. It can be clearly seen that the maximum temperature is distributed at the inner corner of the trace. Here the maximum temperature determines the current carrying capacity of the trace.

Two figures below summarize the maximum temperatures on the different bended PCB trace with DC current and AC current, respectively. Fig. 5.47 shows the results of the DC current case. The trace widths under test are of 2 mm, 5 mm, 10 mm and 20 mm. The curve rate r/R are of 0.5 (dashed line) and 0.65 (thin solid line), and the straight trace case (bold solid line) is measured and compared as well.

It can be concluded from Fig. 5.47 that

- The bended trace has a significantly higher maximum temperature rise than the straight one at the same current, which in turn means that the current rating of the bended trace is smaller than the straight case to obtain certain amount of maximum temperature rise. The wider trace will be subjected to a more serious de-rating in the current carrying capacity.
- The difference in the maximum temperature rises on the bended traces with different curve ratio r/R becomes more and more obvious when the trace width is small.
- If the trace width is wide, e.g. larger than 5 mm, different trace curvatures have a negligible influence on the maximum temperature rise.

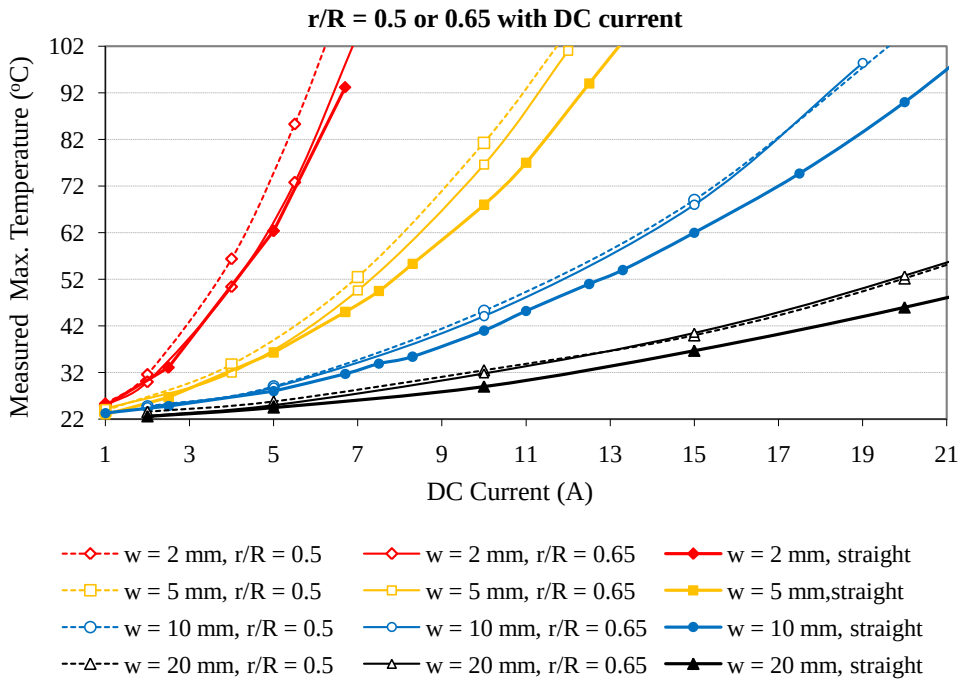


Fig. 5.47 The measured maximum temperatures at the inner corner of the bended trace with different trace widths, different r/R and with different injected DC current.

As indicated by the conclusions drawn above, the PCB designer should keep in mind that the current carrying capacity of the designed traces has to be primarily determined by the trace bends, especially in a high-current case where the wide trace is present.

Fig. 5.48 gives the measured maximum temperatures on the bended traces under AC current of two frequencies, 34.4 kHz and 198 kHz. The bended traces have widths of 2 mm, 5 mm, 10 mm and 20 mm, and the curve rates r/R of 0.5 and 0.65.

One could find that when the trace width *w* is larger than 1 mm, the AC effect does not make remarkable differences in maximum temperatures for all the bended traces under two current frequencies. However, when the trace is narrower than 1 mm, the AC effect does affect the temperature when RMS current increases. For example, the bended trace with r/R = 0.5 has an approximately 10 ^{o}C higher maximum temperature than the one with r/R = 0.65, when the RMS current is 5 A and the frequency is 34.4 kHz. The higher frequency makes the AC effect on the temperature rises more pronounced.

Fig. 5.49 shows the measured maximum temperature of bended traces at DC case, 34.4 kHz and 198 kHz. It can be seen again that AC effect makes trace hotter. Hence, the CCC of traces has to be derated.

Trace with a return conductor as a copper plane

The temperature rise of a trace with its return conductor as a copper plane on the other side of the PCB is measured. The tested PCB structure is shown in Fig. 5.50. Note that T1 is the terminal of the trace on the top side and T2 is the terminal of the copper plane fully covering the

other side of the PCB. The top trace and the bottom copper plane are electrically connected by the through vias on the right hand side of the PCB. The top trace is 2 mm wide. AC current is injected into the structure via T1 and T2.

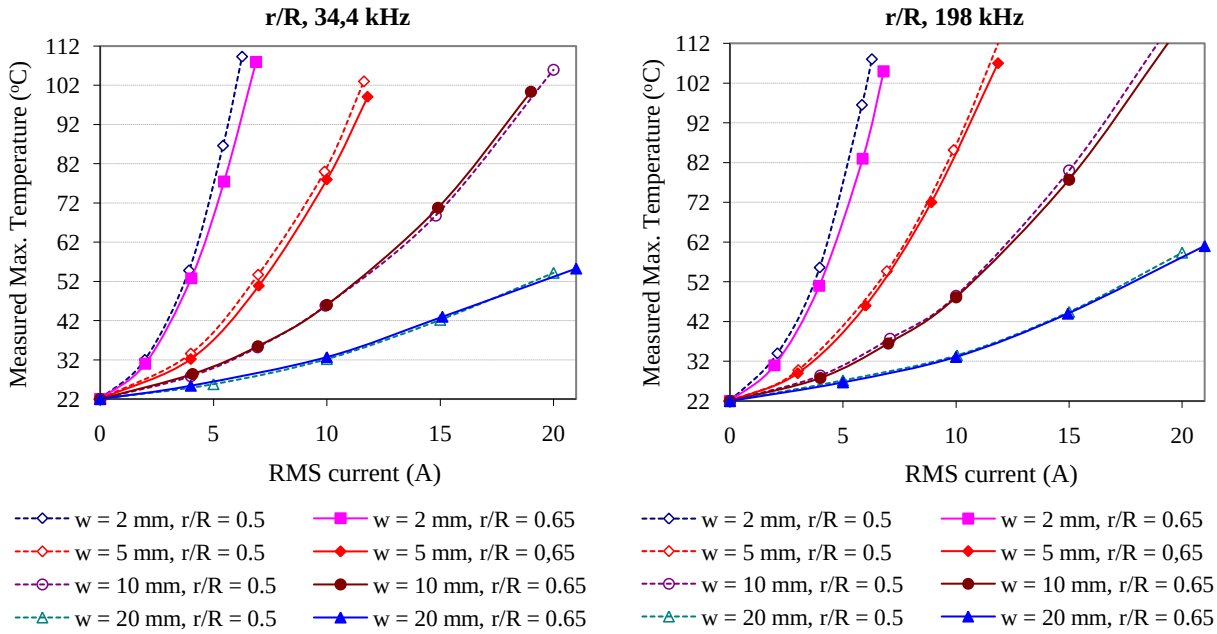


Fig. 5.48 The measured maximum temperatures at the inner corner of the bended trace with different trace widths, different r/R and with different injected AC current.

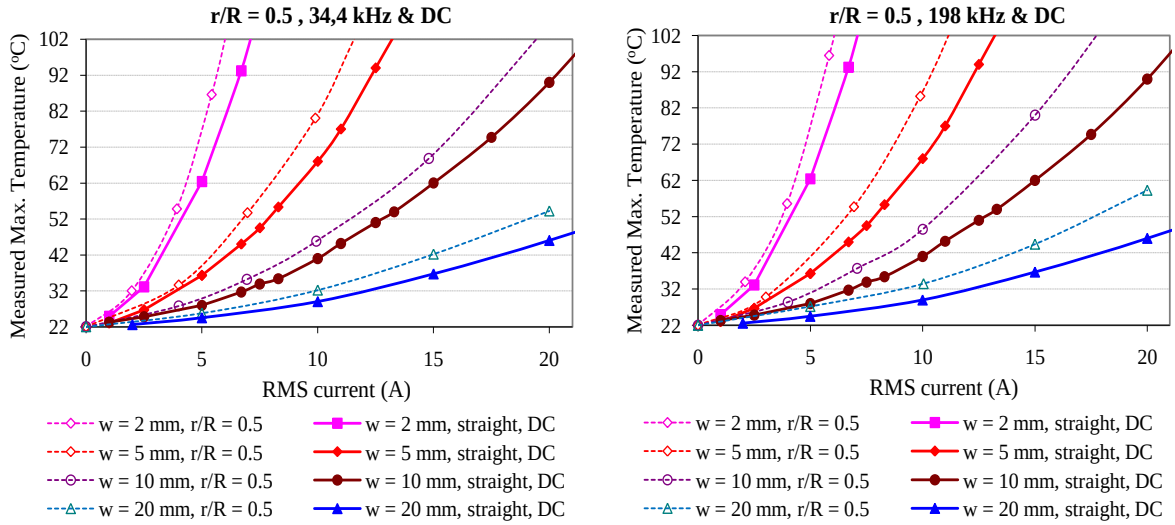


Fig. 5.49 Measured maximum temperatures at the inner corner of the bended trace with different traces under AC current with 34.4 kHz and 198 kHz and DC current

The temperature rises of the trace under AC currents (34.4 kHz and 198 kHz) are measured and compared with the two other PCB structures. One is the single sided PCB with M = 4 cm and another one is the double-sided PCB with a 2 mm trace on top (where M = 0) and the copper plane at the back side only for heat spreading. In these two cases, the current only flows on the trace between T1 and the other end where through vias stands in Fig. 5.50. The measured results are given in Fig. 5.51. The temperature rise in the single-sided PCB (no copper plane case) is significantly higher than in the others, as expected. From the other two,

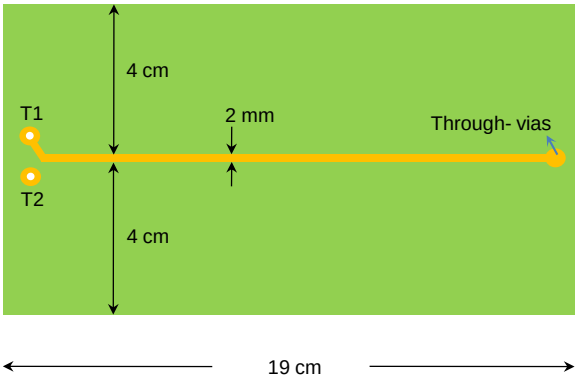


Fig. 5.50 The top view of the trace structure with the backside copper plane as the return conductor

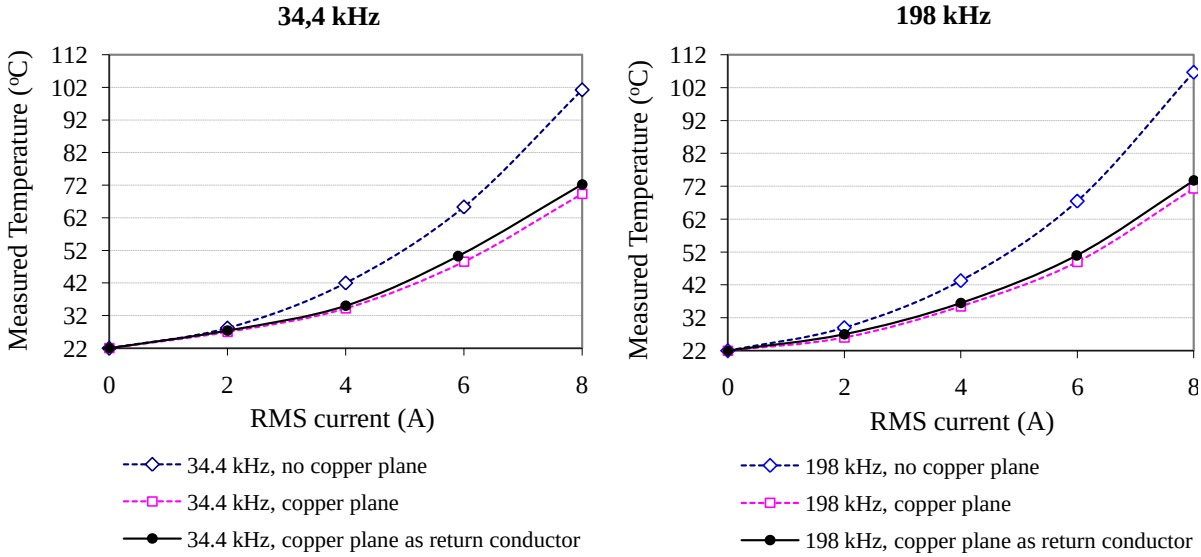


Fig. 5.51 Measured temperature rises of the trace on three PCB structures (T_{amb} = 22 °C)

the important finding is that if the copper plane is used on the return conductor, the temperature rises is higher than the case where the copper plane is only used for spreading the heat. This is remarkable as high frequency AC return current will flow mainly under the trace.

Transposed trace

In a Litz wire, each strand constantly shifts its position in the magnetic field in such a way that the increase of the AC resistance due to the proximity effect is minimized and the current is evenly distributed over all strands. Based on the same principle, a transposition arrangement of the position of the traces is also supposed to decrease the high-frequency resistance of traces in the AC magnetic field. This section investigates thermal performance of the enclosed traces with transposition structure under AC currents.

Fig. 5.52 shows the simple structure of the non-transposed (left) and transposed (right) traces. The T1 and T2 are the trace terminals where the AC current is injected. The two parallel traces are connected at T1 and T2. In the non-transposed structure, the outer (inner) trace stays inner (outer) along the path. The inner trace would have lower impedance than the outer one,

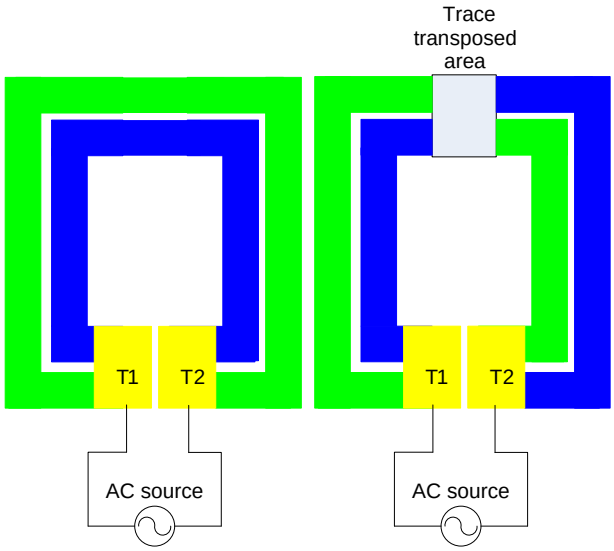


Fig. 5.52 Illustrations of the non-transposed and transposed traces structures

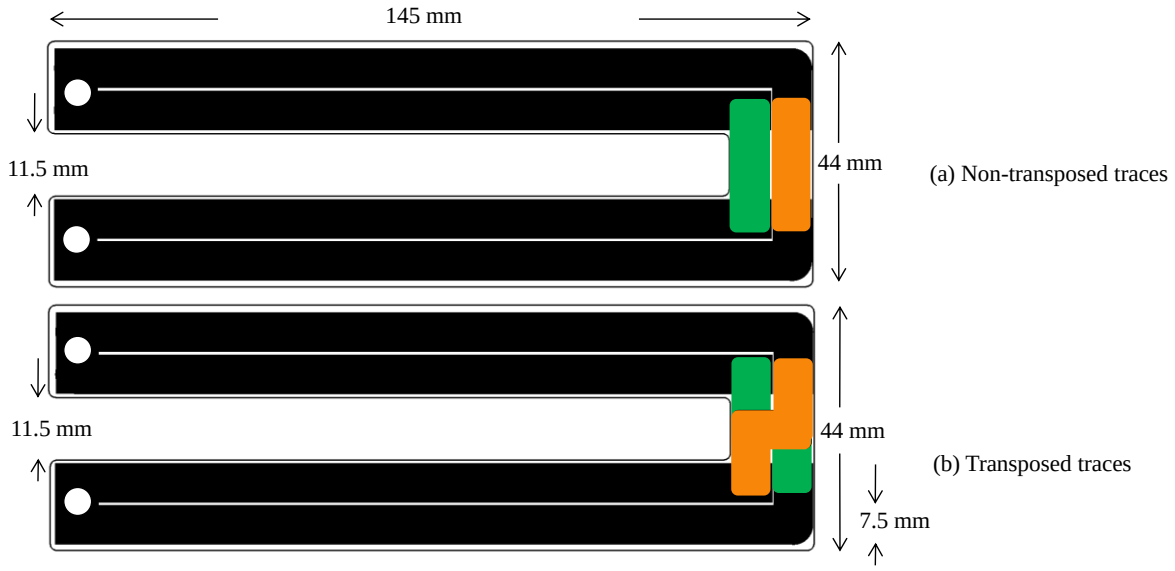
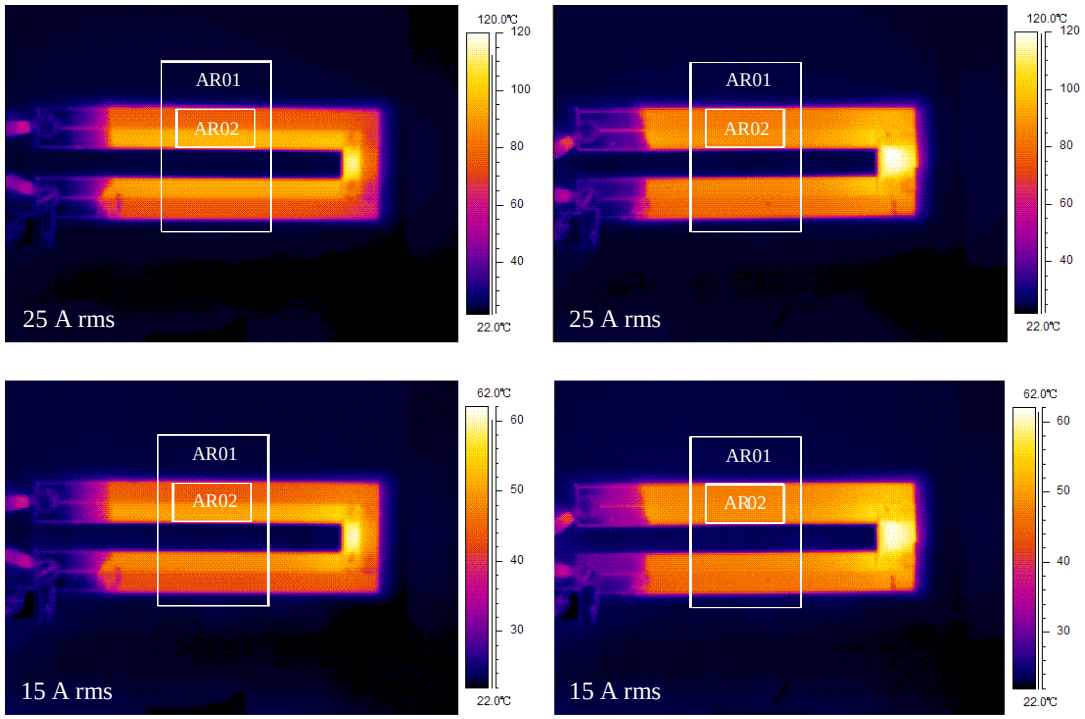


Fig. 5.53 Designed non-transposed traces (a) and transposed traces (b). 1oz thick copper strips (in green and orange color) are used to bridge the traces on two legs. Isolation exists between two strips in (b)

hence inducing a higher current as well. But in the transposed structure, the inner (outer) trace on the left leg switches to the outer (inner) on the right leg, via a trace transposed area. In this way, two parallel traces alter their position in the magnetic field and bears the equal impedance, having the current equally shared on two traces. In the trace transposed area, the traces can switch position in two ways, either one trace is routed into a second layer by vias or the two traces are bridged by two separated copper strips with isolation in between them. The second way is used in the test and designed boards are shown in Fig. 5.53. This kind of structures can also be seen as the winding of transformers and inductors.



a) Non-transposed traces structure b) Transposed traces structure

Fig. 5.54 Infrared pictures of the non-transposed (a) and transposed (b) traces structures under AC currents (206 kHz, 15 A rms and 25 A rms, T_{amb} = 22 ^{o}C)

The temperature rises of both structures under AC current with frequency of 206 kHz and RMS values of 25 A rms and 15 A rms are recorded by a thermal camera. The infrared pictures are given in Fig. 5.54. The upper two pictures represent the 25 A rms current case and the bottom is for the 15 A rms case. Due to the contact resistance or overlapped current carrying strips, the temperature rises are distinctly higher than the other part, which will not be accounted for in the thermal performance comparison. However, the temperature distribution along the leg parts (rectangular area AR01) is normal and the temperatures of these parts are measured and compared.

In Fig. 5.54, one can observe that the inner trace in the non-transposed structure has an obviously higher temperature than the outer trace, but in the transposed structure the temperature rises on two parallel traces vary only slightly. The maximum temperatures in rectangular area AR01 are measured and recorded in Fig. 5.55. The transposed traces have lower maximum temperatures than the non-transposed case (3 ^{o}C less at 15 A rms and about 8 ^{o}C less at 25 A rms).

The tests above demonstrates that the transposed structure is able to lower the maximum temperature rises on the traces, which means higher current carrying capacity can be achieved. It implies that the wide PCB traces, as the high-current transformer winding, can be transposed to reduce the winding loss or increases the current rating.

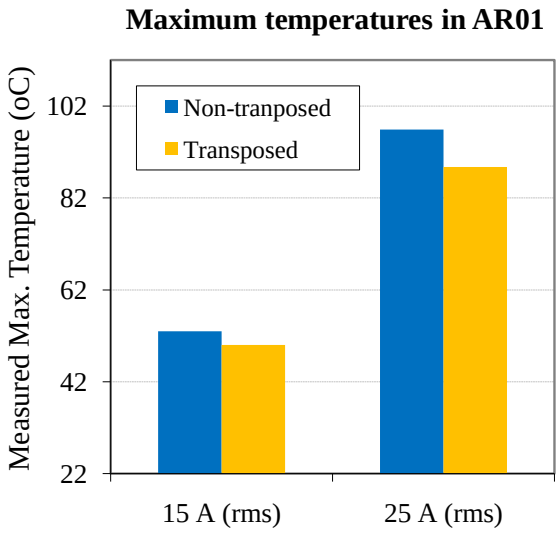


Fig. 5.55 Measured maximum temperatures in AR01 and minimum temperatures in AR02 (206 kHz)

5.5.3 Discussions

This section experimentally investigates the PCB trace CCC in various trace structures and operating conditions, taking into consideration a wider scenario than included in the old PCB trace thermal design guidelines. However, this work also has some limitations and they are discussed below.

This work has been done based on FR4 material only. However, due to the increasing loss density on PCBs, base materials with higher thermal conductivity than that of the commonly used material FR4 are emerging for better PCB thermal management. 99ML and T-preg are typical representatives and are becoming increasingly popular in PCBs with high losses. Therefore, the development of CCC design guideline for PCBs with high thermal conductivity materials is recommended.

The test boards in this work are only placed vertically in a natural convection condition. Horizontal placements and forced convection are not considered.

Most of the trace thermal design charts included in this research are obtained under room temperature. However, many power PCBs work in ambient temperatures over 40 ^{o}C. This decreases trace CCC to reach a fixed temperature rise, since trace resistances and loss generated will rise at higher temperatures.

PCB trace thermal design guidelines can be only used as the starting point of PCB design. There are limitations to accurately predicting the temperature rises of traces in modern PCBs where high loss generating components are densely populated. For critical parts of PCBs, correctly derived analytical and even FEM analysis are still required to closely check the design reliability.

5.6 Conclusions

This chapter first compares the geometrical properties of commercial planar and barrel E-shaped magnetic cores. It is found that the planar transformers generate less core loss at the same flux density, but more winding loss at the same current density. However, planar cores bear more core and winding surface area to dissipate heat, indicating better cooling properties.

To minimize the transformer loss at low-voltage and high-current applications ($\geq$ 100A), using a single-turn winding for high-current winding is proved to be the optimal option. Three high-current planar transformer prototypes based on commercial ferrite cores have been compared in terms of hotspot temperature, efficiency and volume. It is concluded that the winding loss of planar transformer may be alleviated by using copper foil and Litz wire because of their higher filler factors than PCB windings. To control the leakage inductance in planar transformer, the integrated leakage layer between windings is proved to be effective by tuning the distributed air gaps.

Planar transformer concept based on nanocrystalline C-shaped cores is proposed and the core dimension optimization is addressed to minimize the transformer loss for a given DAB converter design at steady state. The optimized transformer design also significantly reduces the winding loss at transient state. In comparison with a ferrite planar transformer design, the proposed nanocrystalline transformer demonstrates the following advantages:

- High power density for high-current application.
- More effective cooling surface due to the designed C-shaped core structure.
- Freedom to tune the leakage inductance by manipulating the core distance and winding structures.

The state-of-art CCC guideline of PCB traces is out-of-date compared to modern high-current high power density PCB designs. This work has experimentally investigated the PCB trace CCC in various trace structures and operating conditions, which contains a wider scenario than the old guidelines. The limits and use recommendations of the proposed trace thermal design guidelines are also discussed.

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Chapter 6

Collective Cooling Strategy for Planar DAB Converters

6.1 Introduction

Previous chapters have addressed the optimal heat generation management of a high-current PE system. It is accomplished with the circuit topology selection (Chapter 3) and transformer design (Chapter 5) based on the proposed loss modeling approach (Chapter 4). Heat generation management provides optimized loss inputs to heat removal management or, otherwise stated, a cooling design. However, if not effectively dissipated through a cooling system, even minimal loss creates serious hotspots within a PE system, which may result in an insufficient system lifetime. The lifetime of PE converters is influenced by numerous factors, e.g. temperature, temperature fluctuation magnitude, electrical stress, humidity, mechanical vibration, and software errors. In this aspect, temperature has been ascertained as the dominant failure mechanism [6-1]. Therefore, the primary objective of the cooling design is to control critical temperatures below certain thresholds so that the system lifetime meets specified requirements.

In vehicle applications where the amount of space is significantly limited, the cooling design is required to be not only thermally effective but also volumetrically efficient. This means that low enough thermal impedance must be achieved within limited volume. In reality, the cooling function of mid- and high-power PE systems contributes a lot to total system volume [6-2]. In addition to inefficient heat generation management, two primary root-causes exist from a heat removal perspective:

– *Ineffective Heat Interface Design*

The cooling structure from a component to the coolant (such as air or liquid) consists of three main elements: the heat generator, heat interface, and heat exchanger as illustrated in Fig. 6.1(a) which is a simplified representation of reality. Heat generators are loss-generating components within a PE system, and the heat interface is a thermal bridging structure that

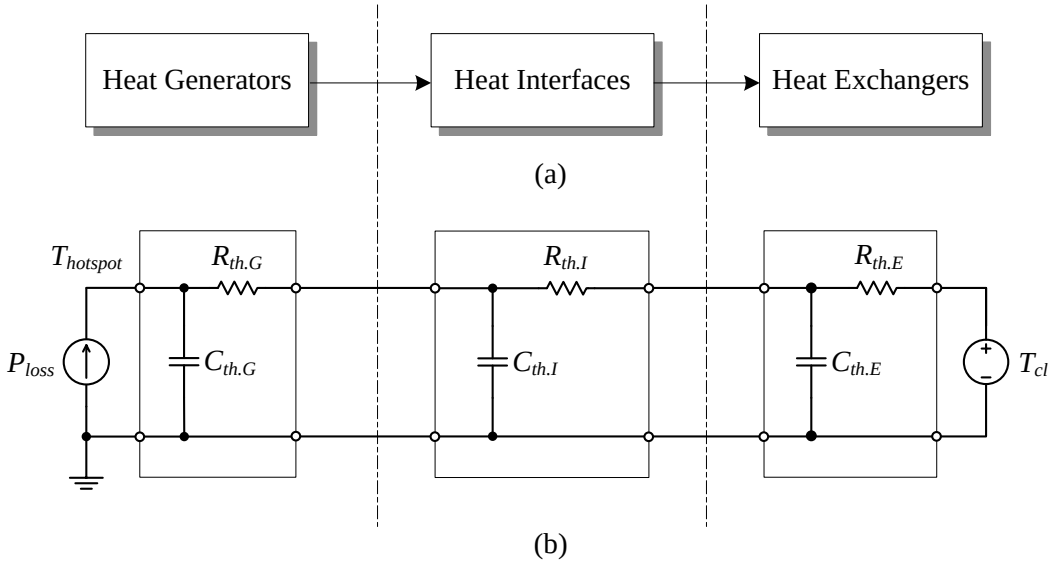


Fig. 6.1 Thermal impedance network of the cooling structure for a power component

conducts heat to the heat exchanger (e.g. heatsink, cooling plate) where heat is exchanged with the coolant. This cooling structure can be described by the thermal impedance network depicted in Fig. 6.1 (b) where loss (P_{loss}) is equivalent to a current source; coolant temperature (T_{cl}) is considered as a voltage source; and thermal resistance and thermal capacitance of each part ($R_{th.G}$, $R_{th.I}$, $R_{th.E}$, *and* $C_{th.G}$, $C_{th.I}$, $C_{th.E}$) are analogous to the electrical resistance and capacitance [6-3]. They are calculated as:

$$R_{th} = \frac{d}{\sigma_{th} \cdot A} \tag{6-1}$$

$$C_{th} = c \cdot \rho \cdot d \cdot A \tag{6-2}$$

where d is the material thickness, σ_{th} is the thermal conductivity, A is the cross section area, c is the specific heat capacity, and ρ is the density. In the thermal steady state, the increase in temperature of a component can be described as:

$$T_{hotspot} = T_{cl} + P_{loss}\left(R_{th.G} + R_{th.I} + R_{th.E}\right) \tag{6-3}$$

With defined power loss and coolant temperature, these three thermal resistances ($R_{th.G}$, $R_{th.I}$, $R_{th.E}$) determine the component temperature. If the heat interface resistance is not carefully designed, a heat exchanger with an expansive surface area must be exploited to compensate for an acceptable hotspot temperature. As a result, an ineffective heat interface causes a cumbersome cooling system.

– *Differentiated cooling strategies*

By nature, power components differ in packaging structures and loss density levels [6-3], therefore, their cooling designs are usually differentiated. It can often be seen in a state-of-art PE converter that high power semiconductors are directly attached against heatsinks using various methods depending on the their packages and, on the other hand, power capacitors are cooled by residual forced air flow which is originally engaged at semiconductor heatsinks.

Magnetic components have either cooling method according to the applied power and design options. This differentiated and localized cooling strategy leads, to a large extent, to:

- An uneven converter structure due to unmatched component and heatsink shapes. This leaves a significant amount of waste air in the system that does not play any functional role such as convection cooling and isolation.
- Inefficient cooling. For example, the air blown against a local heatsink also circulates unnecessarily over the components that are much less dissipative.
- potentially larger size of components that cannot be involved in strong cooling. For example, if magnetic components can somehow be coupled with the heatsink for semiconductors, this collective cooling effort may enable a smaller transformer volume with a little marginal cost.

Objective

The objective of chapter is to propose and investigate a collective cooling strategy as a heat removal management approach for high-current DAB converters. The goal of this strategy is to create a thermally effective and volumetrically efficient cooling structure. The principle of this cooling strategy is to collect heat from the main power components via different heat interface designs and conduct it to a common heat exchange surface where heat is dissipated in a centralized manner. The characteristics of this cooling strategy include:

- It is based on a low-profile converter structure. The planar structure should be initially targeted to create a large, flat, and accessible cooling surface area of power semiconductors and high-current transformers. This is to create a solid foundation for the effective heat interface design.
- Double-sided collective cooling is feasible by enabling two heat conducting paths from each side of the low-profile structure to the heat exchanger.
- It is a system-level heat removal management approach. The heat is collected, conducted, and collectively dissipated.
- Heat exchange extends over the entire converter footprint area to guarantee a large cooling surface and short access to all critical heat generators.

The structure of this chapter is described below. In Section 6.2, thermal structures of power semiconductors and planar magnetic components will be introduced, and their heat interface designs are addressed. The collective cooling concept is explained in Section 6.3 where a high-current 1 kW DAB converter will be built as a demonstrator. To fully exploit the large surface area of the low-profile structure, a double-sided collective cooling (DSCC) strategy is proposed in Section 6.4. A high current DAB converter with 2 kW nominal power and 10 kW peak power will be designed according to this strategy where pros and cons of this cooling strategy will be analyzed.

6.2 Low-Profile Components and Their Heat Interface Design

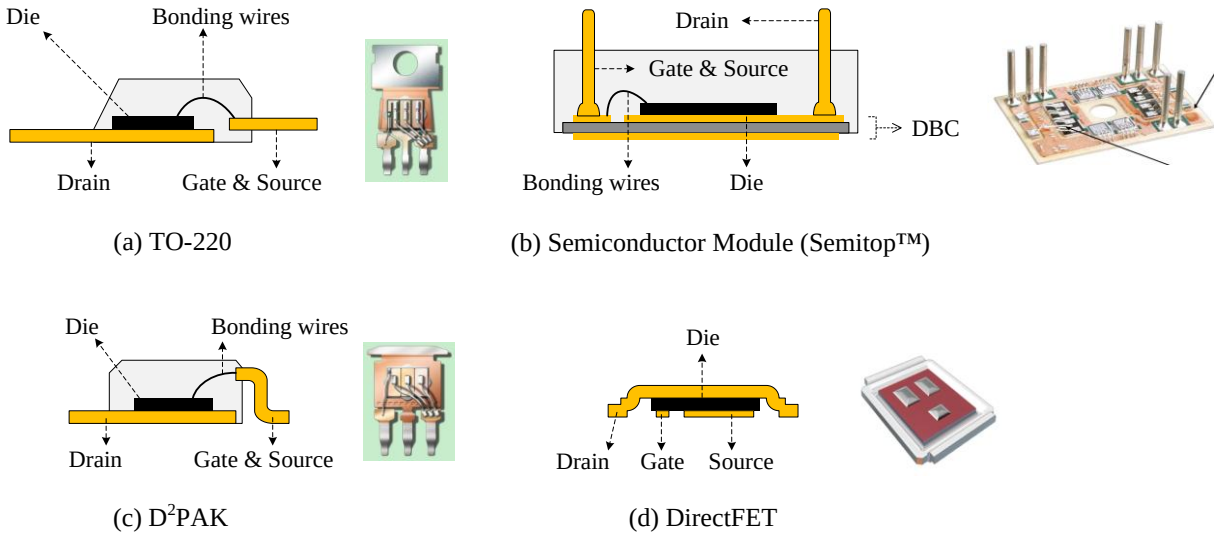
The low-profile structure is characterized by a large accessible surface area and small thickness. A planar heat generator is thermally advantageous since its thermal resistance perpendicular to the wide surface area (A) is low, referring to Eq. (6-1). This part will introduce the thermal structures of various low-profile power components and their heat interface design possibilities. It also provides the background for subsequent sections. Due to the significant loss density compared with other components [6-3], power semiconductors and magnetic components are addressed in this section.

6.2.1 Power Semiconductors

High-current power semiconductors are equipped with large dies for lower on-state resistance. Loss density on a small die is so enormous that a cooling structure design must be conducted on the packaging level for a small $R_{th.G}$. Fig. 6.2 illustrates the cross-section view of four typical high-current packages: two through-hole packages (TO-220 and Semitop™ module) and two SMD packages (D²PAK and DirectFET). Their open-frame pictures are provided as well. High-current semiconductor dies are often soldered directly onto one of the terminal leads or other thermally conductive substrates (e.g. direct bonding copper used in Semitop™ [6-4]). This structure spreads heat over a more extensive cooling area and hence results in decreased heat generator thermal resistance, which is also known as junction-to-case resistance ($R_{th.jc}$). Fig. 6.3 provides an overview of the range of $R_{th.jc}$ and thickness of four semiconductor packages with a current rating larger than 100 A. Note that the DirectFET [6-5] package has an ultra-thin structure (<1mm) with a double-sided cooling possibility which provides another degree of freedom for the cooling design.

Heat Interface Design

For a constant temperature drop from junction to coolant, lower thermal resistance of the heat



(a) TO-220 (b) Semiconductor Module (Semitop™)

(c) D²PAK (d) DirectFET

Fig. 6.2 Cross-section views and open frame pictures of four high-current MOSFETs: (a) TO-220 [6-7], (b) Semitop modules [6-4], (c) D²PAK [6-7] and (d) DirectFET [6-5].

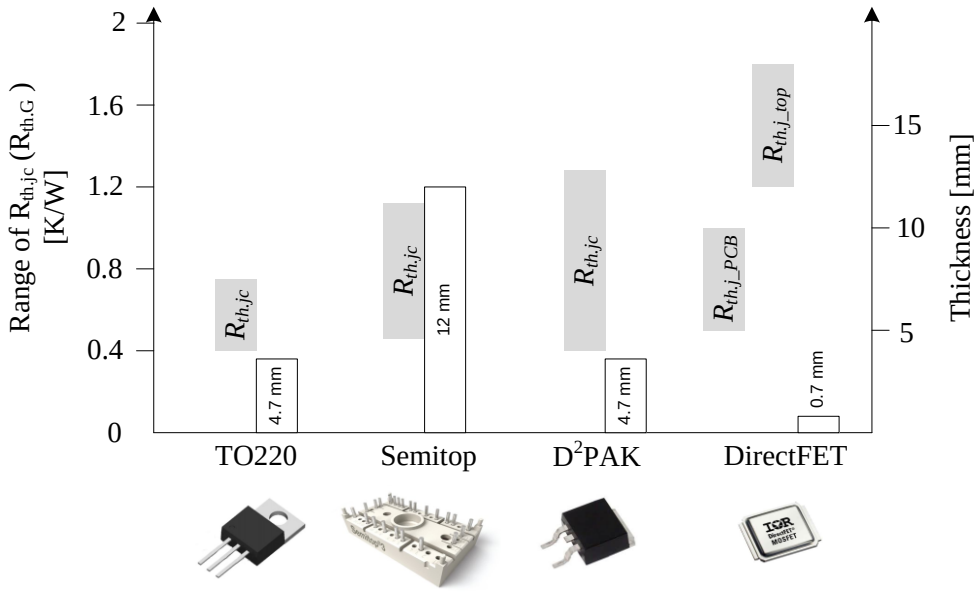
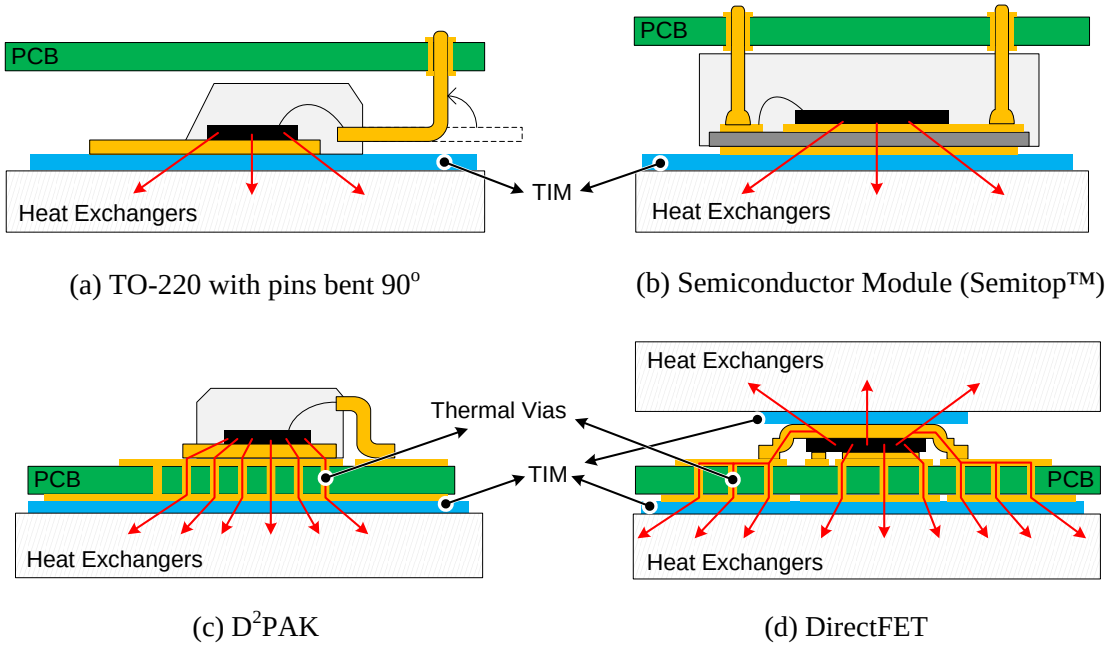


Fig. 6.3 Range of case-to-junction thermal resistance ($R_{th.jc}$) and thickness of four varied semiconductor packages with current rating larger than 100 A ([6-4][6-6]).



(a) TO-220 with pins bent 90°

(b) Semiconductor Module (Semitop™)

(c) D²PAK

(d) DirectFET

Fig. 6.4 Heat interface design for (a) TO220, (b) Semiconductor Module, (c) D²PAK and (d) DirectFET. Red arrows indicate the heat flow directions. (Figures not to scale)

interface allows larger thermal resistance of heat exchangers, in other words, smaller heat exchangers. Due to different packaging methods, the heat interface design varies for power semiconductors.

– *TO-220*

TO-220 packages are often mounted vertically onto the PCB which requires the attached heatsink to stand perpendicularly on the PCB. This protruding heatsink undermines the low-profile system structure. To overcome this disadvantage, the leads of the TO-220 can be bent 90°, and the package can be clamped between the PCB and heatsink as illustrated in Fig.

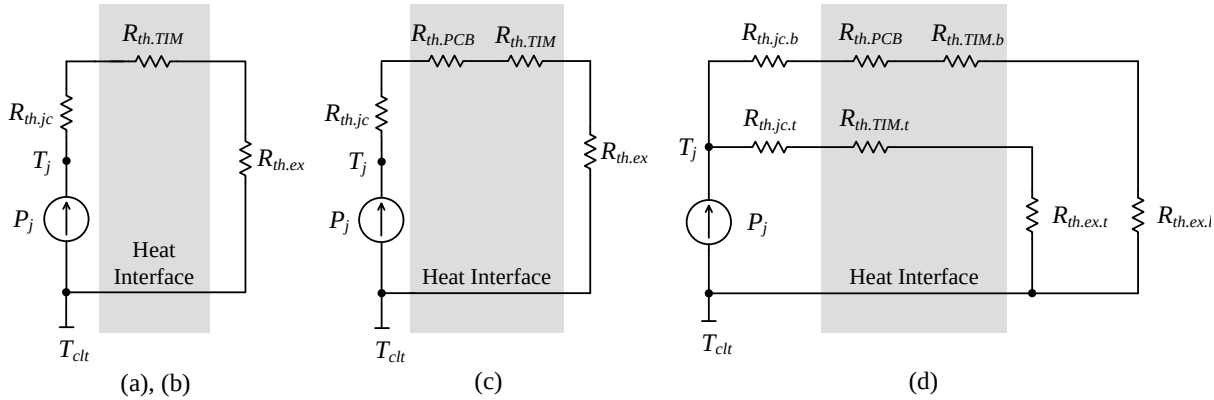


Fig. 6.5 Lumped thermal network of (a, b) TO220 and Semiconductor module, (c) D^2PAK and (d) DirectFET

6.4(a). An electrically-isolating Thermal Interface Material (TIM) layer is required be placed between the semiconductor and the heat exchanger which facilitates the usage of an inexpensive TO-220 package in a low-profile structure. However, this is not a standard assembly method: mounting and fixation become complex and time-consuming.

– *Semiconductor Module*

Multiple semiconductor dies can be placed in the same through-hole module as an integrated and compact solution. The Semitop^{TM} package is an example. The thickness of the semiconductor modules is normally greater than 10 mm [6-4], however, it complies with the standard assembly method and can be directly coupled with the heatsinks. The lumped thermal networks of the TO-220 and modules are depicted in Fig. 6.5(a, b). The heat interface design of these two packages is straightforward insofar as only having to select a TIM layer between the packages and heat exchanger surface for a low enough thermal resistance ($R_{th.TIM}$).

– *D^2PAK*

At a minimal loss level, this SMD package only requires a copper plane underneath it to spread heat and cool down through convection. At an elevated loss level, both the copper plane and through-hole thermal vias must be deployed beneath and around the package to spread and conduct heat to the heat exchanger attached against the other side of PCB. Here, a TIM layer is also required. This concept is illustrated in Fig. 6.4(c). The heat interface design aims at an appropriate thermal resistance of the TIM layer ($R_{th.PCB}$) and thermal vias ($R_{th.PCB}$) as indicated in Fig. 6.5(c).

– *DirectFET*

Two thermal paths are available in a DirectFET package. Just as with a D^2PAK, the copper plane and thermal vias can be applied to spread and conduct heat to the heat exchanger at the other side of PCB (Fig. 6.4(d)). If extra cooling is required, an additional heat exchanger can be pushed against the topside of DirectFET. The thermal impedance network is provided in Fig. 6.5(d) where $R_{th.ex.t}$ and $R_{th.ex.b}$ represent the resistances of two thermal paths. The ultra-

thin structure and double-sided cooling capability generate DirectFET superior thermal performance.

6.2.2 Magnetic Components

Magnetic components have a more complicated thermal structure compared to power semiconductors since two internal heat sources (cores and windings) are structurally intertwined. A coordinate system of planar transformer cores is illustrated in Fig. 6.6. Under this coordinate, the planar transformer can be partitioned into eight thermally symmetrical parts in both the ZX and ZY cross-section views. One of eight parts in each view is depicted in Fig. 6.7. Lumped thermal networks in both views are also illustrated. Here, losses in primary and secondary windings (P_{wp}, P_{ws}) and core loss in the middle of beam, left leg, and center leg (P_{c1}, P_{c2}, P_{cm}) are lumped into the positions shown in Fig. 6.7. Assuming the transformer is only thermally coupled to ambient, temperatures of windings (T_s, T_p) and three points in cores (T_{c1}, T_{c2}, T_{cm}) are determined by the ambient temperature T_a, losses, thermal resistances from different loss sources, and to ambient.

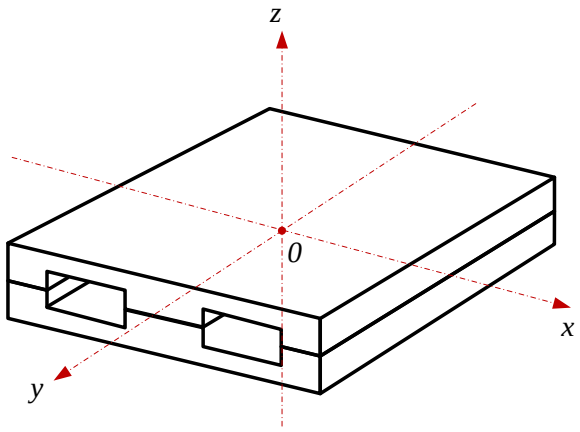
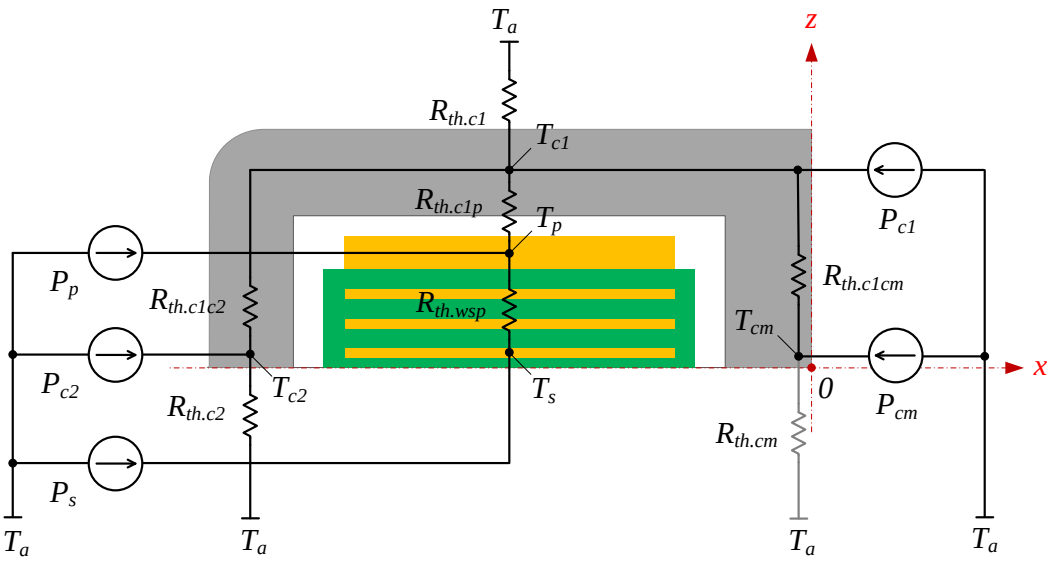


Fig. 6.6 XYZ coordinates of a planar transformer

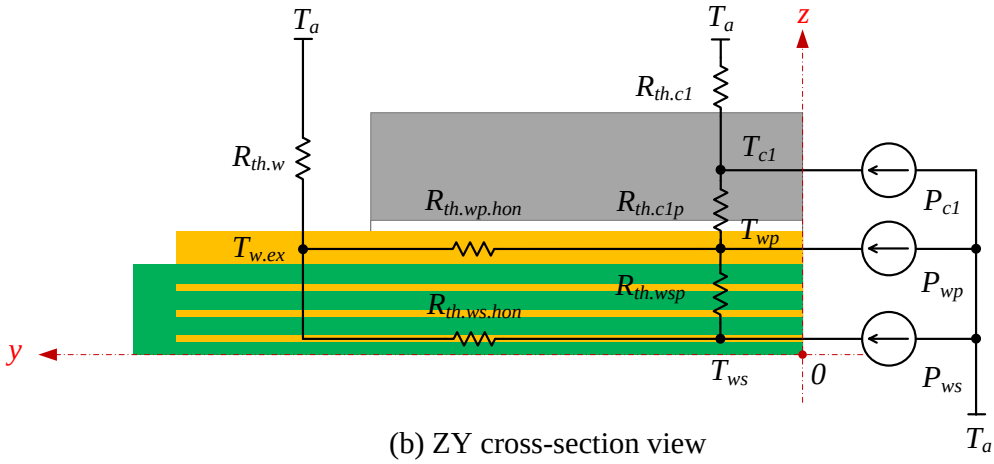
Heat Interface Design

Since wider in the XY directions and shorter in the Z direction, planar transformers bear a lower $R_{th.c1}$, $R_{th.c1c2}$ and $R_{th.c1cm}$ (labeled in Fig. 6.7) than the barrel transformers. However, large part of windings is still sealed by magnetic cores that are not so thermally conductive. This results in a relatively high value $R_{th.c1p}$, $R_{th.wp.hon}$ and $R_{th.ws.hon}$ for planar transformers. In other words, due to the enclosed structure, heat in windings is difficult to extract which consequently incites elevated winding hotspot temperatures (T_{wp} and T_{ws}), especially in high-current applications. Several heat interface designs have been proposed in literature to improve the thermal issues related to transformers:

- Attach heatsinks against core surfaces [6-8] and apply heat extractors in or around cores [6-9][6-10] in order to further decrease $R_{th.c1}$ and $R_{th.c2}$;
- Copper bar [6-11] and heat pipe [6-12] are thermally buried between cores and windings, coupling windings, and cores to external heat exchangers to reduce $R_{th.wp.hon}$, $R_{th.ws.hon}$, $R_{th.w}$ and $R_{th.c1p}$;



(a) ZX cross section view



(b) ZY cross-section view

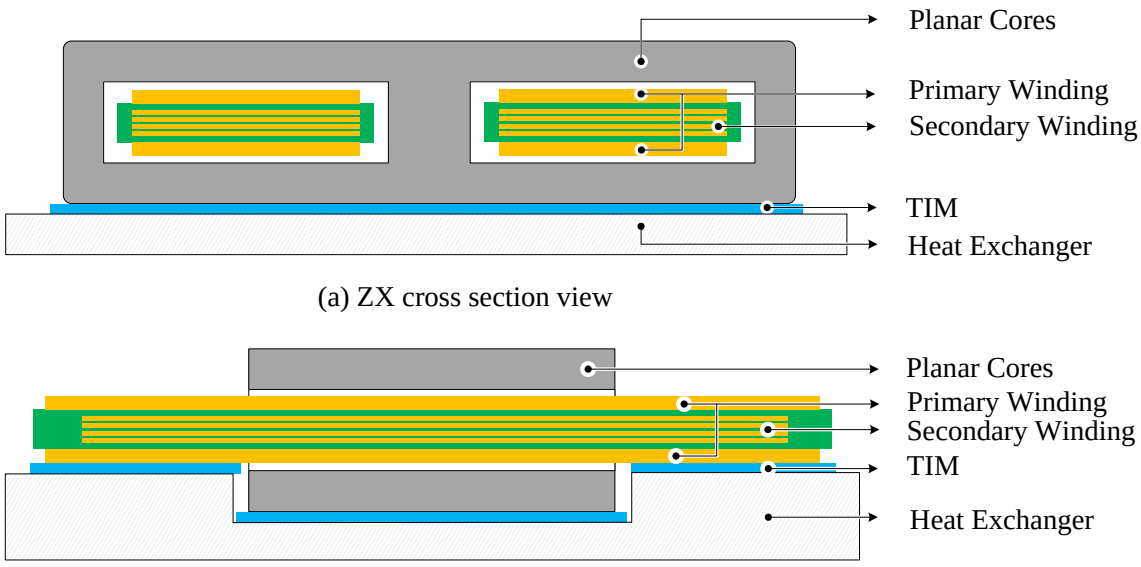
Fig. 6.7 Lumped thermal network of a planar transformer with (a) ZX cross-section view and (b) ZY cross-section view (Figures not to scale)

- Attach windings on thermally conductive substrates [6-13] to alleviate $R_{th.wp}$ and $R_{th.wp.hon}$, $R_{th.ws.hon}$.

Below, single-sided cooling for ferrite planar transformer is reviewed, and double-sided cooling is proposed for the nano-crystalline planar transformer designed in Section 5.4.

– *Single-sided cooling of ferrite planar transformer*

To extract the heat buried deeply in cores, windings are extended out of magnetic cores. The exposed winding part and cores are attached against the heatsinks with TIM layers in between. Fig. 6.8 visualizes this structure from a ZX and a ZY perspective. Here, the bottom core is situated in a cavity in the heatsink such that the exposed winding surfaces can also be attached against the cooling surface (Fig. 6.8b). Due to the sufficient exposed surface area of planar cores and winding, this method reduces $R_{th.c1}$ and $R_{th.w}$ (Fig. 6.7). Flexible TIM layers are placed between heat exchangers and the transformer surface for a sound thermal contact and electrical isolation.



(a) ZX cross section view

(b) ZY cross-section view

Fig. 6.8 Single-sided cooling heat interface design of ferrite planar transformer in (a) ZX and (b) ZY cross-section view in Fig. 6.6(Figures not to scale)

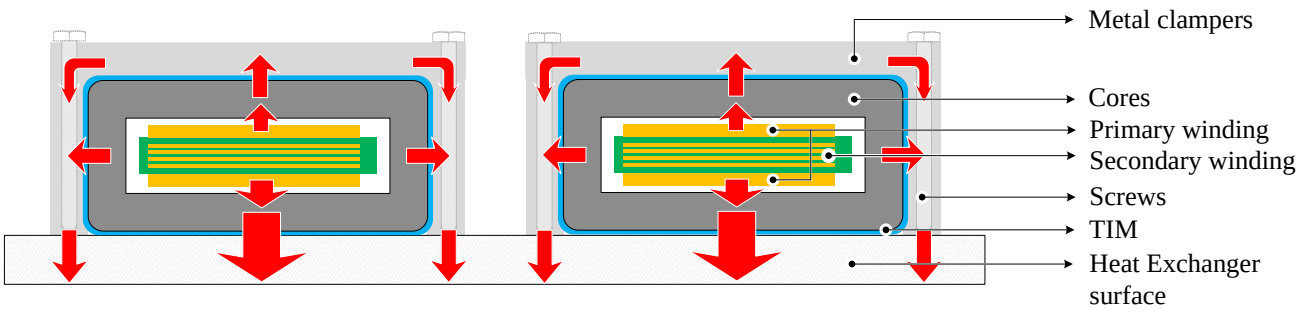
– *Nanocrystalline Planar Transformer*

Nanocrystalline magnetic material is known for higher saturation flux density and lower core loss at the same flux density, compared with ferrites. A nanocrystalline planar transformer proposed in Chapter 5 is employed to minimize loss in high-current applications. Several design efforts are conducted to facilitate an effective cooling design:

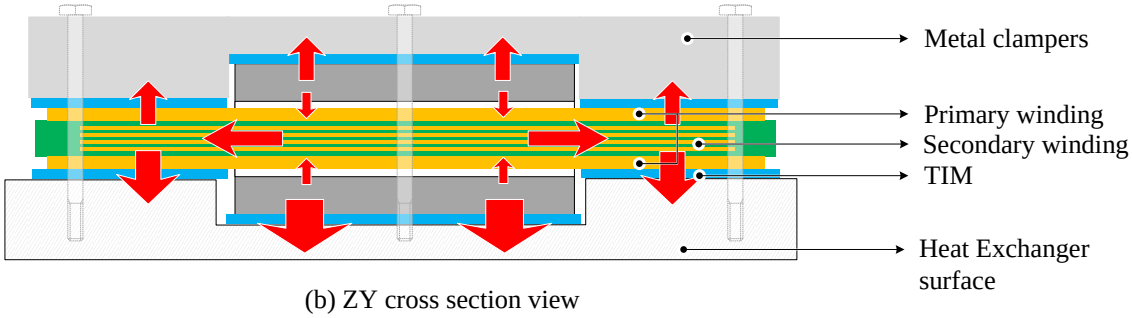
1. Separated C-shaped core sets. They enlarge the total core surface area for cooling compared to E-core sets.
2. Shallow core depth and big core winding window width. Cores are designed not only for minimal winding loss but also for lower thermal resistances from the internal winding hotspot to the external environment ($R_{th.wsp}$, $R_{th.wp.hon}$ and $R_{th.ws.hon}$ depicted in Fig. 6.7).
3. Double-sided cooling. Metal foils and screws can be used to wrap and clamp the entire transformer structure onto the heat exchange surface with flexible TIM layers placed in between them for better thermal contact, electrical isolation, and as a mechanical buffer. Fig. 6.9 illustrates this concept in the ZX and ZY cross-section views in coordinates of Fig. 6.6. Now, each core set has four sides to spread out heat (Fig. 6.9a), and exposed windings have both sides for cooling (Fig. 6.9b). The primary heat flows are shown in Fig. 6.9 with red arrows.

6.3 Collective Cooling Strategy

In the last section, the thermal interface design of the power semiconductor and planar magnetics has been introduced on a component level. This section will present the system-level collective cooling concept of low-profile PE converters, aiming at a compact cooling structure.



(a) ZX cross section view



(b) ZY cross section view

Fig. 6.9 Double-sided cooling separated C-core sets in (a) ZX and (b) ZY cross-section views in Fig. 6.6 (Figures not to scale)

6.3.1 Concept

The principle of collective cooling is to couple the most dissipative components inside a PE system with differentiated heat interfaces to one single heat exchange surface for centralized heat removal. A planar PE system structure is a favorable prerequisite. The thoughts behind this concept are:

- Taking advantage of an extensive surface area from low-profile converters, the thermal interface resistance is naturally low.
- It integrates normally localized cooling elements into one and is, therefore, able to flatten the heat exchanger structure. As a result, the waste air is squeezed out from the system, and the cooling system becomes more compact.
- Coupling bulky magnetic components with the collective heat exchanger assists in reducing temperature. For high-current transformers, thermally coupling the high-current windings with heat exchangers is important.
- A collective heat exchanger with a wide surface can be employed as a mechanical function.

To explain this concept, a high-current DAB converter is considered as an example. The dominant heat generators in a DAB are the transformer, LV, and HV semiconductor bridges while losses in capacitors, control, and semiconductor drivers are considerably less. The collective cooling concept of such a DAB is represented in Fig. 6.10. With the heat interface design introduced in the previous section, semiconductor bridges and transformers are thermally cou-

TABLE 6.1 MAIN COMPONENTS USED IN 1 KW DAB CONVERTER

Components	Packaging	Main Ratings
MOSFET Modules (×2) (LV side)	SK300MAA055T package; Semitop3 from Semikron.	Die: SUM110N06-04L; 60V, 110A, Vishay; 3 in parallel at each switch position.
IGBT Module (×1) (HV side)	SK80MD055 package; Semitop2 from Semikron.	Die: SKW30N60HS; 600V, 30A, Infineon; 1 at each switch position.
Planar Transformer	EE 65/50/5 Copper foil + Litz wire	Material: 3C90 ferrite Design details seen in Table 5.3 (Planar transformer II).
Input capacitors	EEUFC1V152 (D18 ×L20)	35V, 1500 μF, ×8, Panasonic
Output capacitors	EETED2G151JJ (D25 ×L30)	400V, 150 μF, ×4, Panasonic

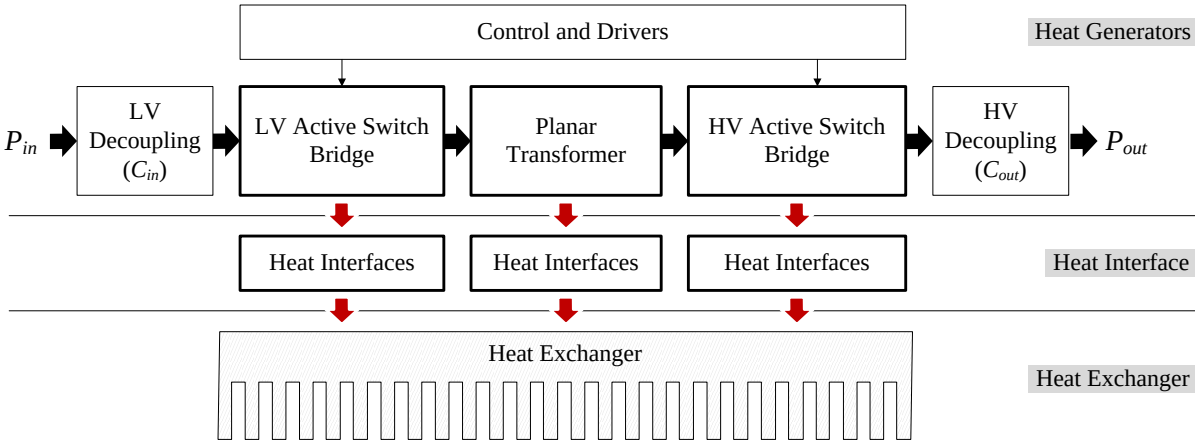


Fig. 6.10 Collective cooling concept of high-current DAB converter (black and red arrows means electrical and thermal power, respectively) (figures not to scale)

pled to a common heat exchanger cooled with forced air or liquid. A 1 kW DAB converter has been constructed to demonstrate this concept and is presented below.

6.3.2 Experimental Demonstration

The applied DAB transfers 1 kW power from a 12V battery (10 V~15 V) to 350V (300 V~ 450 V) load. The details of main power components selected and designed are summarized in TABLE 6.1. Semitop modules from Semikron are selected for containing the LV and HV switch bridges due to their highly integrated solution and low thermal resistance. Note that different semiconductor dies are implanted into the modules: MOSFET dies from Vishay and IGBT dies from Infineon are deployed for LV and HV bridges, respectively. This integrated module solution realizes a low profile as well as a compact and thermally superior structure. The planar transformer II designed in Section 5.3.3 is used here.

Mechanical Structure

In accordance with the collective cooling concept illustrated in Fig. 6.10, the DAB converter is developed. Fig. 6.11 depicts the mechanical structure with only the main power components involved. This converter utilizes PCB with FR4 material as the substrate on which all

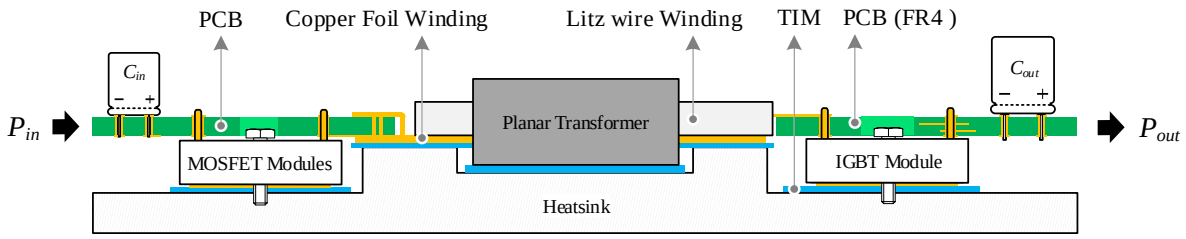


Fig. 6.11 Cross-section view of collectively cooled 1 kW DAB converter (Figures not to scale)

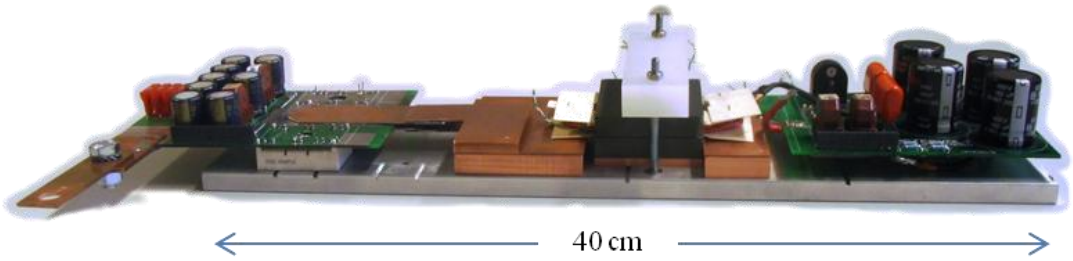


Fig. 6.12 1 kW DAB prototype photo

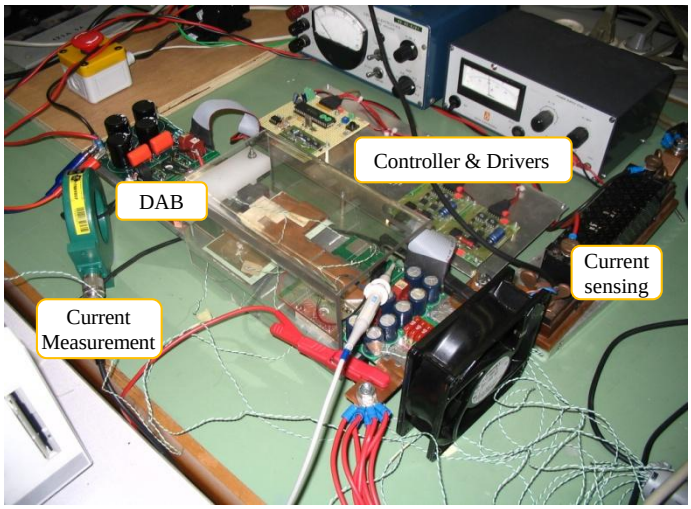


Fig. 6.13 Measurement setup of 1 kW DAB

components in the power stage are mounted. The converter structure is designed such that the dominant heat generators, i.e. semiconductor modules, transformer core, and windings, are all directly coupled with a low-profile fin-less heatsink plate that is stretched out to cover the entire converter structure:

Thin TIM layers are inserted between power components and the heatsink for effective thermal contact and electrical isolation. The prototype picture of this DAB and measurement setup are illustrated in Fig. 6.12 and Fig. 6.13, respectively.

Measurement results

The measured losses of MOSFET modules, the IGBT module, and the planar transformer at nominal operating condition (12V~350V, 1 kW) are provided in Fig. 6.14. The efficiency and temperature measurement under natural and forced convection conditions are also measured

TABLE 6.2 TEMPERATURE AND EFFICIENCY MEASUREMENTS

12V/350V/ 1 kW DAB	Test Conditions	η [%]	MOSFET Modules [^{o}C]	IGBT Module [^{o}C]	Sec. winding [^{o}C]	Pri. Foil winding [^{o}C]	Core [^{o}C]
Planar Transformer II	Forced convection + Collective cooling	92	68.5	57.8	60.6	55.1	55.5
Planar Transformer II	Natural convection + Collective Cooling	91.4	88.2	72.2	73.3	78.0	69.0
Planar Transformer I	Natural convection without collective cooling	90.2	88.0	66.7	124.4	102.0	88.0

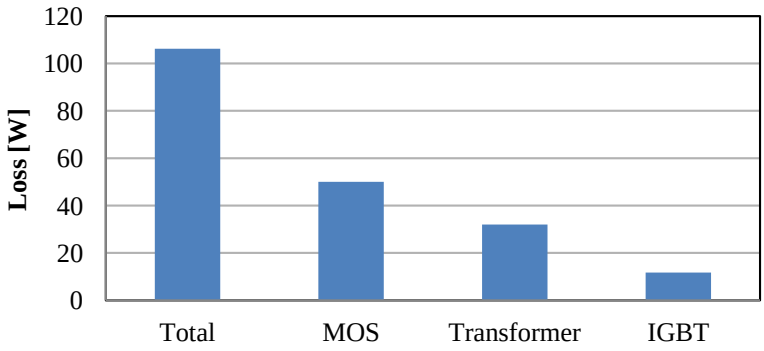


Fig. 6.14 Loss distribution in the DAB prototype at nominal condition (12 V/350 V, 1 kW)

and demonstrated in TABLE 6.2. As a comparison, the measurement results of the DAB with planar transformer I (TABLE 6.2) are also given. Note that planar transformer I is not thermally coupled with the heatsink.

It can be found from the converter structure and measurements that:

- Although without fins, the deployed long heatsink plate has sufficient cooling area to maintain the critical temperatures low, even with natural convection. This low temperature level implies that the converter can potentially be decreased in size (e.g. the exposed winding area can be reduced) or is able to manage additional power.
- In addition to the thermal function, the heatsink also mechanically supports the entire converter.
- Planar transformer II (Litz wire as the HV winding) and collective cooling overcomes the extremely high temperature in planar transformer I (PCB tracks as the HV winding).

6.4 Double-Sided Collective Cooling (DSCC) Design

Due to an intrinsically significant aspect ratio, the cooling surface area of low-profile structures is relatively expansive. The thermal interface resistance will be substantially reduced if the heat can be extracted from both sides of this structure. As a result, power-handling capability will be increased. DSCC strategy has been applied to high power semiconductor modules [6-14][6-15] where large, thin semiconductor dies facilitate the heat extraction. Similarly,

TABLE 6.3 SPECIFICATION OF 2 KW DAB CONVERTER

Steady State	
Battery (input) Voltage V_i	24 V (20 V ~ 32 V)
Bus (output) Voltage V_o	360 V (300 V ~ 450 V)
Nominal Load $P_{o.nom}$	2 kW
Transient State	
Battery (input) Voltage V_i	20 V ~ 24 V
Bus (output) Voltage V_o	360 V
Load in transient state I	10 kW (5 sec)
Load in transient state II	5 kW (30 sec)

a low-profile converter structure equipped with a large and flat accessible surface area also presents an important prerequisite condition for a double-sided cooling design on the system level. This cooling approach utilizes parts that not only extract the heat from two large and flat sides of the planar structure but also mechanically supports and packages the system. As a heat removal management approach, double-sided cooling actually integrates mechanical and thermal functions into one structure which is potentially able to boost system power density.

This section will investigate the DSCC strategy for a high-current low-profile DAB converter aiming at high power density. The main specification of the DAB employed as the carrier has been described in Chapter 5 and is relisted below in TABLE 6.3. Note that the peak load (10 kW) lasts for 5 seconds at start-up in order to start the diesel engine which also presents the worst thermal load to the electronic system. Three modulation methods described in Chapter 4 will be implemented for this DAB to minimize heat generation. According to the system analysis conducted in Chapter 5, the switching frequency is fixed at 50 kHz for this DAB design.

Since this DAB is designed for marine vehicles, a novel seawater based cooling plate is proposed [6-16] by Gutierrez- Alcaraz to circulate the coolant with almost infinite thermal mass around the cooling system. The DAB converter will be attached against one side of this cooling plate. The cascaded bus capacitors and the DC-AC converter to drive the electric motor are placed against the other side.

In Section 6.4.1, the DAB converter is optimized from heat generation perspective including the optimal number of paralleled LV and HV MOSFETs, the optimal operating range of three different modulation methods. The calculated component losses will be the inputs to the subsequent thermal simulation. The DSCC design is presented in Section 6.4.2, and thermal simulation of the design is performed in Section 6.4.3. Discussions of this DSCC design are provided in Section 6.4.4.

6.4.1 Heat Generation Management

Heat generation management is conducted as the first step to:

- Minimize loss in a cost-effective manner.
- Select and/or design the component packaging to facilitate the cooling design in the next step.

Since power semiconductors and the transformer handle enormous amounts of current in the given specification, LV and HV MOSFETs and transformer design are concentrated on in the following discussion.

LV-MOSFET

Two key performance requirements are primarily considered when selecting an appropriate LV MOSFET:

- Ultra low on-state resistance (R_{dson});
- Planar and thermally advantageous packaging.

DirectFET-L8 packaged MOSFET (IRF7749L2PbF, 60V) is targeted as the option for the LV MOSFET due to its 1 mΩ R_{dson} and ultralow thickness with novel double-sided cooling capability. Several units should still be placed in parallel to manage the high current and distribute the loss geometrically.

Based on the loss model proposed in Chapter 4, loss in the LV MOSFET is modeled according to different operating conditions and modulation methods. Fig. 6.15(a) plots the total LV MOSFET loss as a function of a number of paralleled units, rectangular and trapezoidal modulation methods at a nominal operating point, and Fig. 6.15(b) shows the loss in a single

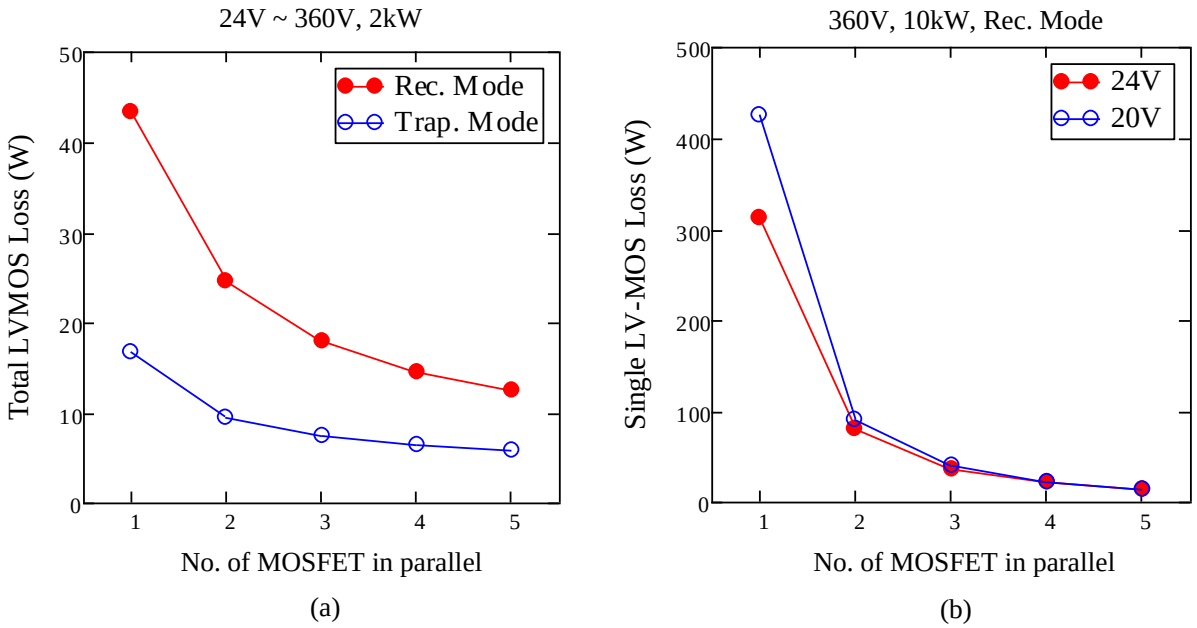


Fig. 6.15 (a) Total loss in LV MOSFETs at nominal condition (24V~360V, 2 kW) with rectangular and trapezoidal modulations and (b) loss in single LV MOSFET at 360V and 10 kW with rectangular modulation

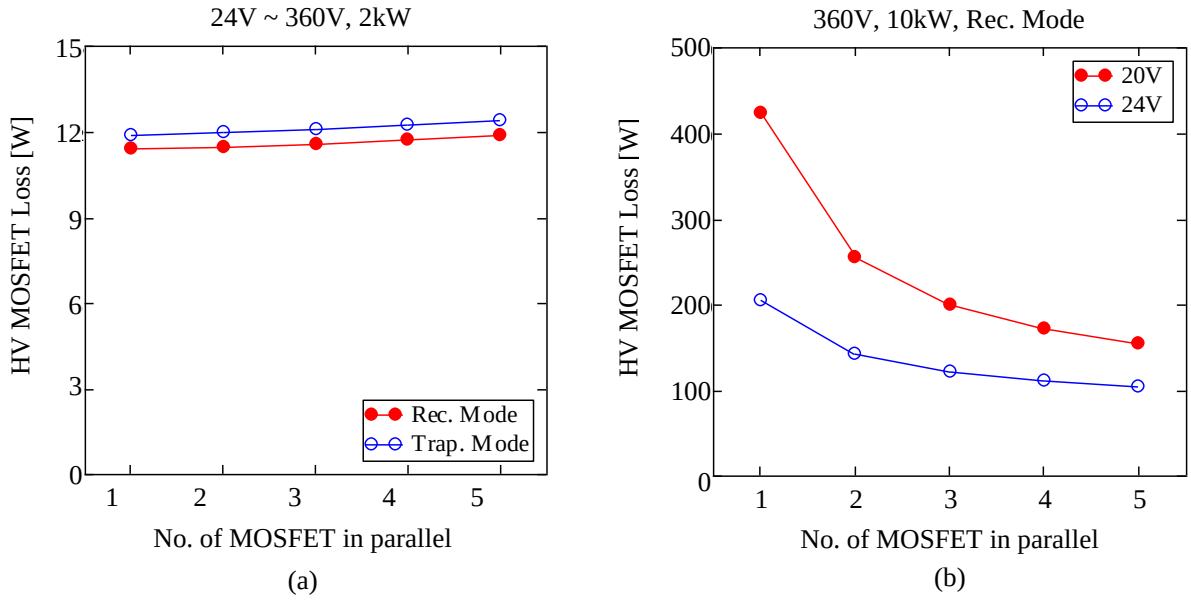


Fig. 6.16 (a) Total loss in HV MOSFETs at nominal condition (24V~360V, 2 kW) with rectangular and trapezoidal modulations and (b) loss in single HV MOSFET at 360V and 10 kW with rectangular modulation

MOSFET at 10 kW peak load with rectangular modulation. It can be from Fig. 6.15 that three LV MOSFETs (IRF7749L2PbF) can be considered as the most economic option. This is because the three paralleled units at each switch position significantly decrease loss, however, any additional paralleled units do not reduce loss much more.

HV MOSFET

Surface mounted D^2PAK packaging is selected for HV MOSFET due to its low thermal resistance compared with other HV SMD discrete devices and low-profile structures. 600V IPB60R099CP is used considering the current rating and relatively fast switching speed. Fig. 6.16(a) plots the modeled total HV MOSFET loss as a function of the number of paralleled units, rectangular and trapezoidal modulation methods at a nominal operating point, and Fig. 6.16(b) shows the loss in a single MOSFET at 10 kW peak load with rectangular modulation. Two units in parallel is confirmed as the best option in terms of loss and cost.

Planar Nanocrystalline Transformer

The proposed design has been described in detail in Chapter 5. It is aimed to:

- Minimize the transformer loss in high-current applications;
- Increase the cooling surface area;
- Integrate the required leakage inductance in the structural design.

Table 6.4 summarizes the key power component parameters. Schematics of the power stage and control/drive stage are attached in Appendix C.

Modeled System Loss

Triangular and trapezoidal modulation methods are applied at ≤ 5 kW load. Fig. 6.17(a) and (b) plot the system loss at 2 kW and 5 kW in 2D and 3D methods according to the DAB loss

TABLE 6.4 MAIN POWER COMPONENTS USED IN 2 KW DAB CONVERTER TO BE DESIGNED

Main power components	Details	Typical Rating	Package
LV MOSFET	IRF7749L2PbF ×3	40V, 200A	DirectFET/L8
MV MOSFET	IPB60R099CP ×2	650V, 31A	D^2PAK
Planar Trans-former	Nanocrystalline FT-3M FR4 PCB with copper tracks as windings	N_s: N_p = 1:16, L_{lk} = 15 µH Copper thickness: 6 oz 6 layers	Design seen in Fig. 5.34.
input capacitors	16 in parallel	50 V, 10 µF, X7R	SMD 2220 (AVX)
output capacitors	16 in parallel	600V, 0.22 µF, X7R	SMD 2225 (AVX)

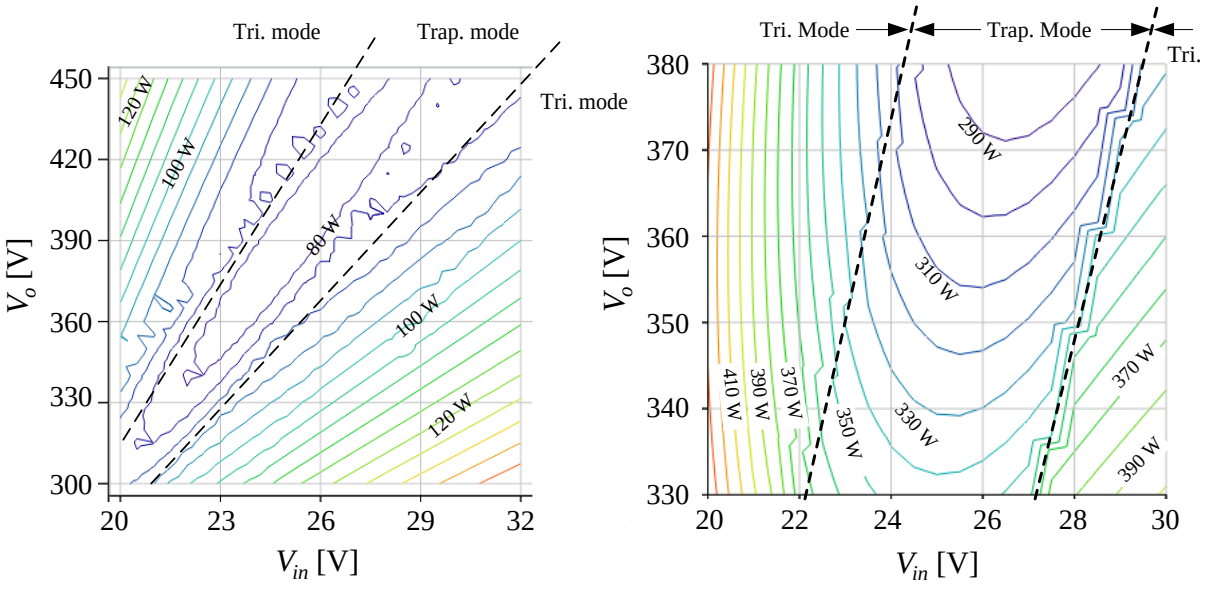


Fig. 6.17 Plots of DAB loss at 2 kW (a) and 5 kW (b) with triangular and trapezoidal modulation methods

model where the modulation method and its operating range that generate less loss than the others are identified. System efficiency at 2 kW and 360 V output is plotted in Fig. 6.18 as a function of input voltage where modulation with high efficiency is indicated. This efficiency curve indicates the system performance at the nominal condition.

Rectangular modulation is implemented at 10 kW due to its high power transfer capability compared with the other two. A modeled system loss map across the full input and output voltage ranges is plotted in Fig. 6.19 which indicates the system loss at the peak power. Note that the specified worst transient thermal condition occurs at V_{in} = 20 V and V_o = 360V.

Loss Distribution

Component losses under peak power should be well known since the cooling structure should have been designed accordingly to address the worst thermal condition in order to keep the component temperature rises low enough. Modeled loss distribution at the worst thermal condition (20V~360V, 10 kW) is estimated in Fig. 6.20. It can be found that the transformer windings and the MOSFETs are the most significant heat contributors where conduction loss

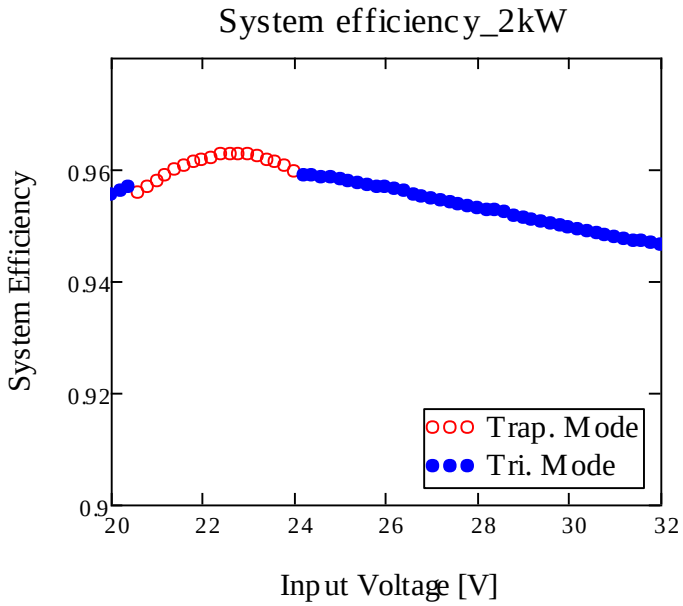


Fig. 6.18 Modeled system efficiency at 2 kW with trapezoidal and triangular modulations

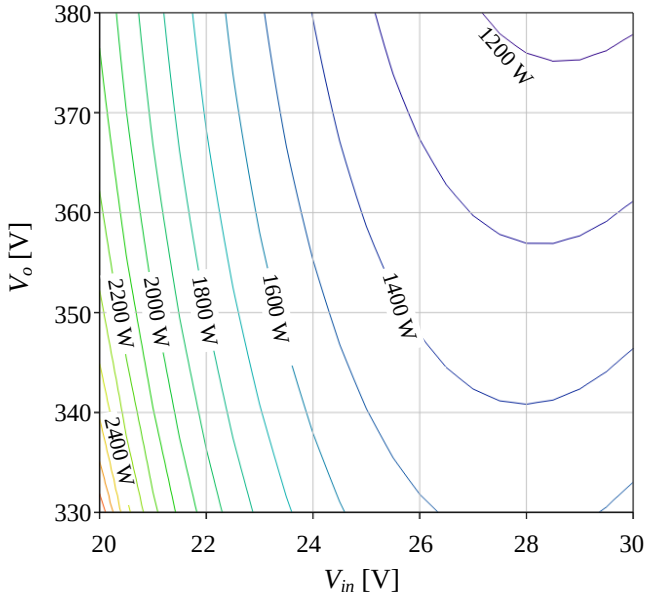


Fig. 6.19 Modeled system loss at 10 kW with rectangular modulation

is more dominant over other loss generation mechanisms. The total loss in parasitic components is also noticeably high, which includes loss in the input fuses, PCB traces and high-current connectors.

Heat generation management controls the loss to an advantageous level. However, heat removal management should be conducted such that the critical temperature in the system is controlled below a certain level to guarantee sufficient system lifetime. This is addressed in the next section.

6.4.2 Heat Removal Management

Many approaches [6-17][6-18][6-19] are available to estimate the lifetime of an electronic system based on the electrical stress, temperature, reference failure data, and acceleration fac-

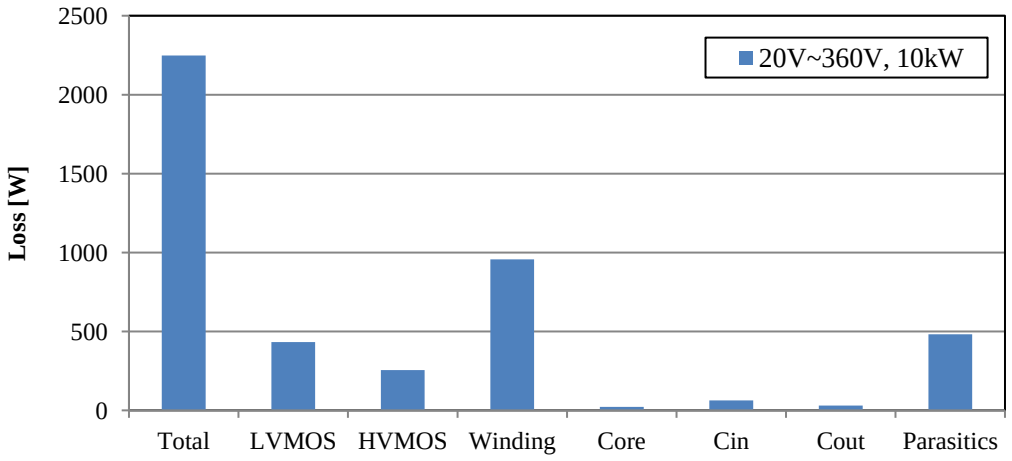


Fig. 6.20 Modeled loss distribution in 10 kW DAB converter

tors. Since lifetime specification is not given, a rule of thumb is targeted for a DAB to be designed: control the junction temperature of semiconductors 20°C below the maximum allowed value ($T_{j.max}$) given in a datasheet in any operating conditions.

Mechanical Structure

– *Power Stage*

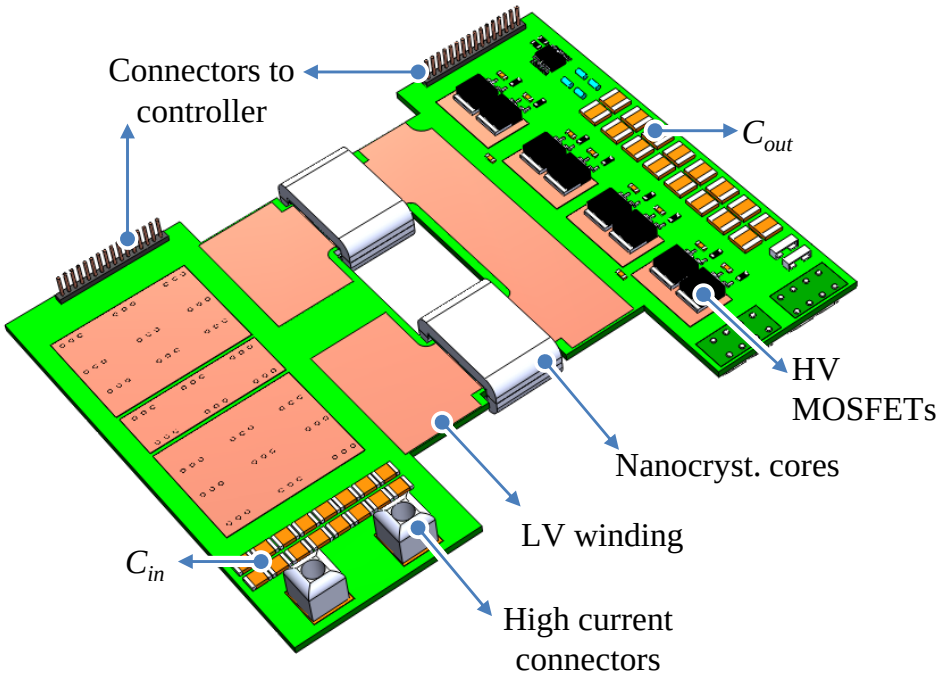
To realize the planar system structure, a PCB with FR4 material is deployed as the circuit substrate. For conduction loss reduction that is crucial for such a high current application, six-layered PCB with 6 oz (≈ 0.21 mm) copper thickness in each layer is designed.

The planar nanocrystalline transformer designed in Chapter 5 is located in the middle part in a PCB structure. Low-voltage (battery side) and high-voltage (bus side) parts are arranged on each side of the transformer. LV-MOSFETs are directly soldered onto the high current winding on the PCB side facing the cooling plate (down side) and dispersed evenly over the surface. HV-MOSFETs are placed on the other side of the PCB with a 20 mm x 15 mm copper plane beneath each of two MOSFETs for heat spreading. Connectors from the two voltage sides to the controller board are situated on the edge of the PCB. These connectors contain the PWM signals and sensing signals. High-current connectors with press-fit [6-20] are utilized to reduce contact resistance with the PCB. 3D model and prototype pictures of the power stage of this DAB are illustrated in Fig. 6.21 and Fig. 6.22.

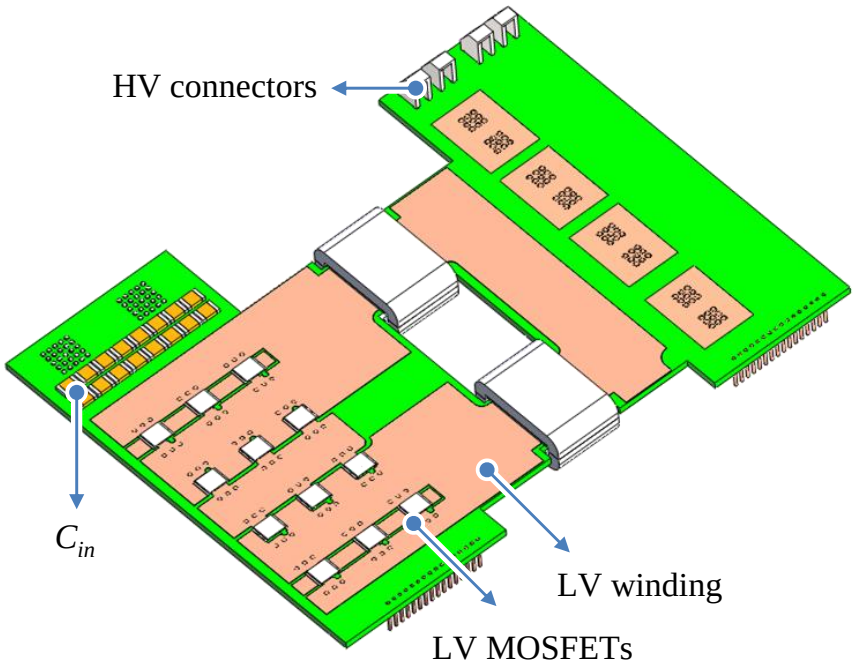
– *Packaging*

Two flat copper clamps are designed to mechanically clamp and fix the power stage in between. Since the power structure is equipped with large flat surface area on both sides, two more copper clamps are produced to maximize the contact area with the transformer windings on the top side of the LV MOSFETs and the PCB surface. The thickness of two clamps is 5 mm. The top side clamp has 5 mm wide legs on the edges. These legs connect two clamps together so that heat from the top clamp can be conducted to the bottom clamp. Several holes are drilled on the legs through which M3 screws are used to attach the entire structure onto

the seawater cooling plate. Flexible TIM films (5000S35, [6-21]) of 0.5 mm thickness are placed between the clamps and the power stage for effective thermal contact and electrical isolation. An exploded and complete view of the system structure are shown in Fig. 6.23 and Fig. 6.24, respectively. Similar clamps are used to wrap the transformer core sets from four sides with the same TIM film. The cores are also fixed to the cooling plate with M3 screws.

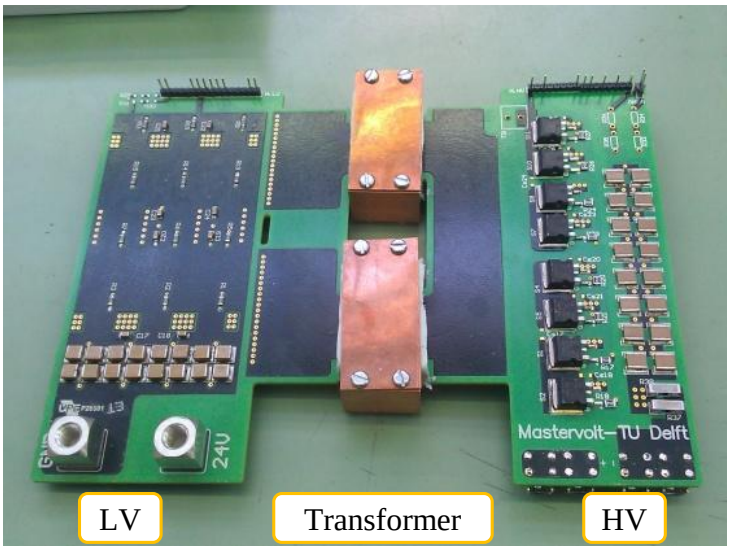


(a)

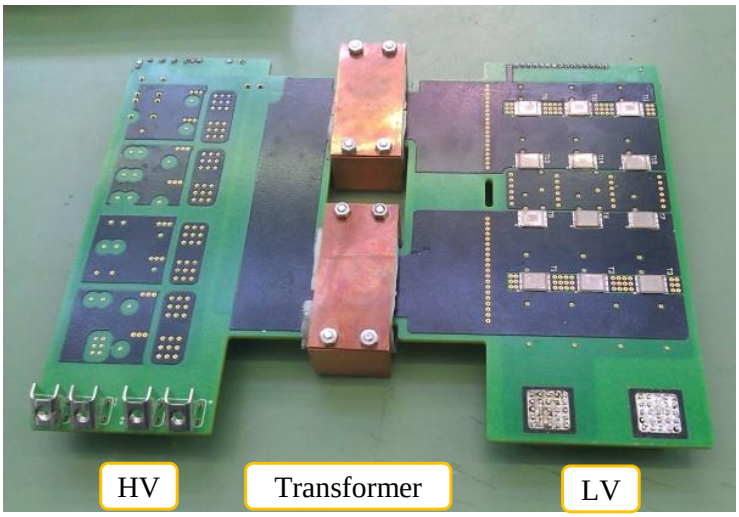


(b)

Fig. 6.21 3D model of 2 kW DAB power stage without copper clamps and isolated material (a) top side and (b) bottom side

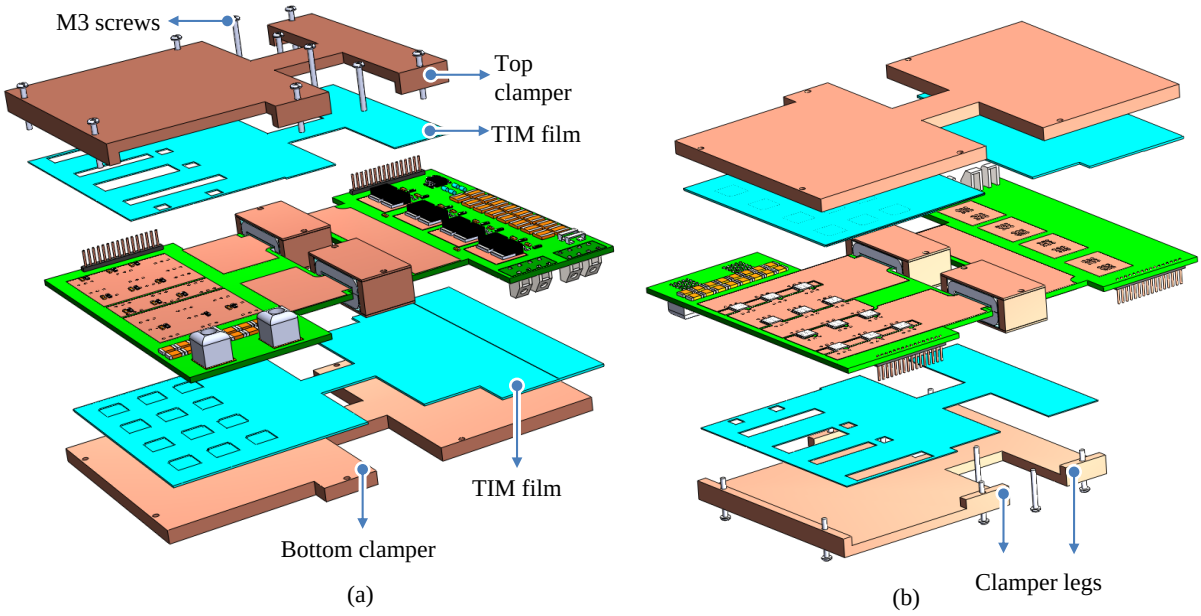


(a)



(b)

Fig. 6.22 Picture of 2 kW DAB power stage (a) top side and (b) bottom side



(a) (b)

Fig. 6.23 Exploded view of 2 kW DAB converter with DSCC
(a) top side and (b) bottom side

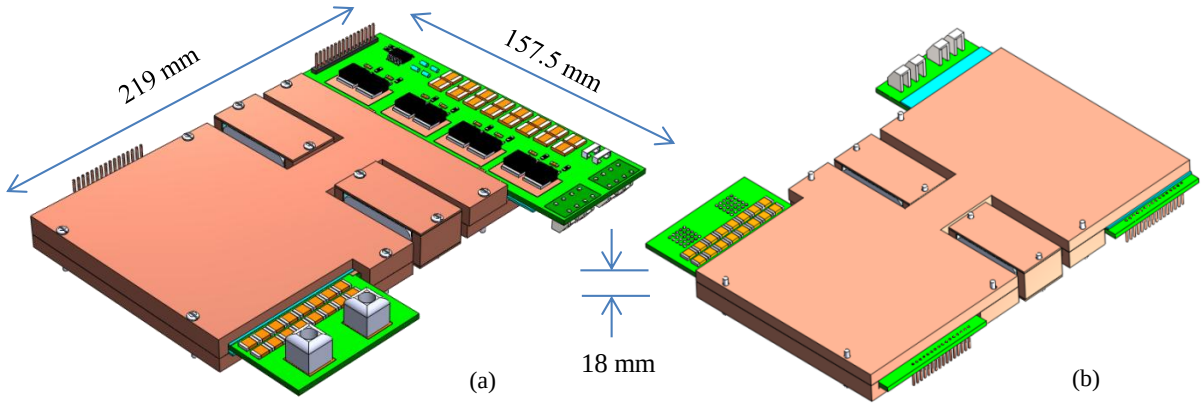


Fig. 6.24 Complete DAB converter with DSCC (a) top side and (b) bottom side

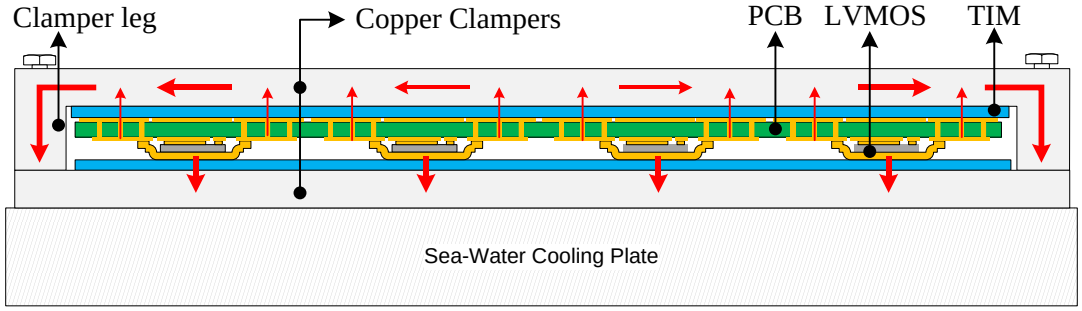


Fig. 6.25 Cross-section view of thermal structure of LV MOSFETs (DirectFET package)

Thermal Structure

– *LV MOSFET*

The DirectFET package provides two heat paths and facilitates heat removal management with one more direction to extract heat. The component-level heat interfacing design illustrated in Fig. 6.4(d) is deployed here: the top side of DirectFET package is pushed against the bottom clamp while thermal vias are placed around the MOSFETs on the PCB which are pressed against the other clamp. The cross-section view of the LV MOSFET thermal structure on the system level is depicted in Fig. 6.25 where the heat flow is denoted by red arrows. The heat spreading to the top clamp is conducted back to the cooling plate from the clamp legs.

– *HV MOSFET*

Thermally interfacing D^2PAK from the PCB to the cooling surface has been described in Fig. 6.4(c). Keys to success are the copper planes beneath the MOSFET and on the other side of the PCB that spread heat and through-hole thermal vias that significantly reduce thermal interface resistance. In this context, 9 vias with 0.7 mm diameter are placed beneath each HV MOSFET. TIM film is clamped between the PCB and the bottom clamp.

– *Planar Nanocrystalline Transformer*

The cooling structure of magnetic cores has been described in Fig. 6.9(a). High-current transformer windings are designed with a large area that are extended out of cores, which results in

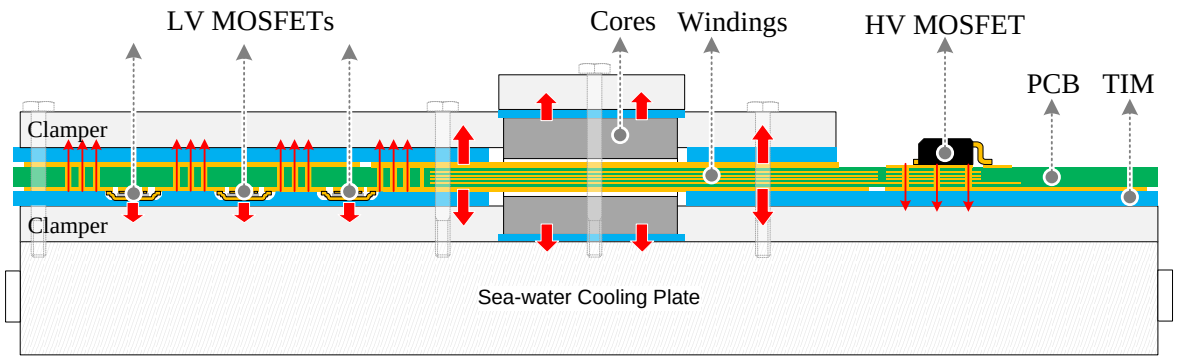


Fig. 6.26 Cross-section view of thermal structure of 2 kW DAB converter (figure is not to scale)

a significant contact area with clamps on the two sides of the PCB. This helps to decrease the $R_{th.w}$ labeled in Fig. 6.7(b). Cores are designed to be shallow in depth which also enables the moderate $R_{th.wp.hon}$ and $R_{th.ws.hon}$ labeled in Fig. 6.7(b).

A side cross-section view of entire system is illustrated in Fig. 6.26 in which the heat flow of main power components is illustrated with red arrows. The heat extracted to the top clamp is conducted back to the cooling plate from the clamp legs.

6.4.3 Thermal Simulation

Thermal simulation is performed with Finite Element Method (FEM) package ANSYS workbench to calculate the temperature profile over the entire converter structure during the transient states. The goal of FEM thermal simulation is to check whether critical semiconductor temperatures are below the limits at the worst thermal condition.

Load Profile

The load profile for thermal simulation is depicted in Fig. 6.27. At engine start-up, the DAB converter sinks 10 kW power from the battery in the first five seconds (transient state I), and 5 kW follows for 30 seconds as the transient state II. Following these two states, the DAB continuously transfers 2 kW to the load. During the two transient states, the worst thermal condition occurs at the lowest battery voltage of 20 V due to the higher input current that is required.

Loss Distribution

The modeled losses in the main heat generators during the two transient states are given in TABLE 6.5. It can be found that LV and HV MOSFETs and transformer windings experience significant loss during the 10 kW transient state.

Main material parameters and Settings

The main material parameters required in the transient thermal simulation are listed in TABLE 6.6. Contact thermal conductance of TIM (5000S35)-to-copper and copper-to-copper at approximately 50 N/cm^2 are measured around 10 kW/(m^{2}K) and 25 kW/(m^{2}K). The natural

TABLE 6.5 LOSS DISTRIBUTIONS IN MAIN POWER COMPONENTS DURING TWO TRANSIENT STATES

Main Heat Generators (24V~360V)	Loss [W]	
	Transient State I	Transient State II
LV-MOSFETs	430 (total) 35.8 (each)	79.6 (total) 6.6 (each)
HV-MOSFETs	248 (total) 31 (each)	57 (total) 7.1 (each)
Transformer cores	22.7	22.7
Transformer windings	930	145.3
Input capacitors	58.6	8.3
Output capacitors	28.5	3.6

TABLE 6.6 MATERIAL PROPERTIES USED IN THE THERMAL SIMULATION

Material	Density [g/mm^3]	Thermal Conductivity [W/m/K]	Specific heat [J/g/K]
FR4 (PCB)	1.9	1(X) / 1(Y) / 0.3 (Z)*	0.6
Copper	8.3	401	0.385
FT-3M	7.3	9	0.5
TIM (5000S35)	3.6	5	1

* Thermal conductivity of FR4 lamination is orthotropic in three directions (X,Y are in-plane directions and Z is perpendicular to the plane).

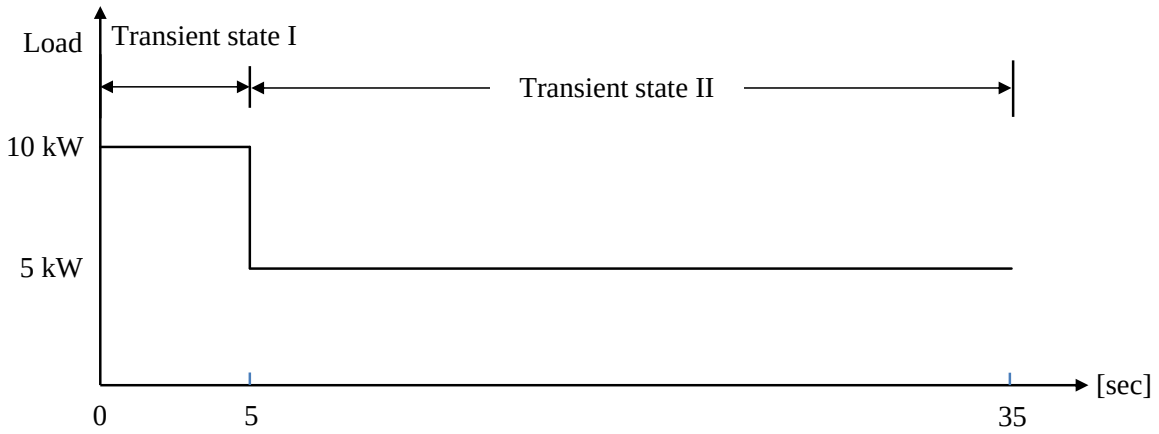


Fig. 6.27 Load profile for transient thermal simulation

convection coefficient and radiation emissivity are specified at 5 W/(m^{2}K) and 0.9, respectively. Due to the infinite thermal capacitance of sea water circulating in the cooling plate, the temperature of the bottom clamp surface to the cooling plate are assumed to be 45^{o}C in the worst case scenario as a requirement for the cooling plate design. Considering all of the information presented above, an FEM transient thermal simulation is performed with ANSYS workbench.

Simulation Results

The FEM simulated temperature profile of the entire converter at the end of transient state I is exhibited in Fig. 6.28. The case temperatures of LV and HV MOSFETs are plotted in Fig. 6.29. From the simulation results, it can be observed that:

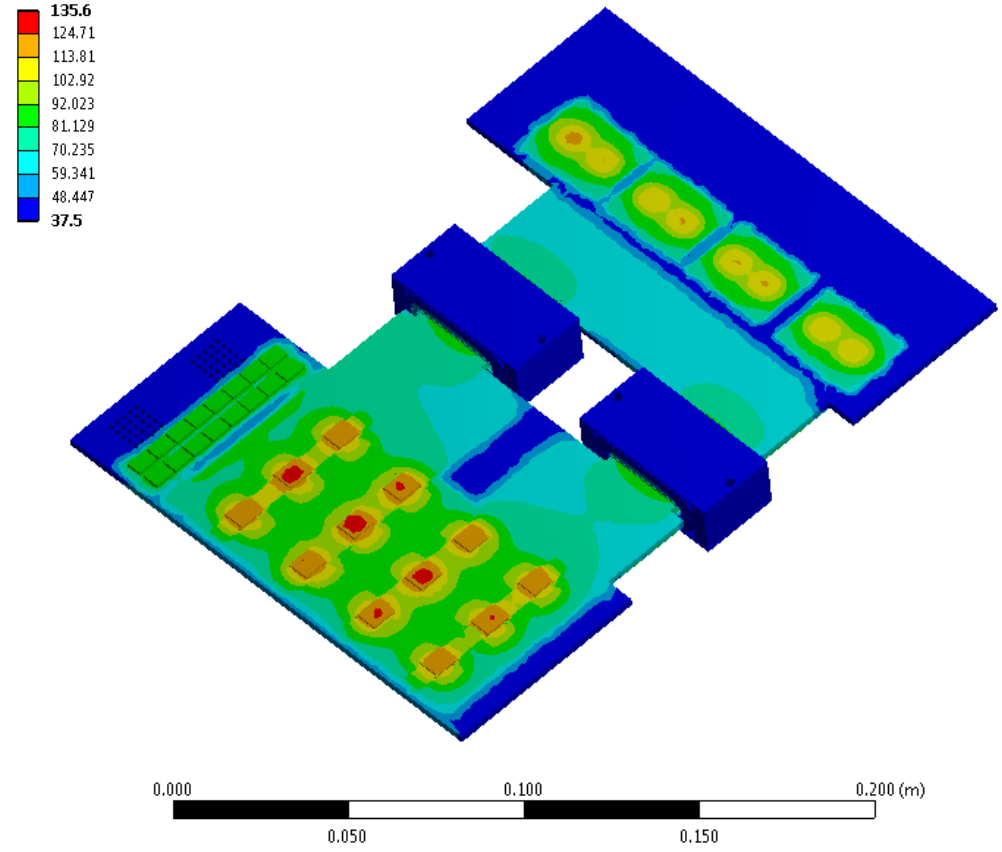
- All components reach the highest temperature at the end of transient state I whereby the power semiconductors are the hottest.

- Semiconductor temperatures are controlled below the limits. At the end of transient state I, the case temperatures of LV and HV MOSFETs are 128 ^{o}C and 122 ^{o}C, respectively. Assuming the thermal time constants of MOSFET packages are negligibly short and according to the case-to-junction thermal resistances of used semiconductor packages, the junction temperature of LV and HV MOSFETs are approximately 141 ^{o}C and 126 ^{o}C, respectively. Considering the maximum allowed junction temperatures ($T_{j.max}$ = 175 ^{o}C for LV MOSFETs IRF7749L2PbF) and (150 ^{o}C for HV MOSFETs IPB60R099CP), the proposed heat removal management is able to satisfy the specified thermal requirements (20 ^{o}C below $T_{j.max}$).

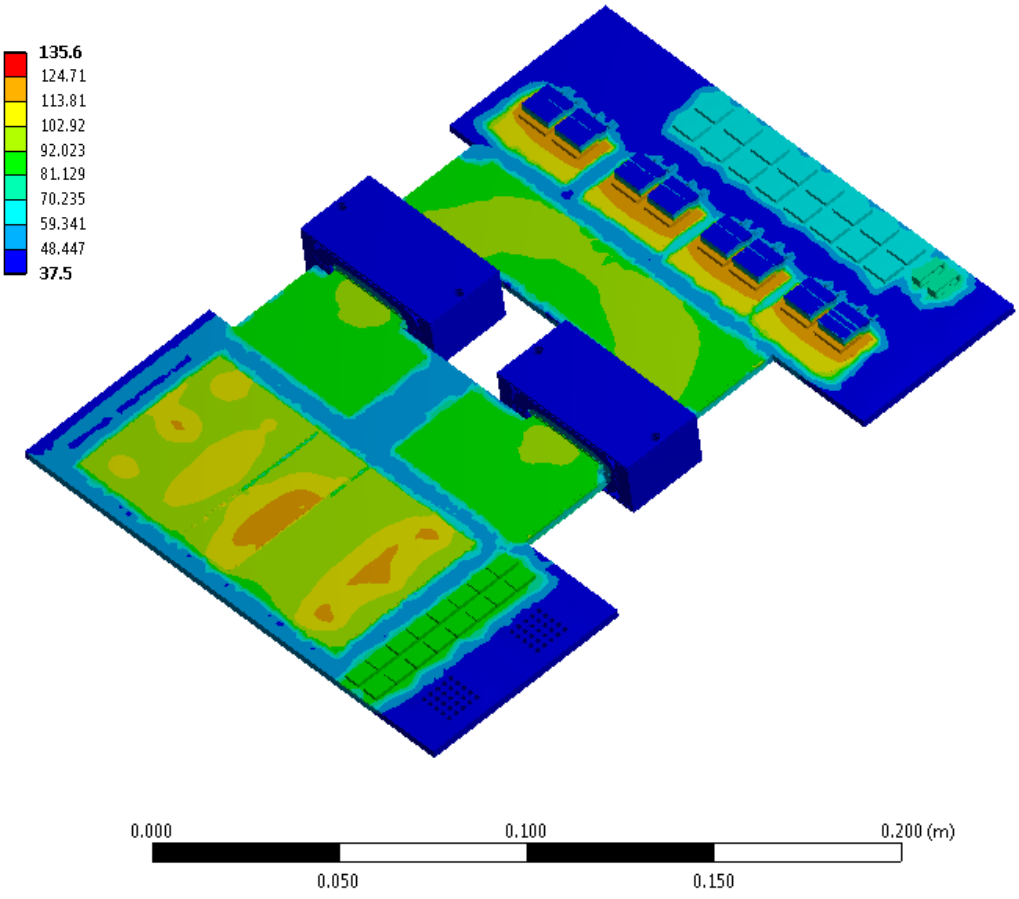
- LV MOSFETs have a much greater volume loss density than that of their HV peers, however, the junction temperature is still well controlled. This is because: 1) LV MOSFET's double thermal paths greatly lower the junction-to-case thermal resistance; and 2) The DSCC strategy effectively utilizes these two paths for low heat interface thermal resistance.

- The thermal capacitance in the system is employed to avoid the semiconductor temperature from reaching the limit during the transient state. Thermal resistances from semiconductor junctions to the cooling plate can be calculated from transient state II. At the end of transient state II, thermal steady state has been achieved where LV and HV MOSFETs arrive at 63 ^{o}C (=$T_{LVMOS.II}$) and 75 ^{o}C (=$T_{HVMOS.II}$), respectively. According to the loss in each LV MOSFET ($P_{LVMOS.II}$=6.6 W), HV MOSFET ($P_{HVMOS.II}$ =7.1W) found in TABLE 6.5, the thermal resistances from the case of MOSFETs to cooling plate are calculated as

$$R_{th.\mathrm{LVMOS\_cp}} = \frac{T_{LVMOS.II} - T_{cp}}{P_{LVMOS.II}} = \frac{63-45}{6.6} \approx 2.7\frac{K}{W}$$
$$R_{th.\mathrm{HVMOS\_cp}} = \frac{T_{HVMOS.II} - T_{cp}}{P_{HVMOS.II}} = \frac{75-45}{7.1} \approx 4.2\frac{K}{W} \quad (6\text{-}4)$$



(a)



(b)

Fig. 6.28 Simulated temperature profile at the end of transient state I (10 kW) (a) bottom and (b) top sides of the converter power stage

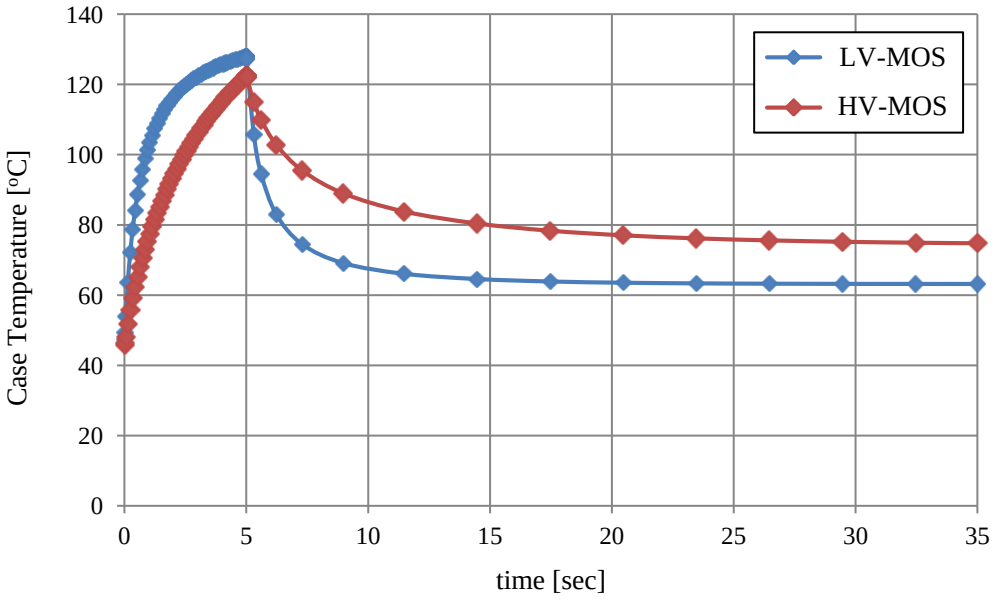


Fig. 6.29 Simulated case temperature of LV and HV MOSFETs during transient states

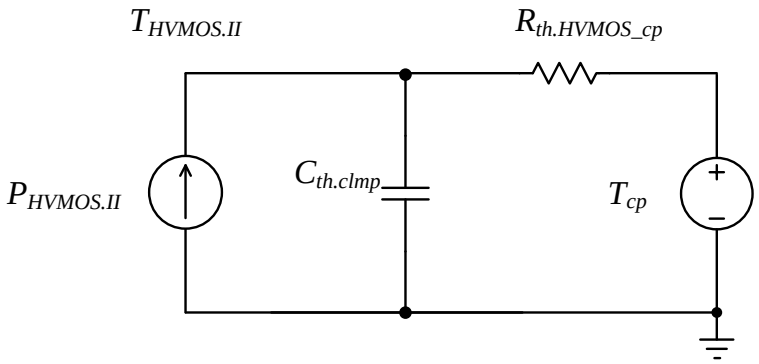


Fig. 6.30 Simplified thermal network of HV MOSFETs

With these systematic thermal resistances, if the high load condition would last for a longer period until the thermal steady state is , the case temperatures of LV and HV MOSFETs would be 141 °C and 175 °C. This level would destroy the HV MOSFET. In fact, the thermal structure of the HV MOSFET can be described by an electrical RC network as illustrated in Fig. 6.1. Since the thermal mass of the copper clamp dominates the system, the thermal capacitance of the other parts can be neglected. The thermal network of HV MOSFET can then be simplified to a 1st RC circuit as demonstrated in Fig. 6.30 where $C_{th.clmp}$ is the thermal capacitance of the bottom copper clamp. The amount of time for HV MOSFET to achieve the steady state is approximately 25 seconds. As the time constant (τ_{RC}) of the 1st RC circuit equals the time to reach 63% of steady value [6-22], τ_{RC} is estimated to be 5 seconds. Then, $C_{th.clmp}$ can be calculated as:

$$C_{th.clmp} = \frac{\tau_{RC}}{R_{th.\mathrm{HVMOS\_cp}}} \approx 1.2\ Ws/K \tag{6-5}$$

Fig. 6.31 illustrates both the 2 kW DAB prototype and 1 kW DAB with planar transformer I that are described in Section 5.3.3. With DSCC, the system power density of 2 kW DAB reaches 3.2 kW/L at the steady state and 16 kW/L during the transient state.

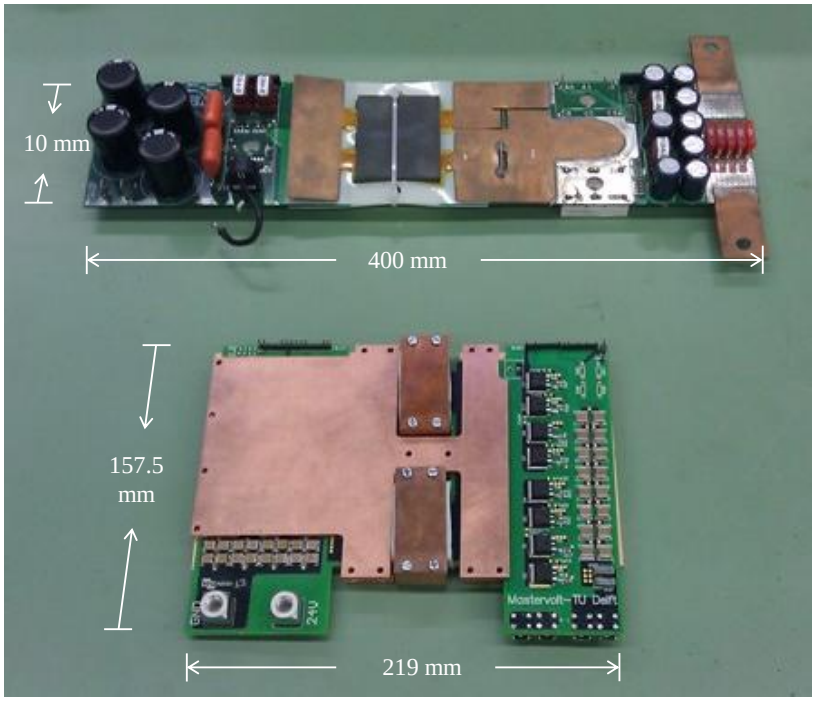


Fig. 6.31 Pictures of (top) 1 kW DAB with planar transformer I described in Section 5.3.3 and (bottom) 2 kW DAB with DSCC

6.4.4 Discussions

- The maximum junction temperature of LV and HV MOSFETs are successfully controlled below the limit by the low-profile structure and the DSCC strategy. However, power semiconductors experience a considerable temperature fluctuation from 50°C to 130°C. This substantial temperature variation will severely stress the bonding structure inside semiconductors and external solder joints on a PCB [6-23]. This may result in accelerated solder fatigue and shorten the system lifetime to an undesirable level. To suppress the temperature fluctuation, thermal resistance should be decreased or system thermal mass should be boosted.

- System thermal mass primarily concentrates in the copper clamps and the bulky cooling plate. The time constant of a plate-shaped homogeneous material can be calculated as the product of thermal resistance Eq. (6-1) and capacitance Eq. (6-2) [6-24] as shown in Eq. (6-6). It can be found that the thermal time constant is proportional to the square of plate thickness *d* but independent on the area *A*. Increased thickness will handle the more peak power within 5 seconds but whether it leads to a higher or lower power density is an interesting topic for further studies.

$$\tau_{RC} = R_{th}C_{th} = \frac{c \cdot \rho}{\sigma_{th}} d^2 \tag{6-6}$$

- In this low-profile converter structure and DSCC design, LV and HV sides will be more electromagnetically coupled due to the large surface area that LV and HV trans-

former windings have to face each other. This may potentially increase the difficulty of the EMI filter design.

- The designed DAB converter did not operate successfully before the end of this work. The insufficient soldering quality of the LV MOSFET has been found to incite system failure. The reasons include:
  - The PCB constructed for high current carrying capability has a very high copper content. Because of this large thermal mass, a proper temperature profile for soldering is difficult to control under lab conditions.
  - DirectFET hides some pins beneath its package, which makes it difficult to check the solder quality.
  - Many (12) LV MOSFETs are utilized which increase failure probability.

Manually soldering a semiconductor package such as DirectFET onto a PCB with heavy copper content is considerably not recommended in the lab environment. Professional reflow soldering equipment that is able to sufficiently control the temperature profile over such a heavy copper PCB must be employed for reliable assembly.

6.5 Conclusions

In this chapter, a collective cooling strategy has been proposed as the heat removal management approach. The aim is to achieve a compact and effective cooling function for low-current high-current DAB converters used in marine vehicle applications. The principle of this cooling strategy is to collect heat from the main power components via different heat interface designs and conduct it to a common heat exchange surface where heat is dissipated in a centralized manner. A 1 kW DAB converter is experimentally constructed to demonstrate this cooling concept. It can be found that:

- A planar converter structure facilitates a low thermal impedance heat interface design.
- The low-profile heatsink plate extends over the entire converter structure. The resultant large surface area decreases the system temperature to a significantly low level. Hence, this system has thermal margin for size reduction or handling more power.
- It helps greatly to cool the high-current transformer winding by directly coupling the part of the windings that extend out of the cores with the heat exchanger.
- The heatsink plate not only dissipates heat but also mechanically supports the entire system. It integrates both thermal and mechanical functions.

To further exploit the potential of a low-profile converter structure, the double-sided collective cooling (DSCC) strategy has been proposed in section 6.4. A high-current DAB converter with 2 kW nominal power and 10 kW transient power has been built to demonstrate this concept. Two flat copper clamps are designed to achieve the double-sided cooling, and they directly extract the heat from critical power components and the PCB surface. This DAB converter is cooled with the seawater-based cooling plate defined in [6-16]. The FEM thermal

simulation has been performed to analyze the system temperature profile during transient states. It can be found from this design that:

- The large and accessible surface area has been created by the planar structure design, including the use of low-profile MOSFET package (DirectFET), planar nanocrystalline transformer (designed in Chapter 4) and SMD D^2PAK MOSFET packages.
- DSCC strategy is able to fully utilize the large surface area on both sides of the planar DAB structure.
- The ultra-thin DirectFET package, which is equipped with two cooling paths, can effectively dump heat into the double-sided cooling structure.
- The immense accessible surface area of the nanocrystalline transformer cores and windings are effectively coupled with the heat exchanger in a 3D manner. The high-current winding temperature can be controlled below 100^{o}C during 10 kW transient.
- HV MOSFETs (with a D^2PAK package) exhibit high thermal resistance from the case to the heat exchange surface even with through-hole thermal vias directly beneath the packages. However, the thermal capacitance of the copper clamp helps to suppress the junction temperature 20^{o}C below the maximum allowed value (150^{o}C) during 10 kW transient.
- The planar copper clamps, which are designed to realize DSCC, integrate both thermal and mechanical functions.

The system power density of this double-sided cooled DAB has achieved 3.2 kW/L at steady state and 16 kW/L during transient states. Disadvantages of such a planar high-current DAB converter with the DSCC strategy are also discussed, e.g., a high-current PCB with heavy copper creates difficulties with the component assembly, significant temperature fluctuation during thermal transients is unavoidable on the low-profile system structure, and the EMI issue is another potential design risk.

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Chapter 7

Conclusions and Recommendations

7.1 Conclusions

As mentioned in Chapter 1, there is a demand for High Power Density (HPD) DC-DC converters in yacht applications where space is limited. These converters often interface the low-voltage rechargeable battery-tanks with DC-AC converters to drive electrical motors and other electrical apparatus on board. They are characterized by high current ($\geq$ 100 A) on the low-voltage side, bidirectional power transfer capability, and galvanic isolation.

In order to guarantee the specified performance and lifetime of a power electronic system, we must carefully control the thermal conditions of all of the components that are involved. In this aspect, thermal management is required. The traditional "thermal management" term refers to heat removal (cooling) techniques that encompass various thermal interface and heat exchanger designs that suppress temperature rises of electronic components. However, just cooling is not sufficient enough to realize a HPD system; heat generation must also be cautiously controlled within thermal management designs in order to realize the HPD system.

The aim of this thesis is to develop an effective thermal management approach that addresses both heat generation management and heat removal management in order to achieve HPD for high-current bidirectional isolated DC-DC converters that are utilized in marine vehicle applications. Heat generation management is responsible for minimizing loss in a cost-effective manner, and heat removal management focuses on realizing low system thermal resistances in a compact volume. The conclusions of this work are presented as follows:

Topology selection for High-Current Applications
Conduction loss is significant in high-current power electronic converters. Different converter topologies transfer the same power to loads with differed Root-Mean-Square (RMS) current values in the power components. The topology with the lowest RMS current values will generally be more efficient in high-current applications. It is ascertained in Chapter 3 that:

- Topologies with triangular and sinusoidal current shapes demonstrate greater RMS current values than those with quadrilateral shapes.
- Topologies with lower reactive power are more efficient in terms of conduction loss than topologies with more substantial PF.
- Topologies with capacitors carrying the power current experience more conduction loss while also being bulky and are, therefore, not beneficial.

It is concluded that Dual Active Bridge (DAB) topology is a positive candidate for low-voltage high-current bidirectional isolated DC-DC converters. This is not only due to its low RMS current values, wide soft-switching range, and voltage operating range enabled by versatile modulation methods but also a result of the low component count and immunity to parasitic inductance.

Accurate Loss Modeling Methods

Accurate loss modeling is essential as a tool for analyzing heat generation and consists of two steps: waveform modeling and loss calculation. Waveform modeling is based on the inductor voltage-second balance and capacitor charge balance principles. The losses are calculated based on the loss equations introduced in Chapter 2. In this modeling process, a lossless circuit is assumed. It is addressed in Chapter 5 that, in order to improve the loss modeling accuracy for high-current converters, the impact of conduction loss on the two abovementioned steps must be considered. By taking into account the parasitic resistances, semiconductor on-resistance, winding resistances, and diode forward voltage on the waveforms, it has been experimentally demonstrated on a 1 kW DAB converter that the modeled waveforms and losses are very much in accordance with the measurements. Based on this accurate loss model, operating parameters and component parameters of a DAB converter (2 kW nominal and 10 kW peak in 5 seconds) have been optimized.

Modulation Methods for DAB with High Transient Power

There are three typical modulation methods available for DAB converters including rectangular, trapezoidal and triangular which differ in conduction and switching loss, operating range, and power transfer capability. One of them outperforms the other two in a certain operating range in terms of efficiency and depending on operational conditions. The proposed loss model is able to identify the optimal operating boundaries of these three modulation methods. For the 2 kW/10 kW DAB converter, it is found in Chapter 6 that:

- The rectangular method should be applied at a transient condition (10 kW) due to its highest power transfer capability.
- Trapezoidal and triangular methods should be applied when there is a load $\leq$ 5 kW because of higher efficiency where the trapezoidal method works when the input and output voltage ratio is close to the transformer turns ratio; the triangular method is applied for the remaining conditions.

High-Current Planar Ferrite Transformer

By thoroughly analyzing the product data from major ferrite manufactures in Chapter 5, it can be concluded that, compared with the commercially available E-shaped barrel cores, planar cores have:

- A greater core cooling surface area, however,
- A smaller winding cross section area (A_w) and longer winding length with the same flux cross section area (A_c).

It indicates that planar ferrite transformers generally have more winding loss and, hence, are required to increase the copper fill-factor of the winding window for improved efficiency in high-current conditions.

To minimize the transformer loss, a high-current planar ferrite transformer is optimized based on the proposed loss modeling approach discussed in Chapter 4. For the low-voltage and high-current DAB converters with frequency below 50 kHz, it is discovered from the analytical loss model that the optimal turns-number of the high-current winding of the planar ferrite transformer is less than one. Therefore, a single-turn low-voltage winding is the most appropriate selection for low-voltage high-current DAB converters in terms of efficiency. This conclusion is also applicable for the planar nanocrystalline transformer designed in Chapter 5.

To increase the fill-factor of the transformer winding window, Litz wires can be a more suitable option than PCB-based windings. This has been demonstrated on a 1 kW high-current DAB converter where a Litz-wire (High-voltage winding) based planar transformer demonstrates approximately 1% better efficiency than the PCB track based transformer.

High-Current Planar Nanocrystalline Transformer

Nanocrystalline magnetic material is known for its higher saturation flux density and lower loss density compared to ferrites. It is normally deployed in medium/high power range for a HPD transformer design. The use of this material for high-current planar transformers is investigated in Chapter 5. The design boundaries include:

- The minimal core plate thickness is 5 mm;
- Only C-shaped cores are possible to ensure sufficient mechanical strength.

To realize low-profile cores, 5 mm core plate thickness is employed throughout the design.

The A_w/A_c ratio of commercially available planar ferrite cores has been specified, however, the dimensions of nanocrystalline transformer cores have not yet been standardized by the industry. Therefore, the geometry of the nanocrystalline transformers can be customized for loss minimization in the high-current applications. For a DAB converter with 2 kW nominal power and 10 kW peak power, a planar nanocrystalline transformer has been designed and optimized. The C-shaped core dimension and two core-sets are treated specially:

C-shaped Core Dimension Optimization

At certain required flux density, the width of the winding window width of a single C-shaped core has been optimized for a minimal transformer loss. A broader winding window decreases the winding loss; however, core loss is boosted due to greater core volume. The width of an optimal winding window is determined at the balance between the winding loss and core loss during the nominal condition of the 2 kW DAB.

Separated Core-Sets Structure

A core-set consists of two C-shaped cores, and the nanocrystalline transformer comprises two core-sets. Two core-sets are separated at a certain distance in order to:

- Increase the core surface area that is exposed to the cooling system;
- Manipulate the transformer leakage inductance by tuning the distance between core-sets for the required maximum power transfer capability by the DAB converter.

The proposed nanocrystalline transformer is compared with a similar planar ferrite design on the 2 kW/10 kW DAB carrier. According to the analytical loss model proposed in Chapter 4, it has demonstrated that the nanocrystalline transformer experiences similar loss at 2 kW, however, the loss is half at 10 kW peak compared with the ferrite transformer. This is due to the fact that the nanocrystalline core dimensions have been specifically treated for high-current applications. Additionally, the nanocrystalline transformer achieves this with much smaller core volume.

Double-Sided Collective Cooling (DSCC) Strategy

As an effective heat removal management technique, a double-sided cooling strategy has been applied to address the extreme loss density in high-power semiconductor modules. In Chapter 6, DSCC strategy has been proposed to manage the heat removal on the converter level in order to achieve high power density for a high-current PE system. “Collective” implies that losses of all critical heat generators are collected, transferred, and dissipated in a centralized way. To apply the DSCC strategy, it is essential that:

- PE converters should be designed with a low-profile structure that enables large, flat, and accessible cooling surface areas on both sides. This facilitates the low thermal-impedance heat interfaces from heat generators to heat exchangers.
- The low-profile converter structure should be realized with planar transformers, SMD semiconductors, and ceramic capacitors that are assembled on a PCB substrate. Ultra-thin semiconductor packages equipped with two thermal paths (e.g. DirectFET) fits greatly in the DSCC strategy.
- The high-current transformer windings should be extended out of magnetic cores to enable an effective thermal interfacing with the heat exchanger.

- A clamper system can be designed to: 1) thermally bridge the heat on both sides of the system to a common heat exchanger and 2) mechanically support the entire system structure.

This DSCC strategy is implemented with the 2 kW/10 kW DAB converter which is cooled by a seawater cooling plate. FEM simulation analysis has shown that the lifetime-critical temperatures have been controlled below specified values during transient states. It can be found that:

- It is primarily the thermal capacitance of the copper clamper system that absorbs the transient thermal power and successfully suppresses the temperature.
- High power density is achieved: 3.2 kW/L in the nominal condition and 16 kW/L at transients.
- Significant temperature fluctuation occurs during transient states due to the small thermal capacitance resulting from a low-profile cooling structure. The interconnection elements such as solder joints and bonding wires will be greatly stressed because of this large temperature swing.

Soldering the DirectFET Package onto a PCB with larger copper volume

The 2 kW/10 kW DAB converter is designed based on a PCB with large copper volume in order to reduce the transformer winding loss and conduction loss in parasitic resistance. During final tests, this converter fails in operation. The failures always occur in the MOSFETs with DirectFET package. It is found that the failure originates from the inadequate soldering quality of the hidden pins directly beneath the DirectFET packages on the PCB with such a high thermal mass. To improve this soldering quality, professional reflow soldering equipment that is able to precisely control the temperature profile of such a heavy copper PCB should be deployed.

7.2 Recommendations

With the proposed thermal management approach, two DAB demonstrators have achieved compact system structures and good power density. However, a number of issues must be addressed in future research.

Iterative Design Loop

In the proposed heat generation management, converters are optimized by assuming certain component temperatures. These losses are subsequently supplied to the system thermal model to estimate the realistic temperatures. Depending on the cooling design, the actual temperature may deviate from the original assumption. Modeled loss would be more accurate if the loss model and thermal model can be linked as an iterative design loop.

Current-Crowding Effect in High-Current Transformer Windings

High-current planar transformers required a broader winding-window for lower winding loss. However, wide winding also signifies that the AC current tends to concentrate in the inner loop and corners of windings due to lower resistance there and the proximity effect. This current-crowding phenomenon generates an increased temperature around the winding corners. The seriousness of this hotspot and possible solutions can be investigated further.

Leakage Inductance Modeling of the Proposed Nanocrystalline Transformer

The proposed nanocrystalline transformer has a complex three dimensional structure where the two C-core sets are separated at a certain distance in order to obtain the required leakage inductance. The leakage inductance is tuned experimentally on a dummy transformer. A leakage inductance model of the proposed three dimensional transformer structure will facilitate the DAB design with different operating specifications.

Lifetime of interconnections

With low thermal mass of the low-profile converter structure, large temperature fluctuation will occur during transient operating conditions. It will accelerate the wear-out failure of bonding wires inside semiconductors and solder joints from all components to the power PCB. Power thermal cycling tests should be performed to evaluate the lifetime of interconnections with the solder materials and substrates that are utilized.

Wide Band-Gap (WBG) Semiconductor Applications

As mentioned in Chapter 2, theoretically, WBG semiconductors enable lower on-resistance and faster switching speeds compared with a Si device. How much the power density of the low-voltage and high current converters can benefit from the WBG semiconductors is interesting to investigate.

Appendix A

Analytical Calculation of Planar Winding Loss

This appendix derives the analytical calculation of the loss of planar windings of high-current transformers. The winding loss of the magnetic components consists of two parts: one resulted from the skin effect and the other from the proximity effect. Dowell [2-19] has showed that both components are independent from each other in one-dimensional (1D) modeling. 1D magnetic field distribution is valid in planar windings. Therefore, the winding loss of a planar conductor with width w, thickness h, a sinusoidal peak current I_{pk} in a uniform sinusoidal magnetic field with peak value H_{pk}, can be expressed by the sum of two terms:

$$P_w = P_{sk} + P_{prx} = F_{sk} \cdot I_{pk}^2 + F_{prx} \cdot H_{pk}^2 \tag{A-1}$$

where

$$F_{sk} = R_{dc} \frac{\nu}{4} \frac{\sinh \nu + \sin \nu}{\cosh \nu - \cos \nu} \tag{A-2}$$

$$F_{prx} = w^2 R_{dc} \nu \frac{\sinh \nu - \sin \nu}{\cosh \nu + \cos \nu} \tag{A-3}$$

here, R_{dc} is the DC resistance of the planr conductor, ν is the ratio between h and the skin depth δ, $\nu = h/\delta$. The skin depth is a function of the switching frequency f_s, which is given as

$$\delta = \sqrt{\frac{1}{\pi \mu \sigma f_s}} \tag{A-4}$$

where μ is the permeability and σ is the conductor conductivity. The first term P_{sk} in Eq. (A.1) represents the skin effect loss and the second P_{prx} stands for the proximity effect loss.

As the number of winding layers increases, the proximity effect increases the copper loss dramatically but the skin effect does not play a great role. This often occurs in a transformer with high turns ratio. An important way to reduce the copper loss is to interleave the windings. Instead of having windings separated from each other, interleaved structures have one winding sandwiched between the other at alternative positions. Fig. A.1 illustrates examples of the non-interleaved and two interleaved winding structures in a cross-section view of halved

transformer cores, where the primary winding is assumed to have one turn and the secondary (with slash lines) have *4N* turns. H-fields in the winding windows are plotted along the position in x-axis.

It can be found from Fig. A.1 that no matter in non-interleaved or in interleaved structures, the H-field has one or multiple sections (number *n*) where H-field rises from zero and drops back to zero. To analyze the influence of interleaving techniques on the copper losses, we derive the copper loss of the secondary winding on basis of single H-field section. Assume that the turns in primary winding and in secondary winding are connected in series and parallel, respectively. Assume that the number of layers in each H-field section of secondary winding is *M*, then the total turns of secondary winding is *nNM*.

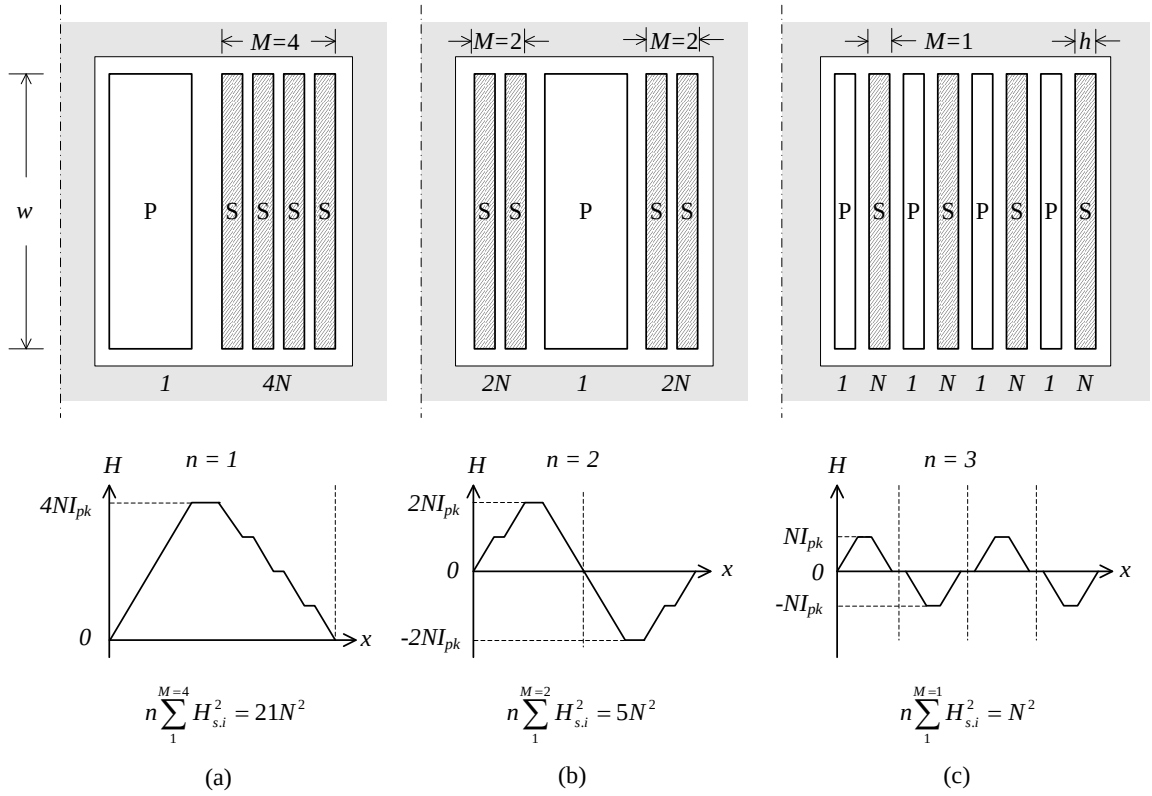


Fig. A.1 (a) Non-interleaved and (b, c) interleaved winding structures with their H-field plotted as a function of position

The winding loss resulted from skin effect can be calculated via Eq. (A-2):

$$P_{sk} = F_{sk} \cdot I_{pk}^2 = R_{DC} \frac{v}{4} \frac{\sinh v + \sin v}{\cosh v - \cos v} \cdot I_{pk}^2 \tag{A-5}$$

where R_{DC} is the DC resistance of entire secondary winding. To calculate the loss caused by the proximity effect (proximity loss), the average magnetic field around m^{th} layer should be obtained. Using Ampere-Law, the magnetic fields on right- and left-hand sides are given as:

$$H_{right} = N \frac{m-1}{w} I_{pk}$$
$$H_{left} = N \frac{m}{w} \cdot I_{pk} \tag{A-6}$$

Then the average magnetic field of m^{th} layer is

$$H_{av}\Big|_{m^{th}} = \frac{H_{right} + H_{left}}{2} = \left(\frac{2m-1}{2}\right) N \frac{I_{pk}}{w} \tag{A-7}$$

From Eq. (A-3), the total proximity loss can be calculated as the sum of the proximity loss in each section:

$$\begin{aligned} P_{prx} &= N \cdot P_{p-per-sec} = N \cdot \sum_{m=1}^{M} F_{prx} \cdot \left(H_{av}\Big|_{m^{th}}\right)^2 = N \cdot I_{pk}^2 \cdot \frac{R_{dc}}{M} \nu \frac{\sinh\nu - \sin\nu}{\cosh\nu + \cos\nu} \cdot \sum_{m=1}^{M} \left(m - \frac{1}{2}\right)^2 \\ &= N \cdot I_{pk}^2 \cdot \frac{R_{dc}}{M} \nu \frac{\sinh\nu - \sin\nu}{\cosh\nu + \cos\nu} \cdot \frac{\left(M - \frac{1}{2}\right)\left(M + \frac{1}{2}\right)(2M)}{6} \\ &= \nu R_{DC} \frac{\sinh\nu - \sin\nu}{\cosh\nu + \cos\nu} \cdot \frac{4M^2 - 1}{12} N \cdot I_{pk}^2 \end{aligned} \tag{A-8}$$

Since the sinusoidal peak current is $\sqrt{2} I_{rms}$, the total copper loss can be:

$$P_w = P_{sk} + P_{prx} = R_{DC} \frac{\nu}{6} \left[\frac{\sinh\nu - \sin\nu}{\cosh\nu + \cos\nu} \cdot N \cdot \left(4M^2 - 1\right) + 3 \frac{\sinh\nu + \sin\nu}{\cosh\nu - \cos\nu} \right] \cdot I_{rms}^2 \tag{A-9}$$

The AC resistance of the secondary winding can be derived as

$$R_{AC} = \frac{P_w}{I_{rms}^2} = \frac{P_{sk} + P_{prx}}{I_{rms}^2} = R_{DC} \frac{\nu}{6} \left[\frac{\sinh\nu - \sin\nu}{\cosh\nu + \cos\nu} \cdot N \cdot \left(4M^2 - 1\right) + 3 \frac{\sinh\nu + \sin\nu}{\cosh\nu - \cos\nu} \right] \tag{A-10}$$

Then, the ratio between the DC resistance and the AC resistance is

$$F_{AC} = \frac{R_{AC}}{R_{DC}} = \frac{\nu}{6} \left[\frac{\sinh\nu - \sin\nu}{\cosh\nu + \cos\nu} \cdot N \cdot \left(4M^2 - 1\right) + 3 \frac{\sinh\nu + \sin\nu}{\cosh\nu - \cos\nu} \right] \tag{A-11}$$

The winding loss and the AC resistance of the primary winding can be obtained in the same way. It can be found that if the number of layers increases, the proximity loss increases rapidly with the power of two (see Eq. (A-8)), while the loss caused by skin effect does not change with the winding structure (A-5).

Note that the derivations above assume a sinusoidal current. When the current in transformer winding is not in sinusoidal shape, the modeled current waveforms should be decomposed through Fourier series and the copper losses of each harmonic can be calculated via Eq.(A-9) and summed up to obtain the total copper losses.

The calculation above assumes the magnetic field is in one direction, which is parallel with the conductors. However, the gaps among turns and the distance to the core add smaller second vector to the magnetic fields. To compensate this two-dimensional (2D) effect, a "layer porosity factor" η is introduced [2-19]. This factor "stretches" the conductors out such that conductors fully fill the winding window width w_w and 2D effect disappears. The layer porosity factor η is defined as:

$$\eta = \frac{w}{w_w} \tag{A-12}$$

Assume the winding in each layer has an equal width of the core winding window, the conductivity of the "stretched" windings should be modified by a factor of η in order to maintain its DC resistance R_{DC} identical to the real case [Dowell64]. The modified resistance should be used in (A.10) to calculate the copper loss.

Appendix B

Current-Carrying Capacity of PCB Traces

This appendix contains three parts that support the PCB trace thermal design guideline work in Section 5.5. Three parts are:

- Literature review of PCB thermal design guidelines
- Thermal conductivity measurements of PCB under test
- PCB Trace Temperature measurement setups

B.1 Literature Review of PCB Thermal Design Guidelines

B.1.1 Conductor-sizing chart in IPC-2221

The external conductor-sizing chart in IPC-2221 (Fig. B.1) presents the relations between the current rating and the trace cross-section area for several values of the temperature rises above ambient. This chart can be traced back to 1950s, but detailed test board description is unknown. However, it is believed that it was measured on a PCB with an external trace located in the middle of one side and with a 35 μm thick copper plane on the other. Several flaws of this chart in IPC-2221 are noticed. First, because of little copper content in the test board, the measured data is conservative if applied to PCB with the same size but higher copper content. Moreover, the assumption that CCC of inner trace is simply 50% of an

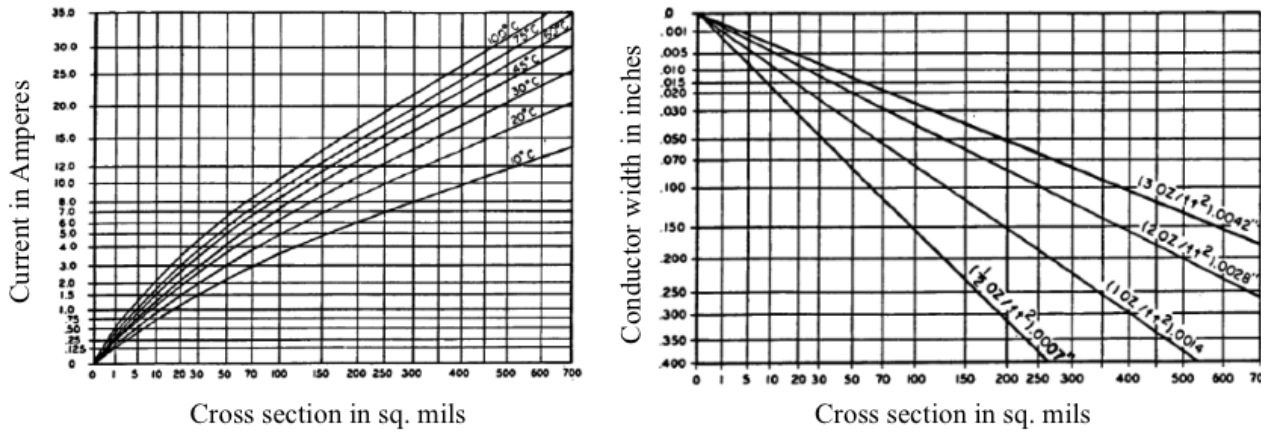


Fig. B.1 External conductor sizing chart in IPC-2221 (Top: temperature rise vs conductor cross-section area; Bottom: dimensions of conductors)

external one is oversimplified and erroneous [5-24][5-27][5-28]. Another important drawback is observed that the trace temperature rise is independently related to the cross-section area of traces and hence, the varying convection effect due to different trace surfaces on CCC is neglected. Realizing this oversimplified treatment, Brooks [5-24] adds the dependence on trace width and thickness in his CCC equation (1), derived by curve-fitting experimental results.

$$I = k \cdot \Delta T^{0.46} w^{0.76} t^{0.54} \tag{B-1}$$

where ΔT is the allowed temperature rise above ambient, w is trace width, t is trace thickness and k is a constant that is sensitive to the variations in test conditions.

B.1.2 Adam's work

With a mathematical thermal model validated by experimental data, Adam [5-24] presents calculated results about the temperature rise of traces in different board scenarios, such as boards with different base materials: FR4, ceramics and polyimide. The tested FR4 boards are also equipped with copper planes of different thickness and of different number of layers at varying board positions. All used boards have a dimension of 100 mm x 160 mm x 1.6 mm and the ambient temperature is 20 ^{o}C. The traces have a thickness of 35 μm and various widths. In this work, data shows that 1) different PCB base materials have varied influence on

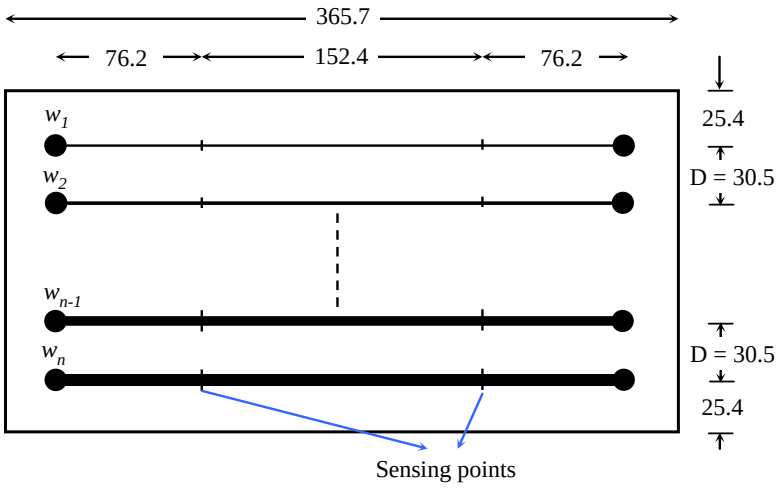


Fig. B.2 Test board configuration in IPC-TM-650, method 2.5.4.1a (unit: mm)

Table B.1 Summary of three main design guidelines

Design Guidelines	Board dimensions	Base Materials	Environment	Measurement Vehicle Description
IPC-2221	unknown	epoxy	Still air @ Room temperature	External trace with a 35 μm back copper plane
Adam's work	100 mm x 160 mm x 1.6 mm	FR4, ceramics, polyimide	Still air @ 20 ^{o}C	35 μm thick external traces of various widths, copper planes with different thicknesses and distances to the trace
IPC-2152	See [IPC-M-650]	FR4, polyimide	Still air & vacuum @ 25 ^{o} ± 5 ^{o}C	External traces of various widths and thicknesses on boards with various thicknesses

trace temperature rises; 2) high copper content improves the heat spreading and decreases the trace temperature rise.

B.1.3 IPC-2152

After many years preparation, IPC committee releases IPC-2152 in 2009, which is a specific standard about the trace CCC in PCB design. Considered as a more precise and comprehensive guideline for sizing conductors than that in IPC-2221, IPC-2152 is based on experimental measurements of CCC of PCB traces with multiple widths and thicknesses, on boards with multiple thicknesses and base materials, in environments of still air and vacuum. The tests are performed following test method 2.5.4.1a in IPC-TM-650 [5-29]. The test board is illustrated in Fig. B.2. Several external traces of various widths are located with fixed spacing *D* 30.5 mm. The temperature rises of the excited trace are calculated by measured resistance changes of the center part of according trace. The center part is 152.4 mm long and has a homogeneous temperature distribution because it's far away from the power cable connection where temperatures are disturbed by the contact resistance and heat-extracting effect of cables.

B.1.4 Discussion on Spare Space

Accuracy and applicability of three guidelines above are increased gradually. A summary of these three guidelines is given in Table B.1. Despite improvements realized in the latter two, they still have a common flaw that all tests are confined to PCBs with large bare spaces. This flaw undermines their use in modern power PCBs with quite limited spare area.

B.2 Thermal Conductivity Measurements of PCBs under test

The thermal conductivity of PCBs under test are measured to clarify its thermal property. Due to the laterally laminated structures, the thermal conductivities of PCB substrate differ in directions of in-plane and through-plane. This part describes the method to measure the in-plane and through-plane thermal conductivities of the FR4 substrate materials from two suppliers. Fig. B.3 shows the designed board to measure the through-plane (Fig. B.3.1) and in-plane (Fig. B.3.2) thermal conductivities.

B.2.1 *Through-plane thermal conductivity*

Fig. B.3.1a depicts the top view of the designed PCB to measure the through-plane conductivity of FR4 material. The 3 mm wide traces (orange) are homogeneously distributed on the top side of a square PCB board (11 cm × 11 cm). The bottom side of the PCB is the copper layer of 1 oz (35 μm) thick. This PCB is pressed against a heatsink, with a foam block (13 cm × 13 cm × 5 cm) covered on top. The foam is engraved on bottom side into to a deepness of 1.5 mm with the shape of the used PCB, so as to completely seal the PCB between the foam and heatsink with no air gap at all. This foam is made of EPS polystyrene

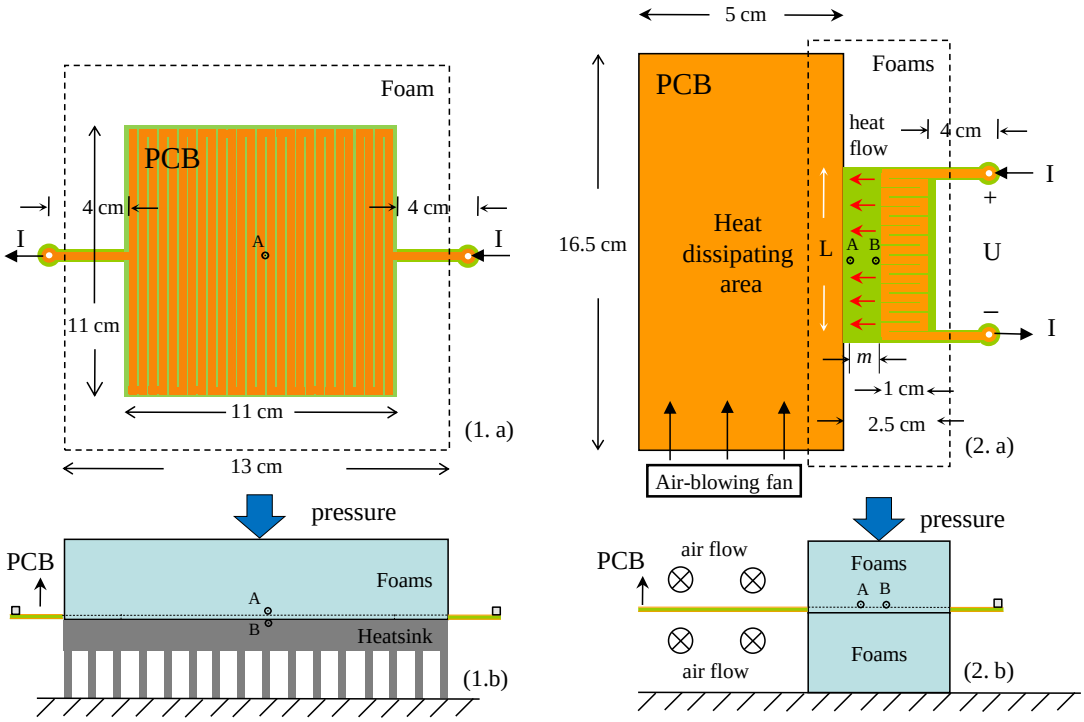


Fig. B.3 PCB structures designed to measure the in-plane (1) and in-plane (2) thermal conductivities of the used FR4 material. (a. top view, b. side view)

material with a thermal conductivity of 0.038 W/(m·K), which is approximately 10 times smaller than the through-plane thermal conductivity of common FR4 material. From the trace terminals to the square board is 4 cm long to make sure the only a tiny amount of heat in the square board can transfer to the terminal wires. A power supply injects DC current into the traces to generate the desired loss. The current I is measured with a current shunt resistor and the voltage drop U on the trace is measured by a multimeter. The dimensions are measured with vernier caliper. In order to measure the temperatures on the top and bottom sides of the PCB, two square slits (1.5 mm × 1.5 mm) are cut on bottom side of foam and on top side of heatsink so as to measure the temperatures (T_A and T_B) in the center (point A and B in Fig. B.3) of PCB with thermal couples. The thermal conductivity through-plane can be calculated from Eq. (B-2).

$$R_{th} = \frac{t}{\sigma_{th} \cdot A_{cs}} = \frac{\Delta T}{P_{loss}} \tag{B-2}$$

where R_{th} is the thermal resistance of FR4 material, t is the thickness of the FR4 material (1.5 mm in this test), A_{cs} is the cross-section area of the heat transfer path, P_{loss} the loss power and ΔT is the temperature difference between top side and bottom side of PCB. And then the through-plane thermal conductivity could be expressed as

$$\sigma_{th.through} = \frac{U \cdot I \cdot 1.5mm}{(T_A - T_B) \cdot 11cm^2} \tag{B-3}$$

Two FR4 materials from two suppliers are tested. One has a through-plane thermal conductivity of 0.31 W/(m·K) and the other has 0.38 W/(m·K).

Table B.2 Measurement of the in-plane thermal conductivities of FR4 materials from two manufacturers

Manufacturer	t (mm)	m(mm)	w (mm)	I (A)	U (V)	T_A(^{o}C)	T_B(^{o}C)	$\sigma_{th.in}$ (W/(m·K))
unknown	1.26	9.49	102.2	3.713	0.3685	39.7	107.4	1.489
LPKF	1.4	9.39	102.25	3.715	0.2975	42	86	1.648

B.2.2 In-plane thermal conductivity

Fig. B.3.2a presents the top view of the PCB design to measure the in-plane conductivity of FR4 material. The board consists of three parts:

1. The right part is the heat generating part. It consists of the 4 cm long trace terminals and 3 mm wide 10 mm long trace evenly distributed on both sides of the PCB as Fig. B.3.2b depicts.
2. The middle part (green) is the heat conduction part which has copper removed on both sides removed and has FR4 material of ***t*** mm thickness left.
3. Heat dissipating part (16.5 cm × 5 cm) on the left has copper planes on both sides of the PCB. It is exposed to the forced flowing air for effectively removing the heat.

The heat generating part, heat conduction part and a portion of the heat dissipating parts are sealed between two foam blocks (18 cm × 6 cm × 5 cm). A power supply injects DC current *I* in to the trace shown in Fig. B.3.2a. Due to the low thermal conductivity of the foam material and relatively low temperature potential of the heat dissipating part, it is assumed that all the generated heat will only transfer to the heat dissipating part, through the bare FR4 material in heat conduction part. The temperature difference between point A and B on the FR4 surface and the loss power are measured in the same way described above. The in-plane thermal conductivity can be calculated with Eq. (B-2). Two FR4 materials are tested here as well and the measurement results are given below in Table B.2.

In this test, two foam blocks have a large contacting area with the PCB board. Although the employed foam material has about ten-fold smaller thermal conductivity than that of FR4, another thermal path via foam material does exist due to the large contacting area between the PCB and the foam. This causes the measured thermal conductivity to be higher than the real one. Foam is the best thermally isolating material available in author's lab. More accurate measurement [5-30] utilizes vacuum as the thermal isolating medium around PCB, yet greater cost and test effort are required.

The FR4 substrate material from LPKF is used throughout all PCB trace CCC tests.

B.3 Temperature Measurement Setups

The temperature of PCB traces under test is measured with infrared camera. The temperature measurement setup is shown in Fig. B.4. The tested board (green) is vertically placed 5 cm above the table surface. A trace of *w* mm wide, located in the middle the board, is 4 cm to top and bottom edges of the PCB. The board is 19 cm long and 1.5 cm thick. The two terminals are connected to a DC or AC source with Litz wires. The picture of the measurement setup is given in Fig. B.5.

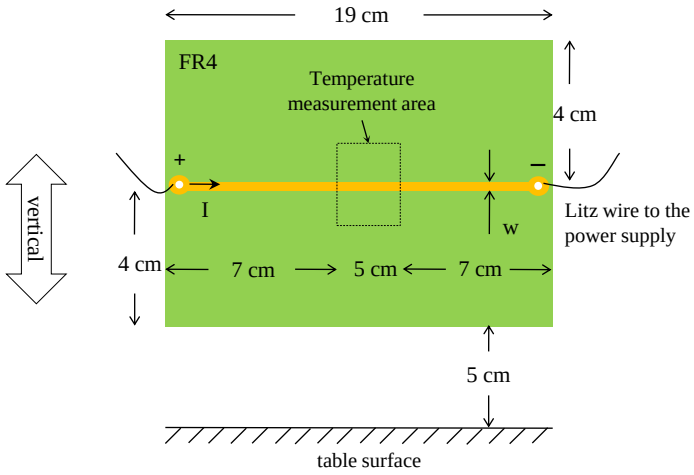


Fig. B.4 Temperature measurement setup in PCB CCC tests for *M* = 40 mm

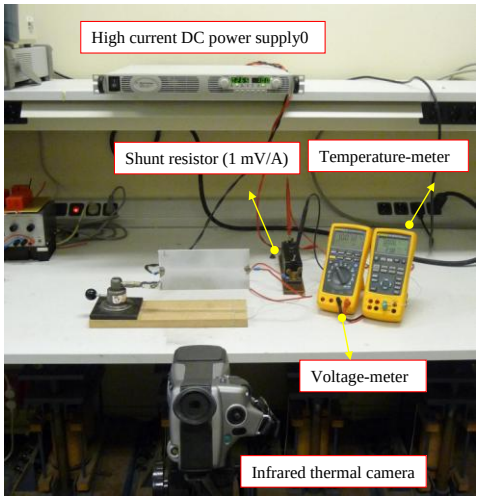


Fig. B.5 Picture of temperature measurement setup with board (*M* = 40 mm)

Infrared thermal camera FLIR S40 is used to measure the temperature distribution along the traces. Since the emissivity of the copper is different from that of FR4 material, direct temperature measurement of the full PCB with the thermal camera will be erroneous. Furthermore, the emissivity of the copper varies as the copper surface is gradually corroded with time. To obtain a homogeneous and constant emissivity across the trace and FR4 material, a white spray solvent (SKD-S2 SPOTCHECK, mainly used as the solvent developer) is sprayed evenly over the entire PCB surface. After the liquid is vaporized, a thin layer of white powder of a constant emissivity stays on the trace. The emissivity of white powder is measured to be 0.88 and it is an input to the thermal camera. The thermal couple is not used here, since the thermal couple and its thermal pad to fix thermal couples on the trace surface can disturb the temperature distribution along the trace and violate the accuracy of the temperature measurement. All measurements are done after the temperature becomes stable.

When measuring the temperature of traces with thermal camera, one should keep some issues in mind. Firstly, the lens of the camera should be focused on the trace under test. Secondly, the air around the PCB should be absolutely still for a real natural convection condition. The ambient temperature in all tests is controlled at 22 ^{o}C ± 0.5 ^{o}C. Thirdly, due to the heat-extracting effect of the power wires connected to the trace, temperature measurement can only

be done in the center of the trace where the temperature gradient reaches zero. The similar principle can be also found in IPC-TM-650, Method 2.5.4.1. This effect can be observed in Fig. B.6. A picture taken by infrared camera FLIR S40 shows the temperature distribution along 10 mm by 19 cm copper trace (M = 0) with 13 A dc current. It can be found that close to the terminal wires (purple) the temperature is lowered, and the part in the center part stays constant. Therefore, a length of 5 cm area located at the trace center will be the area to record the trace temperature, as shown in Fig. B.4.

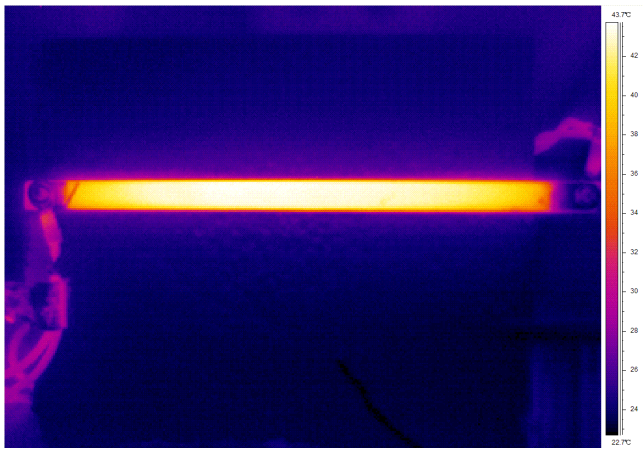
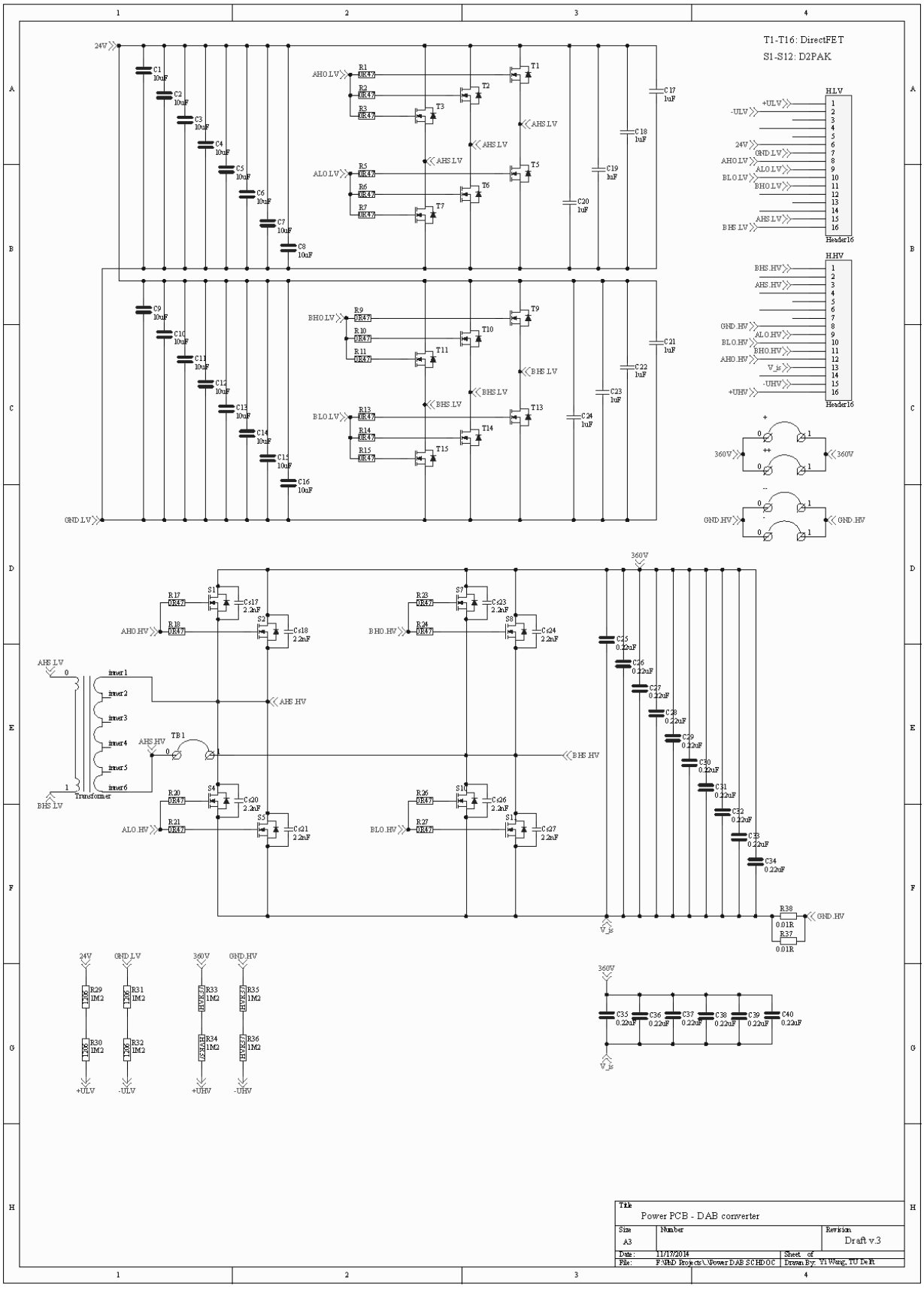


Fig. B.6 Infrared picture of the temperature distribution of the 10 mm wide 19cm long trace (board margin M = 0) with 13 A DC current flowing through, taken by the infrared thermal camera Flir S40 (T_{amb} = 22 ^{o}C)

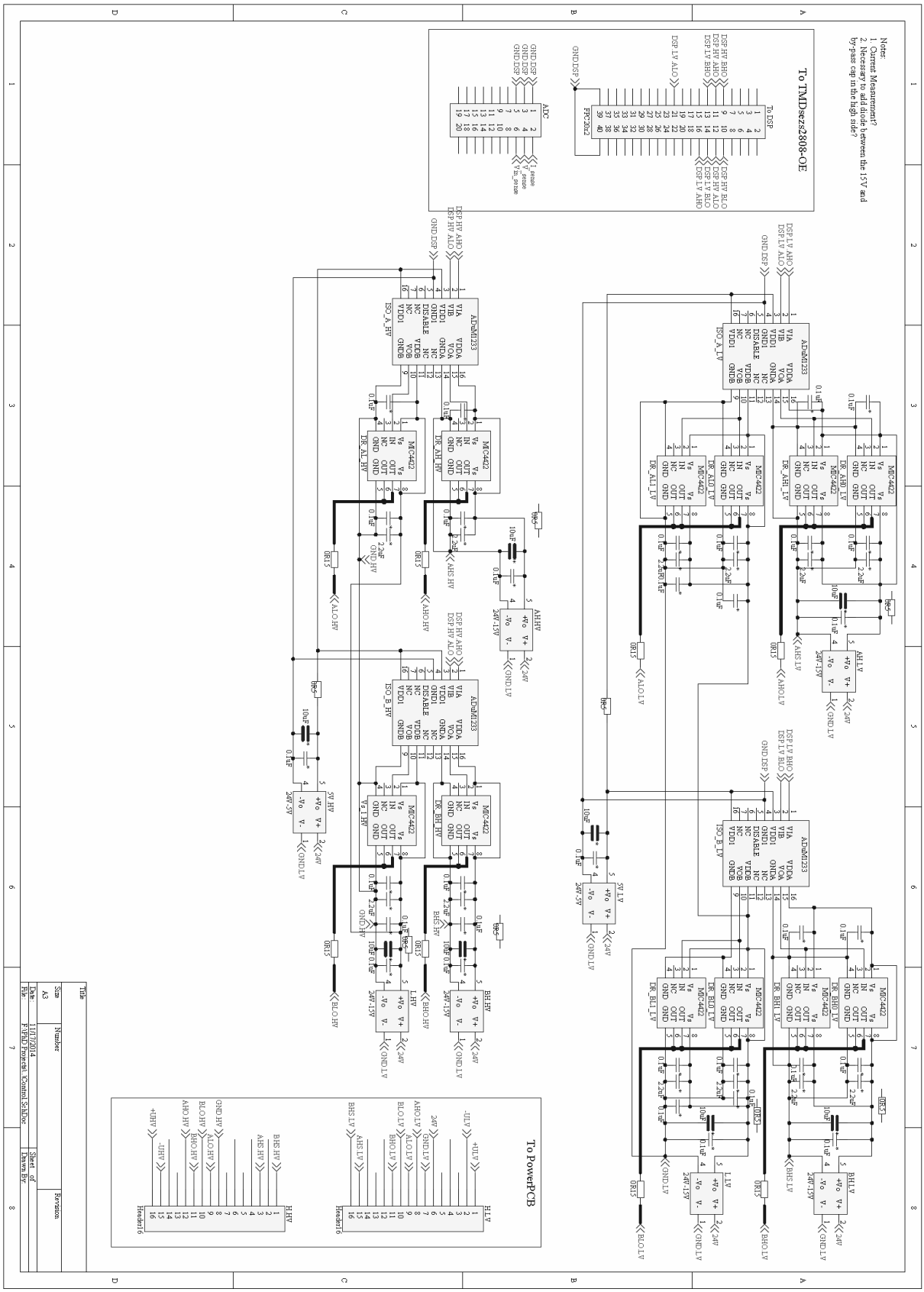
Appendix C

2 kW DAB schematics

C.1 Power Stage Schematic



C.2 Control and Drive stage Schematic



Summary

Thermal Management of High-Current Bidirectional Isolated DC-DC Converters

In autonomous power systems for yachts high-current isolated DC-DC converters are normally deployed to interface the energy storage battery-tanks with the high-voltage DC bus that powers electrical machines and other loads on board. These converters are equipped with bidirectional power flow ability in order to charge the battery-tanks with generators when cruising or with the on-shore grid when idle in the harbor. They are also often characterized by high transient power to start up the diesel engine on-board.

Due to the limited available space on private marine vehicles, high power density for these converters is in great demand. Processing the required power within a compact volume requires effective thermal management to suppress the component temperatures below a specified threshold such that a satisfactory system lifetime can be achieved. Conventional "thermal management" indicates various cooling techniques that reduce the component temperature. These techniques, however, are inadequate in the given limited space.

This thesis investigates an extended thermal management approach to achieving the high power density of high-current bidirectional isolated DC-DC converters. This approach manages heat systematically throughout its origin, flow path, and dissipation surface and comprises two components: *heat generation management* and *heat removal management*.

Heat Generation Management (HGM)

Heat originates from component losses in power electronic converters. This thesis first examines how losses are generated in a high-current isolated DC-DC converters and how to reduce these losses on component, circuit, and system levels, respectively. It is discovered that the topology that utilizes the partial resonance to achieve soft switching is preferred for high-current applications. The analytical equations to calculate the critical losses are summarized as a preparation for the quantitative management of heat generation.

The proposed HGM minimizes power component losses and system loss in a cost-effective manner and provides an advantageous loss input to the subsequent heat removal management. HGM addresses the following aspects: converter topology selection, loss modeling, detailed converter design, and component optimization.

First, this thesis evaluates and compares three typical categories of bidirectional isolated DC-DC topology in order to identify the most suitable candidate for high-current applications

when considering efficiency and potential volume. A full-bridge DAB converter is selected due to its simple circuit structure, low component count, immunity to parasitic inductance, soft switching, and the wide operating range enabled by multiple modulation methods.

Second, this thesis proposes an analytical and accurate loss modeling approach for high-current converters. By considering the impact of conduction losses on the waveform construction, the accuracy of the proposed model is significantly improved compared to the ideal modeling approach. Furthermore, this model is featured with low computational complexity, multivariable analysis, and the capability of full operating range calculation. A loss model constructed for a high-current 1 kW DAB converter has been validated experimentally. Based on this loss model, a high-current DAB with 2 kW nominal and 10 kW peak power are designed. The optimal operating ranges of the three modulation methods (i.e. rectangular, trapezoidal, and triangular modulations) applied to DAB are also identified to maximize the system efficiency at full working range.

Third, this thesis investigates the usage of a high-current planar ferrite transformer in high-current applications. It is demonstrated that the small A_w/A_c ratio (A_w: winding window area, A_c: flux area) of the planar cores diminishes the efficiency of the high-current planar ferrite transformer. To alleviate this drawback, the fill factor of the winding windows of planar cores is increased by employing Litz wire and copper foils instead of PCB tracks.

Nanocrystalline magnetic material has less loss compared with ferrites at the same flux density. This thesis proposes and investigates a planar nanocrystalline transformer for high-current DAB. The geometry of the proposed nanocrystalline transformer is optimized for minimal loss. When comparing with an equivalent ferrite transformer on the 2 kW/10 kW DAB converter, the nanocrystalline design indicates a comparable loss in nominal conditions but only a 50% loss at peak power. Such a design can considerably relax the thermal pressure in the peak power conditions. Additionally, the nanocrystalline transformer is more moderate in size.

Heat Removal Management

Without careful heat removal management, even minimal loss resulting from an effective HGM can generate extreme hotspots within the converter. This thesis proposes a collective cooling strategy for a thermally effective and volumetrically efficient cooling structure. The principle of this strategy is to collect heat from the primary power components via different heat interface designs and to conduct it to a common heat exchange surface where heat is dissipated in a centralized manner. This cooling strategy requires a low-profile converter structure to achieve low thermal resistance for heat interfaces between the critical power components and the heat exchanger. Such a method is demonstrated on a 1 kW planar DAB converter.

To accomplish a high power density level, a double-sided collective cooling (DSCC) strategy is further proposed and implemented to the aforementioned 2 kW/10 kW DAB converter. A low profile converter structure with an expansive and accessible cooling area on both sides has been realized by employing the ultra-thin LV MOSFET package with a double-sided cooling structure (DirectFET), SMD high voltage MOSFETs, and the planar nanocrystalline transformer. Two flat copper clamps are designed to extract the heat from both sides of the converter and conduct the heat to a cooling plate that exploits seawater to decrease the temperature. FEM simulation has demonstrated that, during the 10 kW transient, the double-sided cooling structure succeeds in controlling the critical semiconductor temperatures 20 ^{o}C below the maximum specified values. A theoretical system power density of 3.2 kW/L at steady state and 16 kW/L during transient is achieved. The disadvantages of this 2 kW DAB designed with DSCC are also discussed.

SAMENVATTING

Thermal Management of High-Current Bidirectional Isolated DC-DC Converters

In zelfstandige energie systemen voor jachten worden normaal hoge-stroom geïsoleerde DC-DC omvormers toegepast als verbinding tussen de energie opslag accu's met een hoge DC bus spanning en de hoge vermogens systemen en andere belastingen aan boord. Deze omvormers voorzien in bidirectioneel bedrijf en zijn zo in staat om de accu's te laden vanuit de generator als het schip vaart, of vanuit een wal aansluiting wanneer het schip in de haven ligt. Dit type omvormer is ook in staat om kortstondig hoge stromen te leveren voor het starten van de diesel motoren aan boord.

Vanwege de beperkte ruimte op privé schepen is er een sterke behoefte aan een hoge vermogens-dichtheid bij dit soort omvormers. Het verwerken van de gewenste vermogens binnen een compact volume vraagt om een effectieve thermische huishouding om component temperaturen beneden kritische waarden te houden en de gewenste levensduur te garanderen. Conventionele koel methodes bieden meerdere mogelijkheden voor het reduceren van component temperaturen. Deze technieken zijn echter niet toereikend binnen het beperkte volume beschikbaar.

Deze thesis onderzoekt de realisatie van een hoge energiedichtheid, hoge-stroom, bidirectionele ge-ïsoleerde DC-DC omvormer. Het onderzoek begint bij het optimaliseren van de bron van de warmte generatie en kijkt hierna hoe de warmte efficiënt kan worden afgevoerd.

Warmt Generatie Beheer (WGB)

Warmte ontstaat door verlies in de componenten van de omvormer. Deze thesis kijkt als eerste hoe de verliezen ontstaan in de omvormer en hoe deze verliezen gereduceerd kunnen worden op component, circuit en systeem niveau. Een deels resonante topologie waarmee zacht schakelen mogelijk is heeft de voorkeur voor deze applicatie. De analytische vergelijkingen voor het berekenen van de kritische verliezen zijn opgesomd als voorbereiding op een kwantitatief beheer van de gegenereerde warmte.

Het voorgestelde WGB minimaliseert het verlies in de vermogens componenten op kosten effectieve manier en zorgt voor minimale warmte generatie om de afvoer te vereenvoudigen. WGB adresseert de volgende aspecten; omvormer topologie selectie, modelering van de verliezen, ge-detailleerd omvormer ontwerp en component optimalisatie.

Als eerste vergelijkt deze thesis drie typische categorieën van bi directionele geïsoleerde DC-DC doxologieën om de meest geschikte kandidaat voor deze applicatie met de aandacht op efficiëntie en potentieel volume te identificeren. Een volle brug DAB omvormer is geselecteerd vanwege het eenvoudige circuit, kleine aantal componenten, immuniteit voor parasitaire zelfinducties, zacht schakelende gedrag en brede bedrijfsgebied mogelijk gemaakt door meerdere modulatie technieken.

Als tweede wordt een aanpak voor het nauwkeurig modeleren van de verliezen in de omvormer voorgesteld in deze thesis. Door de invloed van geleidings verliezen op de golfvorm opbouw mee te nemen heeft het voorgestelde model een aanzienlijk hogere nauwkeurigheid in vergelijking met een ideaal model. Daarnaast heeft dit model een lage reken complexiteit, multivariabele analyse en de mogelijkheid om berekeningen over het volledige bedrijfs gebied uit te voeren. Het verlies model van een 1 kW DAB omvormer is experimenteel gevalideerd. Gebaseerd op dit verlies model is een DAB omvormer van 2 kW nominaal en 10 kW piek vermogen ontworpen. Het optimale bedrijfs-gebied voor de drie modulatie methodes (rechthoekig, trapezoïde en driehoek modulatie) toegepast op DAB zijn ook geïdentificeerd om de systeem efficiëntie te maximaliseren over het volle werk gebied.

Als derde is het gebruik van hoge stroom planaire ferriet transformatoren in deze applicatie onderzocht. Het is gedemonstreerd dat een kleine A_w/A_c verhouding (A_w: winding venster oppervlak, A_c: flux oppervlak) van planaire kernen de efficiënte teniet doet. Om dit te compenseren is de vullings factor van het wikkel venster van de planaire transformatoren vergroot door de toepassing van Litze draad en koper folie in plaats van PCB sporen.

Nanokristallijn magnetica materiaal heeft minder verlies vergeleken met standaard ferriet materiaal bij dezelfde flux dichtheid. Het derde deel van de thesis stelt planaire Nano kristallijne transformatoren voor DAB voor en onderzoekt deze constructie. De geometrie van de voorgestelde transformator is geoptimaliseerd voor laagste verliezen. Vergeleken met een standaard ferriet transformator voor de 2 kW/10 kW DAB omvormer geeft het Nano kristallijne ontwerp een vergelijkbaar verlies in nominale condities maar slechts 50% verlies bij het piek vermogen. Een dergelijk ontwerp kan de thermische belasting tijdens piek vermogen bedrijf aanzienlijk verlagen. Daarnaast heeft de Nano kristallijne transformator kleinere afmetingen.

Warmte Afvoer Beheer

Zonder goede warmte afvoer kunnen zelfs kleine verliezen als gevolg van een goed WGB resulteren in lokale oververhitting in de omvormer. Deze thesis stelt een collectieve koel strategie voor die thermisch effectief is en efficiënt gebruik maakt van het beschikbare volume. Het principe van deze strategie is het verzamelen van de warmte bronnen via verschillende thermische interfaces en om de warmte te geleiden naar een centraal warmte uitwissel vlak waar de warmte op een centrale manier wordt afgegeven. Deze koel strategie

vereist een omvormer met een laag profiel om een lage thermische weerstand voor de interface tussen de kritische vermogens componenten en de warmte wisselaar mogelijk te maken. De methode wordt gedemonstreerd op een 1kW planaire DAB omvormer.

Om een hoge vermogens dichtheid te realiseren is een dubbelzijdige koelings strategie voorgesteld en geïmplementeerd op de eerder genoemde 2 kW/10 kW DAB omvormer. Een lage bouwhoogte van de omvormer geeft een groot toegankelijk koelings oppervlak aan beide kanten, dit is gerealiseerd door de toepassing van een ultra dunne LV MOSFET behuizing met een dubbelzijdige koel structuur (DirectFET), SMD hoog spannings MOSFETs en planaire Nano kristallijne transformatoren. Twee platte koperen klemmen zijn ontworpen om de warmte aan beide kanten van de omvormer af te voeren naar een warmte wisselaar die gebruik maakt van zeewater om de warmte aan over te dragen. FEM simulaties hebben aangetoond dat tijdens het 10 kW piek bedrijf de dubbelzijdige koel constructie in staat is om de halfgeleiders 20 ℃ onder de gespecificeerde maximale temperatuur te houden. Een theoretisch systeem vermogens dichtheid van 3.2 kW/l in normaal bedrijf en 16 kW/l tijdens piek belastingen is gehaald. De nadelen van deze 2 kW DAB ontwerp met dubbelzijdige koeling worden ook besproken.

List of Publications

1. Y. Wang, S. W. H. de Haan, J.A. Ferreira, "Design of low-profile nanocrystalline transformer in high-current phase-shifted DC-DC converter," *2010 IEEE Energy Conversion Congress and Exposition (ECCE'10),* Atlanta, USA, 12-16 Sept. 2010, pp. 2177-2181.

2. Y. Wang, S. W. H. de Haan, J.A. Ferreira, "High power density design of high-current DC-DC converter with high transient power," *2010 IEEE Energy Conversion Congress and Exposition (ECCE'10),* Atlanta, USA, 12-16 Sept. 2010, pp. 3001-3008.

3. Y. Wang, S. W. H. de Haan, J.A. Ferreira, "Thermal design guideline of PCB traces under DC and AC current," *2009 IEEE Energy Conversion Congress and Exposition, 2009. (ECCE'09),* San Jose, USA, 20-24 Sept. 2009, pp. 1240-1246.

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5. Y. Wang, S. W. H. de Haan, J.A. Ferreira, "Optimal operating ranges of three modulation methods in dual active bridge converters," *IEEE 6th International Power Electronics and Motion Control Conference, 2009. (IPEMC'09),* Wuhan, China, 17-20 May 2009, pp. 1397-1401.

6. Y. Wang, S. W. H. de Haan, J.A. Ferreira, "Methods for experimental assessment of component losses to validate the converter loss model," 13th *Power Electronics and Motion Control Conference, 2008 (EPE-PEMC'08),* 1-3 Sept. 2008, pp. 187-194.

7. Y. Wang, B. Roodenburg, S. W. H. de Haan, "Comparative study of three transformer concepts for high current dual active bridge converters," *5th International Conference on Integrated Power Systems, 2008 (CIPS'08),* Nuremburg, Germany, 11-13 March 2008, pp. 1-4.

8. Y. Wang, S. W. H. de Haan, A. van Zwam, "Novel dual-band controller for regulating DC-bus voltage that contains a large voltage ripple," *7th International Conference on Power Electronics, 2007 (ICPE'07), Daegu, South Korea,* 22-26 Oct. 2007, pp. 192-196.

9. Y. Wang, S. W. H. de Haan, A. van Zwam, "Analysis of sensitivity of the performance of interleaved flyback converter to the principal design parameters," *7th International Conference on Power Electronics, 2007 (ICPE'07), Daegu, South Korea,* 22-26 Oct. 2007, pp. 85-89.

Curriculum Vitae

Yi Wang was born in Xingtai, Hebei province, China, on 4 Oct. 1981. He received the B. Sc. degree in 2003 from the Department of Electrical Engineering and Automation of Hebei University of Technology in Tianjin, China.

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Since Sept. 2006, he joined the Electrical Power Processing group of Delft University of Technology to purse the PhD degree in the field of high power density power electronics. His research focuses on realizing high power density of the high-current bidirectional isolated DC-DC converters, which is employed for interfacing the storage batteries with high-voltage DC bus in the autonomous electrical system such as marine vehicles.

From 2011 until now, he works as a senior electrical engineer in Philips Lighting. His main responsibility is to design electrical drivers for retrofit LED lamps that are required to be compatible with electronic transformers and ballasts.