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Analysis of signal attenuation in global shutter CMOS image sensor

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ABSTRACT

This paper focuses on a new non-ideal phenomenon induced by the power supply crosstalk (PSC) of the row drive circuit in 8 T global shutter (GS) CMOS image sensors (CISs). A method to eliminate the non-ideal phenomenon is presented. Based on the circuit simulation, the relationship between the parasitic resistance and PSC is analyzed. The PSC would cause a charge leakage on the sampling hold (S/H) capacitors in the 8 T pixel, which in turn attenuates the output signal of the image sensor. Through the mathematical model of the in-pixel S/H circuit, the effect of PSC and exposure on signal attenuation is analyzed. To eliminate signal attenuation, this paper utilizes a separate power layout method that isolates the row drivers in different columns by using multiple power supplies. In contrast to the method of sharing the power supply, the proposed method can reduce the maximum power supply crosstalk noise from 1.17 V to 2.58 μV in the 2000 × 2 row drive array. Based on the 0.13 μm CMOS process, the measurement results of the 1st chip design using the typical shared power structure and the 2nd chip design using the separate power supply structure are compared. The measurement results show that the output signal of the 1st chip design is limited to about 303 ADU due to the power supply crosstalk. The saturated output signal of the 2nd chip design is 2200 ADU, which is in accordance with the theoretical signal output value (2200 ADU) when the pixel is saturated. The proposed method can effectively eliminate signal attenuation induced by the PSC, thereby improving the image quality of 8 T GS CIS.

1. Introduction

CMOS image sensors (CISs) have attained great popularity in many consumer and professional applications [1]. The typical shutter type for most CISs is rolling shutter (RS) [2]. RS CISs cannot avoid the inherent distortion of rolling exposure no matter how much exposure speed improves for capturing a moving target [3,4]. Thus, CISs with global shutter (GS) pixels are designed to overcome the issues of image distortion which is often unavoidable in RS CISs

Five-transistor (5 T) pixel is the earliest GS pixel structure suffered from high read noise and poor shutter efficiency due to the lack of correlated double sampling (CDS) [5,6]. Hence, several pixel structures combining CDS with GS functionality are proposed to eliminate the reset noise and improve global shutter efficiency (GSE). These structures are mainly in three types: the 6 T and 7 T pixels that store charges under the MOS storage gates (SGs) [7,8], the 6 T pixels that store charges in pinned charge storage diodes (SDs) [9,10], and the 8 T pixels that store signal voltages in in-pixel sampling hold (S/H) circuits [11,12]. The 6 T and 7 T pixels, however, typically require an additional charge storage site and significant process changes, which would increase the cost or reduce the performance of the CISs [13]. Ref. [14] pointed out that during the process of pixel signal storage, the storage node is susceptible to contamination by parasitic light, resulting in a reduction in GSE of the CIS with 6 T or 7 T pixel structure. 8 T pixels have better noise performance than 5 T global shutter pixels, and typically also have better global shutter efficiency than 6 T and 7 T pixels after the exposure time [15]. Nowadays, 8 T pixel is widely used in GS CIS for its good performance in GSE [16] Voltage based S/H pixels impose severe requirements on the CIS supplies and any disturbance at the substrate or the pixel supplies leads to non-ideal phenomena. Ref. [16] pointed out that at the end of the exposure, the parallel operation of discharging all 8 T pixel capacitors and enabling the bias current of the first source follower would generate a large peak current on the pixel array power supply and cause the damage. In this paper, another non-ideal phenomenon was also discovered during the process of the signal charge storage in the S/H capacitors of the 8 T pixel. This non-ideal phenomenon is that the parallel operation of the row driver array may cause a large peak current on the row driver power supply during the 8 T pixel global operation phase, which would result in signal attenuation. This paper analyzes the mechanism of the signal attenuation and proposes a solution to improve signal integrity

This paper briefly introduces the operating principle of 8 T pixel in

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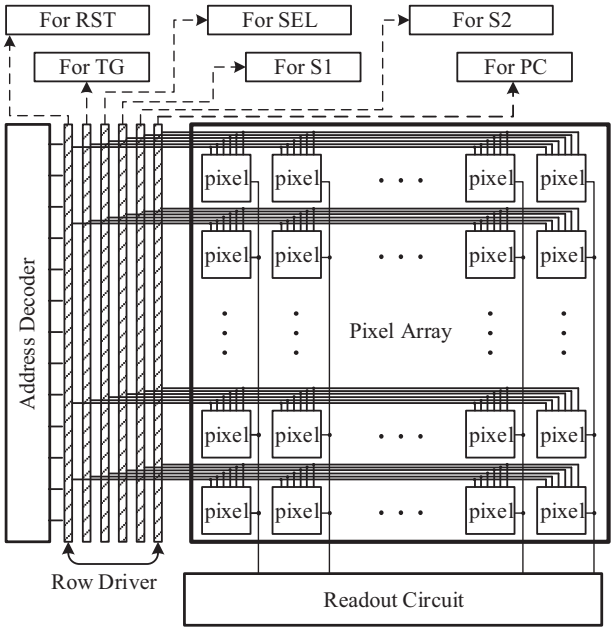

Fig. 1. The basic architecture diagram of 8 T GS CIS.

Section 2. A circuit model of the row driver array with parasitic resistance and capacitance is established in Section 3. A mathematical model with power supply crosstalk (PSC) and exposure is also established. Through simulations and model analyses, the effects of PSC, parasitic resistance, and exposure on output signals are analyzed. In Section 4, a separate power supply structure that isolates the row drivers in different columns by using multiple power supplies is utilized to eliminate the signal attenuation. In Section 5, the measurement results of the 1st chip design using the shared power supply structure and the 2nd chip design using the separate power supply structure are compared. The conclusions were drawn in Section 6

2. Analysis of 8 T global shutter CMOS image sensor

Fig. 1 shows the basic architecture diagram of 8 T GS CIS, which consists of a timing control circuit, a readout circuit, a row driver array, and a pixel array. The row driver array is used for driving the controlling lines of the pixel array. Moreover, several column-level row driver arrays in CIS typically employ a shared power supply structure as shown in Fig. 2.

The timing diagram of 8 T GS pixel is shown in Fig. 4, which can be divided into two stages called frame overhead time (FOT) and row overhead time (ROT). Stage A indicates that the signal charges have

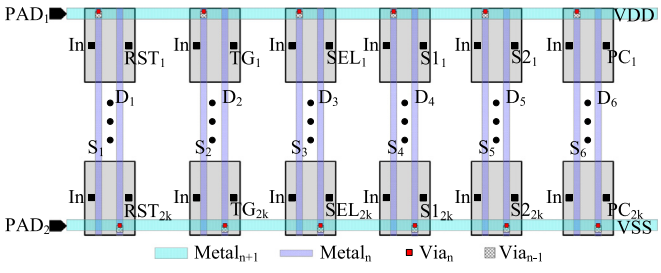

Fig. 2. The shared power supply layout diagram of the row driver circuit in CIS.

The 8 T pixel structure including eight transistors, one pinned photodiode (PPD), and two MOS capacitors, is shown in Fig. 3. As shown in the figure that the 8 T pixel is controlled by six signals from the row driver array. The control signals are sensing node reset (RST), photodiode charge transfer gate (TG), precharge (PC), sampling switch one (S1), sampling switch two (S2), and row select switch (SEL).

been transferred from PPD to C1. The portion marked by the red circle indicates the timing operation that would cause PSC in the row driver circuit. During the FOT, all pixels have the same timing operation, which can be divided into three main phases: integration, reset, and sampling.

After FOT, the reset voltage V_{reset} and the signal voltage V_{signal} would be stored on C2 and C1 until they are read out row by row. Signal storage time is shorter for the earlier readout pixels, vice versa. The longer the signal is stored, the more likely it is to be disturbed.

During the ROT, the M_{SEL} is switched on, so as to activate the M_{SF2} of that row. The reset voltage V_{reset} stored on C2 will be read out first. Then, the M_{S2} is switched on by S2 to short C1 and C2 so that the signal charges stored on C1 are redistributed in both C1 and C2. According to the conservation of electric charge:

$$Q_s = C1 \cdot \Delta V_{sig} = (C1 + C2) \cdot \Delta V_{redis} \tag{1}$$

where Q_S is the amount of charge in C1 before charge redistribution, $\triangle V_{sig} = V_{reset} - V_{signal}$ is the voltage drop on C1 due to the charge transfer, $\triangle V_{redis}$ is the voltage drop on C2 owing to the charge redistribution. Hence, the voltage ΔV_{redis} can be calculated by:

$$\Delta V_{redis} = \frac{C1}{C1 + C2} \cdot (V_{reset} - V_{signal}) \tag{2}$$

After charge redistribution, the attenuated signal V_{rs} ($V_{rs} = V_{reset} - \triangle V_{redis}$) is read out as the pixel signal. According to (1) and (2), after using CDS, the output of the 8 T pixel can be expressed as:

$$\begin{aligned} V_{output\text{-}CDS} &= V_{reset} - V_{rs} \\ &= \frac{C1}{C1 + C2} \cdot (V_{reset} - V_{signal}) \end{aligned} \tag{3}$$

According to (3), if the V_{reset} and V_{signal} stored in the S/H capacitor are disturbed, the pixel output voltage will be affected, reducing the imaging quality of the CIS. As shown in Fig. 3, V_{reset} and V_{signal} are actually stored at the source or drain of the M_{S2}, during which the control signal of M_{S2} is always held low (0 V). Similarly, if M_{S2} is disturbed during turn-off, it would also lead to non-ideal phenomena.

A new non-ideal phenomenon was discovered during the process when signal charges were stored in the S/H capacitors. That is, the parallel operation of turning off M_{PC} and M_{S1} in all 8 T pixels may generate a large peak current on the row driver array power supply, which would cause PSC in the row drive array, ultimately resulting in signal attenuation.

3. Non-ideal effect analysis

3.1. Analysis of non-ideal phenomena in 8 T pixels

In order to describe the non-ideal phenomenon of signal attenuation, this paper establishes a simple electrical model for 8 T pixels, as shown in Fig. 5. The source followers M_{SF1} and M_{SF2} are modeled by amplifiers with attenuation factors A_1 and A_2, respectively. V_{signal} and

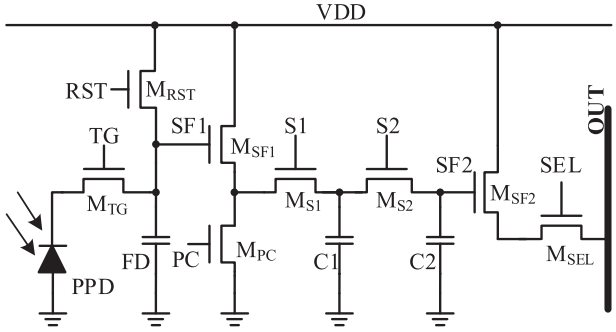

Fig. 3. The schematic diagram of the 8 T global shutter pixel.

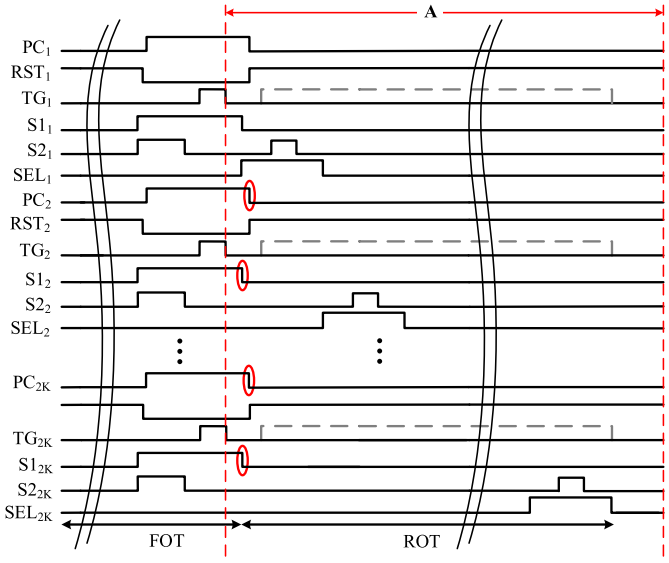

Fig. 4. Basic timing diagram of the 8 T GS CIS.

V_{reset} are the signal voltage and reset voltage at the floating diffusion (FD) node, respectively. ΔV is a voltage spike.

In the 8 T pixel, the control signal S2 is mainly used to control the transfer of the signal charge in C1. In phase A of Fig. 4, S2 will remain low to ensure that the signal voltage is consistently stored in C1 before being read out. During this period, if a voltage spike ΔV greater than the threshold voltage $V_{th\text{-}MS2}$ of M_{S2} is added to S2, M_{S2} would be turned on. Afterwards, the signal charge that should have been stored in C1 would leak into C2. In other words, a severer charge leakage will result in a lower gray value for the corresponding pixel row in the final output image. In the most extreme case, the charge leakage would make the voltage on C1 and C2 equal. As a result, the final output after CDS will be zero, which leads to static black stripes in the output image as demonstrated in Section 5.

3.2. Effect of row driver power supply crosstalk on 8 T pixels

In fact, as shown in Fig. 4, M_{S1} and M_{PC} of all pixels need to be globally turned off after the signal charges are transferred from PPD to C1. The parallel operation of the row drivers that drive the pixel control signals may generate a large peak current on ground bus. This peak current would destroy the operating state of the adjacent row driving circuit through the shared ground bus, causing power supply crosstalk in the row driver circuit. Ultimately, this will result in signal attenuation as described in Section 3.2.

To illustrate the effect of PSC on CIS in detail, an equivalent circuit model of the row driver array is established as shown in Fig. 6. The R_{par} and C_{par} in the equivalent circuit represent the parasitic resistance and parasitic capacitance of the interconnection lines, respectively. C_{L1} and C_{L2} represent the output loads of the row driver circuit for PC or S1 (named RDC1) and the row driver circuit for S2 (named RDC2), respectively. R_{gnd} represents the parasitic resistance of the metal interconnect lines from the ground pad to the Nth buffer. I_A is the sum of the peak currents (i_{fall}) produced by N drivers. This circuit model simulates the circuit work state when the input V_{in1} of RDC1 is a ramp signal switching from high to low during setup time, and the input V_{in2} of RDC2 remains static at low. Since the initial input voltage of RDC2 remains at low, the NMOS transistors in RDC2 can be replaced by a 2R2S (two resistors and two switches) equivalent circuit as shown in Fig. 6. R_n and R_p represent the on-resistance of the NMOS and PMOS transistors, respectively. When the input of RDC1 switches from high to low, a large transient current I_A is generated during the transition. Then, the transient current I_A would flow through each NMOS transistor of RDC2 and charge the output capacitors C_{L2} through the shared ground bus V_{SS}.

As a result, the voltage of the output nodes that should be fixed at 0 V will rise depending on PSC. Since the output of RDC2 is directly

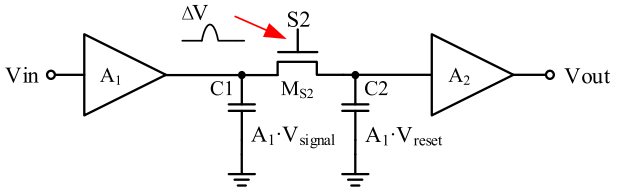

Fig. 5. The simple electrical model for 8 T pixel.

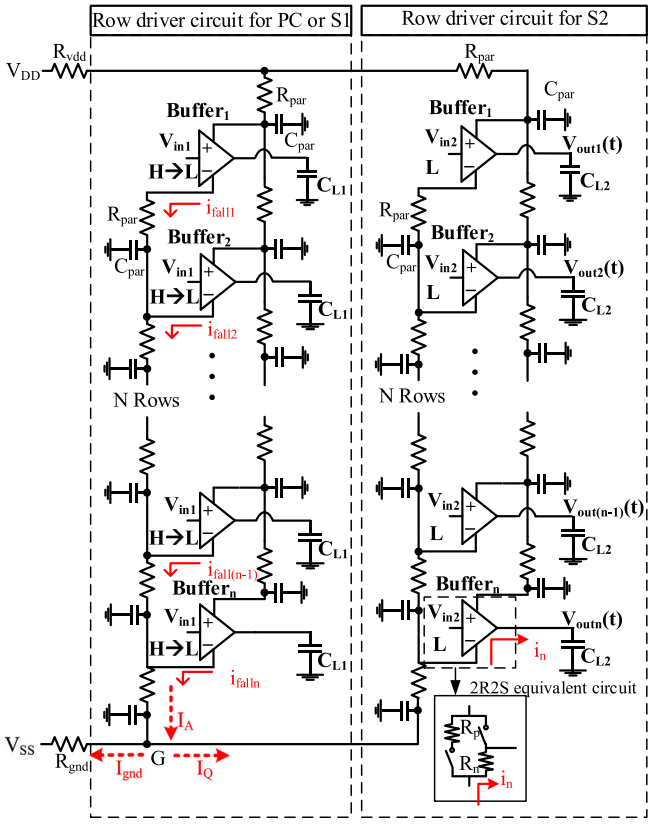

Fig. 6. Equivalent circuit for power supply crosstalk simulation of row driver array in 8 T GS CIS.

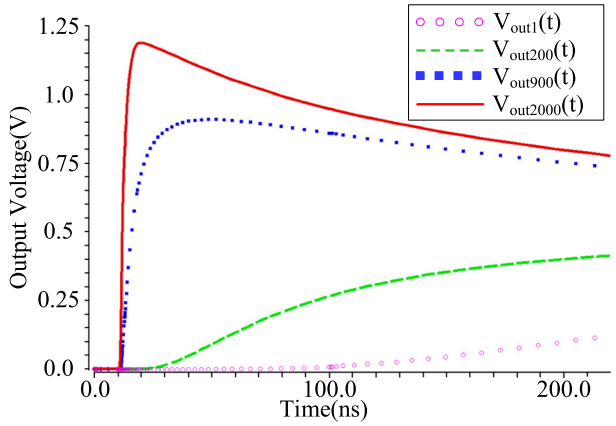

Fig. 7. The PSC simulation results of RDC2 in a 2000 × 2 row driver array.

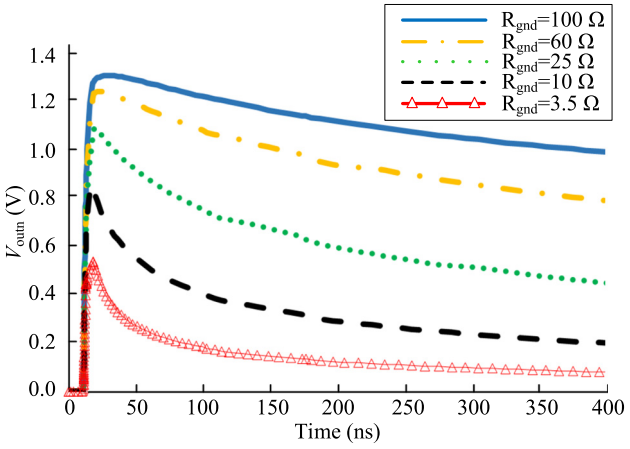

Fig. 8. The simulation results of V_{outn}(t) under different R_{gnd}.

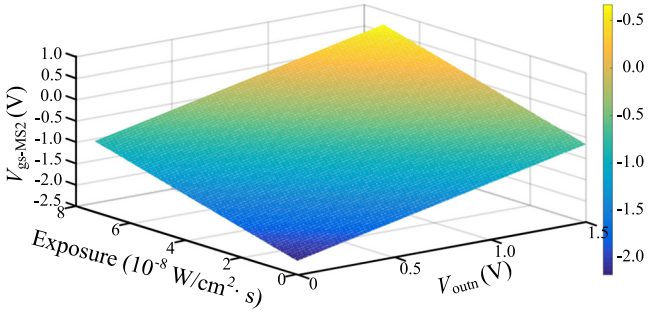

Fig. 9. The relationship among $V_{gs\text{-}MS2}$, exposure and V_{outn}.

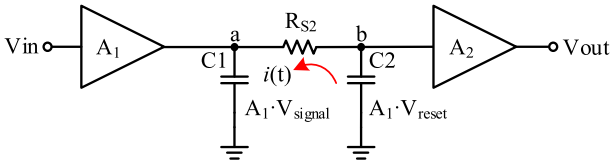

Fig. 10. The noise equivalent circuit model of 8 T pixel.

connected to the gate of M_{S2}, the change in its output voltage would affect the operating state of M_{S2}. When the voltage spike ΔV of the RDC2 output node is higher than $V_{th\text{-}MS2}$, M_{S2} would be turned on falsely, resulting in signal attenuation.

In this chapter, a CMOS image sensor with 2 k × 2 k pixels is measured. Each unit pixel is in the size of 5.5 μm × 5.5 μm. The distance from the ground pad to the nearest row driver is 0.18 cm. And the distance between two adjacent row drivers is 5.5 μm. In the 0.13 μm CMOS process, the parasitic resistances R_{gnd} and R_{par} of 8 T CIS (shown in Fig. 6) are

$$R_{par} = R_s \frac{L}{W} = 100\,m\Omega/\square \times \frac{5.5\,\mu m}{1.2\,\mu m} = 0.46\,\Omega \tag{4}$$

$$R_{gnd} = R_s \frac{L}{W} = 100\,m\Omega/\square \times \frac{1800\,\mu m}{4.12\,\mu m} = 43.69\,\Omega \tag{5}$$

where, W and L respectively represent the width and length of the metal interconnection line, and R_s represents the sheet resistance of the interconnection line.

Fig. 7 shows the PSC simulation result of RDC2 in a 2000 × 2 row drive array. All the parameters used are shown in Table I. V_{out1}, V_{out200}, V_{out900}, and $V_{out2000}$ represent the output voltages of the 1st, 200th, 900th, and 2000th rows in RDC2, respectively. The simulation results show that the output voltage of RDC2 is not zero, which proves that the parallel operation of the M_{PC} that turns off all pixels does cause a PSC in

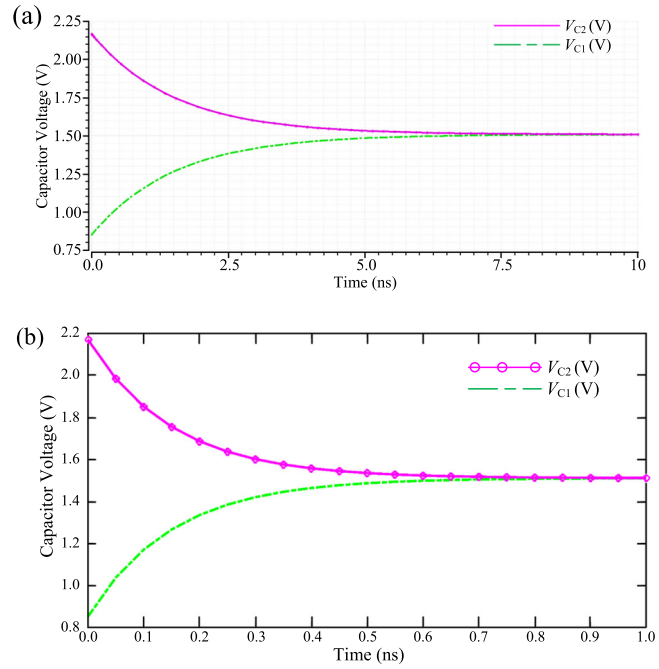

Fig. 11. The simulation result of V_{C1} and V_{C2} under different conditions: (a) The SPICE simulation result; (b)The simulation result of mathematical model.

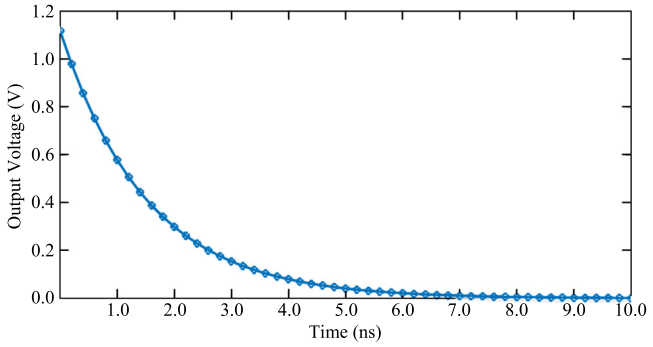

Fig. 12. The mathematical model simulation result of signal attenuation.

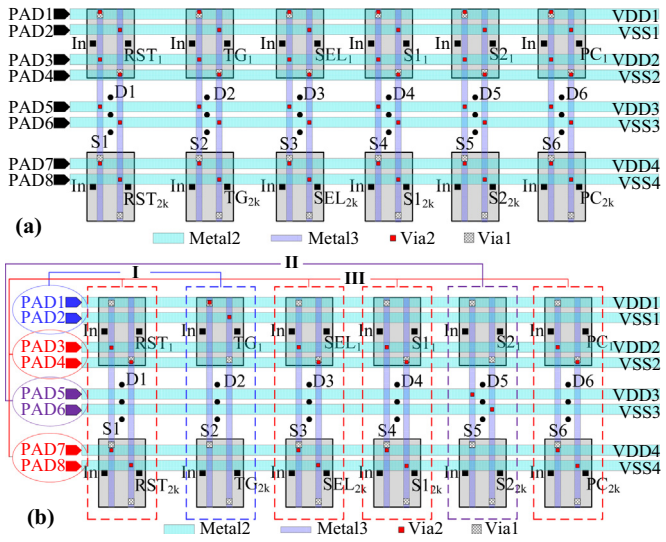

Fig. 13. Different power supply structures: (a) The shared power supply structure before optimization; (b) The separate power supply structure proposed in this paper.

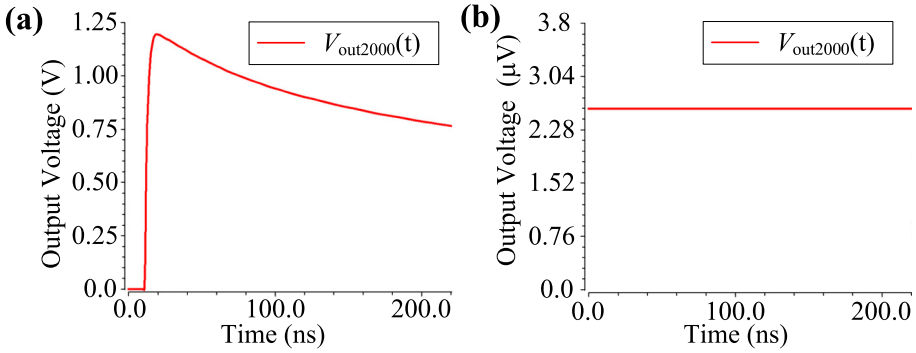

Fig. 14. (a) The simulation output voltage of 2000th row driver in RDC2 before the power supply structure is optimized; (b) The simulation output of 2000th row driver in RDC2 after the power supply structure is optimized.

the CIS. As can be seen from this figure, the voltage increments on the output nodes of RDC2 caused by PSC are different. This phenomenon originates from the voltage drop caused by the parasitic resistance on the power bus connecting different row drivers. The further away from the ground pad, the lower the voltage increment becomes.

When the output V_{out}(t) of RDC2 satisfies the relation:

$$V_{out}(t) \geq A_1 V_{signal} + V_{th\text{-}MS2} \tag{6}$$

the M_{S2} would be turned on by mistake. The signal charge stored in C1 will be leaked into C2. As a result, the signal voltage on C1 will increase and the reset voltage on C2 will decrease, which will attenuate the output signal of the CDS circuit. Therefore, only a part of row drivers in RDC2 can cause signal attenuation.

If the equivalent resistance of RDC2 is assumed to be R_Q, I_Q can be expressed as:

$$I_Q = \frac{R_{gnd}}{(R_{gnd} + R_{S2})} \cdot I_A \tag{7}$$

This formula shows that R_{gnd} is also one of the main factors affecting PSC. Fig. 8 shows the simulation results of V_{outn}(t) (the output voltage of the Nth row driver that closest to the ground bus V_{SS}) under different R_{gnd}. Simulation results indicate that a larger R_{gnd} leads a severer PSC.

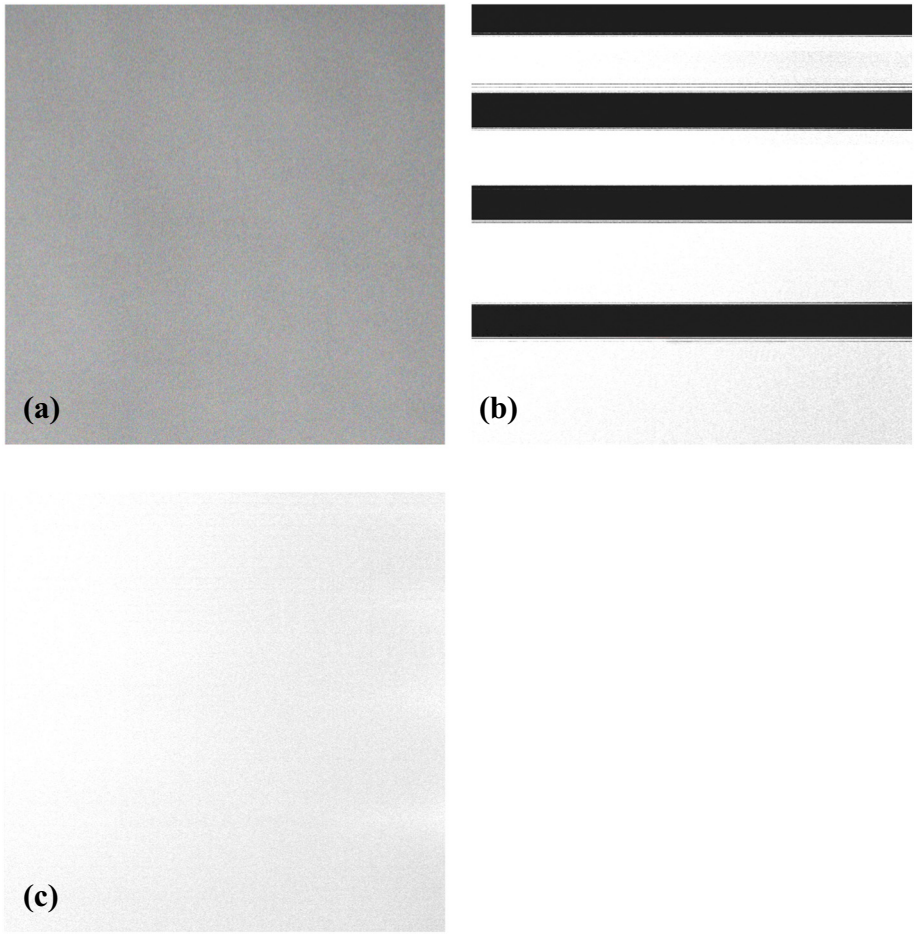

Fig. 15. Images captured by different chips: (a) The image without static black stripes captured by the 1st chip design under middle light intensity; (b) The image with static black stripes captured by the 1st design of test chip under saturated exposure; (c) The image without static black stripes captured by the 2nd chip design under saturated exposure.

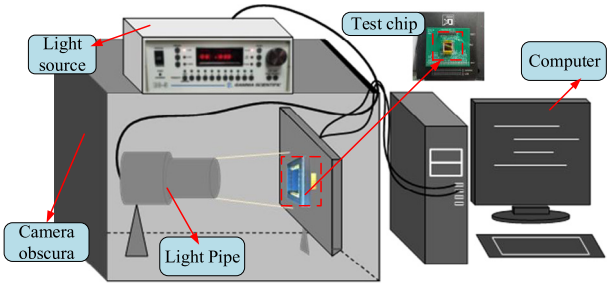

Fig. 16. The diagram of the test system used in this paper.

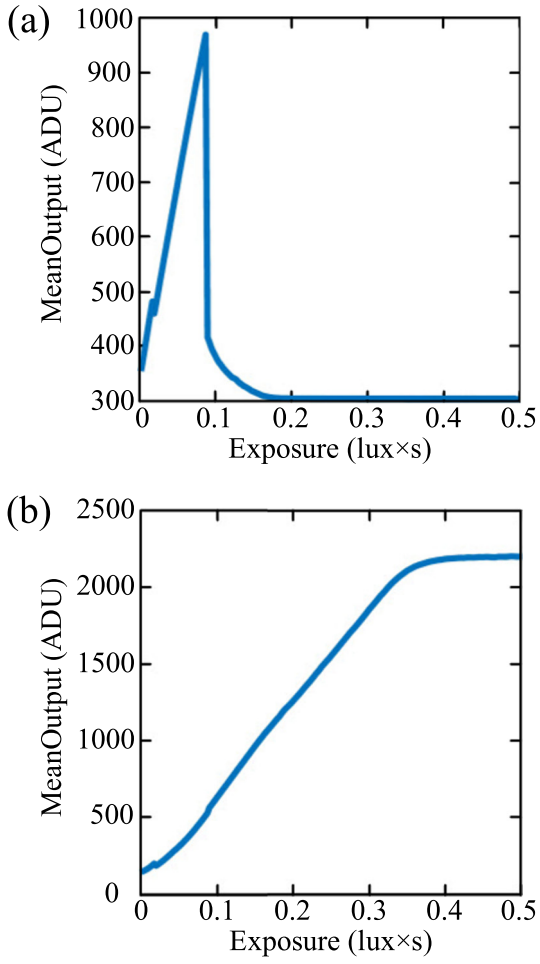

Fig. 17. (a) Photoresponse of the pixels at the black strip in the 1st chip design; (b) Photoresponse of the 2nd chip design.

Table I
Parameters of the simulation circuit.

Symbol	Parameter	Value
V_{DD}	Power supply voltage	3.3 V
C_L	The value of load capacitor C_L	4 pF
C_{par}	The value of parasitic capacitor C_{par}	6 fF
R_S	The sheet resistance of interconnect lines	0.1 Ω/□

Along with the increase in R_{gnd}, the time constant of each 2R2S equivalent circuit in RDC2 increases. Then, the downward trend of $V_{outn}(t)$ would be smoother. In summary, the severity of the PSC depends on the R_{gnd} and the relative distance to the ground pad.

Based on the photoelectric conversion characteristics, the voltage drop on C1 caused by photogenerated electrons can be expressed as:

$$\triangle V_{sig} = \frac{P \cdot A_{pixel} \cdot t_{INT} \cdot \lambda \cdot QE \cdot CG}{h \cdot c} \cdot A_1 \tag{8}$$

where P is the input optical power in (W/cm^2), A_{pixel} is the pixel size in (cm^2), t_{INT} is the integration time, h is Planck's constant(J·s), c is the velocity of light, λ is the optical wavelength, QE is the overall quantum efficiency per pixel, CG is the conversion gain per pixel in (μV/e$^-$).

As shown in Fig. 4, when the input of RDC1 is the falling edge of the 8 T pixel signal PC or S1, and the input of RDC2 is S2 (keep 0 V), the voltage $V_{gs\text{-}MS2}$ can be expressed as:

$$\begin{aligned} V_{gs\text{-}MS2} &= V_{out}(t) - A_1 V_{signal} \\ &= V_{out}(t) - A_1 (V_{reset} - \triangle V_{sig}) \\ &= V_{out}(t) + \frac{P \cdot A_{pixel} \cdot t_{INT} \cdot \lambda \cdot QE \cdot CG}{h \cdot c} \cdot A_1 - A_1 V_{reset} \end{aligned} \tag{9}$$

From Eq. (9), $V_{gs\text{-}MS2}$ is mainly related to the exposure and PSC. When the PSC and exposure follow

$$V_{gs\text{-}MS2} \geq V_{th\text{-}MS2} \tag{10}$$

M_{S2} would be falsely turned on, leading a signal attenuation.

To further describe the effect of PSC and exposure on pixel signal in 8 T global shutter CIS, this section simulates the relationship among $V_{gs\text{-}MS2}$, exposure, and V_{outn} based on (8). All the parameters used are shown in Table II and the simulation results are shown in Fig. 9. The output signal would be attenuated when $V_{gs\text{-}MS2}$ reaches the turn-on voltage of M_{S2}. Fig. 9 shows that $V_{gs\text{-}MS2}$ can only be turned on under strong exposure (or long-exposure) and high V_{outn}.

3.3. Calculation of signal attenuation

The reset voltage of a pixel is generally much higher than the signal voltage at which the pixel is saturated. Therefore, M_{S2} is in the saturated region when it is turned on. At this time, the pixel circuit can be replaced by a circuit model as shown in Fig. 10, where R_{S2} is the saturation resistance of M_{S2}.

At the same time, C1, C2, and R_{S2} should be regarded as a series relationship. According to Kirchhoff's law:

$$V_{ba}(t) + \tau \frac{\partial V_{ba}(t)}{\partial t} = 0 \tag{11}$$

where τ is the time constant, $V_{ba}(t)$ is the voltage across R_{S2}. $V_{ba}(t)$ and τ can be calculated as:

$$\begin{cases} V_{ba}(t) = V_{C2}(t) - V_{C1}(t) \\ \tau = \dfrac{C1 \cdot C2 \cdot R_{S2}}{C1 + C2} \end{cases} \tag{12}$$

Eq. (11) is a first order linear differential equations with constant coefficients, so its general solution is

$$V_{ba}(t) = C \cdot \exp\left(-\frac{t}{\tau}\right) \tag{13}$$

where C is an arbitrary constant. By (11) and the initial condition:

Table II
Parameters of the mathematical model for $V_{GS\text{-}MS2}$.

Symbol	Parameter	Value
A_{pixel}	Pixel size	5.5 μm × 5.5 μm
V_{reset}	Reset voltage of pixel	2.55 V
h	Planck constant	6.626 × 10^{-34} J·s
c	Velocity of light	3.0 × 10^{10} cm/s(λ = 550 nm)
QE	Quantum efficiency	70%(λ = 550 nm)
CG	Conversion gain	36.42 μV/e$^-$
$V_{th\text{-}MS2}$	The threshold voltage of M_{S2}	0.35 V
A_1	The gain of M_{SF1}	0.85

$$\begin{cases} V_{C1}(0_+) = A_1 V_{signal} \\ V_{C2}(0_+) = A_1 V_{reset} \end{cases} \tag{14}$$

The $V_{ba}(t)$ can be gotten

$$V_{ba}(t) = (A_1 V_{reset} - A_1 V_{signal}) \cdot \exp\left(-\frac{t}{\tau}\right) \tag{15}$$

Then the loop current $i(t)$ can be expressed as:

$$i(t) = \frac{A_1 V_{reset} - A_1 V_{signal}}{R_{S2}} \cdot \exp\left(-\frac{t}{\tau}\right) \tag{16}$$

Since the capacitance values of C1 and C2 are equal, the same voltage change across the two capacitors can be given as:

$$\Delta V_C = \frac{1}{C} \cdot \int_0^t i(t)dt \tag{17}$$

According to (16) and (17), the voltages of C1 and C2 in Fig. 10 change with time as:

$$V_{C1}(t) = A_1 V_{signal} + \frac{(A_1 V_{reset} - A_1 V_{signal}) \cdot \tau}{R_{S2} \cdot C1} \cdot \left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \tag{18}$$

$$V_{C2}(t) = A_1 V_{reset} - \frac{(A_1 V_{reset} - A_1 V_{signal}) \cdot \tau}{R_{S2} \cdot C2} \cdot \left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \tag{19}$$

In order to verify the correctness of (18) and (19), the SPICE simulation and mathematical model simulation were performed based on the circuit in Fig. 10 and the parameters of Table III. The simulation results are shown in Fig. 11(a) and (b), respectively. And the simulation results of V_{C1} and V_{C2} are shown respectively in green and red line in Fig. 11. Comparing these two figures, it can be found that the circuit simulation results are similar to the results of mathematical model. Thence, the change over time of the voltages on C1 and C2 can be correctly represented by Eqs. (18) and (19).

According to (18) and (19), the pixel output after using CDS is:

$$V'_{output-CDS} = A1A2 \cdot \left(V_{reset} - V_{signal} - \frac{V_{reset} - V_{signal} \cdot \tau}{R_{S2} \cdot C2} \cdot \left(1 - \exp\left(-\frac{t}{\tau}\right)\right)\right) \tag{20}$$

According to (20), the output voltage of the CDS is as shown in Fig. 12 when the image sensor is interfered by the PSC. The simulation parameters are the same as in Table III.

Fig. 12 shows that the output signal voltage is attenuated to 0 V in about 8 ns. The simulation results of power crosstalk in Fig. 7 and Fig. 8 show that there is a slow decline in crosstalk noise after reaching a maximum, which is typically between tens of nanoseconds and hundreds of nanoseconds. The output signal attenuation time is much shorter compared with the crosstalk noise decline time. If the voltage spike caused by power crosstalk in RDC2 can make M_{S2} turn on, the output signal $V'_{output\text{-}CDS}$ of the corresponding row would be attenuated to 0 V. Then, a static black stripe with a gray value of zero would appear in the final output image.

Table III
Simulation parameters for *V*c1 and *V*c2.

Symbol	Parameter	Value
R_{S2}	Saturation resistance of M_{S2}	1.22×10^5 Ω
C_0	The unit-area capacitance of gate oxide	5.75 fF/μm^2
S_{C1}	The area of C1	4.32 μm^2
S_{C2}	The area of C2	4.32 μm^2
$C1$	Capacitance value of C1	24.84 fF
$C2$	Capacitance value of C2	24.84 fF
A_1	The gain of M_{SF1}	0.85
A_2	The gain of M_{SF2}	0.85
V_{signal}	Signal voltage of pixel	1 V
V_{reset}	Reset voltage of pixel	2.55 V

4. Optimized power supply structure

In this paper, a separate power supply structure with four groups of power supply to enhance power drive capability and eliminate the signal attenuation is utilized. Figs. 13(a) and (b) show the shared power supply structure and the discrete power supply structure, respectively. The proposed method divides the four groups of power supplies into three parts. The first part (PAD1 and PAD2) is used to power the row drive circuit that drives the TG separately. The second part (PAD5 and PAD6) is used to power the row driver circuit that drives S2 separately. The third part (PAD3, PAD4, PAD7, and PAD8) is used to power the row driver circuits that drive RST, SEL, S1, and PC simultaneously. In this way, the peak current caused by RDC1 does not charge the output capacitors C_{L2} of RDC2 through the ground bus, which causes no voltage spike on the outputs of RDC2. Thus, the signal attenuation caused by PSC of row drive array is eliminated. Fig. 14 shows the equivalent circuit model simulation outputs of the RDC2 before and after employing the above method. As shown in Fig. 14(a) and Fig. 14(b), the voltage spike induced by PSC in RDC2 can be reduced from 1.17 V to 2.58 μV under the proposed method.

5. Test and results

In this paper, two 8 T GS CISs made in 0.13 μm CMOS process are compared and measured. The CIS using the typical shared power supply structure is called the 1st chip design, and the CIS using the proposed power supply structure is called the 2nd chip design. The pixel array of each test chip counts 2000 × 2000 pixels with a 5.5 μm pitch. The chip output is the digital signal converted by a 12-bit analog to digital convertor.

Fig. 15 shows the images captured by the two chips under uniform illumination of different irradiances. Fig. 16 shows the diagram of the test system. The exposure time and signal gain used in the measurement were 7.27 ms and 1.2 times, respectively. Fig. 15(a) shows the image without static black stripes captured by the 1st chip design under middle light intensity. Then, the image captured by the 1st chip design under saturated exposure is shown in Fig. 15(b). There are four static black stripes caused by PSC, whose position is the location of the four ground pads that power the row drive array in the 8 T GS CIS. Fig. 15(c) is the image captured by the 2nd chip design under saturated exposure. As can be seen from this figure, the static black stripes have been eliminated, which means the signal attenuation caused by the PSC is eliminated.

Based on above measurement conditions, the photoresponse curves of these two chips measured under various illumination intensities are shown in Fig. 17. Fig. 17(a) shows the photoresponse curve of the pixels at the black strip in the 1st chip design, and the pixel array size is 100 × 100. At lower exposure, the output value increases linearly with exposure. When the exposure reaches 0.09 lx × s, M_{S2} is turned on so that the signal charge in C1 leaks into C2, which causes the output value to drop from 960 ADU to 460 ADU. Thereafter, as the exposure continues to increase, the signal charge leaking from C1 to C2 increases. When exposure ≥0.2 lx × s, the most severe signal attenuation will occur. Fig. 17(b) shows the photoresponse curve of the 2nd chip design. From Fig. 17(b), the same conclusion as Fig. 15(c) can be obtained, that is, the separate power supply structure can eliminate signal attenuation. And the output value of the 2nd chip design is increased from 303 ADU to 2200 ADU (the theoretical output signal value when the pixel is saturated) under strong exposure.

6. Conclusion

In this paper, a 2000 × 2 driver array circuit model and a mathematical model with power supply crosstalk and exposure are established to show the effect on pixel output. Based on this model and the simulation, the signal attenuation induced by power supply crosstalk of

row driver array has been investigated. The simulation results indicate that PSC would be more severe with the increase of R_{gnd} in 8 T GS CIS. And the closer the pixel distance is to the shared ground bus, the greater the impact by the PSC. From the mathematical model analysis, it can be concluded that the output signal is attenuated only under strong exposure (or long-exposure) and large PSC. Then, a method by changing the power supply structure is adopted. The utilized method is designed to eliminate the PSC by using multiple power supplies to separately power different columns of the row driver array, thereby eliminating signal attenuation. To support this conclusion, the measurement results of the 1st chip design using the shared power supply structure and the 2nd chip design using the separate power supply structure are shown. The comparison results prove that the proposed method can eliminate the signal attenuation induced by power supply crosstalk of row driver array in global shutter CMOS image sensor.

CRediT authorship contribution statement

Jiangtao Xu:Resources, Writing - review & editing, Supervision.**Feng Li**:Conceptualization, Methodology, Writing - original draft.**Liqiang Han**:Software, Writing - review & editing.**Zhiyuan Gao**:Software, Writing - review & editing.**Han Wang**:Writing - review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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