Nano-MOSFET - Foundation of Quantum Computing Part I

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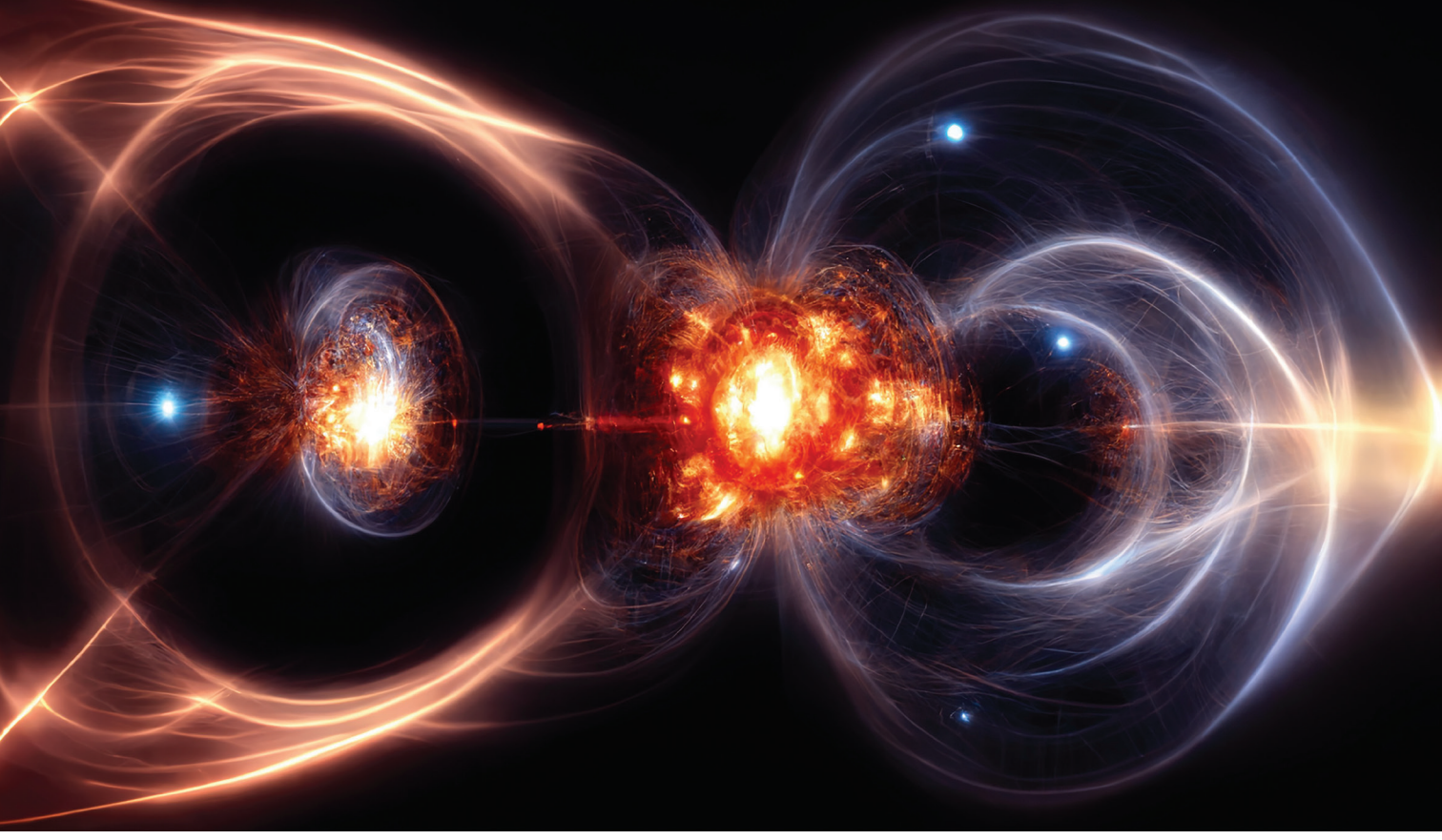

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Nano-MOSFET – Foundation of Quantum Computing Part I

Qubits, Quantum Architecture and Control, Cryo-CMOS

AS BIG STRIDES WERE BEING made in many science fields in the 1970s and 80s, faster computation for solving problems in molecular biology, semiconductor technology, aeronautics, particle physics, etc., was at the forefront of research. Parallel and super-computers were introduced, which enabled problems of a higher level of complexity to be solved. At about the same time, Nobel-laureate physicist Richard Feynman launched what seemed at the time a wild idea; to build a computer based on quantum physics concepts such as superposition and entanglement [1]. The outrageousness of his ideas is documented in the book "Surely, You're Joking, Mr. Feynman" [2].

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INTRODUCTION

QUANTUM COMPUTING, BETWEEN WILD IDEA AND REALITY

Soon thereafter a number of applications were proposed that could be solved on a quantum computer in a fraction of the time it would take on a classical computer, such as the Shor algorithm of prime number factoring [3]. This led to the start of research towards building a quantum computer, but many challenges were in front of its implementation, such as the milli-Kelvin temperatures in most cases, at which the quantum elements holding and processing the information needed to be operated in order for their quantum state to be preserved long enough to be detected. These challenges prolonged the introduction of the first practical quantum computers into the 21st century when important technological advances took place in different domains, most importantly in semiconductor technology.

QUANTUM COMPUTING (QC) ENVIRONMENT TODAY

From timid attempts at QC in the first 15 years of the 21st century, the development of practical quantum computers has transitioned into high gear over the past few years. There are three key elements contributing to this accelerated progress. First, and most importantly, is the unparalleled advancement of semiconductor technology with devices approaching atomic material limits enabling implementation of the hardware base of a practical QC. Second, the level of investment in QC start-ups reached last year $3 Billion of the $5 Billion invested in the last 20 years; QC is a $490 million market this year growing at 24% for the next 3 years, according to Hyperion Research. In addition to IBM, Rigetti, D-Wave and Quantinuum, which have introduced their QCs a number of years ago, new companies such as IonQ, Quantic Inc., EeroQ, Quantum Motion, Quantum Machines, etc., tout their entry in this field. Last, but not least, is the interest of enterprises in applying quantum computation in their business; while only 3% of the polled companies are using it today many others are preparing for its use, according to a study by Cap Gemini.

From timid attempts at QC in the first 15 years of the 21st century, the development of practical quantum computers has transitioned into high gear over the past few years. There are three key elements contributing to this accelerated progress.

With the expansion of the offer of QCs there is the question how to estimate the compute potential of one or another offering. The widely accepted measure is the number of *Quantum Bits* (qubits), equally representing the memory capacity and the number of elementary gates (compute elements). Today, existing QCs have around 100 qubits (127 for IBM Eagle [4]), the number of which is projected to grow by one order of magnitude within 2 years [4]. There are new proposals to quantify the power of a QC, such as *Algorithmic Qubits*[5] or '*Scale (number of qubits) + Quality (quantum volume) + Speed (CLOPS)*' [6].

As outlined in the following section, quantum bits can be implemented by different quantum elements; as applications that will benefit from the power of QC will need hundreds of thousands and maybe up to one million qubits, the technology that will achieve this complexity will be the one with the highest scalability.

QUANTUM COMPUTING BASICS

THE QUBIT

CONCEPT, IMPLEMENTATION ALTERNATIVES

A quantum computer (QC) is generally made of an array of qubits implemented in one of many solid-state technologies and operating at deep-cryogenic temperatures (10 to 20 mK). The unit of information and, at the same time, the elementary logic gate processing the information it stores, the qubit, can be implemented as the quantum state of the spin of an electron, spin-qubit, or of that of a superconducting resonator, transmon [7], or in other technologies, such as ion traps [8]. Superconducting qubits are a more mature

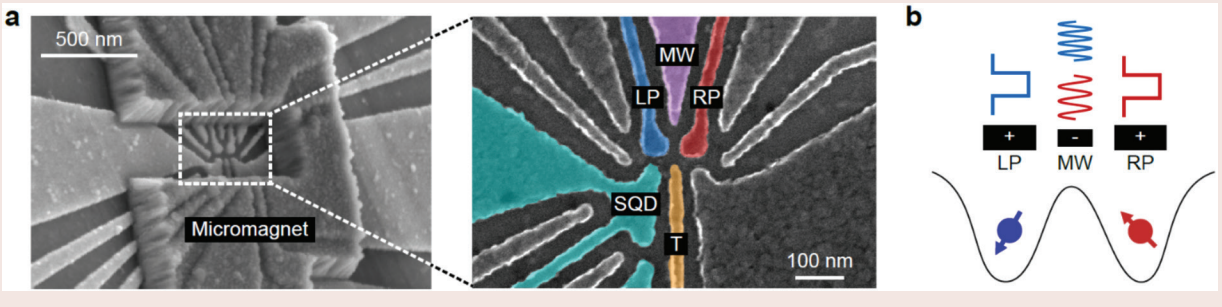

FIGURE 1 a. SEM of a ^{28}Si/SiGe DQD Left: Top view with micromagnet, Right: Detail of DQD b. Pulsing scheme of the DQD.

technology and currently make up the majority of large-scale QCs [4], [9], [10].

Silicon spin qubits are a promising candidate for scalable QCs, [14], [17], [22], due to their size, long coherence times, the duration during which their state is preserved and can be detected, and potential for co-integration with the required classical control and readout electronics. In addition, recently semiconductor spin qubits have been demonstrated to operate at 4K, thus accelerating the achievement of a compact QC [22].

The qubit can assume the value of one of the base states, $|0\rangle$ and $|1\rangle$, equivalent to the '0' or '1' in a classical computer, but at any time, it can be in a superposition of quantum states $|0\rangle$ and $|1\rangle$ with probability α_0 and α_1, respectively, represented by its quantum state $|\psi\rangle$:

$$|\psi\rangle = \alpha_0 |0\rangle + \alpha_1 |1\rangle,$$

The state is represented by a unitary vector in a 3D coordinate system z, x, y, commonly visualized as the *Bloch sphere*. The state can be modified by an external excitation in the form of a train of microwave pulses; the result is a rotation of a specified angle on the Bloch sphere, which represents an elementary instruction in a QC.

The following subsection describes the practical implementation of Silicon spin qubits using semiconductor fabrication technology, as it is the strong belief of the authors that this is the technology that will lead to the implementation of a QC with hundreds of thousand qubits.

SPIN-QUBIT IMPLEMENTATION

Spin-1/2 particles, such as electrons, are perfect two-level systems in nature, making them ideal candidates for qubits, as there is no other state for quantum information to leak out of the computational space [11]. Single electrons can be trapped in quantum dots (Figure 1) in semiconductors such as silicon. These quantum dots are defined electrostatically by biasing the voltages on the metal gates, LP and RP in Figure 1, which are lithographically patterned on top of the substrate, resembling the conventional semiconductor MOSFET. Leveraging existing advanced manufacturing technologies, these qubits can be produced in large scale, and integrated with CMOS-based electronics for control and readout [12], [29], [30].

Spin states are highly robust against electric field fluctuations, granting them good coherence. Isotopic purification of silicon substrates reduces the abundance of ^{29}Si, the only Si isotope that carries non-zero nuclear spin, further improving the coherence times of electron spins. The dephasing time ($T2^*$) of spin qubits in purified silicon (^{28}Si) is reported to be 10 - 120 µs [13], [14], while the relaxation time (T1) is typically in the range of a few hundred milliseconds to a few seconds [13]. Such relatively long coherence times and the highly biased error syndrome ($T1 >> T2^*$) position spin qubits favorably for realizing fault-tolerant quantum computers using quantum error correction. Figure 1a shows a scanning electron microscope (SEM) view of a double quantum dot (DQD) device made in isotopically enriched ^{28}Si/SiGe heterostructure. The device is wire-bonded onto a printed circuit board (PCB), which is cooled in a dilution refrigerator to below 10 mK. The quantum dots are formed underneath the tips of the plunger gates LP and RP, where the single electrons are captured. The gate SQD stands for a Sensing Quantum Dot, which is used to detect the states of the two qubits.

The qubit frequencies are determined by the Zeeman splittings of the spin states in an in-plane magnetic field (B_{EXT}), generated by an external superconducting magnet and a micromagnet made of Cobalt sitting on top of the device (Figure 1a and Figure 2), which is magnetized in the same direction (z). We can thus encode the spin-up state as $|1\rangle$ and the spin-down state as $|0\rangle$. The micromagnet is designed such that the two qubits feel different local magnetic fields (longitudinal gradient (y) assuring the addressability of the qubits). In addition, the micromagnet also creates a transverse field gradient (x), forming synthetic spin-orbit interaction [15]. Single-qubit gates are enabled by electric-dipole spin resonance (EDSR), in which microwave signals at the qubit frequencies are sent to gate MW (Figure 1a and b.) to spatially oscillate the electrons in the z direction. The electrons are therefore subject to oscillating magnetic field signals along the x direction, which rotate the spins in the Bloch sphere. Moreover, single-qubit gates can also be implemented by EDSR with intrinsic spin-orbit interaction in certain materials [15], or by electron spin resonance (ESR), in which the magnet field component in microwave signals is utilized [15].

QUANTUM CIRCUITS AND IMPLEMENTATION

Universal quantum computation requires a gate set containing not only single-qubit gates but also at least one type of two-qubit entangling gate, such as a controlled-NOT gate or a controlled-phase gate.

The gate T (Figure 1a) controls the tunnel barrier between the two dots and thus is used to turn on and off the exchange interaction between the two spins for two-qubit gates [15], [16]. The exchange interaction makes the anti-parallel spin states, $|01\rangle$ and $|10\rangle$, shift down in energy (Figure 3). Therefore, the frequency of each qubit becomes dependent on the state of the other one, giving rise to direct implementations of controlled-rotation (CROT) gates and controlled-phase (CPHASE) gates [13]. A CPHASE gate can be implemented by directly applying a baseband voltage pulse to the T gate to open the barrier, such that each qubit obtains a conditional phase under the exchange interaction. A CROT gate

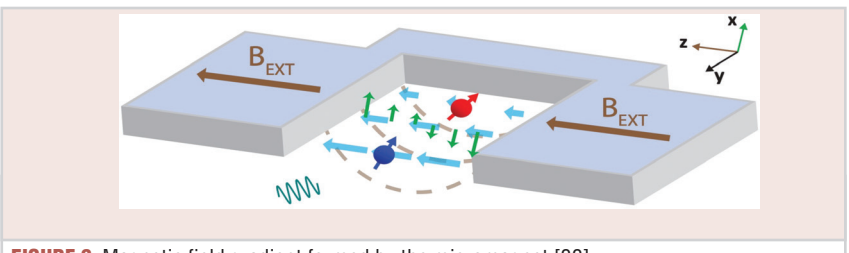

FIGURE 2 Magnetic field gradient formed by the micromagnet [22].

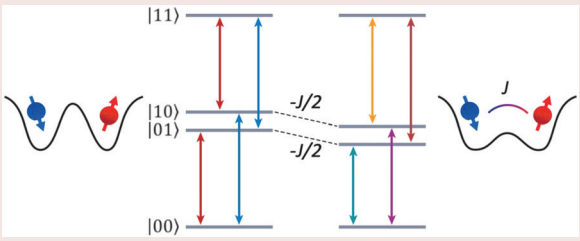

FIGURE 3 Energy level diagram without (left) and with (right) exchange coupling (J) [22].

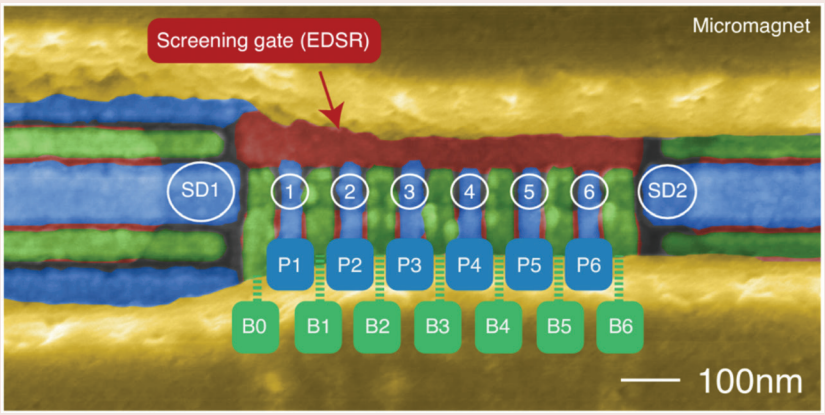

FIGURE 4 A six-qubit array implemented in ^{28}Si/SiGe at QuTech [19].

can be implemented by driving one of the conditional frequencies (such as the green or yellow transition of qubit 2) while opening the barrier (Figure 3).

Performing an operation on a single qubit is equivalent to performing a rotation of the qubit state in the Bloch sphere. The accuracy of an actual qubit operation can be measured by the *fidelity*, which is similar to the bit error rate in a classical digital system. The fidelity of a perfect operation is 100%, but in practice, the fidelity is limited by nonidealities in the control signals and by the implementation of the physical qubits.

Spin qubits in semiconductors have been successfully operated with very high fidelities, with the single-qubit gate fidelities approaching 99.99% [17] and the two-qubit gate fidelities recently exceeding 99% [14], the widely quoted fault-tolerant threshold [18]. Operations of multiple qubits have been demonstrated in a linear 6-dot array [19] (Figure 4), and a 2×2 array [20], with further scaling underway. Leveraging advanced manufacturing technologies, spin qubits have been successfully made by Intel using commercial FinFET technology on 300 mm wafers [21]. The potential of silicon spin qubits is underlined by recent efforts on advancing this technology, such as IBM [22], HRL [23], IMEC [24], and CEA-LETI [25], which have reported their home-made qubits. It is worth noting that in silicon, spin qubits have been proved functional at elevated temperatures. The first demonstrations show single- and two-qubit gates at above 1 K [26], [27] with the readout fidelity remaining high (~95%) up to 1 K [28]. Remarkably, a recent publication reports single-qubit gates implemented at above 4 K [22], a critical temperature, which allows co-integration with cryogenic electronics and cooling by liquid Helium.

QUANTUM COMPUTER ARCHITECTURE AND CONTROL

QC FULL STACK

The control of a qubit starts from a quantum algorithm, described in a certain programming language that is compiled into quantum circuits, i.e., a sequence of operations to be applied on a set of qubits. Quantum arithmetic is also used in this context, along with compilation of certain functions into a quantum instruction set used for quantum execution (QEX) and error correction (QEC). Finally, the QEX and QEC are implemented using the quantum-classical interface, which operates directly on the qubits. This process is depicted in Figure 5 and is referred to as the quantum-computing full stack.

CONCEPTUAL QUANTUM PROCESSOR

The high-level architecture of a QC is shown in Figure 6 and is comprised of the Quantum Processor containing the qubits typically cooled at 10-100 mK for solid-state technologies and the classical control electronics generating the electrical signals needed to perform quantum instructions and retrieve the results by sensing the states of the qubits. Today, the bulky instrumentation generating the necessary high-precision signals used to control qubits is placed outside the dilution refrigerator at room temperature and its connections to the cryogenic qubits require long coaxial cables and several steps of thermalization.

In 2016, we proposed to move the control functions to cryogenic temperatures, close to those of the qubits, so as to achieve a more compact and scalable solution [29]; the most important advantage of this solution, however, is reliability. In this context, many components necessary to control qubits were implemented in standard CMOS technologies and successfully tested at ~4 K [30], [31], [32], [33]. CMOS technologies operating at deep-cryogenic temperatures are known collectively as *Cryo-CMOS* integrated circuits and, while theoretically possible, so far, no IC has been demonstrated for the control of qubits that also includes detection of and correction of error for a fault-tolerant QC.

The proposed quantum-classical interface based on cryo-CMOS is shown in more detail in Figure 7. The signals generated with a very tight control in amplitude, frequency, and phase use an envelope that must be programmable both in shape, usually Gaussian or raised-cosine, or even square, and in duration, generally around 20 to 60ns.

Once the components of the quantum-classical interface are defined, one must implement them, so as to meet the specifications at a wider range of temperatures than just the nominal temperature of operation of 1-4 K considering self-heating; see the Cryo-CMOS Section. The specifications for a cryo-CMOS control interface are not enumerated in any standard as today's approach in quantum-computing labs is to use topnotch equipment placed at room-temperature to ensure that qubit performance is not limited by the electrical control and readout. Although the fidelity should be as close as to 100%, as mentioned in the Quantum Circuits and Implementation Section above, a target fidelity above 99% is usually assumed as the threshold to enter the so-called fault-tolerant quantum computation regime, in which practical quantum algorithms can be executed reliably made also possible by the use of quantum error correction.

When scaling to larger quantum processors, the use of off-the-shelf equipment starts to show limitations even with room-temperature electronics, as direct copying the control system for 2-qubit experiments to a 100-qubit experiment is unfeasible due to both cost and size. This has led to the ad-hoc design of room-temperature control systems, e.g., as described in [34]. Having to design such application-specific equipment, even at room temperature, already requires a clear quantification of specifications on the electrical signals to be generated and read out.

In general, the trend is to achieve higher levels of integration, possibly including the qubit, depending on whether they will be operated at higher temperatures than milli-Kelvin in the future. Regardless of the feasibility of the latter, designers are likely to choose the (Bi)CMOS technology node that best satisfies the requirements in terms of scalability, power dissipation, noise, etc., for system level integration. For example, for a truly scalable QC and over 1000 qubits, an overall power dissipation per qubit of cryo-CMOS control will need to be restricted to about 1mW/qubit to enable today's refrigeration units to absorb the thermal emissions of the control circuits.

When scaling to larger quantum processors, the use of off-the-shelf equipment starts to show limitations even with room temperature electronics, as direct copying the control system for 2-qubit experiments to a 100-qubit experiment is unfeasible due to both cost and size.

This is currently one of the hardest challenges. Furthermore, in the case of Cryo-CMOS circuits the design process must be supported by proper modeling of transistors and passive elements described in the Cryo-CMOS Section below.

Such a very tight constraint on the power dissipation is exacerbated by the need to maintain high performance in the electronic interface–in terms of noise, accuracy and speed–not to degrade the fidelity of the quantum operations, which are affected both by the inherent fidelity of the qubits and the systematic and random errors introduced by the electronics.

One of the first challenges in the design of the quantum-classical interface is the derivation of specifications on the overall performance of the interface and, in turn, on its components. Ultimately, the constraint on fidelity must be met that in turn, must be related to the components in a given control architecture. To address this issue, we have completed a comprehensive study of the impact of any non-ideality of the control electronics on the qubit fidelity by investigating via simulations and analytical derivations how errors in the control electronics, such as noise and inaccuracies, result in a fidelity degradation for each quantum

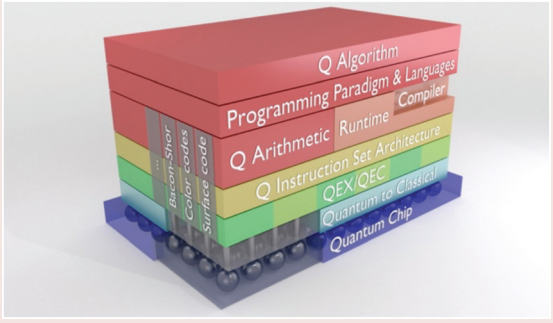

FIGURE 5 The quantum-computing stack from the public talk in [29]. Drawing by Harald Homulle (2016).

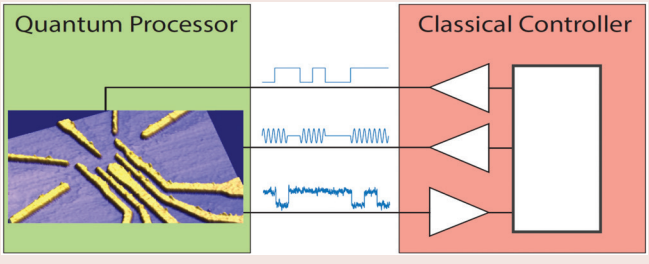

FIGURE 6 Conceptual Architecture of a QC.

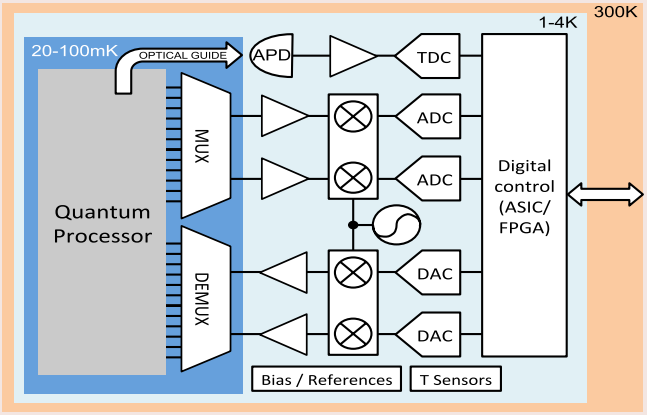

FIGURE 7 Generic architecture of quantum-classical interface for the control of qubits.

TABLE 1 **Example of error budget on the specifications of a microwave pulse used to perform a rotation by an angle π at a 1-MHz Rabi frequency on a single-electron spin qubit and targeting a fidelity of 99.9%, i.e., an infidelity of 10^{-3} (including only the infidelity related to error in the electronics and assuming the qubit ideal).**

	NOMINAL VALUE	ERRORS		INFIDELITY
		INACCURACY	NOISE	
Frequency	10 GHz	11 kHz		125×10^{-6}
			11 kHz_{rms}	125×10^{-6}
Phase	0°	0.64°		125×10^{-6}
Amplitude	2 mV	14 μV		125×10^{-6}
			14 μV_{rms}	125×10^{-6}
Duration	500 ns	3.6 ns		125×10^{-6}
			3.6 ns_{rms}	125×10^{-6}
Wideband oscillator noise			7 $nV/\sqrt{Hz}$	125×10^{-6}
Total				10^{-3}

operation, including single-qubit, two-qubit operations, and read-out [35].

As an example, Table 1 illustrates how a total infidelity budget of 10^{-3} (equivalent to a fidelity of $1\text{-}10^{-3} = 99.9\%$) could be *equally* split over the inaccuracy sources listed above. As it will be clear later in the description of the design of the cryo-control IC Horse Ridge [31] in Part II, the minimum power dissipation in the circuit can only be achieved when optimally allocating the infidelity budget. For instance, the budget allocated in Table 1 for timing jitter and inaccuracy can be easily satisfied by a CMOS circuit without incurring any significant power increase, so that most of that part of infidelity budget can be redistributed to more power-hungry specifications, such as the phase and amplitude noise. Regarding the target fidelity, the current approach in the design of cryo-CMOS electronics, including the Horse Ridge chip, aims at minimizing the infidelity induced by the electronics to a level that is negligible with respect to the infidelity of the whole system. For instance, for spin qubits achieving a fidelity of 99.9%, thus beyond the threshold for enabling fault-tolerant operation, a typical target fidelity for the electronics can be set in the order of 99.99%, so that the electronics is not limiting the total fidelity. This is reasonable today as the qubits are the most precious resource in the system, but the situation will likely be different in the near future. With the constant improvement of qubit material and operation, and especially with the increasing scale of quantum processors, the electronics could become a major bottleneck, pushing for a larger share of the infidelity budget to be assigned to the electronic interface. As a consequence, optimization of the electronics and its impact on the fidelity will have an even higher relevance in the coming years.

For this reason, Van Dijk et al. designed a tool, SPINE (SPIN Emulator) [36] described in Part II, with the purpose of deriving specifications for the quantities contributing to the inaccuracy, such as, the amplitude, frequency, phase of the carrier, the duration of the envelope and the overall noise of the oscillator, so as to achieve a fidelity of 99.9%, as can be seen listed in Table 1. The availability of a design tool such as SPINE to co-simulate integrated electronics and qubits in a typical VLSI EDA environment, such as Cadence, was instrumental in the design of the Horse Ridge chip that can control up to 128 qubits. We foresee that the growing complexity of the cryo-CMOS electronics will need to be supported by an increased flexibility and coverage of EDA tools, eventually extending the verification beyond the pure electronic/qubit interface and including the higher layers in the quantum-computing stack in Figure 5.

CRYO-CMOS – SEMICONDUCTOR DEVICE OPERATION AT CRYOGENIC TEMPERATURES

OPERATION, CHARACTERIZATION AND MODELING

The first question that needed to be answered before embarking on the complex design of the quantum control electronics was whether MOSFETs fabricated in deep-submicron (DSM) technologies operated at 1-4 K similarly to room temperature. In order to answer this question a test chip was designed and fabricated in 2015 in two technologies, 0.16-μm and 40-nm [29], [37]. Transistors with geometries of varying aspect ratios and dimensions were implemented.

These two mature CMOS processes were characterized at cryogenic and room temperatures; the differences in behavior and the physics underlying several cryogenic effects are summarized below. The main observation was that measured devices showed correct

transistor operation from 4 K down to 100 mK and our measurements matched previous observations from older processes. The correct MOSFET operation at cryogenic temperatures is however not sufficient for designing the quantum control ICs, as accurate compact models for these temperatures are needed; foundries do not provide such models limiting the range of validity to -55 to 120 °C. Extending the validity of existing models such as PSP or BSIM4 by deriving appropriate model parameters and augmenting them with the physical effects observed, was an essential endeavor for designing the quantum interface.

A sample of measurements of 0.16-µm and 40-nm CMOS-transistor I_d-V_{ds} and I_d-V_{gs} characteristics are shown in Figure 8. The upper row shows the I_d-V_{ds} characteristics of a 0.16 µm Narrow (S) and Long (L) NMOS.

The first plot contains the measurements at 4 K (solid lines) and 300 K (dashed lines). A general increase of ~2x in mobility is clearly visible in the I_d-V_{ds} characteristics of the NMOS, but at the same time, a ~30% increase in threshold voltage was observed. The former is due to an overall decrease in electron scattering, while the latter to an increase in ionization energy [37]; the V_T increase has however a lower impact on I_d. Another difference at 4 K is the reduction of velocity saturation, leading to I_d curves that saturate at a lower V_{ds} compared to those at 300 K.

The following two plots show good matching of simulated characteristics (solid lines) using the extended models compared to measurements (dotted lines) for both 1 K and 100 mK. The appropriate temperature dependence needed to be built into the key model parameters for obtaining the correct behavior, which was easier achieved with a physics-based model (PSP).

The second row of Figure 8 shows the I_d-V_{gs} characteristics of a 40 nm NMOS at temperatures from 300 K down to 4 K, and a 0.16 µm Wide (L) and Long (L) PMOS device at 1 K and 100 mK. From 300 K to 4 K the subthreshold slope (SS) improves between 3.8x for the 0.16-µm NMOS and 3.2x for the 40-nm NMOS, see Figure 9, due to the intrinsic temperature dependence of the diffusion current. However, the measured *SS* improvement of only 3.2-3.8 times is not equal to the ratio of temperatures as implied by the relation between the two:

$$SS(T) = \left[\frac{\partial \log(I_D)}{\partial V_{GS}}\right] - 1 = \ln(10)\frac{nkT}{q}$$

where n is the nonideality factor related to the interface states. The discrepancy can be explained by the incomplete ionization of impurity atoms at cryogenic temperatures, leading to an important increase in the nonideality factor $n(T)$. Figure 9 illustrates the interdependency between n and *SS* as a function of temperature down to mK, which leads to an *SS* improvement to only 25-30 mV/decade. There are other physical phenomena observed at 4 K not present in the standard temperature interval, such as carrier freeze-out of the substrate, which can lead to a "kink" effect in the I_d-V_{ds} characteristic above 2 V in some older processes, starting with 0.16 µm. This is due to the increase of the substrate potential caused by impact ionization at the drain, generating electron-hole pairs with holes flowing through the substrate raising its potential, thus forward biasing the

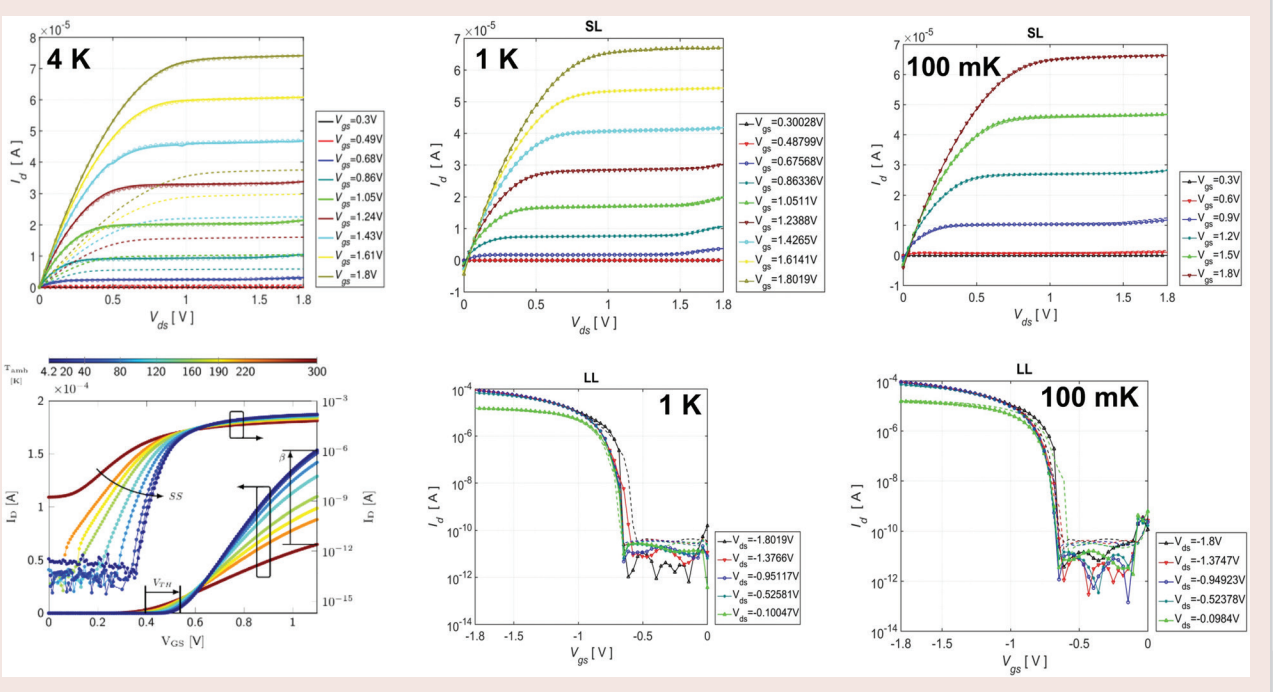

FIGURE 8 Upper Row: 0.16 µm Long/Narrow NMOS I_d-V_{ds}; Lower Row: Bottom left: 40 nm NMOS I_d-V_{gs} as function of temperature, parameter changes indicated; Right two plots: 0.16 µm Large PMOS I_d-V_{gs}.

source–substrate junction. This effect is however not present in processes with feature sizes of 90 nm and below due mainly to the lower supply voltage range; this led us choosing 40-nm CMOS bulk technology for designing the first set of quantum control ICs [30]. Another physical effect observed at cryogenic temperatures in DSM MOSFETs is the discontinuous or bumpy behavior of the subthreshold current explained by the incomplete ionization of dopants and Coulomb barrier [38]. This behavior eliminates subthreshold operation as a choice for analog circuits.

Different behaviors of MOSFETs are observed at cryogenic temperatures depending on the technology they are fabricated; thus, Fully-Depleted Silicon-on-Insulator (FDSOI) MOSFETs and FinFETs show different behavior at 4K than a MOSFET in a standard bulk CMOS process. All MOSFETs in state-of-the-art technologies, however, show correct transistor operation in moderate and strong inversion. From a circuit design point of view, the important differences at cryogenic temperatures are the increase in transconductance efficiency (g_m / I_D) and the reduction in leakage by up to 3-4 times in weak inversion [37]. However, other effects such as device variability, mismatch and self-heating are generally higher at cryogenic temperatures, as detailed in the following subsection. Additionally, while thermal noise is lower, other types of noise, such as flicker noise can be significant, thus especially impacting analog and mixed-signal circuits.

VARIABILITY AND MISMATCH

Apart from the primary *individual* cryogenic DC and AC device behavior, effects involving multiple co-existing devices in a circuit must not be overlooked.

Many precision circuits base their operation on identically sized matched device pairs, assumed to have identical behavior. However, this assumption can become a challenge in reality, as variability inevitably introduces random fluctuations in device parameters. In practice, device pairs become mismatched, resulting in circuits that shift out of specification or even malfunction all together.

Since the cryogenic controller comprises many of these precision circuits, such as references and ADCs/DACs, knowledge and modeling of device matching at deep-cryogenic temperatures is of primary importance during the design phase.

Dedicated test chips were designed featuring large populations of matched pairs of different sizes. By studying the matching of these pairs at different ambient temperatures and device operating regions, the temperature dependency was extensively investigated, in particular, at cryogenic temperatures [39], [40].

It was shown that strong-inversion device matching can be modeled from room temperature down to 4.2 K by [41]:

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \sigma^2(\Delta V_T)\left(\frac{g_m}{I_D}\right)^2 + \sigma^2\left(\frac{\Delta\beta}{\beta}\right)$$

where I_D is the drain current, V_T the threshold voltage, g_m the transconductance, and β the current factor. The σ and Δ operators indicate the standard deviation and parameter difference between devices forming a matched pair, respectively.

The results for devices operated in strong inversion are shown in Figure 10 left. It can be concluded that matching worsens with decreasing temperature and

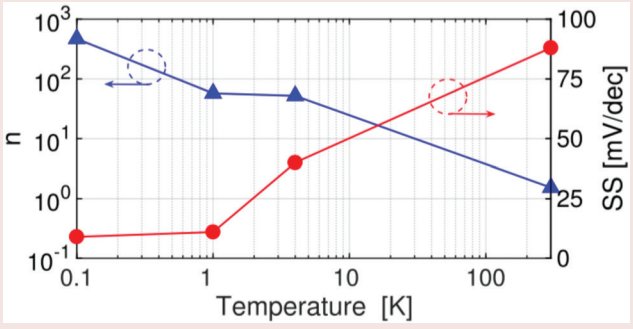

FIGURE 9 Subthreshold Slope (SS) and non-ideality factor (n) temperature dependence.

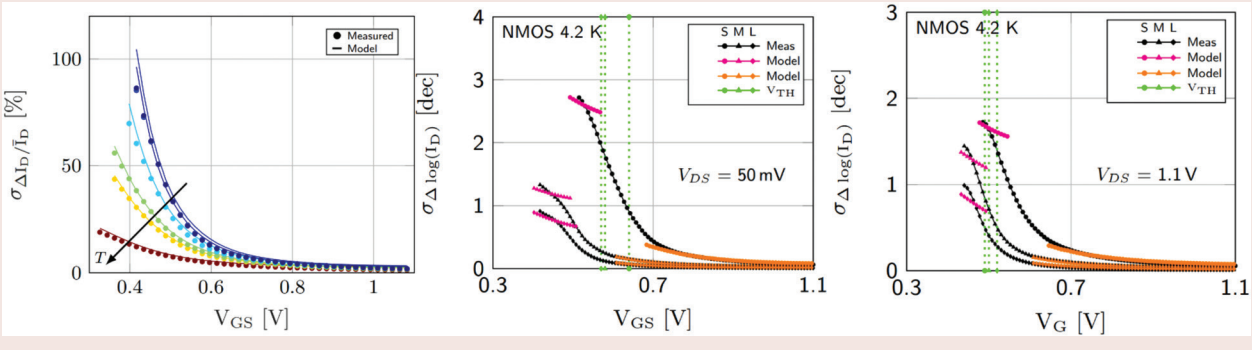

FIGURE 10 Left: Drain-current mismatch as a function of temperature (T = 4.2, 40, 100, 150, 200, 300 K) for a W/L = 1.2µ/400n NMOS device in the moderate to strong inversion regime. Right: Drain-current mismatch for W/L = 120n/40n (S), 360n/120n (M) and 1.2µ/400n (L) NMOS devices at 4.2 K, including subthreshold operation.

that β-variability is the main contributor for devices operated in strong inversion. Devices operating in the subthreshold regime suffer from the additional impact of severely increased subthreshold swing variations [40], marking this regime inappropriate for proper precision circuit operation at cryogenic temperatures, as can be seen in Figure 10 right. The good matching between measurements and the Croon mismatch model augmented for subthreshold [40] can also be seen in these plots.

SELF-HEATING

The different aspects of cryogenic device behavior have one important parameter in common: the temperature at which the device is operating. It is well known that the temperature of active devices can be significantly higher than the ambient temperature due to Joule heating. This is a particularly critical issue as the power budget for the entire CMOS quantum controller is limited to 1 W. Especially in technologies like SOI, that suffer from a limited thermal contact to the surrounding substrate due to the buried oxide, this effect can be very pronounced [42], [43]. Bulk devices are considered to be far less susceptible to self-heating, since these devices are in direct contact with the surrounding silicon. However, since the thermal conductance of silicon is highly temperature dependent, situations similar to those observed in SOI can be expected in bulk cryo-CMOS devices. Recent studies focused on self-heating in bulk devices found at deep cryogenic temperatures, a device temperature significantly higher than the ambient temperature [44]. Some important results of a test chip specifically designed to characterize self-heating by measuring the MOSFET channel temperature and the temperature of individual diodes, can be seen in Figure 11. The temperature sensitivity of the employed sensors, e.g., MOSFET gate material and individual diodes, is shown in Figure 11 left. At extremely low temperatures their sensitivity diminishes, a common challenge in cryogenic temperature sensors [45]. Employing the gate resistance as temperature sensor, the MOSFET channel temperature was extracted at different ambient temperatures and device operating conditions as shown in Figure 11 right. The self-heating effect at deep-cryogenic temperatures can be clearly seen, with a striking 50 K device temperature increase above 4.2 K ambient temperature, at 6 mW power dissipation. After jumping to 50 K, the difference between device and ambient temperature ΔT_G levels off, as shown in the inset. As many device parameters are highly temperature dependent, capturing these temperature effects during circuit simulation are paramount for accurate cryogenic device modeling.

CONCLUSION

In Part I of this article dedicated to the state-of-the-art of QCs based on spin-qubits, we overviewed the technological and societal environment, the fundamental element of a QC, the qubit and its implementation in silicon, the overall QC architecture, a novel electronic control based on Cryo-CMOS, the feasibility of such controller based on the MOSFET operation at 1-4 K, and last, but not least, the challenges for its design.

The facts provided make a strong case for the choice of semiconductor spin-qubits for implementing the QC of the near future with tens or hundreds of thousand qubits.

Part II of this article will present in detail the design, simulation, and implementation of the Cryo-CMOS quantum controller, which can support up to 128 qubits today.

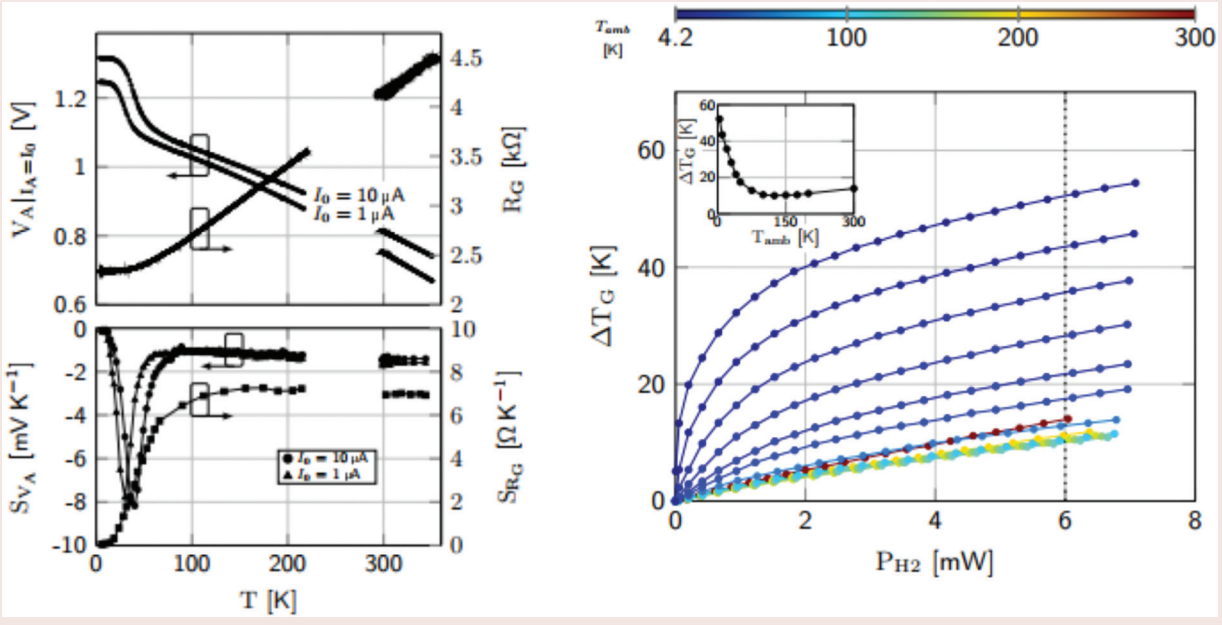

FIGURE 11 Left: Temperature response (top) and sensitivity (bottom) of a MOSFET gate material (right axis) and silicon diodes (left axis) as a function of temperature. Right: Self-heating of a MOSFET as a function of ambient temperature and dissipated power.

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