# Modular time-of-flight image sensor for light detection and ranging

## A digital approach to LIDAR

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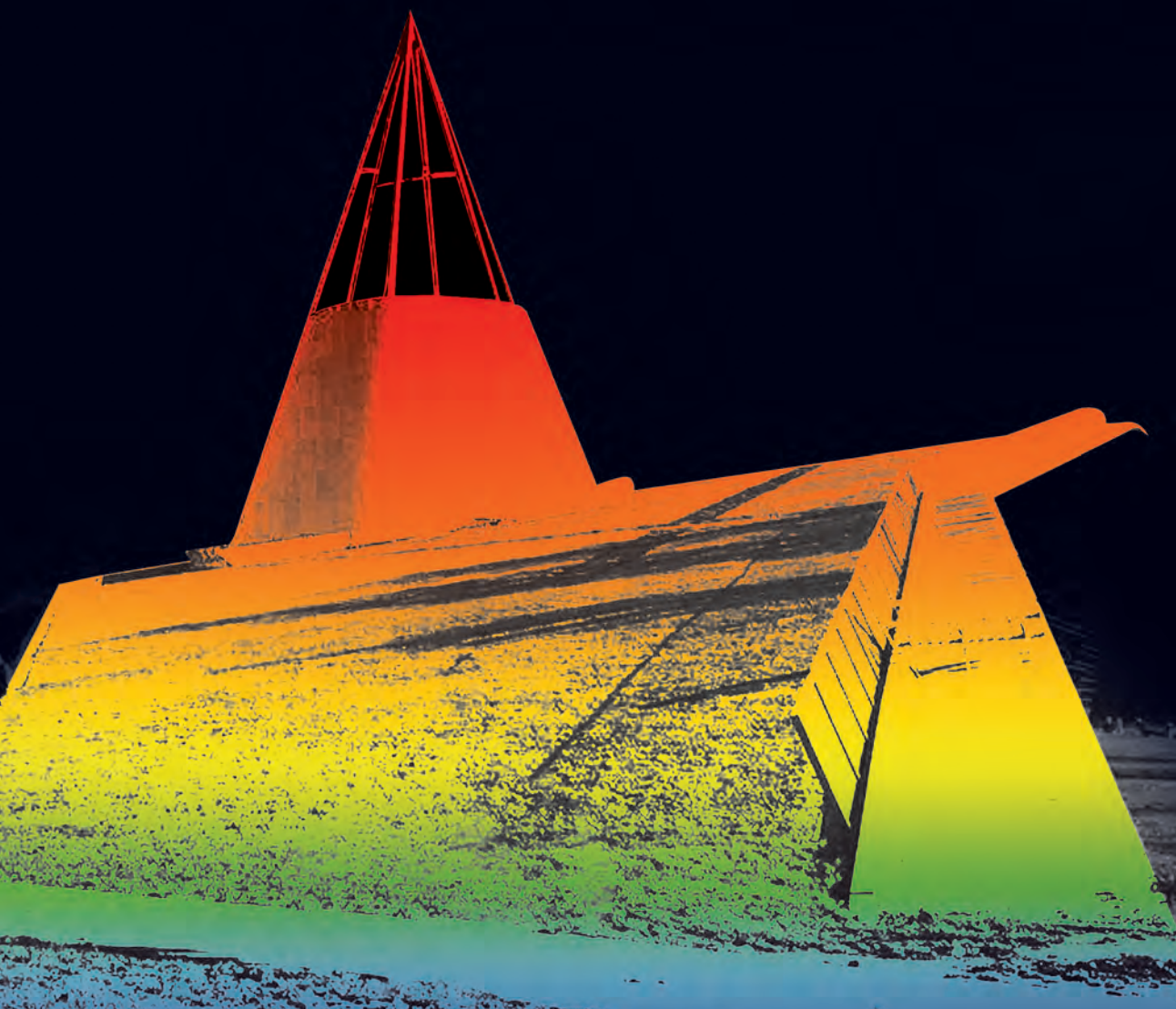

Augusto
**RONCHINI XIMENES**

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## Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. dr. ir. T.H.J.J. van der Hagen.,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op vrijdag 12 juli 2019 om 15:00 uur

door

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geboren in Americana, Brazilië.

Dit proefschrift is goedgekeurd door de promotoren.

*Samenstelling promotiecommissie:*

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|---|---|
| Rector Magnificus, | voorzitter |
| Prof. dr. E. Charbon, | Technische Universiteit Delft, promotor |
| Prof. dr. R.B. Staszewski, | Technische Universiteit Delft, promotor |

*Onafhankelijke leden:*

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| Prof. dr. C. Vaucher, | Technische Universiteit Delft |
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To my family

# Propositions

accompanying the dissertation

**MODULAR TIME-OF-FLIGHT IMAGE SENSOR FOR LIGHT DETECTION AND RANGING**

A DIGITAL APPROACH TO LIDAR

by

**Augusto RONCHINI XIMENES**

1. Access to cutting-edge technology an essential ingredient to complex designs, especially when *in-situ* processing is needed (Chap. 2).
2. Physical constraints and optical setups play a much more important role in active sensing than the sensor itself (Chap. 3).
3. Precise timing measurement is very difficult to achieve: the earlier in the process it can be obtained, the more robust the system is (Chap. 4).
4. An effective circuit resource reuse can greatly improve the system performance; 3D-stacking technology in this respect is essential (Chap. 5).
5. Depth sensing can greatly benefit from digital circuits that are automatically synthesized (Chap. 6).
6. PhD candidates should not be bounded by normal university opening hours.
7. In general terms, a good PhD project should not require more than two tapeouts.
8. Complex system designs, such as direct time-of-flight, often requires complex metrics for evaluation and comparison; those are rare in literature.
9. The success of a PhD thesis is exponentially proportional to the quality of the group where it is developed.
10. A well-guided PhD project can motivate and produce excellent work; the contrary is equally true.

These propositions are regarded as opposable and defendable, and have been approved as such by the promotor prof. dr. E. Charbon and prof. dr. R. Bogdan Staszewski.

# CONTENTS

# SUMMARY

Constant increase in data processing efficiency has enabled, among many other things, the intensive use of depth mapping technologies. Consumer applications, such as gaming, augmented and virtual realities (AR/VR), and other human-machine interfaces, are typically based on intensive image processing, either by triangulation and/or structured light, which has limitations on speed, resolution, range, and robustness to background noise. On the other hand, TOF depth sensing has been investigated in the academic and industrial engineering communities for several years, as an alternative to solve such restrictions, and few products are emerging. Direct time-of-flight (dTOF), specifically, requires more elaborate detectors and data processing, but it has the potential of reaching much longer distances at higher speed and accuracy, with the advantage of being robust to high background noise, making it suitable for space, automotive and consumer applications.

One known drawback of dTOF, however, is data volume. For instance, automotive applications require over 100 m range, only few centimeters accuracy, and multiple measurements for a reasonable precision, which produce data rates that can reach tens or even hundreds of Gbps, in large sensors, thus setting processing constraints to even very efficient GPUs, as well as chip readout capability. It is essential to provide as much on-chip processing as possible, in order to reduce data throughput, thus reducing power consumption and speeding up processing time. Some architectures have been proposed attempting to solve this problem, but the required memory renders them only feasible for an SiPM, single-pixel approach. Another known issue with light detection and ranging (LiDAR) is regarding the interference of multiple systems on each other. A software-based approach has been implemented, but requiring intensive post-processing resources.

In this thesis, a novel approach for on-chip processing is proposed. With the use of cutting-edge 3D-stacking technologies, more flexibility and computational power can be spent on the chip, while not compromising fill factor. A novel proposal for dealing with external interferes is introduced, as well as novel phase/frequency locking solution at the sensor level, as a reference for timing measurements.

# 1

# INTRODUCTION

*Often, the less there is to justify a traditional custom, the harder it is to get rid of it.*

Mark Twain

*In this introductory chapter, an overview on the different aspects of time-resolved imaging will be discussed, including the different approaches, with respect to their basic system operations, technical benchmarks, and the current commercial scenario for the applications. The aim is to provide the reader with the basic technical background to follow the dissertation development and to justify the reasons why this work is relevant for the field. Moreover, in this chapter, the dissertation structure and organization will be discussed, as well as the goals set.*

1

## 1.1. INTRODUCTION

DEPTH sensing technology is a broad definition that relates to the ability of obtaining distance measurement to targets in its field-of-view (FOV). Different technologies are capable of providing distinct information and resolution, by direct depth measurement or through a series of software estimations. With certain overlap or in a completely complementary fashion, each solution is adopted depending on the application.

Nowadays, automotive applications are among the most stringent and demanding. Depth sensing is required to support some level of driving assistance and/or for complete driving autonomy. It is believed that its requirements of robustness and reliability can be met not by a single sensor, but only by a set of complementary technologies [1]. Light detection and ranging (LiDAR) is believed to be an essential technology to enable such applications.

## 1.2. DEPTH SENSING TECHNOLOGIES

The main depth sensing technologies are categorized as shown in Figure 1.1. These technologies are all based on electromagnetic energy, but they are denominated differently depending on the wavelength (or frequency) used. In optical sensing, the energy involved can be treated as waves or particles, which are, once again, characterized with a different name, depending on their relation with the depth estimation.

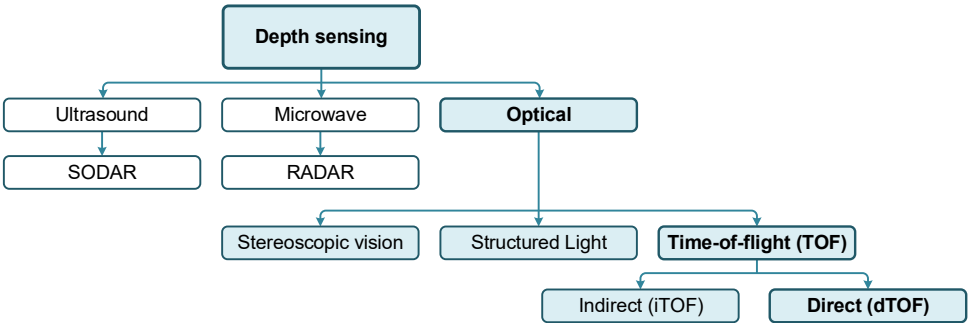



Figure 1.1: Depth sensing technologies: target of this thesis in **bold** text.

The focus of this thesis is on direct time-of-flight (dTOF) imaging. It is based on illuminating the scene with a periodic, short train of pulses of light, and by measuring the time passed during the round trip of the light, between emitter, target, and receiver. By accumulating multiple events into a histogram, the depth can be reconstructed.

Several other approaches of time-resolved imaging are available. Indirect time-of-flight (iTOF) is another *hardware-based* depth estimation, where a modulated light source is used to illuminate the scene, where the captured intensity is used to estimate the phase offset between the emission and detection and, consecutively, the depth; it is commonly used in short-range LiDAR and RADAR. Among *software-based* depth estimation, the most common are stereoscopic vision and structured light; in the former, two cameras provide slightly different RGB images that are digitally processed, and a depth perception can be obtained from parallax extraction; in the latter, a patterned light (typically an array of small dots or stripes) is shone onto the scene and depending on the reflection, *i.e.* size and shape

of the returning pattern, a depth can also be estimated.

Hardware-based depth estimations are more accurate, precise and faster, but they require an active illumination with a certain specific conditions, which are typically expensive. Software-based detections are cheaper, but lack precision, range, accuracy and robustness to environment conditions, while requiring more post-processing, which implicates in the speed and power consumption. DTOF provides the best speed and resolution, but the overall system cost could still be an issue.

In order to diminish the main disadvantage of dTOF, CMOS technology is making its way into the market (in the past, it was dominated by III-V devices), driven by other mass-produced hardware technologies, including the same platforms that RGB CMOS image sensors are designed, which will eventually drive the overall cost of dTOF systems down.

In this dissertation, different aspects of dTOF image sensors are discussed, some paradigms revisited and different hardware approaches proposed. Moreover, an overview of different applications will be examined, but focus will be given to LiDAR applications using CMOS technology.

### 1.2.1. APPLICATIONS

Time-of-flight imaging can be found applicable in many different fields. In the next sections, some of the current applications are briefly described.

#### AUTOMOTIVE

As briefly mentioned before, and as the main focus of this thesis, automotive applications are the main driver for time-of-flight depth sensing technologies. The reasons are robustness to background illumination and depth reconstruction speed, while requiring very light image processing. Driving assistance requires the knowledge of environmental conditions where the vehicle is navigating, including other vehicles, pedestrians, road obstacles and urban signs. Most importantly, detecting transient and unexpected obstacles reliably and rapidly is the main challenge.

#### AUGMENTED AND VIRTUAL REALITY (AR/VR)

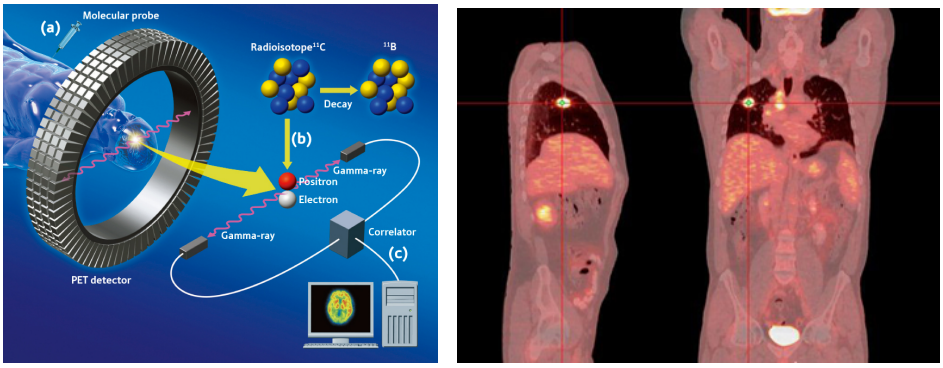
A new application in the scope of this thesis is related to AR/VR. More specifically for AR, where a layer of digital information is overlapped over the real world, it is essential to locate real objects in space, with millimeter precision. Up-to-date, software-based depth estimation is used, since it requires either regular RGB cameras or well-established technologies. However, it requires high power consumption and data processing which might not be viable for small form factor devices.

DTOF technologies take advantage of very little data processing, which speeds up the depth acquisition, and are able to operate under low light, as well as high background noise. Moreover, more processing on the sensor level can enable lower power consumption and reduce overhead processing power.

#### POSITRON EMISSION TOMOGRAPHY

Positron emission tomography (PET) is a nuclear medicine imaging technique where patients are injected with radiopharmaceutical compounds, which are labeled with a short-lived radioactive tracer isotope, that tend to concentrate in cancerous cells, in a very early

stage of abnormal activity. As these radioisotopes undergo positron emission decay, they emit protons that are shortly combined with surrounding electrons, which during the annihilation process generate pairs of gamma photons in opposite directions (180°), as sketched in Figure 1.2 (a). The pairs of gamma photons are then detected by opposite sensors, where data post-processing identifies coincident events, thus obtaining the emitter's position (*i.e.*, the cancerous cells), recreating a 3D map of the abnormal sample, as depicted in Figure 1.2 (b) [2].




(a) (b)

Figure 1.2: PET application: (a) operation principle; (b) abnormal cell image identification [3].

Historically, the detectors were constructed by crystal scintillators, coupled to photomultiplier tubes (PMTs). The crystals convert incoming gamma photons into visible photons, which are then amplified and detected. More recently, PMTs are being replaced by solid-state elements, through arrays of digital and analog silicon photomultipliers (SiPMs) [4]. To exploit the Fishburn-Seifert lower bound [5] in timing resolution, a large number of photon timestamps must be generated, typically performed through multi-channel digital SiPM (MD-SiPM) [6], requiring similar dTOF sensors for time stamping and photon counting.

### FLUORESCENCE LIFETIME IMAGING

Fluorescence imaging [7] is a technique that has been adopted in various scientific fields, specially for mapping chemical and biological interactions at molecular level, since the lifetime of a fluorophore depends on its environment but not on its concentration, thus allowing the investigation of its composite, independently of the, usually unknown, concentration of the fluorophore. Fluorescence techniques are noninvasive and generally nondestructive, and thus can be applied to live specimens. The development of fluorescence techniques has especially benefited from the introduction of multidimensional microscopy techniques, where data over three spatial dimensions and different wavelengths can be obtained, including time and the polarisation of light.

Apart from the the spatial distribution of the fluorescence intensity and spectrum, a decay function is also present. It occurs when a molecule absorbs a photon and it enters an excited state, from which it can return to the ground state by emitting a photon, This photon emission is the result of internal conversion of the absorbed energy into heat, transfer of

energy to its molecular environment, or state change (into a triplet state and return to ground state) [8]. For a homogeneous population of molecules, the resulting fluorescence decay is a single exponential function, whose time constant is the fluorescence lifetime, which is the reciprocal sum of the rate constants of all possible return paths. Multiexponential behavior can also be present, which requires more elaborate post processing to efficiently reconstruct the lifetime. The rate constants, and thus the fluorescence lifetime, depend on the type of molecule, its conformation and on the way the molecule interacts with its environment.

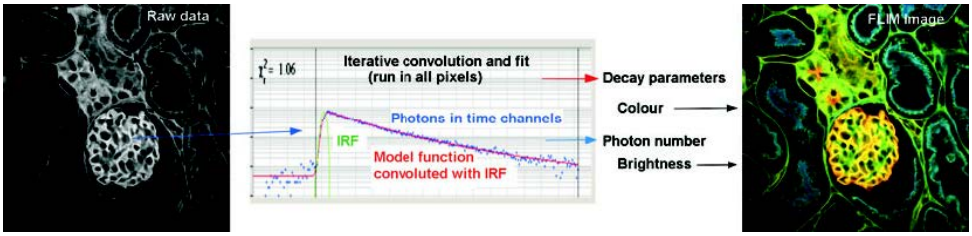



Figure 1.3: Time-resolved FLIM data analysis [7].

Recently, fluorescence lifetime imaging microscopy (FLIM) has become a practical alternative to fluorescence intensity thanks to affordable pulsed laser sources and counting electronics. This type of imaging requires time-resolved measurements and single-photon detection, which is one of the possible applications of the sensors designed in this thesis. An example of FLIM reconstruction can be seen in Figure 1.3. It is possible to compare a regular (RAW) intensity image with FLIM information. In FLIM, different lifetimes can be associated with different structures of the cell, serving as a practical and useful tool for live sample analysis.

### QUANTUM RANDOM NUMBER GENERATOR

Digital operations are a big part of our daily life. They are present in low levels of communication and system authentication, as well as high-level digital transactions, which require, due obvious reasons, a certain level of security. Typically, these operations are performed through a set of cryptographic operations, which is a mathematical function used in the encryption and decryption, throught the use of a key. The security of encrypted data is entirely dependent on two things: the strength of the cryptographic algorithm and the secrecy of the key. Cryptography can simply be described as "the art and science of keeping messages secure" [9].

Random number generators (RNGs) are a very important aspect in the generation of the key. Random number generation can be defined as the generation of a sequence of numbers, which cannot be predicted better than with a random chance [10]. By having random numbers, systems can be secured and privacy can be guaranteed. The quality of the RNG will contribute to determine the level of security of the cryptographic process.

RNGs can be distinguished in two categories; pseudo-random number generators (PRNGs) and true-random number generators (TRNGs). Pseudo-random number generators make use of mathematical implementations of functions whose statistical properties are the ones of a random distribution, while TRNGs make use of physical sources of entropy, which are

unpredictable and thus intrinsically safe. Thus, all strong cryptography requires TRNGs to generate keys, which is why it is important to have true random number generators.

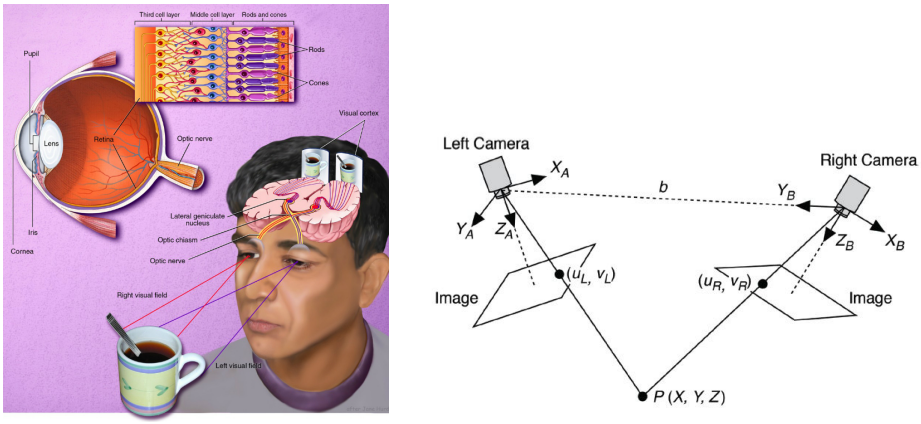
Single-photon detectors (such as SPADs) have been exploited due their quantum nature [11, 12], as a source of true random generators, and it is one of the possible applications of the circuits and devices covered in this thesis.

### 1.2.2. OPTICAL SENSING TECHNOLOGIES

Depth sensing is a very broad term that accounts for a collection of techniques that are used to estimate and/or measure the distance between sensor and objects, in order to create 1D (single-point distance) or 3D (2D array + 1D depth) maps. Next, an overview of the many technologies used for depth sensing will be described, and a justification made for the technology used throughout this thesis.

#### STEREOSCOPIC VISION

Stereoscopic vision is in general used for systems based on triangulation to estimate a point in a 3D space, giving its projection onto two (or more) images. It mimics our own human vision, based on two eyes that acquire two different images, which are then processed by the primary visual cortex, in the back of the brain, in order to provide depth perception. Figure 1.4 (a) shows a simplified sketch of the vision system in humans.




(a) (b)

Figure 1.4: Stereoscopic vision system: (a) human biological vision; (b) machine triangulation vision.

This is one of the most intuitive and commonly used depth sensing technologies, largely due to its hardware simplicity, since no special sensor or illumination is required. In fact, these systems are often passive, thus no source of light whatsoever, simply implemented via regular image sensors (CMOS or CCD), connected to image processing hardware.

A typical stereoscopic depth sensor is depicted in Figure 1.4 (b). Unlike our brain, powerful and efficient image processing algorithms can not only provide depth perception but also accurate distance estimations.

The main advantages of such systems is that, as mentioned before, it uses inexpensive,

off-the-shelf components. They are also designed to *see* colors, allowing important scene information to be processed accordingly (such as traffic lights, for example).

### STRUCTURED LIGHT

Structured light is another popular ranging technology based on image processing. It consists on generating a signal pattern onto the target (typically in the near infrared – NIR – wavelenghts ) and, by measuring the pattern deformation, the depth and shape can be estimated, whilst different patterns can be used, from stripes to dots. It has been widely used for human-machine interface (HMI), commonly adopted in the gaming industry, where the most famous example is the Kinect system, for Microsoft's XBOX game consoles [13]. Another, more recent example of such systems, is the FaceID, used in the iPhone, from Apple Inc. [14]. Figure 1.5 shows some examples of such technique.

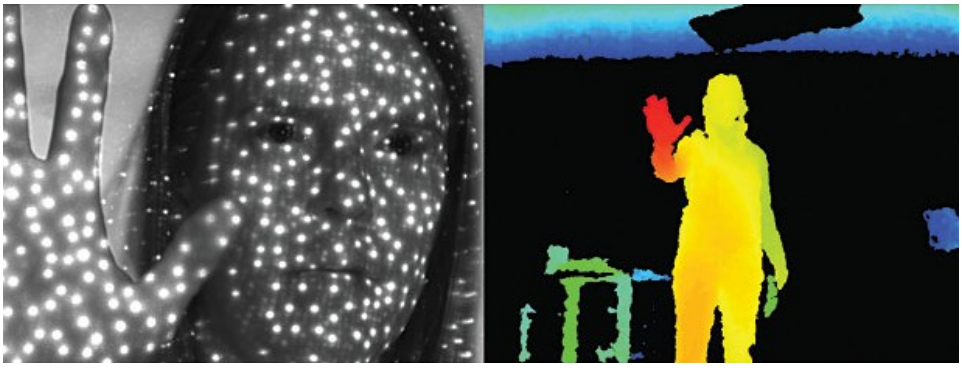



Figure 1.5: Structured light system: (a) dot projection; (b) reconstructed depth image [15].

Since such systems require their own illumination, they are very robust in dark environments, not relying on natural light to operate. However, under high background light, the signal-to-noise ratio (SNR) becomes very low, thus compromising system performance. Typically, such systems are used indoors and at short distance (up to few meters), not being able to handle outdoor operations.

### TIME-OF-FLIGHT – TOF

The sensing technologies covered before are all based on depth estimation via software, which is advantageous when image processing capability is available. However, the previous techniques are based on the intensity, which is subject to external conditions, thus being less effective in low light, due to lack of photons, and high background light, due to sensor saturation. Moreover, accuracy depends on the distance to the target, as well as the sensor physical construction, as discussed before. Moreover, software based estimation is typically slow and power hungry, a bottleneck for some applications.

Time-of-flight, however, is an active technique, based on hardware measurements, which consists on using travel time to calculate the target distance to the sensor. It relies on the propagation of waves or pulses of light, traveling through a medium (air, vacuum, water,

1

etc.) and bouncing back from the target. Depending on the specific technique to calculate the depth, different classes of TOF are used, known as indirect or direct.

Indirect time-of-flight (iTOF) is a technique where the sensor operates in an intensity mode. A known and modulated optical signal is applied onto the scene and, by integrating it in different windows, the phase of the returning signal can be calculated. The phase difference between the source and target is then used to calculate the time-of-flight, which can be translated to the absolute target distance. The signal can be modulated using a sinusoidal wave or a pulse [16–18]. The concept is shown in Figure 1.6 for a sinusoidal and pulsed operation, for sub-figures (a) and (b), respectively.

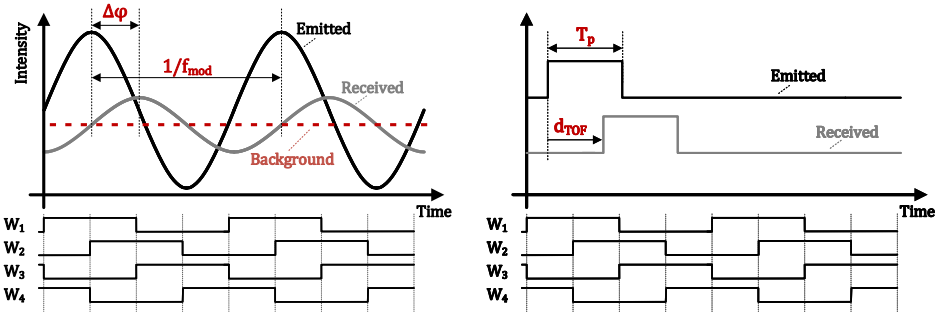



Figure 1.6: Indirect TOF system: (a) Sinusoidal modulation; (b) Pulsed modulation.

By integrating the photons over different windows, distance can be calculated by [19]:

$$\begin{aligned} d_{\text{sine}} &= \frac{c}{4\pi f_{mod}} \cdot \arctan\left(\frac{C_3 - C_1}{C_4 - C_2}\right) \\ d_{\text{pulse}} &= \frac{c}{2T_p} \cdot \arctan\left(\frac{C_3 - C_1}{C_4 - C_2}\right) \end{aligned} \tag{1.1}$$

where $c$ is the speed of light, $f_{mod}$ is the sinusoidal modulation frequency, $T_p$ is the signal pulse width, and $C_{1...4}$ are the accumulated intensity over the windows $W_{1...4}$. The arctan provides the phase difference and, by calculating the difference of integrated counts over multiple windows, the background noise can be canceled, while the target reflectivity is compensated for by the ratio of integration windows. This technique is widely used, especially for consumer applications, where indoor and short-range conditions are applied.

One of the drawbacks of such techniques is related to the modulation frequency. Since the resolution is proportional to the modulation frequency, the higher the modulation frequency, the higher the precision. However, the maximum unambiguous range is inversely proportional to modulation, setting a relation between maximum range and precision [20]. This trade-off can be somewhat compensated for by constantly changing the modulation frequency and providing a post-processing calculation [20].

Another important property of such mechanism is that iTOF operates as an intensity sensor. Thus, the signal over the background noise (SNR) must be higher than the sensitivity of the sensor. This means two things: the illumination system requires a high optical power

and/or the background noise cannot be too high. These limitations reflect on the maximum range, so far not higher than few meters [18] and/or high optical power, in the range of several hundreds of milliwatt [20].

Direct time-of-flight (dTOF) is the focus of this thesis. Differently from iTOF, it concentrates the light energy within a short time. It consists on the generation of a packet of photons, through a short pulse of laser or LED, and the direct calculation of the travel time of those photons to the target and back. Then, a technique called time-correlated-single photon counting (TCSPC) [21, 22] is used to accumulate multiple events into a histogram, in order to identify the target peak location over a typically uniform distributed background noise. The concept is presented in Figure 1.7 (a) and an example histogram is shown in Figure 1.7 (b).

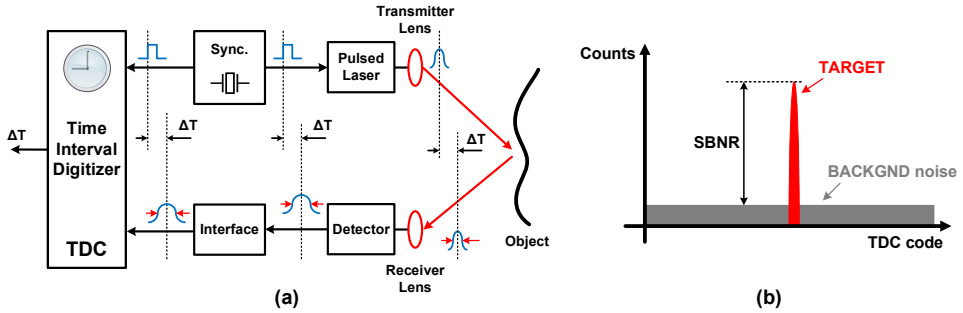



Figure 1.7: Direct TOF system: (a) architecture; (b) TCPSC histogram.

From the histogram of Figure 1.7 (b), the mean value of the returning light, of the signal peak location, can be used to calculate the absolute distance to the target, by the simple relationship of the speed of light and the histogram bin resolution, related to the least-significant bit (LSB) of the time-to-digital converted (TDC) used to measurement the travel time, such as:

$$d[k] = \frac{c}{2} \cdot TDC_{RES} \cdot h[k], \tag{1.2}$$

where $c$ is the speed of light ($\approx 3 \cdot 10^8 ms^{-2}$), $TDC_{RES}$ is the TDC resolution, in seconds, and $h[k]$ is the histogram bin in which the peak is located. More advance techniques, using data fusion and convolution neural networks (CNN), can be used to obtain the distance with better accuracy by locating the histogram peak with sub-bin accuracy.

This technique allows the system to operate under very low signal-to-noise ratio (SNR), depending on the laser pulse width and other sources of uncertainty. In other words, it means that the system is more robust to higher background illumination and/or requires less average optical power, thus reducing overall power consumption, while maintaining the precision independent on the target distance. The system is potentially much faster than software-based estimation, since it does not require elaborate image processing (only histogram), while consuming less power. Another important feature of dTOF systems is the time correlation between the incoming photons, which can allow a smarter detection, potentially filtering out noise [23, 24]. More details will be discussed throughout the thesis,

more specifically during modeling in Chapter 3, and the sensor implementation in Chapter 6.

## 1.3. TECHNOLOGY IMPROVEMENTS

CMOS technology has always benefitted from technology node advances. Driven by digital circuits, the transistor node has been reduced continuously since its initial commercial implementation in the 70's. The use of CMOS for image sensors has also allowed the reduction of the pixel size down to the theoretical limit of 0.7$\mu$m, since it is the upper limit of the detectable spectrum (red color – about the visible wavelength of 700 nm), where smaller pixels cannot provide better spatial resolution.

### 1.3.1. SMALL SPADS

Similarly to regular RGB sensors, it is desirable to reduce SPAD-based pixel sizes, so more pixels per area can be obtained, providing a higher resolution image with a small sensor size. However, SPADs require several structures for correct operation, in special guard-rings (GR), which are required to prevent premature edge breakdown. As a result, SPADs are geometrically less efficient and thus suffer from low fill factor. Up to now, the smallest fabricated SPAD has a pitch of 7.83$\mu$m, sharing the same n-well, reaching a maximum of 45% fill factor [25]. The sensor also features an opaque deep trench isolation (DTI) so as to reduce potential optical crosstalk.

Apart from the insensitive regions of the SPAD themselves, in a monolithic implementation, where the SPAD shares the pixel area with the electronics, the fill factor is severely degraded. An important move from old technologies to more advanced CMOS nodes have been pushing the reduction of the electronics area within the pixel, allowing more area to the SPAD, from about 1% in 0.8$\mu$m [26] to about 35% in 65 nm. In addition, process shrinking provides certain advantages in terms of timing resolution and power consumption, as well as a more cost-effective fabrication. In general, however, reducing feature size has negative effects on SPAD performance due to higher doping concentrations resulting in a narrower depletion region. As a result, higher tunneling-based dark count rate (DCR) and lower photon detection probability (PDP) are generally to be expected.

### 1.3.2. 3D-STACKED TECHNOLOGY

Typically, the technology process that guides the detectors design requires extensive optimization, which can include different doping profiles and extra mask generation, otherwise a poor performance is inevitable. When the readout circuit, which is designed in a regular CMOS, is placed at the same die as the detector, the detector performance is somewhat compromised. This trend becomes even more pronounced in small node technologies, due to shallow and highly doped implantation.

Moreover, SPADs require a certain insensitive structure to function properly, which reduces their active area further. Figure 1.8 shows a comparison of fill factor (detector sensitive area over pixel area) for different technologies. As we see by shrinking technology node, the fill factor increases, due to smaller electronics.

In general terms, the electronics for the readout circuit should be designed in the smallest technology node possible, so more logic can be packed per area, while the detector

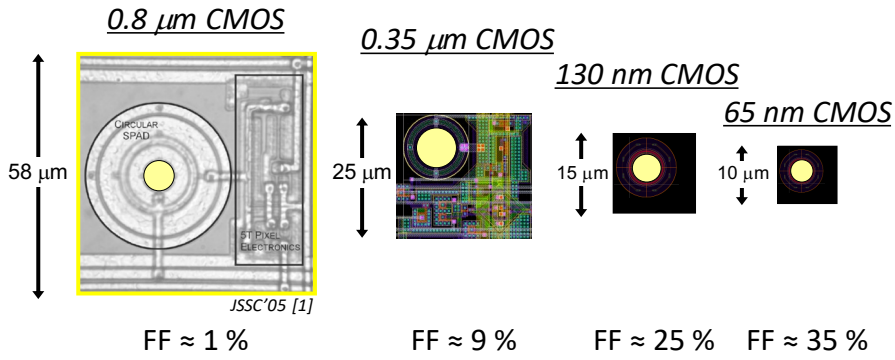



Figure 1.8: Examples of SPAD's fill factor increases according to the technology node shrinking. The yellow circles represent the SPADs' active areas [27].

maintains certain constraints and is typically designed in a modified CMOS technology, for image sensor, optimized for quantum efficiency, breakdown voltage, noise, etc.

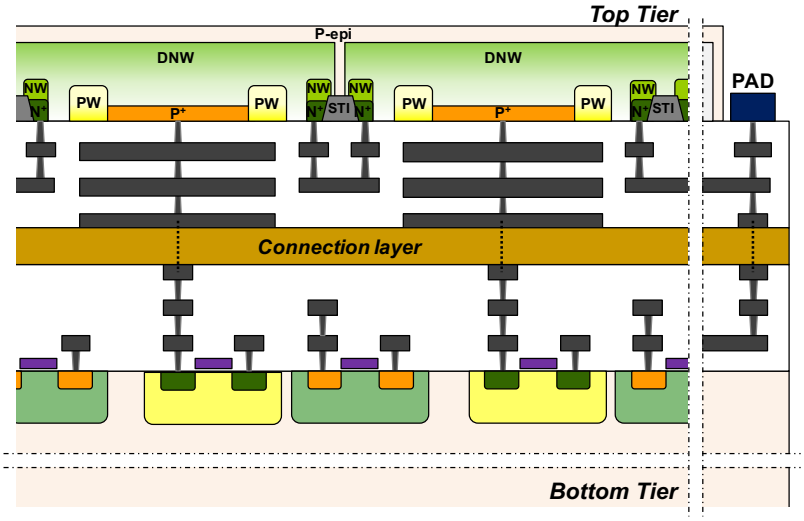



Figure 1.9: Cross section of the proposed back-illuminated 3D-integrated SPAD.

A recent solution provided by the industry is to implement image sensors in two separated silicon wafers, where the processing electronics and the SPADs are designed in dedicated technologies, and stacked. A cross-section example of such implementation can be seen in Figure 1.9 [27]. This way, a better decision on the readout technology, with respect to cost/function can be made independently from the detectors, which can be optimized separately and independently. In fact, the technologies do not even need to be CMOS, since wafer bonding works for almost every pair of technologies.

In this thesis, two similar 3D-stacked technologies were used, provided by two different foundries. In both implementations, a maximum fill factor and processing power is obtained.

### 1.3.3. TOWARDS MULTI MEGAPIXEL IMAGERS

The initial goal of this thesis was to develop a design methodology that would allow the scaling of current SPAD-based dTOF sensors towards multi megapixels arrays. Traditional RGB imaging systems have long ago broken the 1 megapixel barrier, which is appropriate for display purposes, where better (and larger) the image can be obtained. Currently, the largest CMOS sensor contains 120 megapixels [28], where the standard is >10 megapixels.

However, for computer vision, especially in the case of depth sensors, some specialists suggest that such high resolution is not necessary. Limitation on data throughput, laser power, background illumination noise, etc., are some of the reasons for such claims and not completely from the operation perspective. Undoubtedly, if a large resolution sensor can provide depth maps at very low power, high frame rates, under safe laser illumination, there is no reason to believe it would not be useful. The problem is to offer such performance.

Current LiDAR systems operate in scanning mode, based on a single/multiple [29] or on a line of detectors [24, 30], providing reasonable long range (>100 meters), wide FOV, but low spatial resolution. Those systems are bulky, they require moving parts, and complicated optical setups, often used in applications where physical volume is not an issue (thus, not a mobile system). The main reason for their use, however, is the fact that at each particular measurement point, the total laser power is concentrated while the measurement occurs for very little time (low accumulation of background noise), thus improving the system's SNR.

Moreover, since the system is not static, where the mirrors are moving continuously, the integration time per pixel can be compromised. For instance, in [30], a 202×96 system provides 10 frames/s, through a rotating six-facet polygonal mirror, corresponding to an integration time of only 44$\mu$s per pixel. With a laser frequency of 133 kHz, only 6 laser pulses are available during each pixel integration, which can be an issue during transient conditions of rain and fog. Although this is a single-axis scanner (with 6-face mirror that covers only vertical steps), it is a clear limitation in frame rate and resolution. A dual-axis scanner has even tighter constraints and it is unlikely to be commercially viable for the automotive industry.

Flash LiDAR systems (uniform illumination and static sensor array), on the other hand, can potentially provide much faster frame rate, longer effective integration time, while not requiring expensive moving parts. However, these systems suffer from very low SNR, to levels that would prevent the detection altogether. In order to improve that, few techniques can be implemented.

Perhaps the most intuitive technique uses nearby pixels spatial-temporal correlation to classify and evaluate a particular detection, named coincidence detection [23, 24]. Normally, it is impossible to discriminate between signal and noise events, however, by operating the system under dTOF, photons generated by a pulsed source (and reflected by the target) arrive onto the sensor relatively close-by, while noise is uniformly distributed. By applying an observation window for any incoming photon, statistically, signal events will contribute to useful measurements, while noise will be disregarded. A sketch of the histogram, for a single laser pulse (period $T_0$), of such systems can be seen in Figure 1.10.

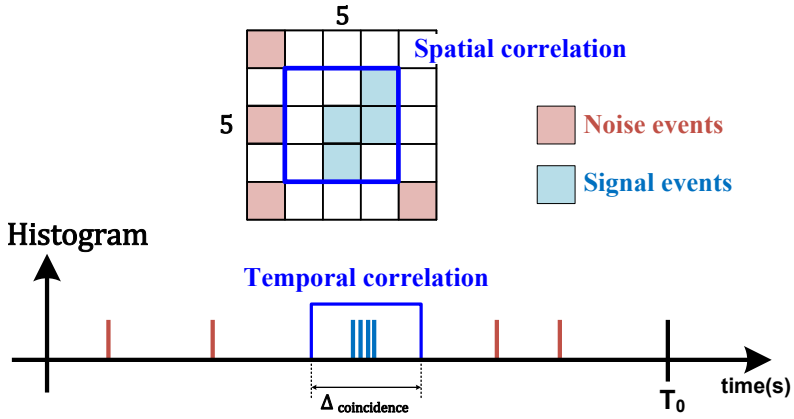



Figure 1.10: Coincidence detection arrangement, using 3×3 pixels for spatial correlation and $\Delta_{coincidence}$ for timing correlation.

A relation between the observation window (temporal correlation), number of pixels participating in each coincidence detection (spatial correlation), sensor FOV, and target shape will play a role in the probability of detecting signal photons, but also false noise coincidence events. Ideally, one can maximize the SNR, by increasing the number of pixels in the coincidence, while under short observation window. By increasing the sensor resolution, wide FOV can be used, since each pixel would cover only a small portion of the scene. It allows the combination of multiple pixels into a coincidence detection, while keeping the observation window short.

Large sensors can also increase the system statistics. In case very fine resolution is not required, multiple pixels can be combined into a single macro-pixel, via firmware, to increase frame rate. In fact, a LiDAR system can operate under non-uniform resolution, where for close-by targets, where a more precise image is required, providing more details when needed, and more returning photons are available, each sensor pixel can correspond directly to an image pixel, while for far away targets, multiple pixels can be used for a faster histogram (when only a rough distance estimation is needed). Ultimately, an optimum image frame rate can be created, with re-configurable sensor granularity.

## 1.4. COMMERCIAL ASPECTS

Depth sensing technology has been recently considered for a number of applications, from consumer applications, such as the Face ID technology, employed on the Apple's iPhone® [14], to automotive LiDAR[31], allegedly an essential tool for autonomous vehicles. Medical imaging and robotics are other examples of potential markets for the work developed in this thesis. The commercial aspects of each industry, however, is different. Some of them prioritize reliability, others cost. It is not the goal of this thesis to provide a business survey on the commercial potential of all of them, but as an engineering PhD thesis, it is important to have a tangible and clear market target, so important performance parameters can be favored.

At the beginning of the work that led to this thesis, the automotive LiDAR industry was the target. Autonomous vehicles are believed to reduce road accidents. There are over 1 billion cars in the world, 260 million in the US alone. For instance, in 2015, it has been estimated that 38,300 people were killed and over 5.4 million crashes on US roads alone (estimations say 1.2M deaths on road in the whole world), with a steady rise every year since 1921, although the number of deaths per mile has been reduced. Despite the improvement provided by technology, it has not been enough and a paradigm change is needed. Until fully autonomous cars are available (which will require even more sensors and embedded intelligence), making the current cars safer can substantially help in reducing death and injuries, where alcohol, speed and distracted driving are the three major causes of fatalities on the road.

A study by Markets and Markets [32] claims that the LiDAR market is going to hit 1,809.5 Million USD and will grow at a compound annual growth rate (CAGR) of 17.2% from 2018 to 2023. However, analysts at Technavio [33] predict that the global automotive LiDAR sensor market will see a CAGR of more than 19.2% by 2023. Massive investments from venture capitalists and a flurry of partnerships and acquisitions happening in the LiDAR domain hints on the size of this burgeoning market. The great market potential has led the investment in several companies, some of them reaching billion dollar valuation.

One of the most important companies in LiDAR is Velodyne [31], that uses a rotating LIDAR system with multiple lasers and detectors, creating an all-around depth map at the rate of 5 to 20 Hz, with unit cost in the range of $75,000 (model used in the Google car) down to $8,000 (for the most affordable model), where the frame rate might not be enough to acquire the potential fast moving targets on the road. Similarly, another important company that has been attracting attention is Quanergy [34], that uses optical phase-array, instead of rotating mirrors, to steer the laser beam over the target, with a much higher frame rate, but with range usually shorter than the requirements of the automotive industry. Another, yet radical, approach to the problem has been given by Oryx Vision [35], that treats the upcoming photons as waves, at a wavelength that has very low absorption on water (thus unaffected by fog or rain) and it is not affected by the visible spectrum of a broad day light.

These are only few examples of LiDAR companies on the scene now. There are hundreds of hardware companies competing for this market, due to its potential impact and size. However, the automotive industry is very difficult to approach, and some companies are focusing on consumer applications, such as gaming for mobile and virtual/augmented realities, as well as delivery drones and cars.

In summary, the applicability of dTOF sensors, for LiDAR systems, is extensive. It can potentially change several industries, replacing other depth sensing technologies (human-machine interface, in general) with a much higher accuracy, speed, and lower power.

## 1.5. ORGANIZATION OF THIS DISSERTATION

In Chapter 2 the detectors used throughout this thesis are examined. It is not the goal of the present thesis to do an extensive review of the device operation or design, since it is not part of the work, but to provide an overview of the device operation itself, since its behavior influences the detection probabilities of incoming photons, as well as the circuit saturation. Although the devices themselves were either provided by a foundry our designed by colleagues in the research group, everything else has been the focus of this thesis, includ-

ing multiple passive quenching circuits, described in the Chapter. Moreover, the SPADs characterization performance is also reported.

In Chapter 3, an important step towards the system optimization is developed. Differently from a passive image sensor, active configurations require the optimization of the illumination system, as well as optics, etc. Moreover, the system architecture largely influences the effectiveness of the detection, but also it is desirable to share and reuse the circuit as much as possible, allowing a more efficient use of the silicon area. Thus, a probability modeling to optimize the system is required. Also, different operation schemes are discussed, such as scanning and flash.

In Chapter 4, timing references used in dTOF systems are discussed. Since a precise timing reference is extremely necessary and difficult to deal with, with respect to signal accommodation and conversion rate, different architectures are discussed. More stringent applications are explored, with more compact and robust solutions proposed.

In Chapter 5, an innovative approach to TDC sharing is proposed, while keeping rejecting collisions between groups of pixels and maintaining skew symmetry between pixels while generating the timing information. An important feature of such structure is event source preservation, thus keeping the granularity of the sensor as a single SPAD.

In Chapter 6 two different dTOF sensors are described, discussed, and characterized. With the use of the previous modeling, devices, and building blocks preparation, two different approaches to design a modular sensor are presented.

In Chapter 7, the conclusion for the thesis will be drawn. The main contributions and findings are listed and discussed, along with recommendations for future work.

1

# REFERENCES


[1] Y. Bar-Shalom, P. K. Willett, and X. Tian, *Tracking and data fusion* (YBS publishing Storrs, CT, USA:, 2011).

[2] D. L. Bailey, M. N. Maisey, D. W. Townsend, and P. E. Valk, *Positron emission tomography* (Springer, 2005).

[3] B. Hochhegger, G. R. T. Alves, K. L. Irion, C. C. Fritscher, L. G. Fritscher, N. H. Concatto, and E. Marchiori, *Pet/ct imaging in lung cancer: indications and findings,* Jornal Brasileiro de Pneumologia **41**, 264 (2015).

[4] P. Eckert, H.-C. Schultz-Coulon, W. Shen, R. Stamen, and A. Tadday, *Characterisation studies of silicon photomultipliers,* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **620**, 217 (2010).

[5] S. Seifert, H. T. van Dam, and D. R. Schaart, *The lower bound on the timing resolution of scintillation detectors,* Physics in Medicine & Biology **57**, 1797 (2012).

[6] A. Carimatto, S. Mandai, E. Venialgo, T. Gong, G. Borghi, D. R. Schaart, and E. Charbon, *A 67,392-SPAD PVTB-compensated multi-channel digital sipm with 432 column-parallel 48ps 17b tdcs for endoscopic time-of-flight pet,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2015) pp. 1–3.

[7] W. Becker, *Fluorescence lifetime imaging–techniques and applications,* Journal of microscopy **247**, 119 (2012).

[8] J. R. Lakowicz, *Principles of frequency-domain fluorescence spectroscopy and applications to cell membranes,* in *Fluorescence Studies on Biological Membranes* (Springer, 1988) pp. 89–126.

[9] B. Schneier, *Applied cryptography: protocols, algorithms, and source code in C* (John Wiley & Sons, 2007).

[10] C. Paar and J. Pelzl, *Understanding cryptography: a textbook for students and practitioners* (Springer Science & Business Media, 2009).

[11] M. W. Fishburn, *Fundamentals of CMOS single-photon avalanche diodes* (fishburn, 2012).

[12] E. Charbon, *Single-photon imaging in complementary metal oxide semiconductor processes,* Phil. Trans. R. Soc. A **372**, 20130100 (2014).

[13] Y.-J. Chang, S.-F. Chen, and J.-D. Huang, *A kinect-based system for physical rehabilitation: A pilot study for young adults with motor disabilities,* Research in developmental disabilities **32**, 2566 (2011).

[14] *Apple Inc., Cupertino – CA, USA.* http://apple.com (2018).

[15] Z. Zhang, *Microsoft kinect sensor and its effect,* IEEE multimedia **19**, 4 (2012).

[16] R. Lange and P. Seitz, *Solid-state time-of-flight range camera,* IEEE Journal of quantum electronics **37**, 390 (2001).

[17] K. Yasutomi, T. Usui, S.-M. Han, T. Takasawa, K. Kagawa, and S. Kawahito, *An indirect time-of-flight measurement technique with impulse photocurrent response for sub-millimeter range resolved imaging,* Optics Express **22**, 18904 (2014).

[18] D. Stoppa, N. Massari, L. Pancheri, M. Malfatti, M. Perenzoni, and L. Gonzo, *A range image sensor based on 10-µm lock-in pixels in 0.18-µm cmos imaging technology,* IEEE J. Solid-State Circuits **46**, 248 (2011).

[19] M. Perenzoni and D. Stoppa, *Figures of merit for indirect time-of-flight 3d cameras: Definition and experimental evaluation,* Remote Sensing **3**, 2461 (2011).

[20] C. S. Bamji, P. O'Connor, T. Elkhatib, S. Mehta, B. Thompson, L. A. Prather, D. Snow, O. C. Akkaya, A. Daniel, A. D. Payne, *et al.*, *A 0.13 µm cmos system-on-chip for a 512× 424 time-of-flight image sensor with multi-frequency photo-demodulation up to 130 mhz and 2 gs/s adc,* IEEE J. Solid-State Circuits **50**, 303 (2015).

[21] C. Veerappan, J. Richardson, R. Walker, D.-U. Li, M. W. Fishburn, Y. Maruyama, D. Stoppa, F. Borghetti, M. Gersbach, R. K. Henderson, *et al.*, *A 160× 128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2011) pp. 312–314.

[22] M. Wahl, H.-J. Rahn, I. Gregor, R. Erdmann, and J. Enderlein, *Dead-time optimized time-correlated photon counting instrument with synchronized, independent timing channels,* Review of Scientific Instruments **78**, 033106 (2007).

[23] M. Perenzoni, D. Perenzoni, and D. Stoppa, *A 64×64-pixels digital silicon photomultiplier direct tof sensor with 100-mphotons/s/pixel background rejection and imaging/altimeter mode with 0.14% precision up to 6 km for spacecraft navigation and landing,* IEEE J. Solid-State Circuits **52**, 151 (2017).

[24] C. Niclass, M. Soga, H. Matsubara, S. Kato, and M. Kagami, *A 100-m range 10-frame/s 340×96-pixel time-of-flight depth sensor in 0.18-µm cmos,* IEEE J. Solid-State Circuits **48**, 559 (2013).

[25] T. Al Abbas, N. Dutton, O. Almer, S. Pellegrini, Y. Henrion, and R. Henderson, *Back-side illuminated spad image sensor with 7.83µm pitch in 3d-stacked cmos technology,* in *Electron Devices Meeting (IEDM), 2016 IEEE International* (IEEE, 2016) pp. 8–1.

[26] C. Niclass, A. Rochas, P.-A. Besse, and E. Charbon, *Design and characterization of a cmos 3-d image sensor based on single photon avalanche diodes,* IEEE J. Solid-State Circuits **40**, 1847 (2005).

[27] M.-J. Lee, A. R. Ximenes, P. Padmanabhan, T.-J. Wang, K.-C. Huang, Y. Yamashita, D.-N. Yaung, and E. Charbon, *High-performance back-illuminated three-dimensional stacked single-photon avalanche diode implemented in 45-nm cmos technology,* IEEE J. Sel. Topics Quantum Electron. **24**, 1 (2018).

[28] *Canon Inc., Tokyo, Japan.* http://www.canon.com/technology/future/cmos.html (2018).

[29] R. Halterman and M. Bruch, *Velodyne hdl-64e lidar for unmanned surface vehicle obstacle detection,* in *Unmanned Systems Technology XII*, Vol. 7692 (International Society for Optics and Photonics, 2010) p. 76920D.

[30] C. Niclass, M. Soga, H. Matsubara, M. Ogawa, and M. Kagami, *A 0.18-µm cmos soc for a 100-m-range 10-frame/s 200×96-pixel time-of-flight depth sensor,* IEEE Journal of solid-state circuits **49**, 315 (2014).

[31] *Velodyne LiDAR, San Jose – CA, USA.* http://velodynelidar.com (2018).

[32] MarketsandMarkets, *LiDAR Market worth 1,809.5 Million USD by 2023.* (2018).

[33] Technavio, *Global LiDAR Market 2014-2018.* (2015).

[34] *Quanergy LiDAR, Sunnyvale – CA, USA.* http://quanergy.com (2018).

[35] *Oryx Vision, Kiryat Ono , Israel.* http://oryxvision.com/ (2018).

# 2

# SINGLE-PHOTON AVALANCHE DIODE IN 3D-STACKING CMOS TECHNOLOGY

*There is one simplification at least. Electrons behave in exactly the same way as photons; they are both screwy, but in exactly the same way.*

Richard P. Feynman

*Single-photon avalanche diodes (SPADs) are an essential part of the direct time-of-flight image sensor developed in this thesis, as single-photon detectors. Their characteristics of ultra-high gain, fast timing response, and low timing jitter allow them to be exploited in many applications. Apart from the detectors themselves, the front-end circuit plays a major role in extracting the best SPAD performance, and it is essential to optimize them for the application. In this chapter, the front-end circuits used in this thesis will be described.*

## 2.1. INTRODUCTION

THE front-end of a direct time-of-flight detector consists on a reverse biased diode, operating in Geiger-mode, which is known for its high gain and short timing response, being suitable for picosecond event detection, which allows millimeter precision on depth measurements.

In this chapter, the parameters related to the detector will be examined. In Section 2.2, the parameters that characterize SPADs are described. In Section 2.3, two passive quenching circuits are provided, from two different 3D-stacking CMOS technologies. In Section 2.4, the BSI SPADs used in this thesis is be discussed and conclusions are drawn in Section 2.5.

## 2.2. SPAD OPERATION

SPADs are especially designed p-n junctions that, when reverse biased far above breakdown voltage ($V_{BD}$), creates a region of high electric field capable of single photon detection, with ultra-fast response, through a process of avalanche multiplication [1]. Differently from linear avalanche photodiodes (APD), which refers to devices that are reverse-biased slightly below $V_{BD}$, can provide moderate current gain (in the range of 200), and relatively wide bandwidth (few gigahertz), SPADs operate in a high-gain regime, called Geiger-mode [2], and its main property is very fast timing response, suitable for picosecond photon detection.

SPADs designed in standard CMOS technology have been under increasing attention from both the scientific and industrial communities, since they can benefit from high cost-effectiveness, mass-production capability, and easiness of integration with readout circuits. Consequently, photon sensing applications, especially LiDAR for advanced driver-assistance systems (ADAS), autonomous vehicles (AV), virtual and augmented realities (VR/AR), aerial drones, industrial robotics, machine vision, space navigation, etc., are becoming more popular. Another important class of applications include biomedical imaging and diagnostic techniques, such as positron emission tomography (PET), fluorescence-lifetime imaging microscopy (FLIM), etc. [3–6].

One of the main limitations of monolithic SPAD is the relatively low fill factor, due to area-intensive structures, such as guard-ring, isolation, etc., and pixel circuitry for quenching and recharge circuits [3]. This problem is exacerbated whenever advanced in-pixel functionality is required, such as timestamping, photon counting, signal processing, etc. [7, 8]. A way to optimize the active area is to implement the sensor in a smaller node technology, minimizing the processing circuitry, and thus allowing more area for the SPAD [9].

## 2.3. PASSIVE QUENCHING AND RECHARGE

SPADs operate by generating an avalanche current triggered by single or multiple photons. To avoid permanent damage to the device, this fast and intense current must be quenched as soon as possible. In its simplest form, the quenching mechanism can be performed by a single transistor, passively, operating as a high-impedance resistor. It is defined as passive quenching and, depending on the type of SPAD, the type of quenching, nMOS/pMOS transistor, also varies. At the beginning of SPAD sensor development, large devices were implemented, which presented intrinsic large junction capacitance. In order to avoid its complete discharge during an avalanche event, preventing also the generation of an exces-

sive number of carriers, active quenching was proposed [1, 10, 11]. With the reduction of the SPAD size, the junction capacitance also reduced to levels that made active quenching unnecessary and, with a simple passive quenching, a deadtime of 32 ns and full discharge in 3 ns was achieved [12, 13].

Similarly to the avalanche quenching, the second function of a SPAD front-end circuit is to recharge (reset) the SPAD bias voltage to its nominal value. This function can also be implemented as an active recharge or passive. The reasons for these two approaches are the same ones discussed about quenching, which is related to the parasitic junction capacitance (also including the connection wiring). Since passive quenching of SPADs with large capacitance can also lead to inaccurate timing resolution [14], active quenching was often required, especially for off-chip quenching. However, in fully-integrated SPAD sensors, especially in 3D-stacking technology such as presented in this thesis, passive quenching is preferred due to simplicity [12].

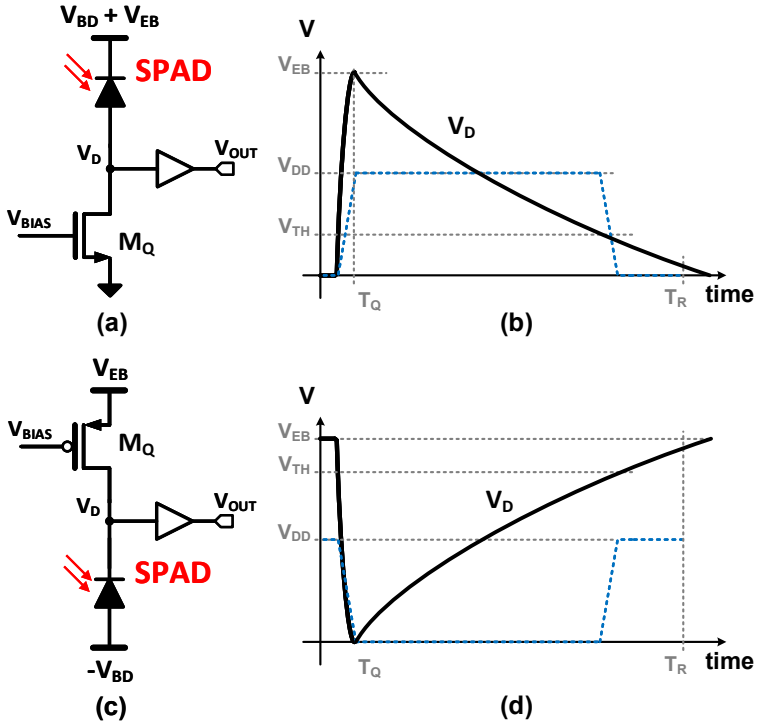



Figure 2.1: Passive quenching and recharge: (a) nMOS configuration; (b) nMOS voltage response; (c) pMOS configuration; (d) pMOS voltage response.

Typically, passive quenching and recharge circuits can be implemented through a single transistor, minimizing the required area and complexity. A typical front-end passive quenching configuration is sketched in Figure 2.1 (a) and (c), for a nMOS and pMOS configurations, respectively, along the corresponding voltage response at the front-end circuit, in Figure 2.1 (b) and (d). The quenching transistor is biased to provide several tens of

hundreds of Ohms of impedance, which is much larger than the internal SPAD resistance. Before the event, the voltage drop over $M_Q$ is zero, assuming the current flowing through the SPAD and junction leakage is zero, thus the bias voltage over the SPAD terminals is $|V_{BD} + V_{EB}|$. Upon the avalanche multiplication, current start to flow over the impedance provided by $M_Q$, creating a voltage drop over the transistor, setting the SPAD bias back to $V_{BD}$, quenching the current. Then, through the same $M_Q$, a recharge process starts, resettling the SPAD bias back to $|V_{BD} + V_{EB}|$. Both, nMOS and pMOS, operate the same way as demonstrated in Figure 2.1.

Next, the two different types of quenching circuits used in this thesis are discussed.

### 2.3.1. DUAL SPAD-TYPE QUENCHING

One of the main advantages of 3D-stacking technology is the ability to completely detach the design of SPAD detectors from the readout circuit. In order to design the best SPAD for a certain application, such as spectrum responsivity, dark-count noise, etc., the technology process play the most important role, which is often distinct from the design targets of the readout circuit. The best SPADs in CMOS are based on older technology nodes, such as 0.18$\mu$m and 0.35$\mu$m [15], although recent advances in smaller nodes are emerging [9, 16], including the ones used in this thesis. Nevertheless, the flexibility is always desirable.

The flexibility of re-utilizing the readout circuit design for different SPAD detectors can be increased by implementing a dual-type quenching circuit. Although it increases the overall area, the possibility using the same readout circuit for different SPAD technology and type (p+/n or n+/p), by simply configuring it via software, adds value to the design. This investigation has been conducted and the quenching topology implemented is shown in Figure 2.2.

The transistors in **green** are all thick-oxide devices, which allow up to 2.5 V operation. The front-end circuit is implemented in standard 40 nm CMOS technology. The circuit is a combination of Figure 2.1 (a) and (c), where the passive quenching and recharge transistors are $M_{QP}$ and $M_{QN}$, for the pMOS and nMOS, respectively. $M_{S^*}$ are configured by an external control bit ($SEL$), which defines the type of SPAD used, whereas $M_{M^*}$ provides an optical masking, in case of hot pixel. If the nMOS quenching circuit is used, $M_{SP}$ is off all the time (logic one is applied) and, depending if a particular pixel is masked ($MASK$) or not, $M_{SN}$ and $M_{MP}$ are set to logic zero or one, respectively. Similar control is provided in case of pMOS quenching, with the inverse logic. Moreover, since $V_{EB}$ can reach up to 2.5 V and the core voltage of 40 nm is 1.1 V, local level-shifters are necessary to control the pMOS transistors, as seen in the bottom of Figure 2.2.

The remaining logic, after the quenching circuit, is kept the same, including the signal sensitivity. In order to accommodate the inverse logic of different quenching circuits, the signal $SEL$ also selects a proper internal signal node, thus providing an always positive output from the quenching circuit, independently on the type of SPAD. Lastly, an electrical masking is implemented at the output by a combination of $EN$ through an AND gate.

One of the issues of the proposed dual SPAD-type quenching from Figure 2.2 is area. It requires too many thick transistors, with an area of 7×4 $\mu m^2$. An alternative to it is presented in Figure 2.3 (a).

The goal of this implementation is to utilize all the transistors for different purposes, depending on the type of SPAD used, by selecting the quenching transistor using the masking

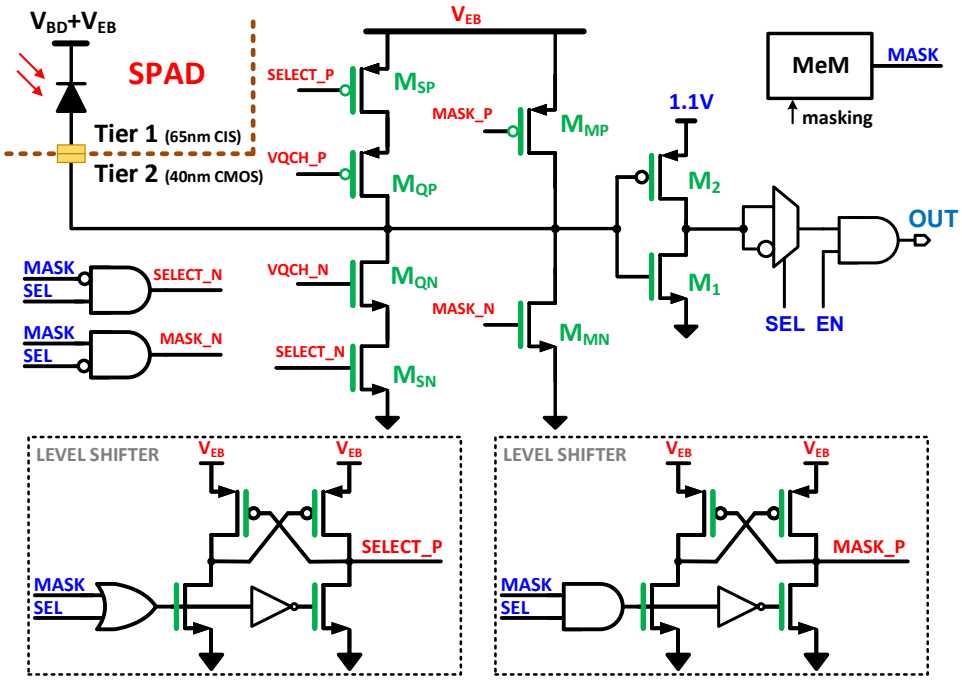



Figure 2.2: Dual passive quenching and recharge with optical masking and electrical gating [17].

bit. For instance, if $MASK$ has logic zero, the level-shifter turns $M_1$ on, and $M_2$ operates as passive quenching and recharge. Since $M_4$ is off, $M_3$ is also off and does not influence the operation; in this case, p+/n SPADs are the used, as shown in Figure 2.3 (a). The optical and electrical masking can be performed by setting $MASK$ to logic one, so $M_1$ is off, and $M_4$ is on, allowing $M_3$ to set the internal node $X$ to $V_{EB}$, effectively disabling the pixel. If a n+/p SPAD is used, the bit $MASK$ has similar effect, by an inverted logic. Moreover, since it is desirable to always have a positive output pulse, an XOR logic gate is added, which uses $MASK$ to modify the signal coming from the passive quenching.

In this topology, dual SPAD-type quenching is provided with much less thick-oxide transistors (10 against 16 of Figure 2.2). Moreover, since thick-oxide transistor typically requires wide separation to thin-oxide transistors, 4 elements are abutted back-to-back, minimizing the wasted area, as shown in Figure 2.3 (b). This topology has been implemented in 28 nm and occupies only 2.2×4 $\mu m^2$.

### 2.3.2. DUAL-MODE OUTPUT

Another simpler passive quenching element is displayed in Figure 2.4. In this topology, only one type of SPAD (p+/n) can be used, since area is very restricted. It is based on a single nMOS transistor capable of passive quenching and recharge, connected to a thick-oxide inverter, so high voltages could be converted to regular core levels (1.2 V).

The optical masking is obtained by configuring an internal 1-bit SRAM memory, which sets $M_Q$ gate-source voltage ($V_{GS}$) to either $V_Q$ or to ground. The masking memory also sets

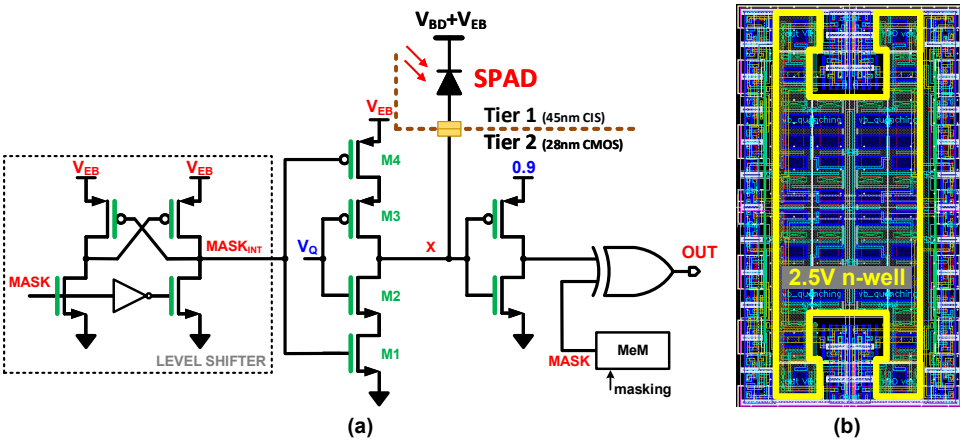



Figure 2.3: Alternative dual passive quenching and recharge with optical masking: (a) schematic; (b) layout of 4 quenching elements sharing high-voltage n-well.

the output to a constant one, through an SR-latch. Although it would make more sense to set the output to zero, in case of masked pixel, it is irrelevant, since the quenching elements are connected to an edge-sensitive element afterwards, as seen in Chapter 5, and constant values are ignored all together.

One particularity of the proposed quenching element is its electrical operation. After the effective passive quenching, buffering, and signal accommodation to core voltage, the signal is connected to a modified SR-latch, with 3-inputs each NOR. The purpose of such structure is to provide a dual-mode output, which could be a pulsed or state. When the bit *MODE* is set to logic one, the SR-latch becomes transparent, so the element output is a pulse, whose pulse width is proportional to the pixel dead time. If *MODE* is set to zero, the SR-latch is effective, where the output remains one after one event, only being reset through the assertion of the signal *RST*.

The dual-mode output is particularly important for applications where the noise is very low and the user is interested in the total number of events that occurred within a particular time frame, even if the timestamp of all of them are not available. A common application would be PET, so the energy of a scintillation event could be measured by the end of the time frame, where a reset signal would restart the pixels.

This quenching circuit is implemented in a low power, 65 nm CMOS technology, integrated with a 45 nm CIS SPAD array, through a 3D-stacking, face-to-face bonding technology, where each element occupies an area of $5.3\times3.6\ \mu m^2$.

## 2.4. 3D-STACKING, BSI SPADS CHARACTERIZATION

In this section, the characterization results of the different types and sizes of SPADs used in this thesis is presented. There are two types of SPADs, both based on 3D-stacking technologies, one provided by ST Microelectronics [18] and another by Taiwan Semiconductor Manufacturing Company (TSMC) [19].

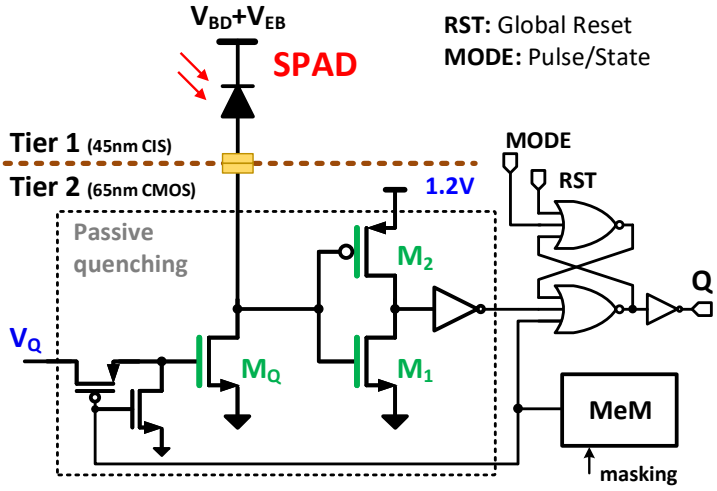
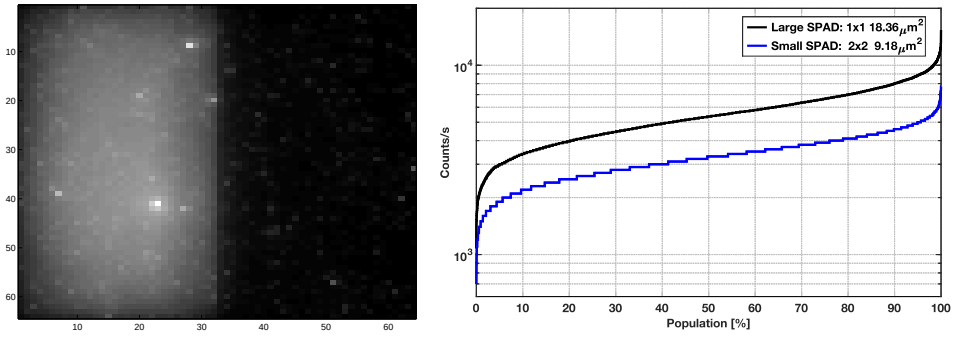



Figure 2.4: Dual-mode passive quenching and recharge with optical and electrical masking.

### 2.4.1. SPAD IN 65 NM BSI CIS

The first SPAD array is implemented in a standard 65 nm BSI image sensor process technology, provided by ST microelectronics. Connected to the quenching circuit described in Section 2.3.1, through a face-to-face hybrid bonding pads (HBP) [20], the SPAD performance is obtained. Two different SPAD configurations are used to build the pixels. In the first, a 1×1 large SPAD of 18.36$\mu m^2$ is used; the second, a 2×2 array of 9.18$\mu m^2$ small SPADs are combined on the top tier to create similar pixels. At this point, the arrangement is not relevant for the SPAD/quenching performance report, however, more details are discussed on Section 6.2.




(a) (b)

Figure 2.5: Internal noise (DCR) of ST Microelectronics SPAD device for $V_{HV}$ =12 V ($V_{EB}$ =2.4 V): (a) DCR map for large SPAD (1x1 18.36$\mu m^2$) on the left, and small SPAD (2x2 9.18$\mu m^2$), on the right; (b) DCR population.

A micrograph of the SPAD pixel is shown in Figure 2.6 (a), and both types of pixels have the similar structure. They are based on a "Fermat" [21] shaped, with 74.3% and 54% fill

factor, for the large and small SPAD, respectively. Similar results, from the same project, are reported in [16, 22]. The breakdown voltage was measured to be 12 V, and different excess bias voltages are applied. A DCR map and population are shown in Figure 2.5, for $V_{EB}$ =2.4 V, reaching a medium value of 5.3 kcps and 3.3 kcps for pixels using one large and a 2x2 small SPAD array, respectively. Although relatively high, these results are expected to improve with process refinement. Furthermore, for LiDAR, the DCR is less of a concern due to the dominant contribution of background noise. The afterpulsing probability is calculated by determining the deviation from the exponential fit, and is reported to be 0.08%, which is the lowest for 8 ns dead time, as reported in [22]. Figure 2.6 (b) shows the photon detection probability (PDP) for different $V_{EB}$, where a maximum of 22.3% at $V_{EB}$ =2.4 V is observed.

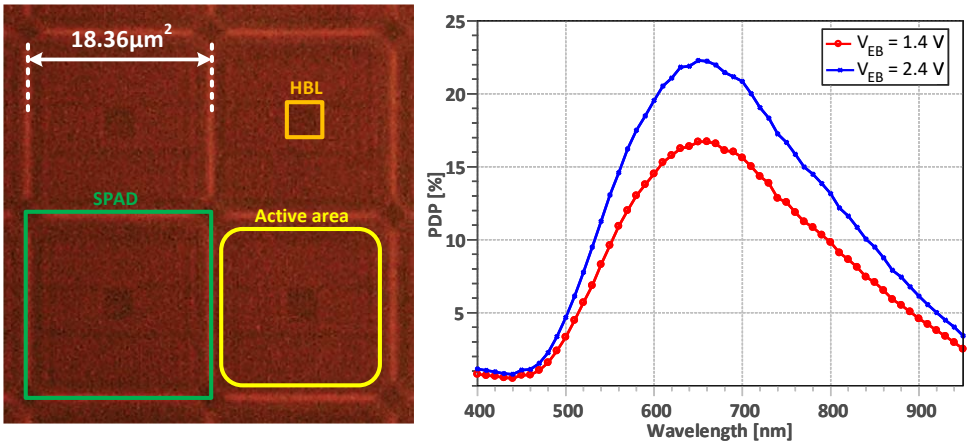



Figure 2.6: Back-side illumination SPAD; (a) micrograph of large device; (b) PDP results for different $V_{EB}$.

Timing jitter measurements were performed by illuminating the sensor with a super-continuum laser source and acousto-optic tuneable filter at a wavelength of 700 nm. The time interval between the SPAD pulses and the seed pulse of the laser was measured with a Lecroy Waverunner 204MXi-A oscilloscope. The full-width at half maximum (FWHM) of the timing responses are 122 ps and 114 ps, for $V_{EB}$ =1.4 V and 2.4 V, respectively, as reported in [22]. More details and discussions on the SPAD performance can be found at [22].

### 2.4.2. SPAD IN 45 NM BSI CIS

Another SPAD array has been designed, based on a 45 nm CIS technology provided by TSMC, whose performance is reported here. This implementation has several advantages over existing designs, especially in the newly available 3D-stacked technology, employing BSI detectors. Its fill factor is optimized thanks to a metal-free substrate, and the PDP is enhanced at shorter wavelengths, thanks to an ultra-thin substrate, minimizing carrier re-combination on the surface in backside illumination. The DCR of 55.4 cps/$\mu m^2$ and a jitter of 107 ps FWHM at 2.5 V excess bias voltage are achieved. This performance was reached

through optimized 3D-stacking with a tight control of crystal damage, improved doping profiles, and an especially designed optical stack [23–25]. This performance is achieved through careful analysis of the devices via extensive TCAD simulations, with many more details at [9]. Each pixel comprises a SPAD detector, a passive quenching and recharge circuit described in Section 2.3.2, as well as time-resolved circuitry for single-photon time stamping, which was done off-chip with a Teledyne LeCroy WavePro 760Zi-A oscilloscope.

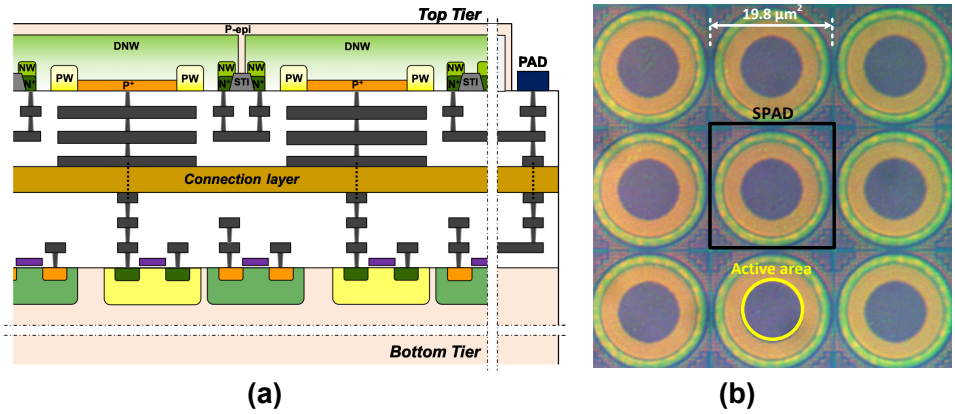



Figure 2.7: Circular SPAD design in 65 nm CIS: (a) cross section; (b) chip micrograph.

The SPAD cross section is displayed in Figure 2.7 (a). The bottom tier hosts the passive quenching (and the rest of the readout) array. Both tiers are connected with similar bonding technology as presented in Section 2.4.1, although in this case, the hybrid bonding density is much higher, in the order of 2$\mu$m pitch, in comparison of about 10$\mu$m in the previous case. The higher density of connections allow a more reliable coupling, while also allowing the sharing of metals of the top tier for the bottom tier circuits and vice-versa.

Figure 2.7 (b) shows the implemented circular shape SPAD array. In this case, none of the structure is shared among the pixels, which are separated by a shallow trench isolation (STI) region, also observed in the cross section in Figure 2.7 (a). It allows a better isolation between the pixels, avoiding cross talk from electrical nature. The optical cross talk, however, is expected to be higher than the SPAD presented in Section 2.4.1, since in that case, the array employs an opaque deep trench isolation (DTI) process between the pixels [16].

Figure 2.8 (a) presents the anode current of a single SPAD with and without an indoor (2 klux) background illumination. No color filters were used and a sharp transition due to avalanche current can be seen, indicating a Geiger-mode operation. The breakdown voltage as measured around $V_{BD}$=28.5 V with a variation over 128 SPADs of 0.11 V.

The internal noise level (dark-count rate – DCR) of a population of 128 SPADs can be seen in Figure 2.8 (b), where the median value of 6.8 kcps was obtained, under an excess bias voltage of 2.5 $V_{EB}$, above the breakdown.

At 2.5 $V_{EB}$, a peak PDP of 32% at 600 nm wavelength was obtained, whilst providing over 5% over the whole range of 420 – 940 nm, being suitable for LiDAR application as well as medical (PET), shown in Figure 2.9 (a) The timing jitter performance was obtained

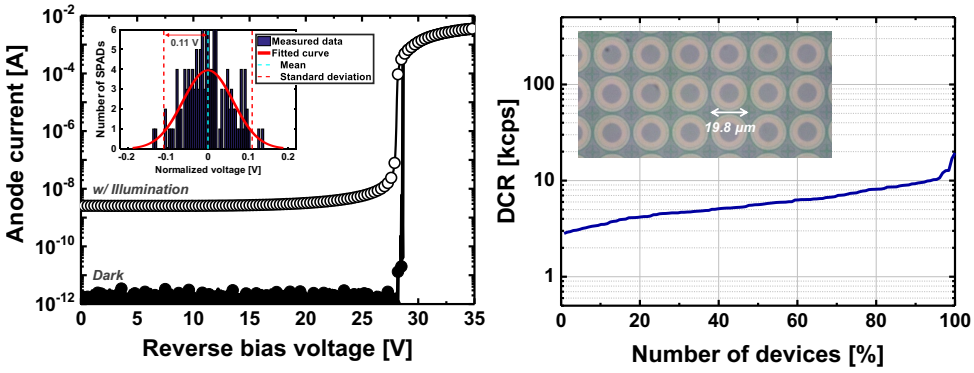



Figure 2.8: SPAD array (128 devices) performance under $V_{EB}$ = 2.5 V: (a) anode current with and without 2 klux of background illumination; (b) DCR distribution.

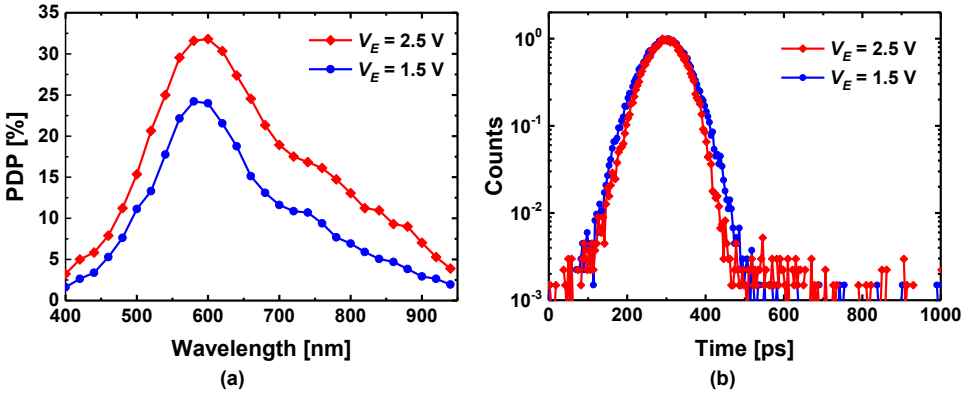



Figure 2.9: SPAD performance under 1.5 V and 2.5 V: (a) photon-detection probability (PDP); (b) timing jitter.

through a 637 nm low power, 40 ps pulse width laser, and the results are presented in Figure 2.9 (b), where a minimum of 107 ps FWHM uncertainty was obtained. This result is not the state-of-the-art if compared to other custom-designed SPADs, however, it is more than enough for LiDAR applications, where other sources of uncertainty can reach an order to magnitude higher, or more.

The SPAD performance is uniform across the array, whereas breakdown voltage and PDP variability are kept to a minimum. The results presented here are the product of a first attempt, without doping adjustments, and a better result is expected if desirable. Nevertheless, for LiDAR applications, only the PDP at longer wavelengths must be optimized.

A more detailed analysis, including the design steps for the SPADs developed in this section can be found in [9].

### 2.4.3. SPAD ISSUES AND LIMITATIONS

The main advantage of using SPADs, operating in Geiger-mode, is their intrinsic high current gain, which can provide very fast time responses, essential to dTOF operation. This operation mode, however, also implicates into some reliability issues, since the devices require high-voltage bias and potentially high power consumption, at the same time as its sensitivity is typically much lower than photo-detectors.



Moreover, some trade-offs during the design of SPADs are being investigated, by optimizing the devices for sensitivity, internal noise, timing jitter, area, fill factor, after-pulsing, and cross-talk. Some of these parameters are more important than others, depending on the application, and more attention should be given also on the circuit design, which shall be able to handle the device performance. More specifically:

- **Sensitivity:** related to the photon-detection probability and fill factor, its overall response is given by the material in which the device is fabricated. In silicon, for instance, the material is more sensitive to visible wavelengths, providing a typical response and peak around 600 nm, as shown in Figure 2.9 (a). Most of LiDAR applications, such as automotive and consumer, the desirable wavelength is around 850 nm, 905 nm, and 940 nm, in the near-infrared (NIR) spectrum, where the sun spectrum is most absorbed in the atmosphere, which appears as less ambient noise. However, some other applications, such as PET, the desirable wavelength is in the ultra-violet (UV) range, below 450 nm, requiring different design considerations. Other materials are also under investigation, such as Si-Ge [26], which has higher sensitivity at longer wavelengths due to lower bandgap potential, but suffer more from internal noise (DCR). In outdoor applications, the internal noise is typically much lower than the ambient noise, thus rendering SiGe as a good potential for future LiDAR systems. Other technologies, such as InGaAs/InP [27] are also considered, but they are expensive and not easily integrated with CMOS.

- **DCR and after-pulsing:** Internal noise is generated by defects and thermal noise internally on the devices. Lower bandgap energy, such as SiGe and InGaAs/INP devices are more sensitive in longer wavelengths, but suffer more from noise, which often require them to operate under low temperature [26, 27]. Automotive applications, however, require the system to operate outdoors, which can be a considerable limitation due to ambient noise, thus favoring wavelengths where the sun is mostly absorbed. After-pulsing is related to traps generated during an avalanche process that are stored and released after the main event, causing distortions on signal detection. One of the most straightforward ways to dealt with is by increasing the SPAD dead time, which reduces its dynamic range.

- **Timing jitter:** The timing response of SPADs will directly affect the distance precision, since it will appear as measurement uncertainties. The overall requirement, however, will also depend on other sources of uncertainty, the largest being the laser pulse width duration. In typical consumer/automotive applications, the laser pulse width duration is low-limited to 0.5 - 1 ns, since the system cost will increases exponentially as the pulse width reduces. As a rule of thumb, the SPAD jitter should be limited to one order of magnitude lower than the laser pulse width. Moreover,

the shape of the timing response and its overall integrated value will influence on the measurement precision and it is one of the main concerns on SPAD design.

- **Area and fill factor:** Ideally, the detectors should be reduced in size, in favor of a better optical design as well as cheaper cost. However, SPADs require certain structures, such as guard-ring, that limits its minimum size. Also, reducing the detectors size and spacing between one another can drastically implicate in higher cross-talk, which can impact on the depth quality, as well as it can limit the use of coincidence detection, as it will be seen in Section 3.3.1.

Overall, for automotive applications operating outdoors, the SPADs should be optimized for higher sensitivity in NIR wavelengths, with low timing jitter, and low cross-talk probability, while internal noises are less of a concern. Ideally, room temperature operation is also desirable, reducing system cost and increasing reliability, since no active cooling would be required. Also, there is a tendency to increase the number of pixels in the array, so a wider field of view (FOV) can be covered while increasing the array dynamic range, by reducing the covered area per pixel and, thus, the integrated noise.

## 2.5. CONCLUSIONS

A state-of-the-art comparison table, including the 65 nm (Section 2.4.1) and 45 nm (Section 2.4.2) BSI SPAD performance presented in this chapter is presented in Table 2.1. The 45 nm SPAD achieves superior DCR and PDP among all BSI 3D-stacked CMOS SPADs, while the 65 nm SPAD offers lower breakdown voltage, which is typically a desirable feature in consumer applications. In addition, the 45 nm SPAD also exhibits better timing jitter performance and the highest fill factor, which is very useful in many applications using the time-of-arrival technique, such as the dTOF proposed in this thesis.

Table 2.1: State-of-the-art comparison table for backside-illumination CMOS SPADs.

| | Unit | **65 nm** | **45 nm** | [28] | [29] | [16] |
|---|---|---|---|---|---|---|
| Top tier | nm | 65 | 45 | 130 | 130 | 65 |
| Bottom tier | nm | 40 | 65 | 130 | 130 | 40 |
| Active area | $\mu m^2$ | 250/182* | 122.7 | 28.3 | 28 | 27.6 |
| Fill factor | % | 74.3/54* | 60.5 | N/A | 23.3 | 45 |
| $V_{BD}$ | V | 9.6 | 28.5 | 12.3 | 16.5 | 12 |
| $V_{EB}$ | V | 2.4 | 2.5 | 4 | 1.5 | 3 |
| DCR | kcps/$\mu m^2$ | 5.3/3.3* | 6.8 | 265.3 | 35 | 10.8 |
| PDP peak | % @ nm | 22 @ 640 | 32 @ 600 | 11 @ 725 | 13 @ 600 | 27 @ 640 |
| Jitter @ $\lambda$ (FWHM) | ps @ nm | 120 @ 637 | 108 @ 637 | N/A | 505 @ 750 | 205 @ 773 |

* For 1×1 large (18.36$\mu m^2$) and 2×2 small (9.18$\mu m^2$) SPADs.

# REFERENCES


[1] S. Cova, A. Longoni, and A. Andreoni, *Towards picosecond resolution with single-photon avalanche diodes,* Review of Scientific Instruments **52**, 408 (1981).

[2] D. Renker, *Geiger-mode avalanche photodiodes, history, properties and problems,* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **567**, 48 (2006).

[3] C. Niclass, A. Rochas, P.-A. Besse, and E. Charbon, *Design and characterization of a CMOS 3-D image sensor based on single photon avalanche diodes,* IEEE J. Solid-State Circuits **40**, 1847 (2005).

[4] C. Niclass, M. Gersbach, R. Henderson, L. Grant, and E. Charbon, *A single photon avalanche diode implemented in 130-nm CMOS technology,* IEEE J. Sel. Topics Quantum Electron. **13**, 863 (2007).

[5] E. Charbon, *Single-photon imaging in complementary metal oxide semiconductor processes,* Phil. Trans. R. Soc. A **372**, 20130100 (2014).

[6] F. Villa, R. Lussana, D. Bronzi, S. Tisa, A. Tosi, F. Zappa, A. Dalla Mora, D. Contini, D. Durini, S. Weyers, *et al.*, *CMOS imager with 1024 SPADs and TDCs for single-photon timing and 3-d time-of-flight,* IEEE J. Sel. Topics Quantum Electron. **20**, 364 (2014).

[7] J. Richardson, R. Walker, L. Grant, D. Stoppa, F. Borghetti, E. Charbon, M. Gersbach, and R. K. Henderson, *A 32× 32 50ps resolution 10 bit time to digital converter array in 130nm CMOS for time correlated imaging,* in *IEEE Custom Integrated Circuits Conference (CICC)* (2009) pp. 77–80.

[8] R. J. Walker, J. A. Richardson, and R. K. Henderson, *A 128× 96 pixel event-driven phase-domain $\delta\sigma$-based fully digital 3D camera in 0.13 µm cmos imaging technology,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2011) pp. 410–412.

[9] M.-J. Lee, A. R. Ximenes, P. Padmanabhan, T.-J. Wang, K.-C. Huang, Y. Yamashita, D.-N. Yaung, and E. Charbon, *High-performance back-illuminated three-dimensional stacked single-photon avalanche diode implemented in 45-nm cmos technology,* IEEE J. Sel. Topics Quantum Electron. **24**, 1 (2018).

[10] P. Antognetti, S. Cova, and A. Longoni, *A study of the operation and performances of an avalanche diode as a single-photon detector*, Tech. Rep. (U.S. Department of Energy Office of Scientific and Technical Information, 1975).

[11] F. Zappa, A. Lotito, A. Giudice, S. Cova, and M. Ghioni, *Monolithic active-quenching and active-reset circuit for single-photon avalanche detectors,* IEEE J. Solid-State Circuits **38**, 1298 (2003).

[12] A. Rochas, G. Ribordy, B. Furrer, P. Besse, and R. Popovic, *First passively-quenched single photon counting avalanche photodiode element integrated in a conventional CMOS process with 32ns dead time,* in *Applications of Photonic Technology 5*, Vol. 4833 (International Society for Optics and Photonics, 2003) pp. 107–116.

[13] A. Rochas, *Single photon avalanche diodes in CMOS technology*, Ph.D. thesis, École polytechnique fédérale de Lausanne (2003).

[14] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, *Avalanche photodiodes and quenching circuits for single-photon detection,* Applied optics **35**, 1956 (1996).

[15] D. Bronzi, F. Villa, S. Tisa, A. Tosi, and F. Zappa, *SPAD Figures of merit for photon-counting, photon-timing, and imaging applications: A review,* IEEE Sensors Journal **16**, 3 (2016).

[16] T. Al Abbas, N. Dutton, O. Almer, S. Pellegrini, Y. Henrion, and R. Henderson, *Backside illuminated SPAD image sensor with 7.83 µm pitch in 3D-stacked CMOS technology,* in *Electron Devices Meeting (IEDM), 2016 IEEE International* (IEEE, 2016) pp. 8–1.

[17] S. Lindner, *Time-resolved Single-photon Detector Arrays for High Resolution Near-infrared Optical Tomography*, Ph.D. thesis, École polytechnique fédérale de Lausanne (2018).

[18] *ST Microelectronics, Edinburgh, Scotland.* http://www.st.com (2018).

[19] *Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan.* http://www.tsmc.com (2018).

[20] S. Lhostis, A. Farcy, E. Deloffre, F. Lorut, S. Mermoz, Y. Henrion, L. Berthier, F. Bailly, D. Scevola, F. Guyader, *et al.*, *Reliable 300 mm wafer level hybrid bonding for 3D stacked CMOS image sensors,* in *Electronic Components and Technology Conference (ECTC), 2016 IEEE 66th* (IEEE, 2016) pp. 869–876.

[21] J. A. Richardson, E. A. Webster, L. A. Grant, and R. K. Henderson, *Scaleable single-photon avalanche diode structures in nanometer CMOS technology,* IEEE Trans. Electron Devices **58**, 2028 (2011).

[22] S. Lindner, S. Pellegrini, Y. Henrion, B. Rae, M. Wolf, and E. Charbon, *A high-pde, backside-illuminated SPAD in 65/40-nm 3D IC CMOS pixel with cascoded passive quenching and active recharge,* IEEE Electron Device Lett. **38**, 1547 (2017).

[23] D. Yaung, B. Hsieh, C. Wang, J. Liu, T. Wang, W. Wang, C. Chuang, C. Chao, Y. Tu, C. Tsai, *et al.*, *High performance 300mm backside illumination technology for continuous pixel shrinkage,* in *IEEE International Electron Devices Meeting (IEDM)* (2011) pp. 8–2.

[24] C. C.-M. Liu, C.-H. Chang, H.-Y. Tu, C. Y.-P. Chao, F.-L. Hsueh, S.-Y. Chen, V. Hsu, J.-C. Liu, D.-N. Yaung, and S.-G. Wuu, *A peripheral switchable 3d stacked cmos image sensor,* in *IEEE VLSI Circuits Symp. Tech. Papers* (2014) pp. 1–2.

[25] J. Liu, D. Yaung, J. Sze, C. Wang, G. Hung, C. Wang, T. Hsu, R. Lin, T. Wang, W. Wang, *et al.*, *Advanced 1.1 um pixel cmos image sensor with 3d stacked architecture,* in *IEEE VLSI Circuits Symp. Tech. Papers* (2014) pp. 1–2.

[26] R. E. Warburton, G. Intermite, M. Myronov, P. Allred, D. R. Leadley, K. Gallacher, D. J. Paul, N. J. Pilgrim, L. J. Lever, Z. Ikonic, *et al.*, *Ge-on-si single-photon avalanche diode detectors: design, modeling, fabrication, and characterization at wavelengths 1310 and 1550 nm,* IEEE Transactions on Electron Devices **60**, 3807 (2013).

[27] S. Pellegrini, R. E. Warburton, L. J. Tan, J. S. Ng, A. B. Krysa, K. Groom, J. P. David, S. Cova, M. J. Robertson, and G. S. Buller, *Design and performance of an ingaas-inp single-photon avalanche diode detector,* IEEE journal of quantum electronics **42**, 397 (2006).

[28] E. Charbon, M. Scandini, J. M. Pavia, and M. Wolf, *A dual backside-illuminated 800-cell multi-channel digital sipm with 100 tdcs in 130nm 3d ic technology,* in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2014 IEEE* (IEEE, 2014) pp. 1–4.

[29] J. M. Pavia, M. Scandini, S. Lindner, M. Wolf, and E. Charbon, *A 1×400 backside-illuminated spad sensor with 49.7 ps resolution, 30 pj/sample tdcs fabricated in 3d cmos technology for near-infrared optical tomography,* IEEE J. Solid-State Circuits **50**, 2406 (2015).

# 3

# LiDAR OPERATION AND MODELING

*All models are wrong, but some are useful.*

George E. P. Box

*Time-of-flight imaging uses the principle of active illumination to detect the distance between sensor and targets. An optimum optical power is then required to attain certain accuracy and precision levels, whilst generating desirable image frame rates. Moreover, typical direct time-of-flight systems require the accumulation of multiple chip readouts (several timestamps) to construct a histogram, where the signal peak can be detected over a background noise. This process can take up large amounts of computer resources, slowing the processing time, image frame rate, etc. It is essential to understand the scene characteristics (signal and noise) before performing such histograms. In this chapter, the optical budget and an statistical model will be developed, serving as an optimization tool for the system design and operation.*

Parts of this chapter have been published in [1].

## 3.1. Introduction

Understanding the optical scene conditions is essential to develop any optimized imaging system. Active imaging, in particular, requires not only the receiver to be optimized, such as the sensor, optics, chip communication, etc., but also the transmitter, such as the light source. Its study is not only required in order to improve the system accuracy and precision, but it must also be evaluated with respect to eye-safety. Meeting both limits, maximum possible optical power and minimum required for the system, will define the imaging architecture and operation.



In the first section of this chapter, the generated avalanche events will be calculated, based on the source optical power, angular field-of-view (AFOV), distance to the targets, number of pixels, lens aperture, etc. Then, the influence of background noise will be included, allowing the evaluation of the optical power limits. Several other operation schemes will be introduced and modeled, as a way to improve the detection, reject noise and, ultimately, reduce the required optical power.

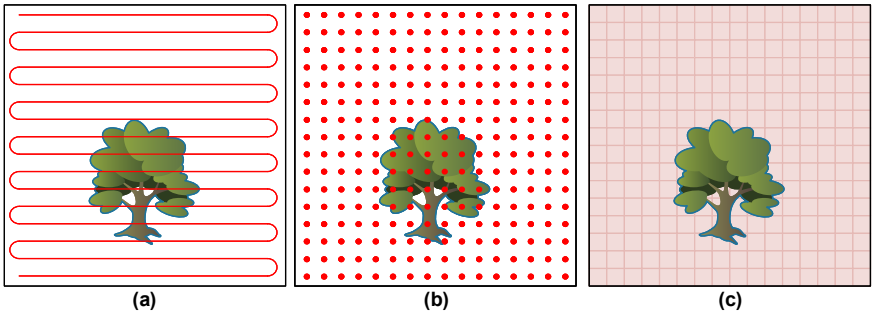



Figure 3.1: Different operation conditions: (a) dual-axis scanning (Condition 1); (b) flash with laser generated by a diffraction lens (Condition 2); (c) flash with laser generated by uniform diffuser.

For the following simulations and plots, two of the most common LiDAR approaches will be considered: scanning (Condition 1) and flash (Condition 2). In scanning, such as in Figure 3.1 (a), a narrow AFOV and a laser beam is used, whereas the chip readout and image frame rate must be high, in order to provide the same number of points as the latter condition. In the flash condition, such as Figure 3.1 (b) and (c), the AFOV is wider, with the laser energy being spread over it, allowing a slower chip readout and image frame rate, although for a much larger array. In essence, the two flash operations of Figure 3.1 (b) and (c) are similar, assuming the laser that illuminates the scene is the same. The main difference, though, is on the returning light, since the case where the laser energy is distributed in points (Figure 3.1 (b)), the target shape and uncertainty do not produce any variation on the timing response, whereas in the case of Figure 3.1 (c), the target shape, within each pixel, produce a spread, in time, of the laser energy, reducing its peak when recovered in a histogram. For this chapter, the case of Figure 3.1 (b) is considered.

Thus, both conditions (scanning and flash) are examined and compared, with discussion and conclusions drawn in the end of the chapter. For the laser optical power, based on eye-safety and AFOV, the conclusions obtained in the Appendix A are used, identically for both conditions.

- **Condition 1 (Scanning):**
  - **Laser:** $P_{laser}$ (avg) = 16 mW; $F_{laser}$ = 100 kHz; $\lambda$ = 840 nm; $FWHM$: 1 ns;
  - **System**: AFOV = 4.13°; $T_{int}$ = 1 $\mu$s ($RANGE$: 150 meters); $\rho_{target}$ = 0.1;
  - **Lens:** D = 11.42 mm; focal length = 16 mm; f/# = 1.4; $\eta_{lens}$ = 0.7;
  - **Sensor:** $M$ = 16×16 pixels; $A_{pixel}$ = 324 $\mu$m$^2$; $PDP$ = 0.15 @ 840 nm; $FF$ = 0.5;
  - **frame rate:** Chip readout = 256 kfps; Image = 10 fps (256×256);
  - **Noise:** background noise = 98 klux; DCR = 5 kcps;
- **Condition 2 (Flash):**
  - **Laser:** $P_{laser}$ (avg) = 16 mW; $F_{laser}$ = 100 kHz; $\lambda$ = 840 nm; $FWHM$: 1 ns;
  - **System**: AFOV = 60°; $T_{int}$ = 1 $\mu$s ($RANGE$: 150 meters); $\rho_{target}$ = 0.1;
  - **Lens:** D = 11.42 mm; focal length = 16 mm; f/# = 1.4; $\eta_{lens}$ = 0.7;
  - **Sensor:** $M$ = 256×256 pixels; $A_{pixel}$ = 324 $\mu$m$^2$; $PDP$ = 0.15 @ 840 nm; $FF$ = 0.5;
  - **frame rate:** Chip readout = 1 kfps; Image = 10 fps (256×256);
  - **Noise:** background noise = 98 klux; DCR = 5 kcps;

In both conditions, the final image resolutions is the same (256×256), at the same image frame rate. Setting similar final results allows a better evaluation and comparison of both approaches.

A typical TCSPC system operates by accumulating the total number of events, over multiple laser pulses, into a histogram, where a consistent signal return produces a distinct peak, which mean value can then be used to calculate the absolute distance to the target, by the simple relationship of the speed of light and the histogram bin resolution, related to the least-significant bit (LSB) of the time-to-digital converted (TDC) used to measurement the travel time, such as:

$$d[k] = \frac{c}{2} \cdot TDC_{RES} \cdot h[k], \tag{3.1}$$

where $c$ is the speed of light ($\approx 3 \cdot 10^8 ms^{-2}$), $TDC_{RES}$ is the TDC resolution, in seconds, and $h[k]$ is the histogram bin in which the peak is located. More advance techniques, using data fusion and convolution neural networks (CNN), can be used to obtain the distance with better accuracy by locating the histogram peak with sub-bin accuracy.

Multi-path photon reflections and imaging through semi-transparent targets (such as glass) can generate histograms with multiples peaks, in different locations. In a intensity-based sensor, such as iTOF, these secondary reflections are difficult to distinguish and, inevitably, produce measurement errors. In dTOF, on the other hand, these peaks can be treated with much more precision and disregarded when convenient, allowing a much more reliable target detection.

## 3.2. Optical power budget

Power optimization is essential in any electronic system, even when ideal power supplies are available. The reason is that, since power efficiency is rarely close to 100%, excessive power consumption inevitably leads to losses that are converted, normally, in thermal energy, thus requiring thermal dissipators (passive and, in some cases, active), raising not only the costs, but also the overall physical volume, which is one of the biggest limitations in mobile applications.



Illumination systems, such as LED and lasers, are no different. Solid-state LED/laser diodes efficiency ranges around 15-60% [2], whilst their spectrum stability, output power, and overall efficiency can vary largely with the temperature [3]. Thus, an optimally designed illumination is an essential component on the development of an efficiency LiDAR imaging system.

The required light source power will depend on the conditions in which the sensor will operate. For a well-controlled, cooled, and dark ambient, the noise is not necessarily a problem. This scenario is typically found in medical and space applications. For an automotive application, however, the most limiting factors are the potentially high background noise, coming mostly from the sun, but also from other artificial sources, and a limitation on the optical power, since it can easily surpass the limits of eye-safety.

As expected, the amount of photon events is proportional to the total energy that reaches the sensor, for signal and noise alike. Next, the energy of both, signal and noise, will be calculated and the amount of avalanche events extracted. At this point, the average activity (based on average energy) suffices, but later, more details on the nature of those events will be discussed.

### 3.2.1. Signal events

The total number of signal events can be calculated based on the energy per pixel that is reflected by the target and is focused by the lens onto the sensor. It is assumed that the totality of the laser power matches exactly the desired AFOV of the sensor, so no laser energy is wasted in out-of-view regions.

For the returning light, the target is assumed to be a diffusely reflecting surface, where its apparent brightness to an observer is the same regardless of the observer's angle of view, i.e., the surface luminace is isotropic. This type of target is called Lambertian reflector. In Figure 3.2, the setup of the active imaging system is displayed, where the distance to the target is $R$, the lens aperture is $D$, focal length $f_0$, and the sensor height is $h$.

The reflected optical power from the target, $P_{target}$, is given by the source power, $P_{source}(R)$, and the reflectivity of object, $\rho_{target}$. This energy is then collected at the lens, which corresponds to the area ratio at aperture D and the sphere surface with diameter R, thus:

$$\begin{aligned} P_{lens} &= P_{target} \cdot \frac{A_{lens}}{A_{sphere}}, \\ P_{lens} &= P_{source}(R) \cdot \rho_{target} \cdot \left(\frac{D}{2 \cdot R}\right)^2. \end{aligned} \tag{3.2}$$

The power source, $P_{source}(R)$, is a function of the distance. For a clear day and relatively short distance, $P_{source}(R)$ can be approximated to a constant, equals to the source, meaning

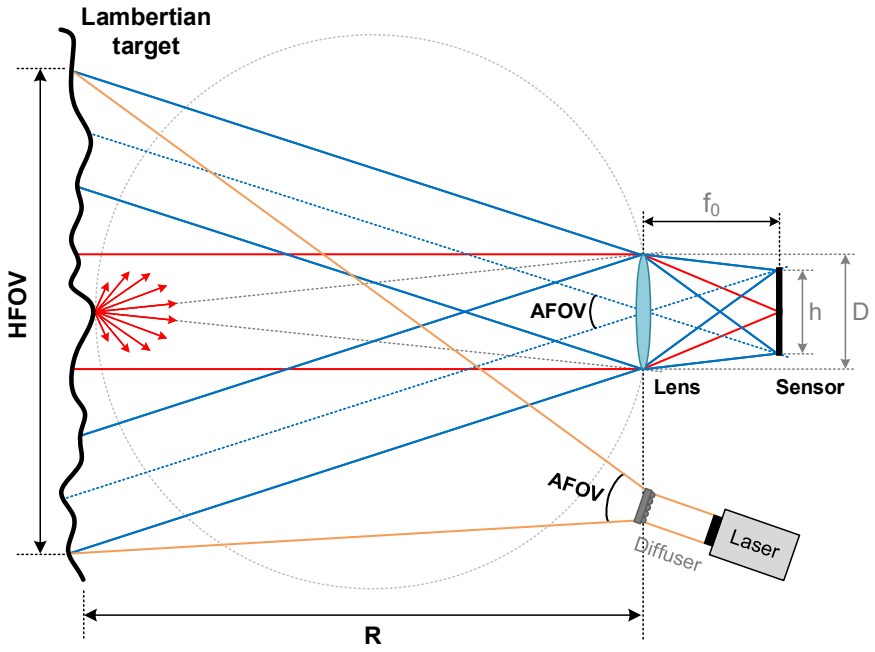



Figure 3.2: Typical active imaging system, using a Lambetian reflectance as target.

that all the power leaving the illumination system reaches the target and it is reflected back, without interaction with the air. In the presence of a scattering medium, such as fog, rain, and smoke in the air, a dependency on the distance $R$ is necessary. This will be re-visited in Section 3.3.3.

The optical power is collected by the lens, concentrated, and projected at the sensor sensitive area. Since the lens is designed to cover the whole sensor, as depicted in Figure 3.3, the usable fraction of the projection is given by the ratio between $A_{sensor}$ and $A_{lens\_proj}$ $(2/\pi)$. Often, the lens projection covers a larger area than the sensor itself, thus this ratio must be adjusted; it can be added to the lens/filter efficiency (also used to account for losses), $\eta_{lens}$, leading to:

$$P_{pixel} = P_{lens} \cdot \eta_{lens} \cdot \frac{2}{M \cdot \pi}, \tag{3.3}$$

where $M$ is the total number of pixels in the sensor. By combining (3.2) and (3.3), we obtain:

$$P_{pixel} = P_{source} \cdot \rho_{target} \cdot \left(\frac{D}{2 \cdot R}\right)^2 \cdot \eta_{lens} \cdot \frac{2}{M \cdot \pi}. \tag{3.4}$$

From (3.4), the power per pixel can be directly calculated based only at the source power and physical dimensions of the system. Sometimes, however, it is more convenient to represent (3.4) using the desirable AFOV, f/# of the lens, and pixel area ($A_{pixel}$). Thus,

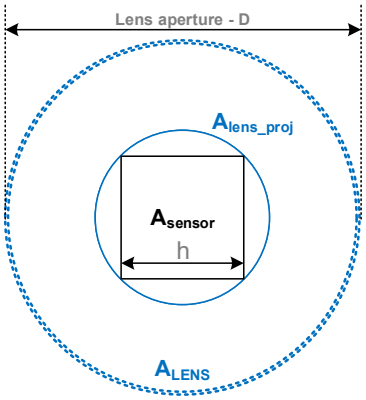



Figure 3.3: Lens projection and sensor coverage.

by using the following relation:

$$\begin{aligned} D &= \frac{f_0}{f/\#}, \\ f_0 &= \frac{h \cdot R}{HFOV}, \\ HFOV &= 2 \cdot R \cdot \tan(AFOV/2), \end{aligned} \tag{3.5}$$

where $HFOV$ is the horizontal field-of-view, (3.4) can be rearranged such as:

$$P_{pixel} = P_{source} \cdot \rho_{target} \cdot \left(\frac{1}{2 \cdot f/\#}\right)^2 \cdot \eta_{lens} \cdot \frac{2 \cdot A_{pixel}}{\pi} \cdot \left(\frac{1}{2 \cdot R \cdot \tan(AFOV/2)}\right)^2. \tag{3.6}$$

Both (3.4) and (3.6) can be expressed in terms of average power, integrated over a certain time window, or, in the case of pulsed light, normalized to the laser frequency ($F_{laser}$), allowing it to be expressed in terms of energy per pulse, such as:

$$E_{pixel\_pulse} = P_{pixel} \cdot \frac{1}{F_{laser}} \tag{3.7}$$

Thus, the number of photons $N_{p\_pulse}$, per pulse, per pixel, can be calculated as:

$$\begin{aligned} N_{p\_pulse} &= \frac{E_{pixel\_pulse}}{E_{photon}} \\ N_{p\_pulse} &= P_{pixel} \cdot \frac{\lambda}{F_{laser} \cdot h \cdot \nu}, \end{aligned} \tag{3.8}$$

where $\lambda$ is the light source wavelength used, $h$ is the Planck's constant ($6.62607004 \times 10^{-34}$ m$^2$ kg/s), and $\nu$ is the speed of light ($\sim 2.998 \times 10^8$ m/s). This value defines the total number of photons per laser pulse that reaches each pixel, but not all will generate an avalanche event.

As discussed in the introductory chapter, SPADs convert photons into electric current. The $PDP$ defines the probability of generating an avalanche if a photon reaches the SPAD active region. However, it is more accurate, during the power density calculation, to use the photon detection efficiency ($PDE$), which is the product of the $PDP$ and the pixel fill-factor ($FF$), thus accounting for the photons reaching insensitive regions as well. Thus, the effective number of signal events, per laser pulse, per pixel will be:

$$\begin{aligned} N_{signal\_events/pulse} &= N_{p\_pulse} \cdot PDE \\ N_{signal\_events/pulse} &= P_{pixel} \cdot \frac{\lambda}{F_{laser} \cdot \hbar \cdot \nu} \cdot (PDP \cdot FF), \end{aligned} \tag{3.9}$$

Finally, the combination of (3.9) with (3.4), or (3.6), determines the effective number of generated signal events, which will then be used during the statistical model in Section 3.3.

### 3.2.2. NOISE EVENTS

Similarly to the signal event calculation, several optical aspects of the system influence the number of detected events from background noise, namely, the AFOV, aperture, and number of pixels. Differently from the signal calculation, though, the noise will depend on an specific integration time ($T_{int}$), which can be as long as the laser period ($1/F_{laser}$), but shorter as well if gating is used. The reason being that the laser frequency might not be as flexible as the desirable coverage distance (related to $T_{int}$), but also a way to keep the average laser power constant, whilst increasing the pulse peak level, which increases the probability of signal detection, as will be discussed in Section 3.3.

Background noise can be originated from different sources, including artificial light (other illumination systems), which are difficult to evaluate, since they depend entirely on the wavelength, incident angle, etc., and must be analyzed case-by-case. Natural light coming from the sun, however, is the major contributor to noise. It can be evaluated based on normal irradiance at Earth's surface. The energy coming from the sun interacts with several media (different atmospheric compositions) and can have different paths. Figure 3.4a illustrates the interaction of the sun rays with Earth's surface composition.

At sea-level, the direct irradiance, normal to the surface with the sun at zenith, is shown in Figure 3.4b, including the absorption valleys in different states of $O_2$, $O_3$, $H_2O$, and $CO_2$ molecules, commonly found in the atmosphere. The most widely used standard spectra are those published by The Committee Internationale d'Eclaraige (CIE), the world authority on radiometeric and photometric nomenclature and standards. The American Society for Testing and Materials (ASTM) publishes the sun spectra [4], depending on the angular incidence light, in units of air mass (AM), shown in Figure 3.4c. Figure 3.4d shows the irradiance with AM 1.5, which best represents the average conditions of the USA and Europe.

Evidently, direct sun irradiance is very high and would overload most of image sensors. However, very rarely the total energy is directly irradiated onto the sensor and/or the target. Multiple reflections, between the floor and multiple objects, scattering, etc., promotes a reduction of the overall noise level reaching the sensor lens. A possible scenario situation can be seen in Figure 3.5.

The amount of sun irradiance reaching the lens of the sensor can be very complicated to estimate (if not impossible). Multiple reflections in several objects, even outside the AFOV

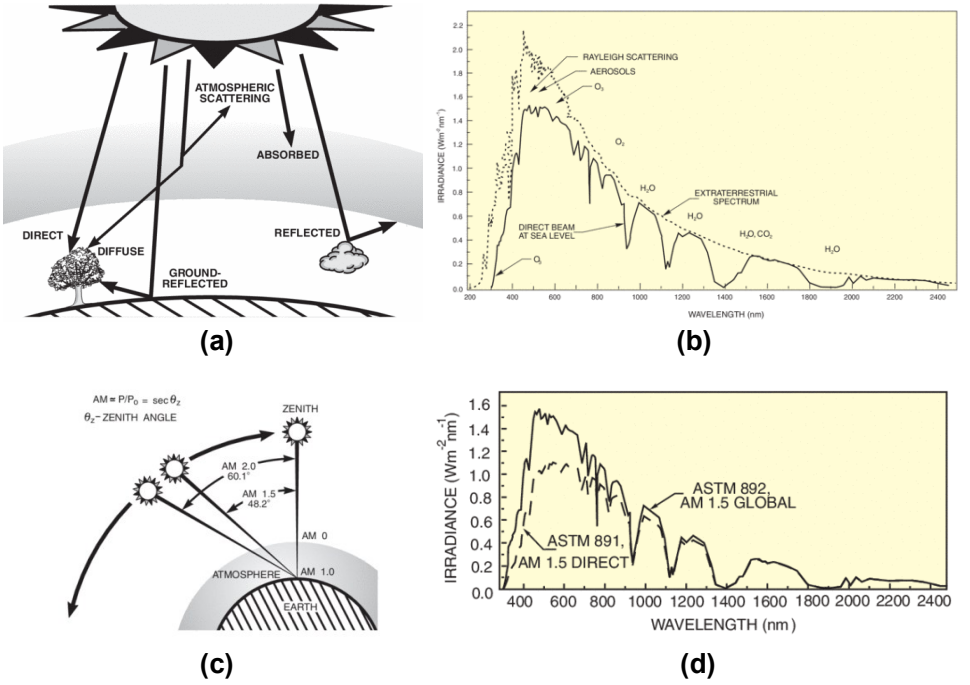



Figure 3.4: Background noise: (a) Total global radiation on the ground with direct, scattered and reflective components; (b) Normal incident solar spectrum at sea level, on a clear day; (c) Path length, in units of Air Mass (AM), changes with the zenith angle. (d) Standard spectra for AM 1.5, for ASTM E891 and global ASTM E892 [4].

of the sensor, can influence the overall noise level. For this reason, we will assume that no direct sunlight will reach the sensor lens but only reflected light from the target, which will be also illuminated by indirect rays (reflected on the floor, trees, etc.), adding another efficiency term, $\epsilon$. Thus, the reflected power from the target, due to noise, per pixel, is similar to (3.4) and/or (3.6), becoming:

$$P_{pixel\_noise} = (P_{sun}(R)\cdot\epsilon)\cdot\rho_{target}\cdot\left(\frac{D}{2\cdot R}\right)^2\cdot\eta_{lens}\cdot\frac{2}{M\cdot\pi}$$
$$P_{pixel\_noise} = (P_{sun}(R)\cdot\epsilon)\cdot\rho_{target}\cdot\left(\frac{1}{2\cdot f/\#}\right)^2\cdot\eta_{lens}\cdot\frac{2\cdot A_{pixel}}{\pi}\cdot\left(\frac{1}{2\cdot R\cdot\tan(AFOV/2)}\right)^2, \tag{3.10}$$

where $P_{source}(R)$ is replaced by $P_{sun}(R,\theta)\cdot\epsilon$, and $\theta$ is the incidence sun light angle with the medium. The energy coming from the sun will suffer from several interactions with the medium, and these dependencies will be examined in Section 3.3.3. At this point, a clear sky will be considered, approximating $P_{sun}(R,\theta)$ to $P^0_{sun}$, which can be extracted from Figure 3.4d, by integrating the irradiance $E_\lambda$ over a certain spectrum bandwidth ($\Delta_\lambda$ – depending on a band-pass filter in front of the sensor) and the AFOV, such as:

$$P^0_{sun} = (2\cdot R\cdot\tan(AFOV/2))^2\cdot\int_{\lambda-\Delta_\lambda/2}^{\lambda+\Delta_\lambda/2} E_\lambda\, d\lambda \tag{3.11}$$

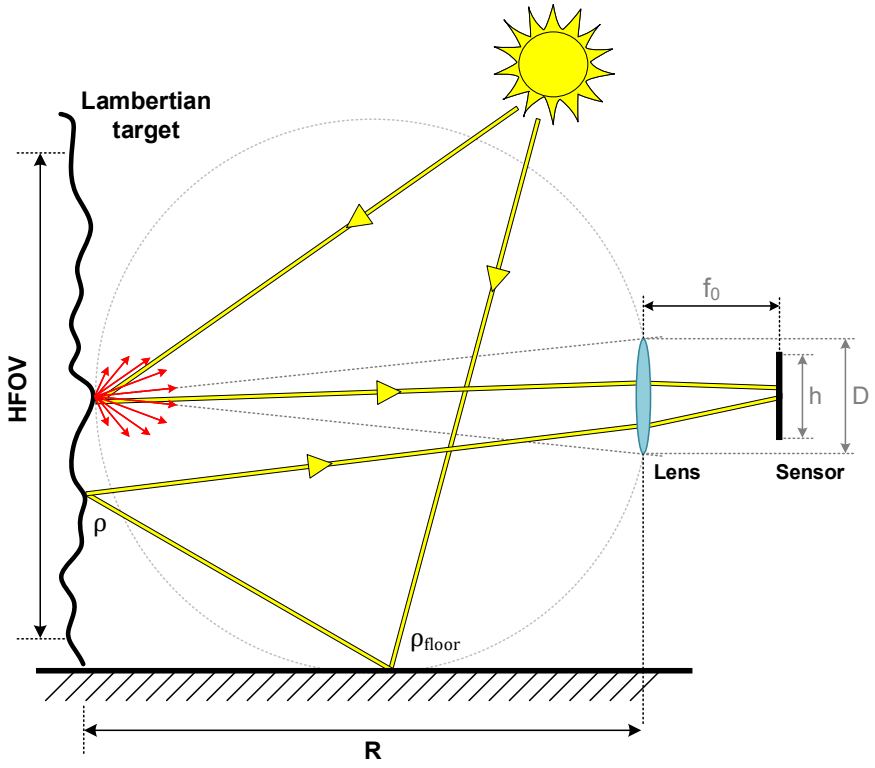



Figure 3.5: Multiple noise reflections.

The effective number of noise events, per second, can be normalized to the laser frequency, similarly to (3.9), as:

$$N_{noise\_events/pulse} = P_{pixel\_noise} \cdot \frac{\lambda}{F_{laser} \cdot h \cdot \nu} \cdot (PDP \cdot FF). \tag{3.12}$$

Commonly, the solar irradiance is given by the luminous flux per area, in lux. By integrating $E_\lambda$ over the whole spectrum, a total power of 1050 W/m$^2$ can be obtained, which can be readily converted into lux by the luminous efficacy of white light, of 93 lm/W, to a total of 98 klux. Per se, the luminous flux per area does not provide enough information to be able to calculate the effective noise for a imaging system, which depends largely on the wavelength, but it gives a common sense on the level of sunlight the sensor is inserted on.

Differently from the signal, the overall accumulated noise depends on the integration period ($T_{int}$). For instance, the unambiguous distance a dTOF system can provide is the inverse of the laser frequency ($T_0 = 1/F_{laser}$). If the integration window is exactly that, the system is always integrating photons, from signal and noise. However, it is often desirable to slow $F_{laser}$ so the energy per pulse can be higher, while keeping the average optical power constant, thus shortening $T_{int}$ with respect to $T_0$. So, this ratio should be added to

(3.12).

Moreover, internal SPAD noise will also contribute to generate undesirable avalanche events on the sensor. Although, background noise can be several orders of magnitude higher than the detector noise (typically reported as dark-count rate – DCR –, which ranges between $10^{-2}$ and $10^{3}$ cps/$\mu$m$^2$), it is important to add this extra component to (3.12), for completion and for photon-starved conditions, thus becoming:

$$N_{noise\_events/pulse} = T_{int} \cdot \left( P_{pixel\_noise} \cdot \frac{\lambda}{h \cdot \nu} \cdot (PDP \cdot FF) + DCR \right) \tag{3.13}$$



## 3.3. Statistical model

SPAD devices have a unique property that enables single-photon detection, with fast response and low timing uncertainty, which allows fast depth measurement and high accuracy. However, after each detection, they require a recharging time that renders them insensitive, in a process called dead time.

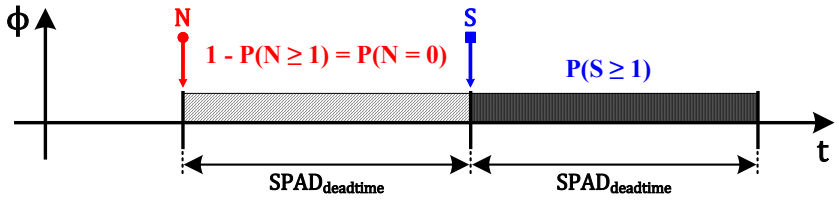



Figure 3.6: Probability of signal detection.

A signal event detection requires that the detector is active upon the arrival of a signal photon, graphically represented in Figure 3.6. In other words, the probability of detecting a signal ($p_{s\_mod}$) is given by the product of the probability of at least one signal event [$p_s = P(S \geq 1) = 1 - P(S \leq 0)$], and the probability of not having a noise event, prior the signal event itself, [$q_n = 1 - P(N \geq 1) = P(N = 0)$], such as:

$$p_{s\_mod} = p_s \cdot q_n = [1 - P(S \leq 0)] \cdot P(N = 0) \tag{3.14}$$

Due to random activity, the noise process has a Poisson distribution, thus $q_n$ can be calculated by $P(N = 0) = e^{-\lambda n\_dead}$, where $\lambda_{n\_dead}$ is the average noise activity within the $SPAD_{deadtime}$, obtained by de-normalizing (3.13) with $F_{laser}$, such as:

$$\lambda_{n\_dead} = N_{noise\_events/pulse} \cdot F_{laser} \cdot SPAD_{deadtime}. \tag{3.15}$$

The signal, on the other hand, can be calculated by the complementary cumulative distribution function or, by simply assuming $P(S \leq 0) = P(S = 0)$, since no negative outcome is possible, thus $p_s = 1 - P(S = 0) = 1 - e^{-\lambda_s}$, where $\lambda_s$ is the average activity per laser pulse, given by (3.9). Thus:

$$p_{s\_mod} = [1 - e^{-\lambda_s}] \cdot e^{-\lambda n\_dead}. \tag{3.16}$$

Strictly speaking, the probability of detecting a noise event should also follow the principle of pixel availability, i.e., the pixel is not busy (dead time) upon a noise event. Thus, the probability of detecting a noise event is then:

$$p_{n\_mod} = [1 - e^{-\lambda_n}] \cdot e^{-\lambda n\_dead}, \tag{3.17}$$

where $\lambda_n$ is the average noise activity, per laser pulse, given by (3.13).

Considering Conditions 1 and 2, at the beginning of this chapter, the probability of signal and noise detection can be calculated, plotted, and compared. Also, the total number of available photons that could potentially generate timestamps, per laser pulse, is plotted in Figure 3.7.



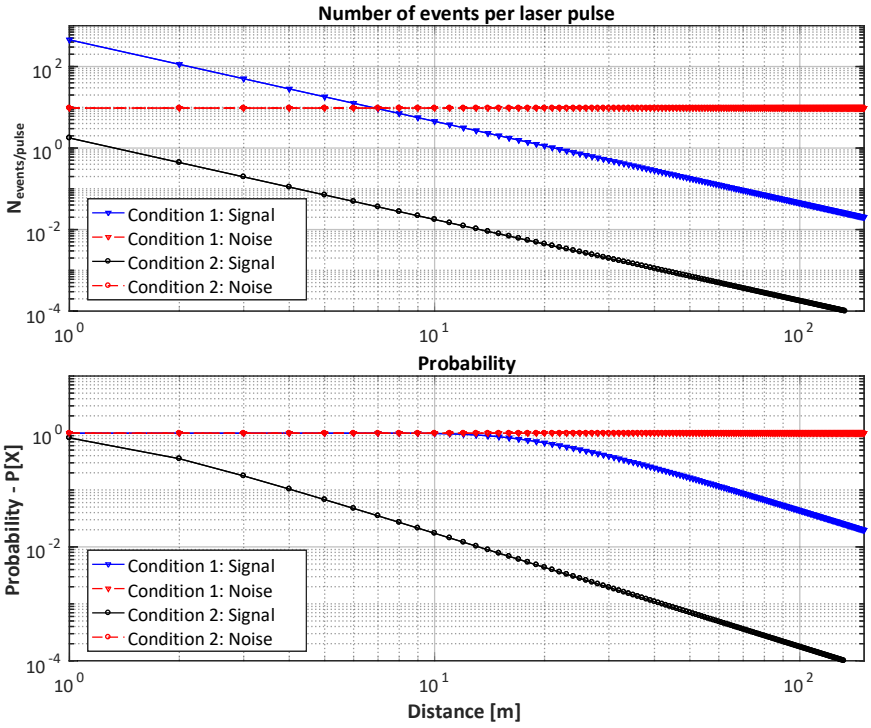



Figure 3.7: Total available number of events, per laser pulse, per pixel and probability of detection.

Here, some of the advantages of scanning (Condition 1), over flash (Condition 2), are noticeable. The probability of detection for Condition 1 is much larger than for Condition 2, which reflects on the maximum number of signal events, per laser pulse, that the illumination can potentially provide. Although, if the total number of signal events, per second, are considered, both conditions are similar, since in flash, all pixels are illuminated at all times, differently from scanning. However, for the noise, the continuous exposure of pixels to noise, from Condition 2, implies in the accumulation of much more noise than in Condition 1. An adjusted number of events, per second, is displayed in Figure 3.8, where the

relation between noise and signal is more explicit. The SNR of each pixel, per second, is much larger in Condition 1 than in 2.

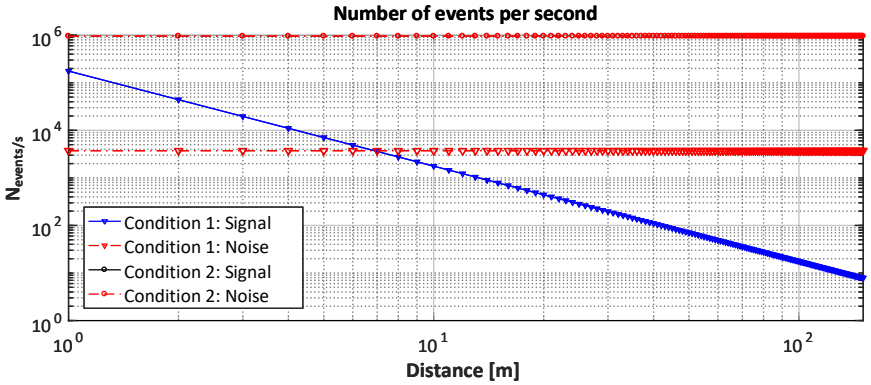



Figure 3.8: Total available number of events, per second, per pixel.

### 3.3.1. Coincidence detection

One of the most powerful features of dTOF systems is their robustness to high background noise and the ability to operate under low ambient illumination, through the accumulation of multiple events into a histogram, in a so-called time-correlated single-photon counting (TCSPC). Under TCSPC operation, multiple timestamps are accumulated into a histogram, where the object reflection signal ($< S >$) is consistently located within few bins, whereas noise ($< N >$) is uniformly spread.

Thus, assuming the laser pulse and overall system timing noise a Gaussian shape (in time), the target location can be extracted based on the signal-to-noise ratio ($SNR$), full width at half maximum ($FWHM$) of the returning signal and the measurement range, sketched in Figure 3.9. The signal-to-background noise-ratio ($SBNR$) is used to qualify the target detection, providing the ratio between the histogram peak over the uniform noise level.

The detected histogram shape will capture the uncertainties in the system, as a combination of the laser pulse width, detector and converter timing noise, and scattering effects in the air. Although more robust to negative $SNR$, a TCPSC system has its limitation in that the signal can only be detected if $SBNR > 1$, independently on the number of accumulated frames. The minimum condition for SNR must be:

$$SNR > \frac{FWHM}{0.9395 \cdot RANGE}. \tag{3.18}$$

If the example on Figure 3.9 is examined, the minimum SNR must be > -32dB, and much larger for a faster image frame rate. In fact, as will be seen in Section 3.3.4, this level of SNR is not very different from reality.

Moreover the limitation of signal acquisition, the presence of high background noise can produce several negative effects on the system. The most immediate is on the sensor

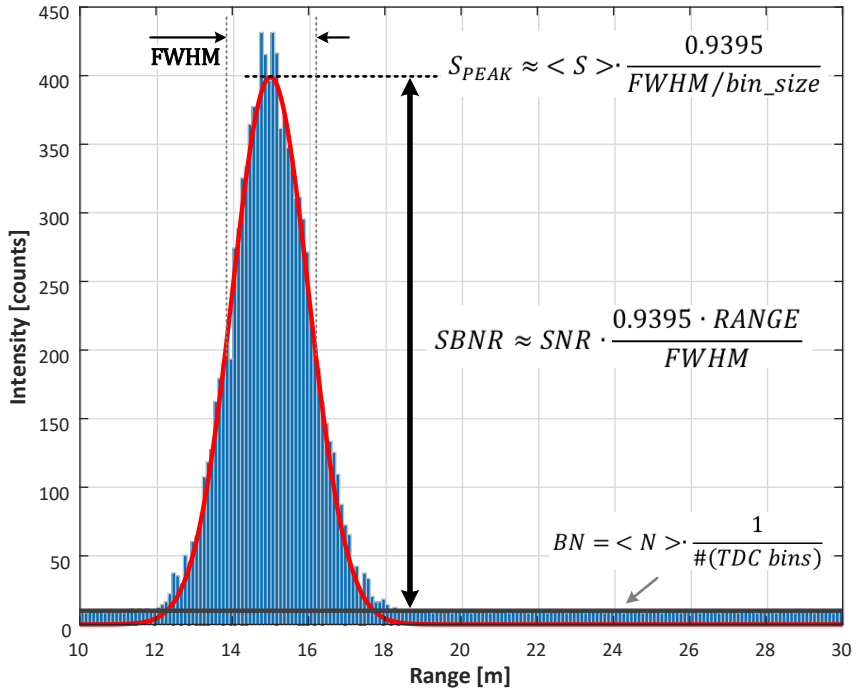



Figure 3.9: Histogram simulation of dTOF timestamps, for a fixed target: SNR = 1 (20k points), 1k TDC bins, signal FWHM = 2.355m, and 100m range.

operation, since a limitation on the maximum detection rate has an impact on signal detections, when flooded with noise. Also, the increase in sensor activity can drastically produce side effects on the operation uniformity, with an important impact on accuracy and precision. A secondary, and very important, effect is on data processing resources and power consumption, which can further limit the image frame rate.

Ideally, from the system point of view, it is optimum to read signal (and no noise) timestamps that matches exactly the chip readout frame rate, assuming that multiple events would be overwritten in the pixel memory. In other words, a single, new signal timestamp information suffices for the image sensor operation. However, this is far from reality in most of LiDAR cases.

It is of utmost importance to increase SNR and to limit the overall activity on the sensor, especially from noise. A useful way to perform such task is to make use of spatial and temporal correlation of photons that a dTOF system can provide. Since the light source is operated periodically and the returning photons from the target are correlated to it, neighbor pixels share also such correlation. Temporal, since targets at the same depth location (or close by) return at roughly the same time, and spatial (among neighbor pixels) can allow a discriminatory event acquisition that can reject noise, which is, in principle, uncorrelated.

A graphical illustration of such correlation is shown in Figure 3.10. In this hypothetical group of 5×5 pixels, some noise events, in red, are shown to be randomly spread over a time frame, which is a fair assumption. However, for signal events, in blue, because they

are the result of reflections from the target, and generated by the same source, roughly at the same time, they all fall in a coincidence window ($\Delta_{coincidence}$). A circuit that is capable to qualify coincident events produce a strong noise filtering.

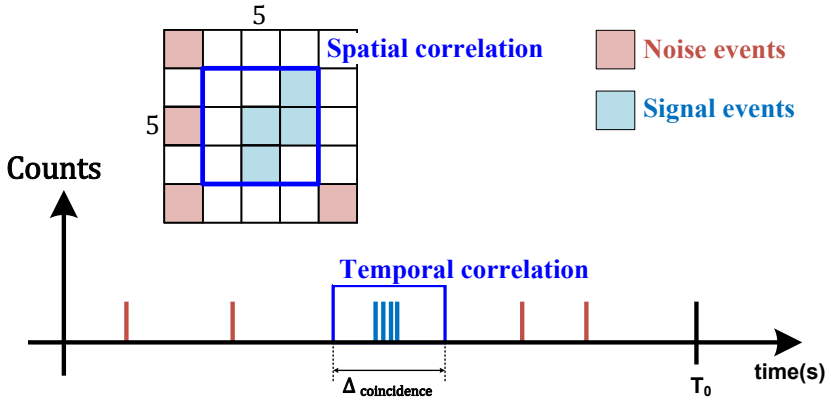



Figure 3.10: Graphical representation of temporal and spatial correlation of photons.

The number of pixels participating on the coincidence (spatial correlation) and the time width (temporal correlation), as well as the total number of events will depend on the application. The probability of both, signal and noise, calculated in (3.16) and (3.17), respectively, will change accordingly.

To calculate the probability of multiple events among several pixels, a binomial distribution can be used, as the $k$ number of success (positive coincidence detection) in a sequence of $n$ independent experiments, where $n$ is the number of pixels participating in the coincidence detection.

It is important to evaluate three distinct types of coincidence events:

1. True coincidence: between two or more signal events;

2. False "bad" coincidence: between two or more noise events;

3. False "good" coincidence: between one or more signal events and one or more noise events.

In case 1, the probability of detecting a coincidence event will be the product of the probability of detecting the signal itself, and a binomial distribution of any $k$ events among the remaining pixels:

$$p_{s\_true\_coinc.} = P(C \geq k) \cdot p_{s\_mod} = [1 - P(C < k)] \cdot p_{s\_mod}. \tag{3.19}$$

Changing the variable to $k' = k + 1$:

$$p_{s\_true\_coinc.} = [1 - P(C \leq k')] \cdot p_{s\_mod}, \tag{3.20}$$

where $P(C \leq k')$ is the binomial cumulative distribution function for $k-1$ events, among $n-1$ pixels of the coincidence pixel set, thus:

$$p_{s\_true\_coinc.} = \left[1 - \sum_{i=0}^{k-1} \binom{n-1}{i} \cdot p_{s\_mod}^{i} \cdot (1 - p_{s\_mod})^{n-1-i}\right] \cdot p_{s\_mod}, \tag{3.21}$$

where $k = 1, 2, 3, ..., n-1$. For $k = 1$, no coincidence is required, thus the probability reduces to simply $p_{s\_mod}$. Moreover, no coincidence window is actually applied, assuming that $\Delta_{coincidence}$ is large enough to accommodate all signal photons coming from the target, since the probability of detecting a signal, outside an expected window, is zero.

In case 2, where false coincidence events are generated solely by noise, the effect of noise suppression will be reduced. The probability of detecting this false coincidence will be the product of a single noise event, given by (3.17), and the probability of another event occurring among $n-1$ pixels, within $\Delta_{coincidence}$, defined by a Poisson distribution with average activity related to the coincidence window, such as:

$$p_{n\_false\_coinc.} = \left[1 - \lambda_{nc} \cdot \sum_{i=0}^{k-1} \frac{\lambda_{nc}^{i}}{i!}\right] \cdot p_{n\_mod}, \tag{3.22}$$

where $\lambda_{nc} = \lambda_n \cdot (n-1) \cdot \Delta_{coincidence}$.

In case 3, the probability of false "good" coincidence is the product of $p_{s\_mod}$ and the Poisson distribution with average activity related to the coincidence window, such as:

$$p_{s\_false\_coinc.} = \left[1 - \lambda_{nc} \cdot \sum_{i=0}^{k-1} \frac{\lambda_{nc}^{i}}{i!}\right] \cdot p_{s\_mod}. \tag{3.23}$$

Since a false "good" coincidence is still a valid signal, the total signal probability will be a combination of (3.21) and (3.23), limited to one event per laser pulse. In summary:

$$\begin{aligned} p_{s\_coinc.} &= min\left(p_{s\_true\_coinc.} + p_{s\_false\_coinc.}, 1\right) \\ p_{n\_coinc.} &= p_{s\_false\_coinc.} \end{aligned} \tag{3.24}$$

The ultimate goal of coincidence detection is to artificially increase the SNR. Inevitably, some signal events will also be filtered out by the system, however, noise events should suffer a much stronger suppression.

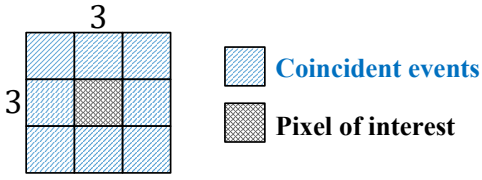



Figure 3.11: Arrangement of 3×3 pixels, for coincidence detection.

Figure 3.11 shows a hypothetical arrangement of 3×3 pixels that can participate on the coincidence detection, thus $n = 9$. Each pixel, independently, have a probability of detecting

a signal event equals to $p_{s\_mod}$, as calculated before. The probability of detection events depending on the constraints defined by the minimum number of events (max. of 9) and coincidence window ($\Delta_{coincidence} = 2$ ns) is shown in Figure 3.12.

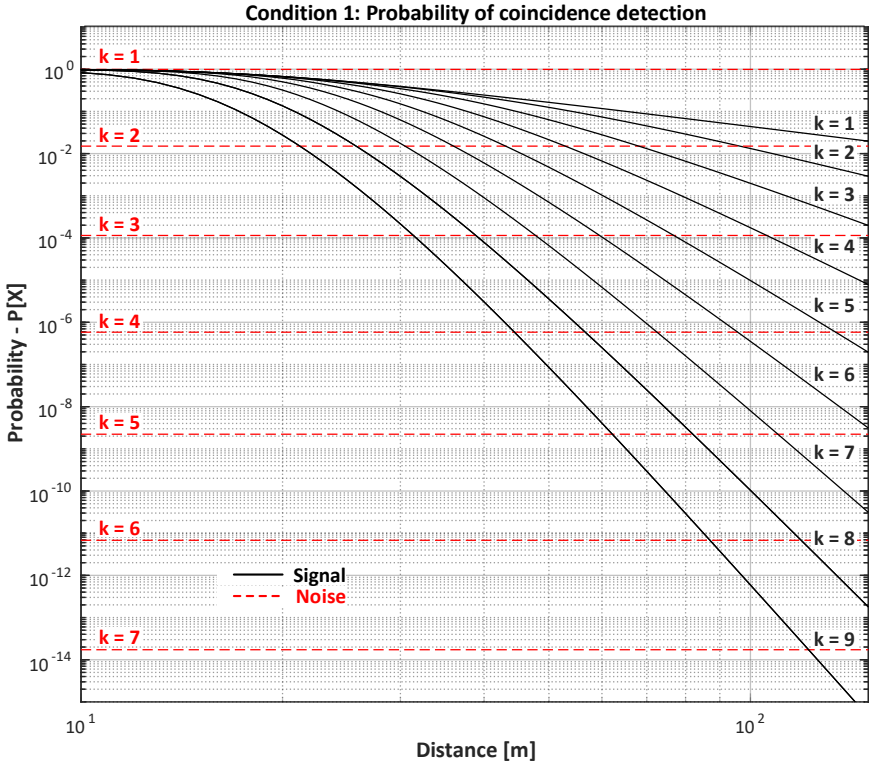



Figure 3.12: Coincidence detection for scanning (Coindition 1), for signal and noise.

The relation between probabilities of signal and noise detection must be compared for the same $k$. As mentioned before, $k = 1$ means no coincidence detection; if $k = 9$, as in this example, it means that all pixels of the 3×3 group need to detect an event each to be considered a valid hit, which, as can be seen from Figure 3.12, it is very low. Nevertheless, the appropriate coincidence configuration will depend on the condition (distance, perhaps) and should be set appropriately.

Figure 3.13 shows the similar case for Condition 2. Due to much lower signal power per pixel, the probability of detection is also much smaller. If both plots are compared, a clear indication of the superiority of scanning system in comparison to flash can be seen, as far as the signal detection is concerned.

Similarly, if the total number of events per second is adjusted for both conditions, the plot in Figure 3.14 is obtained. If the condition of (3.18) is respected, using the system conditions of $FWHM$ and $RANGE$ (SNR > -60dB), it is possible to calculate the maximum resolvable distance each configuration can provide, for both conditions and number of coincidence detection, given by in dashed lines in the plot.

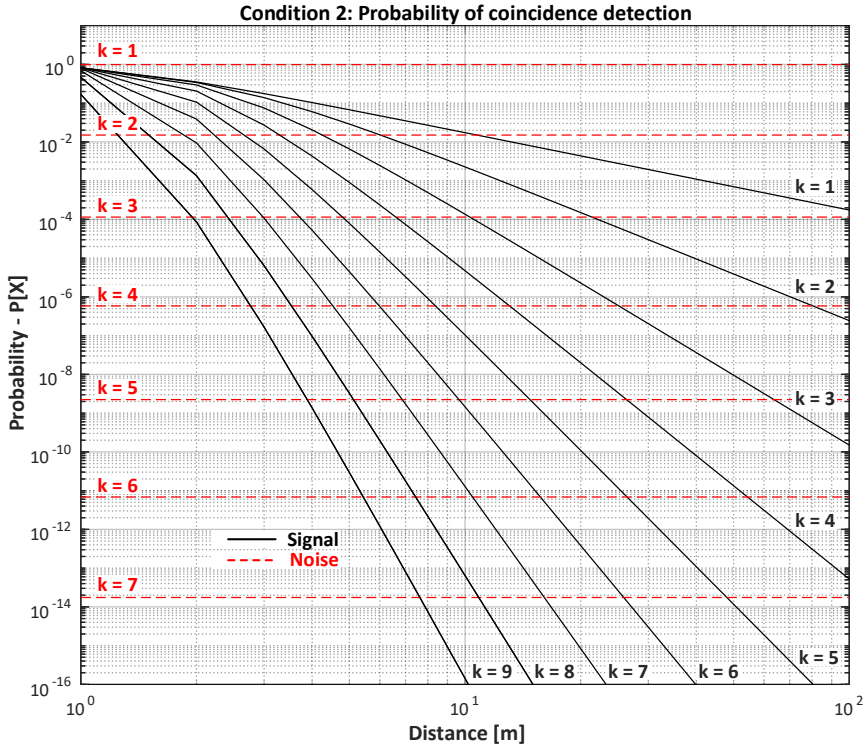



Figure 3.13: Coincidence detection for flash (Coindition 2), for signal and noise.

For Condition 1, the maximum ranges are 104 m and 128 m, for no coincidence ($k = 1$) and with at least 2 coincidence events ($k = 2$), respectively; For Condition 2, on the other hand, the maximum ranges are only 4 m and 20 m. A way to increase the maximum range of Condition 2 would be to shrink the integration window ($T_{int}$), reducing the amount of accumulated noise, but with penalty on the range. For instance, if $T_{int} = 200$ ns ($RANGE = 30$ m) is used instead of 1 $\mu$s, the maximum resolvable range increases to 13 m and 30 m. In the end of this chapter, the subject will be re-visited, where other modifying parameters (yet to be developed further on) will be included, and a family of plots for maximum range will be obtained.

An important observation about these results is that they are based on the overall sensor activity, without any restriction due to image or chip frame rate. It means that the measurement is performed indefinitely and all the data is gathered, thus setting the absolute maximum measurable range. As will be seen in Section 3.3.4, however, limitations on data access will reduce the maximum observable range considerably, where a minimum of events are to calculate the histogram.

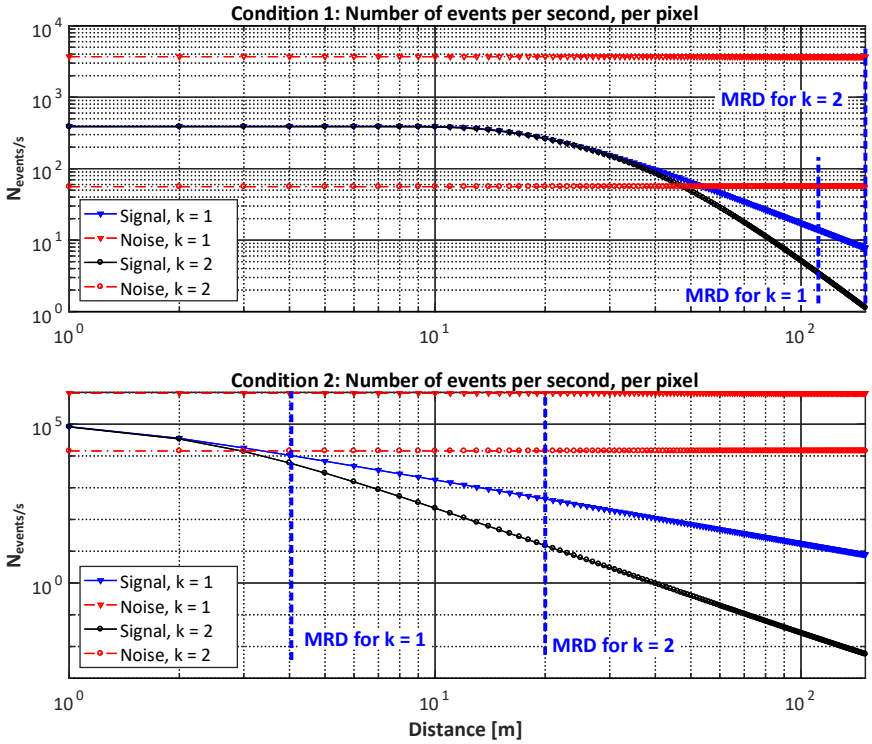



Figure 3.14: Coincidence detection comparison for both Conditions, with dashed line for maximum resolvable distance (MRD).

### 3.3.2. Sharing

Very often, in order to reduce silicon area and power consumption, several pixels share common elements, similarly to what happens in RGB imagers, where a single ADC per column is used to readout and convert the voltage/charge all pixels in that column. Although dTOF sensors deal with timing information, which is typically difficult to store for later conversion, they too often share the conversion blocks, such as TDCs. In some cases, each pixel contains all necessary circuitry for detection and conversion, rendering a very low fill-factor and setting constraints on maximum activity due to excessive power consumption [5–7].

When combining pixels, for instance, sharing a single TDC, column-wise timing, etc., such as the arragements of Figure 3.15 a dead time it is expected in the combination circuit ($T_{win}$), which would limit the saturation of the sensor for short pulses (typical of laser pulses). Extremely high background noise can also de-sensitize the sensor, since potential noise events would occupy the combination circuit when the actual event occurs. The concept is shown in Figure 3.16.

The compressed counting rate can also be analyzed using the probability of detecting a signal or noise event, once the maximum detection per pixel will be one (at most, a single signal event, per pulse). The compressed probability, due to sharing, can be calculated

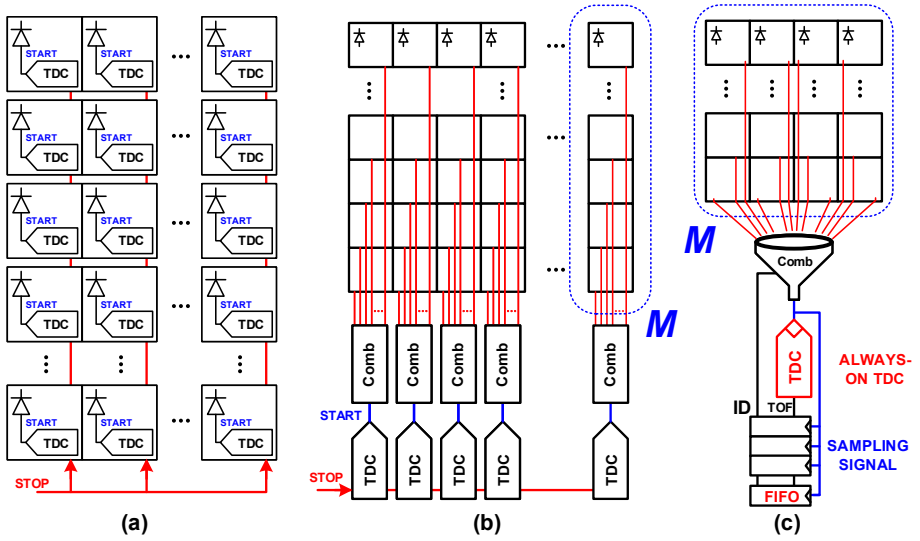



Figure 3.15: TDC arrangement. (a) per-pixel, event-driven TDC; (b) column-wise shared TDC; (c) continuously running, shared TDC concept.

by [8]:

$$p_{s\_compressed} = \frac{p_{s\_coinc.}}{1 + (M-1) \cdot \frac{T_{win}}{FWHM_{system\_grp}} \cdot min\left(p_{s\_coinc.} + p_{n\_win}, 1\right)}, \tag{3.25}$$

where $M$ is the total number of pixels sharing a TDC, $T_{win}$ is the combination circuit dead time, $p_{s\_coinc.}$ is given by (3.24), and $p_{n\_win}$ is the probability of having at least one noise event within $T_{win}$, given by:

$$\begin{aligned} p_{n\_win} &= 1 - P(N_{win} = 0) = 1 - e^{-\lambda_{n\_win}}, \\ \lambda_{n\_win} &= (\lambda_n \cdot F_{laser}) \cdot (M-1) \cdot T_{win} \cdot p_{n\_coinc.}, \end{aligned} \tag{3.26}$$

where $\lambda_{n\_win}$ is the average noise rate per combination dead time, for all $M$ pixels. $FWHM_{system\_grp}$ is the total $FWHM$ for the whole group of $M$ pixels. Here, the spread would depend on the target, where we can assume it to be the same as the $FWHM_{system}$, which is the worst-case scenario (equidistant target). The compressed activity of noise is assumed negligible, since it is very close to $p_{n\_coinc.}$, which is also the worst-case scenario, since a compression on the noise detection would be beneficial for the system.

An example of such compression can be analyzed considering a system where several pixels share a single converter, where multiple timestamps can be acquired (in a First-In-First-Out memory, for instance), but they are restricted to a processing dead time ($T_{win}$). Let us assume 8 pixels participate in such scheme, through a chain of OR logic gates (for symmetry, 3 levels – 8-to-1), where $T_{win} = 360$ ps. Those values are assumed based roughly on typical CMOS processes. The compression can be seen on the maximum detectable signal events, shown in Figure 3.17.

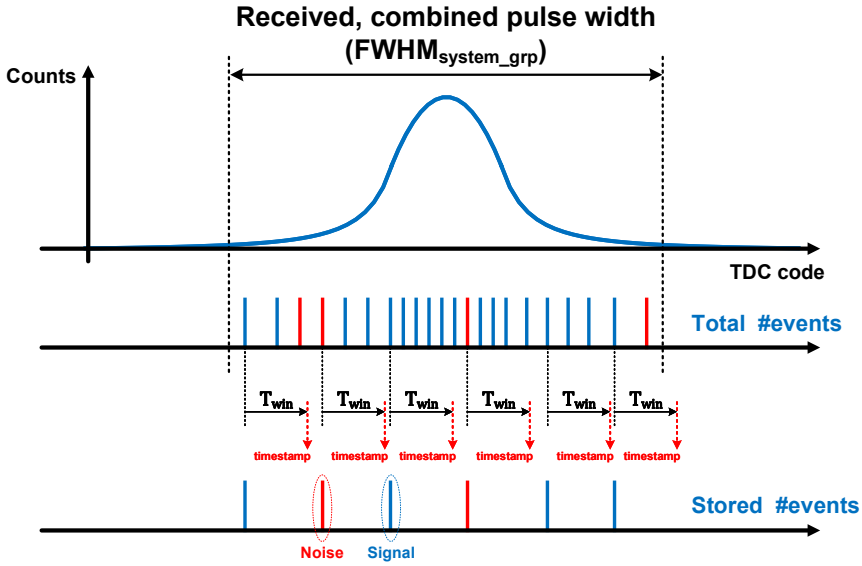



Figure 3.16: Effects on sensor sensitivity due to finite dead time on the combination circuit. Total #events indicates the incoming events at the detectors, whereas the stored #events are the events that are propagated.

The available signal events are the total number of photons that reach the sensor and are capable to generating a avalanche event, similarly as seen in Figure 3.8. The effective signal events are actual photons that generated an avalanche event, once again assuming only a single signal event per laser pulse is possible. The detected events (signal and noise) are those events that finally made through the process and which timestamp has been registered.

As can be seen from Condition 1 of Figure 3.17, the effects of sharing are very well pronounced, limiting the maximum number of signal events per pixel, per second, to about 100, until the distance of 28 m, with a natural drop due to low intensity (where the compression is not relevant, due to low activity) for longer distances. On Condition 2, on the other hand, the total amount of detectable events is much larger (to over 20k at 1 m), since they are weak, which means less conflicts and, consequently less compression, and are exposed all the time.

By comparing the total number of detected events between Conditions 1 and 2, it is counter-intuitive to think that scanning mode can provide better results in distance ranging than flash. The reason is the overall noise the system acquires, which in Condition 1 is much lower than in Condition 2. It also allows the assumption that, in the absence of background illumination and DCR, flash mode is far superior than scanning, specially for distances shorter than 30 m (in our hypothetical cases, obviously).

### 3.3.3. Gating

Another way to filter the background noise is to enable the sensor only around the target. A sketch of a typical histogram, with and without gating, is shown in Figure 3.18. In this example, the noise is uniformly distributed over the time frame ($T_0$), which means that it

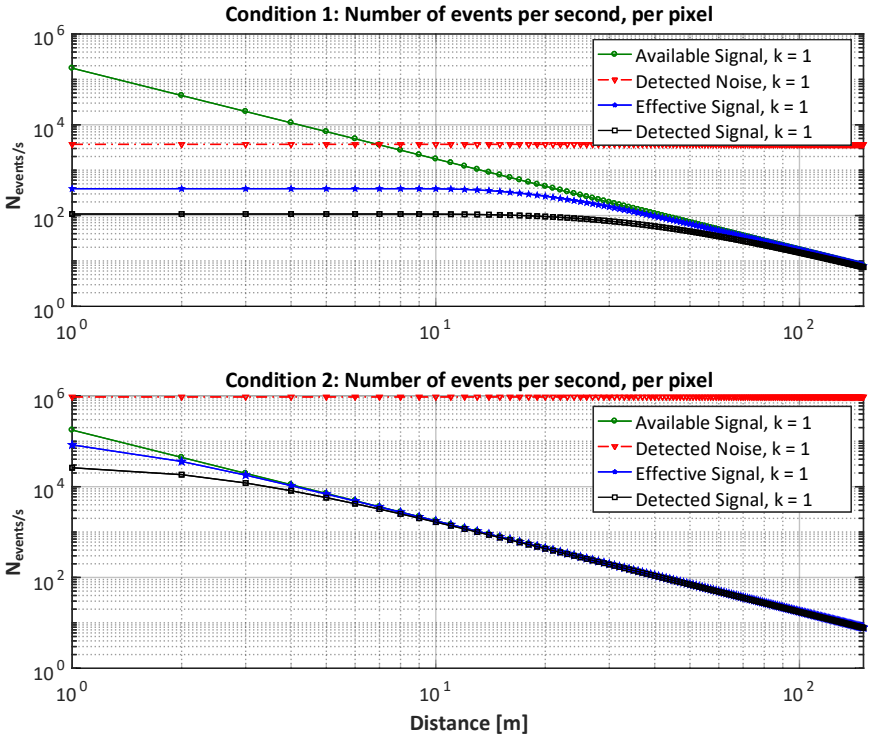



Figure 3.17: Effects of short bursts saturation and sharing on detectable signal events (coincidence detection is disabled – $k = 1$), for Conditions 1 and 2.

comes from a random source and has not correlated interaction, typical from a clear, sunny day.

As it can be deducted from Figure 3.18, the SBNR does not change inside the gate window, although it is improved elsewhere. The signal peak, over a background noise level, is still bounded to the same constraints of a situation without gating, however, the amount of events the sensor is required to handle is much smaller, so is the data processing resource required to perform histrogramming. For situation such as the example, it is required, from the system point of view, to know what is the target location and, most importantly, that there is only a single target location for the whole sensor.

Evidently, if targets in different locations are present and only a single gating mechanism for the whole array is possible, the gating window should be swept constantly over $T_0$, thus no target is missed. In this condition, not much improvement is obtained, especially if only uniformly distributed noise is present, although it can still be beneficial for low SNR, since the histogram of each window can be performed separately. The drawback, however, is related to the image frame rate, since the signal, like the noise, are both reduced by $T_{gate}/T_0$.

The challenge is to implement a system with multiple gating regions and a selection mechanims capable of dynamically switching between different time gates, in order to offer

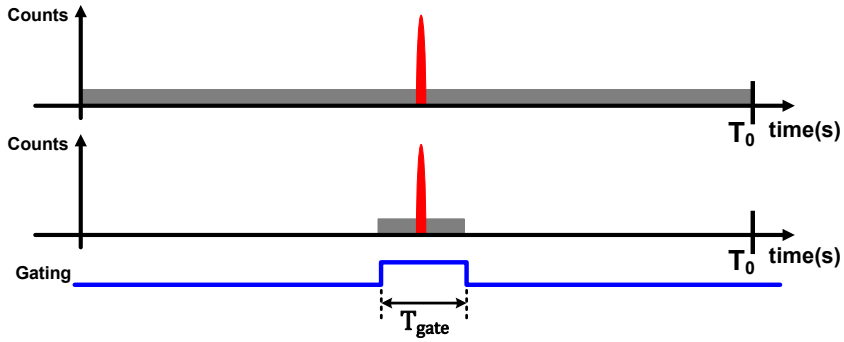



Figure 3.18: Gating effects on the histogram, in the presence of uniformly distributed background noise.

optimum noise filtering in different regions of the sensor.

Perhaps, the most important advantage of gating is for situations where the noise is not uniformly distributed. The presence of fog and rain, for instance, can produce a noise profile that can overcome the target reflection counts, although around the target the signal return could be stronger. A sketch of such conditions is displayed in Figure 3.19.

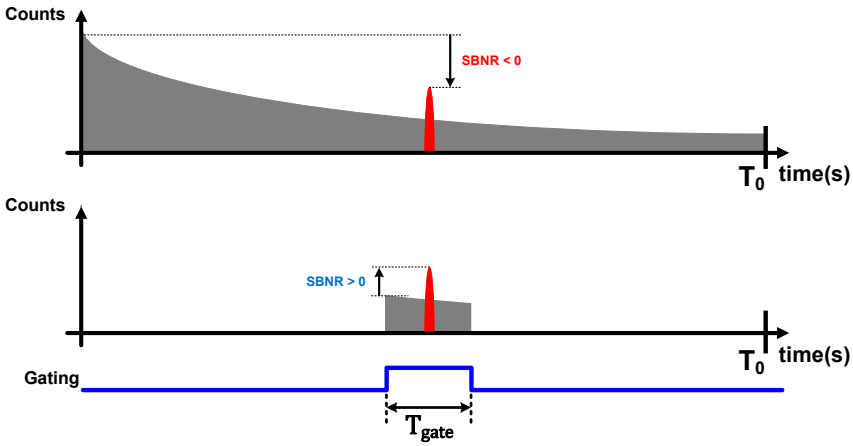



Figure 3.19: Gating effects on the histogram, in the presence of non-uniformly background noise.

### Fog and rain

There are several atmospheric light scattering phenomena that would influence the signal detection, which is not bounded to only fog, smoke, and rain conditions, but for a regular clear sky day. The light scattering is a combination of two distinct sources: extinction and in-scattering. The former is related to light extinction, though absorption or out-scattering (out of the observer field-of-view), and the latter is related to light addition, from the sun, for instance. It can be expressed by [9]:

$$L_{scattering} = F_{ex} \cdot L_0 + L_{in}, \tag{3.27}$$

where $F_{ex}$ is a extinction factor, $L_0$ is the source power, and $L_{in}$ is the added light intensity, as functions of the distance $s$. The light extinction has two a exponential components, $\beta_{ab}$ and $\beta_{sc}$, for absorption and out-scattering, respectively, which are shown in Figure 3.20. Thus:

$$F_{ex}(s) = e^{-(\beta_{ab}+\beta_{sc})\cdot s}. \tag{3.28}$$

Both scattering components will depend on the type of media. Different fog density, smoke particle size, and water droplet will influence the scattering coefficients.



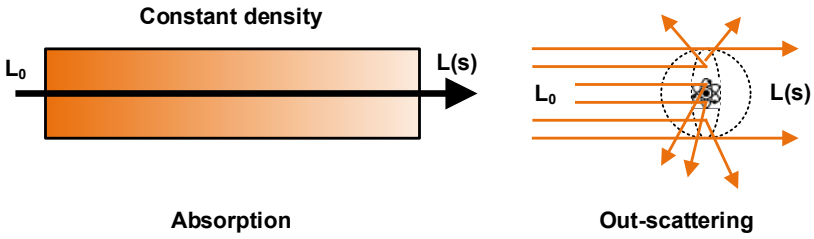



Figure 3.20: Extinction scattering components: absorption and out-scattering.

For in-scattering, the scattering depends on the angle of incident light traversing the media. The light intensity can be expressed by:

$$L_{in}(s,\theta) = \frac{1}{\beta_{ex}} \cdot E_{sun} \cdot \beta_{sc}(\theta) \cdot (1 - e^{-\beta_{ex} s}), \tag{3.29}$$

where $\beta_{ex} = \beta_{ab} + \beta_{sc}$.

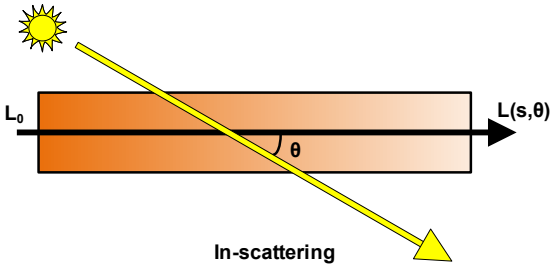



Figure 3.21: Extinction scattering components: absorption and out-scattering.

By successfully modeling the scattering occurring in conditions of fog and rain, which have different particle sizes, a model can be created. One important remark regards the type of noise such scattering medium would produce. For the background noise, there is no correlation with the system operation frequency, thus would still appear as uniformly distributed noise. However, the returning light from the system illumination source, which

produces the profile seen in Figure 3.19, produce correlated events, which reduce the power of coincidence detection, allowing more false "bad" coincidence events, as well as it reduces the overall optical power delivered to the target and returned, since there is scattering in both trips.

### 3.3.4. System considerations

From the system point of view, the maximum number of events (signal and noise), as calculated before, is an indication of the maximum activity, but it does not represent the actual number of acquired timestamps. In fact, the maximum conversion rate and chip readout rate defines the available timestamps to the "outside world" to perform the required histograms. When image frame rate is considered, even fewer timestamps per image are available, setting constraints on the minimum SNR (and SBNR) to perform a acceptable image.

The system architecture plays an important on the maximum number of timestamps. Event-driven architectures, such as per-pixel TDC [5–7], for instance, are limited to a single detection per time frame, thus the maximum conversion rate is $F_{laser}$, assuming the chip can also be readout at $F_{laser}$ rate or multiple memory levels, which are both not easily implementable. Always running, shared TDC architectures [10] can allow a higher throughput, increasing the conversion rate and easing the memory allocation, but are dependent on the combination circuit, which also limits the conversion rate.

The expected number of signal events is a combination of (3.24), (3.9), and the $F_{laser}$. For the noise, it is a combination of (3.24) (3.24), (3.13), and the $F_{laser}$, such as:

$$\begin{aligned} N_{total\_signal\_events} &= N_{signal\_events/pulse} \cdot F_{laser} \cdot p_{s\_coinc}, \\ N_{total\_noise\_events} &= N_{noise\_events/pulse} \cdot F_{laser} \cdot p_{n\_coinc}. \end{aligned} \tag{3.30}$$

Statistically, the total number of events can be calculated by a down-sampling the total number of events by the minimum rate between the actual number of recorded events, chip readout, and conversion rate, such as:

$$\begin{aligned} N_{total\_events} &= N_{total\_signal\_events} + N_{total\_noise\_events} \\ N_{effective\_events} &= \Downarrow \left( N_{total\_events}, min\left( N_{total\_events}, CR, RR \right) \right), \end{aligned} \tag{3.31}$$

where $CR$ is the conversion rate, per pixel, and $RR$ is the readout rate. In event-driven architectures, the readout is performed based on the activity, thus the limitation is the total number of events themselves.

One special case is when gating (section 3.3.3) is performed. Depending on the architecture (3.31) and if the gating is fixed or moving, the down-sampling will be non-uniform. For a fixed gating, the number of noise events will be scaled by by the gating ratio, whereas the signal is unaltered, using the same down-sampling rate; for a moving gating, however, both signal and noise events scale by the gating ratio, already contemplated by (3.31).

### 3.3.5. Discussion

Time-of-flight imaging can be very complicated, involving several parameters that require optimization, as seen during the development in this chapter. For this reason, a MATLAB model has been written, taking all previous discussions into account, i.e., signal and noise

probabilities, coincidence detection, gating, effects of sharing, maximum conversion rate, chip readout rate, etc.

There are several approaches to design the system. One can start from setting the maximum and minimum limits of detection and desired AFOV, and work backwards to define the minimum laser power required, considering the expected background noise, whilst maintaining eye-safety. In our case, a couple of conditions were established at the beginning of the chapter, with exactly the same specs, but different operation approaches (scanning and flash modes), so they could be compared. A 60°AFOV, maximum background noise of 98 klux, and maximum optical power of 16 mW were used.



The main differences between scanning and flash with respect to $SNR$. In flash mode (Condition 2), the pixels operate all the time, accumulating noise continuously, whereas the scanning, for each point, the total integration time is very short, so the system can move on to detect the next point, etc. For the signal, both approaches receive the same amount to energy, which makes the $SNR$ of flash much lower than the scanning. This was shown in Figure 3.8, with the total available events, per second. From that plot, the $SNR$ of scanning is equal to 1 at 7 m for the scanning mode, whilst it always negative for flash, which means that single-shot measurement is compromised in the latter case. Although single-shot measurements are not the scope of this work (which would be improved by reducing the AFOV), it is an indication of the energy levels both conditions operate.

One important observation that needs to be made regards the pixel saturation for short bursts of activity. Since the laser pulse and, consequently, the reflected light, are relatively short ($FWHM$ = 1 ns, in our case) compared to the SPAD dead time ($SPAD_{deadtime}$ > 10 ns), it is assumed that for each laser pulse, the maximum of a single detection can occur, independently on how strong the laser pulse is. This saturation is represented by the bounded probability and effective number of signal events obtained at Section 3.3.

This condition is somewhat worsened when several pixels are arranged in a sharing configuration, in case the sensor is designed to re-utilize some of the blocks, such as column-based TDC architectures [11, 12]. The inevitable conflicts that will occur, coming mostly from the signal, since the target photons will arrive near to each other, in space and time, but also in the presence of high background noise. This extra saturation is discussed in Section 3.3.2.

Regarding the maximum observable range, for each distance measurement, a histogram needs to be calculated and, depending on the signal uncertainty and maximum range, a large number of events must be recorded for a good $SBNR$. These dependencies were already considered by (3.18), but, as discussed, this limit is valid for an indefinite integration only. Since the system is discrete, where the timing information is accumulated in histogram bins, the $SBNR$ found in (3.18) is not sufficient to determine the efficiency of the system. For a more robust limit, we can set the requirement of $SBNR >> 1$, so a high ratio can be obtained, as well as a minimum absolute number of signal events.

Figure 3.22 displays the effects of limited data availability, for a 10 fps image, and different coincidence events. For the ideal case, where $SBNR = 1$ and the number of signal events per frame (Signal/Frame) is also 1, the maximum range is obtained, but in reality the image quality and the ability to actually detect the signal would be compromised. For a more robust case, where the $SBNR = 10$ and at least 10 signal events per frame is required, the range reduces, but the quality is maintained. Effectively, no difference on the operation

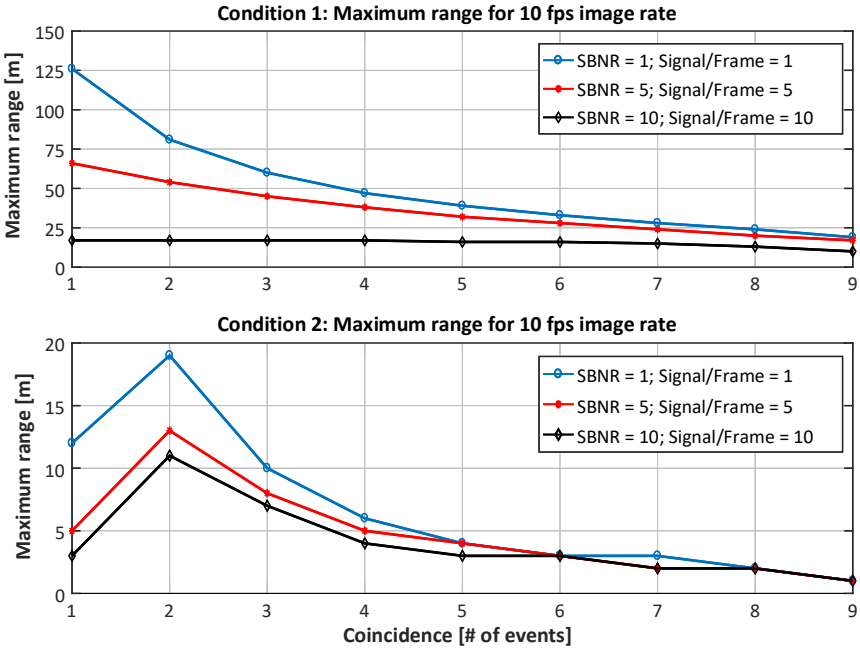



Figure 3.22: Maximum detectable range with chip readout and image frame rate are considered.

is simulated, only the parameters for establishing a good picture.

From Figure 3.22, an important observation can be made regarding Condition 1: coincidence detection does not increase the maximum observable range. It appears that without any coincidence (index 1 in the plot), the range is the maximum. The reason is that, for scanning, the noise is already low, compared to signal, due to short integration time. Sharing reduces the maximum range, due to conflicts between signal events, but it has little influence on shape of the curve. In Condition 2, on the other hand, coincidence detection can really increase the maximum observable range, although much lower than Condition 1, as discussed.

One welcomed effect that coincidence can bring to the system is on the reduction of the overall sensor activity, while guaranteeing an improvement in $SNR$. Since the amount of noise can completely saturate the sensor, data throughput, post-processing capability, etc., coincidence detection can be used to modulate the sensor activity, reducing also power consumption. Figure 3.23 shows a simulated histogram based on Condition 1, for none or 2 coincidence events. Without coincidence, the amount of noise events the system is required to process dropped from almost 3700 to only 56, while the signal reduced from 40 to 31. As expected, from Figure 3.17, the number of signal events at 54 m is still very high, while the noise is relatively low, providing a substantial increase in $SNR$ and $SBNR$ of over 34 dB in both. The system activity is expected to be very low, as well as its power consumption.

A similar result was obtained for Condition 2, which is plotted in Figure 3.24. Since the noise behaves similarly in both systems (except for what relates sensor saturation), its reduction is almost the same as Condition 1, of about 66x, dropping from almost 1 million

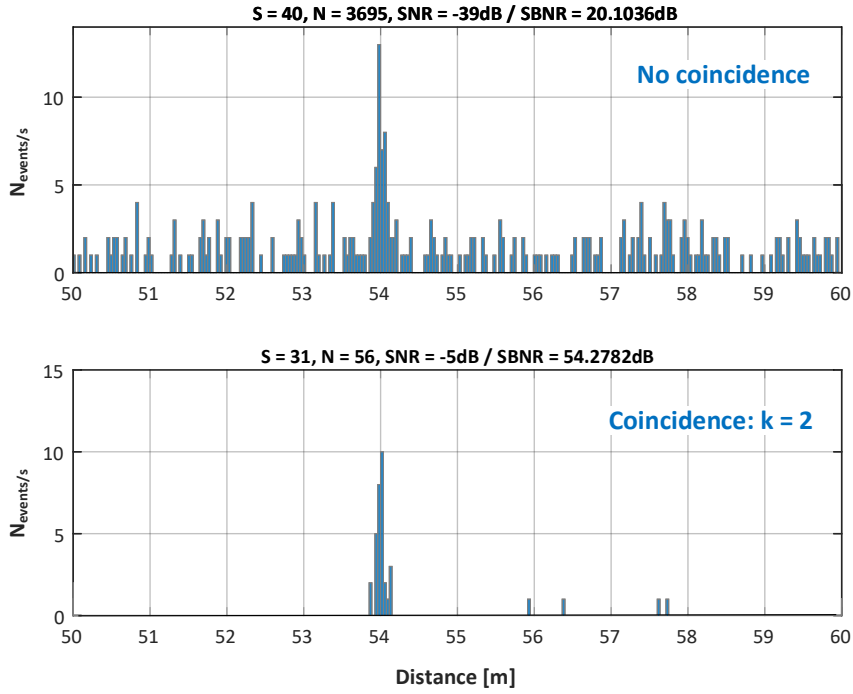



Figure 3.23: Histogram of Condition 1, without and with at least 2 coincident events.

noise events to less than 15,000. However, due to low signal intensity, the filtering effect of coincidence is also strong on the signal, of about 10x. Although not as impressive as the scanning condition, the $SNR$ and $SBNR$ for flash mode also improved with coincidence, of about 16 dB for both parameters.

## 3.4. CONCLUSION

In this chapter, some important techniques to increase the system $SNR$ were exploited and modeled. The main one, coincidence detection, relies on the spatial and temporal correlation of photons among neighboring pixels, coming form the target, to distinguish between signal and noise. If, on the one hand, this technique inevitably reduces the probability of detecting a valid, target photon, on the other hand, the effects on the noise reduction are much stronger, allowing a gain in $SNR$. However, it does require a certain optical power level, thus favoring less frequent, higher energy pulses (to maintain constant the average optical power), as discussed in Section 3.3.1.

It is unquestionable the superiority in signal detection of scanning systems, in comparison to flash LiDAR. For the same conditions, scanning can reach farther distances than flash, with higher reliability, although mechanical restrictions can limit image frame rate, as well as adding issues on scan/sensor synchronization. That being said, flash mode LiDAR have the advantage of no moving parts and, for short distances and lower background illumination, it can be a viable solution for mobile applications. Solving the issues of moving

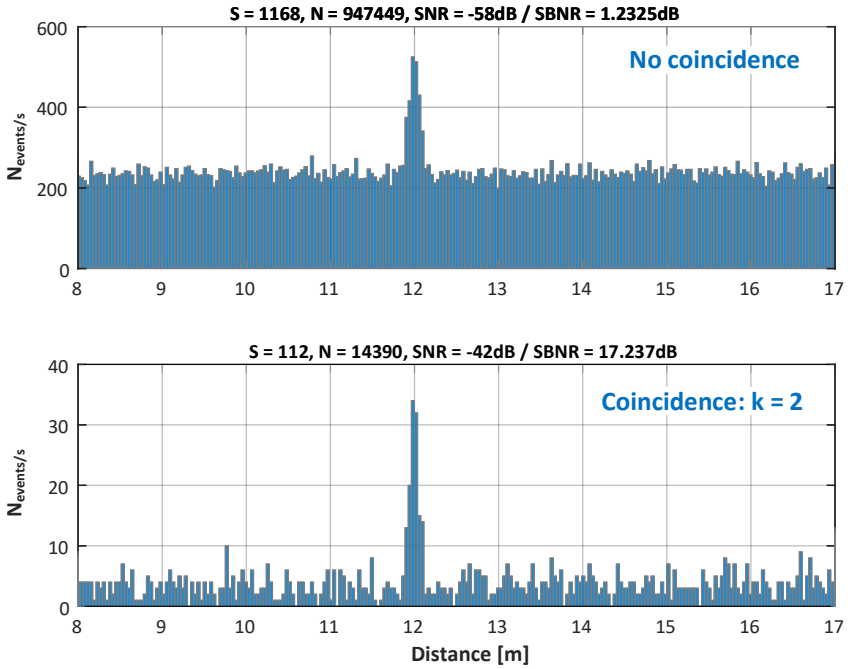



Figure 3.24: Histogram of Condition 2, without and with at least 2 coincident events.

parts, through optical phase arrays for example, a potentially ideal solution for integrated LiDAR systems can be obtained. Moreover, as discussed in Section 3.3.3, gating does not change the *SNR* around the target, but it allows the sensor to increase its dynamic range, producing similar effects on the power consumption, as well as being capable of handling scattering mediums, such as fog and rain conditions.

# REFERENCES


[1] A. Ronchini Ximenes, P. Padmanabhan, and E. Charbon, *Mutually coupled time-to-digital converters (tdcs) for direct time-of-flight (dtof) image sensors,* Sensors **18**, 3413 (2018).

[2] J. J. Wierer Jr, J. Y. Tsao, and D. S. Sizov, *Comparison between blue lasers and light-emitting diodes for future solid-state lighting,* Laser & Photonics Reviews **7**, 963 (2013).

[3] Y. Wang, W. Yang, H. Zhou, M. Huo, and Y. Zheng, *Temperature dependence of the fractional thermal load of nd: Yvo 4 at 1064 nm lasing and its influence on laser performance,* Optics express **21**, 18068 (2013).

[4] A. E892-87, *Tables for Terrestrial Solar Spectral Irradiance at Air Mass 1.5 for a 37-Deg Tilted Surface* (ASTM International, West Conshohocken, PA, 1992).

[5] C. Veerappan, J. Richardson, R. Walker, D.-U. Li, M. W. Fishburn, Y. Maruyama, D. Stoppa, F. Borghetti, M. Gersbach, R. K. Henderson, *et al.*, *A 160× 128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2011) pp. 312–314.

[6] F. Villa, R. Lussana, D. Tamborini, D. Bronzi, B. Markovic, A. Tosi, F. Zappa, and S. Tisa, *Cmos single photon sensor with in-pixel tdc for time-of-flight applications,* in *Time-to-Digital Converters (NoMe TDC), 2013 IEEE Nordic-Mediterranean Workshop on* (IEEE, 2013) pp. 1–6.

[7] F. Villa, R. Lussana, D. Bronzi, S. Tisa, A. Tosi, F. Zappa, A. Dalla Mora, D. Contini, D. Durini, S. Weyers, *et al.*, *Cmos imager with 1024 spads and tdcs for single-photon timing and 3-d time-of-flight,* IEEE J. Sel. Topics Quantum Electron. **20**, 364 (2014).

[8] S. H. Lee and R. P. Gardner, *A new g–m counter dead time model,* Applied Radiation and Isotopes **53**, 731 (2000).

[9] R. V. Klassen, *Modeling the effect of the atmosphere on light,* ACM Transactions on Graphics (TOG) **6**, 215 (1987).

[10] S. Lindner, C. Zhang, I. M. Antolovic, M. Wolf, and E. Charbon, *A 252×144 spad pixel flash lidar with 1728 dual-clock 48.8 ps tdcs, integrated histogramming and 14.9-to-1 compression in 180nm cmos technology,* in *2018 IEEE Symposium on VLSI Circuits* (IEEE, 2018) pp. 69–70.

[11] L. H. Braga, L. Pancheri, L. Gasparini, M. Perenzoni, R. Walker, R. K. Henderson, and D. Stoppa, *A cmos mini-sipm detector with in-pixel data compression for pet applications,* in *IEEE Nuclear Science Symp. and Medical Imaging Conf. (NSS/MIC)* (2011) pp. 548–552.

[12] A. Carimatto, S. Mandai, E. Venialgo, T. Gong, G. Borghi, D. R. Schaart, and E. Charbon, *A 67,392-SPAD PVTB-compensated multi-channel digital sipm with 432 column-parallel 48ps 17b tdcs for endoscopic time-of-flight pet,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2015) pp. 1–3.

# 4

# INTEGRATED TIMING SOLUTIONS FOR VARIOUS APPLICATIONS

*For distinct systems to operate in consonance, they must share a common reference. Most of current communication systems use timing references to play this role, where imprecision can lead to bit error a total loss of data. Some system can tolerate the operation under relative timing reference, where the absolute phase and/or time is not relevant, such as wireless communication, however, some other systems require an absolute timing reference, such as the global positioning system (GPS). In both cases, timing is required to be kept known and precise. In direct time-of-flight, a precise time difference is essential for a good depth estimation. There are several ways to obtain a precise timing in silicon. In this chapter, some of the solutions found in communication and time-of-flight image sensing will be discussed.*

Parts of this chapter have been published in [1, 2].

## 4.1. INTRODUCTION

DIRECT time-of-flight (dTOF) imaging requires precise time measurements, in order to accurately reconstruct the targets distances. As for any imaging system, most of the silicon area must be dedicated to the active photo-detectors (in this case, SPADs), limiting the remaining available area for signal processing, timing, memory, etc. The goal is to minimize the circuitry around the pixel, thus allowing pixel fill-factor maximization, while guaranteeing the timing uniformity required for a particular application. One alternative that relaxes such constraint lies on sharing architectures, such as column-wise TDCs [3], for instance, where a single converter is capable to convert multiple pixels timing information. Such arrangements have their own implications, more pronounced on sensor saturation and time skew between pixels, which will be discussed on Chapter 5.



Power consumption is another important parameter that requires optimization. Excessive power dissipation could lead to temperature variations and high IR-drop, which could, consequently, produce performance variations on detectors and converters, or event a complete operation failure [4]. Therefore, a solution for dTOF imaging must be small and consume low power. Other applications, such as wireline communication, clock recovery in microprocessors, etc., have similar performance constrains and shall also be used in this chapter, as a guideline for topology exploration.

Time-to-digital converter (TDC) is the most widely used time digitizer in CMOS, with its origin in all-digital phase-locked loops (ADPLL) [5]. It is a very important block and it has been serving as the foundation for monolithic dTOF sensor [6] development. There are many TDCs topologies available, which will be chosen depending on its application, size, range, resolution, conversion time, etc. Flash-TDC [7] is a very simple structure, however, its range is very limited, linearly proportional to the number of stages, $N$, and the TDC LSB, $\Delta_{LSB}$, as $TDC_{range} = N \cdot \Delta_{LSB}$. For instance, a timing range of 30 ns (about 4.5 m in distance) and a resolution of 30 ps requires 1000 stages, which is very area inefficient; it is difficult to control its linearity, etc. For these reasons, it has been widely used to obtain only short range and fine resolution, in both PLLs [5] and dTOF sensors [8]. Vernier-line TDCs can provide even finer resolution than the in case of flash-TDC. Here, it is the difference in delay between two chains of inverters; however, their range is even shorter with larger area [9] than with the flash-TDC. Although the area and range can be improved by means of ring oscillator (RO) based Vernier-line TDC [10], it still cannot provide very long range. Up to now, it has been employed mostly in PLLs due to its complexity and size. Time-to-amplitude-converter (TAC) is another way to digitize time, by means of first converting the time difference into a voltage, which is then digitized by an ADC [11]. It benefits from advances in the design of ADCs, yet its large area and analog nature, which degrades with the technology node, impose extra challenges on the design.

For imaging systems, the most common solution for time digitizers are based on ROs connected to ripple counters. They can be designed in a very small area, since the RO is typically small (depending on how it is controlled, its noise performance, etc.) and the number of stages in the counter increases only with $\log_2 N$. For example, for similar specs of 30 ns range and 30 ps resolution, only a 2-stage pseudo-differential RO and 8-bit counter is required, whereas the linearity depends only on the RO, since the ripple counter itself is intrinsically linear. However, it is very sensitive to supply voltage and temperature variations, thus normally requiring a PLL loop for its precise frequency operation. Other methods

helping to operate the open-loop RO-based TDCs are possible, such as a foreground calibration, for a precise resolution acquisition, with a penalty on the overall operation. Normally, a PLL is available to provide a precise timing reference for local (column-wise [3] or per pixel [12]) interpolation TDCs.

In this chapter, a different timing generation will be provided. Firstly, two ADPLLs will be described and proposed as a possible reference frequency for the dTOF image system. A comparison between the RO-based and LC-tank based ADPLLs will be examined, exploring the fact that the ROs are intrinsically noisy and sensitive to supply and temperature variations, whereas the LC-tank can ensure a much cleaner and robust reference; however, its area will be much larger. Thus, an ultra-compact LC-tank based ADPLL is proposed and their aspects evaluated. Finally, an alternative for a synchronized and distributed clock generation will be provided, based on future 3D-stacked technologies.



## 4.2. FREQUENCY SYNTHESIZER

Frequency synthesizer is a generic name given to electronic circuitry capable of generating precise frequency clocks. The most common synthesizer is based on a PLL, which consists on a negative feedback system designed to control the output frequency using a more stable crystal reference. Often, the desired frequency is a multiplied version of the reference, by an integer ratio ("integer-N" mode) and/or fractional ("fractional-N" mode). A block diagram of a generic PLL-based frequency synthesizer is shown in Figure 4.1.

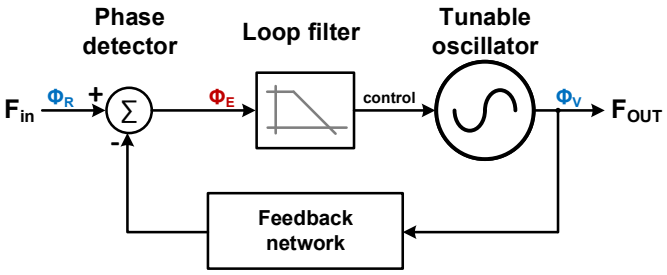



Figure 4.1: Generic PLL-based frequency synthesizer.

The tunable oscillator generates the desired output clock controlled by an analog voltage and/or a digital word, generated by the loop-filter, which is, in turn, in type-I proportional to the difference between the reference and output phases. The loop filter is responsible for setting the dynamics of the system, i.e. controlling the loop bandwidth and final phase error. It also determines the so-called type of the PLL, related to the total number of integrators in the loop. Since the PLL has always at least one integrator (the oscillator is a natural phase integrator, outputting the frequency), if the loop does not contain another integrator, it is called a type-I PLL, which is more stable at wider loop bandwidths, but it exhibits a non-zero phase error. If the loop contains another integrator, the loop becomes a type-II PLL, zeroing our the phase error.

Moreover, a wider bandwidth provides a faster settling time, but it offers less filtering capabilities; a narrow bandwidth filters out more unwanted spurs (from the reference and/or fractional, in case of Fractional-N mode), but results in longer settling times [13]. The

overall dynamics will depend largely on system specifications.

### 4.2.1. CHARGE-PUMP PLL

The term charge-pump PLL has been used to describe a widely popular analog frequency synthesizer topology, whose block diagram is shown in Figure 4.2 [14]. In this architecture, the high-frequency signal ($F_{OUT}$), from the voltage controlled oscillator (VCO), is divided and connected to the phase-frequency detector (PFD), along with an also divided version of the reference frequency ($F_{in} = F_{REF}/R$). The two phases, $\phi_R$ and $\phi_V$, are then compared and a pair of rectangular pulses, whose widths are proportional to the phase difference between $\phi_R$ and $\phi_V$, are generated. If the reference phase $\phi_R$ precedes $\phi_V$, then a pulse "Up" is produced, otherwise "Dn" is generated. Since the time difference between the two edges can exceed one output clock delay, in case the frequency differs, it is important to also acquire the absolute frequency. This is performed by combining "Up" and "Dn" pulses through a charge pump, which generates a charge integrated in a loop-filter. Depending on whether an "Up" or "Dn" pulse is applied, current is drawn from the supply to charge up or drain the loop-filter capacitors, respectively. As a result, the pulses are converted into a voltage that tunes the VCO. The combination of the loop-filter and the negative feedback connection creates a type-II loop, which is capable of phase and frequency locking, with zero residual phase.

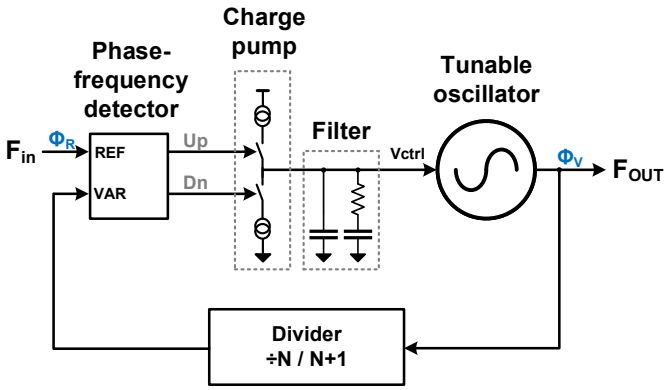



Figure 4.2: Generic charge-pump PLL.

The divider in the feedback path scales $F_{OUT}$ down to a $F_{REF}/R$ for the comparison to take place at the PFD. In the integer operation (integer-N mode), $N$ is chosen as a constant, in order to provide the desired frequency multiplication of $N/R$. For a fractional operation (fractional-N mode), the division is toggled between two values, in such a way that the average division ratio is the fractional factor for the desirable frequency. The frequency multiplication function is provided by:

$$F_{OUT} = F_{REF} \cdot \frac{N + K/F}{R}, \tag{4.1}$$

where $F$ is the system fractional resolution, and $K$ is the desired fractional channel. The toggling rate and pattern determines the amount of spurs produced at the output, appearing

as a undesirable frequency component. This can be somewhat overcome by the use of high order ΣΔ modulators [15, 16], which are capable of noise shaping, while reducing patterns that generate spurs.

The main issue of charge-pump based PLLs is their analog nature. The loop-filter specifications have to be carefully selected in order to fulfill a certain overall PLL specification, with very little flexibility for on-the-fly changes, such as, loop bandwidth optimization for locking time and/or minimum phase noise. Moreover, calibration is very difficult (between VCO and charge-pump gains, for example) and, due to the highly spurious output of the charge pump, the loop filter capacitor has to be very large, making it difficult to integrate in an advanced CMOS technology. Other analog parameters, such as MOS output resistance, also degrades in the nanoscale CMOS technologies, making the design of high performance charge-pump PLLs very challenging. Therefore, there has been a constant shift towards digital approaches during the last years, for most of modern applications.



### 4.2.2. ALL-DIGITAL PLL

In this section, the design of two ultra-compact ADPLLs is presented, which makes use of a phase prediction algorithm, as described next. This work has been published in [1]. The design was carried out in a 40 nm CMOS technology provided by TSMC. The two frequency synthesis modules provide wide tuning range of 2.4–3.8 GHz and 9.4-14.8 GHz, for the ring DCO (R-DCO) and a LC-tank DCO (LC-DCO), respectively, from a reference frequency ranging from 20 to 200 MHz. The block diagram is shown in Figure 4.3.

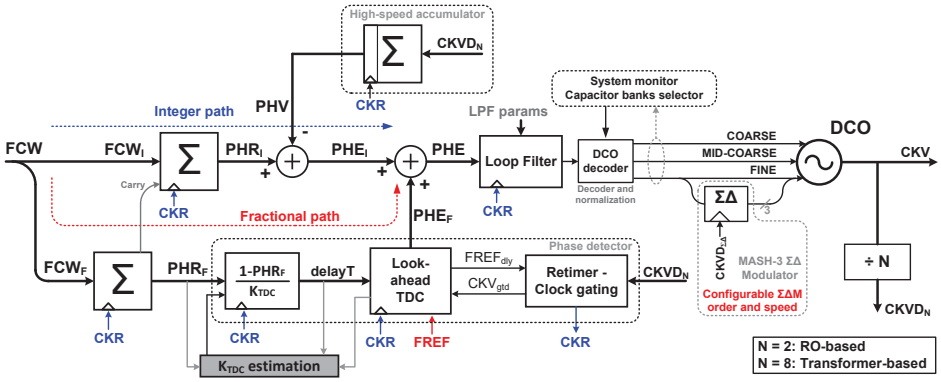



Figure 4.3: Block diagram of the accumulator-based, phase-prediction ADPLL.

#### LOOK-AHEAD TDC

Traditional phase-domain (i.e., counter-based) ADPLL implementations [17] are resistant to a deep power consumption reduction because the TDC of fine resolution has to cover at least one variable clock period, $T_V$. Solutions, such as clock-gating of the variable clock at the TDC, have been proposed [7, 18], however, none of them provides an optimal circuitry that would allow only the single necessary clock edge to pass to the TDC.

In this implementation, the deterministic nature of the phase error when the ADPLL is fully settled is taken advantage of to modify the traditional ADPLL architecture. Indeed,

it has been shown in [19] that for every frequency reference (FREF) clock cycle, assuming locked type-II loop (both in frequency and phase lock), the deterministic time difference between the rising edge of FREF clock and the next rising edge of feedback clock (CKV) is given by:

$$\Delta_t = (1 - \mathrm{PHR_F}) \cdot T_V, \tag{4.2}$$

where, $\mathrm{PHR_F}$ is a fractional part of the accumulated frequency command word FCW = $T_R/T_V$, where $T_R$ is the period of FREF. In other words, FCW is the targeted ADPLL frequency multiplication ratio. Equation (4.2) suggests that each FREF rising edge can be delayed by a deterministic amount of time so that a delayed version of FREF is created, namely $\mathrm{FREF_{dly}}$, which is aligned (to within a small constant offset) to the next CKV rising edge. This predictive effect will be referred to as the look-ahead action.



The advantages of implementing the look-ahead architecture are numerous. First, the delay operation occurs at FREF rate, which is typically two orders of magnitude lower than the CKV rate. It should be stressed that, even when proper prediction occurs, there is always a non-deterministic component of the FREF-to-CKV delay that renders the use of a TDC to resolve the $\mathrm{FREF_{dly}}$-to-CKV residual delay necessary. Nevertheless, the TDC action is carried out by only a few delay elements. Most importantly, since $\mathrm{FREF_{dly}}$ and CKV are now aligned, $\mathrm{FREF_{dly}}$ can be used to clock-gate the TDC, allowing its operation at the FREF rate. Another key benefit of the look-ahead action is that retiming of FREF to create a digital clock (CKR) for the feedback loop, as in [17], is now a metastability-free operation and, therefore, no significant circuit-level effort and power consumption are required to resolve it. Instead, a conventional re-sampling of $\mathrm{FREF_{dly}}$ by a divided version of CKV suffices as the CKR generation mechanism.

Figure 4.4 shows the conceptual block diagram of the look-ahead TDC and its interconnections with the clock-gating and retiming circuitry, as well as the time diagram of all waveforms associated with the look-ahead action. The FREF signal is delayed within the look-ahead TDC to generate $\mathrm{FREF_{dly}}$, which is then used to generate CKR and a clock-gated version of the CKV, called $\mathrm{CKV_{gtd}}$. CKR is used as a *digital* global clock, while $\mathrm{CKV_{gtd}}$ (at the FREF rate) samples the TDC to resolve the residual error between $\mathrm{FREF_{dly}}$ and CKV. Unlike the TDCs in conventional ADPLL implementations [7], where the CKV is propagated through the inverter chain and sampled by FREF, in our case it is much more convenient to propagate $\mathrm{FREF_{dly}}$ instead and sample it with a gated version of CKV, operating at the reference frequency. As seen from the example of Figure 4.4, the output of the flip-flops can be converted to an integer number, by identifying the location of two consecutive identical logic values in the output bit stream. This integer number can be normalized to yield a representation of the fractional part of the phase error between FREF and CKV ($\mathrm{PHE_F}$) when the ADPLL is locked. In the example of Figure 4.4, the decoded output of the delay is 3, which corresponds to a delay of three inverters ($3 \cdot t_{inv}$).

A detailed schematic of the look-ahead TDC is shown in Figure 4.5. The look-ahead TDC is implemented as a chain of identical controllable delay cells that can be used either as delay elements – for the look-ahead action – or as sampling elements – to resolve the $\mathrm{FREF_{dly}}$-to-CKV time delay. Each delay cell consists of an inverter and a pair of set/reset transistors that can pull up or down the corresponding cell input node [20]. Additionally, a compact D flip-flop (DFF) optimized for a minimum input capacitance and small setup and hold times is placed at each intermediate node. The simulated typical delay of the generic

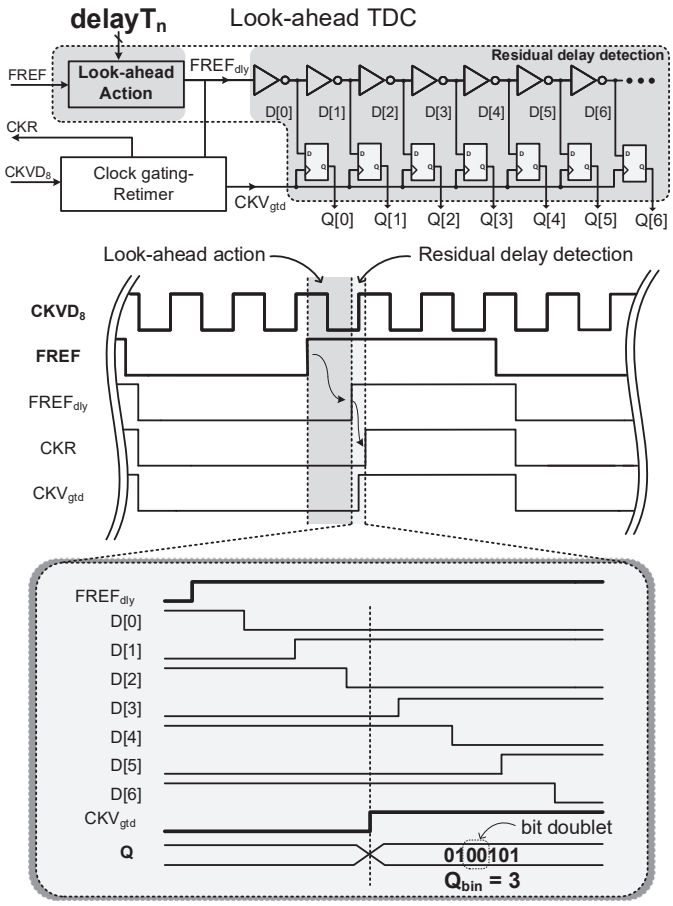



Figure 4.4: Look-ahead TDC block diagram with interconnection to clock-gating and retiming circuit along with all the signal waveforms.

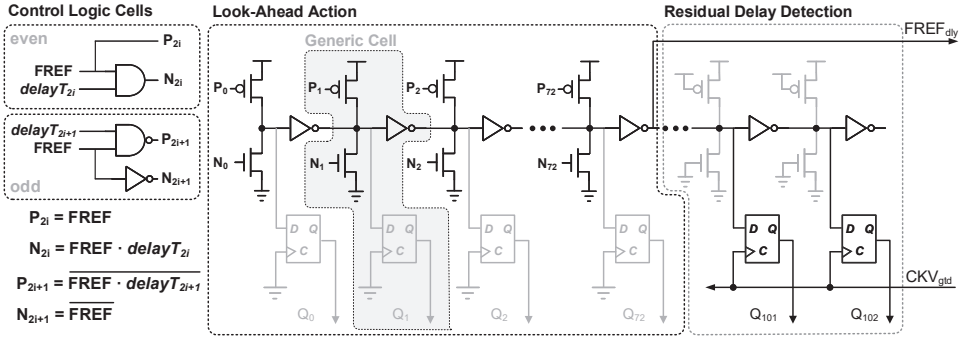



Figure 4.5: Look-ahead TDC schematic implemented with identical controllable delay cells.

cell is 15 ps while the DNL and INL values are 0.5 LSB and 1 LSB, respectively.

The cells located at the beginning of the inverter chain perform the look-ahead action, effectively acting as a digital-to-time converter (DTC). In this case, the DFFs act only as dummy loads (shown in gray in Figure 4.5) and the set-reset transistors are active. The intended functionality of the DTC part is the propagation of a single pulse through a desired number of inverter delays. Since the $\text{FREF}_{\text{dly}}$ output is fixed, the FREF input has to be dynamically selected every reference cycle, via the control of set/reset transistors. A logic control cell, shown in Figure 4.5, converts a thermometer-coded input into the control signals for the pMOS and the nMOS transistors, respectively.

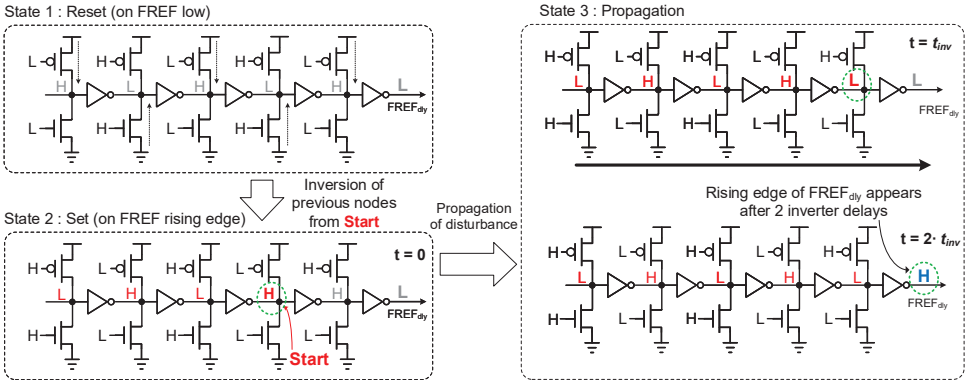



Figure 4.6: Transition of the look-ahead part of the TDC through the *reset*, *set* and *propagation* states, for the generation of a delay equal to two inverter delays.

An example of the look-ahead action of the TDC is illustrated in Figure 4.6, where a delay equal to two inverter delays is generated. The operating principle can be extended, without loss of generality, over any multiple of the inverter delays ($t_{inv}$). As shown in Figure 4.6, the look-ahead TDC goes through three distinct and consecutive states during every FREF cycle, namely, the *reset* state, the *set* state and the *propagation* state. The reset state occurs when FREF is low and sets the output $\text{FREF}_{\text{dly}}$ to a low steady-state, whereby the internal nodes of the look-ahead cells are set accordingly. In the *set* state, upon a rising FREF edge, a disturbance is generated at one specific internal node. The selected node changes progressively at every FREF edge (in a fractional-N operation). In this example, the disturbance starts two cells away from the output ($\text{FREF}_{\text{dly}}$). To achieve this, all nodes from *Start* backwards are inverted through the set-reset transistors, while the rest of the nodes, i.e., up to the end of the delay line, are set as floating by turning off their corresponding set-reset transistors. In fact, the disturbance manifests itself as two consecutive identical logic states, i.e., at the input and output of the same inverter. As a result, during the propagation state, the disturbance is propagated through the rest of the delay line and eventually enters the residual detection section, so the time difference between $\text{FREF}_{\text{dly}}$ to CKV can be resolved. At the same time, the $\text{FREF}_{\text{dly}}$ is used to clock-gate the CKV and for the CKR generation.

Knowing the cell delay $t_{inv}$, we can calculate the number of cells that the disturbance has to propagate through at each FREF cycle. Defining the gain of the look-ahead TDC as

$K_{TDC} \triangleq t_{inv}/T_V$ and combining it with (4.2), we obtain:

$$delay_{NR} = \frac{1 - PHR_F}{K_{TDC}}. \tag{4.3}$$

A pseudo-thermometer coding of $delay_{NR}$, as a number of the most significant zeros in a bit-stream of ones, is applied as a signal delay$T_n$ at each logic cell, as shown in Fig 4.5. Each logic cell needs to convert delay$T_n$ and FREF signals into the appropriate controls of the set-reset transistors. Based on the example of operation of Figure 4.6, a truth table for each signal $P_k$ and $N_k$ is constructed and logic functions as in Figure 4.5 deducted.

It should be mentioned that, apart from the controllable delay, there is a certain offset delay that is associated with the inversion of the nodes during the *set* state. Because all the nodes are inverted simultaneously, the offset delay can be considered constant, to a first-order approximation, irrespective of the number of the nodes that are inverted. As long as the offset remains constant, it plays no role in the alignment of the clocks. As highlighted in Figure 4.4, FREF is propagated through the chain of inverters while the $CKV_{gtd}$ samples the intermediate node values by means of the DFFs. The flip-flop vector output is decoded as the location of a doublet of high or low logical values and should be then normalized by $K_{TDC}$ to yield a representation of the fractional part of the FREF-to-CKV phase error ($PHE_F$).

With a single element delay of 15 ps, 64 elements are used to perform the look-ahead action in order to cover the worst-case delay of 830 ps (1.2 GHz feedback clock) and account for PVT variations. As far as the fractional phase error detection is concerned, this can be theoretically achieved by one element (equivalent of a bang-bang TDC). However, this could have an unpredictable impact on the settling time of the phase error, if no additional frequency settling loop is employed. In our implementation, an output word of the eight delay element FFs is read out, which is equivalent to a 3-bit TDC, to ensure fast settling on the order of microseconds.

It should be noted that the "next clock edge prediction" approach has already been widely used in previous ADPLL implementations. In [21], a divider-based ADPLL architecture with a bang-bang detector was implemented. However, it requires a secondary loop with a complex frequency acquisition to ensure the proper large-frequency step locking. In [22], an accumulator bang-bang phase detector is utilized instead of a small range TDC for fractional error detection. However, it might cause unpredictable or long frequency locking transients. In addition, no advantage is taken of the aligned nature of the $FREF_{dly}$ and CKV clocks resulting in a power-hungry sampler-based counter. Lastly, [23] implements separate DTC and TDC parts, an approach that is more prone to delay mismatches and requires different gain estimation blocks. In this implementation, a single delay element, embedded in the look-ahead TDC is used to ensure identical unit delays of the look-ahead action and the residual error detection. As a result, a single look-ahead TDC gain estimation block suffices for the estimation of the average delay of the elements. Furthermore, a dynamic element matching for the purpose of eliminating close-in fractional spurs can be straightforwardly implemented by employing a rotation of unit cells.

### DUAL-PATH DTC/TDC

As discussed in the previous section, one of the main issues with the current DTC/TDC implementations is their intrinsic non-linearity, which can generate fractional spurs when

arranged within a digital PLL, limiting their use for more stringent protocols of communication. As can be seen at an overview of different DTC/TDC topologies [24], typically only one of the signals, the reference or the variable clock, is modified (delayed) and compared to the other signal. Thus, due to the cyclic operation of the phase detector, the fixed pattern of non-linearity will appear as a tone distortion to the PLL output, generating the aforementioned fractional spur. A cyclic TDC, as a continuation of the work developed in the previous section, was proposed in [25], but yet to be validated in silicon. It connects the TDC elements in a circle, where there is no strictly defined input or output, thus, for the same desirable delay, different pairs of input/output could be used as interface, reducing the fixed pattern non-linearity.

A different approach, as an alternative to such operation, is proposed below. Instead of feeding only one signal to the DTC/TDC, both signals are connected to a well-defined input and collected at the output, forcing the signals to go through all stages all the time, independently from the desirable delay, as sketched in Figure 4.7.

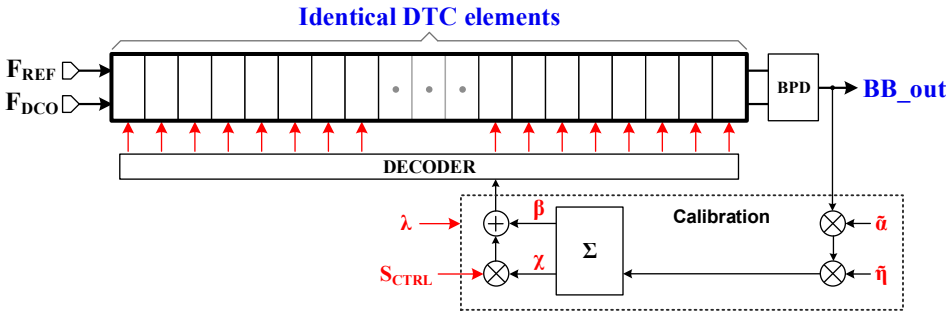



Figure 4.7: Proposed, dual-path DTC chain.

By feeding both signals through the whole chain, independently of the DTC code, any potential mismatch and/or noise, in one or more elements, affect both signals at the same time, and are, consecutively, canceled, minimizing the non-linearity. Each element contains a fast path and a slow path. The selection is done by the control bits ($S_M$), flipping individual DTC elements by a control bit, which can produce a $\pm\Delta_{LSB}$. By controlling the number of elements flipped, a positive or negative delta delay is applied to the input delay difference of $F_{REF}$ and $F_{DCO}$. The idea is to compensate for the input signal offset, by applying the complementary delay to each input path, in order to achieve an approximate alignment of the signals at the output of the DTC, in case the PLL is phase-locked. The output signals can then be compared in a phase detection, that can be a bang-bang phase detector (BBPD) [26] or a residue TDC.

The DTC consists of identical elements, whose resolution $\Delta_{LSB}$ is given by the delay difference between two paths, thus the length of the chain will be determined by the ratio between the desirable range (at least one variable period $T_{DCO}$) and the step size. The digital control word, $S_{CTRL}$ is defined by the accumulation of the fractional part of the frequency command word ($FCW_F$), which is then normalized by a least-mean-square (LMS)

algorithm in order to calibrate the DTC gain. The calibration is performed by:

$$\begin{aligned} \Delta_{DTC} &= (S_{CTRL} - M/2) \cdot \Delta_{LSB} \\ \Delta t &= -sgn\{\Delta_{in} + \Delta_{DTC}\} \quad \in \quad \{-1, +1\} \\ \tilde{\alpha} &= (S_{CRTL}[MSB] - 1) \cdot 2 \quad \in \quad \{-1, +1\} \\ \tilde{\eta} &= (FCW_F - 1) \cdot 2 \quad \in \quad \{-1, +1\} \\ \chi &= (1 - \lambda \sum (\tilde{\alpha} \cdot \tilde{\eta} \cdot \Delta t) \\ \beta &= M/2 \cdot \lambda \sum (\tilde{\alpha} \cdot \tilde{\eta} \cdot \Delta t) \end{aligned} \tag{4.4}$$

where $M$ is the number of DTC elements, $\Delta_{DTC}$ is the total delay produced by the DTC, $\Delta_{in}$ is the delay between the inputs, $\Delta t$ is the output delay, which is a binary $\pm 1$ value if a BBPD is used and the other variables as defined in Figure 4.7.

A sensible difference between a regular single-path TDC/DTC to this dual-path architecture is related to their transfer function. Since the single-path structures rely on the absolute delay added to a signal, it can be very sensitive to offsets variations and supply noise injection, requiring a very precise calibration system, in order to obtain a precise gain. For the dual path, on the other hand, the difference between the delays (between fast and slow paths) is de-sensitized by the total chain delay, rendering a much more robust structure. An illustration of such transfer functions are shown in Figure 4.8.

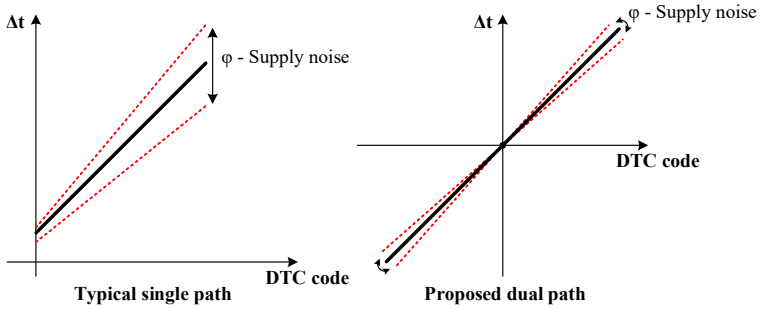



Figure 4.8: DTC transfer function: (a) single-path with errors in bias (DC level) and gain (inclination); (b) dual-path with errors in gain only.

There are many ways to implement the DTC element. Some options are shown in Figure 4.9. The straightforward approach is to use two MUXES, in both the inputs and the outputs (Figure 4.9 (a)), so no signal position inversion is performed, with impact on the maximum chain delay, which can limit the maximum reference frequency. Thus, a single flip can also be implemented (Figure 4.9 (b) and (c)), as long as the control is accounted for to consider the signal position inversion.

A simple control for the two types of cells can be implemented by a gray decoder of the control word ($S$), as shown in Figure 4.10, generating $C$. In two implementations are equivalent with respect to which cells are flipped. That is important, as it can be seen further in this section, to accommodate an eventual noise shaping technique.

The DTC chain can be re-drawn using variables to describe non-linearities and noise that real elements will most certainly have, as can be seen in Figure 4.11. Another important

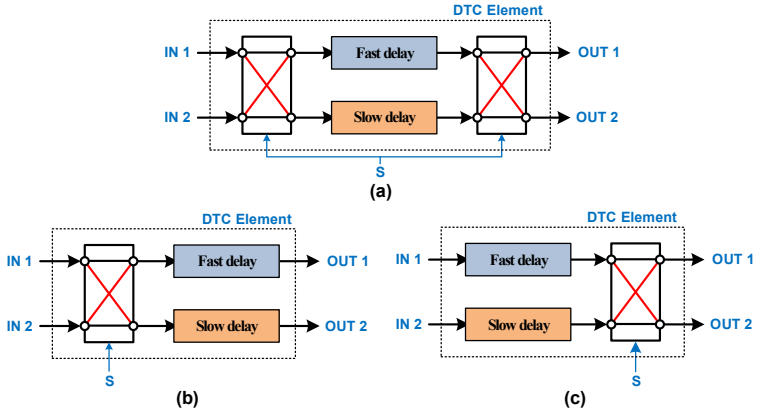



Figure 4.9: Dual-path DTC elements: (a) dual flip; (b) single flip, at input; (c) single flip, at output.

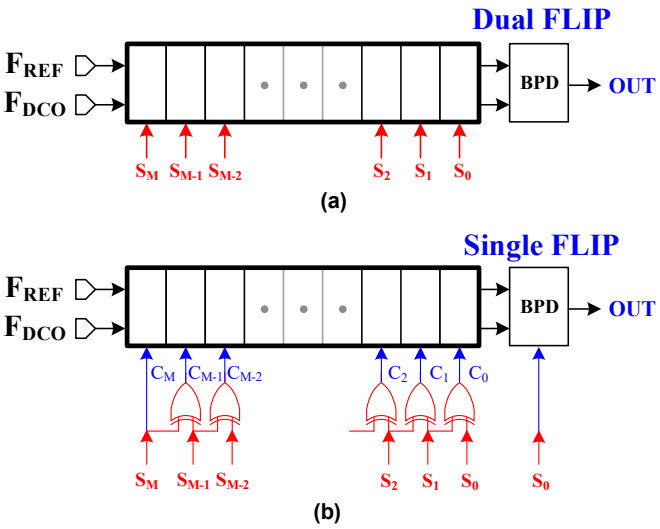



Figure 4.10: Alternative controls for equivalent operation of dual and single flip, dual-path DTC.

parameter of DTC/TDC is their sensitivity to supply voltage noise coupling. Since these elements operate synchronously with the reference frequency, it is common to experience large and short current draws from the supply, which can produce delay variations and noise injection, resulting in reference spurs on the PLL (although not very important, since the reference spur, from the phase detector, is filtered by the loop filter.)

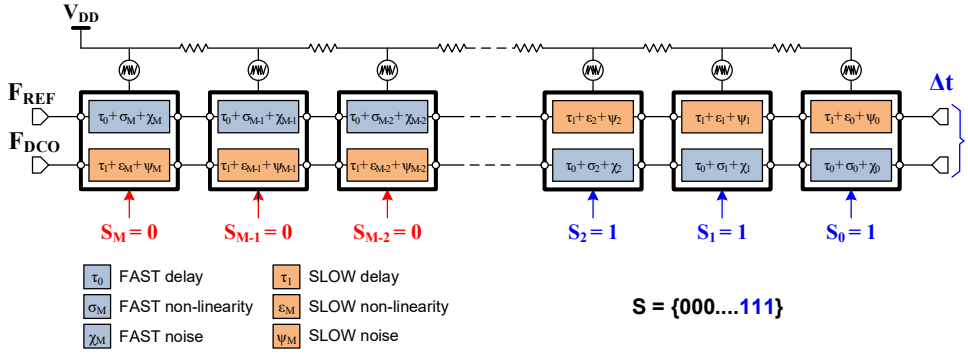



Figure 4.11: Dual-path DTC with delay modifiers to accommodate non-linearity and noise, for the fast and slow paths.

As the example of Figure 4.11 indicates, some cells are flipped, some are not. It is possible to write the total delay each signal will experience, assuming first that the control is linear (such as shown in Figure 4.11), although it is irrelevant which cells are flipped. For instance, if 10% of the cells are flipped, the results (time difference between the outputs, assuming both inputs are in phase) will be 10% of the total DTC range, independently of which cells are flipped. In fact, the operation of DTC is opposite: a code is predicted, based on the FCW accumulation, which is applied to the DTC in order to align the signals in the output, targeting the average $\Delta t \approx 0$. Thus, the delays for $F_{REF}$ and $F_{DCO}$ signals can be written as:

$$\begin{aligned} T_{REF} &= \sum_{i=code+1}^{M} \tau_0 + \sigma_i + \chi_i + \sum_{i=0}^{code} \tau_1 + \epsilon_i + \psi_i, \\ T_{DCO} &= \sum_{i=0}^{code} \tau_0 + \sigma_i + \chi_i + \sum_{i=code+1}^{M} \tau_1 + \epsilon_i + \psi_i, \end{aligned} \tag{4.5}$$

where $\tau_0$ and $\tau_1$ are the fast and slow DTC delays, $\sigma_i$ and $\epsilon_i$ are the non-linearity (and correlated noise) associated to the i-th fast and slow element, and $\chi_i$ and $\psi_i$ are the uncorrelated noise associated to the i-th fast and slow element, respectively. $M$ is the total number of elements. The final output delay is the difference between both paths, thus:

$$\begin{aligned} \Delta t &= T_{REF} - T_{DCO} \\ \Delta t &= (M - 2 \cdot code) \cdot (\tau_0 - \tau_1) + \sum_{i=code+1}^{M} \left[ (\sigma_i - \epsilon_i) + (\chi_i - \psi_i) \right] \\ &\quad - \sum_{i=0}^{code} \left[ (\sigma_i - \epsilon_i) - (\chi_i - \psi_i) \right]. \end{aligned} \tag{4.6}$$

A parameter to define the mismatch ratio between the different paths within each element can be used, one for the non-linearity ($\gamma_{Li} = \epsilon_i/\sigma_i$) and one for the noise ($\gamma_{Ni} = \chi_i/\psi_i$), respectively. Also, the mismatch ratio between the fast and slow paths can also be assumed constant throughout the chain, even though the absolute value might differ. Then, (4.6) becomes:

$$\begin{aligned}\Delta t = (M - 2\cdot code)\cdot(\tau_0 - \tau_1) + (1-\gamma_L)\left[\sum_{i=code+1}^{M}\sigma_i - \sum_{i=0}^{code}\sigma_i\right] \\ + (1-\gamma_N)\left[\sum_{i=code+1}^{M}\chi_i - \sum_{i=0}^{code}\chi_i\right].\end{aligned} \tag{4.7}$$

Equation (4.7) provides that, if the mismatch between fast and slow paths is kept small, the non-linearity and the noise is also suppressed. Figure 4.12 shows a simulation result when a maximum of 50% variation on $\sigma$, where the ratio $\gamma_L$ and $\gamma_N$ of 10% is introduced in the chain. The chain contains 128 elements and 5% noise variation on the inputs. Since all elements have the same global mismatch and the chain is controlled thermometically, the DNL appears as a linear variation, whereas the INL is accumulated to a peak of 1.7 LSB. If this DTC is directly implemented in a PLL, a very strong fractional spur would be expected.

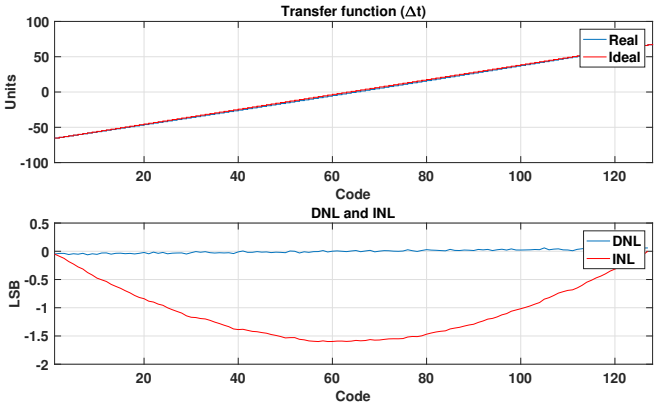



Figure 4.12: Transfer function simulation of 128 cells, with thermometric control, for $\gamma_L = \gamma_N = 0.9$, $\sigma = 0.5$

Since the chain is completely uniform, with identical elements, and the whole chain is used independently on the DTC code, by simply applying a scrambling code, the INL and DNL can reduced considerably, but most importantly, the fixed pattern can be reduced. The result is shown in Figure 4.13. Althoug scrambling is already helping with the operation of the DTC, more elaborated control (going directly on the decoder) can be implemented, taking advantage of noise shaping such as $\Sigma\Delta$ [27, 28]. In fact, the same techniques employed in DAC linearization and matching can be applied.

DTC/TDC structures are often very sensitive to supply variations, including noise coupling through the substrate. High frequency noise, in general, is not a major issue, since the

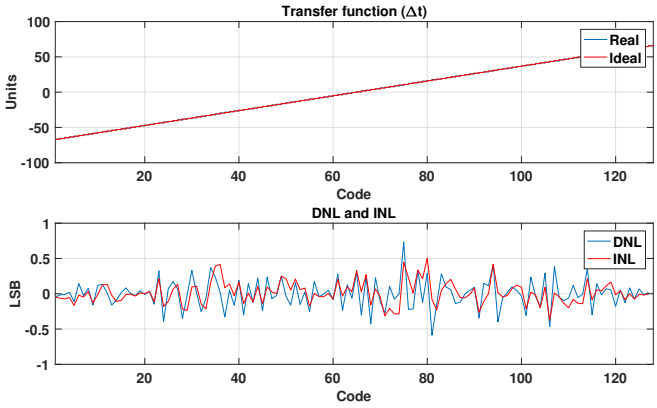



Figure 4.13: Transfer function simulation of 128 cells, with cells randomly selected, for $\gamma_L = \gamma_N = 0.9$, $\sigma = 0.5$



low-pass filtering behavior of the PLL, from the reference to the output, is capable to attenuate most of its components. However, strong leakage from the reference can still appear at the PLL output, requiring a large loop capacitor (in case of a charge-pump PLL) or higher order digital filter. One of the advantages of the proposed dual-path DTC chain is the high rejection to supply noise, since the differential observation of both signals attenuates the absolute delay variations caused by the supply. A simulation in which it was added noise components at different frequencies, at the power supply, through a RLC network shown in Figure 4.14 (a), and a 128 dual flip DTC elements (Figure 4.14 (b)) was performed.

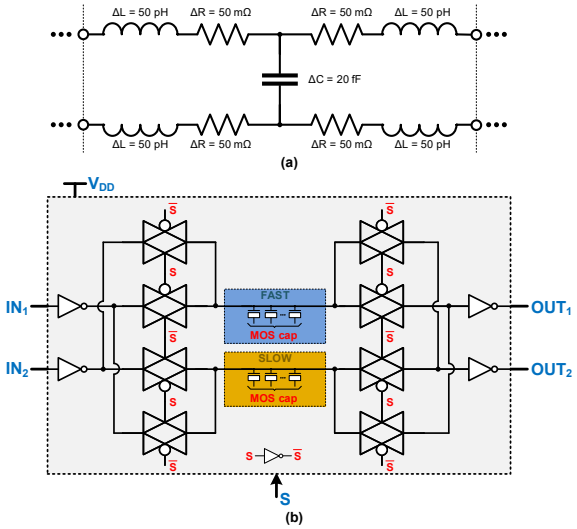



Figure 4.14: Supply noise simulation; (a) Distributed supply network; (b) dual flip DTC element.

Figure 4.15 (a) shows the absolute delay variation for both paths, for noise tones at 1, 2,

46, and 50 MHz. In all cases, except at 50 MHz (the input frequency is also 50 MHz, which produces a natural rejection of in-phase noise), the absolute delay variation is in the order of 110 ps, which is 8% of the total DTC coverage (target at 2 ns range). This high sensitivity would potentially produce a very high in-band phase noise, requiring large LDO, filters, and separated supply for the DTC, increasing power consumption, area, and complexity. The differential delay variation, on the other hand, is only 1.6% of the absolute delay. It is shown in Figure 4.15 (b), producing only 0.12% variation of the total DTC coverage, without any filter on the supply. It is possible to conclude that, even without elaborate supply management, the dual-path DTC is robust to supply noise, enabling ultra-low jitter PLL implementations.



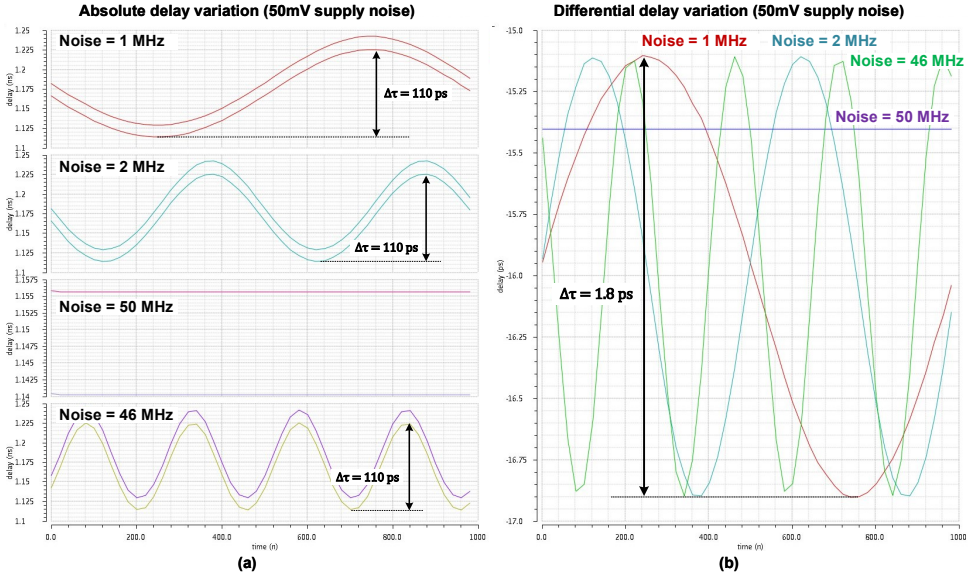



Figure 4.15: Delay variation under supply noise of 50mV in different tone frequencies; (a) absolute delay; (b) differential delay.

A system simulation was also performed. Using the model from Figure 4.3 (replacing the look-ahead TDC with the proposed DTC), in Verilog and Verilog-AMS, with the DTC modeled with Verilog-A based on the DTC element of Figure 4.14 (b), including an edge-selection for the variable clock, all necessary calibrations, etc. As previously mentioned, the selection of the DTC elements can be performed in various ways. The simplest way is to select the elements to flip in a thermometric way, which produces a fixed-pattern that translates the DTC non-linearity into fractional spurs in the PLL. The second, easiest way, would be randomly selecting which elements to flip, based on the control word, which scrambles the non-linearity into noise. Other techniques are also possible, including noise shaping [27, 28].

Figure 4.15 shows the phase profile of the modeled PLL, operating in a fractional channel at 10.000390625 GHz (FCW = 200 + 1/128), in different cases. First, in black, a reference phase noise is plotted, when there is no mismatch between the DTC elements, thus

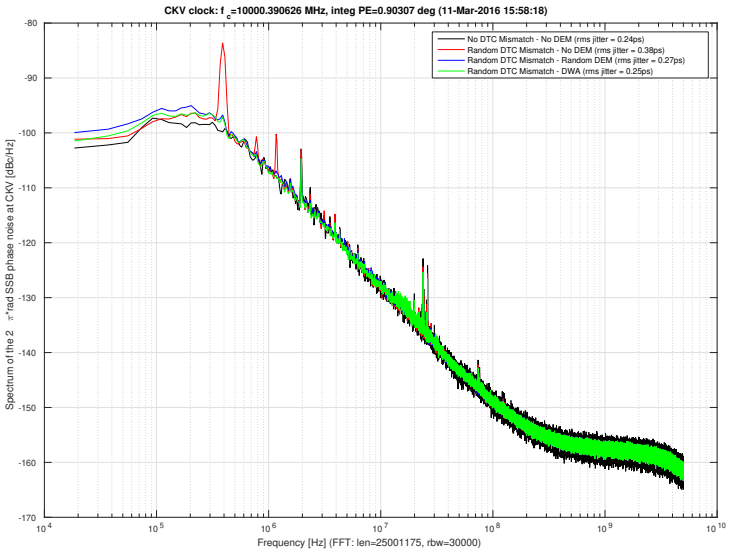



Figure 4.16: System simulation for a perfectly linear DTC, and with 10% random mismatch between elements, for thermometric selection, as well as using two simple DEM techniques.

containing only quantization noise. In red, a random 10% mismatch is added to the DTC elements; by controlling them without any dynamic element matching (DEM) technique, where a spur can be seen at 390 kHz (1/128 fractional channel), which is not filtered by the loop. With random selections of the elements, the spur is scrambled and a higher in-band phase noise is observed. Another simple DEM technique is applied, making use of data weight averaging (DWA), which also reduced the spur, while moving the noise to higher frequencies that were filtered by the loop. The integrated RMS jitter is also shown, with one of the simplest DEM techniques (DWA), only 10 fs is added to the integrated jitter of perfectly matched DTC (250 fs against 240 fs). Other more elaborated DEM techniques can also be used, improving further the DTC operation, for even lower jitter PLLs.

The main drawback of the proposed architecture is that, although the absolute delay of each element is not important for the DTC operation, its value will influence the maximum reference frequency the system can operate. As it is well-known, the reference frequency plays an important role in the total jitter of the PLL, thus for ultra-low jitter and mm-wave PLLs it if important to have faster reference frequencies (150–300 MHz). If, for example, $M = 128$ elements and each element has 40 ps absolute delay, the maximum reference frequency that the system can operate is 200 MHz. In order to reduce this constraint, the DTC can be implemented using a segmented approach, with identical elements for coarse, mid-coarse and fine resolution. A block diagram is shown in Figure 4.17.

In this approach, the DTC is split into three segments, but it could be as well split into 2 or more. The operation is the same as the single segment, with the difference on the calibration and coverage. The finer resolution should cover more than 2 LSBs of the

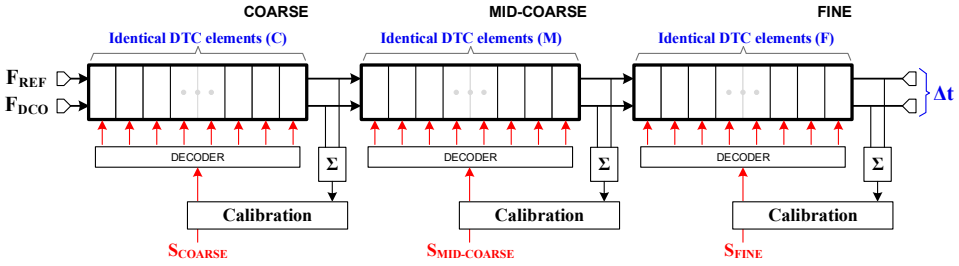



Figure 4.17: Proposed segmented dual-path DTC chain.



previous segment, in order to guarantee proper coverage over PVT. Its operation is more complex, since the gains of different segments need to be calibrated in parallel, but the operation frequency can be pushed to gigahertz range, if desirable.

Regarding the phase detector, it was assumed first a BB-PD due to its simplicity. However, it is possible to implement a fine resolution TDC to obtain a finer quantization of the output, speeding up the dynamics of the loop. There are many topologies for fine resolution, short range TDCs, where the most suitable would be a Vernier-line [10].

### 4.2.3. DIGITALLY-CONTROLLED RING OSCILLATOR – RO-DCO

The implemented RO is a 3-stage current-starved topology shown in Figure 4.18. The frequency tuning is performed exclusively by digital control words, with very coarse steps (“band selection") provided by switched current sources, and finer frequency steps by single-ended switched capacitors. The capacitor bank is divided between 4-bit binary-weighted coarse, a 30-bit unit-weighted mid-coarse and a 15-bit unit-weighted fine banks. Also, a 3-bit unit-weighted bank for 2nd-order MASH ΣΔ dithering is implemented to enhance the frequency resolution.

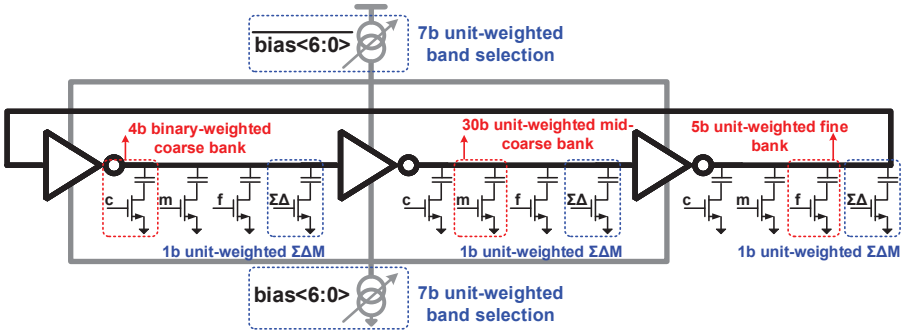



Figure 4.18: 3-stage current-starving fully digitally controlled ring oscillator (DCRO).

To ensure the circuit’s symmetry and balance, thus keeping the output load symmetric, consequently lowering the $1/f^3$ PN corner, the coarse and mid-coarse banks are switched at

the same time at all three DCO stages. For the fine bank and the ΣΔ dithering capacitors, the control is applied in a thermometer manner to only one of the DCO stages at a time so finer resolution could be achieved with monotonic frequency steps. All capacitors are based on a unit cell, with an nMOS switch and a MOM capacitor that are combined in groups according to the desired bank capacitance. Moreover, a single-ended topology was chosen, since it provides a better FoM when compared to its counterpart (pseudo-) differential topology.

The complete RO is packed in a square of 120x120 $\mu m^2$, the same as the transformer-based DCO. The relatively large area of the RO is due to accounting for the decoupling capacitors, which occupy 40% of the whole area (approximately 4 pF as a combination of MOS and MOM capacitors), and the ΣΔ modulator.

### 4.2.4. ULTRA-COMPACT TRANSFORMER-BASED OSCILLATOR – LC-DCO



Efficiently scaling down an inductive element requires multiple optimizations to deliver the salient features of an RO (i.e., wide tuning range and small area) while keeping high power efficiency (i.e., better PN with less power) [29]. The goal is to pack a sufficient inductance into a small area, without drastically degrading the Q-factor. Moreover, parasitic capacitance of the inductor and of its accompanying $g_m$ stage transistors should be kept low for a reasonable SRF, so that the desired tuning range can be achieved. At the same time, the stringent metal density requirements of advanced CMOS must be fulfilled.

Electromagnetic coupling between the inductive structure and its surroundings is another point of concern, specially in SoC environments. A way to relax the inductor sensitivity is to use a quadrupole, as in [30, 31]. It has been demonstrated that the electromagnetic coupling of a quadrupole is much lower than that of a single inductor, allowing a more compact overall design. It is pertinent to notice the superior advantage of a 4-lobe quadrupole [30], which is able to minimize the magnetic field in both symmetric axis, in comparison to the 2-lobe, which is only able to do so in one axis [30, 31]. However, even at the maximum coupling for the 2-lobe, it provides a 16 dB lower magnetic coupling than that of a single spiral [30].

For our proposed split-transformer oscillator, a 2-lobe quadrupole was used, but in a different arrangement and driving configuration. Based on the results of this work, another version was implemented in 10 nm FinFET technology [32]. In the next section, a more thorough analysis is performed and conclusions are drawn.

#### ELECTROMAGNETIC FIELD CANCELLATION

The large size of high-Q inductors inevitably makes them very sensitive to their surroundings, as they act like antennas. By either picking up noise or inducing currents in nearby circuits, these inductors could potentially lead to various operational issues, such as frequency pulling of two or more close-by oscillators, noise induction in analog circuits, etc., thereby requiring special countermeasures. Maintaining the inductor isolation and space between the circuits would be expensive due to extra silicon and not always permitted due to the stringent metal density rules.

In literature, solutions are proposed [33, 34] to deal with strong magnetic fields, such as 8-shape inductors. However, they are bulky and thus not very suitable for low-area implementations. On the other hand, transformers can additionally benefit from field cancellation while, at the same time, provide passive voltage gain between drains and gates of the cross-

coupled pair of $g_m$ devices, in order to alleviate any startup issues associated with the use of small devices as required for low parasitic capacitance.

In our proposed split topology, shown in Figure 4.19 (a), the magnetic fields ($\vec{B}$) generated by the coils are in opposite direction to each other (when driven differentially). To quantify this interaction, the magnetic coupling factor $k_m$ between the transformer and a (probing) single coil was analyzed. This approach emulates the current induction caused by the transformer in nearby circuits, tested at distance $d$ and direction ($\theta$) of 45°.

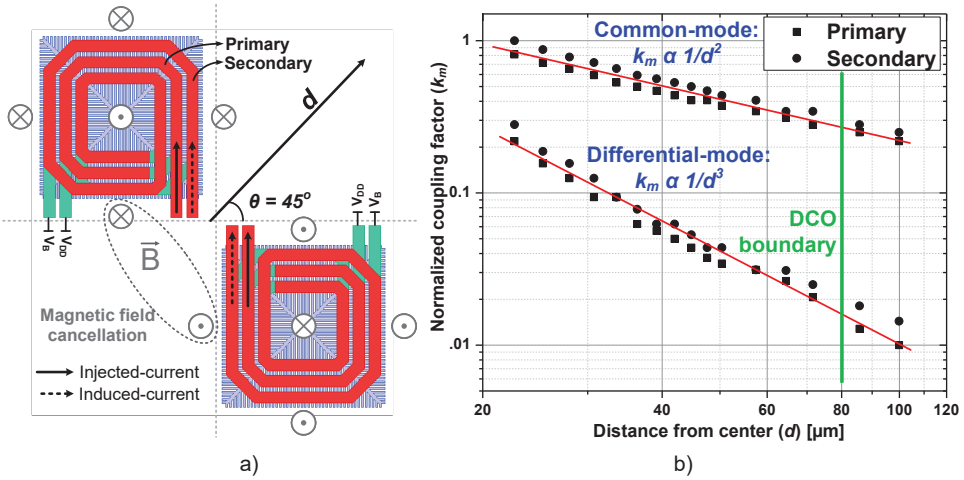



Figure 4.19: Magnetic field cancellation: a) Magnetic field directions; b) Simulation of coupling factor ($k_m$) for common-mode and differential mode excitations.

Figure 4.19 (b) shows the normalized $k_m$ under common-mode and differential-mode excitations. The terminology used here is related to the injected current into the coils; i.e., in the common-mode, the injected currents in both coils have the same phase, generating similar magnetic fields, while in the differential-mode, the phases of the injected currents are 180° apart, generating opposite magnetic fields. In a typical single-inductor solution, only one magnetic field is generated, so it can be related to the common-mode excitation, even though the coil itself is excited differentially. The efficiency of the magnetic field cancellation can be shown firstly by the magnitude of $k_m$, which is 75% smaller for the differential-mode when compared to the common-mode, and the slope, $1/d^2$ and $1/d^3$, for the common-mode and differential-mode, respectively, according to the theory of dipoles [35].

The electric and magnetic fields can also be evaluated by plotting the magnitude of finite-element method (FEM) 3D EM simulations under common-mode and differential-mode, as shown in Figure 4.20. Both the electric and magnetic fields undergo strong cancellations in the direction ($\theta$) of 45°.

The simulations presented in Figure 4.19 & 4.20 indicate the benefit of exciting the structure in the differential-mode rather than in the common-mode (which would be the case of a single inductor as well), where the near-field is beneficially canceled. Moreover, our proposed structure is similar to an 8-shape inductor (with respect to the generated EM

fields), where the common-mode magnetic field is rejected and the differential-mode field vanishes for far-field observation (rejection of coupling to nearby signals).

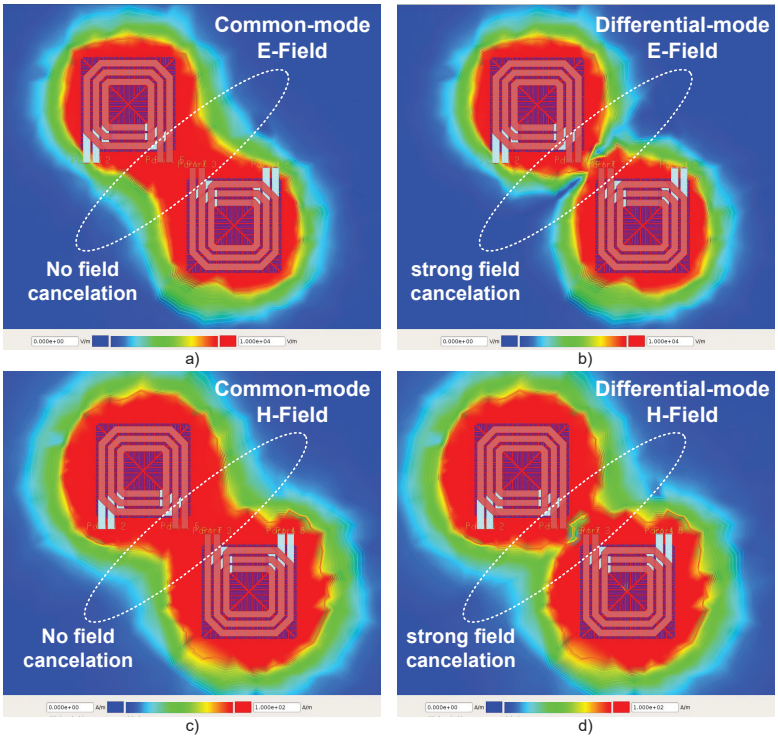



Figure 4.20: FEM Simulation: a) E-field common-mode; b) E-Field differential-mode; c) H-field in common-mode; and d) H-Field in differential-mode.

Thus, a transformer-based LC cross-coupled topology which enjoys a freedom to low-pass filter the gate bias voltage $V_B$ of the active devices is proposed. This is to obtain a very low sensitivity of frequency pushing by minimizing gate-source capacitance, $C_{GS}$, modulation due to the gate-source voltage, $V_{GS}$. The proposed transformer-based DCO is shown in Figure 4.21. The transformer is composed of two independent multi-turn single-ended transformers, using top-layer metal conductors (thickness 0.85$\mu$m), in a digital 40 nm CMOS technology without ultra-thick metals, while satisfying all restricted metal density design rule check (DRC) requirements that cannot be waived in advanced CMOS. The two independent transformer units are placed symmetrically to the center of the DCO, in order to obtain magnetic field cancellation.

The transformer is fully custom-designed (see Figure 4.22 for more details) including pattern-ground shield in poly and all six thin metals (at the center of the coils) following the same pattern as the poly ground shield. It was simulated using the method of moments. Each coil has a winding width of 2.9 $\mu$m and spacing of 1.15 $\mu$m, where the outer and inner diameters are 38.9 $\mu$m and 16.9 $\mu$m, respectively. The $V_{DD}$ and GND connections are done in Alucap. The transformer has a coupling coefficient $k_m$ = 0.7 between the 350 pH

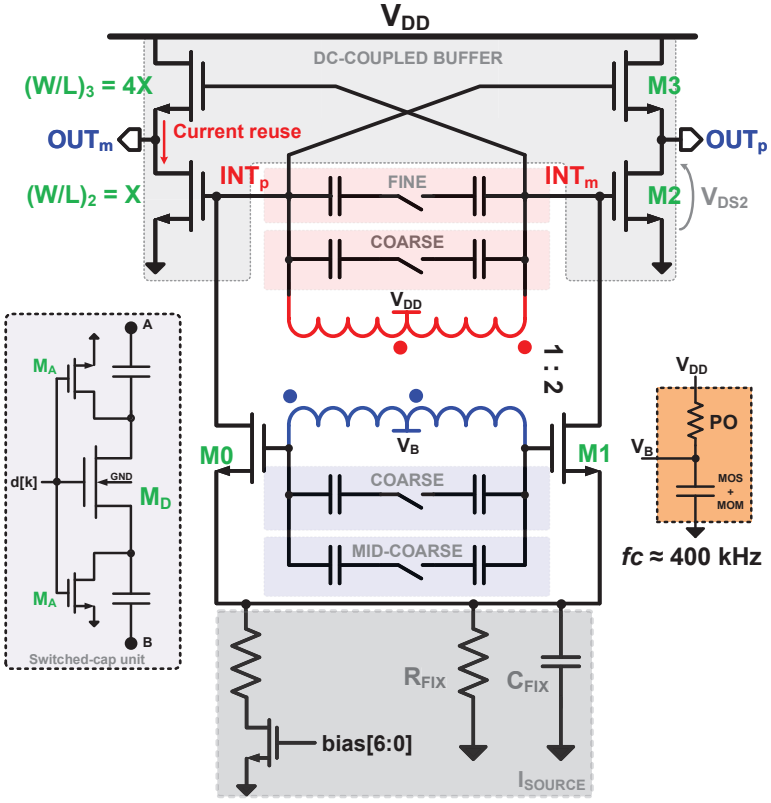



Figure 4.21: Simplified ultra-compact transformer-based DCO core.

primary and 1 nH secondary, peak quality factor of $Q = 8$ around 13 GHz and self-resonance frequency (SRF) at 50 GHz.

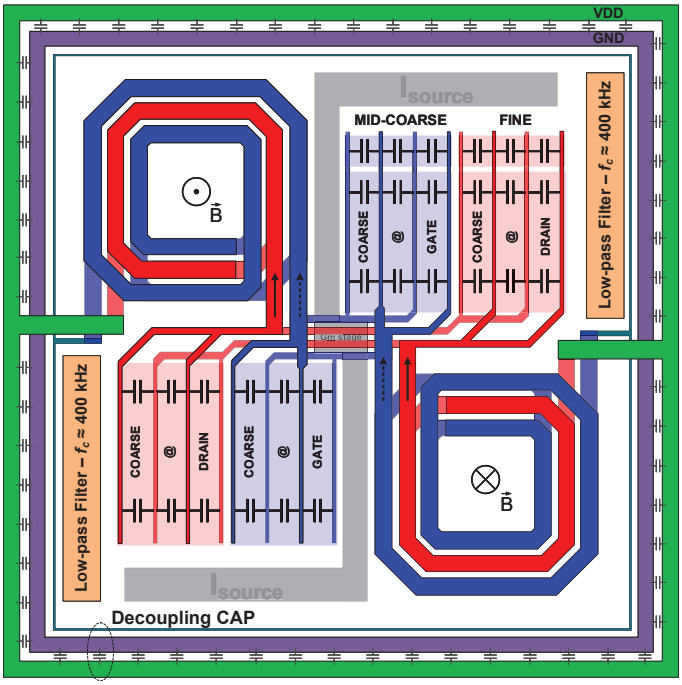



Figure 4.22: Details on the layout of the DCO.

The capacitor banks are divided between the transformer's primary and secondary. The coarse banks (6-bit binary-weighted) are switched simultaneously, enhancing the overall Q-factor of the transformer over individual inductors [36]. Mid-coarse and fine banks are both 14-bit unit-weighted, but the effective capacitive weight of the former is $n^2$ (= 4 times) larger than the latter's, since the mid-coarse is connected only at the secondary and the fine bank is connected only at the primary. The slight asymmetry caused by that does not degrade the Q-factor of the whole tank. Moreover, it can provide the required frequency range overlap as well as fine resolution.

In order to improve the effective frequency resolution, a $2^{\text{nd}}$-order MASH $\Sigma\Delta$ dithering is applied to three unit-weighted bits of the fine bank. It uses a divided version of the DCO output frequency ($\div 32$ or $\div 16$) to modulate capacitance of these three bits, thus effectively obtaining fractions of the minimum capacitance and, consequently, finer frequency resolution.

The switched-capacitor units were designed using the topology shown in Figure 4.21. It is a differential metal-oxide-metal (MOM) capacitor with a main differential-mode switch, assisted by two common-mode auxiliary switches. The main nMOS switch ($M_D$ in Figure 4.21) turns the capacitor on and off, while two smaller auxiliary nMOS transistors ($M_A$) provide a weaker dc path to ground for the source and drain of the main switch. Note that even in the off-state, the tiny leakage current of the auxiliary transistors ensures a high

impedance path to ground, thus avoiding risky forward biasing of the junction diodes of $M_D$. The capacitor bank design is very critical, especially the connection between the switch and the capacitors, since excessive parasitic capacitance in these lines, due to cross-coupling, would affect the on/off state capacitance ratio. To accomplish the desired tuning range, the $C_{ON}/C_{OFF}$ ratio was design to be around 3, with Q-factor of 14 and 140 for the on- and off-state, respectively.

For a more coherent analysis, the figure-of-merit (FoM) [37] should be examined. It takes into account the oscillator free-running phase noise (PN), power consumption ($P_{DC}$) and operating frequency ($f_0$). It is widely used and conveniently reproduced here as:

$$\text{FoM} = |\text{PN}| \; + \; 20 \cdot \log_{10}\left(\frac{f_0}{\Delta f}\right) - 10 \cdot \log_{10}\left(\frac{P_{DC}}{1mW}\right) \tag{4.8}$$

An extension of the FoM is expressed by $\text{FoM}_T$, which includes also the oscillator tuning range, and is defined as:

$$\text{FoM}_T = \text{FoM} + 20 \cdot \log_{10}\left(\frac{TR[\%]}{10}\right) \tag{4.9}$$

The FoM and $\text{FoM}_T$ of the transformer-based DCO are 175 dB and 188 dB, respectively. Figure 4.23 depicts the measured $\text{FoM}_T$ along with the occupied chip area and compares it with compact LC oscillators and ROs from literature. The $\text{FoM}_T$ of the proposed transformer-based DCO is at least 20 dB better than other RO's of comparable size. The performance is still improved even when compared to advanced phase noise cancellation techniques applied in ROs [38]. As seen in Figure 4.23, the proposed DCO occupies comparable area to an RO while retaining an $\text{FoM}_T$ equivalent to LC oscillators.

Measurement results confirm a high accuracy of the design methodology. Center frequency, frequency step, power consumption and phase noise were measured within 10% of the simulation predictions. This also indicates the importance of having an accurate metal/oxide stack profile during the design process.

The transformer-based oscillator was designed to operate between 10–16 GHz with FoM of 176 dB and $\text{FoM}_T$ of 189.3 dB but due to a slightly higher power consumption and a narrower tuning range (5.4 GHz instead of 6 GHz – 10% lower), 1 dB lower FoM and $\text{FoM}_T$ were measured. This pre-silicon accuracy appears quite remarkable, especially given the tiny size of the tank, where any extra parasitic capacitance can produce large frequency variations.

The Q-factor of the LC-tank (i.e., the transformer and switched capacitor banks) stays relatively constant at around 6 over the tuning range. The open-loop PN at 10.9 GHz is plotted in Figure 4.24 and corresponds to the mid-point of the control tuning word. Figure 4.25 demonstrates the continuous tuning range coverage of the transformer-based DCO. Sufficient overlap over the different banks (coarse, mid-coarse and fine) guarantees the proper ADPLL locking sequence. The coarse bank is binary-weighted for easier implementation, while the mid-coarse and fine banks are switched in a thermometer way, guarantying monotonicity and tracking of voltage and temperature variations.

### 4.2.5. DC-COUPLED BUFFER

Besides the DCO optimization for the required PN and power consumption performance, another important concern is the immediate DCO output buffer. A non-linearity of the

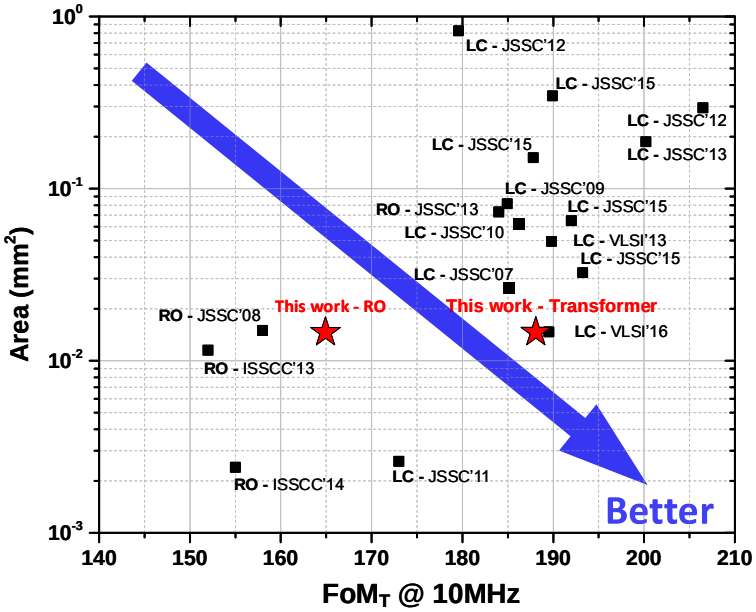



Figure 4.23: $FoM_T$ over area for stand-alone, state-of-the-art oscillators.

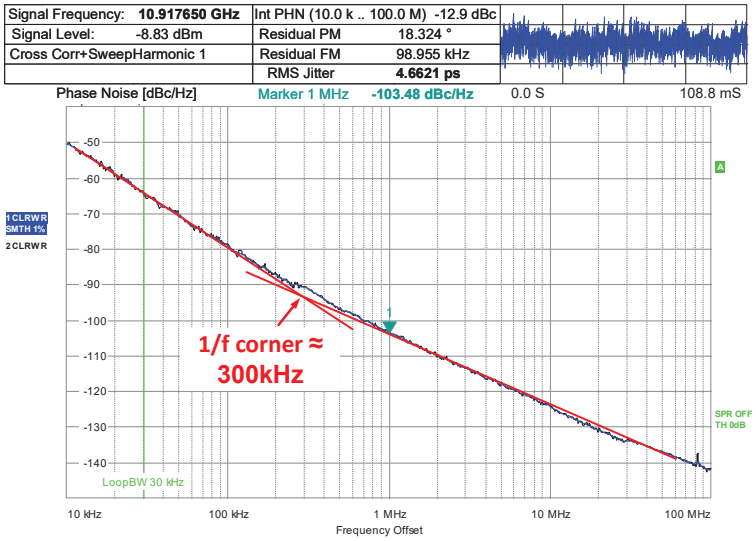



Figure 4.24: Transformer-based DCO phase-noise.

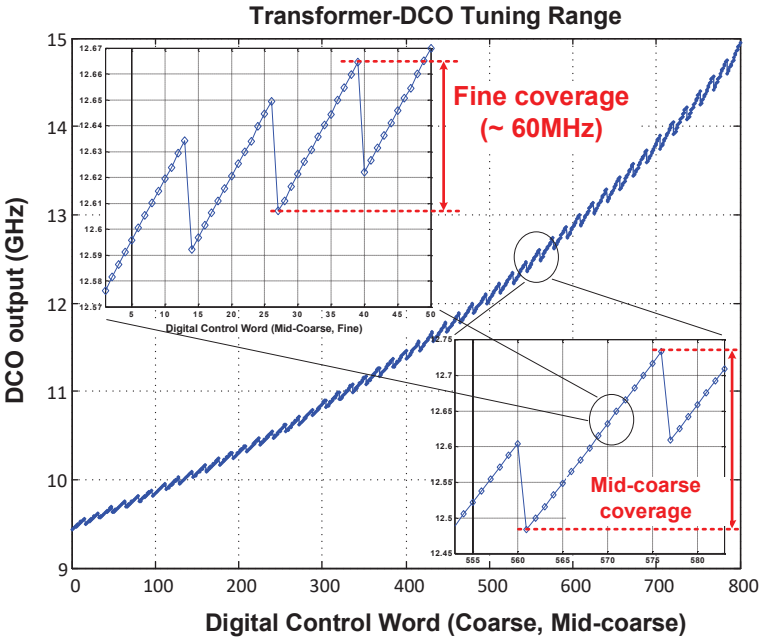



Figure 4.25: Transformer-based DCO frequency sweep over coarse, mid-coarse and fine tuning banks.

driven load (including the buffer's non-linearity itself) and a supply voltage disturbance could degrade the PN and, consequently, reduce the oscillator power efficiency. Also, the incessant technology node shrink requires voltage supply reduction, while the transistor threshold voltage ($V_{th}$) is kept roughly the same, thus requiring new buffer topologies to overcome these issues.

Most of the practical high-frequency buffers are connected to the DCO through dc blockers (i.e., ac-coupling capacitors) [5, 36], allowing the buffer bias voltage to be set locally. This helps to alleviate effects from the statistical process variation, especially pMOS and nMOS mismatches. However, these dc blockers add extra load and area to the oscillator tank and, depending on the frequency, they could be prohibitively large. Moreover, thermal noise of the shunt resistor (generally used for self-biasing) is easily coupled back to the oscillator and then up-converted. Some buffers, however, allow direct dc-coupling to the oscillator. The best example is a source follower, which features a wideband frequency response, but offers a voltage gain often well below unity. In order to increase its power efficiency, a combined source follower and common-source topology is proposed. Its schematic is shown in Figure 4.21.

The buffer is thus dc-coupled to the DCO while sharing the same $V_{DD}$ supply. It uses only nMOS devices to reduce capacitive loading, noise, and process mismatches. From Figure 4.26 (a), we can see that $V_{GS3}$ is kept always constant and equal to $(V_{DD} - V_{DS2})$, which is chosen to be below the threshold voltage, $V_{th}$. In this way, $M_3$ operates in weak inversion and $M_2$, due to a velocity saturation, operates in strong inversion, since both share

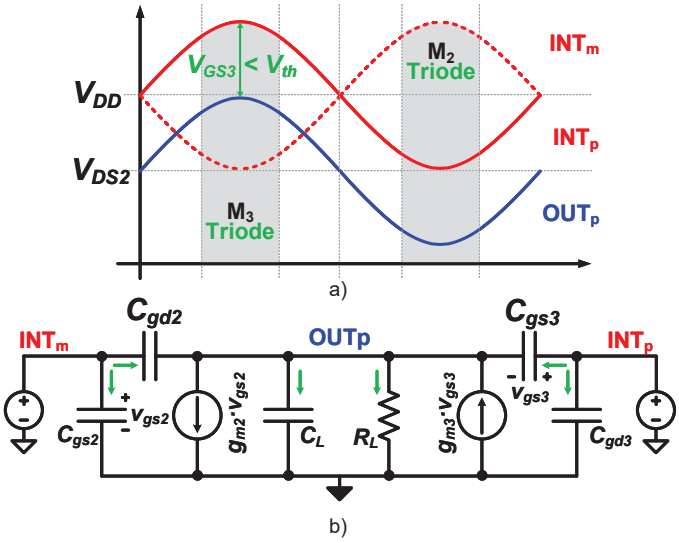



Figure 4.26: DC-coupled low-voltage DCO output buffer. a) Half-circuit large-signal excursions; and b) Half-circuit small-signal simplified model.

the same current and the former is 4x larger than the later. For a short interval of the oscillating period (around 90° and 270° of the cycle), however, either one of the transistors goes into the triode region. Nevertheless, the overall performance of the buffer is not affected since the other transistor is providing an ac gain to the corresponding output. Also, due to a relatively small voltage swing (in our case 250 $mV_p$), this linear region is reached only for a brief angle duration. Therefore, for this analysis, the circuit can still be treated with a small-signal model.

Figure 4.26 (b) shows such a simplified small-signal model of the left-half of the circuit. The current reuse is represented by the addition of $g_{m2}$ to the gain, and the architecture provides a compensation for the gate-source capacitance of $M_3$ ($C_{gs3}$), contributing to an overall voltage gain enhancement of 20%, in our case, when compared to a simple source follower. The voltage gain enhancement, however, depends on the driven load, where the differential overall gain is given by:

$$A_v = \frac{g_{m2} + g_{m3} + s(C_{gs3} - C_{gd2})}{g_{m3} + 1/Z_L + s(C_{gs3} - C_{gd2})} \tag{4.10}$$

where, $Z_L$ is the output load impedance and includes the output dynamic impedance of the transistors.

The overall transformer-based DCO is packed in a square of 120x120 $\mu m^2$, and includes the transformer, capacitor banks, active core, output buffer and decoupling capacitors. One important remark is that, nowadays, process technology has very stringent manufacturing rules that have to be followed. In the past, metal density over larger inductors could be waived at the designers responsibility, however, in modern advanced processes, one side of the die might affect the other and foundries are reluctant to allow it. This situation proves

challenging for the design of high-Q inductors, since they depend on the metal voidness around them to achieve high performance. Therefore, one advantage of keeping the inductor (or transformer in this case) small is that these metal density requirements are easier to fulfill. Another advantage is that the magnetic field is kept mostly around its windings, which contributes to lower interference on its surroundings and, finally, our proposed split transformer architecture reduces even more the far-field through field cancellation, isolating the DCO from the environment.

### 4.2.6. TOP LEVEL

The aforementioned oscillators (i.e., RO and transformer-based) are integrated into two ADPLLs, sharing a common architecture. Thanks to the introduction of a "look-ahead" time-to-digital converter (TDC) as the fractional phase error detector, the ADPLLs feature low power consumption. Both loops operate with a feedback frequency ranging from 1.2 to 2 GHz, coming either from the RO (divided by 2) or the transformer-based DCO (divided by 8), thus keeping the PLL loop identical. The ADPLL operation and design are detailed in this section.

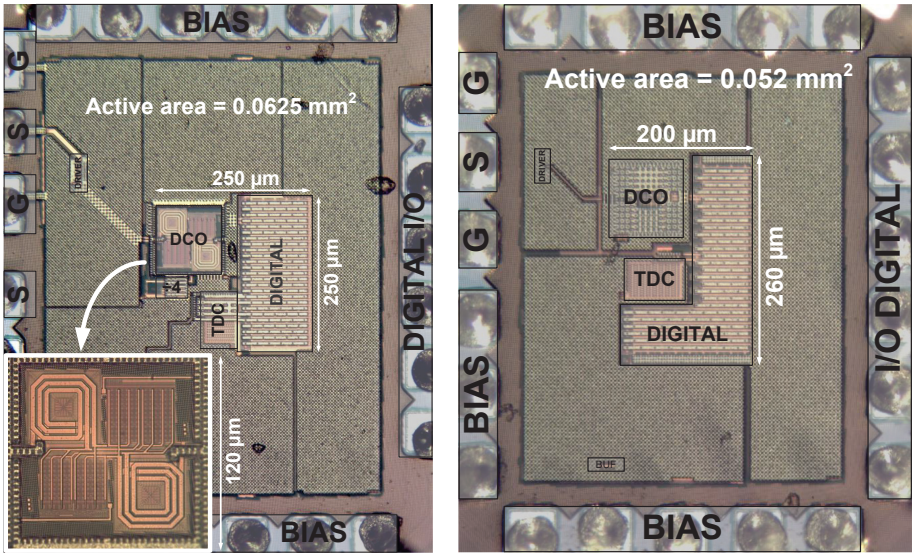
Figure 4.3 shows the block diagram of the ADPLL. The frequency command word (FCW) is split into its integer and fractional parts, with separate reference accumulators that generate the integer and fractional part of the reference phase, $PHR_I$ and $PHR_F$, respectively. In order to properly accumulate the FCW as a whole, a carry-out is transferred to the integer accumulator whenever an overflow of the fractional part occurs. A synchronous 8-bit counter serves as the variable accumulator and produces the variable phase PHV which is subtracted from $PHR_I$ to provide the integer part of the phase error $PHE_I$. $PHR_F$ is used to calculate the TDC delay code, according to (4.3), which is, in turn, applied to the look-ahead TDC, through a gain. A TDC gain estimation block, based on an iterative adaptation algorithm, is implemented on-chip to dynamically track delay estimation errors due to PVT variations [40]. The digitized output of the TDC represents the fractional part of the phase error, $PHE_F$ that is combined with $PHE_I$ to yield the total fixed-point representation of the phase error, PHE.

The phase error PHE needs to be filtered, in order to properly set the loop dynamics. A reconfigurable proportional-integral controller is followed by a DCO decoder to form the oscillator tuning word (OTW). The DCO decoder design varies between the two ADPLLs due to the different capacitor bank configuration of the two oscillators. Both DCOs include switched capacitor banks that are dithered using a $2^{nd}$-order MASH $\Sigma\Delta$ modulator in order to achieve a finer equivalent frequency resolution and to push the quantization noise into higher frequency offsets, where they are more easily filtered out and do not contribute significantly to the total jitter [41]. The operation frequency of the $\Sigma\Delta$ modulators can be dynamically selected from different taps of the divider chain in order to meet the required performance as a trade-off between power consumption and jitter.

For the feasibility of the variable accumulator implementation, the feedback path was chosen to operate at a maximum 2.5 GHz, which means that a divide-by-2 version of the RO output and a divide-by-8 version of the transformer-based DCO output is fed back to the variable accumulator and the look-ahead TDC. Division by 2 in the RO-based ADPLL is achieved by a CMOS digital divider and for the division by 8 in the transformer-based ADPLL, a CML $\div 4$ divider is cascaded with a CMOS digital divider. These dividers are

represented in Figure 4.3 by the block [÷N]. Since in both ADPLLs the loop feedback operates on a divided version of the output, the effective frequency command word has to be adjusted accordingly. Therefore, 1/2 of the multiplication ratio is accumulated at the RO-based ADPLL, and 1/8 of it for the transformer-based ADPLL.

As mentioned above, the clock-retimer gating circuit generates the important clock signals for the ADPLL: The CKR clock is used as a global digital clock of the ADPLL loop (at the reference clock rate), to resample the output of the variable accumulator and to generate a gated version of the variable feedback clock, $CKV_{gtd}$.




(a) (b)

Figure 4.27: Micrograph of ADPLLs : (a) Transformer-based ADPLL chip micrograph; (b) Ring DCO-based ADPLL chip micrograph.

Figure 4.27 (a) shows the micrograph of the proposed transformer-based ADPLL fabricated in 40 nm TSMC LP CMOS technology, with an active area of 0.0625 $mm^2$, where the DCO alone occupies 120x120$\mu m^2$. For a comparison, Figure 4.27 (b) shows the die micrograph of the RO-based ADPLL, in the same technology. The RO-based synthesizer occupies an area of 0.052 $mm^2$, which is only 20% smaller than the transformer-based ADPLL, with both DCOs occupying roughly the same area.

Both ADPLLs operate at a regular 1.1-V supply, while the transformer-based DCO operates at a 1-V supply, in order to optimize its FoM and to allow operating in the lower frequency span. Both ADPLLs can support a wide range of reference frequencies (20 MHz–200 MHz), but for the following results, crystals of 100 MHz and 156.25 MHz are used as references, for the transformer-based and RO-based ADPLLs, respectively. Both support the fractional-N operation, using identical feedback loops (look-ahead TDC and divider-by-2), with an exception of the extra divider-by-4 (CML) for the transformer-based configuration. Figure 4.28 plots the phase noise (PN) and spectrum of the transformer-based

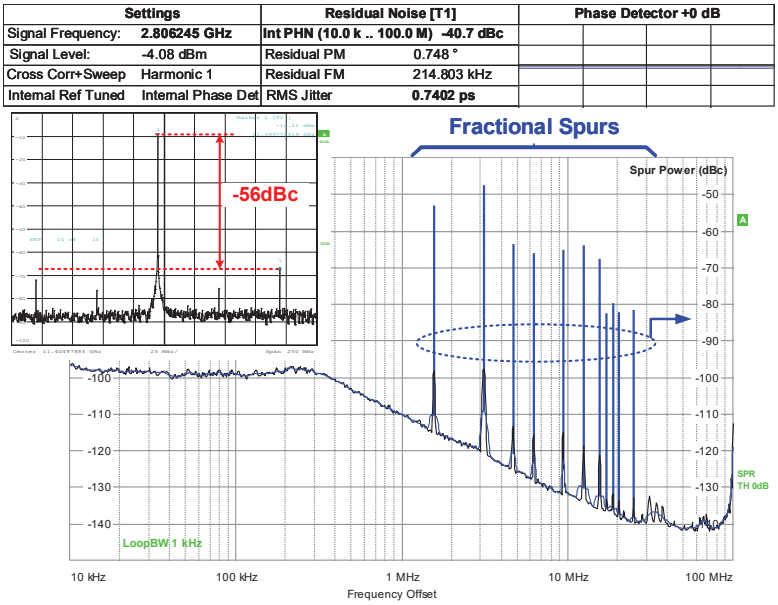



Figure 4.28: Phase noise and spectrum closed-loop of transformer-based ADPLL.

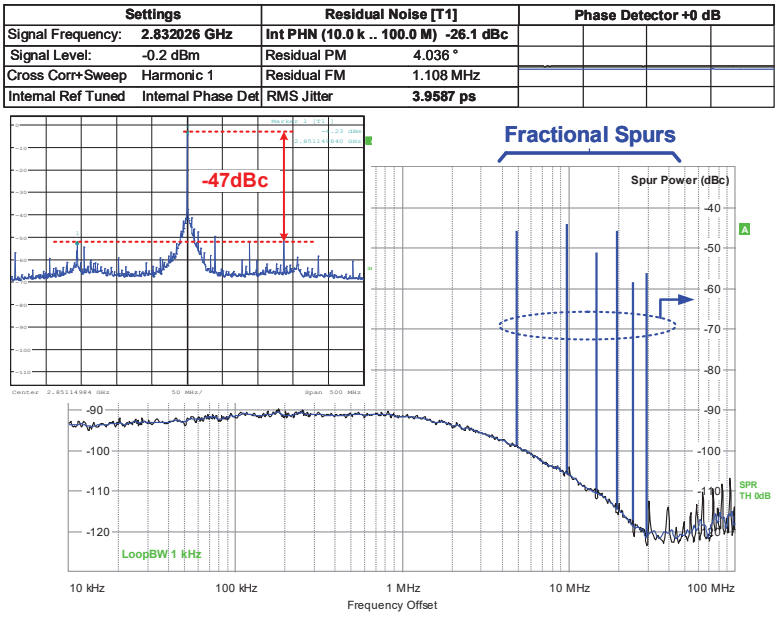



Figure 4.29: Phase noise and spectrum closed-loop of RO-based ADPLL.

ADPLL, with highlighted spurs and after division-by-4, to relax the measurement buffers. In the inset, the spectrum is also shown and the reference spur could be inferred. For comparison, the phase noise and spectrum of the RO-based ADPLL are plotted in Figure 4.29. The fractional FCW for those cases were set to 14.03125 and 9.0625, which correspond to 112.25 and 18.125 for the transformer-based and RO-based ADPLL, respectively, since the feedback loop effectively operates at CKV/8 and CKV/2.

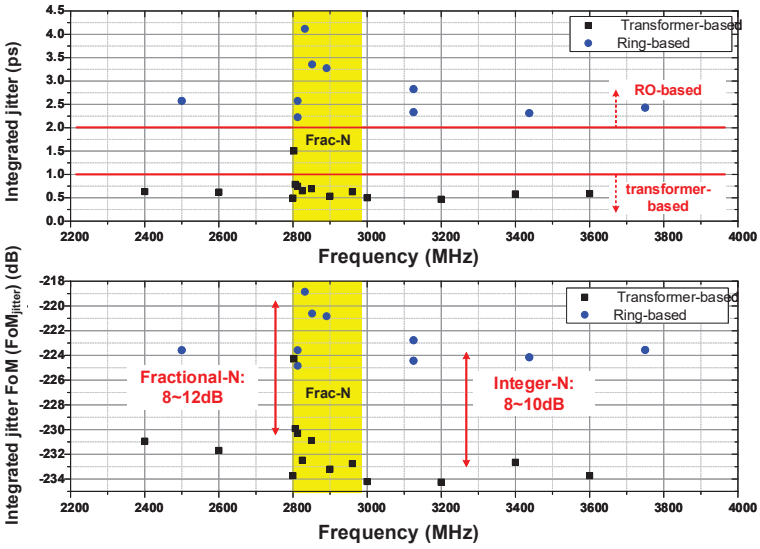



Figure 4.30: Integrated RMS jitter and $\text{FoM}_{\text{jitter}}$ comparison for RO (raw CKV) and transformer-based (CKV/4).

The above measurements were repeated at various FCW values (both in integer-N and fractional-N). A plot of the integrated RMS jitter and integrated FoM jitter ($\text{FoM}_{\text{jitter}}$) is shown in Figure 4.30. The $\text{FoM}_{\text{jitter}}$ characterizes the frequency synthesizers in terms of jitter-power trade-off, which has been introduced by [42], as the product of jitter variance $\sigma_t^2$ and the power consumption in mW, defined as:

$$\text{FoM}_{\text{jitter}} = 20 \cdot \log_{10}\left(\frac{\sigma_t}{1s}\right) + 10 \cdot \log_{10}\left(\frac{P_{DC}}{1\text{mW}}\right) \tag{4.11}$$

A quick inspection of Figure 4.30 reveals a significant performance improvement of the proposed transformer-based ADPLL over the traditional RO-based ADPLL: 8 dB better $\text{FoM}_{\text{jitter}}$ for integer-N channels and 12 dB better for fractional-N channels.

The worst-case reference spur was measured at −56 dBc and −47 dBc for the transformer- and RO-based ADPLL, respectively. Since the dominant fractional spurs are caused by the TDC nonlinearity, they experience a regular low-pass filtering by the ADPLL loop filter. However, the fractional spurs falling within the loop bandwidth (e.g., in case of a very small fractional FCW setting) cannot be attenuated so the two ADPLLs report the worst-case in-band fractional spur of -35 dBc. When not operating at such very small fractional FCW values, the maximum integrated jitter (from 10 kHz to 100 MHz) was measured at

0.74 $ps_{rms}$ and 4 $ps_{rms}$ for the transformer- and RO-based ADPLL, respectively. However, when the in-band fractional spurs are present, the maximum integrated jitter increases to 1.5 $ps_{rms}$ for the transformer-based ADPLL.

Table 4.1: State-of-the-art comparison table for both analog and digital RO-based frequency synthesizers.

| | **This Work** | Kao [43] ISSCC'13 | Marucci [44] ISSCC'14 | Tierno [45] JSSC'08 | Nand. [46] JSSC'15 | Tsai [47] ISSCC'15 | Elkholy [48] JSSC'16 |
|---|---|---|---|---|---|---|---|
| Technology [nm] | 40 | 40 | 65 | 65 | 65 | 16 | 65 |
| Architecture | Dig-PLL | Ana-PLL | MDLL | Dig-PLL | Ana-PLL | Dig-PLL | Dig-PLL |
| **Area [mm$^2$]** | **0.052** | **0.055** | **0.4** | **0.03** | **0.48** | **0.029** | **0.084** |
| Output freq. [GHz] | 2.4-3.8 | 1.9-2 | 1.6-1.9 | 0.5-8 | 4.25-4.75 | 0.25-4.0 | 2.0-5.5 |
| Tuning range [%] | 45 | 5.7 | 17 | 66 | 11 | 67 | 67 |
| Reference [MHz] | 20-200* | 26 | 50 | 125-500 | 50 | 50-200 | 50 |
| Loop BW [MHz] | 0.7-10 | 2 | N/A | 1.25-5 | 12 | 2 | 5 |
| Integ. RMS jitter [ps] | 2.3 \| 4 | 3.4 | 1.4 | 0.7[4] | 1.5 | 1.22 \| 3.48 | 1.9 \| 3.6 |
| Power consump. [mW] | 6.5-8.5 | 9.95 | 3 | 17.2 | 11.6 | 3.9-9.3 | 1.35-4 |
| Supply Voltage [V] | 1.1 | 2.5 | 1.2 | 0.5-1.3 | 1.0 | 0.52-0.8 | 0.7-0.9 |
| $FoM_{jitter}$ [dB] | **-220 \| -218** | **-219** | **-232** | **-231** | **-225.8** | **-228 \| -223** | **-229 \| -228** |
| Reference spur [dBc] | -47 | N/A | -47 | N/A | -60 | N/A | -44 |
| Worst fract. spur [dBc] | -35+ | -50 | -47 | N/A | -50 | -31.2 | -41.6 |
| **Freq. pushing [MHz/V]** | **3200 (100%/V)** | **N/A** | **N/A** | **8000 (100%/V)** | **N/A** | **N/A** | **N/A** |

* Results using 156.25 MHz crystal. + In-band spur.

Table 4.2: State-of-the-art comparison table for both analog and digital LC-based frequency synthesizers.

| | **This Work** | Raczk. [49] JSSC'15 | Ahmadi [50] VLSI'13 | Venerus [51] JSSC'15 | Lee [52] JSSC'15 | Elkholy[53] JSSC'15 | Li [32] VLSI'16 |
|---|---|---|---|---|---|---|---|
| Technology [nm] | 40 | 28 | 40 | 65 | 28 | 65 | 10 |
| Architecture | Dig-PLL | Ana-PLL | Ana-PLL | Dig-PLL | Ana-PLL | Dig-PLL | Dig-PLL |
| **Area [mm$^2$]** | **0.0625** | **1** | **0.39** | **0.56** | **0.07** | **0.22** | **0.034** |
| Output freq. [GHz] | 9.4-14.8 | 9.2-12.7 | 8-12.4 | 2.8-3.5 | 2.7-4.5 / 4-7 | 4.4-5.2 | 10.8-19.3 |
| Tuning range [%] | 45 | 32 | 43 | 22 | 50-54 | 16.7 | 56 |
| Reference [MHz] | 20-200* | 40 | 156.25 | 26 | 54 | 50 | 150 |
| Loop BW [MHz] | 0.7-8 | 1.8 | 0.5-4.3 | 0.04 | 0.35 | 0.75-3 | 2 |
| Integ. RMS jitter [ps] | 0.5 \| 0.74 | 0.23 \| 0.28 | 0.29 \| 0.46 | N/A | 1.0 | 0.45 \| 0.5 | 0.725 |
| Power consump. [mW] | 12-20 | 13 | 16.9 | 21 | 14 | 3.7 | 11.9 |
| Supply Voltage [V] | 1.0 / 1.1 | 0.9 / 1.8 | 1.0 | 1.0 / 1.2 | 1.8 | 1.0 | 0.8 |
| PN @ 10 MHz [dB] | -120 | -132 | -123 | -143 | -122 | -130 | -120 |
| FoM @ 10 MHz [dB] | 175 | 181 | 176 | 184 | 168 | 183 | 174 |
| $FoM_T$ @ 10 MHz [dB] | 188 | 192 | 189 | 190 | 182 | 187 | 189 |
| $FoM_{jitter}$ [dB] | **-234 \| -230** | **-242 \| -240** | **-238** | **N/A** | **-228** | **-240** | **-232** |
| Reference spur [dBc] | -56 | N/A | N/A | -82 | N/A | -69 | -74 |
| Worst fract. spur [dBc] | -35+ | -43 | -57 | -43 | N/A | -51.5 | -30 |
| **Freq. pushing [MHz/V]** | **80 (0.8%/V)** | **200 (1.8%/V)** | **N/A** | **N/A** | **N/A** | **N/A** | **250 (1.7%/V)** |

* Results using 100 MHz crystal. + In-band spur.

A comparison of the $FoM_{jitter}$ shows that our RO-based ADPLL is the best in its class and our transformer-based ADPLL provides an additional 11 dB improvement, being comparable in performance to similar-area LC PLLs [32, 52] and only 8–10 dB worse $FoM_{jitter}$ than the best-in-class, but of large-area, wireless (narrow-band) LC PLLs [49, 50]. Moreover, important parameters, such as frequency pushing (not universally reported), which can be translated as frequency sensitivity to its supply, is intrinsically superior in LC tank DCOs (and also in our case) than in any RO-based. A high frequency pushing would normally require massive filtering (i.e., large silicon area of LDOs) to compensate for it, thus reducing the area advantage [45]. Figure 4.31 shows the measured frequency pushing of both circuits over frequency. The measured frequency pushing of the transformer-based DCO was 80 MHz/V (0.8%/V), which is far more robust than the RO-based, found to be around 3.2 GHz/V (100%/V), being only acceptable if a state-of-the-art LDO is used to supply it [54], which can provide maximum of -54 dB PSRR (at 100 kHz) with area penalty.



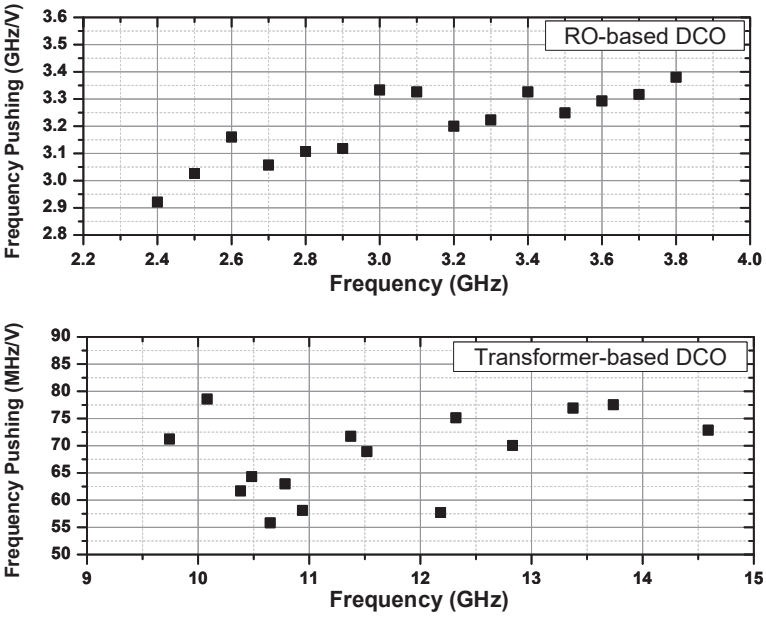



Figure 4.31: DCO frequency pushing comparison of RO (top) and transformer-based (bottom).

The $FoM_{jitter}$ performance of the proposed transformer-based ADPLL is compared in Figure 4.32 to recent state-of-the-art fractional-N synthesizers. It reports the smallest area among all PLLs (analog or digital alike and wide or narrow tuning range) and a very good $FoM_{jitter}$ (<-230 dB). Thus, the proposed miniaturization process proves to be very efficient, with a relatively small impact on $FoM_{jitter}$ when compared to high-end PLLs.

Table 4.1 provides a comparison between state-of-the-art RO-based frequency synthesizers. Serving simply as a reference, this RO-based PLL offers similar jitter performance as [43] and similar area, with much larger tuning range and lower supply voltage. This implementation provides a much smaller area than [44] due to the fully digital approach,

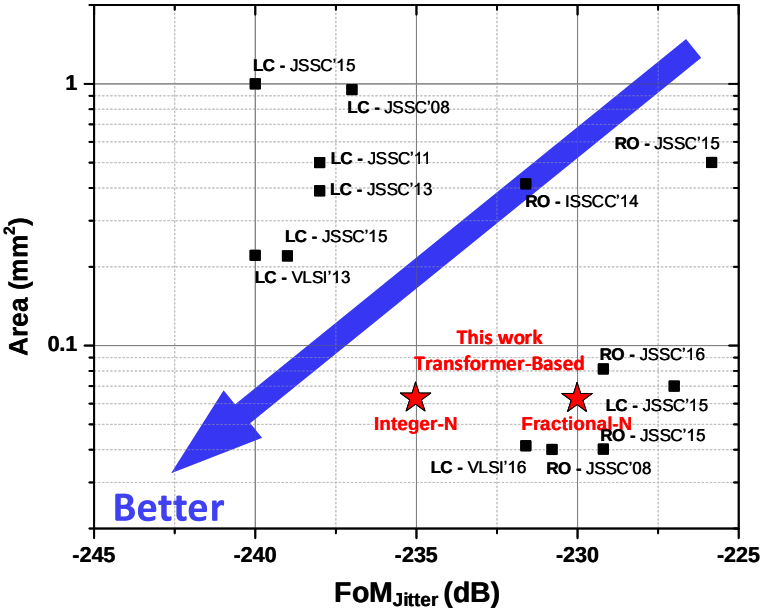



Figure 4.32: $FoM_{jitter}$ over area for recent state-of-the-art fractional-N PLL.

in contrast to the use of DACs in [44]. In [45], a more compact ADPLL with a better jitter performance is presented, yet it is implemented in SOI technology and can only provide integer-N channels along with a fixed number of programmable frequency steps.

Table 4.2 shows the performance comparison between state-of-the-art LC-based frequency synthesizers. Our proposed solution is the smallest, except for [52] which occupies almost the same area. Our solution has moderate jitter performance (in general 10 dB worse than high-end solutions), since it was compromised while trading for the area.

## 4.3. DISTRIBUTED, MUTUALLY COUPLED RING OSCILLATORS

PLLs and DLLs are the most common and robust way to provide a precise timing reference on-chip. As seen in this chapter, and throughout the literature for many years, the powerful negative feedback control plant can be very flexible and accurate, however, PLL/DLLs are bulky, which is, for imaging system, a prohibitive bottleneck. Digital counterparts somewhat relax this constraint by replacing the analog loop filter with a digital one, but yet are not small enough to be used multiple times in a single sensor, where the detector's sensitive area must be maximized. Depending on the sensor topology, such as the ones found in column-wise converters [3, 58, 59] and per-pixel TDCs [12], a single PLL can then be used to generate a precise frequency, as reference, and their phases distributed to local interpolative TDCs. However, this approach either limits the maximum conversion rate, per pixel, or it requires excessive high power consumption for the phases distribution [12].

Two exceptions for these assumptions are sensors based on line detectors, which are used in line scanning LiDARs [59], and SiPM-based detectors, for 2-axis scanning LiDAR

or photon-starved TCSPC applications [60, 61]. In both cases, effectively the number of pixels is small and its usability requires more complex setups, such as the scanning itself. One of the main reasons dTOF image sensors are generally small in size [12, 59] is due to their limitation on providing uniform and precise timing information throughout the sensor, while accounting for variable and, potentially, excessive power consumption, which can drastically impact on IR-drop. It is then essential to provide a solution that can offer frequency/phase synchronization throughout the sensor, whilst occupying a very small area.

Inspired by high-speed clock distribution [62–64] in microprocessors and network-on-chip (NoC) [65], a solution capable of generating a seamless timing reference is proposed and discussed in the next sections. Two different arrangements, (1D and 2D) are shown and measurement results presented. But before that, the core assumption for this approach is that the TDC array must operate continuously, which allow a more uniform and constant power consumption. Although it reduces the effects of resolution variation with sensor activity, an analysis on power consumption and sensitivity reduction must be made, in comparison with other methods.



### 4.3.1. ARRAY OF TDCS

Apart from providing a power efficient timing reference throughout the array, it is essential for the sensor to maintain a well-known and stable resolution, independently of mismatches and PVT variations. The main drawback of event-driven architectures is their dependency on the sensor activity, where power consumption varies with incoming light, which determines how often the TDCs are operating. In these conditions, it is typically difficult to predict the sensor behavior and a constant foreground calibration is required. In laboratory conditions, the sensor calibration can be relatively easy, through the use of an equidistant target, while maintaining a constant temperature and activity rate. In real applications, this if typically not the case and the problem is exacerbated.

By operating the TDCs continuously, the overall power consumption is kept constant, so is the IR-drop, allowing a more predictable resolution. The problem of excessive power consumption such configuration can bring is relaxed by sharing each TDC with several pixels (how many will depend on the system).

The proposed approach exploits the availability of continuously running oscillators by operating them mutually coupled, through a single phase, in a process of injection-locking at the fundamental frequency. When combined, the oscillators provide a much lower phase noise, while operating synchronously (phase/frequency locking), even under potential oscillators mismatches, without any external circuit or additional power consumption. Then, a single PLL can be implemented (using any node of the array as reference for the feedback path), in order to track PVT variations.

The concept is shown in Figure 4.33, where the repeatable unit cell is highlighted. The coupling elements are represented by $Z_{h,L}$, $Z_{h,R}$, $Z_{v,T}$ and $Z_{v,B}$ for the connecting impedances. The oscillators are based on ROs, where capacitive and resistive coupling are studied, as depicted in Figure 4.34. Inductive coupling was not considered, due to practical layout implementations, and parasitic inductance of the wire was neglected due to relatively low operation frequency and short length.

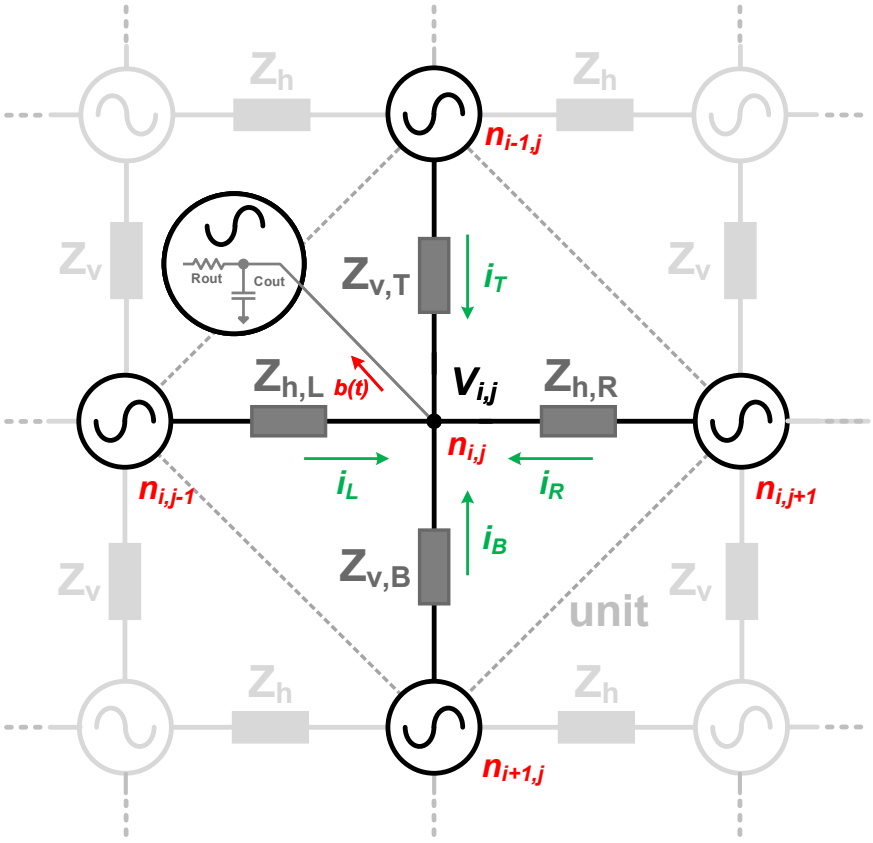



Figure 4.33: Generic mutually coupling oscillators concept.

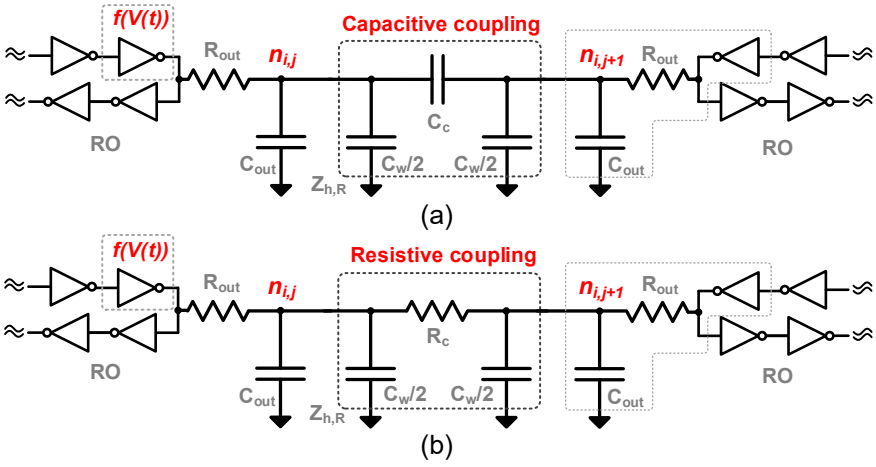



Figure 4.34: Capacitive (a) and resistive (b) coupling elements between two generic ROs (only $Z_{h,R}$ shown).

### NON-LINEAR MODELING

Injection locking has been successfully used in many applications, such as high-frequency clock division [66], quadrature generation [67], clock distribution [62], improvement of RF phase noise in LC-tank oscillators [68], etc. The effect has been extensively studied by several authors, based mostly on the generalized Adler's equation [69, 70], and it is not in the scope of this thesis to revisit the physics of the process any further, but to provide a useful tool to design dTOF image sensors.

The dynamics of the system can be analyzed by performing a nodal analysis on the model shown in Figure 4.34. The process of synchronization occurs by injection-locking through the fundamental frequency, at a single node of each oscillator. The strength of the coupling element and the quality-factor (Q) of the oscillator will define the maximum injection bandwidth, settling time and sensitivity to neighboring disturbances, which depend on the target application and will be discussed further.



A non-linear phase macromodel is used to investigate the injection phenomenon [71]. The ROs dynamics are solved through ordinary differential equations at node $n_{i,j}$, shown in Figure 4.33, under the influence of its neighboring oscillators, at nodes $n_{i-1,j}$, $n_{i+1,j}$, $n_{i,j-1}$, $n_{i,j+1}$, and extrapolating it to the entire system. The numerical analysis of the perturbations is based on the Floquet theory of periodically time-varying systems [72] of ordinary differential equations.

The steady-state voltage response of an oscillator, in the absence of any perturbation, can be represented by the time-dependent function $V_s(t)$. Under an external perturbation, $b(t)$, the RO response becomes:

$$V_{(i,j)} = V_s(t + \alpha(t)) + y(t), \tag{4.12}$$

where the term $\alpha(t)$ is the phase deviation caused by the disturbance $b(t)$. The term $y(t)$ is the orbital deviation reflecting any gain error, in the presence of this external perturbation. However, this term will not be considered for further analysis, as amplitude variations are negligible and the effect of the injection mechanism is dominant on the phase of the oscillator [71]. Thus, the perturbed steady state solution can be approximated by $V_s(t+\alpha(t))$. The perturbation $b(t)$ in this model is represented by currents from the neighboring oscillators $i_L$, $i_R$, $i_T$, $i_B$, as shown in Figure 4.33.

A current analysis of the capacitive coupling, shown in Figure 4.34 (a), at node $n_{i,j}$, can be obtained by:

$$\begin{aligned}\frac{dV_{(i,j)}}{dt} = &\frac{f(V(t))}{R_{out}(C_{out}+2C_w+4C_c)} - \frac{V_{(i,j)}}{R_{out}(C_{out}+2C_w+4C_c)} \\ &+ \frac{C_c}{(C_{out}+2C_w+4C_c)} \cdot \frac{d}{dt}(V_{(i+1,j)} + V_{(i-1,j)} + V_{(i,j+1)} + V_{(i,j-1)}),\end{aligned} \tag{4.13}$$

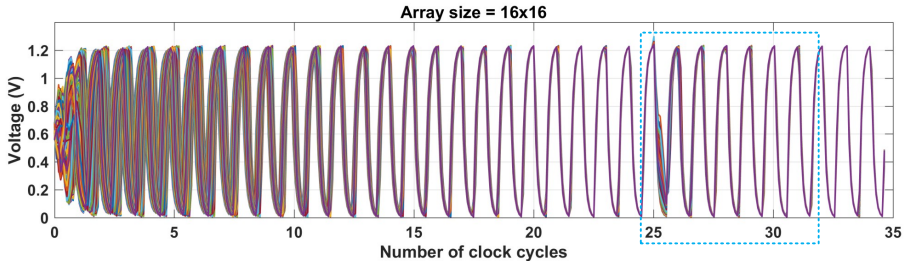
where $V_{(i,j)}$ is the nodal voltage, $R_{out}$ and $C_{out}$ are defined by the RO output impedance. $C_w$ is the shunt parasitic capacitance from the coupling line and $C_c$ is the effective coupling capacitance. The term $f(V(t))$ models the RO stage non-linearity, for the delay stage preceding the coupled node, by a hyperbolic tangent function, $\tanh(G_m V(t))$, where $G_m$ is the large-signal stage transconductance.

Similarly, in the case of a resistive coupling element (Figure 4.34 (b)), the voltage at node $n_{i,j}$ is given by:

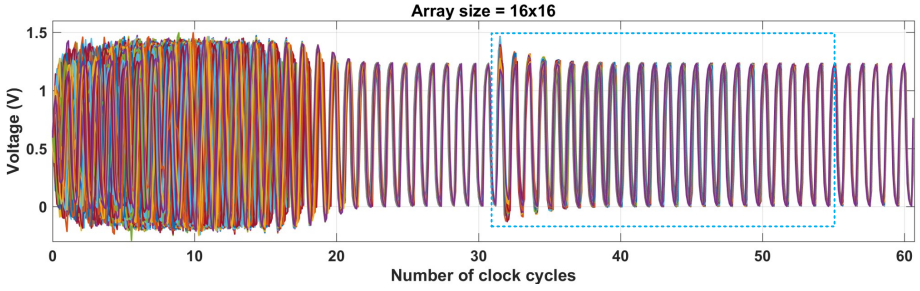
$$\frac{dV_{(i,j)}}{dt} = \frac{f(V(t))}{R_{out}(C_{out}+2C_w)} - \frac{V_{(i,j)}}{R_{out}(C_{out}+2C_w)} + \frac{V_{(i+1,j)} + V_{(i-1,j)} - 2V_{(i,j)} + V_{(i,j+1)} + V_{(i,j-1)} - 2V_{(i,j)}}{R_c(C_{out}+2C_w)}. \tag{4.14}$$

Equations (4.13), (4.14) were numerically solved in MATLAB for TDC networks of 4×4, 8×8 and 16×16, using 7-stage ROs, although the modeling holds true for any number of RO stages, just with an impact on its dynamics. The networks are terminated (at their boundaries) by the same coupling element, however open at one of its ends.

For the following simulations, the parameters $R_{out}$, $C_{out}$ and $G_m$ (refer to Figure 4.34) were chosen (based on typical values) to obtain an average oscillation period of 2 ns (500 MHz). Random mismatches were also included, with an impact of about ±15% period variation among the oscillators, in order to verify the robustness of the method.




(a)




(b)

Figure 4.35: Voltage waveforms of 16×16 coupled RO network under ±15% random initial conditions and with disturbance introduced in 32 ROs in case of resistive coupling with $R_c$ = 250Ω (a) and capacitive coupling with $C_c$ = 240 fF (b).

The steady-state voltage for a 16×16 RO array, using coupling resistance of $R_c$ = 250 Ω, is shown in Figure 4.35 (a). The ROs started with a random period of 2±0.3 ns

(500±77 MHz) and completely arbitrary phases. After 18 cycles (36 ns), the ROs reach locking with a steady state phase skew of 114 ps. Any on-chip disturbance, such as supply spikes and charge injection on the ROs phases, affects directly the attained steady state. Although open-loop TDCs cannot recover from such disturbances, the proposed approach is self-regulated, by the local feedback from neighboring TDCs, allowing continuous phase/frequency locking. In order to simulate this effect, 32 of the coupled 16×16 array nodes were injected with a disturbance that corresponds to 33% of the overall node charge, after 25 clock cycles, in their most sensitive phase – zero-crossing (see Figure 4.35 (a)). The process of re-synchronization starts immediately after the disturbance, taking about 7 clock cycles (14 ns) to reach steady state once again (the same phase skew as before the injection). Figure 4.35 (b) shows similar simulation, but for a capacitive coupling of $C_c$ = 240 fF. After steady state is reached (31 clock cycles), 32 ROs were disturbed with 33% of the total nodal charge. The process of re-synchronization takes about 20 clock cycles to attain steady state again.



The settling time can vary based on the number of ROs disturbed, the size of the array and coupling strength. Figure 4.36 shows this dependency, over a number of disturbed oscillators for the cases of resistive and capacitive coupling.

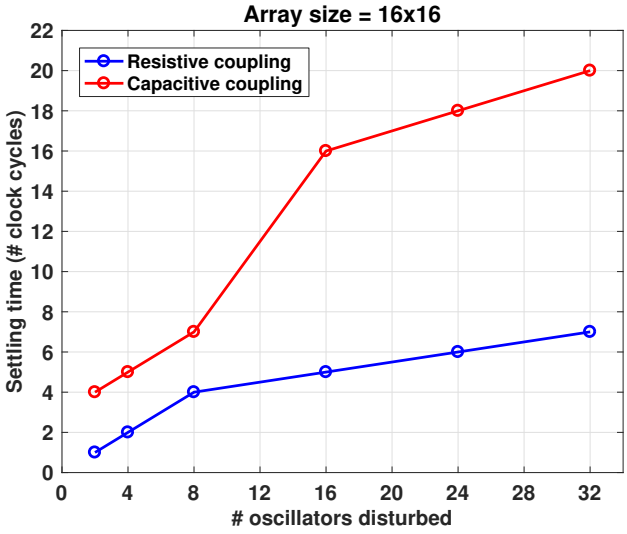
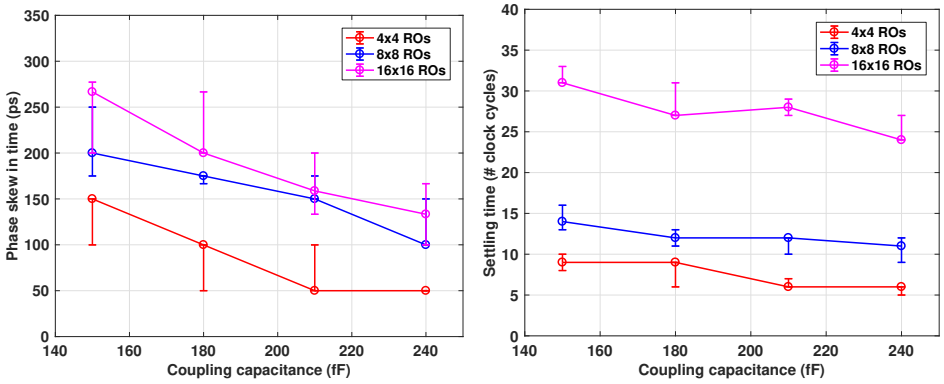



Figure 4.36: Steady state recovery time (in cycles), after different number of ROs disturbed.

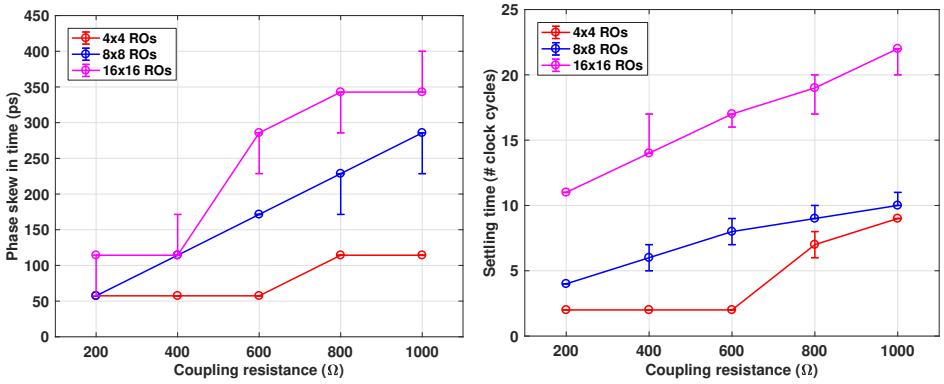
Frequency mismatches and/or PVT variation directly affect the settling time and phase skew. Variations on the coupling impedance also have an impact on the steady state, thus, apart from ±15% variation on the RO periods, another ±10% on the coupling impedance was included in the simulations. Simulation results for the case of capacitive coupling are shown in Figure 4.37. The phase skew increases with the number of coupled ROs and for lower coupling impedances. For instance, for the capacitive coupling ($C_c$ = 240 fF), it takes about 6 clock cycles for a 4×4 array, to reach steady state, whilst it takes 24 clock cycles for the 16×16 array, with the same $C_c$, as can be seen in Figure 4.37 (b). Similarly, the




(a) (b)

Figure 4.37: Steady state phase skew (a) and settling time (b), for different network sizes and coupling capacitance. Settling time is defined by the phase mismatch below 1/(67%) of value obtained in (a); vertical bars indicate variation due to ±10% mismatch in $C_c$

same steady state parameters were obtained for the case of resistive coupling, as shown in Figure 4.38. A 600 Ω coupling resistance produced a maximal residual phase skew of 280 ps for the 16×16 array, while for the 4×4, the skew is only 60 ps. Higher coupling resistances also result in longer settling time, as shown in Figure 4.38 (b).




(a) (b)

Figure 4.38: Steady state phase skew (a) and settling time (b), for different network sizes and coupling resistance. Settling time is defined by the phase mismatch below 1/(67%) of value obtained in (a); vertical bars indicate variation due to ±10% mismatch in $R_c$.

Charge injection through capacitive coupling only occurs during phase transitions, due to transient voltage variation, which produces longer settling time. Fast coupling is possible by increasing the coupling capacitance, but due to area constraints and excessive parasitic capacitance, it may limit the overall linearity and operating frequency. Resistive coupling, however, can provide much stronger coupling (lower impedance) at smaller areas, being

more suitable for our application.

These results provide a quick insight on the dynamics of mutually coupled ROs, using different types of coupling and different strengths, thus enabling better design choices based on the target application. It also provides a qualitative and quantitative analysis on the process of synchronization, allowing better planning for calibration, both foreground and background.

### SPICE-COMPATIBLE MODEL

In addition to the macro-model developed in Section 4.3.1, a SPICE-compatible (based on Verilog-A) model is also used, since electronic circuits are normally designed and simulated in such environments and the interaction with other signals on the readout integrated circuit (ROIC) can be evaluated.



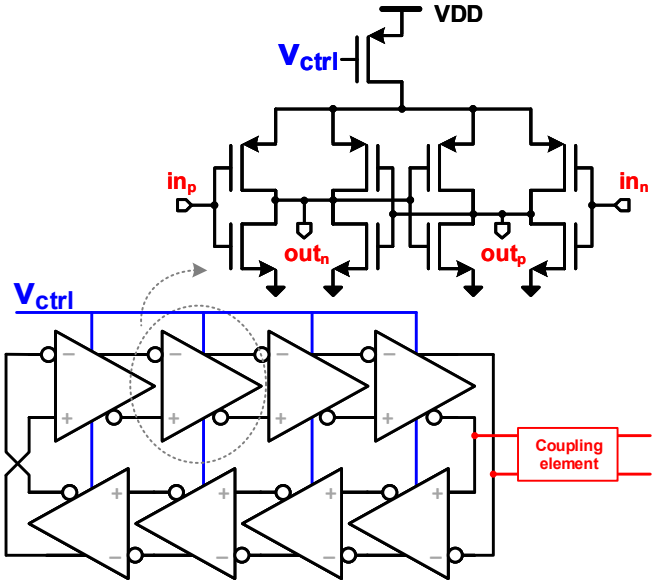



Figure 4.39: Current-starved, 8-stage pseudo-differential RO

The model comprises a large-signal, differential transconductance, coupled to a capacitive impedance, to form each stage of the oscillator [73]. The frequency is controlled by a current source (current-starved RO) and it includes noise effects (thermal and flicker) that are naturally up-converted during oscillation. Although this model can be adapted to different number of stages and topologies, it was designed to match the RO implemented and measured in Section 4.3.1, which is composed by a 8-stage, pseudo-differential topology as shown in Figure 4.39.

Apart from the synchronization, the uncorrelated noise between ROs is filtered out. On average, ROs have low power efficiency – FOM [37] – on the order of 145-160 dB, which relates their noise (phase noise/jitter) and power consumption. For example, without any elaborate filtering, a 500 MHz RO, consuming 400 $\mu$W, and has a FOM of 150 dB, produces an integrated RMS jitter [74] of about 110 ps (from 1 MHz to 100 MHz integration

window), which is prohibitively large for millimetric precision measurements, requiring feedback loops for noise filtering, at the expense of power, area, and complexity. However, by coupling multiple oscillators, the uncorrelated noise among them is filtered out, providing a reduction in phase noise (and jitter) at system level by $10 \cdot \log_{10} M$ [75], where $M$ is the number of coupled oscillators. Although the FOM of the system remains the same and the overall power consumption increases and the noise reduces $M$ times, at each oscillator, the FOM appears to improve also by $10 \cdot \log_{10} M$, with negligible extra power consumption.



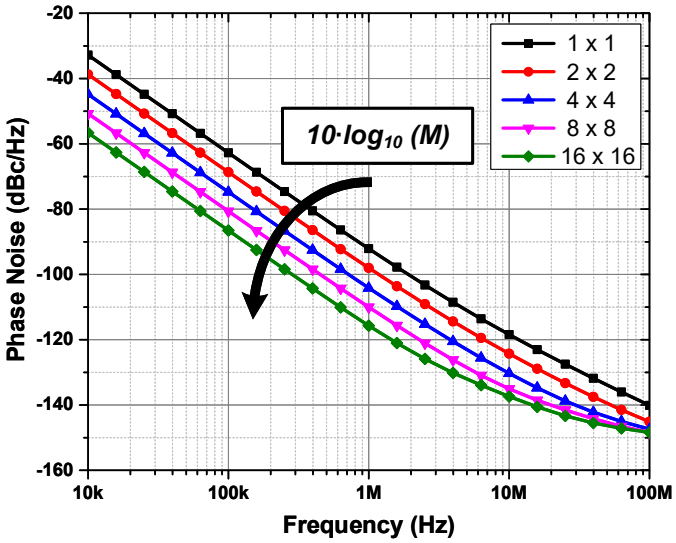



Figure 4.40: Simulation of phase noise reduction from 1 (1×1) to 256 (16×16) mutually-coupled ROs.

To demonstrate the described effect, multiple array sizes of oscillators were coupled with the simulation results depicted in Figure 4.40. The phase noise reduction of the uncorrelated noise (low offset frequencies) behaves as predicted. For the correlated noise (high offset frequencies), such as the thermal noise on the coupling elements, the benefit of the coupling is reduced. A comparison between full SPICE and Verilog-A models was also evaluated. The latter took only 1.5% of the computational power and simulation time than the former, at equivalent precision, providing an essential tool for full chip co-simulation.

The implemented block diagram can be seen in Figure 4.41. Due to resistive coupling, the phase/frequency locking operates throughout the array at all times and, as a result, both, at startup, when the ROs have arbitrary phases (and perhaps different average frequencies), or during any disturbance in one or more of the ROs, the array will be always pushed back to a locked state. That is represented by the phase diagram at the bottom of Figure 4.41. Also, due to the nature of the operation and the fact that all ROs are synchronized and share a common control voltage ($CTRL$), a single PLL can be implemented to define the overall frequency and to track PVT variations, using a single regional phase as reference for the feedback loop.

Thus, starting from the same 150 dB FOM RO at 0.5 GHz and coupling 64 ROs (in an 8×8 structure), the effective FOM is improved by $10 \cdot \log_{10} M \approx 18$ dB, to a moderate 168 dB

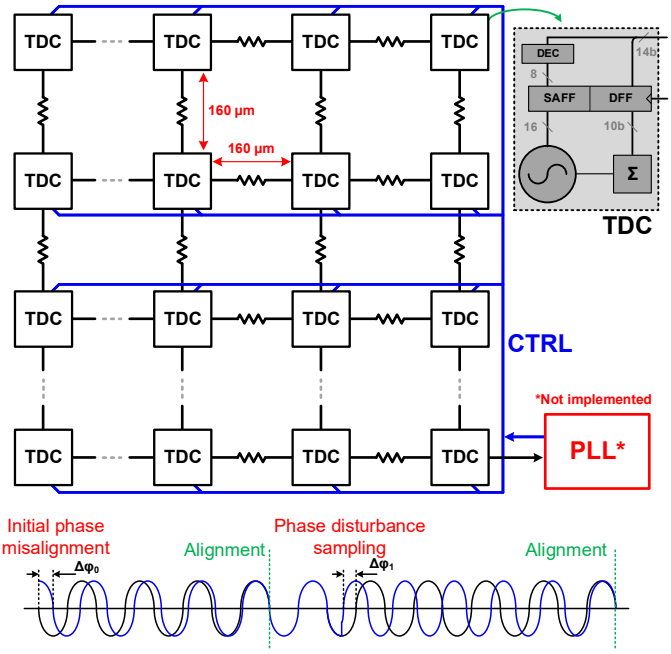



Figure 4.41: Implemented 8×8 mutually-coupled TDC architecture and RO phase misalignment self-correction.

FOM, which produces an integrated RMS jitter (from 1 MHz to 100 MHz) of only 13.75 ps, instead of 110 ps as previously found. For the final topology, an 8-stage, current-starved, pseudo-differential RO was implemented [76].

The process of locking was simulated including ±10% random period variation among the ROs, such as in Section 4.3.1. The variation was performed by introducing a mismatch on the transconductance of each RO. The phase offset in steady state, over time, is shown in Figure 4.42, which is less than 1 LSB after 10 oscillation periods for a coupling resistance of 400 Ω.

Along with the RO, a 10-bit ripple counter and D-type and sense-amplifier flip-flops complete the TDC. A single TDC is expected to be shared among two independent groups of 8 × 8 pixels, as sketched in Figure 4.43. The resistive coupling used was implemented through a transmission gate, shown in Figure 4.43, so the performance in both modes could be compared. Moreover, it can be used to disable the coupling during initial calibration phase, where all ROs can be adjusted to roughly the same frequency, before coupling, thus improving INL and power efficiency.

### RESULTS

The prototype has been fabricated using a 3D-stacked CMOS technology [77], as sketched in Figure 4.43. The 64 ROs were arranged in a 8×8 matrix, only on the bottom tier, which uses low power, 4 metals (3 thin + 1 thick) 65nm TSMC technology, with 1.2 V core supply. The proposed technique is independent of the technology and transistor node, also suitable for monolithic implementation, but the fact that the top tier is placed over the TDC array, a

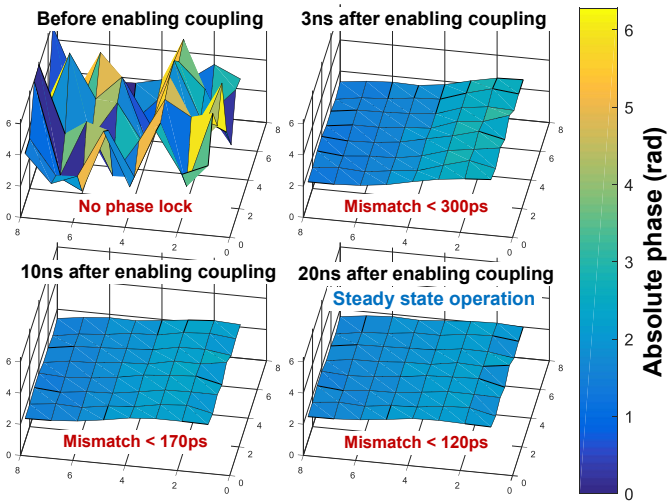



Figure 4.42: Instantaneous phase mismatch progression, for ±10% RO period variation over the implemented 8×8 TDCs.

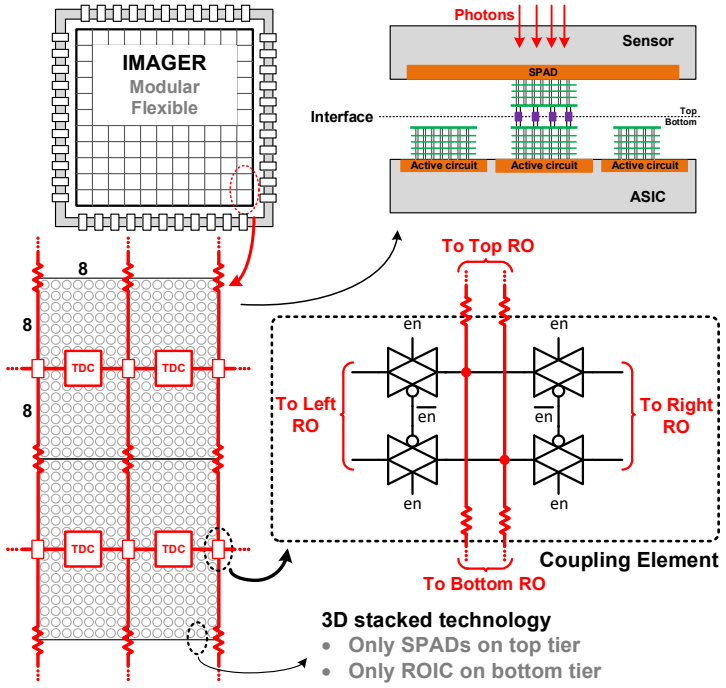



Figure 4.43: Transmission gate as resistive coupling element. 3D stacked technology implementation.

chip micrograph could not be obtained.

Coupled and uncoupled conditions were implemented and measured. To mimic the distribution in a real sensor, the TDCs were placed with a pitch of 160 $\mu$m, horizontally and vertically, thus achieving a total area of 1.3 x 1.3 mm$^2$. Each TDC occupies an area of 76 x 7.2 $\mu$m$^2$, including RO, a 10b counter, sampling latches, and decoupling capacitors, which occupy 60% of the TDC array, whose layout is shown in Figure 4.44.

The effects of the coupling are investigated by measuring the high-frequency clock from the ROs. All 64 ROs are combined through multiplexers and carefully routed to a single high-speed output, connected to Rohde & Schwarz FSUP-50 signal source analyzer or Keysight Infiniium DSOS804A real-time oscilloscope, for spectrum and phase noise, or jitter measurements, respectively.



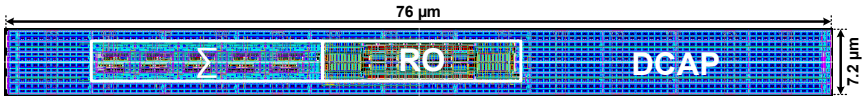



Figure 4.44: TDC layout.

In our fabricated chip, a large IR drop was present, due to only few metal layers (3 thin + 1 thick) available. Its effects on frequency variation can be seen in Figure 4.45 (a). Although the intrinsic frequency of each RO varies substantially (about 24%), the mutual coupling is very robust, reaching frequency locking as shown in Figure 4.45 (b). Ideally, the ROs should be independently tuned to roughly the same frequency (which can be done by foreground calibration), to ease the process of frequency correction, power consumption reduction (less charge exchange between oscillators) and local INL minimization.

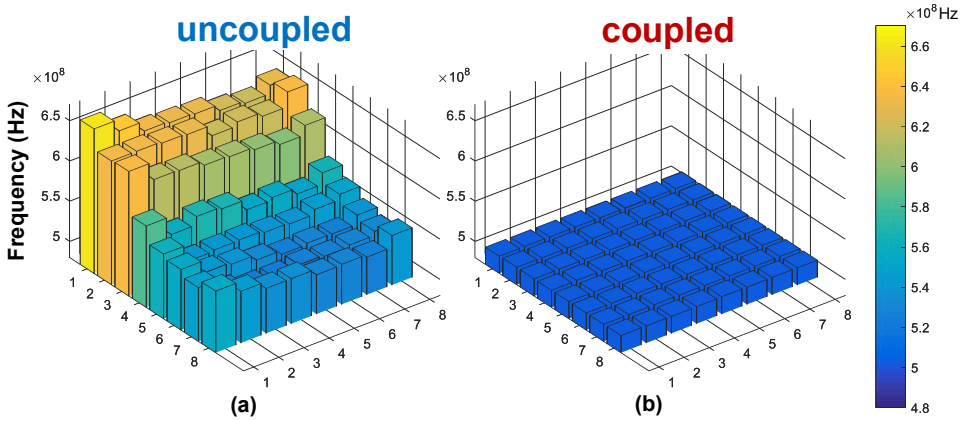



Figure 4.45: Individual frequencies of uncoupled and coupled modes.

The array was measured in the whole range of frequencies, from 150 to 800 MHz. The mean values and variation bars, in coupled and uncoupled modes, are plotted in Figure 4.46. Before coupling, the spread in the instantaneous frequency was 22 – 26%, whereas under

the mutual coupling, this spread reduced to less than 0.11%. Moreover, under the coupling and, consecutively, locking, all ROs operate at the same average frequency.

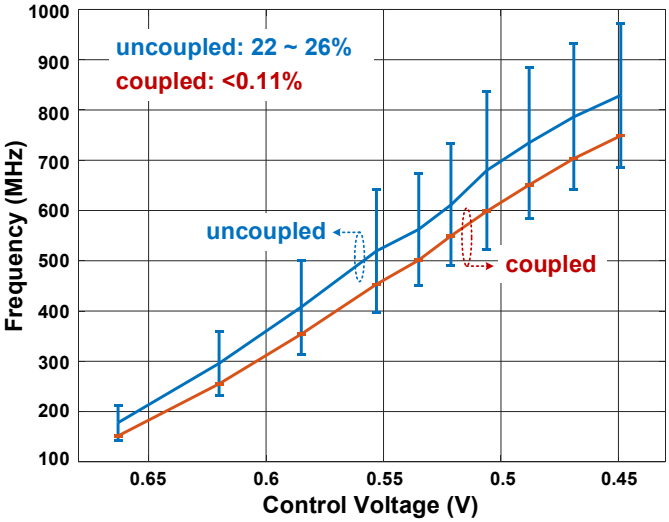


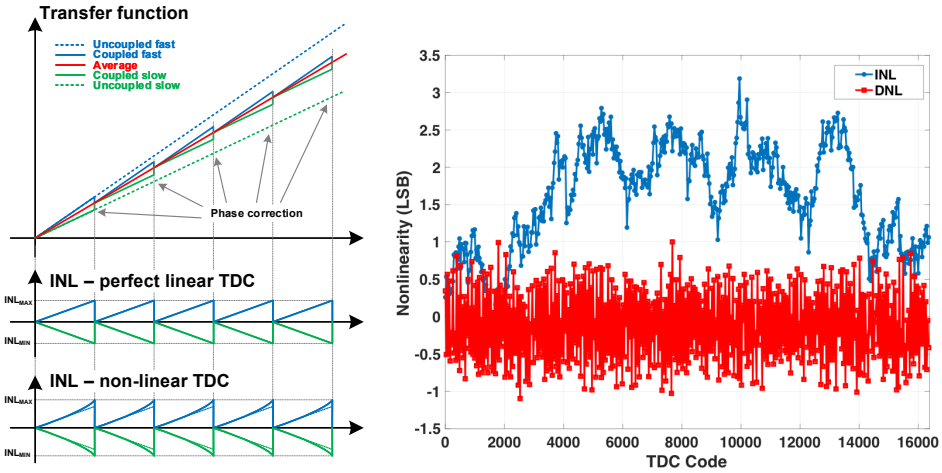

Figure 4.46: Frequency variation of coupled and uncoupled modes, for different average frequencies.

It is pertinent to observe that, after coupling, the operating frequency is lower than the average of the individual oscillators, both in Figure 4.45 and Figure 4.46. The reason is the effect of parasitic capacitance from the coupling element and lines, that is only visible when coupling is enabled. For that reason, the RO was designed with asymmetric stages (stronger for the coupling phase), thus maintaining overall linearity when coupled.

The main goal of this work was to provide an alternative for timing generation and acquisition in large arrays of dTOF sensors. In order to reduce calibration (often difficult to implement in a real application) and resolution uncertainties throughout the sensor, the injection locking technique produced by the mutually coupled oscillators was proposed. However, this technique does not improve the linearity of the individual TDCs and, in fact, it trades resolution uncertainty for short range INL.

For instance, if all TDCs in the array have the same performance (the same RO frequency), by coupling them, they would present the same non-linearity as an uncoupled TDC. However, if variations are present (IR-drop, PVT variations, etc.), they would still be locked in frequency and phase, but a correction in phase would need to occur, rendering an abrupt non-linearity. It largely depends on the performance of each TDC, the system power distribution, etc. An example phase correction is presented in Figure 4.47 (a). For an ideal case of perfectly linear TDC, due to different performance, at every RO period, the phase needs to be aligned, generating a local INL whose maximum and minimum would depend on the RO period difference to the average period ($|INL_{MAX|MIN}| = |T_{RO} - T_{AVG}|$). In the presence of intrinsic TDC non-linearity, $|INL_{MAX|MIN}|$ will be a combination of both effects. An illustration of the local INL is shown in the bottom of Figure 4.47 (a).

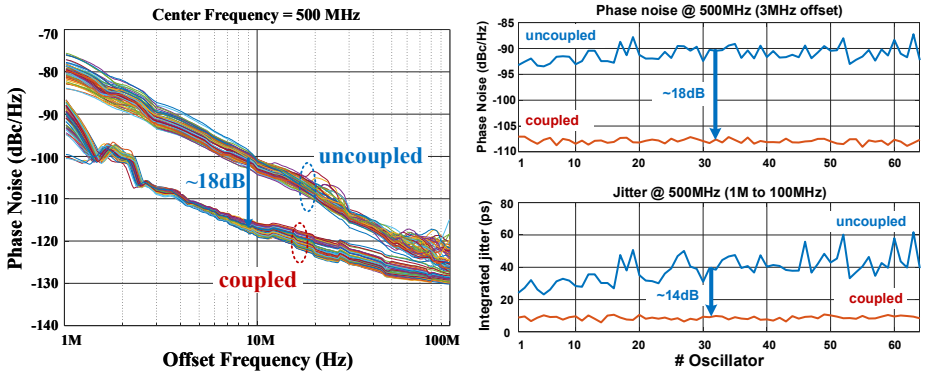
Due to the aforementioned reasons, only the uncoupled TDC non-linearity is presented.




(a) (b)

Figure 4.47: TDC non-linearity effects: (a) Local INL due to phase correction, for a perfect linear TDC and a non-linear TDC; (b) Uncoupled TDC INL and DNL, without calibration.

It has been evaluated using density test and it is plotted in Figure 4.47 (b). The maximum INL and DNL were below 3 LSB and 2 LSB, respectively, over the whole 14-bit of dynamic range, without calibration.




(a) (b)

Figure 4.48: Performance comparison of coupled and uncoupled ROs, at 500 MHz center frequency: (a) measured phase noise; (b) phase noise at 3 MHz offset and integrated RMS jitter.

The phase noise is a key parameter to confirm the effectiveness of mutual coupling on noise filtering and synchronization. Figure 4.48 (a) shows 18 dB phase noise improvement provided by the coupling, for most of the frequency offsets, following the theory. For high frequency offsets, the thermal noise of the coupling elements dominates the phase noise

and, due to its correlation within the array, the coupling is not as effective.

The phase noise of each RO is plotted along with the integrated RMS jitter, in Figure 4.48 (b). Both measurements were performed with the ROs coupled and uncoupled, at a center frequency of 500 MHz. The phase noise at 3 MHz offset frequency shows the effectiveness of the coupling, reaching on average a 18 dB improvement. The jitter reduction reached 14 dB (instead of 18 dB), due to the presence of correlated noise from the coupling elements.

Figure 4.45 and Figure 4.48 (b) show variations of phase noise and jitter, under 'uncoupled' mode. The reason for the variation is the extreme IR-drop present in the system, where the oscillators close to the edge of the chip (lower indexes, starting from #1) have lower impedance to the supply, as well as their PMOS current source have higher drain-source voltage, allowing stronger inversion, and thus lower noise factor. Although such conditions exist, they do not affect the synchronization and the noise filtering proposed, which is proved by the phase noise and jitter, under the 'coupled' mode. Nevertheless, the integrated RMS jitter reduction, from about 40 ps to less than 9 ps, is enough for our application, which contains other noise sources (SPAD timing jitter [77], for instance) that are much higher.



### 4.3.2. CHAIN OF TDCS

Similarly to the 2D TDC array discussed in the previous section, other arrangements can also be realized. The most straightforward approach is to connect the TDC in a chain, in a single direction. This arrangement is particularly useful for a column-wise approaches, where the TDC are allocated on side/bottom of the image array, often being shared among several pixels [3, 59, 78]. The proposed approach can be used as alternative to phase distribution that can consume excessive power [3], but the activity should be considered as well.

The arrangement covered in this section regards the modular architecture described in Section 6.2, where a group of 17 continuously running TDCs are organized in the middle of the sensor,collecting the timestamping events originated on the 4 quadrants of the array. The architecture itself uses 16 TDCs for timing acquisition and an extra TDC for reference, for both, calibration and range extension.

The TDCs arrangement is shown in Figure 4.49. Each TDC can be individually enabled and, depending on the coupling, connected to the horizontal differential line, responsible to carry the locking signal to all the TDCs. Each oscillator is based on a 4-stage, multi-path pseudo-differential RO, and are mutually coupled by one of its phases through a simple transmission gate. The free-running RO frequency can be adjusted from 2 to 4 GHz, so a maximum resolution of 15 ps can be obtained. For monitoring purposes, however, the coupling differential line is connected to a differential-to-single ended buffer that feeds a divider-by-4 block, generating a moderate 0.5–2 GHz output frequency. The lower frequency output is then buffered in such a way to be able to drive the 50 Ω spectrum analyzer input impedance, required for phase noise measurement.

The RO designed is based on Figure 4.39, but instead of 8 stages, only 4 are implemented. Also, instead of only a pMOS transistor as current source, a nMOS as current sink is also implemented. The main reason for such implementation is to maintain the DC level constant, independently of the frequency, preserving the behavior of the sampling elements,

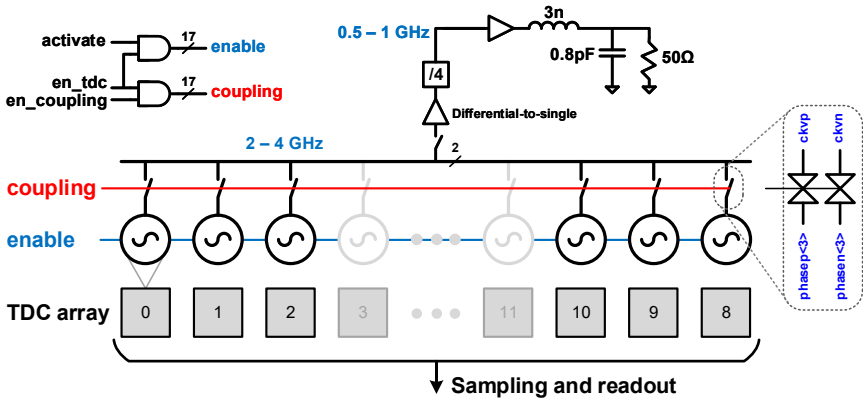



Figure 4.49: In-line mutually coupling TDC arrangement.

during a timestamp acquisition. The frequency is controlled by an external bias, which is low-pass filtered on-chip, for lower phase noise.

The effects of the coupling on the array is also observed. Figure 4.50 shows the phase noise in both conditions. As expected, the phase suffers a suppression of $10 \cdot \log_{10} N$, where $N$ is the number of oscillators, leading to a phase noise reduction of $10 \cdot \log_{10} 17 = 12.3$ dB for most of the noise spectrum, relative to the uncorrelated noise. Due to interference of the digital clock frequency (4 MHz), it is possible to observe spurious tones at 4 MHz and in its higher harmonics. Nevertheless, the overall integrated RMS jitter was reduced from 40 ps (in uncoupled mode) down to 7.5 ps, whiles operating at the internal TDC frequency of 4 GHz (the measured value is divided by 4).

Since the TDCs are concentrated and very close to each other, the coupling impedance is very small, mandated by the transmission gate element. Moreover, they arrangement allows a very robust power routing, while their physical distance keeps their mismatch very small.

## 4.4. CONCLUSIONS

Generating a uniform timing reference, used to capture telemetry and depth maps of large arrays of dTOF is very challenging. Constraints on power consumption, area and technology (*e.g.* limited number of metal layers for proper power distribution) are some of the key limiting factors. Traditional approaches, such as PLL/DLL, are not typically applicable (due to area limitation and complexity), whereas column-wise arrangements [3, 78] and per-pixel TDCs [12, 79] are limited to small arrays and photon-starved mode, respectively.

By comparing event-driven to an always on, shared TDC approaches, with respect to power consumption and area, it is possible to conclude that, for most applications, with moderate/high activity, the latter approach has better power efficiency, with slightly lower saturation of the sensor, especially for short illumination bursts than the former.

Moreover, the always-on TDC array allows uniform and (almost) constant power consumption throughout the sensor, independently of the activity, removing the IR-drop uncertainty – typical of event-driven systems. A phase calibration can be performed to compen-

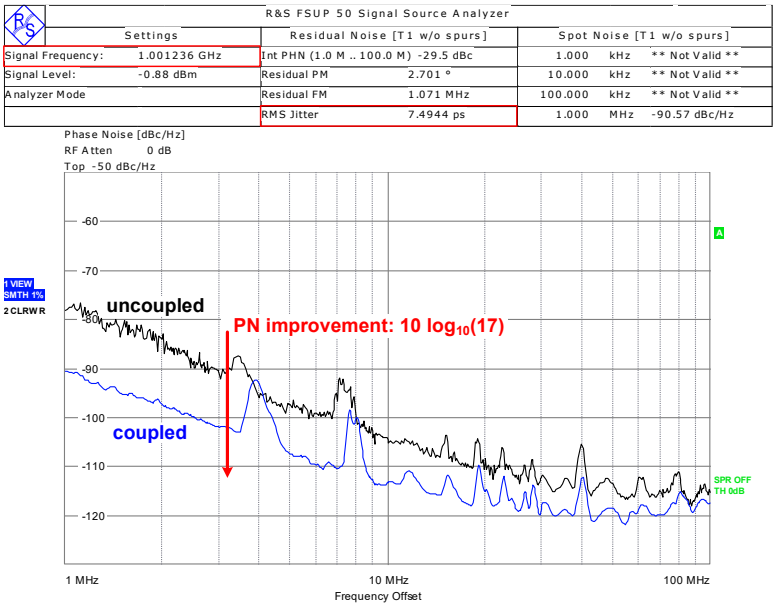



Figure 4.50: Phase noise measurement of coupled and uncoupled TDC chain.

sate residual skew, while PVT tracking is possible through a single PLL, using any phase, in the array, as a reference, since all ROs will be synchronized. The proposed architecture provides also an automatic, fast, and local feedback, where disturbances in the phase of a particular RO are corrected by its neighbors, thus providing a robust, scalable approach to synchronization.

A careful study of the coupling element (resistive/capacitive) was performed and a coupling sensitivity was discussed, as well as its implication on the settling time and phase error. In general terms (also, intuitively), the stronger the coupling (lower impedance), the faster the steady state the array will reach, but then the more sensitive a TDC will be to its neighbors, in the case of disturbances.

# REFERENCES


[1] A. Ximenes, G. Vlachogiannakis, and R. B. Staszewski, *An ultracompact 9.4–14.8-ghz transformer-based fractional-n all-digital pll in 40-nm cmos,* IEEE Trans. Microw. Theory Techn. **65**, 4241 (2017).

[2] A. Ronchini Ximenes, P. Padmanabhan, and E. Charbon, *Mutually coupled time-to-digital converters (tdcs) for direct time-of-flight (dtof) image sensors,* Sensors **18**, 3413 (2018).

[3] A. Carimatto, S. Mandai, E. Venialgo, T. Gong, G. Borghi, D. R. Schaart, and E. Charbon, *11.4 a 67,392-spad pvtb-compensated multi-channel digital sipm with 432 column-parallel 48ps 17b tdcs for endoscopic time-of-flight pet,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2015) pp. 1–3.

[4] C. Veerappan, J. Richardson, R. Walker, D. Li, M. Fishburn, D. Stoppa, F. Borghetti, Y. Maruyama, M. Gersbach, R. Henderson, *et al.*, *Characterization of large-scale non-uniformities in a 20k tdc/spad array integrated in a 130nm cmos process,* in *IEEE European Solid-State Device Research Conference (ESSDERC)* (2011) pp. 331–334.

[5] R. B. Staszewski, J. L. Wallberg, S. Rezeq, C.-M. Hung, O. E. Eliezer, S. K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, *et al.*, *All-digital pll and transmitter for mobile phones,* IEEE J. Solid-State Circuits **40**, 2469 (2005).

[6] C. Niclass, A. Rochas, P.-A. Besse, and E. Charbon, *Design and characterization of a cmos 3-d image sensor based on single photon avalanche diodes,* IEEE J. Solid-State Circuits **40**, 1847 (2005).

[7] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara, *1.3 v 20 ps time-to-digital converter for frequency synthesis in 90-nm cmos,* IEEE Transactions on Circuits and Systems II: Express Briefs **53**, 220 (2006).

[8] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, *A 128×128 single-photon image sensor with column-level 10-bit time-to-digital converter array,* IEEE J. Solid-State Circuits **43**, 2977 (2008).

[9] P. Dudek, S. Szczepanski, and J. V. Hatfield, *A high-resolution cmos time-to-digital converter utilizing a vernier delay line,* IEEE J. Solid-State Circuits **35**, 240 (2000).

[10] J. Yu, F. F. Dai, and R. C. Jaeger, *A 12-bit vernier ring time-to-digital converter in 0.13µm cmos technology,* IEEE J. Solid-State Circuits **45**, 830 (2010).

[11] M. Tanaka, H. Ikeda, M. Ikeda, and S. Inaba, *Development of monolithic time-to-amplitude converter for high precision tof measurement,* IEEE transactions on nuclear science **38**, 301 (1991).

[12] F. Villa, R. Lussana, D. Bronzi, S. Tisa, A. Tosi, F. Zappa, A. Dalla Mora, D. Contini, D. Durini, S. Weyers, *et al.*, *Cmos imager with 1024 spads and tdcs for single-photon timing and 3-d time-of-flight,* IEEE J. Sel. Topics Quantum Electron. **20**, 364 (2014).

[13] F. M. Gardner, *Phaselock techniques* (John Wiley & Sons, 2005).

[14] F. Gardner, *Charge-pump phase-lock loops,* IEEE transactions on Communications **28**, 1849 (1980).

[15] B. Miller and B. Conley, *A multiple modulator fractional divider,* in *Frequency Control, 1990., Proceedings of the 44th Annual Symposium on* (IEEE, 1990) pp. 559–568.

[16] T. A. Riley, M. A. Copeland, and T. A. Kwasniewski, *Delta-sigma modulation in fractional-n frequency synthesis,* IEEE J. Solid-State Circuits **28**, 553 (1993).

[17] R. B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, *et al.*, *All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS,* IEEE J. Solid-State Circuits **39**, 2278 (2004).

[18] L. Xu, S. Lindfors, K. Stadius, and J. Ryynanen, *A 2.4-GHz low-power all-digital phase-locked loop,* IEEE J. Solid-State Circuits **45**, 1513 (2010).

[19] J. Zhuang and R. Staszewski, *A low-power all-digital PLL architecture based on phase prediction,* in *IEEE Intern. Conf. on Electronics, Circuits and Systems (ICECS)* (2012) pp. 797–800.

[20] M. Park, M. Perrott, and R. Staszewski, *An Amplitude Resolution Improvement of an RF-DAC Employing Pulsewidth Modulation,* IEEE Trans. Circuits Syst. I **58**, 2590 (2011).

[21] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, *A 2.9–4.0-GHz Fractional-N Digital PLL With Bang-Bang Phase Detector and 560-Integrated Jitter at 4.5-mW Power,* IEEE J. Solid-State Circuits **46**, 2745 (2011).

[22] N. Pavlovic and J. Bergervoet, *A 5.3 GHz digital-to-time-converter-based fractional-N all-digital PLL,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2011) pp. 54–56.

[23] V. K. Chillara, Y.-H. Liu, B. Wang, A. Ba, M. Vidojkovic, K. Philips, H. de Groot, and R. B. Staszewski, *9.8 An 860μW 2.1-to-2.7 GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth Smart and ZigBee) applications,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2014) pp. 172–173.

[24] G. W. Roberts and M. Ali-Bakhshian, *A brief introduction to time-to-digital and digital-to-time converters,* IEEE Transactions on Circuits and Systems II: Express Briefs **57**, 153 (2010).

[25] G. S. Vlachogiannakis, A. R. Ximenes, and R. B. Staszewski, *Fractional-n frequency synthesizer incorporating cyclic digital-to-time and time-to-digital circuit pair,* (2017), uS Patent 9,722,537.

[26] N. Da Dalt, *A design-oriented study of the nonlinear dynamics of digital bang-bang plls,* IEEE Trans. Circuits Syst. I **52**, 21 (2005).

[27] I. Galton, *Spectral shaping of circuit errors in digital-to-analog converters,* IEEE Trans. Circuits Syst. II **44**, 808 (1997).

[28] R. T. Baird and T. S. Fiez, *Improved/spl delta//spl sigma/dac linearity using data weighted averaging,* in *Circuits and Systems, 1995. ISCAS'95., 1995 IEEE International Symposium on*, Vol. 1 (IEEE, 1995) pp. 13–16.

[29] D. Ham and A. Hajimiri, *Concepts and methods in optimization of integrated LC VCOs,* IEEE J. Solid-State Circuits **36**, 896 (2001).

[30] N. M. Neihart, D. J. Allstot, M. Miller, and P. Rakers, *Twisted inductors for low coupling mixed-signal and RF applications,* in *IEEE Custom Integrated Circuits Conference (CICC)* (IEEE, 2008) pp. 575–578.

[31] A. Poon, A. Chang, H. Samavati, and S. S. Wong, *Reduction of inductive crosstalk using quadrupole inductors,* IEEE J. Solid-State Circuits **44**, 1756 (2009).

[32] C.-C. Li, T.-H. Tsai, M.-S. Yuan, C.-C. Liao, C.-H. Chang, T.-C. Huang, H.-Y. Liao, C.-T. Lu, H.-Y. Kuo, K. Hsieh, *et al.*, *A 0.034 mm 2, 725fs RMS jitter, 1.8%/V frequency-pushing, 10.8–19.3 GHz transformer-based fractional-N all-digital PLL in 10nm FinFET CMOS,* in *IEEE VLSI Circuits Symp. Tech. Papers* (2016) pp. 1–2.

[33] P. Andreani, K. Kozmin, P. Sandrup, M. Nilsson, and T. Mattsson, *A TX VCO for WCDMA/EDGE in 90 nm RF CMOS,* IEEE J. Solid-State Circuits **46**, 1618 (2011).

[34] L. Fanori, T. Mattsson, and P. Andreani, *21.6 A 2.4-to-5.3 GHz dual-core CMOS VCO with concentric 8-shaped coils,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2014) pp. 370–371.

[35] D. J. Griffiths and R. College, *Introduction to electrodynamics*, Vol. 3 (Prentice hall Upper Saddle River, NJ, 1999).

[36] M. Babaie and R. B. Staszewski, *A Class-F CMOS Oscillator,* IEEE J. Solid-State Circuits **48**, 3120 (2013).

[37] P. Kinget, *Analog circuit design* (Springer, 1999) pp. 353–381.

[38] S. Min, T. Copani, S. Kiaei, and B. Bakkaloglu, *A 90-nm CMOS 5-GHz ring-oscillator PLL with delay-discriminator-based active phase-noise cancellation,* IEEE J. Solid-State Circuits **48**, 1151 (2013).

[39] M. Kossel, T. Morf, J. Weiss, P. Buchmann, C. Menolfi, T. Toifl, and M. L. Schmatz, *LC PLL with 1.2-octave locking range based on mutual-inductance switching in 45-nm SOI CMOS,* IEEE J. Solid-State Circuits **44**, 436 (2009).

[40] J. Zhuang and R. B. Staszewski, *Gain estimation of a digital-to-time converter for phase-prediction all-digital PLL,* in *IEEE European Conf. on Circuit Theory and Design (ECCTD)* (2013) pp. 1–4.

[41] R. B. Staszewski, D. Leipold, K. Muhammad, and P. T. Balsara, *Digitally controlled oscillator (DCO)-based architecture for RF frequency synthesis in a deep-submicrometer CMOS process,* IEEE Trans. Circuits Syst. II **50**, 815 (2003).

[42] X. Gao, E. A. Klumperink, P. F. Geraedts, and B. Nauta, *Jitter analysis and a benchmarking figure-of-merit for phase-locked loops,* IEEE Trans. Circuits Syst. II, Exp. Briefs **56**, 117 (2009).

[43] T.-K. Kao, C.-F. Liang, H.-H. Chiu, and M. Ashburn, *A wideband fractional-N ring PLL with fractional-spur suppression using spectrally shaped segmentation,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2013) pp. 416–417.

[44] G. Marucci, A. Fenaroli, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, *A 1.7 GHz MDLL-based fractional-N frequency synthesizer with 1.4 ps RMS integrated jitter and 3mW power using a 1b TDC,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2014) pp. 360–361.

[45] J. A. Tierno, A. V. Rylyakov, and D. J. Friedman, *A wide power supply range, wide tuning range, all static CMOS all digital PLL in 65 nm SOI,* IEEE J. Solid-State Circuits **43**, 42 (2008).

[46] R. K. Nandwana, T. Anand, S. Saxena, S.-J. Kim, M. Talegaonkar, A. Elkholy, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, *A calibration-free fractional-N ring PLL using hybrid phase/current-mode phase interpolation method,* IEEE J. Solid-State Circuits **50**, 882 (2015).

[47] T.-H. Tsai, M.-S. Yuan, C.-H. Chang, C.-C. Liao, C.-C. Li, and R. B. Staszewski, *A 1.22 ps integrated-jitter 0.25-to-4GHz fractional-N ADPLL in 16nm FinFET CMOS,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2015) pp. 1–3.

[48] A. Elkholy, S. Saxena, R. K. Nandwana, A. Elshazly, and P. K. Hanumolu, *A 2.0–5.5 GHz Wide Bandwidth Ring-Based Digital Fractional-N PLL With Extended Range Multi-Modulus Divider,* IEEE J. Solid-State Circuits **51**, 1771 (2016).

[49] K. Raczkowski, N. Markulic, B. Hershberg, and J. Craninckx, *A 9.2–12.7 GHz Wideband Fractional-N Subsampling PLL in 28 nm CMOS With 280 fs RMS Jitter,* IEEE J. Solid-State Circuits **50**, 1203 (2015).

[50] M. R. Ahmadi, D. Pi, B. Catli, U. Singh, B. Zhang, Z. Huang, A. Momtaz, and J. Cao, *A 288fs RMS jitter versatile 8–12.4 GHz wide-band Fractional-N synthesizer for SONET and SerDes communication standards in 40nm CMOS,* in *IEEE VLSI Circuits Symp. Tech. Papers* (2013) pp. C160–C161.

[51] C. Venerus and I. Galton, *A TDC-Free Mostly-Digital FDC-PLL Frequency Synthesizer With a 2.8–3.5 GHz DCO,* IEEE J. Solid-State Circuits **50**, 450 (2015).

[52] C.-H. Lee, L. Kabalican, Y. Ge, H. Kwantono, G. Unruh, M. Chambers, and I. Fujimori, *A 2.7 GHz to 7 GHz Fractional-N LC-PLL Utilizing Multi-Metal Layer SoC Technology in 28 nm CMOS,* IEEE J. Solid-State Circuits **50**, 856 (2015).

[53] A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, *A 3.7 mW Low-Noise Wide-Bandwidth 4.5 GHz Digital Fractional-N PLL Using Time Amplifier-Based TDC,* IEEE J. Solid-State Circuits **50**, 867 (2015).

[54] M. Ho, K. N. Leung, and K.-L. Mak, *A low-power fast-transient 90-nm low-dropout regulator with multiple small-gain stages,* IEEE J. Solid-State Circuits **45**, 2466 (2010).

[55] S. Levantino, G. Marzin, C. Samori, and A. L. Lacaita, *A wideband fractional-N PLL with suppressed charge-pump noise and automatic loop filter calibration,* IEEE J. Solid-State Circuits **48**, 2419 (2013).

[56] W. S. Titus and J. G. Kenney, *A 5.6 GHz to 11.5 GHz DCO for digital dual loop CDRs,* IEEE J. Solid-State Circuits **47**, 1123 (2012).

[57] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, *A low-noise wide-BW 3.6-GHz digital fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation,* IEEE J. Solid-State Circuits **43**, 2776 (2008).

[58] C. Niclass, K. Ito, M. Soga, H. Matsubara, I. Aoyagi, S. Kato, and M. Kagami, *Design and characterization of a 256x64-pixel single-photon imager in cmos for a mems-based laser scanning time-of-flight sensor,* Optics Express **20**, 11863 (2012).

[59] C. Niclass, M. Soga, H. Matsubara, S. Kato, and M. Kagami, *A 100-m range 10-frame/s 340×96-pixel time-of-flight depth sensor in 0.18-µm cmos,* IEEE J. Solid-State Circuits **48**, 559 (2013).

[60] N. A. Dutton, S. Gnecchi, L. Parmesan, A. J. Holmes, B. Rae, L. A. Grant, and R. K. Henderson, *11.5 a time-correlated single-photon-counting sensor with 14gs/s histogramming time-to-digital converter,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2015) pp. 1–3.

[61] T. Al Abbas, N. A. Dutton, O. Almer, N. Finlayson, F. M. Della Rocca, and R. Henderson, *A cmos spad sensor with a multi-event folded flash time-to-digital converter for ultra-fast optical transient capture,* IEEE Sensors J. **18**, 3163 (2018).

[62] H. Mizuno and K. Ishibashi, *A noise-immune ghz-clock distribution scheme using synchronous distributed oscillators,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (1998) pp. 404–405.

[63] V. Gutnik and A. P. Chandrakasan, *Active ghz clock network using distributed plls,* IEEE J. Solid-State Circuits **35**, 1553 (2000).

[64] F. O'Mahony, C. P. Yue, M. A. Horowitz, and S. S. Wong, *A 10-ghz global clock distribution using coupled standing-wave oscillators,* IEEE J. Solid-State Circuits **38**, 1813 (2003).

[65] L. Cho, F. Kuo, R. Chen, J. Liu, C. Jou, F. Hsueh, and R. B. Staszewski, *A 4ghz clock distribution architecture using subharmonically injection-locked coupled oscillators with clock skew calibration in 16nm cmos,* in *2017 Symposium on VLSI Circuits* (2017) pp. C130–C131.

[66] J.-C. Chien and L.-H. Lu, *Analysis and design of wideband injection-locked ring oscillators with multiple-input injection,* IEEE J. Solid-State Circuits **42**, 1906 (2007).

[67] C. Verhoeven, *A high-frequency electronically tunable quadrature oscillator,* IEEE J. Solid-State Circuits **27**, 1097 (1992).

[68] S. A. Ahmadi-Mehr, M. Tohidian, and R. B. Staszewski, *Analysis and design of a multi-core oscillator for ultra-low phase noise,* IEEE Transactions on Circuits and Systems I: Regular Papers **63**, 529 (2016).

[69] R. Adler, *A study of locking phenomena in oscillators,* Proceedings of the IRE **34**, 351 (1946).

[70] B. Razavi, *A study of injection locking and pulling in oscillators,* IEEE J. Solid-State Circuits **39**, 1415 (2004).

[71] A. Demir, A. Mehrotra, and J. Roychowdhury, *Phase noise in oscillators: A unifying theory and numerical methods for characterization,* IEEE Trans. Circuits Syst. I **47**, 655 (2000).

[72] A. Demir, *Floquet theory and non-linear perturbation analysis for oscillators with differential-algebraic equations,* International journal of circuit theory and applications **28**, 163 (2000).

[73] P. R. Gray, P. Hurst, R. G. Meyer, and S. Lewis, *Analysis and design of analog integrated circuits* (Wiley, 2001).

[74] A. Hajimiri, S. Limotyrakis, and T. H. Lee, *Jitter and phase noise in ring oscillators,* IEEE J. Solid-State Circuits **34**, 790 (1999).

[75] H.-C. Chang, X. Cao, U. K. Mishra, and R. A. York, *Phase noise in coupled oscillators: Theory and experiment,* IEEE Trans. Microw. Theory Techn. **45**, 604 (1997).

[76] A. R. Ximenes, P. Padmanabhan, and E. Charbon, *Mutually coupled ring oscillators for large array time-of-flight imagers,* in *International Image Sensor Workshop (IISW) 2017* (IISS, 2017) p. R25.

[77] M.-J. Lee, A. R. Ximenes, P. Padmanabhan, T.-J. Wang, K.-C. Huang, Y. Yamashita, D.-N. Yaung, and E. Charbon, *High-performance back-illuminated three-dimensional stacked single-photon avalanche diode implemented in 45-nm cmos technology,* IEEE J. Sel. Topics Quantum Electron. **24**, 1 (2018).

[78] L. H. Braga, L. Pancheri, L. Gasparini, M. Perenzoni, R. Walker, R. K. Henderson, and D. Stoppa, *A cmos mini-sipm detector with in-pixel data compression for pet applications,* in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2011 IEEE* (IEEE, 2011) pp. 548–552.

[79] C. Veerappan, J. Richardson, R. Walker, D.-U. Li, M. W. Fishburn, Y. Maruyama, D. Stoppa, F. Borghetti, M. Gersbach, R. K. Henderson, *et al.*, *A 160× 128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2011) pp. 312–314.

# 5

# PIXEL COMBINATION WITH SOURCE PRESERVATION

*Truth comes out of error more*
*readily than out of confusion.*

Francis Bacon, 1st Viscount St Alban

*Resource sharing is one of the main challenges in direct time-of-flight imaging. Timing information, differently than voltage/charge, cannot be stored for later conversion and should treated as soon as possible, avoiding signal deterioration. Different approaches have been proposed to solve such issue, however, power consumption and conversion rate limit their use in noisy environments. In this chapter, the power consumption of different topologies and operational modes are investigated, relating the impact of resource sharing structures on the sensor sensitivity, taking also event-driven operation into account. A solution for an edge-sensitive signal selection, as well as its impact on signal sensitivity, is obtained.*

## 5.1. INTRODUCTION

DIRECT time-of-flight imaging requires precise timing measurements that are typically difficult to achieve in large arrays. The main reason is that, differently than charge or voltage, timing information cannot be stored. In RGB image sensors, the pixels translate the incoming photons into voltage or charge, which are, sequentially, converted into digital binary words by common column-based ADCs, by selecting the pixels that connect to the vertical buses. Following a similar approach in dTOF imaging systems can lead to signal degradation, sensitivity reduction, pile-up distortions, and desensitization when operating under strong background illumination noise.

Since the timing cannot be stored directly, it is essential to convert it into another parameter as soon as possible. Since computers operate in the digital domain, ultimately the timing response of the pixels would need to be converted into digital words. This can be done directly, via time-to-digital converters (TDCs) [1], or by using an intermediate parameter, typically voltage, via time-to-amplitude converters (TACs) [2], then eventually converting it to digital domain via ADCs.



However, as array sizes becomes larger, the conversion rate bottleneck of column-wise topologies becomes evident, requiring a higher level of parallelism on-chip. As a response for such demand, the introduction of SPAD devices in deep-submicron CMOS have enabled the design of arrays where the entire photon detection and TOF circuitry is integrated on-pixel [3–5]. Such sensors operate under event-driven mode, shutting down the timing detection in the absence of photons and, consecutively, reducing the overall power consumption. This approach is indeed very power efficient, however, it is only practical under the photon-starving mode, once the presence of high background noise could increase the activity of the sensor, potentially impacting the overall power consumption, and causing serious operational issues due to high and variable IR-drop.

For an optimal design, it is essential to obtain the power consumption of the timing generation and acquisition with respect to the sensor activity, while comparing the conversion rate capabilities of different dTOF approaches.

This chapter is organized as follows. In Section 5.2, the power consumption of different pixel/TDC configuration is analyzed, as well as the sensitivity degradation caused by the sharing structures. An optimum pixel configuration, taking these constraints, is also discussed. In Section 5.3, a proposed binary arbiter tree, which is capable to organize and select multiple simultaneous events in different pixels, while preserving the event source, is introduced. The goal is to provide a modular architecture that can be used to build large arrays, without compromising performance. Finally, Section 5.4 concludes this Chapter.

## 5.2. SHARING APPROACH

Due to the high sensitivity of dTOF imaging systems with respect to timing, it is essential to convert the pixel response into digital words as quick as possible. These requirements, along the practicality of deep-submicron CMOS, allowed the implementation of per-pixel TDC [3–5], as an alternative to shared, column-wise architectures [1]. However, it is important to understand the implications of such architectures on signal quality, and to analyze the operation with respect to sensitivity and power consumption. The main issue with event-driven approaches is that, under different levels of illumination, the power consumption

can vary drastically, producing an unpredictable IR-drop on the TDC power lines. This variation can substantially alter the TDCs performances, incurring in large errors that cannot be compensated for. Foreground calibration can therefore be performed, by estimating the instantaneous TDC resolution, however, it requires elaborate sampling structure and post-processing calibration, which can slows down the system frame-rate and increase the post-processing power consumption.

Any event-driven system behaves similarly, although in column-wise TDCs, the power distribution can be better designed than in a per-pixel TDC, since they are outside the sensitive area and more robust connections can be realized, as well as low-dropout (LDO) regulators. It also allows the implementation of a reference PLL block, whose phases can be distributed to local interpolation TDCs, being more robust to PVT variations [1, 6]. Alternatively, always-on TDC can also be used, which helps with the sensitivity and IR-drop variation, but at higher power consumption cost.

Next, the power analysis and sensitivity degradation of event-driven approaches (per-pixel TDC and shared, column-wise TDC) compared to always-on TDCs, shared among several pixels, is performed.



### POWER CONSUMPTION

Event-driven approach is believed to consume the least energy among dTOF imaging systems. However, it largely depends on the sensor activity, since it might be more efficient to share an always-on TDC with multiple pixels, than to operate multiple TDCs for shorter times. Thus, the power consumption requiring for the timing acquisition must be derived.

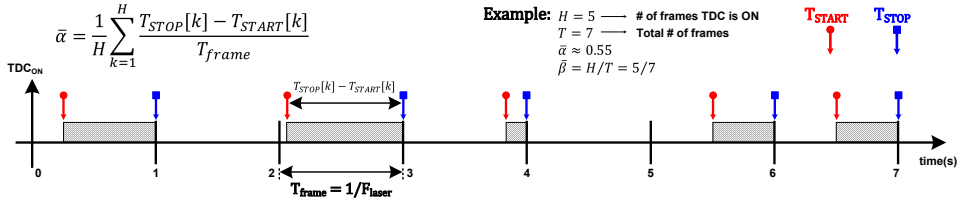



Figure 5.1: Time diagram example of a single TDC in event-driven mode.

Figure 5.1 introduces the concepts used throughout this chapter. The first parameter, $\overline{\alpha}$, provides the average time a particular TDC stays activated. For example, in a noiseless system, $\overline{\alpha}$ would assume a value that corresponds roughly to the location of the target, with respect to the time frame, whereas in a noisy environment, it might assume a value closer to the middle point ($\overline{\alpha} \approx 0.5$), which is the average value of a uniformly distributed variation (since noise in uncorrelated to the time frame). The presence of the signal might shift $\overline{\alpha}$ from the middle point, depending on its intensity compared to the noise. The second parameter, $\overline{\beta}$, is the average activity rate of one pixel, normalized to the laser frequency ($F_{laser}$). If the TDC is activated in all time frames, $\overline{\beta}$ is one, otherwise it assumes a value that indicates how often a TDC is used.

Another interpretation of $\overline{\alpha}$ and $\overline{\beta}$ is that, their product indicates the duty cycle of a TDC, so its power consumption can be calculated. In this short observation of Figure 5.1, the TDC duty cycle is about 39.3% ($\overline{\alpha} \cdot \overline{\beta}$), although longer observation would be required

to obtain such parameters. To be more generic, including the possibility of sharing a single TDC with multiple pixels ($M$), its duty cycle can be written as $\overline{\alpha} \cdot min(\overline{\beta} \cdot M, 1)$, where any pixel could start the TDC, to a limit of activity equals to one.

The total power consumption to generate a timing reference, on chip, can be generically given by a composition by the PLL power consumption ($P_{PLL}$), including all necessary reference buffers, etc., and the dynamic power used on the distribution of multiple PLL phases, thus to be used as fine resolution for interpolative TDC. The number of phases and the frequency will depend on the system architecture. Normally, multiple phases are distributed and used as reference for the local TDCs, in both, column-wise [6] and per-pixel TDC approaches [7]. The power consumption associated with the reference is given by:

$$P_R = P_{PLL} + \#p \cdot C_{line} \cdot V^2 \cdot F. \tag{5.1}$$

The second term refers to the dynamic power consumed in the distribution of multiple ($\#p$), high frequency ($F$) PLL phases, over capacitive wires ($C_{line}$), with voltage swing $V$.

An event-driven TDC starts to operate upon the arrival of a photon and it is stopped by the end of the time frame. Instead of providing a time-frame value, that can be the inverse of the laser frequency ($F_{laser}$) or shorter, we prefer to define the power consumed by a certain TDC based on its duty cycle. In order to do that, two parameters were created, $\overline{\alpha}$ and $\overline{\beta}$. The former, provides an average time a particular TDC stays on, whenever it operated. The latter, defines the activity rate, normalized to the laser frequency ($F_{laser}$). For instance, in the absence of noise, $\overline{\alpha}$ will carry a value that positions the target within the time frame, while in a noisy environment, $\overline{\alpha}$ tends to 0.5 (which is the mean value of a uniformly variation, such as the uncorrelated noise). $\overline{\beta}$, on the other hand, is defined depending on how many events occurred, per laser time frame (which can be larger than 1). If a TDC is shared among $M$ pixels, the compounded activity ($\overline{\beta} \cdot M$) should be used, limited to 1 (the TDC can only be activated once per time frame). Thus, the total power consumption over $N$ TDCs within the sensor is given by:

$$P_{TDC} = \overline{\alpha} \cdot P_{TDC} \cdot N \cdot min(\overline{\beta} \cdot M, 1). \tag{5.2}$$

Finally, in case a single TDC is shared, the power consumption necessary to process such events will depend on the absolute compounded activity of $M$ pixels ($\beta \cdot M \cdot F_{laser}$), limited by the dead time of the combination circuit ($\tau$), and the energy consumed for each event propagation, such as:

$$P_{COMB} = E_{comb} \cdot N \cdot min(\overline{\beta} \cdot M \cdot F_{laser}, \tau^{-1}). \tag{5.3}$$

The total power consumption is given then by the combination of (5.1), (5.2), and (5.3), as:

$$\begin{aligned} P_T = P_{PLL} + \#p \cdot C_{line} \cdot V^2 \cdot F + \overline{\alpha} \cdot P_{TDC} \cdot N \cdot min(\overline{\beta} \cdot M, 1) \\ + E_{comb} \cdot N \cdot min(\overline{\beta} \cdot M \cdot F_{laser}, \tau^{-1}). \end{aligned} \tag{5.4}$$

A combination circuit is necessary in case of sharing structures, so the events in multiple pixels can be processed by the TDC, as sketched in Figure 5.2 (b) and (c). Thus, $E_{comb}$ is the energy consumed, per event, by such a combination circuit. $\tau$ is defined by the dead time

of the combination circuit, limiting the activity among $M$ pixels, and it will be discussed in the next Section. For a more direct comparison between both architectures, the power consumed by the PLL and on the distribution of its phases will be ignored.

The TDCs can operate in two different modes: event-driven or sampled (continuously running TDC). In per-pixel TDC (Figure 5.2 (a)) the TDCs typically operate in event-driven mode, turning on upon a photon event, and stopping by the end of the time frame [5]. In this case, $E_{comb}$ from (5.4)can be neglected (since the pixel is connected directly to the TDC), so the total power over $M$ pixels reduces to:

$$P_{T,per-pixel} = \overline{\alpha} \cdot P_{TDC} \cdot M \cdot min(\overline{\beta}, 1), \tag{5.5}$$

where the number of pixels sharing a TDC is one and $N$ is replaced by $M$, to account for the total power over $M$ pixels ($M$ TDCs). Shared structures, such as Figure 5.2 (b) and (c), can operate either in event-driven and sampled modes. For event-driven, the power consumption of $M$ pixels reduces to:

$$P_{T,shared\_event-driven} = \overline{\alpha} \cdot P_{TDC} \cdot min(\overline{\beta} \cdot M, 1) + E_{comb} \cdot min(\overline{\beta} \cdot M \cdot F_{laser}, \tau^{-1}). \tag{5.6}$$

It is important to observe that, shared architectures that operate in event-driven mode are only viable for photon-starved regime, or in a scanning mode, where at each point in time, the TDC is not effectively shared, but dedicated to a single pixel [8] or it operates as a SiPM [9]. For this reason, this mode will not be considered further in this paper.

For the sampled approach, a continuously running TDC is shared among several pixels, as shown in Figure 5.2 (b) and (c). Different from a pure event-driven approach, upon an event in any of these pixels, the TDC samples a time, *i.e.* a timestamp is created and streamed through a first-in-first-out (FIFO) bus, along with the address of the detecting pixel. Multiple events can occur among those pixels, where the conversion time for the TDC itself is negligible, and the system saturation depends largely on the combination logic dead time.

Thus, from (5.4), the overall power consumption, related to the timing of $M$ pixels, is given by:

$$P_{T,shared\_sampled} = P_{TDC} + E_{comb} \cdot min(M \cdot F_{laser} \cdot \overline{\beta}, \tau^{-1}), \tag{5.7}$$

where, the first term is due to a continuously running TDC, and, the second term, the combination circuit power. It is relevant to observe that, independently of the activity ($\overline{\beta}$) or number of pixels sharing a TDC ($M$), the TDC stays on all the time, which indicates that its power consumption is at its maximum, yet constant. By separating the power grid of the TDC (s) from the rest of the circuit (including the combination circuits), it is expected a constant power drawn by the TDC (s), although the overall power can vary with activity.

Evidently, in the case where a PLL is present, the power consumption would be higher, as is the precision, introducing new quality variables into the comparison. Thus, by analyz-

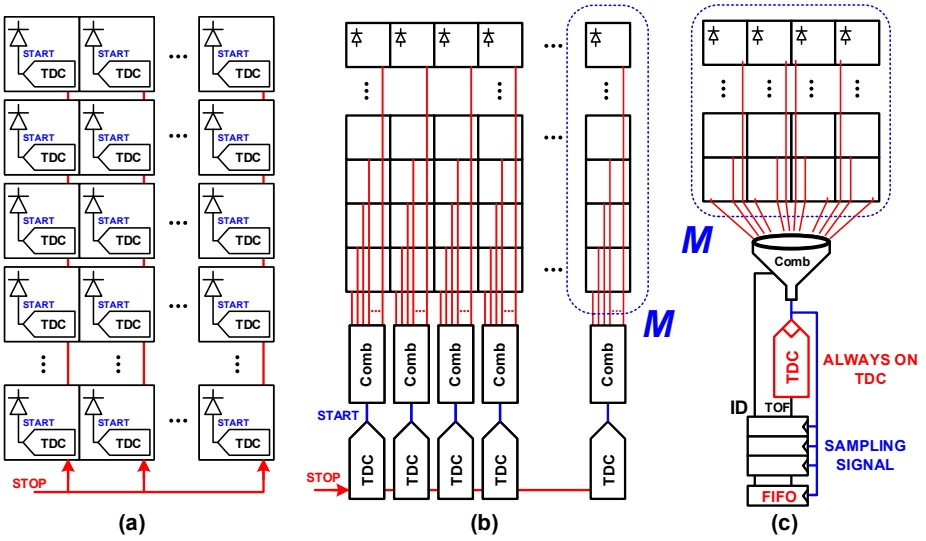



Figure 5.2: TDC arrangement. (a) Per-pixel, event-driven TDC; (b) Column-wise shared TDC; (c) Continuouly running, shared TDC concept.

ing (5.5) with (5.7), it is possible to obtain the following condition:

$$\begin{aligned} P_{T,per-pixel} &\geqslant P_{T,shared\_sampled} \\ \overline{\alpha}\cdot P_{TDC}\cdot M\cdot min(\overline{\beta},1) &\geqslant P_{TDC}+E_{comb}\cdot min(M\cdot F_{laser}\cdot\overline{\beta},\tau^{-1}) \\ \overline{\alpha}\cdot P_{TDC}\cdot M\cdot min(\overline{\beta},1) &\geqslant P_{TDC}+M\cdot E_{comb}\cdot min(F_{laser}\cdot\overline{\beta},(M\cdot\tau)^{-1}) \\ M &\geqslant \frac{1}{\overline{\alpha}\cdot min(\overline{\beta},1)-\left(\frac{E_{comb}\cdot min(F_{laser}\cdot\overline{\beta},(M\cdot\tau)^{-1})}{P_{TDC}}\right)} \end{aligned} \tag{5.8}$$

For the shared approach to offer better power efficiency than pure event-driven systems, the number of pixels sharing a single TDC, $M$, should satisfy (5.8).

### EFFECTS ON SENSITIVITY

The main drawback of sharing topologies is the inevitable chance of event collisions, specifically for signal photons, since they are close in time. The timing response of a target is a combination of the laser pulse width and the target depth variation. The target shape, the amount of pixels sharing a TDC, the disposition of these pixels (in a square or rectangle, in a column, in a row, etc.), and the laser pulse width will influence the collision probability in the combination circuit. Thus, to evaluate the sensitivity reduction of the sharing case, $\overline{\beta}$ can be modified following a non-paralyzable model [10, 11], that evaluates the probability of multiple event occurrences within the combination circuit dead time, which are not recorded, obtaining the effective average activity rate per pixel, such as:

$$\overline{\beta}_{shared} = \frac{\overline{\beta}}{1+M\cdot 1/T_{win}\cdot\overline{\beta}\cdot\tau} \tag{5.9}$$

where $T_{win}$ is the observation window, and $\tau$ the combination circuit dead time. In the arrangement of Figure 5.2 (c), $\tau = \Delta t_{comb} \cdot \log_2 M$, where $\Delta t_{comb}$ is the delay of each binary combination stage. All the uncertainties that would influence the timing reponse of the target can be incorporated into $T_{win}$, such as the laser pulse width and the target shape.

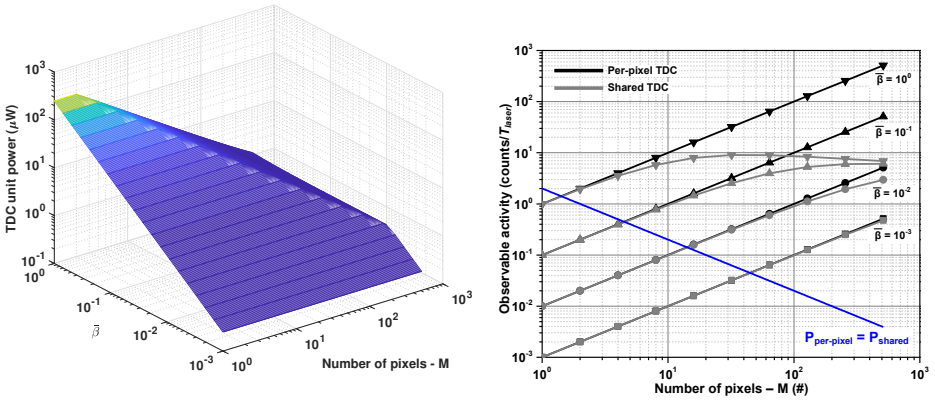
Although per pixel TDC does not suffer the aforementioned saturation, since each pixel is independent, the influence of noise can blind the pixels for the signal, by occupying the TDCs with noise events early on, in the time frame. Moreover, in conditions where background illumination is high (indoor/outdoor applications), and the probability of detecting noise is much higher than signal [12], time-correlated single-photon counting (TCSPC) [7] is generally needed, requiring higher statistics that event-driven architectures would take longer to provide (longer integration time/lower real frame rate). This way, in order to evaluate sensitivity, two different components should be analyzed: the effective average activity rate, limited by the dead time and observation window, and the maximum conversion rate.

As an example, if the following parameters are used: $F_{laser}$ = 1 MHz, for 150m LiDAR measurement, and $\overline{\alpha} \approx 50\%$ (0.5), since the target and/or background noise can arrive anytime within the measurement window (for ultra high background noise, $\overline{\alpha} \rightarrow 100\%$), the power consumption from the combination circuit can be estimated by the switching of $\log_2 M$ capacitors (rough estimation of ~1 fF per gate), in case of a simple OR-tree, thus $E_{comb} \approx 2 \cdot (1/2 \cdot C \cdot V^2) \cdot \log_2 M$.

For a typical TDC power consumption of 500 $\mu$W [13], the relation between power, number of pixels sharing a TDC, and the activity $\overline{\beta}$, is plotted in Figure 5.3 (a). Figure 5.3 (b) presents the maximum observable activity, when a signal width ($T_{win}$) of 5 ns (75 cm, as a combination of laser pulse width and target variation) and a dead time $\Delta t_{comb}$ of 80 ps are used (arbitrary value: shorter, for a simple logic gate; longer, for a flip-flop, in 65 nm CMOS technology, for example). The observable activity relates to the maximum number of detectable events per laser pulse, based on $\overline{\beta}$ and $M$ pixels. Since the event-driven approach can detect only a single event per time frame, the observable activity is the product of $\overline{\beta}$ and $M$ (black curves). However, for the shared approach, with continuously running TDC (column-wise or in a different arrangement), the inevitable dead time required by the combination circuit limits the maximum observable activity (gray curves). Intuitively, the more a single TDC is shared, the lower the power per pixel, but less photons the system can detect (for short observation). For long observations (time frame), the conversion rate of proposed method is inversely proportional to the dead time of the combination circuit, which can reach Gtimestamps/s (per $M$ pixels), whereas, the per-pixel TDC, the maximum conversion rate is still limited to $F_{laser}$ timestamps/s, per pixel.

LiDAR systems typically operate under low detection probability, unless it has a very narrow FOV, high intensity laser, or it is used for short ranges. According to (5.9), for the system conditions mentioned before, if $\overline{\beta}$ of about 10% (0.1) is considered for a group of 5 pixels or more, it is more power efficient to share a single TDC, than to have a per-pixel TDC. If 64 pixels share a single TDC [13], instead of 5, the power of such arrangement is 3.2x lower than that of a per-pixel TDC arrangement, however, it is only able to detect 62% of photons, for the 5 ns $T_{win}$ (see Figure 5.3). If the maximum conversion rate is considered (for activities not related to the laser itself, such as background light), the shared case is capable of 2 Gtimestamps/s (inverse of the combination circuit dead time, where $\tau = 80\text{ps} \cdot \log_2 64$) for the group of 64 pixels, or, on average, 32 Mtimestamps/s/pixel,

whereas a per-pixel approach, only a single conversion per time frame (1$\mu$s) is possible, thus a maximum of 1 Mtimestamps/s/pixel. The choice between shared or per-pixel TDC will depend on the system. For LiDAR, where high background noise is often present, increasing throughput at lower power is essential, favoring the shared approach.




(a) (b)

Figure 5.3: Relationship between power consumption, activity and number of pixels. (a) average power per TDC unit; (b) $\overline{\beta}$ compression due to combination dead time, within a laser pulse ($T_{laser}$) of 5 ns. Conditions above the blue line makes it more power efficient to share a TDC instead of a single TDC per pixel.

In conclusion, event-driven operation is the most power-efficient solution for photon-starved scenarios, where column-wise topologies operating in such conditions can offer even better power efficiency and precision, although lower conversion rate per pixel, especially for short bursts of photons (*i.e.*, in laser pulse width). Our proposed shared structure takes advantage of 3D-stacking technology, offering better power efficiency and higher conversion rate, when the activity in the sensor increases, as well as better silicon utilization (more area for on-chip signal processing and storage), enabling more intelligent sensors. Moreover, column-wise approaches can also be shared and operate continuously, where the TDC array could be coupled linearly (instead of in two dimensions, as proposed), and it is a viable alternative for monolithic implementations, where it benefits from the same advantages discussed in our proposed approach.

For these reasons, a sharing architecture for LiDAR is preferred. Furthermore, since camera-mode is required, where each detector matches a corresponding pixel in the final image, it is necessary to obtain, along with the timing information, the address (or ID) of the events. This is accomplished by a series of edge-sensitive binary arbiters, capable of symmetric connection to the pixels, which will be discussed next.

## 5.3. EDGE-SENSITIVE COMBINATION CIRCUIT

Most of the combination circuits that are used in dTOF sensors are based on simple logic gates, combining multiple events in a state-sensitive manner, typically with the use of pulse-

shrinking techiniques [14], or by time-multiplexing the pixels that share a TDC [8]. In the former case, there is no interest on which pixel generated the event, since it operates as an SiPM for PET application, where camera-mode is not necessary. On the latter, an specific TDC is shared by only few or one pixel, by means of operating different lasers in distinct regions of the sensor, so to avoid ambiguity, which can also be compromised if the sensor operate under strong background noise.

For a robust camera-mode system, it is essential to guarantee that each timing event acquired have a true correspondence with the originated pixel. This can be accomplished by two methods. Either a single pixel is select can operate at a certain time, in a scanning mode (which is more efficient by also scanning the laser), or by combining multiple pixels through a edge-sensitive circuit, by restricting the activity only to the first event, ignoring subsequent hits. Line scanning LiDAR accomplish the same goal by disregarding one of the dimensions and scanning the returning light as well as laser [15]. That is a different approach and requires more elaborated mechanical assembly, which is not the focus of this thesis.

With the goal of operating the dTOF imaging system in "flash" and camera-mode, it is then essential to obtain a combination circuit capable to detect events in an edge-sensitive manner, while being symmetric (no skew between inputs), avoiding calibration, and fast, in order to detect as many events as possible. Also, an architecture capable to also acquire, along the TOF, the address of which pixel generated the event is desirable, thus truly obtaining a one-to-one image correspondence.



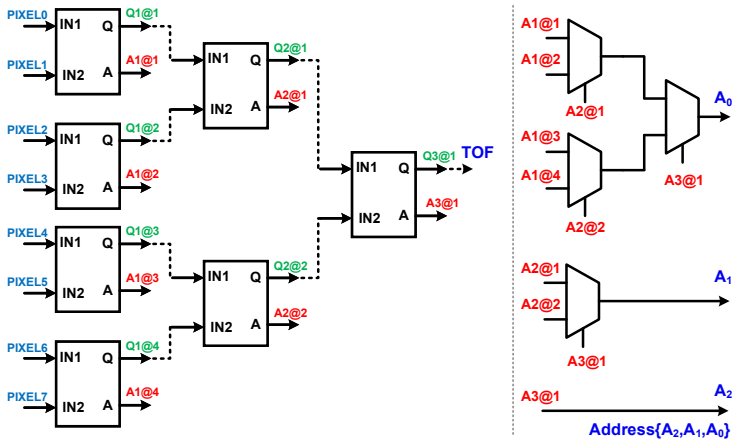



Figure 5.4: Conceptual decision tree. 8 pixels are combined to generate the TOF and 3-bit ID.

A conceptual solution is presented in Figure 5.4. It is called *decision tree* and it is based on *decision-makers*. The pixels are connected through a chain of binary arbiters, that decides which event occurred first, providing the same delay between any of the inputs to the output, while also providing an address word that tells which of the input is responsible for the event. The first level of decision-makers connect directly to the pixels, their outputs connect to the next level and so on, until a single output is generated, corresponding to the TOF plus the accumulated (fixed) delay of the decision tree. It is then used to sample the

TDC. The addresses are combined through a chain of multiplexers, where a digital binary word is ready available at the end of the process. It is then used to access a memory for timing information storage. More details are discussed at Chapter 6.

Moreover, it is more efficient to combine pixels in a power-of-two bases, for symmetry and full utilization of the address bits. The number of levels are given by $\log_2 M$, where $M$ is the number of pixels in the group. In the conceptual example given, 8 pixels are combined, thus requiring 3 levels of decision makers, and proving a 3-bit address output.

For this implementation, based on the best power efficiency/activity obtained in Section 5.2, the optimum number of pixels participating on the TDC sharing, throughout this thesis, is 64. Two arrangements where experimented with, one in a column of 2×32, and one in a square of 8×8 pixels. The reasons for these choices are discussed in Sections 5.3.1 and 5.3.2, respectively.

The concept shown in Figure 5.4 is very simple and for robust operation few modifications needed to be implemented. Firstly, since the tree is based on edge-sensitive elements, suggesting the use of flip-flops, it is necessary to reset the array after each event. This can be done by a self-resetting mode, which means that, at the end of each event, the output itself is delayed and used to reset the tree, maximizing the number of potential event detection. However, there are cases where a user is more interested in the first events, rather than the last, thus the self-reset can be disabled and the tree reset can be performed by an external signal, whenever it is necessary or wanted. Secondly, the address also require to be sampled, done by the same output signal, so events occurring during the reset phase does not disturb the ID/TOF correspondence. A more elaborated block diagram architecture is shown in Figure 5.5 .

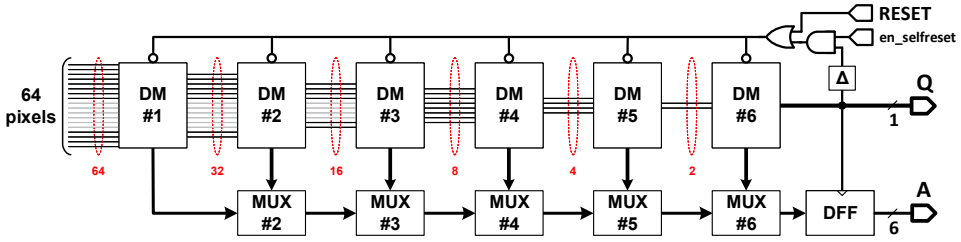



Figure 5.5: Decision tree used in this thesis, combining 64 pixels into one output.

As mentioned earlier, 64 pixels are connected to the first level of decision makers, which are connect subsequently until the generation of a 6-bit address and the Q output. The tree is reset by an external signal or by itself, in the end of the event propagation if configured this way. The multiplexers are digital standard cells, since no care with matching delays is necessary. The decision makers, however, require special design so to reduce metastability and delay variation between the inputs and will be discussed in the next sections. Two approaches to design the decision makers are used. In the first, due to area constraints, a minimum cell is done in the analog domain. In the second, to optimize the design for a more generic implementation, digital standard cells are used, with special structures for metastability mitigation.

### 5.3.1. ANALOG APPROACH

The core element of the proposed decision tree is the decision maker itself. Due to area, the first attempt was designed in an analog way, with the minimum area possible. The decision maker is shown in Figure 5.6. It is based on a modified true single phase clocking (TSPC) flip-flop [16], connected to each of the inputs, serving as the clock. The flip-flops outputs, q1 and q2, are feedback to the input of the cells, in order to block a possible event in the later input. The metastability of the circuit is reduced by the pMOS latch connected between q1 and q2, which slows down the late output, giving time for it to be reset by the early output. The outputs are also combined in a symmetric NOR gate, for symmetric output load and are used in a sense-amplifier flip flop (SAFF) [17], sampled by the output, which provides the address bit.

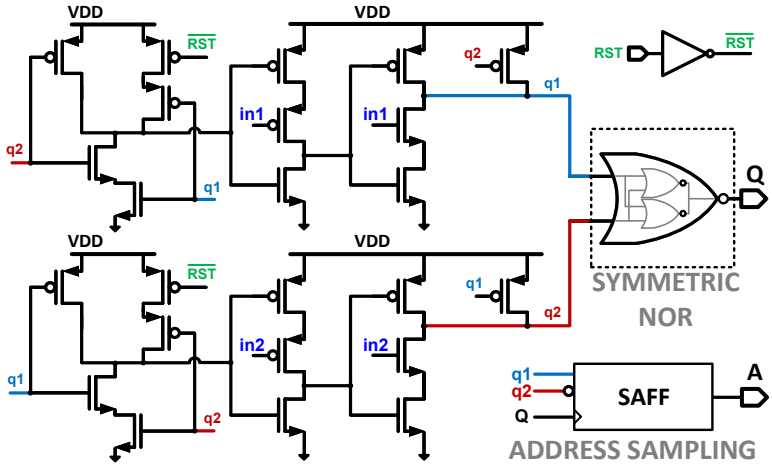



Figure 5.6: Analog approach for the decision maker.

This circuit has a major drawback, related to its dynamic behavior. Since it relies on the preservation of the charge on nodes q1 and q2, until the reset, potentially high leakage over the transistors can lead to a independent "natural" reset, not holding the information indefinitely as it is supposed to. Nevertheless, it is reset often due to high activity that it does not present as a major issue.

The chip was designed in a column base fashion, where each decision tree collects pixels from two columns, 16 columns apart, in a 2×32 way. The sensor contains 64×64 pixels, split into 4 quadrants, where one of the them is shown in Figure 5.7. There are several reasons for such arrangement of pixels and decision trees. The one more relevant, for the signal detection, regards the maximization of the probability of detecting multiple events within a single laser pulse, since by separating the pixels that participate on the decision group, it is more likely to avoid collisions between columns 15 and 31 (as the example) than neighboring columns. Other reasons are discussed on Section 6.2.

In this sensor, a 3D-stacking technology was used. It means that the quenching circuit, designed at Section 2.3.1, is also located on the bottom (processing) tier, thus requiring a symmetric and relatively wide connection between the SPADs and circuit, which is done

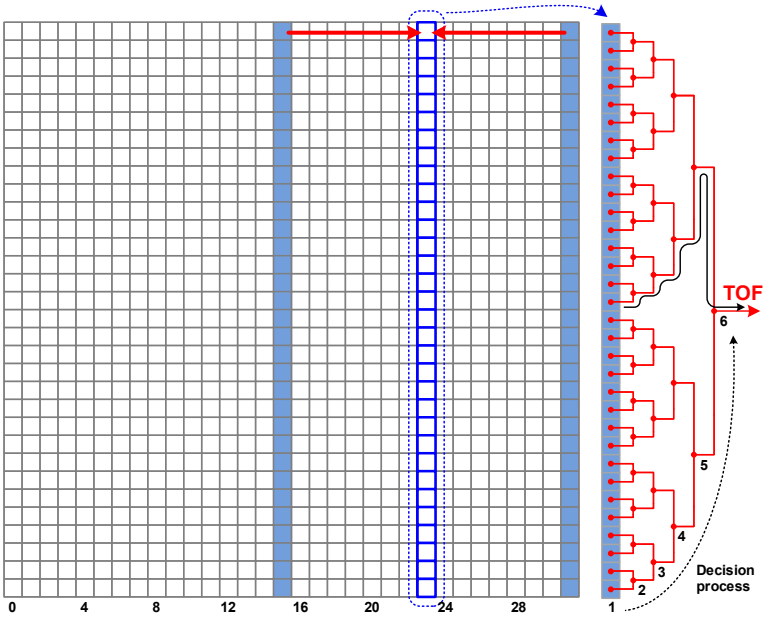



Figure 5.7: Decision flow performed in each column, within a quadrant. Decision tree connecting 2×32 pixels.

manually. The quenching circuit output interfaces with the decision tree by a simple wire connection with the first level of decision makers. Each column contains the quenching array, the decision tree, and a digital interface for pixel masking and energy (one bit activity) readout. The decision tree output (TOF of Figure 5.7) is then routed to the TDC sampling, which will described in Section 6.2.

### 5.3.2. DIGITAL APPROACH

The main drawback of the analog approach, described in Section 5.3.1, is the limitation in area imposed by the architecture, which compromises the design of several blocks, including the decision makers. Although the previous implementation fulfill the requirements of the dTOF system, problems in MOS leakage and sensitivity to supply variation limit their use in more stringent conditions. In order to improve the decision tree robustness, a more stable decision maker element is proposed. Based on digital standard cells, that use master-slave latches, its design follow the same operation condition of its analog counterpart, which is the selection the first event among the two inputs, propagating it with similar delay to the output, and generating an address bit.

The decision maker is shown in Figure 5.8 (a). It is based on two DFFs, one for each input. Upon an event in any of the inputs, the logic one is sampled, where the earlier DFF output resets the later one. The DFF outputs are connected together, through a symmetric OR-gate, to generate the output Q, equalizing the input load seen by the DFFs and the delay of each input to the output. The internal nodes feed also an SR-latch that generated the address A, identifying the event source. The early DFF output force-resets the late DFF,

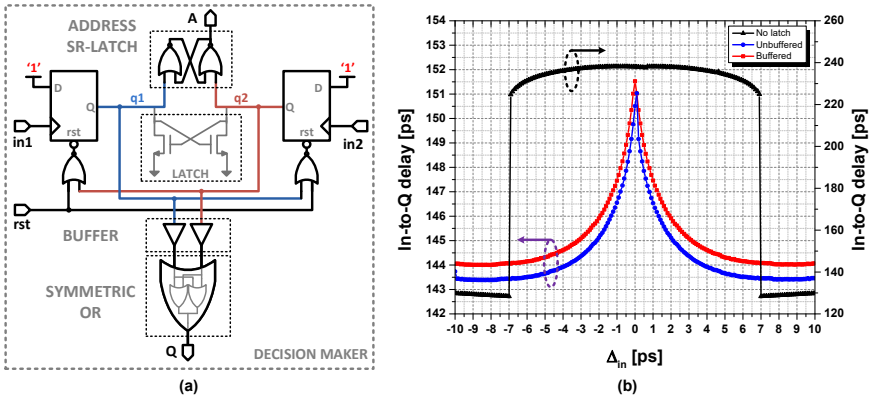



Figure 5.8: Digital approach for the decision maker: (a) schematic; (b) metastability window simulation, after parasitic extraction, with and without nMOS latch.

preventing it to fire after the detection of an early event. The whole structure is reset at the end by the signal **rst**, which can be generated by the tree itself, in the end of a event propagation, or from an external signal.

Although there is no metastability between the inputs, potential conflicts between the DFF outputs could cause propagation delay ($\tau_{in-to-Q}$) variations, affecting directly the timing. This issue is minimized through a nMOS latch placed between the DFF outputs, which reduces the delay variation from 120 ps to 7.5 ps (±5%) for similar window ($\Delta_{in}$ = ±7 ps), as it can be observed in the post-layout simulation in Figure 5.8 (b). In the final implemented circuit, the buffer between the DFF outputs and the symmetric OR gate is removed. The buffer was added to isolate the DFF outputs from the OR inputs, but since a symmetric OR is implemented, very little difference in the load is observed. Thus, from Figure 5.8 (b), very little difference between the use or not of such buffer is noticed, and, for area optimization, it was not implemented.

Differently from the previous approach, in this case, the group of pixels sharing a TDC were designed in a square shape, so is the decision tree. The implementation details and reasons for its choice are discussed in Section 6.3. The number of pixels participating on each decision tree is still 64 (in a 8×8 fashion), however, the decision makers are designed using mostly standard cells. The major benefit of such approach is a rapid design, with easier verification and integration with top level HDL description. In fact, the goal of such approach is to design a digital image sensor, with as little as possible manual design, improving reliability, efficiency, and speeding up the porting to new technologies.

The decision tree is composed by 6 levels of decision makers. Due to its edge-sensitive nature, it suffices to demonstrate the metastability of a single level, since the probability of having more than two events within such short window (±7 ps) is almost null, specially considering the timing response of the SPADs, in the order of tens or hundreds of picosecond. Nevertheless, in case of collisions, the delay added to the signal (7.5 ps) is much smaller than other sources of noise, such as the TDC quantization noise and SPAD timing jitter.

The arrangement of the decision makers is shown in Figure 5.9 (a). The disposition of the quenching circuit (connected directly under each SPAD) and the decision makers

are shown, where all pixels connections are symmetric to each other. Figure 5.9 (b) shows the numbering of pixels within the group, which is directly provided by the decision tree, through the address. The multiplexers and addresses connections are done through automatic place and route tools, in the digital domain, which speeds up the design, and it is not shown here.

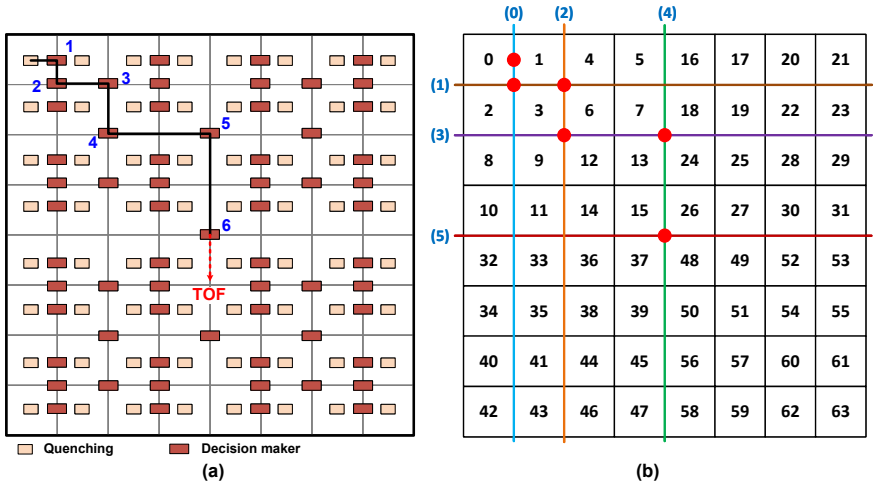



Figure 5.9: Decision flow performed in a group of 8×8 pixels: (a) quenching and decision maker placement; (b) pixel number with respect to digital address.

The design is done in 65 nm CMOS technology, where the delay of each decision maker is a combination of a DFF and a OR gate. Post-layout extraction provides a delay (also given by Figure 5.9 (b)) of about 150 ps, with minimum and maximum ranging from 100 to 250 ps, in different corners, confirmed by measurements results. Since the decision tree requires 6 levels of decision maker, a reset process takes about 150 ps, thus the decision tree dead time is in the order of 0.8 – 1.8 ns. Due to reason described in Section 6.3, the process has been delayed to about 2.4 ns, so other parts of the circuit (synchronized with the event) could meet timing constraints.

The total dead time of 2.4 ns indicates that the maximum conversion rate of about 420 Mevents/s ($1/\tau$), or 6.5 Mevents/pixel/s on average. Although the conversion rate is relatively high, limitation of timing information storage sets the maximum number of events each group can convert, or can store, for that matter. The dead time is also important to estimate the average activity rate ($\overline{\beta}$) compression, as calculated in Section 5.2. There are situations of high background noise that would require even higher conversion rate, which might not be feasible. Thus, it would require some background noise filtering, through spatial/temporal, for instance, as seen in Section 3.3, and introduced in [15, 18]. Nevertheless, the decision tree is capable of accomplish the edge-sensitive detection as required, while preserving the source of the event.

## 5.4. CONCLUSION

Generating a uniform timing reference, used for capturing telemetry and depth maps of large arrays of dTOF detector, is very challenging. Constraints on power consumption, area and technology (*e.g.* limited number of metal layers for proper power distribution) are some of the key limiting factors. Traditional approaches, such as PLL/DLL, are not typically applicable (due to area limitation and complexity), whereas column-wise arrangements [6, 19] and per-pixel TDCs [5, 7, 20] are limited to small arrays and photon-starved mode, respectively.

In this chapter, two approaches of dTOF operation, event-driven to an always-on, shared TDC topology, is analyzed, with respect to power consumption and area. From this investigation, supported by a systematic theoretical analysis and by a solid-state implementation, it is possible to conclude that, for most LiDAR applications, with moderate/high activity, the shared and sampled approach has a better power efficiency, with slightly lower saturation of the sensor, especially for short illumination bursts.

Thus, looking forward to sharing a single TDC with 64 pixels, an edge-sensitive combination circuit is proposed, called decision tree, whilst also preserving the source of the event, for camera-mode. Different approaches are implemented and used on the construction of two dTOF image sensors, discussed in details in Chapter 6.

## REFERENCES

[1] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, *A 128×128 single-photon image sensor with column-level 10-bit time-to-digital converter array,* IEEE J. Solid-State Circuits **43**, 2977 (2008).

[2] K. Maatta and J. Kostamovaara, *A high-precision time-to-digital converter for pulsed time-of-flight laser radar applications,* IEEE Trans. Instrum. Meas. **47**, 521 (1998).

[3] D. Stoppa, F. Borghetti, J. Richardson, R. Walker, L. Grant, R. K. Henderson, M. Gersbach, and E. Charbon, *A 32x32-pixel array with in-pixel photon counting and arrival time measurement in the analog domain,* in *IEEE European Solid-State Circuits Conference (ESSCIRC)* (2009) pp. 204–207.

[4] J. Richardson, R. Walker, L. Grant, D. Stoppa, F. Borghetti, E. Charbon, M. Gersbach, and R. K. Henderson, *A 32× 32 50ps resolution 10 bit time to digital converter array in 130nm cmos for time correlated imaging,* in *IEEE Custom Integrated Circuits Conference (CICC)* (2009) pp. 77–80.

[5] C. Veerappan, J. Richardson, R. Walker, D.-U. Li, M. W. Fishburn, Y. Maruyama, D. Stoppa, F. Borghetti, M. Gersbach, R. K. Henderson, *et al.*, *A 160× 128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2011) pp. 312–314.

[6] A. Carimatto, S. Mandai, E. Venialgo, T. Gong, G. Borghi, D. R. Schaart, and E. Charbon, *A 67,392-SPAD PVTB-compensated multi-channel digital sipm with 432 column-parallel 48ps 17b tdcs for endoscopic time-of-flight pet,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2015) pp. 1–3.

[7] F. Villa, R. Lussana, D. Bronzi, S. Tisa, A. Tosi, F. Zappa, A. Dalla Mora, D. Contini, D. Durini, S. Weyers, *et al.*, *Cmos imager with 1024 spads and tdcs for single-photon timing and 3-d time-of-flight,* IEEE J. Sel. Topics Quantum Electron. **20**, 364 (2014).

[8] C. Niclass, K. Ito, M. Soga, H. Matsubara, I. Aoyagi, S. Kato, and M. Kagami, *Design and characterization of a 256x64-pixel single-photon imager in cmos for a mems-based laser scanning time-of-flight sensor,* Optics Express **20**, 11863 (2012).

[9] T. Al Abbas, N. A. Dutton, O. Almer, N. Finlayson, F. M. Della Rocca, and R. Henderson, *A cmos spad sensor with a multi-event folded flash time-to-digital converter for ultra-fast optical transient capture,* IEEE Sensors J. **18**, 3163 (2018).

[10] G. F. Knoll, *Radiation detection and measurement* (John Wiley & Sons, 2010).

[11] S. H. Lee and R. P. Gardner, *A new g–m counter dead time model,* Applied Radiation and Isotopes **53**, 731 (2000).

[12] C. Niclass, M. Soga, and E. Charbon, *3d imaging based on single photon detectors,* in *2nd Symposium on Range Imaging (RIM'07)*, AQUA-CONF-2008-006 (2007).

[13] A. R. Ximenes, P. Padmanabhan, M.-J. Lee, Y. Yamashita, D. Yaung, and E. Charbon, *A 256× 256 45/65nm 3d-stacked spad-based direct tof image sensor for lidar applications with optical polar modulation for up to 18.6 db interference suppression,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (IEEE, 2018) pp. 96–98.

[14] L. H. C. Braga, L. Gasparini, L. Grant, R. K. Henderson, N. Massari, M. Perenzoni, D. Stoppa, and R. J. Walker, *A fully digital 8× 16 sipm array for pet applications with per-pixel tdcs and real-time energy output.* IEEE J. Solid-State Circuits **49**, 301 (2014).

[15] C. Niclass, M. Soga, H. Matsubara, S. Kato, and M. Kagami, *A 100-m range 10-frame/s 340×96-pixel time-of-flight depth sensor in 0.18-µm cmos,* IEEE J. Solid-State Circuits **2**, 559 (2013).

[16] J. Yuan and C. Svensson, *High-speed cmos circuit technique,* IEEE J. Solid-State Circuits **24**, 62 (1989).

[17] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu, and M. M.-T. Leung, *Improved sense-amplifier-based flip-flop: Design and measurements,* IEEE J. Solid-State Circuits **35**, 876 (2000).

[18] M. Perenzoni, D. Perenzoni, and D. Stoppa, *A 64×64-pixels digital silicon photomultiplier direct tof sensor with 100-mphotons/s/pixel background rejection and imaging/altimeter mode with 0.14% precision up to 6 km for spacecraft navigation and landing,* IEEE J. Solid-State Circuits **52**, 151 (2017).

[19] L. H. Braga, L. Pancheri, L. Gasparini, M. Perenzoni, R. Walker, R. K. Henderson, and D. Stoppa, *A cmos mini-sipm detector with in-pixel data compression for pet applications,* in *IEEE Nuclear Science Symp. and Medical Imaging Conf. (NSS/MIC)* (2011) pp. 548–552.

[20] F. Villa, R. Lussana, D. Tamborini, D. Bronzi, B. Markovic, A. Tosi, F. Zappa, and S. Tisa, *Cmos single photon sensor with in-pixel tdc for time-of-flight applications,* in *Time-to-Digital Converters (NoMe TDC), 2013 IEEE Nordic-Mediterranean Workshop on* (IEEE, 2013) pp. 1–6.

# 6

# MODULAR TOF SENSORS FOR LIDAR APPLICATIONS

*If everyone is moving forward together,*
*then success takes care of itself.*

Henry Ford

*In this chapter, the design of two different direct time-of-flight image sensors is described. In both cases, the sensors are designed in a modular fashion, with self-containing structures for an autonomous operation. Their difference lies in the design technique, where the first attempt uses a typical analogue approach, where every portion of the sensor is custom-designed and assembled manually in the analog environment, and the second, a proposed digital flow is introduced.*

Parts of this chapter have been published in [1].

## 6.1. INTRODUCTION

In previous chapters, several building blocks required for the design of a dTOF image sensor have been introduced. Here, these building blocks are used in the implementation of two sensor versions, following a similar approach, however, fundamentally different in their implementation. The goal of this thesis, and throughout this chapter, is to offer a modular array to serve as a self-containing element, so different future sensor sizes could be implemented without any major change in the design, just by plugging the blocks together.

The first design is done in a typical analogue approach, where each element in the dTOF signal path is custom designed, as well as the assembly on the top level. The data management and readout circuitry are digitally synthesized, but combined in the analog environment. The module contains a 64×64 effective pixel array, connected to TDCs and a readout integrated circuit. This module is relatively large and can be used as standalone.

In the second design, however, a completely different approach is proposed. Implemented mostly in the digital environment, only the very basic elements, that do not exist as standard cells, were custom-designed and characterized as a regular standard cell, so the digital tools could be used. The main advantages of such approach are the design time reduction, thorough verification, and the possibility of implementing more complicated functions, through RTL description. The unit module contains a 8×16 effective pixel array connected to a shared TDC, featuring *in-pixel* memory and *in-locus* signal processing.

In the following sections, both approaches will be described and characterization results will be provided for validation.



## 6.2. ANALOG APPROACH

The first design is part of a European project, entitled "pilot optical line for imaging and sensing (POLIS)" [2], with the goal, among many others, to develop and commercialize SPAD-based TOF sensors, for various applications, including biomedical imaging (PET and FLIM) and consumer/industrial LiDAR. The main project contributor was ST Microelectronics [3], and its relation with the work reported in this chapter, with regards the chip fabrication, including the first backside illumination SPAD detector in 65 nm CIS, the readout circuit in 40 nm CMOS, and the 3D-stacking, face-to-face bonding technologies.

As part of the initial target of the POLIS project, the goal was to develop a sensor capable to provide ranging information (depth measurements), and, at the same time, photon-counting (intensity), while maintaining the sensor granularity as unit, for the camera-mode operation. The main application is for mid-range LiDAR (5 – 30 m), although it was designed to support long-range (up to 200 m) measurements, for industrial robotics, consumer virtual/augmented reality (VR/AR), and potentially self-driving cars.

### 6.2.1. BLOCK DIAGRAM

The sensor is designed in a modular fashion, *i.e.* all the necessary components for an autonomous operation is contained within the module. The module is relatively large, as displayed in Figure 6.1. It contains 64×64 pixels, whose SPADs are designed in 65 nm CIS technology, introduced in Section 2.4.1, connected to a 40 nm readout integrated circuit on the bottom tier.

There are two types of pixels. One composed by a single large SPAD and another com-

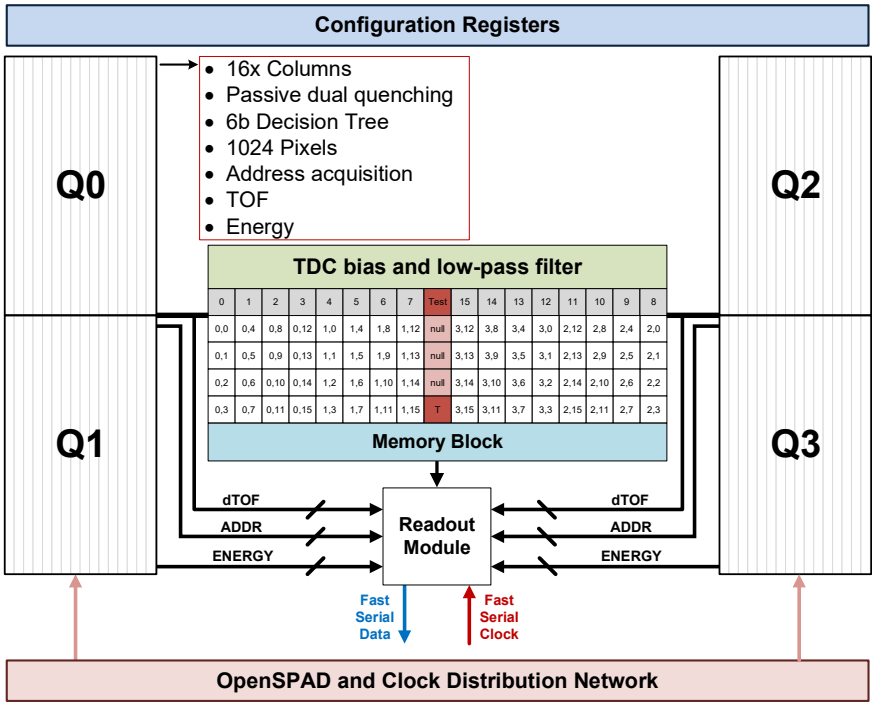



Figure 6.1: Block diagram of 64×64 depth sensing pixels, with shared TDC arrangement.

posed by 2×2 smaller SPADs, to form a similar pixel. The arrangement is shown in Figure 6.2. The two pixels have similar performance, as presented in Section 2.4.1, however, due to lower noise, the 2×2 smaller SPADs arrangement is preferred in future implementations. To maintain identical connection and operation in the bottom tier, the SPADs were connected with a metal wire at the top tier, and a single hybrid bonding connection is made. Since the bias voltage is the same for the whole array, some variation is expected in the final result, with respect to DCR and PDP, however, it is not enough to impact on the normal operation of the whole array.

The sensor is separated in quadrants, numbered from $Q_{0...3}$. Each quadrant contains 16 independent decision trees, where each collects events from 2 columns of pixels (2×32), generating a dTOF signal and an address. The dTOF signal is used to sample a TDC, located in the middle of the array and the ID is used to associate the timing information with the source of the event, keeping the granularity of the sensor as a single SPAD. Each TDC is shared among 4 different decision trees, by connecting a continuously running TDC to 4 different samplers. In total, there are 16 TDCs for TOF acquisition and an auxiliary TDC for calibration and range extension. A more detailed arrangement can be seen in Figure 6.3. The dTOF signal lines are equalized to reduce the skew between the pixels, where the residual offset can be easily calibrated out.

Apart from the timing information, an intensity measurement can also be performed through a series of bit adders, so the energy hitting the sensor can be acquired. This feature

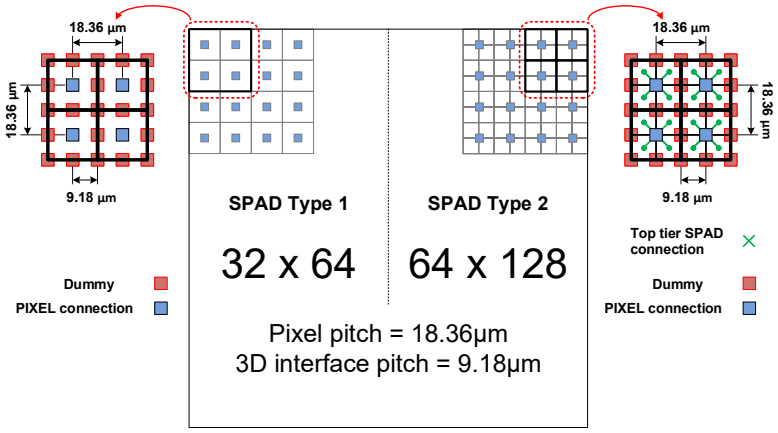



Figure 6.2: Different SPAD configuration, featuring large (18.36$\mu$m) and small (2x2 9.18$\mu$m) pixels.

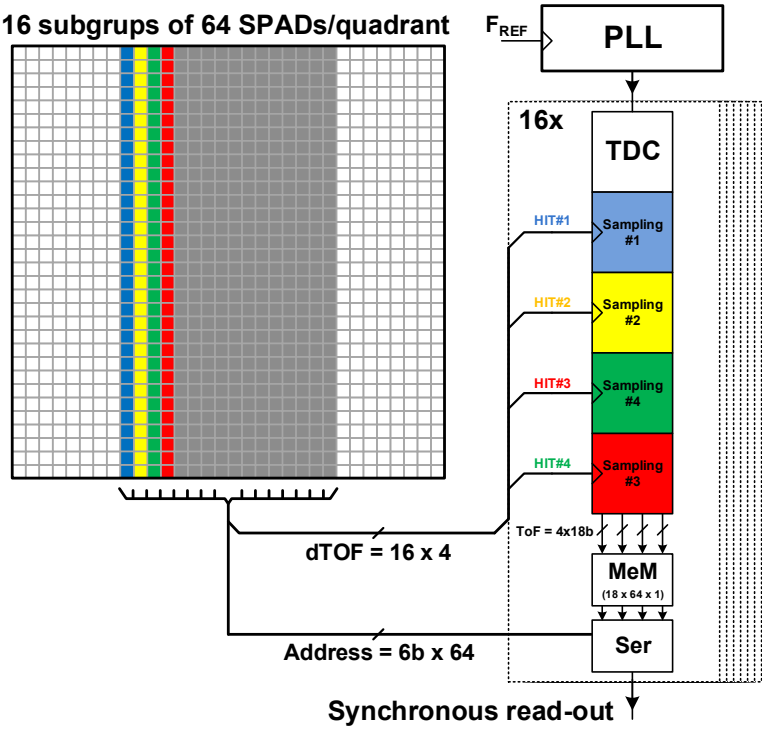



Figure 6.3: Shared TDC and sampler arrangement in one quadrant of the sensor.

is very useful for PET applications, where the total energy from an event is important to classify its quality, but can also be useful for a simultaneous LiDAR application, with dTOF + intensity sensor. These two modes are operated independently and can be simultaneously

accessed at any time.

The timing information from the TDC array is than managed and organized by a digital core, responsible to stream out the desirable information. The system operated under two clock domains, one slow for configuration and energy readout, and another fast, for data serialization. The maximum readout rate is in the order of 10 kfps, but it is often not necessary and operated in a slower rate to reduce power consumption.

### 6.2.2. TIME-TO-DIGITAL CONVERTER

The timing information is acquired using a time-to-digital converter. In this topology, a single TDC is shared among 4 groups of decision trees, each combining 64 SPADs. Each TDC is composed by a ring oscillator (RO) connected to a modified 10-bit gray counter. The RO is based on a 4-stage, pseudo-differential topology, shown in Figure 6.4. It contains "set" transistors that reset the RO phases when the TDC is eventually turned off, in a regular START/STOP operation. However, the proposed topology typically operates the TDCs continuously. The RO frequency and, consecutively the TDC resolution, is controlled by a current source and sink, which are controlled externally and heavily low-pass filtered by a local RC network. By controlling the frequency with both, current source and sink, the common-mode of the oscillation is kept almost constant, maintaining the sampler operation constant.

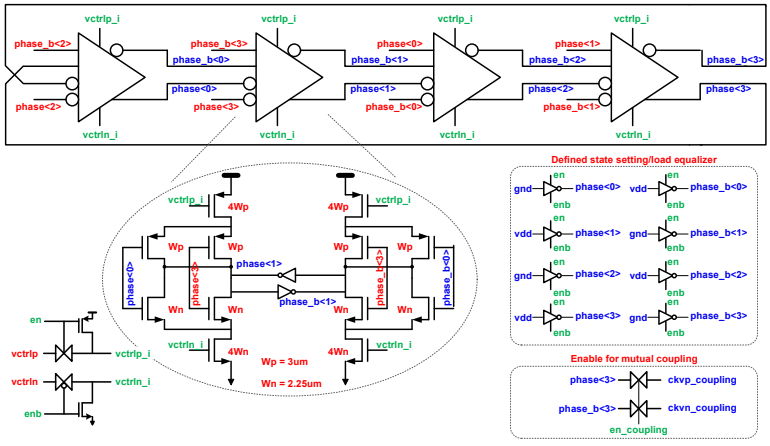



Figure 6.4: 4-stage, multi-path pseudo-differential ring oscillator.

In order reduce the overall frequency variation among the TDCs and to reduce the total integrated RMS jitter, the different TDC's RO are mutually coupled, being pushed to locking state, oscillating synchronously. The RO's can be connected to a common coupling line through a transmission gate. The RO coupling and monitoring structure can be seen in Figure 6.5. As seen in [4], by mutually coupling the TDCs, a much more robust reference generation can be obtained, while keeping the skew between the TDCs to a minimum, with lower phase noise and jitter.

The RO operates up to 4 GHz, thus providing a maximum resolution of 31.25 ps. Its phases can be directly connected to a sampler, typically a sense-amplifier flip-flop (SAFF)

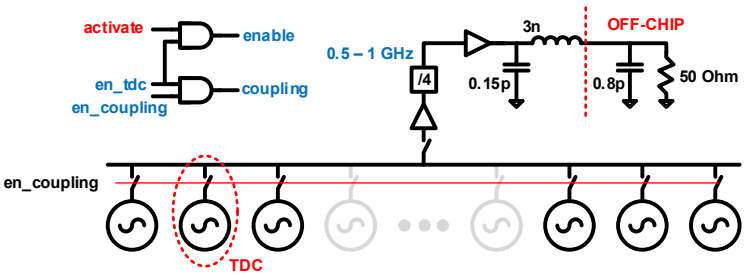



Figure 6.5: Mutually coupling TDCs with high-frequency monitoring structure.

[5]. A modified version of such SAFF is proposed and displayed in Figure 6.6 (b), where a passive interpolation can be obtained at the inputs of the SAFF (Figure 6.6 (a)), by accessing multiple phases of the RO with different strengths, effectively increasing the TDC resolution. The maximum interpolation is 2x, improving the resolution down to 15.625 ps.

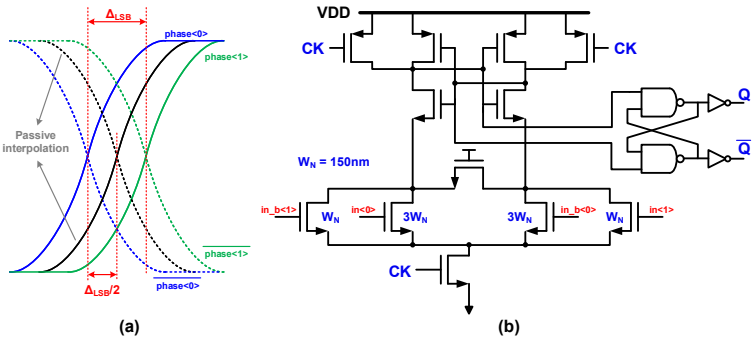



Figure 6.6: TDC phase sampling; (a) Passive interpolation; (b) Modified sense-amplifier flip-flop (SAFF) for passive interpolation.

The RO is then connected to a gray counter. In order to avoid excessive load at one specific RO phase, which would contribute to large non-linearity, a buffer interfaces the RO and counter. Its topology is based on a double push-pull structure, shown in Figure 6.7. It allows a current-reuse, reducing the power consumption on the buffer and the use of smaller devices, reducing its input load.

The buffered RO is then fed to a divider-by-2 structure, which phases are equalized and fed to the counter. It allows the counter to operate with lower input frequency, reducing its power consumption and increasing the operating margins. Nevertheless, the highest input frequency that is fed to the counter (about 2 GHz) sets very strict requirements to its architecture. Thus, the counter was developed minimizing the maximum path to a minimum. Its topolody is shown in Figure 6.8 (a).

The counter is split in 3 groups of 3-bit gray counter, which controls determine the operation of a specific group at each clock edge. In order to utilize all codes of the gray counter, every 8 counts ($2^3$ – 3 bits), two bits change, instead of a pure gray counter. An alternative is to reduce the usable codes, however, it would be only 70% of the codes, also

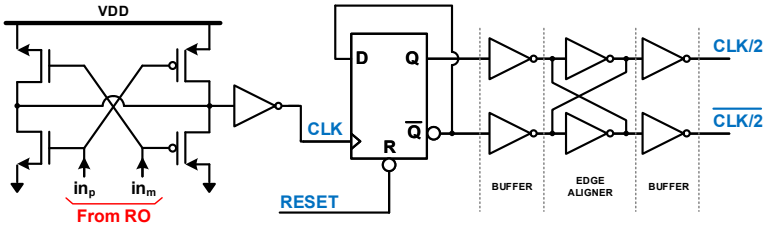



Figure 6.7: Differential to single-ended, double push-pull buffer and frequency divider-by-2.

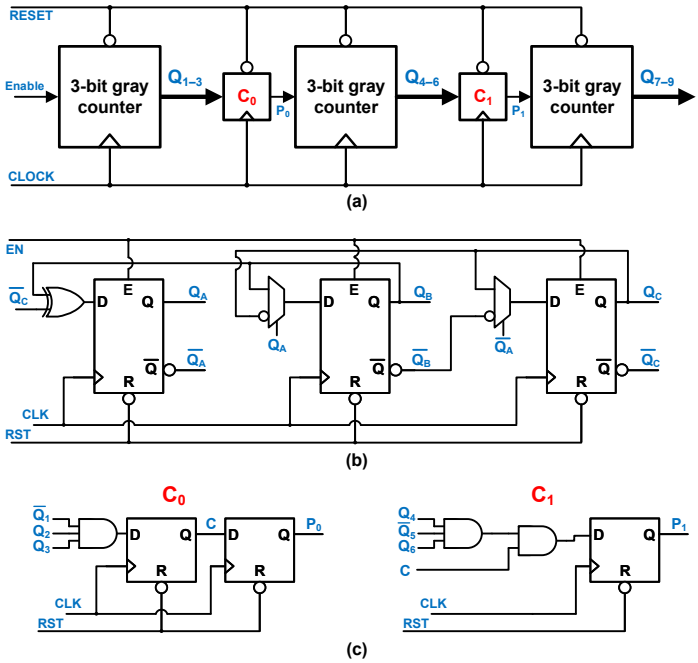



Figure 6.8: High-speed almost-gray counter; (a) Groups of 3-bit gray counters; (b) 3-bit gray counter schematic; (c) Connection logic between groups.

complicating the decoder (gray-to-binary). Each 3-bit counter is shown in Figure 6.8 (b), which control elements are shown in Figure 6.8 (c). This counter was coordinated by this thesis author and developed by a master's student, where more details can be found at [6].

The overall TDC array layout can be seen in Figure 6.9. It shows the 16+1 TDCs, samplers distribution and low-pass filter for the frequency control.

### 6.2.3. OPERATION

In each quadrant, two pixel columns, offset by 16 columns, are connected to a single decision tree, which is responsible to select and generate an dTOF signal, along with the address information, corresponding to the source of the event, as explained in the Chapter 5. In each frame, a single event per decision tree is obtained, to a total of 64 events in the whole sensor,

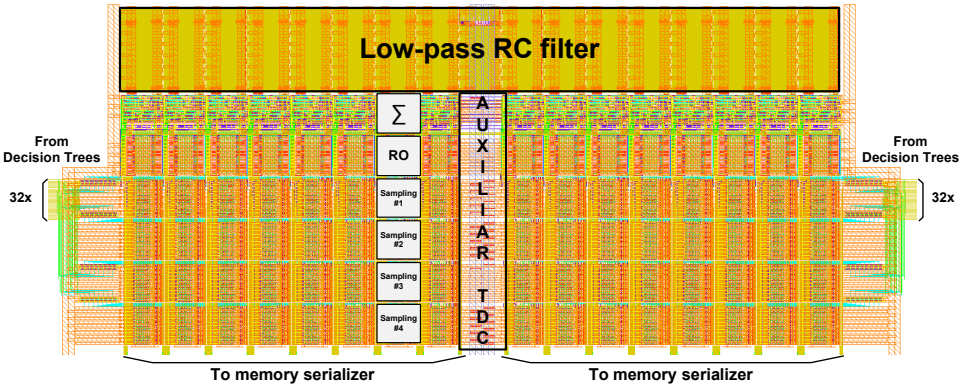



Figure 6.9: 16+1 TDC array layout.

which is then used to sample a particular TDC to generate a TOF information. A readout process is managed by the digital block, controlled by an external FPGA firmware, capable of selecting and arranged the data, which is then serialized out from the chip.

The TOF information is 14-bit long which is combined with a 6-bit address to for a 20-bit word, which totals to 1.28 kbits in a single readout. An auxiliary TDC is used to measure the instantaneous RO frequency (and resolution) of the TDC array, for a correct depth calculation. As mentioned before, all TDCs are mutually coupled and oscillate in the same frequency, reducing uncertainties due to PVT variations and eventual disturbances provokes by the sampling process.

The chip has two distinct clock domains: a slow clock, used during configuration, masking, calibration, and energy readout, and a fast clock, used only for fast data readout. In this way, the power consumption is minimized while the readout frame rate optimized. At the maximum speed, the chip can be read at 100kfps, using a 120 MHz clock, already taking into account start/stop words transmitted

### 6.2.4. CHARACTERIZATION

Figure 6.10 (a) shows the transfer function of the TDC array, along with its integral nonlinearity (INL). The worst-case INL was measured at -3.5 LSB, the differential nonlinearity (DNL) was measured ±0.6 LSB, where $\Delta_{LSB}$ is 15.6 ps. Figure 6.10 (b) shows the mutually coupling effect on the phase noise of the oscillators, which after coupling, compose a signal with integrated RMS jitter of 7.5 ps, at maximum frequency of 4 GHz, where the output frequency is divided by 4, for measurement purposes. The improvement on phase noise and jitter after mutual coupling follows the development in Section 4.3, which correspond to $10 \cdot \log(M)$, where $M$ is the number of oscillators coupled (17, in this case), to a total of about 12.3 dB improvement.

## 6.3. DIGITAL APPROACH

The second design is part of a Dutch project, entitled "L3SPAD: A Single-Photon, Time-Resolved Image Sensor for Low-Light-Level Vision" [7], with the goal of developing a low-

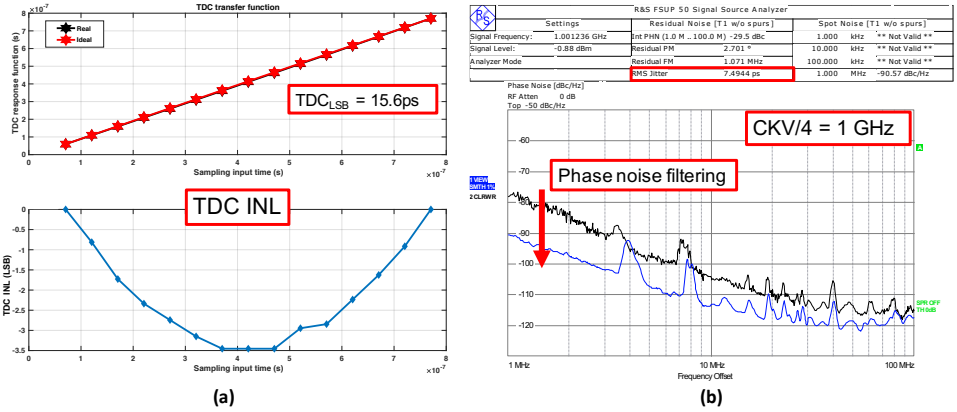



Figure 6.10: TDC characterization: (a) transfer function and INL; (b) coupling effect on phase noise.

light image system for night-vision, mainly for automotive LiDAR applications. The design has been fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) [8], which includes a backside illumination SPAD detector array in 45 nm CIS, and a readout circuit in 65 nm CMOS, using a 3D-stacking technology. The readout circuit is done completely in the digital flow, speeding up the design time and enabling a higher level of functionality.

The most elementary blocks were designed to match the placement grid of the technology standard cells, which were characterized and used in the digital flow. Cadence® and Synopsys® tools are capable to generate power and timing libraries for the digital flow optimization. This procedure minimizes the design time, which typically requires high levels of analog verification that slows the design process, allowing a more efficient implementation, while increasing reliability. The only cells that were custom-designed are the passive quenching, presented in Section 2.3.2, the decision maker, presented in Section 5.3, and a 1-bit SRAM memory used in the memory banks. The TDC is the largest and most complicated block in the system and is also custom-designed and placed as a MACRO. Its design is presented in this Section. Everything else, including *in-locus* signal processing, has been done using the digital flow, by means of RTL description.

In the next sections, the basic architecture and arrangements will be discussed in more details, with experimental results in the end.

### 6.3.1. BLOCK DIAGRAM

As discussed in Chapter 5, there are advantages and disadvantages between event-driven and sampled approaches. Since in the target application the activity is relatively high, a continuously running TDC is favored. Thus, at the core of the proposed architecture lies a continuously running TDC. In order to reduce the overall power consumption, each TDC is shared among several pixels, through a series of edge-sensitive decision makers, as discussed in Chapter 5. By arranging the decision tree in a symmetric way, the sampling signal is generated by the pixels with virtually zero skew between them. At the same time, the source of the event is tracked, maintaining the sensor granularity to a single SPAD. The block diagram of the system is displayed in Figure 6.11 (c).

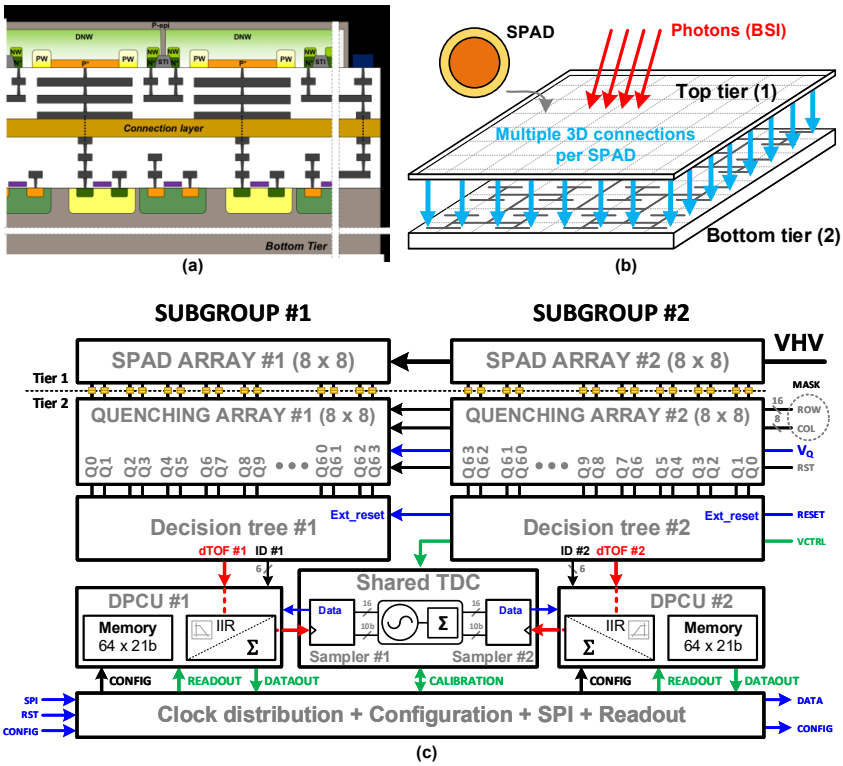



Figure 6.11: Proposed digital module implementation: (a) 3D-stacking cross-section; (b) perspective view; (c) block diagram – 2 subgroups of 8 x 8 pixels (SPADs), shared TDC, *in-locus* processing (DPCU), and memory.

The trade-offs of sharing structures, such as the proposed one, regards two parameters: the power consumption, per pixel, and total dead time, which implicates on the saturation of the sensor, specially for short bursts of events, typical of the returning light from the target, originated by a short, pulsed laser source. The more pixels a single TDC is shared with, the lower the power consumption, but longer the dead time and, consecutively, lower saturation level. Thus, this choice will depend on the application, external conditions (such as target distance and reflectivity, laser pulse width, etc.) and sensor technology, since monolithic implementations might impose more restrictions on the maximum number of sharing pixels if compared to recently available 3D-stacked technology.

According to the developments in Chapter 5, for the expected activity and power consumption, each TDC is shared among 128 pixels, divided into two independent subgroups of 64 pixels (8×8 pixels). The subgroup size was chosen in order to maintain a good compromise between conversion rate and power consumption [4]. Figure 6.11 shows the block diagram of each subgroup. They are composed by a decision tree, responsible to manage multiple events across the pixels, generating a sampling signal, dTOF, and an ID. dTOF acquires the TDC timestamps, while the ID is used as a pointer for the *in-pixel* memory. This arrangement constitutes a module; it is digitally synthesized and it is capable of operating

autonomously, only being accessed during readout.

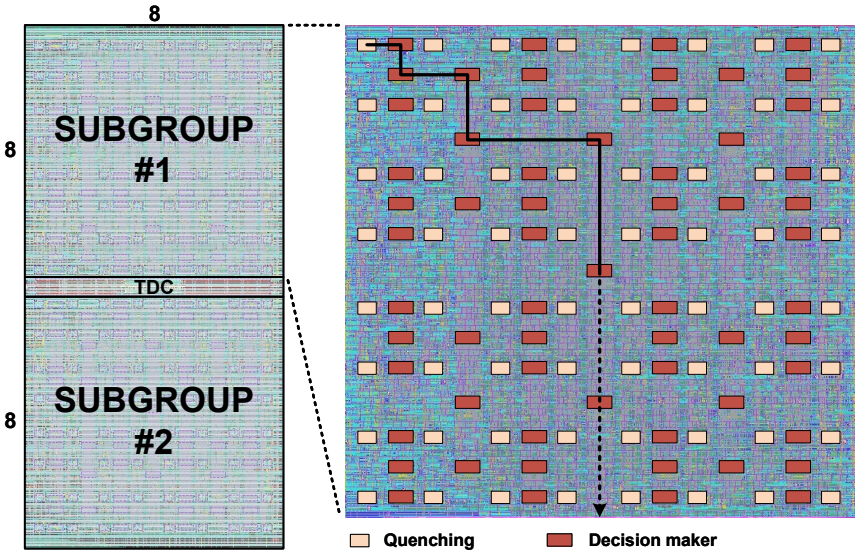



Figure 6.12: Passive quenching, decision makers and TDC location, in the digital flow.



Although the design has been done using the digital flow, some elements and signals are more sensitive to skew and were treated separately. The passive quenching, which must be located right underneath each pixel, and the decision tree that requires symmetric position for matched paths were instantiated in with the use of a script. Their placement within the module can be seen in Figure 6.12. Moreover, the arrangement of the two independent subgroups sharing a single TDC can also be seen in Figure 6.12, with the SUBGROUP #2 being flipped using the horizontal reference with respect to SUBGROUP #1.

The module size and number of pixels was designed based on two parameters; first, since it was the first design cycle of the SPADs, a more conservative approach was adopted, including a relatively large pitch; second, the overall sensor activity was taking into account to design the *decision tree*, as described in Chapter 5. The readout circuit and SPADs are perfectly matched, where some of the components, such as the TDC, the passive quenching, and the decision makers were placed using a script, the rest of the circuitry was automatically placed and routed.

In the next sections, the details of each sub-block will be discussed.

### 6.3.2. TIME-TO-DIGITAL CONVERTER

With the goal of performing digital data processing within the module, it is essential to provide a readily available, binary timing information straight from the TDC, which also imposes area restriction with respect to on-chip calibration and decoding. For these reasons, the TDC was designed using a current-starved 8 pseudo-differential stages RO, capable of providing 4-bit fractional resolution, through a set of sense-amplifier flip-flops (SAFF) [5]. Moreover, since the TDC is shared among two independent subgroups, it must contain

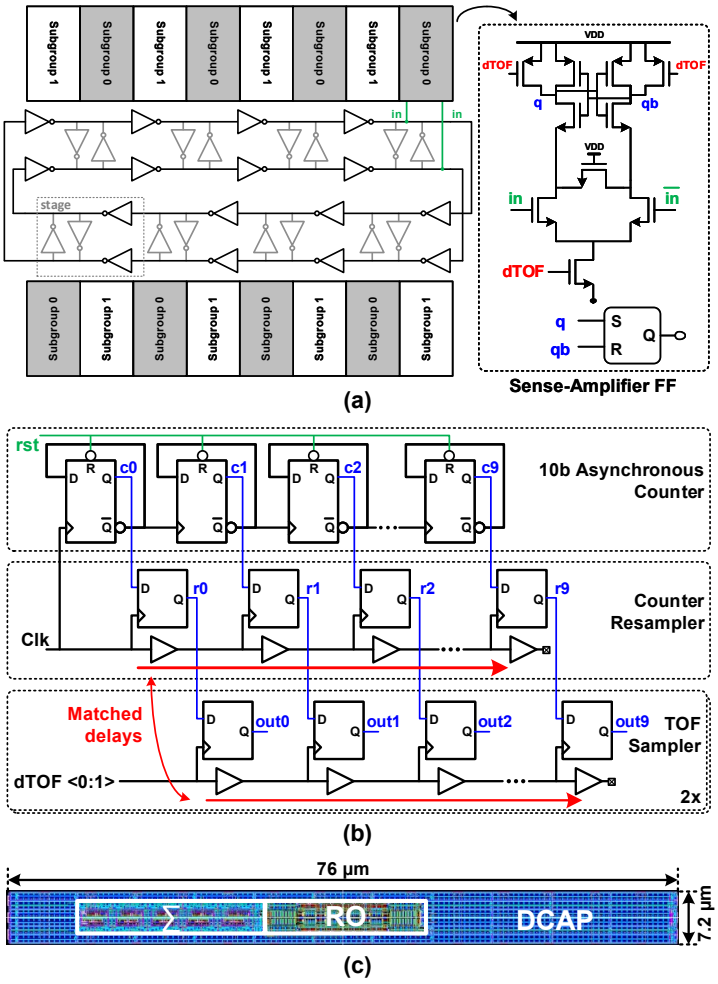



Figure 6.13: Time-to-digital converter: (a) pseudo-differential stages and SAFF arrangement, for the two independent subgroups; (b) counter schematic; (c) layout.

separated sampling structures, as shown by the RO schematic in Figure 6.13. The frequency is controlled by a simple pMOS current source, not shown in the diagram.

Due to a relatively fast speed of the RO (about 1 GHz – $\Delta_{LSB} \approx 62.5$ ps), an asynchronous binary counter was favored instead of a synchronous topology. However, since each bit of the counter is clocked by its predecessor, the delay accumulation through multiple stages can cause sampling errors. This is compensated by re-sampling the counter outputs with the same input clock and a chain of buffers. The block diagram is shown in Figure 6.13 (b). It is not mandatory to match the DFF delay with the re-sampling buffer, as long as the clock period is not extremely high. Hypothetically, if these delays were matched, the maximum counter operating frequency would be the inverse of a single DFF

delay, pushing its limits to about 8 GHz (in 65 nm). Since the input clock is only about 1 GHz, by guaranteeing that the buffer delays is shorter than the DFF (which is most certainly the case, for library standard cells), and it is large enough to compensate partially the DFF delay, the counter operates with a reasonable margin. The sampling lines, coming from the dTOF signals, are then matched through exactly same structure of buffer+DFF, as shown in Figure 6.13 (b).

The TDC occupies a very small area of 550$\mu$m$^2$, where about 40% of the area is dedicated to decoupling capacitors, while providing an equalized and calibration-free binary output. The layout is shown in Figure 6.13 (c).

### 6.3.3. OPERATION

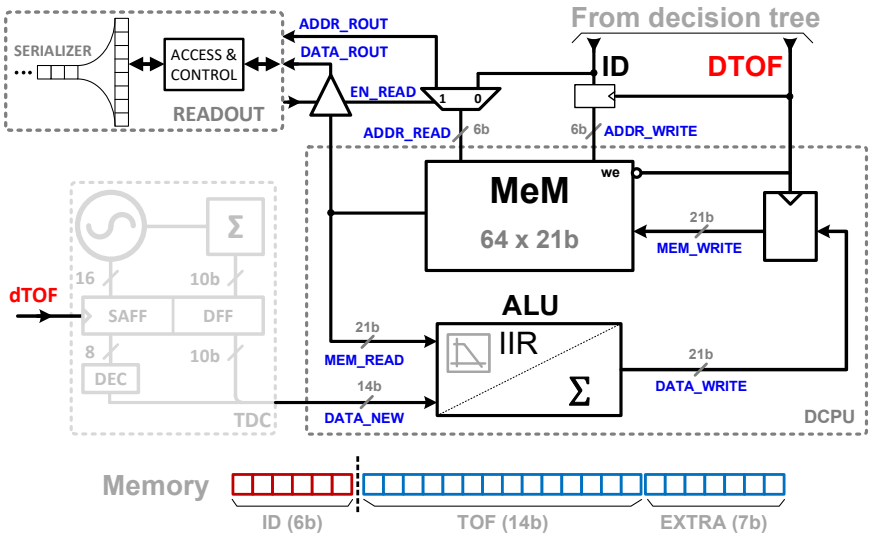



Figure 6.14: Digital processing and communication unit (DPCU) block diagram.

The decision tree generates the timing signal dTOF, and the event source, ID, which are fed to the digital processing and communication unit (DPCU). The DPCU is a synchronous circuit, capable to perform different functions, depending on its configuration. The signal dTOF is used as a clock, whereas the ID is used to access the corresponding pixel memory, reading its previous information stored, and combining it with the new timing information, also sampled at the TDC by dTOF. The result of the current processing information is then stored back into the memory, during the next new, unrelated event. The speed is maximized by keeping the memory bus contained in a small area, which loading time is relatively short. A block diagram of the DPCU is shown in Figure 6.14.

In the current sensor version, the core of the processing unit is an arithmetic logic unit (ALU). One of the advantages of the digital synthesis is that its function can be more easily described and implemented in RTL. In our implementation, it was designed to perform a low-pass filter, through a digital infinite impulse response (IIR) filter, and/or photon counting, for intensity measurement, depending on the external configuration.

According to the specifications, the TOF information is 14-bit and is stored into the memory. In order to host the fraction part of the IIR filter and/or to operate as intensity counter, an extra 7-bit memory was included, as shown at the bottom of Figure 6.14. The 6-bit ID is already used as a pointer for the memory, not requiring it to be stored, thus totaling 21-bit memory per pixel.

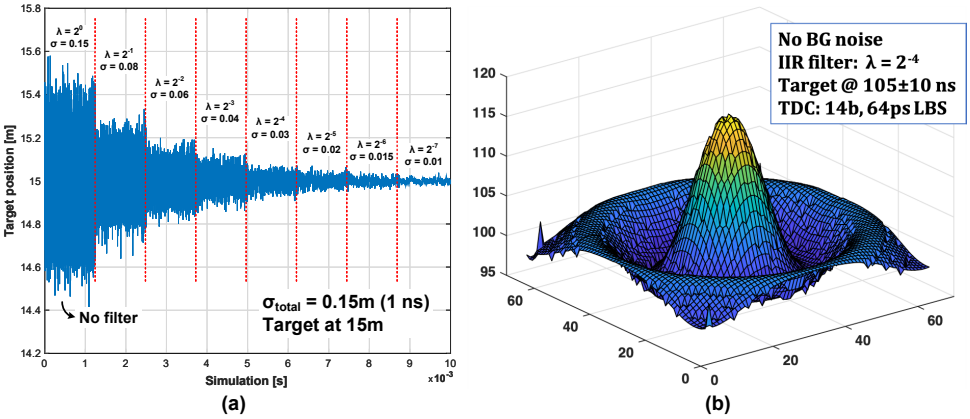



Figure 6.15: IIR filter Verilog simulation: (a) different $\lambda = 2^{0\cdots-7}$ and the effects on the standard deviation, $\sigma_{total}$, in meters; (b) 3D rendering image for $\lambda = 2^{-4}$.

The core of the processing unit is an arithmetic logic unit (ALU). Due to digital synthesis, its function can be more easily described and implemented. In our implementation, it can be configured to operate as a low-pass filter, through a digital infinite impulse response (IIR) filter, and/or photon counting, for intensity measurement. The low-pass filter is responsible to accommodate multiple events between readouts, providing an averaging of the signal, in order to reduce its uncertainty. The frequency characteristics of the IIR filter and, consequently, the pole location, are controlled by the attenuation factor $\lambda$, which is realized as a right-bit-shift operator. The time-domain equation is expressed as

$$y[k] = (1-\lambda)\cdot y[k-1] + \lambda \cdot x[k]. \tag{6.1}$$

An example of the IIR filtering can be seen in Fig. 6.15. Assuming a combination of several timing uncertainties to the system, such as the laser pulse width, SPAD jitter, and TDC integrated jitter and quantization noise, to a total of 0.8 ns, which corresponds to a depth uncertainty of $\sigma = 12$ cm. By changing the pole factor ($\lambda$), the uncertainty progressively reduces to a minimum of $\sigma = 1$ cm, for $\lambda = 2^{-7}$. The averaging effect of the filter produces an uncertainty reduction given by

$$\sigma_{filtered} = \frac{\sigma_{total}}{\sqrt{1/\lambda}}. \tag{6.2}$$

The drawbacks of such signal processing is that, smaller the $\lambda$, the slower the system, which could cause image blur. Moreover, in the presence of noise, this filtering approach is less effective, thus being suitable mostly for low noise applications intrinsically, including

scanning system, with short integration time, small FOV per point and strong laser, and/or via noise suppression [9, 10].

In order to avoid unexpected addressing and mapping issues, a more qualitative simulation of the whole system is performed. By generating a 3D image function in MATLAB® that correspond to the distance information each pixel should have, and applying it to the sensor inputs, the whole system can be simulation, from the photon event, TDC information acquisition and storage, to readout and post-processing. Since the amount of pixels can be very large, a straight forward verification is not trivial, thus by applying a visual identifiable image, the system can be validated. In the example of Figure 6.15 (b), a 3D Sync function, located around 105 ns (15.75 m) and expanding up to 10 ns (1.5 m) is used. The TDC integrated RMS jitter (15 ps) and quantization noise (64 ps $\Delta_{LSB}$), and SPAD timing jitter (100 ps FWHM) was used, but without background noise, whilst utilizing an IIR $\lambda = 2^{-4}$.

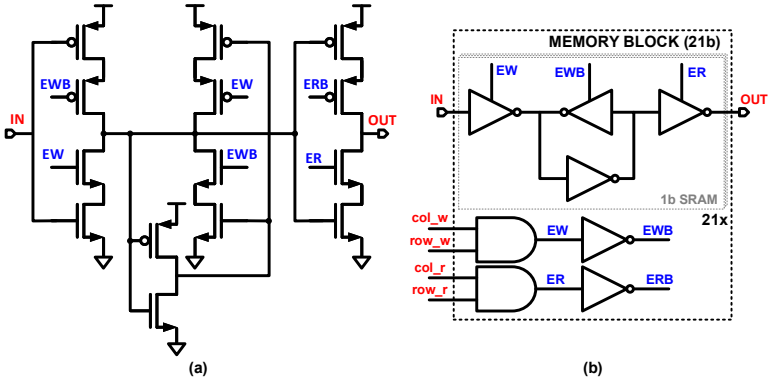



Figure 6.16: Custom-designed pixel memory: (a) single-ended, tri-state SRAM; (b) 21-bit block memory per pixel.

Since the memory takes the largest portion of the available area, it is important to minimize its size. The custom-designed 1-bit SRAM is shown in Figure 6.16 (a). The read time was minimized by using tri-state buffers, capable of driving the whole bank, with rail voltage, without the need of sense amplifiers or comparators. The organization and access of 21-bit pixel memory is shown in Figure 6.16 (b). Read and write times are 1.6 ns and 100 ps, respectively. A typical SRAM bank could also be implemented, but the read/write time is typically much larger and it requires access circuits that can take a large area, being more suitable for large memory banks. For our proposed architecture, the provided approach is more suitable. The total dead time between detections is less than 2.4 ns, which is related to the maximum activity the sensor can process. In the implemented case, it can provide over $830\times10^6$ conversions per second, per module of 128 pixels, split into two parallel subgroups.

### LASER SIGNATURE

In a real scenario, multiple LiDAR systems might be working simultaneously, from the same user or not. In any case, they all appear to each other as interferences and should be dealt with accordingly. Predicting such conditions, a code-based solution has been pro-

posed [11], treating the problem mostly via firmware/software, which might increase post-processing power and latency onto the system.

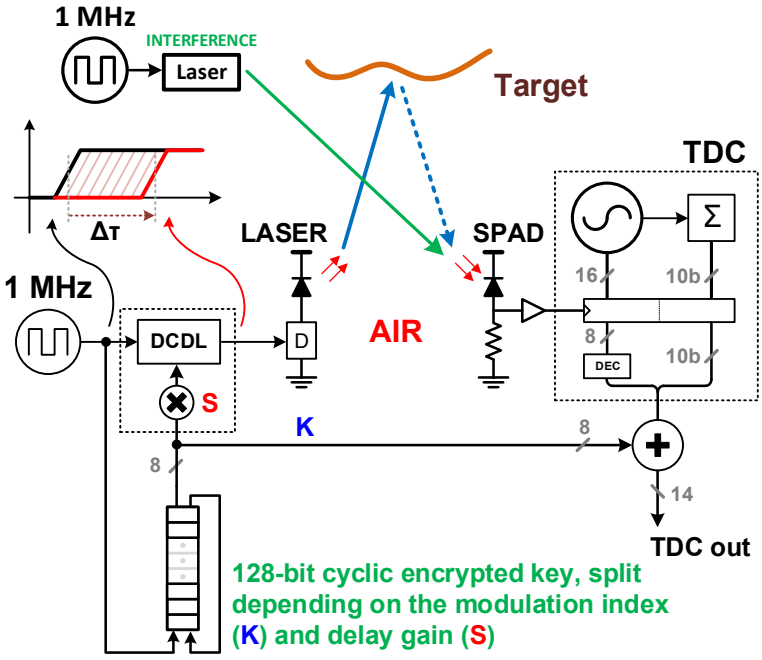



Figure 6.17: Laser signature concept. Implementation via encrypted key, divided according to modulation index and directly combined with digital TDC output.

Alternatively, we propose a simple laser signature, applied directly to the laser trigger, through a digitally-controlled delay line (DCDL), as well as to the acquired timestamp, by digital arithmetic calculation. The concept is shown in Figure 6.17. Due to the discrete nature of the system, by controlling the modulation index ($K$) and delay gain ($S$), the signal can be recovered without any loss of information, while the interferences are scrambled, appearing as noise in the later accumulated histogram. Because the laser is shifted in phase, we associate the polar modulation with phase-shift keying (PSK).

A generic histogram of such a scheme can be inspected in Figure 6.18 (a). In this illustration, the outgoing laser is spread over 16 equidistant chunks, uniformly, while the interference is unaware of the modulation and, consecutively, contained within a single chunk. The transmitted histogram is a representation of the scene, although it is not necessarily ever constructed. In the receiver, by applying the modulation to the TOF information, the detected signal is reconstructed, while the interference is then spread over the histogram. Since the interference energy is scattered, its peak is reduced, easing a successful signal peak detection.

For maximum spectrum efficiency (interference suppression over spread in histogram), the delay offset, produced by the modulation, should correspond to the system uncertainty (FWHM), as qualitatively demonstrated in an illustration shown in Figure 6.18 (b). If the

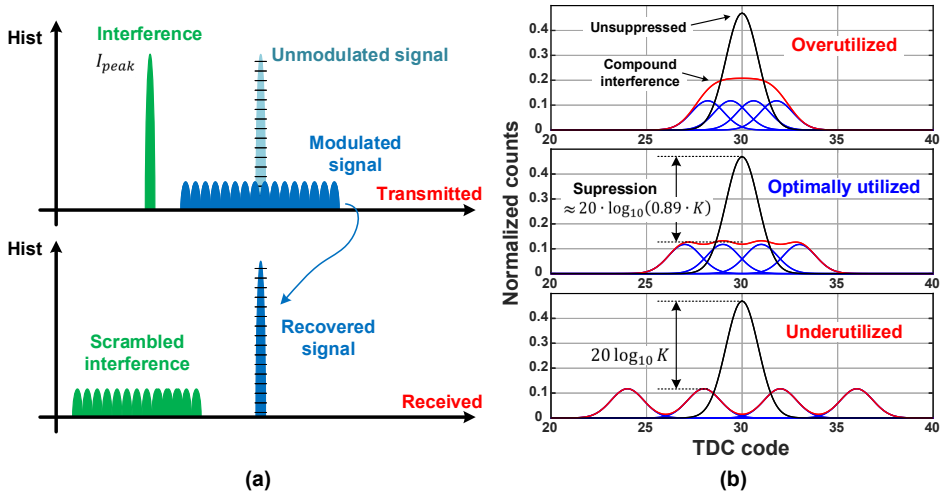



Figure 6.18: Laser signature histogram: (a) signal modulation/recovery and interference scrambling; (b) spectrum utilization for different delay gain (S), for 4-PSK modulation.

delay gain is too low, the compounded histogram peak will have a peak higher than the individual chunks; if the delay gain is too high, the spectrum is overly utilized, putting constraints on the laser triggering capability; pulsed lasers typically require a stable, periodic trigger for maximum efficiency. Moreover, to ease TDC correction, the modulation should be a multiple of the TDC LSB ($\Delta_{LSB}$), unless extra fractional bits can be afforded.

In general, the delay gain $S$, see Figure 6.17, which is effectively part of the DCDL, should be chosen as the next integer of $\Delta_{LSB}$, either in number of histogram bins or seconds, as:

$$S = \left\lfloor \frac{FWHM}{\Delta_{LSB}} \right\rceil \quad \text{and} \qquad \Delta\tau = S \cdot K, \tag{6.3}$$

where $\Delta\tau$ is the time delay, in picoseconds, applied to the laser trigger. The index $K$, is chosen by simply selecting which bits to use, up to 8 bits in our case (256-PSK). A unique 128-bit encrypted key can be added to the system, and subdivided in words of 8 or less bits, depending on $K$, to increase security. If optimized, the system provides interference suppression of about $20 \cdot \log_{10}(0.89 \cdot K)$.

### DUAL-AXIS LASER SCANNER

Flexible lateral resolution was obtained through a dual-axis laser scanning. It was implemented using a Thorlabs Large Beam Diameter Galvo Scanner GVS212, with broadband mirrors, controlled by a waveform generator Keysight 33500b, via MATLAB. By synchronizing laser, readout and scanner, efficient illumination and image reconstruction could be performed. The apparatus is shown in Figure 6.19.

The current setup, due to the small module size, the dual-axis is necessary to create the 3D image. However, since the modules can be arranged in any desirable shape, multiple

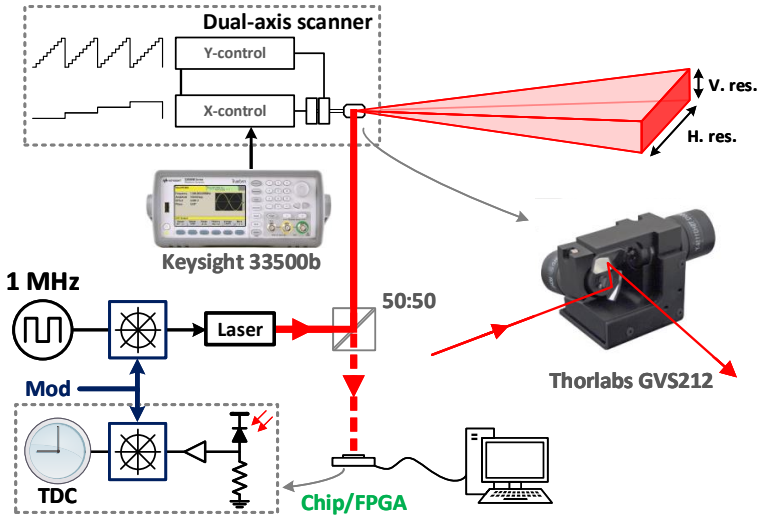



Figure 6.19: Conceptual dual-axis galvo scanning LiDAR system, featuring laser polar modulation for interference suppression.



modules can be allocated in a line, so a single axis scanning can be performed. Moreover, a 2D sensor array can be implemented, avoiding the scanning altogether, however, with an impact on the SNR and maximum detectable range, as discussed in the Chapter 3. Nevertheless, the scanner is a useful apparatus to obtain 3D images as it will be shown next.

### 6.3.4. CHARACTERIZATION

The proposed architecture was implemented using TSMC 3D-stacked technology, featuring a 4-metals, 45 nm CIS backside illumination (BSI) SPAD array, and a 5-metals, 65 nm low-power CMOS readout integrated circuit (ROIC), packaged in a ceramic QFP-120L. Throughout the system operation and characterization, two lasers were used: for all depth measurements, a 532 nm PicoQuant VisUV, and for SPAD characterization and laser signature, a 637 nm ALDS PiL063X.

Depth measurement precision, in dTOF systems, is directly related to timing error, as an independent combination of SPAD response jitter, TDC variation (accumulated RMS jitter and quantization noise), and laser pulse width, as:

$$\sigma_{total} = \sqrt{\sigma^2_{TDC\_RMS} + \frac{\Delta^2_{LSB}}{12} + \sigma^2_{SPAD} + \sigma^2_{laser}}. \tag{6.4}$$

By approximating these sources to Gaussian-shape, $FWHM \approx 2.355 \cdot \sigma$ can be used, which is a widely adopted term in the SPAD sensor community.

The SPAD utilized in this implementation is presented in Section 2.4.2. Its performance of less than 108 ps FWHM timing jitter, 32% peak photon detection probability (PDP), and 55 cps/$\mu$m$^2$ dark-count rate (DCR) when operating under excess bias voltage (above breakdown) of 2.5 V is more than sufficient for LiDAR application.

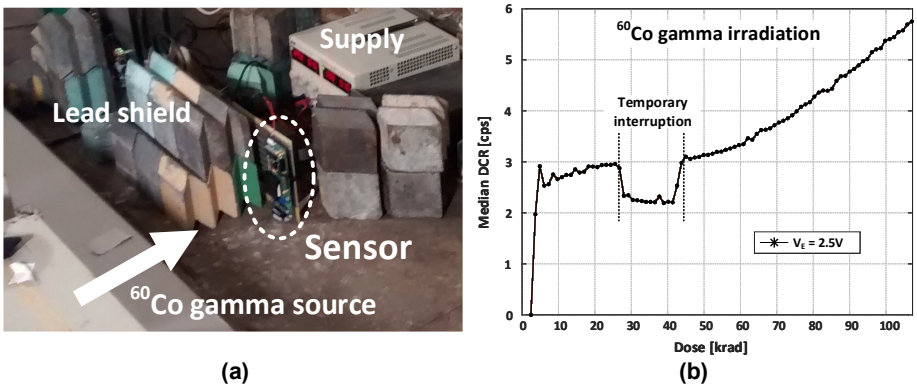



Figure 6.20: Irradiation measurement: (a) setup; (b) DCR increase with accumulated dose.

Moreover, since space applications are among the possible targets of this work, the sensor was exposed to a $^{60}$Co gamma source, seen in Figure 6.20 (a), so the effects of radiation on the device performance could be evaluated. At a dose rate of 73 krad/h, the DCR increases from 2.8 kcps to 5.8 kcps over a 90-minute exposure, as plotted in Figure 6.20 (b), and returned to the original value after annealing. The applied dose is much higher than required for space, thus validating the circuits for such environments.

For real ranging measurements, the sensor was characterized by single-point measurements, using targets with 50% reflectivity, perpendicular to the sensor optical axes. In this configuration, the sensor was operated in two modes: high and low-resolution. In the former, the TDCs were tuned to provide $\Delta_{LSB}$ = 61 ps and maximum range of about 1$\mu$s (14-bit), equivalent to 150 m range. In the latter mode, $\Delta_{LSB}$ was tuned to 204 ps, covering about 3.34$\mu$s, which is equivalent to 500 m range. The characterization of the TDC leads to less than 2 LSB and 3 LSB differential and integral nonlinearities (DNL and INL), respectively, for $\Delta_{LSB}$ = 61 ps. The relatively high and periodic nonlinearity [1] arises from mismatches between the sampling signal and RO + counter phases (Fig. 6.13 (b)). Calibration can be performed to account for some of these issues, but since our solution requires internal binary TDC result, and the power and area budget for the module is scarce, no calibration was performed and reported here.

The laser parameters used here are 4 mW at 1 MHz frequency, and 1.4 mW at 300 kHz, for high- and low-resolution modes, respectively. Since the energy per pulse is roughly constant, in both modes the optical energy per pulse is about 4 nJ, with pulse width of 80 ps FWHM, and 47 W peak power. In both modes, each measurement point was obtained by accumulating 100 chip readouts, and combining the dTOF information of all pixels of a single module, as a digital SiPM, into a histogram in Matlab®, without any other filter. The maximum chip readout is 2000 fps, totaling 20 fps depth measurement. All measurements were physically performed, without any emulation.

In high-resolution mode, the measurements were performed indoor. An aerial view of the location is shown in Figure 6.21 (a). The measured distance and accuracy are shown in Figure 6.21 (b), which was obtained by accumulating 100 readout frames, per point, under indoor ambient light. The maximum accuracy error was below 7 cm (0.3% non-linearity)

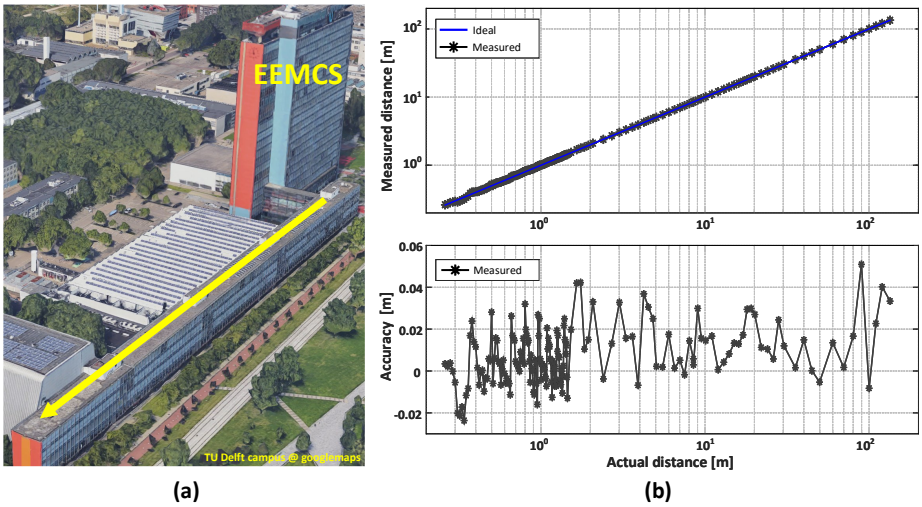



Figure 6.21: High-resolution single-point measurement: (a) aerial view of measurement location; (b) measured distance and accuracy.



and worst-case standard deviation of 15 cm (0.1% uncertainty).

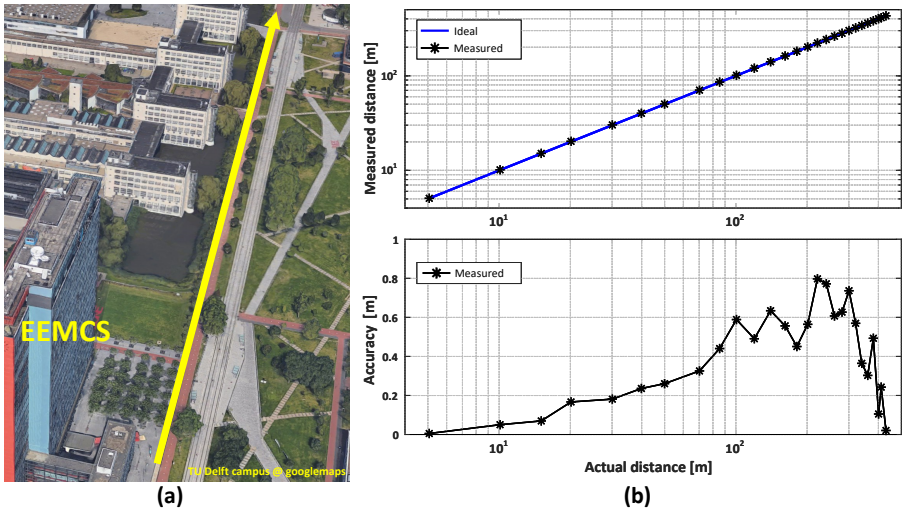



Figure 6.22: Low-resolution single-point measurement: (a) aerial view of measurement location; (b) measured distance and accuracy.

In low-resolution mode, the measurements were performed outdoor. Similarly, an aerial view of the location and the measured distance and accuracy are shown in Figure 6.21, (a) and (b) respectively. The maximum accuracy error was below 80 cm (0.4% non-linearity) and worst-case standard deviation of 47 cm (0.11% uncertainty). The $SNR$ towards the end

of the range (>300 m) was too low to determine the precision accurately.

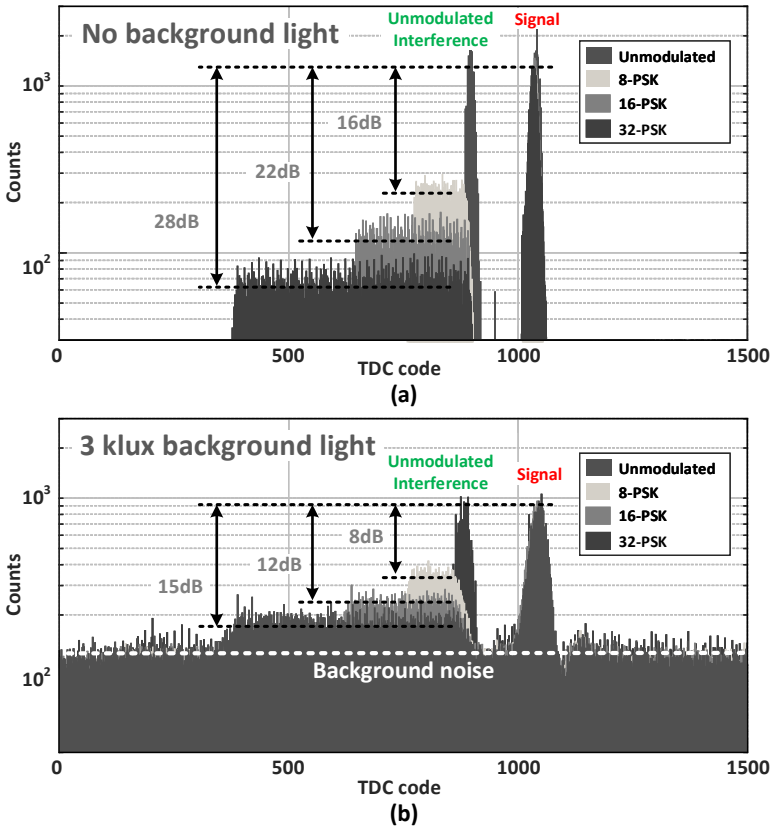



Figure 6.23: Laser signature measurement. (a) no background illumination; (b) 3 klux background illumination.

The laser signature was measured and it is shown in Figure 6.23, for 8-, 16-, and 32-PSK (index $K$ of $2^3$, $2^4$, and $2^5$, respectively, and gain $S = 16 \cdot \Delta_{LSB}$). Two lasers were used in the measurements: a 637 nm, serving as interference, and a 532 nm as signal. Figure 6.23 (a) shows the effects of the modulation without any background illumination, where the interference suppression was measured very close to the expected value (about 1 dB off). Under background illumination, the suppression effectiveness is reduced (see Figure 6.23 (b)), due to two effects: first, the noise adds a bias level for the histogram counts, for both signal and interference, reducing their ratio (suppression); second, our architecture is based on a sharing decision tree, and collisions between noise and signal are reflected on the maximum signal acquisition, thus the overall peaks (unmodulated and signal) are reduced in Figure 6.23 (b), if compared to Figure 6.23 (a).

A dual-axis scanner was used to obtain higher spatial resolution images. In this measurements, a 532 nm wavelength laser was used, with average optical power of 4 mW at 1 MHz frequency, and very small lens aperture. In case of an optimized optical setup and availability of a higher power laser, the integration time per point can substantially reduce,

increasing the frame-rate.

Figure 6.24 shows a 32×32 image, featuring targets with different reflectivity (from 8 to 60%), with targets ranging from 4 to 10 meters and about 30° of AFOV. The integration time in this case was set to 5 ms per point. As can be seen from the depth map and a cross-section (at row 30), the absolute ranging measurement is successfully acquired, without compromise.

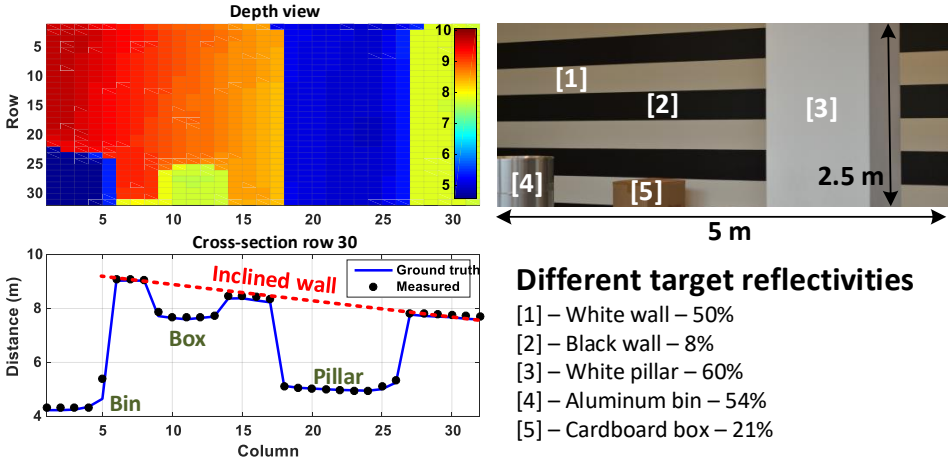



Figure 6.24: Coarse spatial resolution of 32×32 image, featuring multiple targets with different reflectivity.

Another 3D image was obtained through scanning, featuring a finer spatial resolution of 256×256 and 7° AFOV. For this measurement, the same laser was used, but only 500$\mu$s per point integration time was used, due to higher reflectivity index. The result can be seen in Figure 6.25, where millimeter resolution was obtained. A special feature about this image is that, the internal DPCU was configured to obtain simultaneously the dTOF and intensity, where this 3D reconstruction is an effective overlap of both measurements.

Table 6.1 shows a performance comparison of this work to recently published state-of-the-art LiDAR systems. To the best of our knowledge, the proposed sensor provides the longest single-point measurement, the best accuracy and precision, ever reported in a CMOS system. The laser power, wavelength, and the speed of the measurement impact considerably the sensor sensitivity to noise. Ref. [10] uses a 870 nm, 40 mW laser, to operate far away from the maximum of the sun irradiance and, in addition, it uses an narrow band-pass filter. Ref. [9] uses the same wavelength as used in this work and, although capable of handling noise with the use of smart triggering, the results were emulated with a high-power laser and a fiber.

A chip micrograph is shown in Figure 6.26. Since in this work a 3D-stacked technology was used, the ROIC on the bottom tier is not visible, and only the circular shape SPAD array is visible.

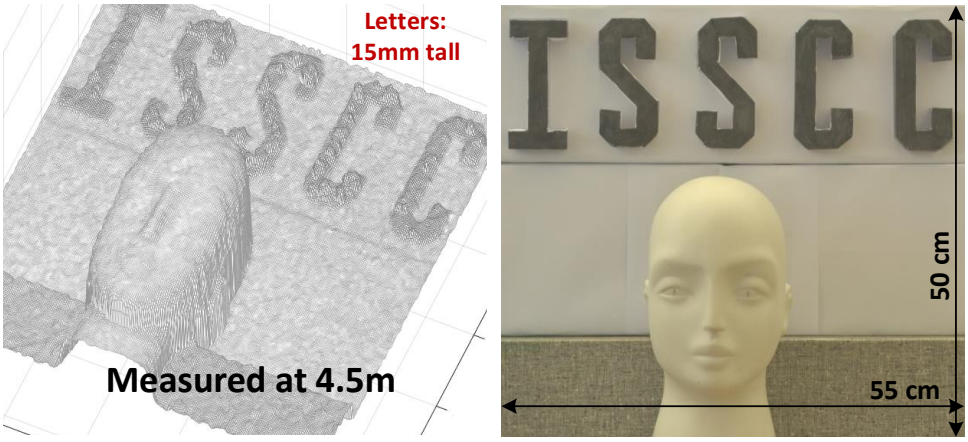



Figure 6.25: Fine spatial resolution, 256×256 image: intensity and depth measurement simultaneously.



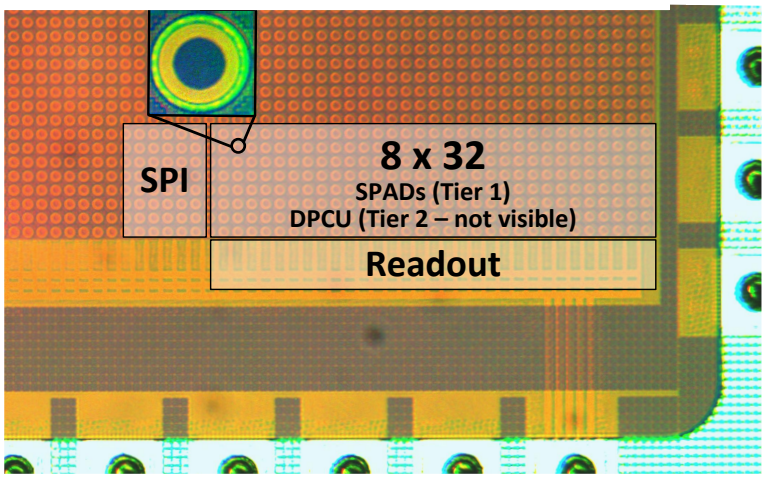



Figure 6.26: Chip micrograph: only top tier (SPAD array) is visible.

Table 6.1: Comparison performance of state-of-the-art CMOS LiDAR

| Parameter | Unit | **This Work** | [9] | [10] | [12] | [13] |
|---|---|---|---|---|---|---|
| Technology | – | 45/65 nm CMOS | 150 nm CMOS | 180 nm CMOS | 130 nm CIS | 0.35$\mu$m CMOS |
| Architecture | – | Always-on, shared TDC | Event-driven, per-pixel TDC | Column-wise shared TDC | Histogramming shared TDC | Event-driven, per-pixel TDC |
| ***Sensor characteristics*** | | | | | | |
| Resolution | - | 256×256[a] | 64×64 | 340×96 | 32×32 | 32×32 |
| Pixel pitch | $\mu$m | 19.8 | 60 | 25 | 21 | 150 |
| Pixel fill factor | % | 31.3 | 26.5 | 70 | 43 | 3.14 |
| SPAD DCR@$V_E$ | cps/$\mu m^2$[b] | 55.4 @ 2.5 V | 57 @ 3 V | 6 @ 3.3 V | N/A | 120 @ 6 V |
| TDC depth | bit | 14 | 16/15 | 12 | 8 | 10 |
| TDC resolution | ps | 60 – 320 | 250 – 20000 | 208 | 71.4 | 312 |
| TDC power | mW | 0.5 – 0.1 | N/A | N/A | 14.1 | 0.35/pixel[f] |
| TDC area | $\mu m^2$[b] | 550 | N/A | 31,000[d] | 30,000 | 5,600[d] |
| TDC linearity | DNL [LSB] | +0.9 / -1 | +1.2 / -1[b] | +0 / -0.52 | +0.75 / -0.61 | +0.06 / -0.06 |
| | INL [LSB] | +3 / 0 | +4.8 / -3.2[b] | +0.73 / -0.49 | +0.65 / -0.2 | +0.22 / -0.22 |
| ***Measured distance performance*** | | | | | | |
| Distance range | m | 150 – 430 | 367 – 5862[c] | 128 | 2.82 – 3.375 | 48 |
| Precision | m | 0.15 – 0.47 | 0.2 – 0.5[c] | 0.1[e] | N/A | 0.04[g] |
| | % | 0.1 – 0.11 | 0.13 – 0.14[c] | 0.1[e] | N/A | 0.8[g] |
| Accuracy | m | 0.07 – 0.8 | 1.5 – 35[c] | 0.37[e] | N/A | N/A |
| | % | 0.3 – 0.4 | 0.37 – 1.9[c] | 0.37[e] | N/A | N/A |

[a] Flexible resolution depending on scanner and available laser optical power. [b] Measured over 5% of the total range.
[c] Emulated results with optical fiber. [d] Estimated by layout. [e] Measured at 100 m. [f] DLL and TDC power. [g] Measured at 5 m

## 6.4. CONCLUSIONS

In this chapter, two modular dTOF sensors were described. The core philosophy in the design of such sensors was to produce a self-containing module, which could be used in the design of a much larger sensor array, without major modifications.

In the first version, a typical analog approach was used, where all components of the dTOF system were custom-designed and implemented in the analog flow, with an exception of the readout and configuration, which was done in the digital domain. The design was performed in ST Microelectronics 3D-stacking technology, featuring 65 nm BSI SPAD array on the top tier, connected to a 40 nm CMOS readout on the bottom tier.

In the second version of the sensor, the complete flow was done in the digital domain instead, shortening the design time and increasing the verification. Each module is digitally synthesized and completely autonomous, which enables scaling to a desirable sensor size, without affecting its operation.

The design was performed in a TSMC 3D-stacking technology, featuring a BSI SPAD array on the top tier, connected to a readout and processing circuit on the bottom tier. A PPM-based laser signature recovery technique is proposed, achieving up to 28 dB interference reduction under no background noise conditions. Single-point measurements up to 150 and 300 m were achieved in two different resolution modes, with accuracy error lower than 0.4%. By using one module as a digital SiPM, 3D images were obtained by a 2-axis galvo scanning system, for up to 10 m range and 30° AFOV. With the future expansion of the single module into multiple modules on chip, different types of illuminator, including fixed laser arrays, will be used in both scanning and flash modes of operation.



This work has been evaluated using lasers in the visible spectrum (532 nm and 637 nm). Although the sensitivity of the SPADs is the highest, the strong solar irradiance spectrum limits the system's maximum range and frame rate. Therefore, under strong ambient light, it is desirable to operate the system using a wavelengths in which the solar irradiance is considerably absorbed in the atmosphere, for instance at 850 nm or 940 nm. In this case, a narrow bandpass filter can greatly improve the overall system performance. Other consideration must be taken into account, such as eye-safety and laser efficiency when designing a LiDAR system, which is out of the scope of this work.

# REFERENCES


[1] A. R. Ximenes, P. Padmanabhan, M.-J. Lee, Y. Yamashita, D. Yaung, and E. Charbon, *A 256×256 45/65nm 3d-stacked spad-based direct tof image sensor for lidar applications with optical polar modulation for up to 18.6 db interference suppression,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2018) pp. 96–98.

[2] *Pilot optical line for imaging and sensing (POLIS),* http://polis.minalogic.net (2018).

[3] *ST Microelectronics, Edinburgh, Scotland.* http://www.st.com (2018).

[4] A. Ronchini Ximenes, P. Padmanabhan, and E. Charbon, *Mutually Coupled Time-to-Digital Converters (TDCs) for Direct Time-of-Flight (dTOF) Image Sensors,* Sensors **18** (2018).

[5] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu, and M. M.-T. Leung, *Improved sense-amplifier-based flip-flop: Design and measurements,* IEEE J. Solid-State Circuits **35**, 876 (2000).

[6] A. Janssen, *Exploration of SPAD Based CMOS QRNG Designs*, Ph.D. thesis, Delft Univeristy of Technology (2017).

[7] *NWO, Netherlands Organisation for Scientific Research, Netherlands.* http://www.nwo.nl (2018).

[8] *Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan.* http://www.tsmc.com (2018).

[9] M. Perenzoni, D. Perenzoni, and D. Stoppa, *A 64×64-Pixels Digital Silicon Photomultiplier Direct TOF Sensor With 100-MPhotons/s/pixel Background Rejection and Imaging/Altimeter Mode With 0.14% Precision Up To 6 km for Spacecraft Navigation and Landing,* IEEE J. Solid-State Circuits **52**, 151 (2017).

[10] C. Niclass, M. Soga, H. Matsubara, S. Kato, and M. Kagami, *A 100-m Range 10-Frame/s 340×96-Pixel Time-of-Flight Depth Sensor in 0.18-µm CMOS,* IEEE J. Solid-State Circuits **48**, 559 (2013).

[11] T. Fersch, R. Weigel, and A. Koelpin, *A CDMA modulation technique for automotive time-of-flight lidar systems,* IEEE Sensors J. **17**, 3507 (2017).

[12] T. Al Abbas, N. A. Dutton, O. Almer, N. Finlayson, F. M. Della Rocca, and R. Henderson, *A CMOS SPAD Sensor With a Multi-Event Folded Flash Time-to-Digital Converter for Ultra-Fast Optical Transient Capture,* IEEE Sensors J. **18**, 3163 (2018).

[13] F. Villa, R. Lussana, D. Bronzi, S. Tisa, A. Tosi, F. Zappa, A. Dalla Mora, D. Contini, D. Durini, S. Weyers, *et al.*, *CMOS imager with 1024 SPADs and TDCs for single-photon timing and 3-D time-of-flight,* IEEE J. Sel. Topics Quantum Electron. **20**, 364 (2014).

# 7

# CONCLUSION

*In this concluding chapter, an overview of the main findings during the development of this thesis will be performed. The initial problem statement and questions posed at the introductory chapter will then be discussed and addressed, with the solutions, provided in each chapter, summarized.*

## 7.1. INTRODUCTION

IN this concluding chapter, the main findings in the development of this thesis are offered. Also, the contributions of this work for the depth sensing community will be performed, with specific points.

## 7.2. MAIN FINDINGS

Since its conceptualization, dTOF systems have been instigating the community on the development of a flash LiDAR, capable of handling high background noise, while achieving long distance depth measurements, at high speed and accuracy. With the introduction of CMOS single-photon detectors, another step towards the popularization of such technology has been made. However, system limitations, specially on the illuminator, still present important bottlenecks.

Nevertheless, dTOF imaging has a great potential in various depth sensing applications. There are already several products using such technology. However, in most cases, the sensors operate under a very small field-of-view, either for a single point mode or as sensing device in a mechanical scanner setup. In both types, for the signal point of view, they are the same. The reason is obtained by the modeling done in the Chapter 3, which can be summarized intuitively by evaluating the SNR of the system.

At the beginning of this thesis, the ultimate stated goal was the implementation of an automotive LiDAR. Its performance, however, is still below those required for the long distance LiDAR, at least for a flash mode under high background noise. In one of the implementations in Chapter 6, it was shown a maximum of 430 m range obtained, but still in single point measurement.



In the system point of view, the main component that determines its performance is the illuminator, including the flexibility to which it can be driven, including peak and average power, frequency, pulse width, etc. However, the illuminator has other restrictions extrinsic to the system, such as maximum optical power, due to eye safety restrictions, as well as maximum power consumption, due to thermal dissipation restrictions. Thus, precise understanding of the environmental conditions to which the system will operate is essential. Yet, for outdoor operations, the background illumination noise must be filtered out in the interest of avoiding the system saturation.

The most common ways to reduce the background noise is to reduce the exposure to the sensor, as well as applying a spatial-temporal correlated sampling. The former can be done by reducing the laser frequency and concentrating the laser power in stronger pulses, thus to reduce the noise, but not the signal. In the latter, neighboring pixels can be used to evaluate origin of the event, filtering the uncorrelated noise out, as described in Chapter 3. In both ways, it is essential to perform such operations on-chip, as close to the pixels as possible, so as to avoid the sensor saturation.

Typically, for an image sensor, it is desirable to increase the number of pixels per area, so a finer spatial resolution can be obtained. Conversely, for dTOF systems, increasing the number of pixels for the same FOV and illumination power can be detrimental. The overall number of events among the whole sensor will always increase with a larger number o pixels, since the detector dead time is alleviated through parallel sensing. Apart from limitations on data throughput, when performing smarter detections, such as coincidence, the

probability of a valid event drops drastically. On one hand, a larger number of pixels allow a more dense target sensing, which improves image quality and coincidence detection. One the other hand, the photon detection probability reduces. Thus, a very good understanding of the system must be done when designing such systems, including a robust system modeling. Although it is essential to have a well-functioning sensor, with precise timing measurement and robust to PVT, its impact on the overall performance is small if compared to the rest of the system. The laser, optics, and how the sensor operates determine the majority of parameters.

## 7.3. MAIN CONTRIBUTIONS

At the beginning of this thesis, the goal was to implement a novel sensor topology, capable of solving some of the issues in the previous sensor topologies, while reducing power consumption and increasing flexibility. The main focus have been the timing generation and acquisition, which typically are responsible for most of the sensor power consumption. It is intrinsically difficult to be achieve precision and low variability, especially in large arrays. Normally, forward calibration is required, which increases power consumption and complexity.

The first contribution refers to the generation of a timing reference in a very small form factor, for communication and other applications. The proposed novel clocking reference can be also used for large arrays of image sensors, through the use of mutually coupled ring oscillators. Timing reference is one of the most important elements in any communication, localization and positioning system. It is by using a global timing reference, those systems can relate and be correlated to, providing an absolute measurement. From wireless and wireline transceivers to GPS receivers, timing is the base reference to coherent synchronization.

From the timing reference implemented with the mutually coupled TDC array, which has the capability of synchronous operation, a sampling structured capable of handling a large number of events is necessary. Moreover, an *in-pixel* storage was necessary, so as to handle such large number of events. Thus, the second contribution of this work refers to the design of a modular dTOF structure, based on a novel binary arbiter, called decision maker, where the event source is preserved. It allows a camera-mode operation, where each pixel is addressable, while being able to handle excessive activity through an edge-sensitive structure.

The third contribution is an extension of the implemented module, which takes advantage of the readily available digital information after timing acquisition, to perform *in-locus* data processing and laser signature. Due to a synchronous operation, linked to a photon event and through the decision tree (series of decision makers), and the presence of a memory per pixel, an intensity counter and low-pass filtering is implemented. Moreover, phase modulation for laser signature is proposed, to accommodate multiple systems at the same time, while being robust to interference.

As discussed previously, modeling is essential for an optimum operation. For this reason, the last contribution was performed in Chapter 3, which provides a benchmark for the minimum system SNR for single-point/scanning operation, as well as flash dTOF, through a more coherent system modeling.

## 7.4. RECOMMENDATIONS FOR FUTURE WORK

The successful design of a dTOF sensor, at least for outdoor LiDAR applications, is directly related to the system design. Since the dTOF is an active system, which requires active illumination, it does not suffice to only improve the sensor's power consumption, sensitivity, etc., which are most likely not the system's bottlenecks.

The ultimate goal of dTOF image sensors is to operate them under flash mode, which would eliminate most of the expensive and wearable components of the system, namely, the scanner. Moreover, laser scanners are bulky and slow and are most likely not suitable for consumer applications, such as the potential AR/VR. Although optical phase arrays (OPA) are recently emerging, the typical optical power level and efficiency are too low.

Some of the recommendations for future work are:

- **Background suppression:** ambient noise is the main issue for LiDAR operating outdoors. The right combination of wavelength and sensor sensitivity can greatly benefit the overall system performance. Thus, providing background suppression is highly desirable. It can be done with a combination of several solutions. First, by optimizing the laser operation for very low duty-cycle, which means very short pulses with high peak power, while maintaining low average power for eye-safety restrictions. Second, smart triggering based on coincidence detection and target aware gating;
- **Improved modeling:** inclusion of environmental conditions of humid air, fog, rain, etc., as well as target uncertainties. Also, multi-path reflections, via ray tracing modeling, is essential for readout optimum design;
- **Neural networks:** Machine learning solutions capable of data fusion and optimization training in order to classify and group pixels, for a target aware detection, reducing the required amount to signal photons and being able to operate in even lower SNR conditions, typical of flash-mode LiDAR;
- **Detector improvement:** development of improved detectors for longer wavelengths, where the sun spectrum is lower, as well as novel architecture and technologies that can include more computational power as close to the detector as possible, in order to reduce power consumption over excessive data readout.

# A

# LASER OPERATION REGARDING EYE SAFETY

ACTIVE imaging systems, such as LiDAR, require a light source capable of illuminating the scene of interest with enough energy for the returning photons to generate a confident detection at the sensor, while remaining under eye and skin safety levels. Background noise (uncorrelated to the system, such as the sun and other light sources) can potentially degrade the depth accuracy, so different technologies have been proposed to deal with it. TCSPC is a commonly used technique in dTOF systems, which relies on the accumulation and detection of short pulses of light, against an uniformly distributed background noise, through histogramming and peak detection.

Ideally, we would like to operate the system at the maximum optical power possible, speeding up detection and increasing measurement confidence. This maximum power will be defined by eye safety limits, which are also influenced by other parameters as well, such as field of view, minimum operation distance, etc. However, light sources (in special nanosecond pulsed lasers) are not 100% efficient, impacting on multiple constraints, especially on thermal dissipation, thus a minimum optical power would be a key parameter for the system.

By knowing the maximum and minimum optical power required, a system designer can define the optimum optical solution. In the following sections, some aspects related to the illumination system will be examined.

## A.1. MAXIMUM AVAILABLE OPTICAL POWER

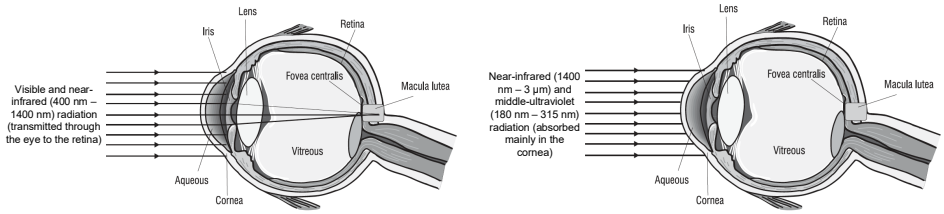
Except in few cases (unmanned spacecraft navigation, for instance) where Human Beings are not around LiDAR systems, typically eye safety is the main limitation on the optical power a system can operate. Skin injuries can also be an issue, although they may affect only the external dead layer of the skin cells; and even more penetrating damage usually will heal eventually. Large-area exposures that can lead to serious skin infections and other complications are not commonly associated with laser use because the beam is relatively

small. Nevertheless, when the light source wavelength is in the UV spectrum, more care should be taken, since it can cause DNA mutation and higher risk of cancer for long exposures. Since LiDAR does not typically use the UV spectrum, it will not be analyzed.

Laser and LED will be treated equally, where the only difference is the size and collimation of the beam. LEDs can operate under CW and pulsed (although typically with wider pulses than lasers) , but since they exit angle is wide (5 – 120°), they will be treated as diffused lasers. Lasers, on the other hand, have higher restrictions due to their typical collimated and small beam, with concentrated energy, and will be considered from this point.

The maximum optical power density depends largely on the photon wavelength and exposure time. For continuous wave (CW) lasers, the average optical power and maximum exposure time define the laser class. For pulsed lasers, though, few other parameters need to be considered, namely the pulse energy (in joules), the pulse width, repetition rate and emerging beam radiant exposure.

The wavelength is another important parameter, where the visible and near-infrared (NIR) range (400 – 1400 nm) imposes the highest constrictions, since the human eye has evolved to focus these wavelengths, and it is very efficient. For a far-away object (almost collimated light), the eye will optimally focus the beam into the retina, as sketched in Figure A.1 (a). The light irradiance of the image formed on the retina is 100,000 times greater than the light irradiance at the front of the eye. It is this considerable optical gain that creates an eye hazard when stray laser beams enter the eye, that can potentially damage permanently the retina, provoking irreversible vision degradation.




(a) (b)

Figure A.1: Light interaction with the eye, for different wavelengths: (a) Visible and NIR; (b) Mid-UV and NIR [1].

For wavelengths in the NIR range (> 1400 nm) and middle UV (180–315 nm), the light do not penetrate the eye (see Figure A.1 (b)), being absorbed mainly in the cornea, thus intrinsically less harmful than in the visible [1]. It allows higher optical power and it is preferred for LiDAR systems.

Sensitivity to a given wavelength varies significantly from person to person. Maximum permissible exposure (MPE) limits indicate the greatest exposure that most individuals can tolerate without sustaining injury. An MPE is usually expressed in terms of the allowable exposure time (in seconds) for a given irradiance (in watts/cm$^2$) at a particular wavelength. According to the primary laser safety standard in use today, the ANSI (American National Standards Institute) Z-136.1 [2], the maximum exposure depending on the wavelength is given in Table A.1.

Table A.1: MPE for Selected Lasers and Exposure Times (Reference: ANSI Z136.1-1993)

| **Laser** | **Wavelength** (μm) | **MPE** (average power density—watts/cm$^2$) | | | |
|---|---|---|---|---|---|
| | | Exposure time in seconds | | | |
| | | 0.25 s | 10 s | 600 s | $3 \times 10^4$ s |
| CO2 | 10.6 | – | 0.1 | – | 0.1 |
| Nd:YAG (cw)[a] | 1.33 | – | $5.1 \times 10^{-3}$ | – | $1.6 \times 10^{-3}$ |
| Nd:YAG (cw) | 1.064 | – | $5.1 \times 10^{-3}$ | – | $1.6 \times 10^{-3}$ |
| Nd:YAG Q-switched[b] | 1.064 | – | $17 \times 10^{-3}$ | – | $2.3 \times 10^{-6}$ |
| GaAs (diode) | 0.840 | – | $1.9 \times 10^{-3}$ | – | $610 \times 10^{-6}$ |
| InGdAlP (diode) | 0.670 | $2.5 \times 10^{-3}$ | – | – | – |
| HeNe | 0.633 | $2.5 \times 10^{-3}$ | – | $293 \times 10^{-6}$ | $17.6 \times 10^{-6}$ |
| Krypton | 0.647 | $2.5 \times 10^{-3}$ | – | $364 \times 10^{-6}$ | $28.5 \times 10^{-6}$ |
| | 0.568 | $2.5 \times 10^{-3}$ | – | $31 \times 10^{-6}$ | $18.6 \times 10^{-6}$ |
| | 0.530 | $2.5 \times 10^{-3}$ | – | $16.7 \times 10^{-6}$ | $1.0 \times 10^{-6}$ |
| Argon | 0.514 | $2.5 \times 10^{-3}$ | – | $16.7 \times 10^{-6}$ | $1.0 \times 10^{-6}$ |
| XeFl[c] | 0.351 | – | – | – | $33.3 \times 10^{-6}$ |
| XeCl[c] | 0.308 | – | – | – | $1.3 \times 10^{-6}$ |

[a] Operating at less common 1.33 $\mu$m
[b] Pulsed operation at 11 Hz, 12 ns pulse, 20 mJ/pulse.
[c] When repeated exposure levels are anticipated the MPE level must be reduced by a factor of 2.5.

Another quantity of interest in laser safety is called the nominal hazard zone (NHZ). This zone describes the region within which the level of direct, reflected, or scattered (diffuse) laser radiation is above the allowable MPE. Depending on the configuration of the laser system, different NHZ can be calculated. The typical arrangements are a direct laser beam, a laser with a focusing lens attached, and diffusely scattered laser light, as sketch in Figure A.2.

For a direct beam and when using a diffuser, the laser power can be calculated over the distance NHZ for a uniform illumination over the sphere surface cap area, given by:

$$NHZ = \frac{P_{laser}}{MPE \cdot 2\pi \cdot (1 - \cos(AFOV/2))} \tag{A.1}$$

where for a direct beam, the AFOV will be given by the exit angle of the laser (not perfectly collimated), and for the diffused light, the desirable AFOV can be assumed. For systems using lens on laser, the NHZ is given by:

$$NHZ = \frac{f_0}{b} \cdot \sqrt{\frac{4P_{laser}}{\pi \cdot MPE}} \tag{A.2}$$

The minimum working distance and/or a combination of different requirements can be used to obtain the safe distance and optimum optical power for the system. For instance, using a diffuser with AFOV = 60° ($\pi/3$ rad), where it is desirable to operate as close as 10 cm

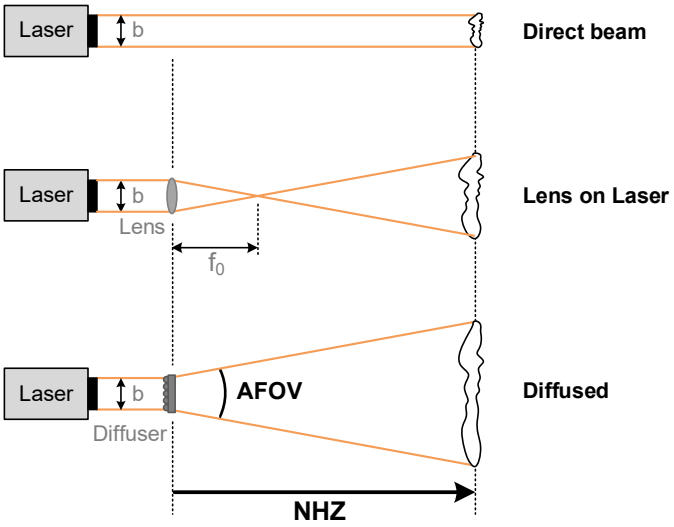



Figure A.2: Illumination arrangement for a direct laser beam, a laser with a focusing lens attached, and diffusely scattered laser light.

(NHZ), the MPE for 10 s exposure is 1.9 mW/cm$^2$ for a 840 nm wavelength (see GaAs laser at Table A.1), which sets the maximum allowable laser power to $P_{laser}$ = 16 mW. For a collimated output beam (1 mrad), on the other hand, the NHZ is the range of 300 m, and the laser would be considered a Class 3B [2], which must be handle with care, as well as eye and skin protections.

Another consideration regards the operation of LiDAR systems, which can be done in scanning or flash modes. In scanning mode, the laser is directly exposed to the scene, with a collimated beam, through the use of one or multiple moving mirrors, in order to cover a desirable AFOV. Since the scanning is performed constantly and it is relatively fast, the average power density equals the laser energy spread over the AFOV, although, for very short exposures, the peak power of the laser should be considered. In flash mode, however, the laser is diffused and the scene is uniformly illuminated. In this mode, the average is the same as the scanning, but without short exposures drawbacks.

Based on the required wavelength (also related to the detector quantum efficiency, component costs, etc.) and the AFOV, the maximum optical laser power can be defined. In the next section, the minimum optical power will be calculated, giving the ranges of average optical power that can be used for an optimized system.

## REFERENCES

[1] F. Seeber, *Light sources and laser safety,* Fundamentals of photonics **1** (2007).

[2] I. White and H. Dederich, *American national standard for safe use of lasers, ansi z 136.1–2007,* Laser Institute of America: Orlando (2007).

# B

# POWER CONSUMPTION FOR TIMING GENERATION

THE total power consumption to generate a timing reference, on chip, can be generically given by a composition by the PLL power consumption ($P_{PLL}$), including all necessary reference buffers, etc., and the dynamic power used on the distribution of multiple PLL phases, thus to be used as fine resolution for interpolative TDC. The number of phases and the frequency will depend on the system architecture. Normally, multiple phases are distributed and used as reference for the local TDCs, in both, column-wise [1] and per-pixel TDC approaches [2]. The power consumption associated with the reference is given by:

$$P_T = P_{PLL} + \#p \cdot C_{line} \cdot V^2 \cdot F. \tag{B.1}$$

An event-driven TDC starts to operate upon the arrival of a photon and it is stopped by the end of the time frame. Instead of providing a time-frame value, that can be the inverse of the laser frequency ($F_{laser}$) or shorter, we prefer to define the power consumed by a certain TDC based on its duty cycle. In order to do that, two parameters were create, $\overline{\alpha}$ and $\overline{\beta}$. The former, provides an average time a particular TDC stays on, whenever it operated. The latter, defines the activity rate, normalized to the laser frequency ($F_{laser}$). For instance, in the absence of noise, $\overline{\alpha}$ will carry a value that positions the target within the time frame, while in a noisy environment, $\overline{\alpha}$ tends to 0.5 (which is the mean value of a uniformly variation, such as the uncorrelated noise). $\overline{\beta}$, on the other hand, is defined depending on how many events occurred, per laser time frame (which can be larger than 1). If a TDC is shared among $M$ pixels, the compounded activity ($\overline{\beta} \cdot M$) should be used, limited to 1 (the TDC can only be activated once per time frame). Thus, the total power consumption over $N$ TDCs within the sensor is given by:

$$P_{TDC} = \overline{\alpha} \cdot P_{TDC} \cdot N \cdot min(\overline{\beta} \cdot M, 1). \tag{B.2}$$

Finally, in case a single TDC is shared, the power consumption necessary to process such events will depend on the absolute compounded activity of $M$ pixels ($\beta \cdot M \cdot F_{laser}$), limited

by the dead time of the combination circuit ($\tau$), and the energy consumed for each event propagation, such as:

$$P_{COMB} = E_{comb} \cdot N \cdot min(\overline{\beta} \cdot M \cdot F_{laser}, \tau^{-1}). \tag{B.3}$$

B

The total power consumption is given then by the combination of (B.1), (B.2), and (B.3), as:

$$\begin{aligned} P_T = P_{PLL} + \#p \cdot C_{line} \cdot V^2 \cdot F + \overline{\alpha} \cdot P_{TDC} \cdot N \cdot min(\overline{\beta} \cdot M, 1) \\ + E_{comb} \cdot N \cdot min(\overline{\beta} \cdot M \cdot F_{laser}, \tau^{-1}), \end{aligned} \tag{B.4}$$

Based on the assumptions and conditions described on Section 5.2, and comparing the power consumption of per-pixel and shared, sampled TDC from (5.5) and (5.7),

$$\begin{aligned} P_{T,per-pixel} &\geqslant P_{T,shared\_sampled} \\ \overline{\alpha} \cdot P_{TDC} \cdot M \cdot min(\overline{\beta}, 1) &\geqslant P_{TDC} + E_{comb} \cdot min(M \cdot F_{laser} \cdot \overline{\beta}, \tau^{-1}) \\ \overline{\alpha} \cdot P_{TDC} \cdot M \cdot min(\overline{\beta}, 1) &\geqslant P_{TDC} + M \cdot E_{comb} \cdot min(F_{laser} \cdot \overline{\beta}, (M \cdot \tau)^{-1}) \\ M &\geqslant \frac{1}{\overline{\alpha} \cdot min(\overline{\beta}, 1) - \left( \frac{E_{comb} \cdot min(F_{laser} \cdot \overline{\beta}, (M \cdot \tau)^{-1})}{P_{TDC}} \right)} \end{aligned} \tag{B.5}$$

## REFERENCES

[1] A. Carimatto, S. Mandai, E. Venialgo, T. Gong, G. Borghi, D. R. Schaart, and E. Charbon, *A 67,392-SPAD PVTB-compensated multi-channel digital sipm with 432 column-parallel 48ps 17b tdcs for endoscopic time-of-flight pet,* in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (2015) pp. 1–3.

[2] F. Villa, R. Lussana, D. Bronzi, S. Tisa, A. Tosi, F. Zappa, A. Dalla Mora, D. Contini, D. Durini, S. Weyers, *et al.*, *CMOS imager with 1024 SPADs and TDCs for single-photon timing and 3-D time-of-flight,* IEEE J. Sel. Topics Quantum Electron. **20**, 364 (2014).

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Valeu!

# CURRICULUM VITÆ

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## EDUCATION

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*Thesis:* Modular time-of-flight image sensor for 3D light detection and ranging
*Promotor:* Prof. dr. E. Charbon
*Promotor:* Prof. dr. R. B. Staszewski

# List of Publications

## Conferences

1. **Ximenes AR**, Padmanabhan P, Lee MJ, Yamashita Y, Yaung DN, Charbon E. A 256× 256 45/65nm 3D-stacked SPAD-based direct TOF image sensor for LiDAR applications with optical polar modulation for up to 18.6 dB interference suppression. 2018 IEEE International Solid-State Circuits Conference (ISSCC) 2018 Feb 11 (pp. 96-98). IEEE.

2. Lee MJ, **Ximenes AR**, Padmanabhan P, Wang TJ, Huang KC, Yamashita Y, Yaung DN, Charbon E. A back-illuminated 3D-stacked single-photon avalanche diode in 45nm CMOS technology. 2017 IEEE International Electron Devices Meeting (IEDM) 2017 Dec 2 (pp. 16-6). IEEE.

3. Li CC, Tsai TH, Yuan MS, **Ximenes AR**, et. al., A 0.034 mm 2, 725fs RMS jitter, 1.8%/V frequency-pushing, 10.8–19.3 GHz transformer-based fractional-N all-digital PLL in 10nm FinFET CMOS. 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits) 2016 Jun 15. pp. 1-2. IEEE.

## Journals

1. **Ximenes AR**, Padmanabhan P, Lee MJ, Yamashita Y, Yaung DN, Charbon E. A Modular, Direct Time-of-Flight Depth Sensor in 45/65nm 3D-stacked CMOS Technology. IEEE Journal of Solid-State Circuits (JSSC). *Under review*.

2. **Ximenes AR**, Padmanabhan P, Charbon E, 2018. Mutually coupled time-to-digital converters (TDCs) for direct time-of-flight (dTOF) image sensors. Sensors, 2018(10), p.3413.

3. Lee MJ, **Ximenes AR**, Padmanabhan P, Wang TJ, Huang KC, Yamashita Y, Yaung DN, Charbon E. High-performance back-illuminated three-dimensional stacked single-photon avalanche diode implemented in 45-nm CMOS technology. IEEE Journal of Selected Topics in Quantum Electronics. 2018 Nov; pp. 1-9.

4. **Ximenes AR**, Vlachogiannakis G, Staszewski RB. An ultracompact 9.4–14.8-GHz transformer-based fractional-N all-digital PLL in 40-nm CMOS. IEEE Transactions on Microwave Theory and Techniques. 2017 Nov; pp 4241-54.

## Patents

1. **Ximenes AR**, Padmanabhan P, Charbon E, inventors; Ecole Polythenique Federale de Lausanne. Photon detecting 3D imaging sensor device. *Application*. PCT/EP2018/053340. 2018 Oct 11.

2. Vlachogiannakis GS, **Ximenes AR**, Staszewski RB, inventors; Short Circuit Technologies LLC, assignee. Fractional-N frequency synthesizer incorporating cyclic digital-to-time and time-to-digital circuit pair. United States patent US 9,722,537. 2017 Aug 1.

3. **Ximenes AR**, Staszewski RB, inventors; Short Circuit Technologies LLC, assignee. Split transformer based digitally controlled oscillator and DC-coupled buffer circuit therefor. United States patent US 9,401,677. 2016 Jul 26.

4. **Ximenes AR**, Staszewski RB, inventors; Short Circuit Technologies LLC, assignee. Split transformer based LC-tank digitally controlled oscillator. United States patent US 9,374,036. 2016 Jun 21.

## WORKSHOPS

1. **Ximenes AR**, Padmanabhan P, Charbon E, Mutually coupled ring oscillators for large array time-of-flight imagers, in International Image Sensor Workshop (IISW) 2017 (IISS, 2017) p. R25.

2. *(Invited)* **Ximenes AR**. Direct Time-of-Flight (dTOF) imaging for depth sensing applications. 10th Workshop on Design for 3D Silicon Integration. Grenoble - Minatec on 2-3 July 2018.

## PROJECTS

1. **Ximenes AR** - Project coordinator - NWO Take-off phase I, Feasibility Study No. 16525: *"LiDAR System for Advanced Driver Assistance System (ADAS) and Fully Autonomous Vehicles", April/2018 - October/2018.*