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DOI
10.1109/IEDM19573.2019.8993587

Publication date
2019

Document Version
Accepted author manuscript

Published in
2019 IEEE International Electron Devices Meeting, IEDM 2019

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Abstract

Perhaps the greatest challenge facing quantum computing hardware development is the lack of a high throughput electrical characterization infrastructure at the cryogenic temperatures required for qubit measurements. In this article, we discuss our efforts to develop such a line to guide 300mm spin qubit process development. This includes (i) working with our supply chain to create the required cryogenic high volume testing ecosystem, (ii) driving full wafer cryogenic testing for both transistor and quantum dot statistics, and (iii) utilizing this line to develop a quantum dot process resulting in key electrical data comparable to that from leading devices in literature, but with unprecedented yield and reproducibility.

Introduction

Quantum computing promises an exponential speedup over classical computing for broad applications spanning the entire economy. This has generated tremendous excitement in the field with significant research activity happening at the device/qubit, cryogenic circuit control, and quantum software/ algorithms level. Intel is actively working on every part of the quantum computing stack, with a particular focus on building a scalable system. At the device level, we are leveraging our expertise in transistor manufacturing to drive silicon based spin qubit research and development. Although there are many challenges facing quantum computing hardware development, perhaps the greatest is the lack of a high throughput electrical characterization infrastructure at the cryogenic temperatures required for qubit measurements. Since all key spin qubit electrical metrics are evaluated at temperature (T) < 2 K, it is not possible to leverage conventional high-volume transistor e-test techniques used by the semiconductor industry. This leads to a massive bottleneck in data collection as state-of-the-art cryogenic testing techniques cannot keep pace with the high volume wafer output of a semiconductor fab.

In this article, we discuss our efforts to develop a high volume cryogenic electrical characterization line for quantum computing. This includes (i) working with our supply chain to create the required cryogenic high volume testing ecosystem to guide 300mm spin qubit process development, (ii) driving full wafer cryogenic testing for both transistor and quantum dot statistics, and (iii) utilizing this line to develop a quantum dot process resulting in key electrical data comparable to that from leading devices [1,2] in the literature, but with unprecedented yield and reproducibility.

Device Design

A variety of different types of physical systems are currently being investigated to assess their viability for qubit applications. These include ion trap [3], superconducting [4], NV center [5], topological [6], and semiconductor quantum dot based approaches [1,2, 7-11]. Spin qubits formed in silicon quantum dots are extremely similar to transistors and naturally lend themselves to being compatible with conventional semiconductor manufacturing and scaling to very large number qubit arrays. We have developed a full 300mm device-integration process line for creating silicon based spin qubits using ^{28}Si epitaxy, shallow-trench isolation and high-k metal gates [8,9]. Figure 1a shows a schematic of such a quantum dot test structure highlighting adjacent plunger and barrier gates used to define the electrostatic potential in the device and confine and couple individual electrons. Additionally, the longer accumulation gates space the contacts far from the active region to eliminate spurious charging from the source/drain dopants. A corresponding cross sectional TEM image of a processed device is shown in Figure 1b.

Electrical Metrics

Similar to high volume transistor research and development, it is imperative to have a key list of metrics to trend and use to guide spin qubit device development. These are presented in Figure 2, and span from well understood transistor parameters to more complex quantum dot and qubit metrics. These metrics would typically be characterized for each of the individual plunger and barrier gates in the device, with many of the metrics needing to be extracted at cryogenic temperatures, such that kT is much smaller than the pertinent energy scales in the device. For example, simpler transistor metrics such as threshold voltage (V_T), subthreshold slope (SS), V_T matching, G_{mLIN}, and 1/f noise, with drain voltage (V_D) ~ 50mV and channel density ~ 1 to $5x10^{12}$ cm^{-2}, can be characterized and correlated across temperatures ranging from room temperature all the way down to T ~ 2K to 20 mK using cryogenic refrigerators. More complex quantum dot measurements such as charge drift, uniformity, noise, and charging energy related to the individual electron Coulomb blockade charging peaks can only be characterized at cryogenic temperatures less than 2K. These parameters are extremely sensitive to the cleanliness of the device from a charge disorder perspective and help quantitatively gauge the quality of the process and potential for achieving good qubit performance. The qubit metrics, including the spin relaxation time (T1), coherence time (T2*) and gate operation fidelity, are typically measured in dilution refrigerators at T~ 20mK. However, recent work has shown the potential to characterize these metrics at much higher temperature, with silicon based spin qubit T1 and T2* characterized at close to T=2K [10,11].

High Volume Cryogenic E-Test Ecosystem Development

Although our 300mm qubit integration line is able to generate a huge volume of wafer experiments in a short period of time, our ability to characterize them is completely bottlenecked by the lack of a high volume cryogenic testing ecosystem. State-of-the-art cryogenic refrigeration systems typically can only accommodate a few samples at a time. These devices typically need to be individually diced, wire-bonded, and mounted on a PCB carrier (Fig. 3a) and then loaded into cryogenic systems such as a dilution refrigerator (Fig. 3b). Accounting for this, along with thermal cycle time of the system, it can take several days to obtain characterization data from just a single device. In order to alleviate this bottleneck we have worked with our supply chain to create a high volume cryogenic testing ecosystem. Figure 4 shows a prototype Cryogenic Wafer Prober that was manufactured by Blue Fors, together with Afore. The tool enables capability to fully autoprobe a 300mm wafer, similar to that done in HVM transistor development, but at temperatures below 2K. To verify the wafer temperature, thermometry experiments (Fig. 5) were performed by gluing a heater and thermometer onto the wafer and cooling the system to base temperature, where the chuck reached T ~ 0.9K. The wafer temperature responds to the heat input as expected; without heat, the wafer exhibits a base temperature ~ 1.9K.

Figure 6 shows a spin qubit wafer undergoing automated testing at T ~ 1.9K, highlighting a cryogenic probecard aligned to the bondpads of our quantum dot testrow. A cross wafer map of V_T extracted from individual quantum dot barrier gates at T = 1.9K is plotted in Figure 7. Additionally, the cryogenic V_T plotted against the corresponding room temperature V_T is presented in Figure 8, showing the data are correlated with a systematic increase in V_T at low temperature. To help guide process development, V_T matching data taken from quantum dot barrier gates is shown in Figure 9 for two different barrier gate process conditions. While the improved process shows a significant improvement in room temperature variability, the corresponding matching data at T = 1.9K shows a weaker improvement, likely indicative of freezing out of defect states in the non-optimized process. This highlights that in order to really understand the disorder in our devices we need to correlate these statistical transistor data at room temperature and low temperature to statistics on quantum dot charging measurements. Cross wafer two-dimensional quantum dots scans at T = 1.9K are shown in Figure 10. Each panel plots the Coulomb blockade current against plunger (x-axis) and barrier (y-axis) gate voltage, with all other gates biased sufficiently above V_T. Such data can be used to (i) correlate to transistor metrics, (ii) screen for disorder and other non-ideal elements in the device, and (iii) identify promising candidates for dilution fridge qubit measurements. Although we verified our wafer is cooling to below 2K, we investigated the temperature dependence of the Coulomb blockade to check the actual device cooling. Varying the chuck from T = 7.2 to 0.9K, the data shows cooling does not saturate until below 2K, consistent with the wafer thermometry data. The FWHM of the peaks does appear to indicate some heating due to the large ~ 1 mV signal limitations on the commercial electronics used to collect the data. This highlights that quantum computing will also require a significant ecosystem development on the electronics end to provide commercial HVM test equipment that can meet the small signal and noise requirements needed for quantum dot and qubit characterization.

Dilution Fridge Quantum Dot Characterization

While high volume testing below T ~ 2K is imperative to generating statistical data to correlate to room temperature, guide process development, and screen for the highest quality devices, ultimately this data needs to be correlated to the final dot and qubit metrics obtained in a dilution refrigerator at T ~ 20 mK. Coulomb blockade data from high quality devices, selected from both room temperature and T ~ 2K screening, is plotted in Figure 12. The plunger gate is swept, while the adjacent gates are used to create a barrier potential. These data, from multiple devices at T=10 mK, indicate very high quality reproducible dot formation. The corresponding Coulomb diamond data measured at 10 mK is shown in Figure 13. This transport data is extremely clean and shows reproducible charging energies in the range of 6-8 meV. The larger charging energy we observe relative to many devices in literature arises from stronger confinement due to shallow-trench isolation, compared to typical electrostatic confinement used in academic devices. In Figure 14 we demonstrate tuneable tunnel coupling in these devices. The drain current is plotted as a function of P1 (x-axis) and P2 (y-axis) gate voltage for three different barrier voltages. The barrier voltage tunes the electron interaction from completely independent (large barrier) to a single large dot (small barrier). At medium barrier height, we observe two strongly tunnel coupled quantum dots, which is necessary in order to perform two-qubit operations. These Coulomb blockade, diamond, and tunnel coupling data are all comparable to leading edge devices in the literature [1,2] and attest to the high quality of the quantum dots fabricated in our full 300mm process line.

Conclusion

Quantum computing is generating tremendous excitement, with significant research activity happening around the world. However, perhaps the biggest obstacle facing qubit hardware development is the lack of a HVM cryogenic testing ecosystem. To address this we developed capability for high volume 300mm cryogenic automated testing, to guide process development and device screening, leading to quantum dots exhibiting key transport data comparable to leading edge devices in the literature. As we continue to advance this new testing capability, we look to strongly correlate data from all three testing platforms: room temperature e-test, cryogenic automated testing, and dilution fridge qubit characterization. Only by efficiently linking these platforms can we have the overall characterization capability to develop a qubit process that can be manufactured.

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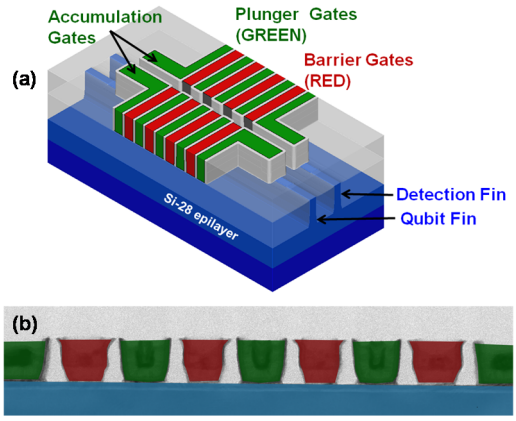

Fig 1: (a): Schematic of a quantum dot device showing multiple plunger, barrier, and accumulation gates, with active qubit and detection fins. (b) Cross-sectional TEM image through a qubit fin showing the various gates used to define the electrostatic landscape in the device and confine/couple individual electrons.

Transistor Metrics	295K	2K	20mK
Idlin / Gmlin			
Threshold Voltage			
VT Matching			
Subthreshold Slope			
1/f Noise; Vd ~ 50 mV, ns ~ 1 to 5x10^{12} cm^{-2}			
Quantum Dot Metrics	**295K**	**2K**	**20mK**
Blockade Uniformity			
Charge Drift			
Charging Energy			
Gate Capacitance			
1/f Noise; Vd ~ 100 uV, on blockade peak			
Qubit Metrics	**295K**	**2K**	**20mK**
T1 Spin Relaxation Time			
T2* Spin Coherence Time			
Single Qubit Gate Fidelity			
Two Qubit Gate Fidelity			

Fig 2: Key electrical metrics for semiconductor spin qubits; transistor, quantum dot and qubit e-test parameters and their applicable measurement temperature(s) are highlighted

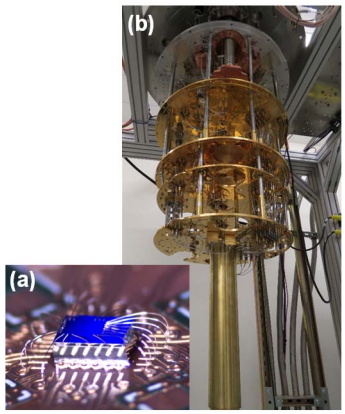

Fig 3: (a): A diced and fully wire bonded spin qubit test structure. (b) Dilution refrigerator at Intel's quantum computing lab used for quantum dot and qubit characterization at T < 20 mK.

Fig 4: Prototype Cryogenic Wafer Prober. The tool allows full 300mm e-test automation at a wafer temperature of T= 1.9K.

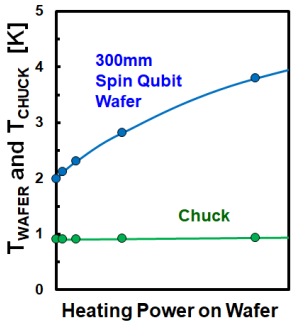

Fig 5: Chuck and wafer temperature vs heating power to the wafer. A thermometer and heater were glued to the wafer, with the chuck at base temperature of T=0.9K. Data indicates wafer is cooling below 2 K.

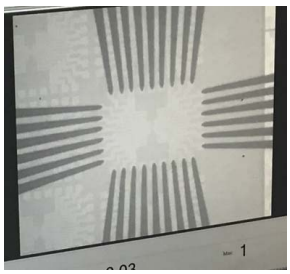

Fig 6: An Intel 300mm spin qubit wafer undergoing automated testing. A cryogenic probecard is shown aligned to the bondpads of a quantum dot testrow, at T = 1.9K.

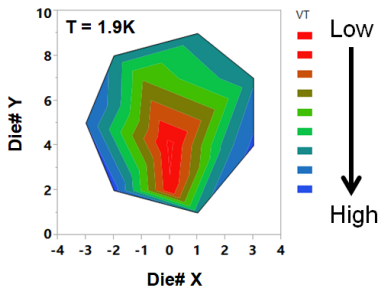

Fig 7: Cross wafer map of V_T of the barrier gates in a quantum dot gate testrow. The map is similar to those used in HVM, but is collected at T= 1.9K.

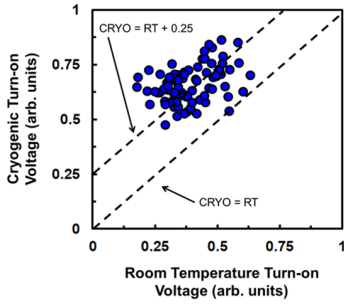

Fig 8: Cross wafer distribution of cryogenic V_T (T~ 1.9K) vs Room Temperature V_T across a full 300mm wafer. The data show correlation with a systematic increase in V_T at low temperature.

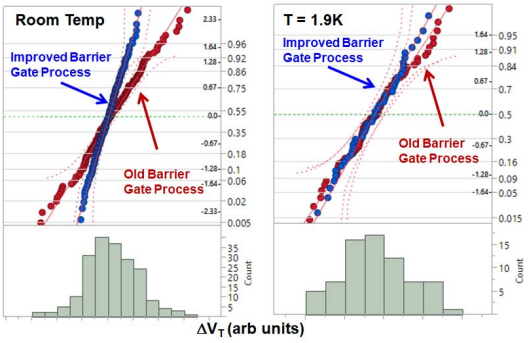

Fig 9: Barrier gate V_T matching data measured at room temperature (left) and at T = 1.9K (right). Data in red are from an un-optimized process with a degraded barrier gate interface. The blue data are from an improved process with a cleaner interface. Note that the variability improvement is less at cryogenic temperature.

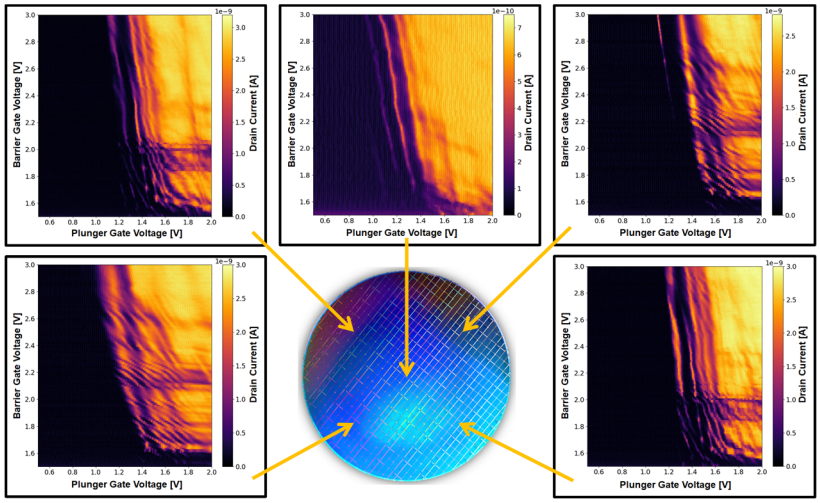

Fig 10: Cross wafer two-dimensional quantum dots scans at T = 1.9K obtained from fully automated measurements on the cryogenic wafer prober. Each panel plots the Coulomb blockade current against plunger (x-axis) and barrier (y-axis) gate voltage, with all other gates biased sufficiently above V_T. Such data can be used to (i) correlate to transistor metrics, (ii) screen for disorder and other non-ideal elements in the device, and (iii) identify promising devices for dilution fridge qubit measurements.

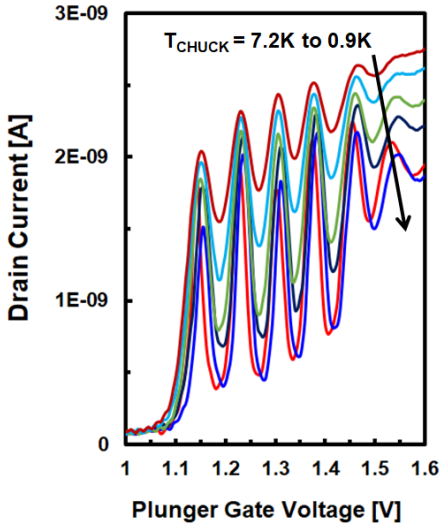

Fig 11: Temperature dependence of Coulomb blockade measured in the cryogenic wafer prober. Varying the chuck from T = 7.2, 5.5, 4, 3.2, 1.6 to 0.9K, the data indicates cooling to below 2K. The FWHM of the peaks does appear to indicate some heating due to the 1 mV signal limitations on the commercial electronics used to collect the data.

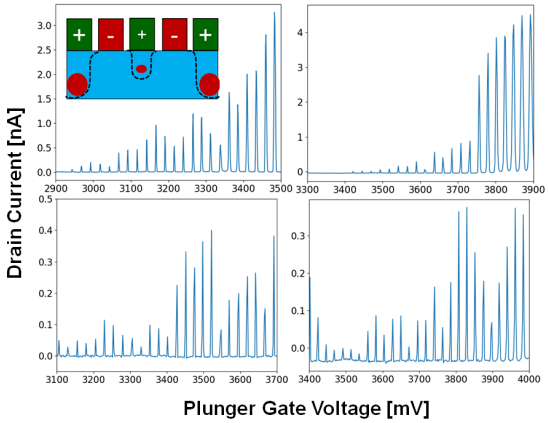

Fig 12: Coulomb blockade data measured at T = 10 mK. Each panel corresponds to data measured from different gates on different devices and indicate high quality reproducible dot formation. Inset: In the measurement the plunger gate (middle) is swept, while the adjacent gates are used to create a barrier potential. Other gates are biased to sufficient V_G-V_T to induce significant electron density.

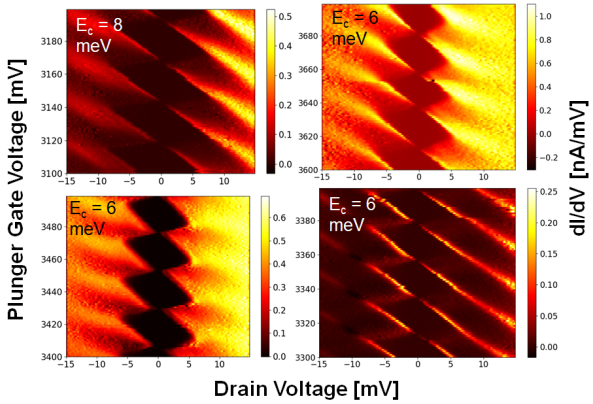

Fig 13: Corresponding Coulomb diamond data, measured at 10 mK, to the blockade data shown in Fig 12. The differential conductance is plotted against drain voltage (x-axis) and plunger gate voltage (y-axis). The data show reproducible charging energies in the range of 6-8 mV.

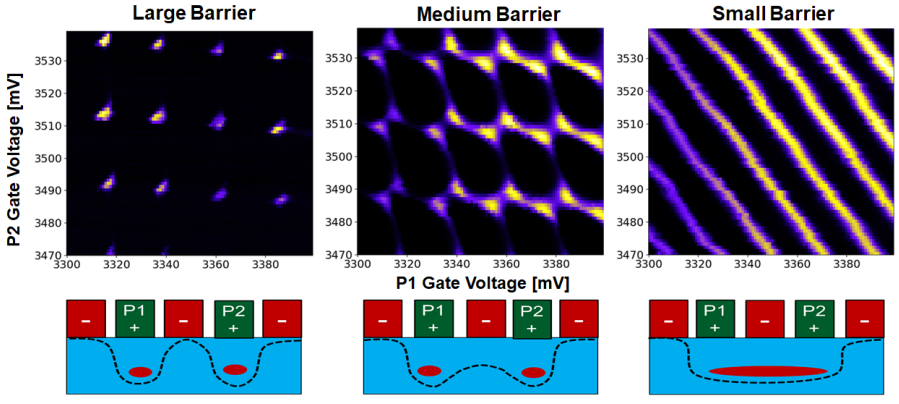

Fig 14: Demonstration of tunable tunnel coupling in a full 300mm processed quantum dot device. The drain current is plotted as a function of P1 (x-axis) and P2 (y-axis) gate voltage for three different barrier voltages. The barrier voltage tunes the electron interaction from completely independent (large barrier) to a single large dot (small barrier). At medium barrier height, we observe two strongly tunnel coupled quantum dots, which is necessary in order to perform two-qubit operations.