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***Abstract*—Resistive Random Access Memories (RRAMs) are now undergoing commercialization, with substantial investment from many semiconductor companies. However, due to the immature manufacturing process, RRAMs are prone to exhibit new failure mechanisms and faults, which should be efficiently detected for high-volume production. Some of those faults are hard-to-detect, and require specific Design-for-Testability (DfT) circuit design. This paper proposes a DfT based on a parallel-reference write circuit that can detect all single-cell RRAM array faults: strong faults (directly causing logic errors) as well as weak faults (caused by parametric deviations). The scheme replaces the regular write driver, and enables the monitoring and comparison of the write current against multiple references during a single write operation. Hence, it serves as a DfT scheme and as a normal write circuit simultaneously. In addition, it enhances production testing speed and online fault detection, while keeping the area overhead low. Furthermore, the DfT is configurable for efficient diagnosis and yield learning. The results of the simulations performed do not only show that the DfT can detect single-cell conventional faults (due to interconnects and contacts) as well as unique RRAM faults (based on silicon data) that have been demonstrated to exist, but also that the DfT is robust to process variations.**

***Index Terms*—RRAM testing, Defects, Faults, Diagnosis, DfT**

I. Introduction

Resistive Random Access Memory (RRAM) is a promising technology to ensure large non-volatile storage as well as new computing paradigm due to its benefits such as high scalability, low access latency, and energy efficiency [1, 2]. However, defects in devices during production and their impact on product quality pose substantial challenges [3]. In addition, the production of RRAM requires extra procedures and the utilization of novel materials, potentially leading to the appearance of new failure mechanisms [4, 5]. Moreover, the existence of parametric derivation degrades the memory block reliability, which may escape from traditional tests [6, 7]. Hence, it is crucial to have a thorough comprehension of manufacturing defects and develop high-quality test solutions.

Several works have focused on test solutions for RRAMs. These proposed solutions can be divided into two broad classes: March algorithms and specific Design-for-Testability (DfT) solutions. Examples of those March algorithms that involve specific sequences of memory operations are March-MOM [8], March W-1T1R [9], and March-CMOL [10]. While they are designed to optimize test time and enhance fault coverage, they only target interconnect and contact defects, and they are not designed to detect *unique defects* in RRAM devices (such as forming defects [3]) and Ion depletion [11]) causing *unique faults* such as undefined state faults [11]. Instead, DfT schemes, such as Weak Write operations [12], On-Chip Sensor [13], and DFT-HR-ET-NOR [14] are employed to detect those unique faults. However, they can only detect a part of this set of faults; they cannot guarantee the detection of the complete set of unique faults shown so far to exist. For example, the intermittent undefined state fault [15] only occurs *intermittently* during the write operation. Its detection cannot be guaranteed by Weak Write operations and DFT-HR-ET-NOR [14, 16]. The On-chip sensor may detect it; however, this DfT induces a large area overhead and requires hundreds of read operations to increase the detection probability. Also, the DfT in [16] fails to detect weak faults (as will be explained in detail in Section IV). Clearly, there is no test solution for RRAMs able to detect strong and weak faults, both due to conventional defects as well as unique defects in RRAMs.

This paper presents a new DfT scheme for RRAM memories. It monitors the write current and compares it against multiple references simultaneously. The DfT circuit replaces standard write drivers. The scheme can be used for manufacturing tests, diagnosis, yield learning, and even for in-field testing; it can detect defects that manifest themselves as a deviation in the write current. The DfT is adjustable such that e.g., the impact of process variability can be minimized. The main contributions of this paper are:

- Propose a multi-comparison write DfT scheme for the detection of RRAM (strong and weak) single-cell faults, in the presence of both conventional and unique defects.
- Implement and validate the DfT under process variations, and show that it outperforms the prior work. Silicon data measurements for unique RRAM defects are used.
- Demonstrate the reconfigurability of the DfT for different purposes such as optimizing yield loss and minimizing the impact of variability.

The rest of this paper is structured as follows. Section II establishes the RRAM basics. Section III classifies the targeted defects and faults in RRAM arrays. Section IV discusses the limitations of existing test solutions. Section V presents the proposed DfT. Section VI validates the DfT. Section VII develops a test for RRAMs. Section VIII discusses the work. Section IX concludes the paper.

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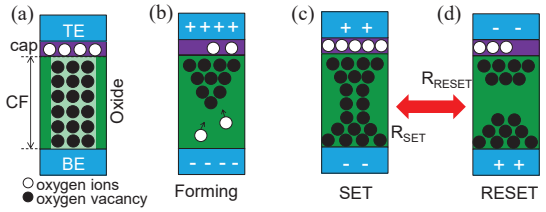


Fig. 1. Evolution of the conductive filament. (a) RRAM stack, (b) Forming, (c) SET, (d) RESET.

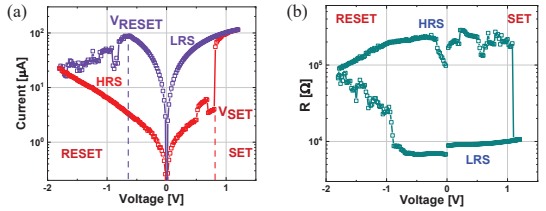


Fig. 2. RRAM electrical switching. (a) Switching I-V curve in log scale, (b) Switching R-V curve in log scale.

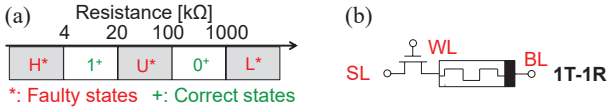


Fig. 3. RRAM technology. (a) RRAM resistance states, (b) 1T-1R cell.

II. RRAM Basics and Background

An RRAM device is a Metal-Insulator-Metal (MIM) stack, as shown schematically in Fig. 1 (a) [17]. In its organization, the middle metallic oxide is between the top and bottom metal electrodes (TE and BE), built with an extra capping layer (cap); the cap is widely used to serve as an oxygen reservoir, which thus facilitates switching performance. Typically, an RRAM device requires a forming process; it is a post-manufacturing step that involves applying a high voltage between two electrodes to form a *Conductive Filament (CF)* consisting of oxygen vacancies (OV), as shown in Fig. 1 (a).

Fig. 2 shows the switching current-voltage (I-V) and resistance-voltage (R-V) curves for an RRAM. The shape of the CF decides the different resistances of the device; the generation of more OV (Fig. 1 (c)), which is referred to as a SET operation, causes the CF length to rise when applying a positive voltage V_{TE} (across TE and BE) greater than a threshold V_{SET} [17]. Oppositely, the dissolution of the CF (see Fig. 1 (d)) is referred to as a RESET operation and takes place when $V_{\mathrm{TE}} \leq V_{\mathrm{RESET}}$.

The formation and dissolution of the CF is a result of the stochastic O^{2-} movement; this can cause cycle-to-cycle and device-to-device variations in the resistance [17]. Hence, the (binary) RRAM can be divided into 5 states, as shown in Fig. 3 (a) [18, 19]: 1) the faulty extremely high conductance state 'H', 2) the correct low resistive state '1', 3) the faulty undefined state 'U', 4) the correct high resistive state '0', and 5) the faulty extremely low conductance state 'L'.

Fig. 3 (b) shows a typical RRAM 1-Transistor-1-Resistor (1T-1R) cell with three terminals connecting with the Bit Line (BL), Source Line (SL), and Word Line (WL). The WL controls the transistor to make the data stored in the desired cells accessible. BLs and SLs are set to appropriate voltages for write (SET and RESET) and read operations.

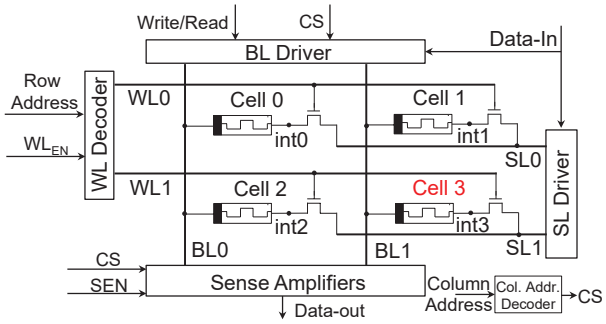


Fig. 4. Schematic of 1T-1R RRAM architecture [20, 21].

Fig. 4 presents a 2×2 1T-1R circuit architecture with related peripheral circuits [20]; it comprises the core memory cell array and peripheral circuits. Cells in the same row share the same WL and SL, while those in the same column share the same BL. The peripheral circuit consists of the WL decoder, BL/SL drivers, and Sense Amplifier (SA). The decoder selects cells, the driver provides write and read currents, and the SA senses the current through the device to read cell states.

III. Targeted RRAM Defects and Faults

This section defines and classifies defects and faults in RRAM arrays, which are considered in this work. We target mainly single-cell faults.

A. RRAM Defects

In this work, we consider both conventional and unique RRAM defects. The former is studied in other memory technologies, while the latter only occurs in RRAM devices.

1) RRAM Conventional Defects: Conventional defects consist of interconnect and contact defects in RRAM arrays, an example is a poorly placed contact [20, 22]. They are typically *modeled* by *linear resistors* [23, 24], and classified into three types: 1) a *bridge* being defined as a resistor between a pair of nodes different from the power nodes, 2) a *short* being an undesired resistive path between a node and a power node (V_{DD} or GND), and 3) an *open* being an increased resistance in an existing connection.

2) RRAM Unique Defects: These are defects that occur inside the RRAM device itself during the manufacturing; defects that have been shown to exist (based on silicon data) so far consist of: 1) an Over/Under Forming (O/UF) defects [3, 19], 2) a low-doping of the capping layer [15], 3) an Ion Depletion (ID) [11, 25], and 4) an Over RESET (OR) [26]. It has been shown that these defects cannot be accurately modeled with linear resistors; therefore, Device-Aware Test (DAT) approach is used for their modeling [3, 27].

B. RRAM Faults

Manufacturing defects can lead to erroneous behavior or a derivation from the correct behavior. Those behaviors are modeled as faults (or fault models) on the functional level. The Fault Primitive (FP) notation is well-known notation used to systematically describe such faults in a compact manner [22]; an FP is denoted as $\langle \mathrm{S/F/R} \rangle$, where S represents the

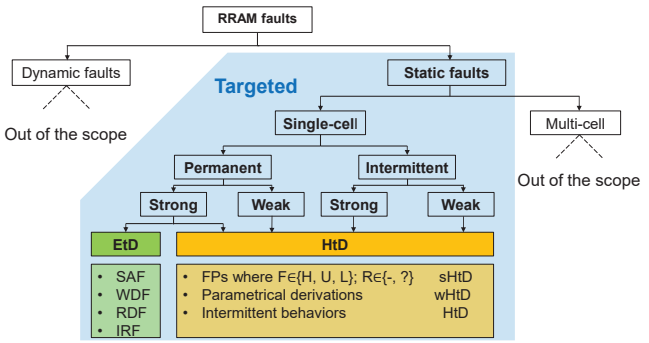


Fig. 5. Fault classification depends on functionality and permanent nature.

sensitizing operation sequence, F represents the cell state after the operation, and R represents the output if the final operation in S is a read operation. For instance, when a sensitizing operation $0r0$ ($\mathrm{S} = 0\mathrm{r}0$) (i.e., apply read 0 operation to a cell with initial state 0) to an HRS cell causes the cell to flip to an undefined state 'U' (i.e., $\mathrm{F} = \mathrm{U}$) and the read output returns '1' ($\mathrm{R} = 1$) rather than the intended '0', then the FP $=\langle 0\mathrm{r}0/\mathrm{U}/1\rangle$.

Fig. 5 shows the targeted RRAM faults in this work, being *static* faults; note that static faults are those sensitized by performing *at the most* one operation; while dynamic faults are those sensitized by performed more than one operation *sequentially* [28].

Depending on the number of involved cells, faults can be divided into *Single Cell (SC)* faults and multi-cell faults (not targeted here). Note that SC faults are those involving at most one cell (which could be the aggressor and the victim at the same time [20, 22]); while multi-cell faults are those involving at least one victim cell and one aggressor cell.

Depending on how long they last, faults can be divided into *permanent* and *intermittent*; permanent faults are permanently present in the memory irrespective of the time of access, while intermittent faults are faults that occur at intervals, usually irregular.

Depending on whether they cause functional errors or not, faults can be divided into *strong* and *weak* [20]; strong faults always cause functional errors even at time zero; while a weak fault does not cause any functional errors but parametric deviations (out of the spec) such as a voltage drop in the BL during a writing operation.

Moreover, and depending on the ease of their detection, strong faults can be classified between *Easy-to-Detect (EtD)* and *Hard-to-Detect (HtD)* faults. EtD faults are those *guaranteed* to be sensitized and detected by regular memory operations; while strong HtD (sHtD) faults are those that cannot be guaranteed to be detected with write/read operations. For example, write/read operations cannot guarantee 100% the detection of the fault, $\langle 0\mathrm{r}0/0/?\rangle$ as a read output has a probability to be either '1' or '0' [20]. Note that weak faults are HtD by nature (wHtD faults).

In this work, we target static single-cell faults that have been shown to exist in RRAMs (either based on defect injection and circuit simulation or based on silicon data), which are either EtD or HtD, as shown in Fig. 5. The EtD static fault consists of [5, 18, 28, 29]:

- Stuck-at Faults (SAF): the RRAM cell is always in a certain state, e.g., $\langle 0\mathrm{w}1/0/-\rangle$.
- Write Destructive Faults (WDF): unintentional alteration of the state of the cell during a write operation, e.g., $\langle 0\mathrm{w}0/1/-\rangle$ and $\langle 1\mathrm{w}1/0/-\rangle$.
- Read Disturb Faults (RDF): a read operation switches the cell state, while the read value is correct, e.g., $\langle 0\mathrm{r}0/1/0\rangle$.
- Incorrect Read Fault (IRF) a read operation returns an incorrect output while the cell state is correct, e.g., $\langle 0\mathrm{r}0/0/1\rangle$ and $\langle 1\mathrm{r}1/1/0\rangle$.

The HtD static faults consist of [8, 15, 18, 30]:

- Deep Faults (DF): the RRAM cell falls into deep states, i.e., 'H', 'L', e.g., $\langle 1\mathrm{w}0/\mathrm{L}/-\rangle$.
- Undefined Write Faults (UWF): a write operation leads to 'U' state, e.g., $\langle 1\mathrm{w}0/\mathrm{U}/-\rangle$.
- Unkown Read Faults (URF): a read operation switches the cell to 'U' state ($\mathrm{F} = \mathrm{U}$) and/or returns random read outputs ($\mathrm{R} =?$), e.g., $\langle 1\mathrm{r}1/\mathrm{U}/?\rangle$.
- Weak faults: parametric deviations of RRAMs without functional errors.
- Intermittent Undefined State Faults (IUSF): RRAM intermittently switches into 'U' states during write operations.

Note that HtD faults are mainly unique to RRAMs; RRAM can store at most five states and thus detecting faults due to such states cannot be guaranteed with existing March tests. Due to the process variation and intrinsic stochasticity in RRAM switching, non-permanent faults occur intermittently, such as the IUSF. Weak faults in RRAMs are caused by degradation or extreme cycle-to-cycle variations [31], especially in the case of RRAM filaments, which have natural randomness in their formation and breakage.

IV. Limitation of Existing Works

Existing tests for RRAMs can be divided into March algorithms and DfT schemes. Table I summarizes all of these tests along with the types of RRAM faults (classified in III-B) that can detect. The DfT schemes generally have two targets: 1) reduce test time (RT), and 2) enhance test coverage (EC). The targets are listed in Table I for each of the DfTs. For example, 'Divide and Conquer approach' DfT [33] is proposed to leverage upon the special current additive property, thus reducing test time. The DfT schemes in [8, 35] read multiple cells at once and thus reduce the number of read operations. However, [35] is not designed to enhance the FC. On the other hand, the DfT schemes in [13, 16] modify and apply multi-reference read operations to enhance the FC. Note that [16] is the only scheme that is able to partially detect intermittent faults since it can monitor the cell states continuously. In [36], an approach that can monitor the RRAM state ratio is presented for detecting read disturb faults; however, it requires testing 32 RRAM parallel cells at once. Furthermore, the DfT schemes in [14, 18, 30, 34] are designed to enhance the FC and reduce the test time by modifying the write or read operations.

TABLE I
TARGETED FAULT DETECTION CAPABILITIES OF EXISTING TESTS FOR RRAMS.

Name	Type	Permanent			Intermittent		Target
		Strong		Weak	Strong	Weak	
		EtD	sHtD	wHtD			
March-MOM [8]	March	Y	N	N	N	N	-
March-1T1R [29]	March	Y	N	N	N	N	-
March C* [19]	March	Y	N	N	N	N	-
March C*-1T1R [32]	March	Y	N	N	N	N	-
March-CMOL [10]	March	Y	N	N	N	N	-
March W-1T1R [9]	March	Y	N	N	N	N	-
March-EtD [21]	March	Y	N	N	N	N	-
Divide and Conquer [33]	DfT	Y	N	N	N	N	RT
Sneak-path [8]	DfT	Y	P	N	N	N	RT
Weak-write [18]	DfT	N	Y	N	N	N	RT; EC
Fast-write [34]	DfT	Y	Y	N	N	N	RT; EC
Parallel March [35]	DfT	Y	P	N	N	N	RT
On-chip sensor [13]	DfT	Y	P	N	N	N	EC
Enhanced March [30]	DfT	Y	Y	N	N	N	RT; EC
DFT-HR-ET-NOR [14]	DfT	Y	Y	N	N	N	RT; EC
Read disturb fault detector [36]	DfT	Y	N	N	N	N	EC
PMRR [16]	DfT	Y	Y	N	Y	N	EC

Y: yes, N: no, P: partial, RT: reduce test time, EC: enhance test coverage

However, none of the existing DfT schemes can guarantee the detection of weak faults. Besides, some DfT approaches can only partially detect sHtD faults; i.e., they cannot cover faults that switch the cell into faulty states 'H', 'U', or 'L', resulting in test escapes. The state-of-the-art clearly shows that none of the existing tests detect all single-cell RRAM faults reliably and efficiently.

V. PROPOSED DFT METHODOLOGY

This section proposes the overall concept of the DfT, and demonstrates details on how it is implemented to efficiently detect all targeted single-cell RRAM faults in this work.

A. DfT concept

Based on the discussion from previous sections, we can derive that a high-quality DfT scheme for RRAMs should be able to detect specific faulty states ('H', 'U', and 'L' states) as well as weak faults (to enhance the chip's reliability). Furthermore, to detect aging degradation and intermittent behavior, the test should be performed during the runtime of the chip (e.g., online monitoring). For example, this is the case for ID defects reported in [11] which cause intermittent undefined write faults.

To detect the targeted RRAM faults, we design a new DfT based on monitoring and comparing two currents. We marginally modify the write drivers, and monitor the currents during the write operation; thus achieving a test without additional read operations. As explained in Sec II, the write operation is performed by write drivers. For instance, during the SET operation, and as shown in Fig. 6 (a), currents from the write driver flow into the RRAM cell through BL (I_{BL}) and out of the cell through SL (I_{SL}). Depending on the magnitudes of such currents, four cases can be distinguished as shown in the table of Fig. 6 (b). For a defect-free circuit, I_{BL} is expected to be the same as I_{SL}, both are within the specification (Case 1). However, the presence of defects (e.g., shorts, bridges) may cause one (Cases 2 and 3) or both (Case 4) of these currents to be out of the specification.

For example, Fig. 6 (c) shows the amplitude of the two currents I_{BL} and I_{SL} during a write ($0w1$) operation in the presence of short defect as shown at the bottom of the same figure. The figure shows that the difference between the two currents is higher for smaller defect sizes (Case 4). As the BL is shorted to the ground in the presence of the defect, I_{BL} is higher than the correct value (out of the specification), and only a small current will flow through the RRAM device; hence I_{SL} is smaller than the correct value (out of the specification). As a consequence, the cell will fail to switch and it will remain in its initial state '0'. As the defect resistance increases, the shortcut current through the defect will reduce, resulting in a reduction of I_{BL} and an increase of I_{SL} following through the RRAM device. As the figure shows, in this case (Case 2), I_{BL} remains still larger than specification while I_{SL} reaches the correct value. When the defect resistance increases further, both I_{BL} and I_{SL} converge towards correct values (Case 1) as the impact of the defect becomes marginal. Note that Fig. 6 (c) uses the same colors as the table in Fig. 6 (b) to indicate the different regions/cases.

Fig. 6 (d) presents another example where a write 0 transition operation (1w0) is performed in the presence of a short. Depending on the defect value, three cases ((1), (3), and (4)) are sensitized. Note that for Case 4, although the two currents I_{BL} and I_{SL} are quite the same, their value is possibly outside the specification (e.g., in the presence of open defects) and therefore it is a faulty case.

Fig. 7 gives a high overview of the DfT process. First, the two currents I_{BL} and I_{SL} are compared (i.e., stage 1); if they are not close to each other within a certain (i.e., one of the two currents is outside the specification), then obviously there is a defect causing this deviation (Case 2 or Case 3). If the two currents are quite close to each other, we proceed to stage 2, where we verify whether the current value falls

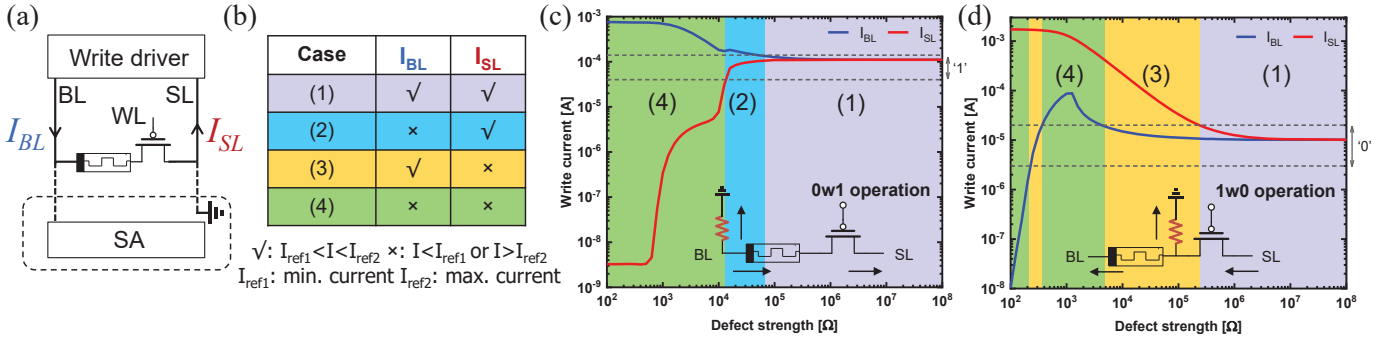


Fig. 6. The concept of I_{BL} and I_{SL} conditions during the write operation. (a) The circuit high-level overview, (b) Four conditions of I_{BL} and I_{SL}, (c) I_{BL} and I_{SL} behavior as a function of one short defect located at the BL node, (d) I_{BL} and I_{SL} behavior as a function of one short defect located at the RRAM/transistor interconnection.

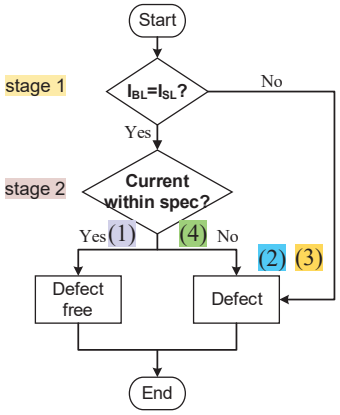


Fig. 7. The flow chart of the proposed DfT process.

within the specified range. If it is, then clearly the design under test is defect-free (Case 1). However, if the current is out of specification, then the circuit is defective (Case 4).

B. Potential implementations

The proposal DfT is based on a comparison of I_{BL} and I_{SL}. This concept of checking current differences and magnitude can be applied not only to write operations but also to read operations. For example, Gomez *et al.* modifies the read operation to check the current difference in MRAMs [37]. The advantages of such an approach are low power consumption and detection of some read faults. However, it has many drawbacks: 1) the need to have the additional read operation for detection after writing the cell, 2) the slight read current is hard to sense, and 3) able to check (read) currents only in one direction. In comparison with checking the difference between read currents, checking the difference between write currents is much more favorable; i.e., it allows the real-time monitoring of the write current and test of the circuit without additional read operations, which is preferred for both defect and reliability testing. Therefore, we select that approach for the implementation of the proposed DfT concept.

C. Selected implementation

Based on the above analysis, we propose to modify the basic write circuit (i.e., write drivers) to measure the difference between the write current flowing into and out of any cell. Besides, we check whether the current is within the specification during the write operation.

Fig. 8 shows the selected implementation of the proposed DfT. The figure shows the specific circuit design for one cell of the array and its modified write drivers (BL driver and SL driver). In the figure, we mark the $w1$ current path as a blue line. During the SET ($w1$) operation, the current flows through transistors P1, P2, and BL, via the RRAM device through the access transistor, into the SL (N2, N1). The current flowing into the cell is $I_{\mathrm{BL}}(w1)$ (via P1, P2), while the current out of the cell is $I_{\mathrm{SL}}(w1)$ (via N2, N1).

The proposed implementation has two stages, as shown in the figure. Stage 1 checks if the difference between the two currents $I_{\mathrm{BL}}(w1)$ and $I_{\mathrm{SL}}(w1)$ is out of the specification, resulting in detection, e.g., of Case 2 with $X0X1 = 11$ if $I_{\mathrm{BL}}(w1)<I_{\mathrm{SL}}(w1)$ and with $X0X1 = 00$ if $I_{\mathrm{BL}}(w1)>I_{\mathrm{SL}}(w1)$. In case this current difference is small (resulting in $X0X1 = 10$), then stage 2 will be used to check if the magnitude is within the specification or not. In the defect-free case, $X2X3 = 10$; otherwise, $X2X3 = 11$ or 00 detecting the fault. Note that stage 1 and stage 2 consist each of two branches. $I_{\mathrm{BL}}(w1)$ and $I_{\mathrm{SL}}(w1)$ are mirrored (via P1 and N1) in each of these branches, which drives the four detection outputs $X0$ to $X3$.

In stage 1, as I_{BL} and I_{SL} may exhibit slight deviations as a result of process variation and non-idealities, the two branches are applied together to set a safe margin of the current difference and guarantee a stable output for the defect-free circuit. For example, the transistor sizes of P4 and N5 are the same as P1 and N1 (the width of P1 is 3 times larger than N1 to achieve the same driving capability); while the transistor sizes of P5 and N4 are r times that of P1 and N1. In this setting, P4 and P5 copy the current from P1 to $I_{\mathrm{BL}}(w1)$ and $r*I_{\mathrm{BL}}(w1)$; N4 and N5 copy the current from N1 to $r * I_{\mathrm{SL}}(w1)$ and $I_{\mathrm{SL}}(w1)$. Hence, the outputs of $X0$ and $X1$ are according to the current difference. For example, if I_{BL} is close to I_{SL} with the specification (i.e., $1/r * I_{\mathrm{SL}}<I_{\mathrm{BL}}<r * I_{\mathrm{SL}}$), then $(X0X1)$ will be set to '10'; if $I_{\mathrm{BL}}>r*I_{\mathrm{SL}}$, then $(X0X1)$ will be set to '00'; and if $I_{\mathrm{BL}}<1/r * I_{\mathrm{SL}}$, then $(X0X1)$ will be set to '11'. The choice of r value is based on the consideration of process variation, and it is assumed to be 1.2 in our design; the analysis and influence of r will be further discussed in Sec VIII. Note that the output $X0X1 = 10$ indicates the presence of Case 1 (defect-free) or Case 4; hence an additional check is needed.

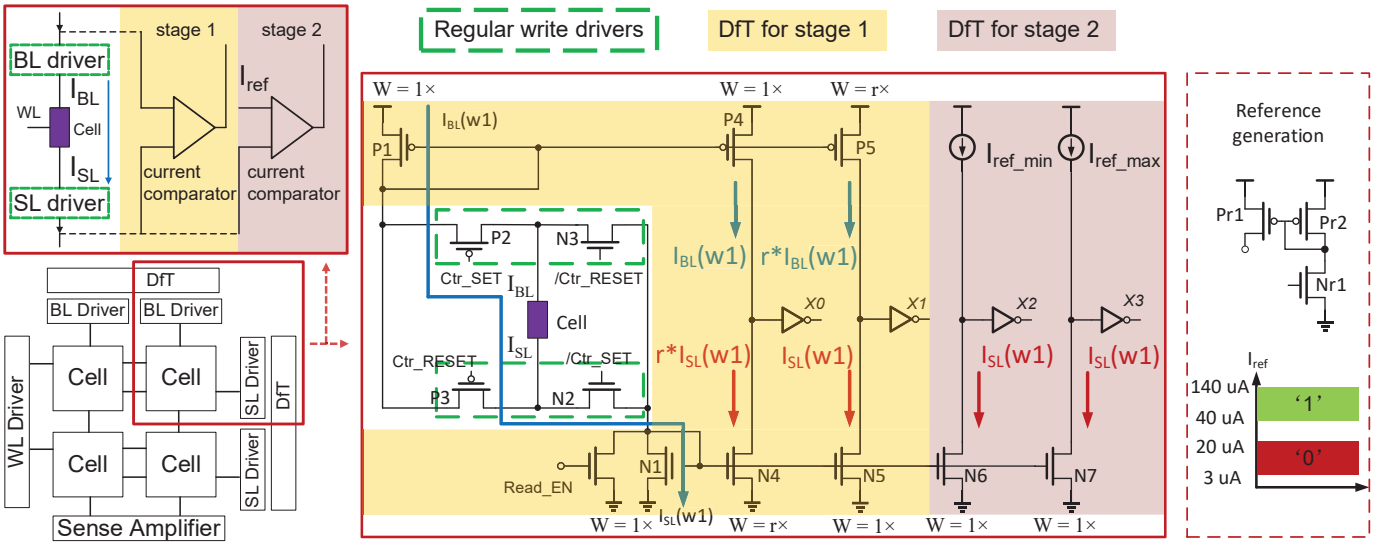


Fig. 8. Modified write driver circuit acting as DfT.

In stage 2, the additional check is performed. The two branches are applied to compare the cell current to two specific reference currents (the minimum and maximum of the correct write current). N6 and N7 copy the current following through N1. If the mirrored current is within the correct boundaries, then outputs of $X2X3$ will be set to '10'. Otherwise, $X2X3$ will be set to '11' (when $I_{\mathrm{SL}}{>}I_{ref-max}$) or to '00' (when $I_{\mathrm{SL}}{<}I_{ref-min}$). The reference currents are generated using the controlled transistor (Nr1) and current mirror (Pr1, Pr2) as shown in the red dotted box of Fig. 8. Adjusting the width and length of Nr1 allows the selection of the right reference current. The correct current range is determined based on the five resistance state values introduced in Sec II.

DFT implementation for monitoring the $w0$ current, which flows in opposite directions as compared to $w1$ current, uses the same principles.

VI. Verification of DfT Methodology

This section shows the verification of the proposed DfT circuit. First, we briefly present the simulation setup of this work. Then, through simulation results, we illustrate the DfT of this work, its advantages compared with previous works. Finally, we analyze the impact of process variations and the robustness of the proposed circuit.

A. Simulation setup

To validate the proposed DfT, we implement a 2×2 RRAM array circuit shown in Fig. 4 with read circuits and proposed write drivers. We use the TSMC $40\,\mathrm{nm}$ $2.5\,\mathrm{V}$ transistor model, and the physics-based JART VCM v1b [38] RRAM compact model to implement the circuit. The RRAM model is designed for BS in a Valence Change Mechanism (VCM)-based device as the change of oxygen vacancies in the HfO_2 oxide layer. We applied the JART VCM v1b model to calibrate the defect-free measurement data. The measured (calibrated) 1T-1R device is fabricated by ST Microelectronics, with the stack of (BE/oxide/cap/TE) = (TiN/$10\,\mathrm{nm}$ HfO_2/$10\,\mathrm{nm}$ Ti/TiN) [11, 26]. The switching in a nominally defect-free device is bipolar. The spec of five resistance states are defined as shown in Fig. 3. Logic '1' is represented by the LRS with $4\,\mathrm{k\Omega}{<}R_{\mathrm{SET}}{<}20\,\mathrm{k\Omega}$, and logic '0' by the HRS with $100\,\mathrm{k\Omega}{<}R_{\mathrm{RESET}}{<}1\,\mathrm{M\Omega}$. The remaining range $[20\,\mathrm{k\Omega}, 100\,\mathrm{k\Omega}]$ is referred to an undefined state ('U'). For simulation purposes, the switching can be described as the ionic migration of oxygen vacancies (OV), which influences the Schottky barrier and, subsequently, the electrical conductivity of the VCM device [38]. N is the parameter used in the model simulation to calculate the OV concentration in the cell and thus affect the resistance state in the RRAM model. N_{min} and N_{max} are limiting parameters to keep N between N_{min} and N_{max} in RESET and SET processes. Fig. 9 shows the fitting result of the I-V loop for the defect-free cell; the fitting parameter values use the same setting as in [26]. The circuit is simulated in Cadence's Spectre simulator. The nominal supply voltage for the memory is $2.5\,\mathrm{V}$. In order to accurately evaluate the circuit, capacitive loads are applied to BLs, SLs, and WLs in the simulation. The defect-free circuit is validated by performing write and read operations within specified design parameters; no faults are sensitized during the applied operations.

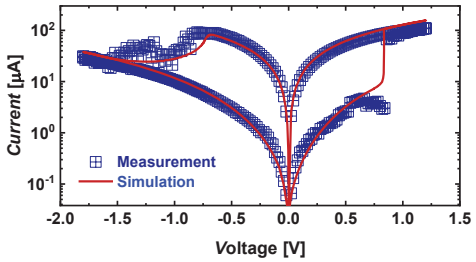
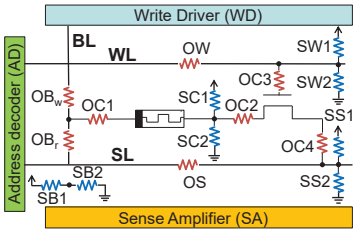


Fig. 9. Simulation vs. measurements of the I-V curve.

We perform three experiments:

1) *Process Variation Analysis for Defect-free circuit*: to validate the feasibility of the DfT circuit, the impact of process variations on the functionality of the circuit is simulated. Here, we perform a sensitivity analysis to study the influence of



Opens	Location	Shorts	Location
OC1	BL_int	SC1	int-V_{DD}
OC2	int	SC2	int-GND
OC3	WL_int	SB1	BL-V_{DD}
OC4	SL_int	SB2	BL-GND
OW	WL_ad	SW1	WL-V_{DD}
OS	SL_ad	SW2	WL-GND
OB_w	BL_WD	SS1	SL-V_{DD}
OB_r	BL_SA	SS2	SL-GND

Fig. 10. Open and short defect locations.

TABLE II
BRIDGE DEFECT LOCATIONS.

Bridges	Location	Bridges	Location	Bridges	Location
BC1	BL1-int3	cBCC3	int1-SL1	rBCC2	BL0-int3
BC2	BL1-WL1	cBCC4	WL0-int3	rBCC3	int2-BL1
BC3	BL1-SL1	cBCC5	WL0-WL1	rBCC4	int2-int3
BC4	int3-WL1	cBCC6	WL0-SL1	dBCC1	int0-BL1
BC5	int3-SL1	cBCC7	SL0-int3	dBCC2	int0-int3
BC6	WL1-SL1	cBCC8	SL0-WL1	dBCC3	int0-WL1
cBCC1	int1-int3	cBCC9	SL0-SL1	dBCC4	int0-SL1
cBCC2	int1-WL1	rBCC1	BL0-BL1		

both cell transistors and RRAM devices. For the transistor variations, we use the variation models that include the statistical mismatch from the TSMC $40\,\mathrm{nm}$ model library. For RRAM device variations, we set up the models as described in [39]. We incorporate both Device to Device (D2D) (from a truncated Gaussian distribution) and Cycle to Cycle (C2C) (change the variable parameters with confined step size, whose maximum is chosen to be $10\,\%$ of the current value) variations of the RRAM cells. For every component combination, we perform 10000 Monte Carlo (MC) simulations, in which all static operations are performed per iteration. For every MC iteration, we record three metrics: 1) write currents, 2) the number of strong faults (functional errors), and 3) the number of incorrect outputs of the DfT scheme.

2) *Detecting Conventional Defects*: we validate the DfT's defect-detecting capabilities by injecting resistive defects into the netlist (the cell array shown in Fig. 4), using a similar simulation platform in [21]. Conventional defects are modeled as linear resistances and injected in the circuit array, one defect at a time. The defect size ranges from $1\,\Omega$ up to $100\,\mathrm{M}\Omega$ in 81 logarithmically spaced steps. In this paper, we consider the complete intra-cell and inter-cell defect space of opens, shorts, and bridges. 8 opens and 8 shorts are injected in one cell for simplification, as listed in Fig. 10. OX is used to denote the opens $(\mathrm{OX}, \mathrm{X} \in \{\mathrm{C}\,(\text{inside the cell}),\ \mathrm{W}\,(\text{in the WL}),\ \mathrm{S}\,(\text{in the SL}),\ \mathrm{B_{w/r}}\,(\text{on the write/read side of BL})\})$, SX is used to denote the shorts $(\mathrm{SX}, \mathrm{X} \in \{\mathrm{C}, \mathrm{W}, \mathrm{S}, \mathrm{B}\})$. Bridges are injected between each pair of nodes in the circuit. They are considered only between at most two adjacent cells (C3 in Fig. 4 is the based cell), which provide three possible locations: cells in the same column, cells in the same row, and cells in the same diagonal. There are 6 intra-cell bridges (denoted as BCn, n from 1 to 6) and 17 inter-cell bridges (denoted as $\mathrm{xBCC}, \mathrm{x} \in \{\mathrm{c}, \mathrm{r}, \mathrm{d}\}$), as listed in Table. II. We apply all static sensitizing sequences: 0w0, 0w1, 1w0, 1w1, 0r0, 1r1.

3) *Detecting Unique Defects*: we inject the following five RRAM unique defects known in the public domain: OF, UF [3], IUSF [15], ID [11, 25], and OR [26] (see Section III). These defects are modeled using a *device-aware* defect modeling approach that incorporates the physical behaviors of the defective device [3, 27]. Fig. 11 (a) presents the dependence between resistances and forming currents. Larger (OF) or smaller (UF) forming currents may make the cell switch into an incorrect state. Fig. 11 (b) presents measurements of IUSF-defective and defect-free devices. The faulty switching behavior results in a 'U' state during SET operation. Fig. 11 (c) presents measurements and simulations of ID-defective and defect-free devices. The faulty switching behavior results in a 'U' state during RESET operation. Fig. 11 (d) presents measurements and simulations of OR-defective and defect-free devices. The faulty switching behavior results in an 'L' state during RESET operation. We inject unique defects in the memory cell by replacing the RRAM model with developed DAT models, one defect at a time. Those DAT models are calibrated with silicon data (the 1T-1R arrays fabricated by ST Microelectronics) and applied in this work. Specifically, we simulate the defect strength that can sensitize unique faults to validate the proposed DfT. In this work, the defect strength is represented by values of the following fitting parameters: radius of the filament (r_{det}) for O/UF defects, N_{max} for IUSF, and N_{min} for ID, and OR defects.

B. Results

Next, we present the verification results. First, we validate the correctness for the defect-free circuit with process variation analysis. Second, we present the result for the detection of conventional defects. Third, we present the results for the detection of unique defects.

1) *Process Variation Analysis for Defect-free Circuit*: Fig. 12 (a) and (b) show histograms for the SET and RESET current flowing through the cell of the defect-free circuit, for 1000 MC simulations. The mean value (μ) of the SET current is $111.31\,\mu\mathrm{A}$, conforming to the $3\,\sigma$ design specification (with standard deviation, σ, of 8.52). Similarly, the mean value (μ) of the RESET current is $10.57\,\mu\mathrm{A}$, also aligning with the $3\,\sigma$ design specification (with standard deviation, σ, of 1.82). Currents are normalized to the mean values and shown in Fig. 12 (a) and (b). The RESET current variation spread is more pronounced than SET, which is also reported in other papers such as [40]. Upon validation of write operations under the process variation, $100\,\%$ of the 40000 write operations result in the correct DfT output, demonstrating fault-free.

2) *Detecting Conventional Defects*: The validation of the detection capability of the DfT scheme is valued by the detected fault numbers and the defect coverage. Fig. 13 shows faults that are sensitized with related sensitizing sequences and defect strengths for one inter-cell bridge defect cBCC4 (see Table II). The figure illustrates faults that are sensitized by each applied sequence ('S'), together with the defect strength range. We only show write operations since the DfT is based on write current measurement. The green shapes indicate ranges for EtD faults, the orange shapes indicate ranges for sHtD faults, the blue shapes indicate ranges for weak faults, the gray shapes

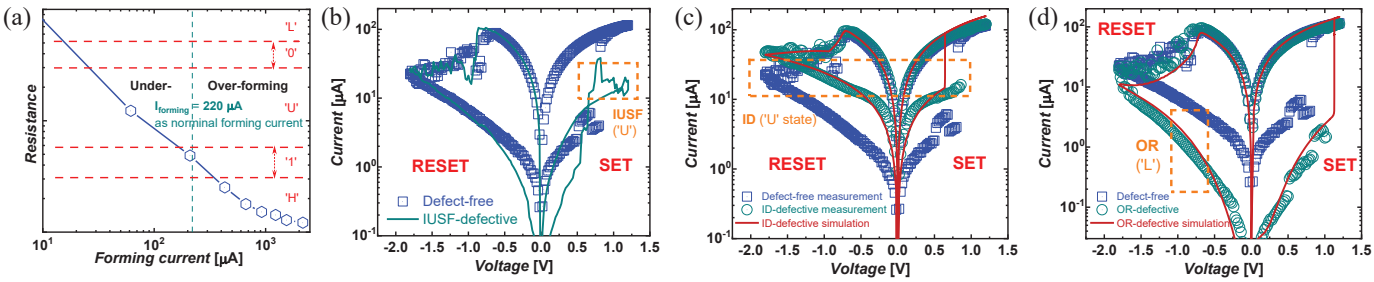


Fig. 11. Targeted unique defects. (a) Characterization of forming defects [3, 4], (b) Comparison of IUSF-defective and defect-free devices [15], (c) Comparison of ID-defective and defect-free devices [11], (d) Comparison of OR-defective and defect-free devices [26].

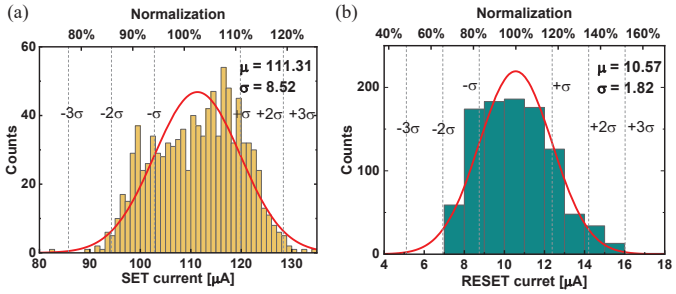


Fig. 12. Histograms of the current distribution of defect-free circuit under variations. (a) SET ($0w1$) current, (b) RESET ($1w0$) current.

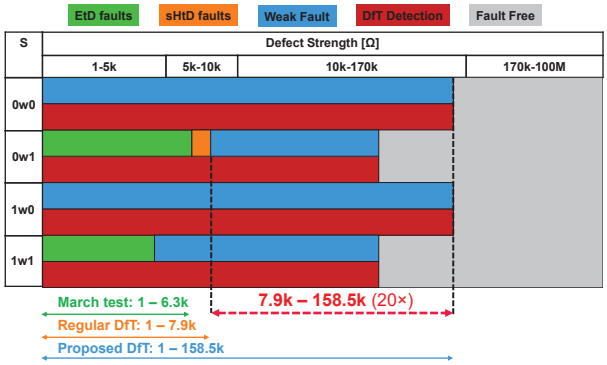


Fig. 13. Fault map and detection range for defect cBCC4.

indicate ranges of fault-free cases, and the red shapes indicate ranges detectable by the proposed DfT scheme. It can be concluded that both strong faults and weak faults are sensitized. For example, both $\langle 0w1/0/-\rangle$ (EtD) and $\langle 0w1/U/-\rangle$ (sHtD) are sensitized by $0w1$. The standard March test is effective in detecting the defect strength corresponding to sensitized EtD faults. However, it may fail to detect sHtD faults (e.g., $\langle 0w1/U/-\rangle$) since the 'U' state may result in unstable read output, particularly under the process variation. Furthermore, weak faults are sensitized by $0w1$ when the defect range is from $7.9\,k\Omega$ to $158.5\,k\Omega$. The proposed DfT provides incorrect values for this range, which indicates the detection of the defect ranges with corresponding weak faults. Note that the weak fault does not have functional errors but may damage the circuit's lifetime reliability. Similarly, $0w0$ and $1w0$ sensitize no strong faults, but the longest range of weak faults (improve the defect coverage from $7.9\,k\Omega$ to $158.5\,k\Omega$). For high test coverage, the longest range of detected faults must be selected; in this case, both $0w0$ and $1w0$ can ensure the maximum defect coverage. Besides, we notice that the write currents of $0w0$ and $1w0$ are correct since this defect supports the RESET operation. Hence, test methods that simply measure the write current will cause test escapes.

We further conduct process variation analysis for the DfT detection robustness. The MC analysis is performed with 1000 iterations for each write sequence within each defect range. Table III shows the overall results of the MC analysis for defect cBCC4. Here, the result for two defect ranges (the maximum and second-largest defect ranges detectable by the DfT, see Fig.13) are listed with the detection probability of the proposed DfT. There is better detection robustness under variations for $w1$ operations compared to $w0$ operations. It can be explained by: 1) the maximum covered defect strength

TABLE III
RESULTS OF THE MC ANALYSIS FOR DEFECT CBCC4.

S	0w0		0w1		1w0		1w1	
MC iteration	1000		1000		1000		1000	
Defect range [kΩ]	126	158	50	63	126	158	50	63
Functional correct	1000		1000		1000		1000	
Detection rate [%]	90.6	62.9	100	96.9	90.5	53.3	100	96.5

for $w0$ ($158\,k\Omega$) is much larger than it for $w1$ ($63\,k\Omega$); hence the large defect range is hard to detect under variations, 2) the amplitude of $w0$ current is much smaller than the amplitude of $w1$ current (around 10 times); hence it is more sensitive to the variation. Fig. 14 presents the detection probability at different defect ranges of cBCC4 for $0w0$ and $1w0$. Compared with the detection at $170\,k\Omega$ of the defect range without process variations, the DfT can guarantee the detection until $85\,k\Omega$ with process variations. As the defect range increases, the detection probability decreases with process variations. Due to process variations, there are test escapes at the defect range between $85\,k\Omega$ and $170\,k\Omega$ and yield loss at the range between $170\,k\Omega$ and $300\,k\Omega$. Note that no functional fault exists at these defect ranges, which indicates both the March test and existing DfT cannot detect all of them. Besides, it is observed that the process variation affects the sensitization of strong faults with a large defect range. For example, only 404 EtD faults and 90 sHtD faults (of 1000 MC iterations) are sensitized by $0w1$ when the defect range is $7.9\,k\Omega$ (strong faults are sensitized up to this range without variation). However, the defect range of $7.9\,k\Omega$ can be $100\,\%$ detected by the proposed DfT under variations. In summary, the result shows that the proposed DfT is decently resilient against process variations.

Then we present the combined verification result for all conventional defects. We observed that the proposed DfT is

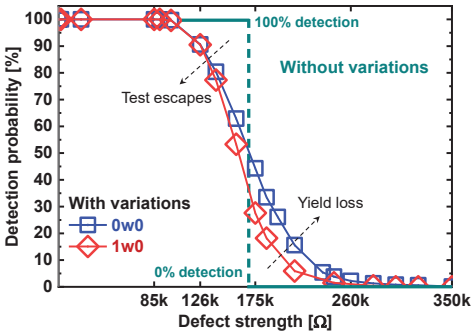


Fig. 14. Variation analysis for defect cBCC4.

TABLE IV
THE OUTPUT AND DETECTION OF PROPOSED DFT FOR UNIQUE DEFECTS.

Defect	Defect range	Unique fault	DfT outputs
OF	$r_{\text{det}} \in [70, 100]$, nm	$\langle 1\text{w}1/\text{H}/- \rangle$	1, 0, 1, 1
UF	$r_{\text{det}} \in [10, 30]$, nm	$\langle 0\text{w}0/\text{L}/- \rangle$	1, 0, 0, 0
IUSF	$N_{\text{max}} \in [1.5, 4.5], 10^{24}\,\text{m}^{-3}$	$\langle 0\text{w}1/\text{U}/- \rangle$	1, 0, 0, 0
ID	$N_{\text{min}} \in [1.5, 4.5], 10^{24}\,\text{m}^{-3}$	$\langle 1\text{w}0/\text{U}/- \rangle$	1, 0, 1, 1
OR	$N_{\text{min}} \in [1, 10], 10^{22}\,\text{m}^{-3}$	$\langle 1\text{w}0/\text{L}/- \rangle$	1, 0, 0, 0

able to sensitize a longer defect range (1323) than that by regular March tests (1083) and existing DfT schemes (1107); the proposed DfT improves the defect coverage with 22.16 % and 19.5 %, respectively. The increased defect coverage is due that the DfT can detect additional faults than existing works.

3) *Detecting Unique Defects*: The targeted unique defects can sensitize unique faults, as listed in Table IV. For example, the cell remains in the 'U' state after the RESET ($1w0$) in the presence of the ID defect [11]. Hence, the $\langle 1\text{w}0/\text{U}/- \rangle$ is sensitized at the defect strength of $N = 3 \cdot 10^{24}\,\text{m}^{-3}$. Note that these unique faults sensitized by unique defects in Table IV cannot be detected by the March test. Due to the real-time monitoring and detection of the writing current by the proposed DfT, the outputs ($X0, X1, X2, X3$) are '$1, 0, 1, 1$' with the injected OF, '$1, 0, 0, 0$' with the UF, '$1, 0, 0, 0$' with the IUSF, '$1, 0, 1, 1$' with the ID, and '$1, 0, 0, 0$' with the OR, respectively. The correct output values of $X0, X1$ ('$1, 0$') indicate that equal I_{BL} and I_{SL} flow through the cell since the unique defects are inside the RRAM cells. The incorrect output values of $X2, X3$ indicate that the write current is out of specification due to unique defects. For example, the 'U' state due to the IUSF results in a decreased SET current and thus incorrect output values of $X2, X3$. Note that unique defects such as IUSF, ID, and OR exhibit the *intermittent* behavior since they do not occur in every cycle. In this work, we assume the injected defect sensitizes faults in this cycle to verify the detectability of the proposed DfT in the worst case. However, the DfT can monitor the write current online and is guaranteed to detect intermittent faults as long as they are sensitized. Furthermore, the robustness of the DfT to detect unique defects is validated. For example, we perform 1000 MC iterations to the OF-defective circuit with the defect strength of $r_{\text{det}} = 80\,\text{nm}$. It shows that the OF defect can be 100% detected under process variations. In conclusion, the proposed DfT has a full defect coverage of targeted unique defects, avoiding test escapes from regular tests.

VII. Test Development

Next, we develop tests using the proposed DfT that detects as many defect sizes as possible while minimizing test time for conventional and unique defects. Note that multiple sequences can sensitize the same fault with a single defect size. In that case, only one of the sequences is needed to design the test with the same defect coverage. Based on this statement, we perform all static operations for the complete conventional defect space and obtain the following set of sensitizing sequences: $\text{S}_{conv} \in \{0w0, 0w1, 1w0, 0r0, 1r1\}$. These sequences can be combined in a March test as follows:

$$\text{March-Conv} = \{\Updownarrow (\text{w1}); \Updownarrow (\text{w0}, \text{w0}, \text{r0}, \text{w1}, \text{r1})\}.$$

Here, $\Updownarrow$ represents an irrelevant addressing direction, wy, $y \in \{0, 1\}$ represents the specific a write operation using the proposed DfT, and ry, $y \in \{0, 1\}$ represents a regular read operation using the SA. Similarly, the following set of sequences is obtained for the targeted unique defects: $\text{S}_{uniq} \in \{0w0, 0w1, 1w0, 1w1\}$. This results in the following:

$$\text{March-Uniq} = \{\Updownarrow (\text{w1}); \Updownarrow (\text{w0}, \text{w0}, \text{w1}, \text{w1})\}.$$

VIII. Discussion

Next, we compare the area overhead of the proposed DfT with other tests, analyze the design margin, elaborate on the tunability of current mirrors, highlight the application for diagnosis, and discuss its drawbacks and limitations.

A. Area overhead and optimization

The proposed DfT is based on the modification of write drivers. The area overhead of the DfT part is the applied current mirrors and reference generators (see Fig. 8). In our array design, each column shares the same BL driver while each row shares the same SL driver. Furthermore, the P1 and N1 (in Fig. 8) can be reused for the BL driver and SL driver of one cell. Therefore, the extra area cost is $10R + 7C$, where R denotes the number of rows in the memory, and C denotes the number of columns. The proposed DfT is also applicable to reuse the extra transistors for every cell since all memory cells have the same criteria. In this case, the total area overhead of DfT will be 17 transistors.

B. The margin of current difference ratio

In Section V, the proposed DfT sets a margin for the write current difference ($|I_{\text{BL}} - I_{\text{SL}}|$) of the defect-free cells. It is achieved by selecting a ratio (r) to copy either I_{BL} or I_{SL} to r times and thus guarantee a stable output of the DfT scheme when I_{BL} is closed to I_{SL} within a margin. Here, we define $r = 1.2$ (20 %). The ratio is selected under the consideration of process variation and RRAM stochasticity. First, we perform 5000 MC iterations at $r = 1.2$ and obtain 100 % correct outputs of the proposed DfT scheme. Then, we perform 5000 MC iterations at $r = 1.1$ and 5000 MC iterations at $r = 1.05$. The result shows 100 % correct outputs when $r = 1.1$ and 94.26 % correct outputs when $r = 1.05$, which indicates that the margin of 5 % is sensitive to variations. Besides, the V_{DD} and temperature may also have variations

and affect the performance of the DfT scheme, there is a trade-off between detection range and robustness.

C. Tunability of current mirrors

The proposed DfT replicates current to different multiples by using transistors with different sizes in parallel. For example, a wider and a thinner transistor can be selected in parallel to generate a higher reference current, or they can be individually selected, resulting in two different, lower currents. This allows the DfT to be tuned after manufacturing for maximal variation robustness, which increases the yield.

D. Application for Defect Diagnosis

The proposed DfT scheme can also be applied to diagnose RRAM defects. Conventional and unique defects have distinctive features and can sensitize unique faults [41]. The diagnosis of those defects requires test patterns with effective detection of all five states of the RRAM cell. Hence, the proposed DfT with tunability can be efficiently used for diagnosis patterns.

E. Drawbacks and Limitations

The proposed DfT also faces drawbacks and limitations that relate to its design and operating conditions. For example, the diode-like transistor used in current mirrors to copy the write current introduces voltage drops, which consume more energy and make it more difficult to switch the cell. Besides, each transistor of the current mirror needs to be specifically designed and is usually large to achieve accurate performance.

IX. Conclusion

This paper proposed a novel write current monitor DfT that guarantees full coverage of validated faults in the RRAM array. We design a specific write driver that performs write operations and measures the write currents simultaneously, allowing fast and efficient detection of faults not only during production testing but also in the field. Our proposed DfT implementations are validated with process variations and detect both conventional defects as well as unique defects (based on silicon data). Results demonstrate the superiority of our design compared to the state-of-the-art. Furthermore, the circuit can be reconfigured to optimize the yield process.

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