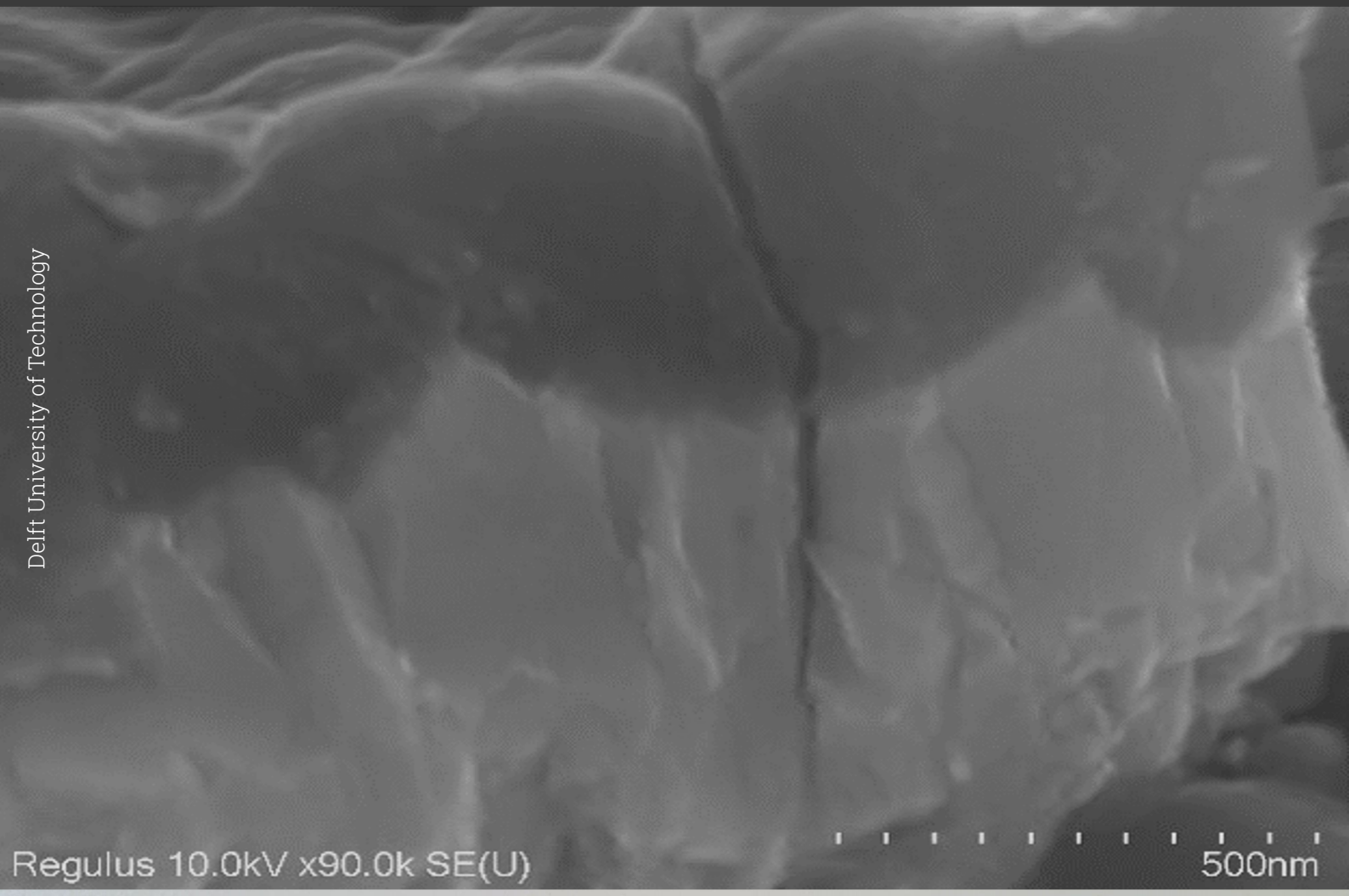
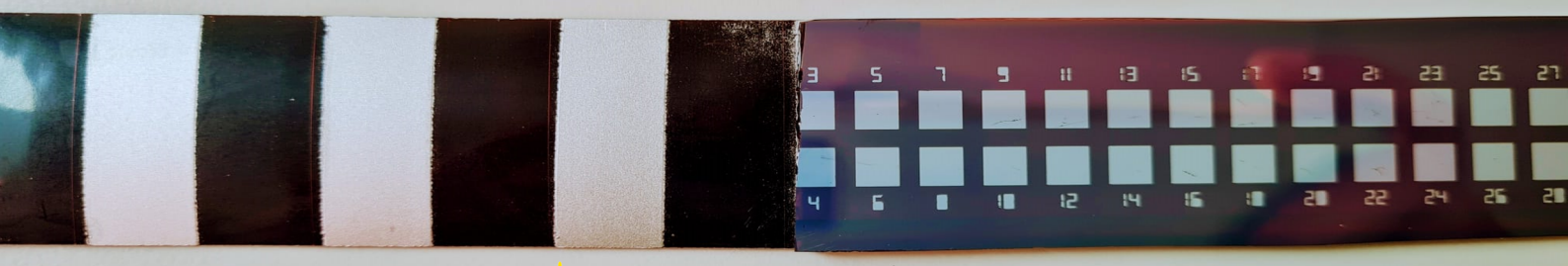
# Shunt Hunt in Thin Film Silicon Solar Cells

## Investigation, Mitigation and Optimization

Shloka Atul Dhavle



Delft University of Technology

TU Delft
PVMD Delft University of Technology
EKL Else Kooi Laboratory
HyET Solar Flexible light weight solar modules

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## Investigation, Mitigation and Optimization

by

Shloka Atul Dhavle

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*This thesis is confidential and cannot be made public until August 14, 2025.*



TU Delft

# Preface

*Dear Reader,*

*This report is written to present the research carried out at the Photovoltaic Materials and Devices group at TU Delft, and HyET Solar, as a part of my masters' thesis. For the purpose of this study, I performed an in-depth root cause analysis of the lowered performance and yield of lab-scale devices fabricated on the flexible aluminum substrate of HyET. At the same time, I optimized the performance of lab-scale single junction a-Si:H devices on glass by experimenting with different a-Si:H properties and tricks for improved charge carrier collection and spectral response. The completion of this report marks the end of my incredible Masters' journey at Delft University of Technology.*

*While writing the report I assumed the reader to have sufficient knowledge of thin-film solar cell technology and basic semiconductor physics. A basic introduction to the thin-film solar module production process at HyET and in the laboratory at TU Delft is provided to help understand the overview of this technology.*

*Readers that are particularly interested in device optimization on glass will find these in Chapter 4. Readers who are more interested in the root cause analysis of lowered performance of devices on aluminum substrate can go through Chapter 5. Lastly, to know more about the best performing device on glass put on foil, the readers can find it in Chapter 6.*

*Shloka Atul Dhavle*
*Delft, August 2023*

# Acknowledgements

*Working on this thesis project for the last 9 months has been an extremely epiphanic, rewarding and a humbling journey. There have been days where I loved to push myself beyond my comfort zone to learn, un-learn and re-learn, and be ambitious about my deliverables and there have been days when I was absolutely distraught by my performance and results. For both my highs and lows, I am happy that I showed up every day, and I thank Ganpati Bappa for providing me with the strength to do so.*

*This journey would not have been even half the delight if not for the people who have guided and cheered me on. My deepest gratitude to Prof. Arno Smets, for being an aura of energy and positivity. Since your first Renewable Energy lecture, I have been striving to be a better learner and researcher every day. I shall miss our catch-up meetings, your dropping by our offices to invite us for drinks, and all the lunch-table discussions about changing the world. Paula and Gianluca, for being such generous and motivating supervisors and for believing in me when I myself could not. Thank you for all your guidance and for making this thesis a little less daunting. Govind and Sreejith, for answering all my silly questions and not running away every time I entered your office with doubts. Stefaan, Tim, and Martijn, for being very proactive with fixing all lab equipment every time something went wrong.*

*To HyET Solar, where I have interacted with some amazing people and learned things I would not have in any other industry setting. Edward Hamers, you have been a tolerant and inspirational teacher, and I shall take your teachings with me throughout my career. Rahul, for so enthusiastically teaching me all about devices on foils, we shall forever be bonded by the shunt-hunt. Jimmy and Mohammed, for providing critical feedback on my work and results. Achinth, for helping with LP3 and patiently encouraging me to the finish line.*

*My thesis study-buddies have been a free therapy session throughout. Tristan, Shriram, Mehdi, Matthias, and Maria, I thank you from the bottom of my heart for all the discussions we have had daily, ranging from very serious knowledge transfer on photovoltaics to absolute trash nerd jokes. You guys gave me the willpower to be at work every day. I am beyond impressed by your determination not to miss out on a single opportunity to avail free coffee from my employee card. My family in Delft: Gaurav, Janki, Kishan, Ritik and Shanti, who have been my pillar of support the last two years away from home and had my back through my darkest days, making sure I came out stronger.*

*Most importantly, to my family who have given me the blessing to chase my ambitions and never believed I could not achieve my dreams. Mom, Dad, and Aditi; I strive to be your Woman of Mettle.*

# Abstract

Thin film silicon solar cells are a type of photovoltaic technology with the advantage of having thin layers of silicon to generate electricity. Unlike traditional crystalline silicon solar cells, which use thick silicon wafers, thin-film silicon solar cells use amorphous silicon that can be made with much thinner layers of silicon. This allows them to be more lightweight, flexible, and potentially less expensive to manufacture. However, their efficiency has traditionally been lower than crystalline silicon solar cells, which are more commonly used in large-scale installations. This is primarily due to the material property of amorphous silicon, which is laden with defects and voids. Nonetheless, ongoing research and development aim to improve the efficiency and commercial viability of thin-film silicon solar cells.

HyET Solar B.V. is a company based in the Netherlands which employs a Roll to Roll (R2R) technology to produce such flexible solar cells. A temporary aluminum foil is used as the substrate on which the solar cell stack is deposited. The temporary foil is etched away, and the layers are encapsulated in low-cost polymer foils. This thesis is part of the ongoing FlamingoPV (Flexible Lightweight Advanced Materials In Next Generation of PV) project in collaboration between HyET Solar and TU Delft, to develop single, tandem, and triple junction cells with 12, 13, and 14% efficiencies, and a lifetime longer than 35 years. Part of the ongoing research to improve the performance of thin-film silicon solar cells is to understand the difference between the thin films deposited on a rigid glass substrate and flexible aluminum substrate and to investigate why the performance is lower on the aluminum substrate. In particular, special emphasis is given to the origin of shunts in thin-film silicon solar cells, and conducting a top-down root cause analysis to investigate the origin of these shunts. Mitigation strategies are suggested to improve the solar cells fabricated on foil. Apart from this, the solar cell layers are optimized for improved electrical and optical performance on the glass substrate, to ultimately implement it on the aluminum substrate.

The key takeaways from this research are that aluminum foil was found to be a major culprit for the origin of the shunts. The foil consists of alloying elements of iron and copper, which get exposed to the surface when the foil is cleaned. When the subsequent layers are grown on the foil, the alloying elements were observed to short-circuit the device, thus causing leakage currents. Another major culprit was the formation and accumulation of silicon dust on the samples during the PECVD deposition, which was more prevalent on devices fabricated on aluminum foil. The key takeaways from the optimization experiments are that by the band-gap profiling of i-layer at a lower thickness (230nm) than the standard (300nm), we could maintain the initial electrical and optical properties of the devices. This gives us room to reduce material usage and costs at the same output performance. A permanent degradation was observed in the metal contacts of these devices, apart from the temporary light-induced degradation commonly seen in a-Si:H based solar cells. The tests conducted to improve the electrical performance did give the desired results, with an increase in the efficiency of the devices. The tests conducted to improve the optical performance did not give the desired results, with a decrease in the electrical performance and no significant increase in the optical response of the devices.

# Contents

# Nomenclature

## Abbreviations

| Abbreviation | Definition |
|---|---|
| a-Si:H | hydrogenated amorphous silicon |
| Al | aluminum |
| APCVD | atmospheric pressure chemical vapor deposition |
| AZO | aluminum-doped zinc oxide |
| c-Si | crystalline silicon |
| $CO_2$ | carbon dioxide |
| Cu | Copper |
| $CuSO_4$ | copper sulphate |
| EQE | external quantum efficiency |
| FF | fill factor |
| FTO | fluorine-doped tin oxide |
| i-ZnO | intrinsic zinc oxide |
| $J_{sc}$ | short circuit current density |
| LID | light-induced degradation |
| nc-Si | nanocrystalline silicon |
| PECVD | plasma enhanced chemical vapor deposition |
| R | reflectance |
| $R_p$ | shunt resistance |
| $R_s$ | series resistance |
| SEM | scanning electron microscopy |
| $S_{pc}$ | arithmetic mean peak curvature |
| SWE | Staebler-Wronski Effect |
| T | transmittance |
| TCO | transparent conductive oxide |
| TRJ | tunnel recombination junction |
| $V_{oc}$ | open circuit voltage |

## Symbols

| Symbol | Definition | Unit |
|---|---|---|
| $\alpha$ | Absorption coefficient | [$cm^-1$] |
| $E_g$ | Band-gap | [eV] |
| $\eta$ | Efficiency | [%] |
| $\lambda$ | Wavelength | [nm] |
| $n$ | Refractive index | [-] |

# 1

# Introduction

The term 'Energy Transition' has received a lot of traction in recent years. This stems from the need to shift from energy derived from conventional fossil fuels (coal, oil, and natural gas) to more *clean* energy sources (wind, solar, hydropower, geothermal, biomass, and tidal). The pressing need for this transition has been to reduce the detrimental environmental effects of burning fossil fuels to generate energy, which is a highly $CO_2$- intensive process. Of this energy, electricity is an important component in today's society. It is the easiest and cheapest to produce, transport, and use. Electricity demand has been on the rise and shall continue to rise as its contribution to transportation and heating increases [Figure 1.1]. Electricity generation through traditional coal-fired power plants is currently the largest source of global $CO_2$ emissions, estimated to reach an all-time high of 1.3GTon $CO_2$ emissions in 2022 [1].

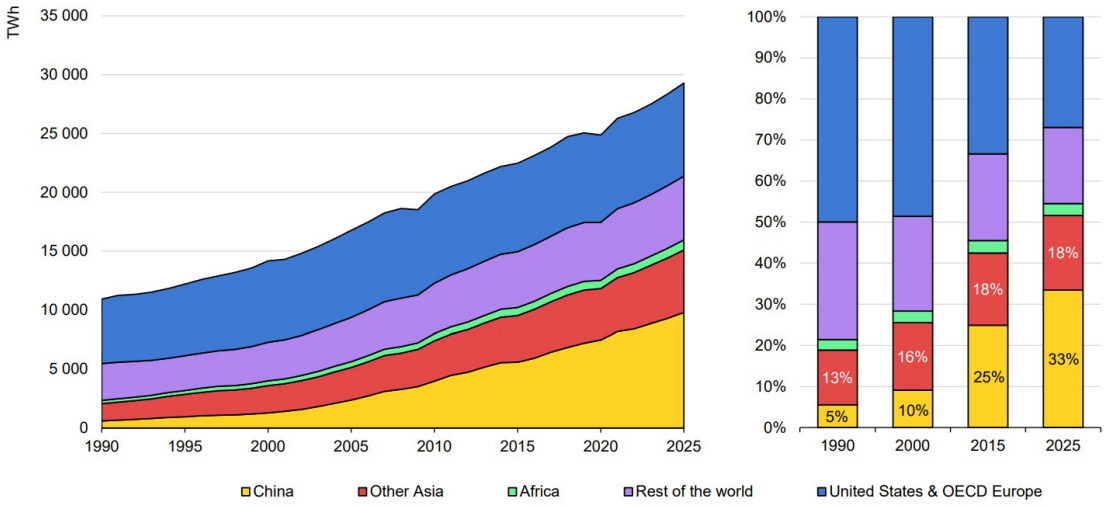



**Figure 1.1:** Evolution of global electricity demand by region (left) and by regional shares (right) [1]

Renewable energy sources have a massive potential to reduce dependency on carbon-intensive fossil fuels to meet our electricity demands. As seen in Figure 1.2, the share of renewables in the total electricity mix has risen from 2015 to 2021 and is expected to increase in the coming years. The share of renewable electricity in the Total Final Energy Consumption (TFEC) grew 3% in the last decade to reach 7% in the year 2020 [2].

## 1.1. Solar Energy

Harvesting energy from the Sun is not a new practice. Ancient Egyptians designed houses in such a way that the heat from the sun was stored during the day and released at night. Sunlight, when correctly

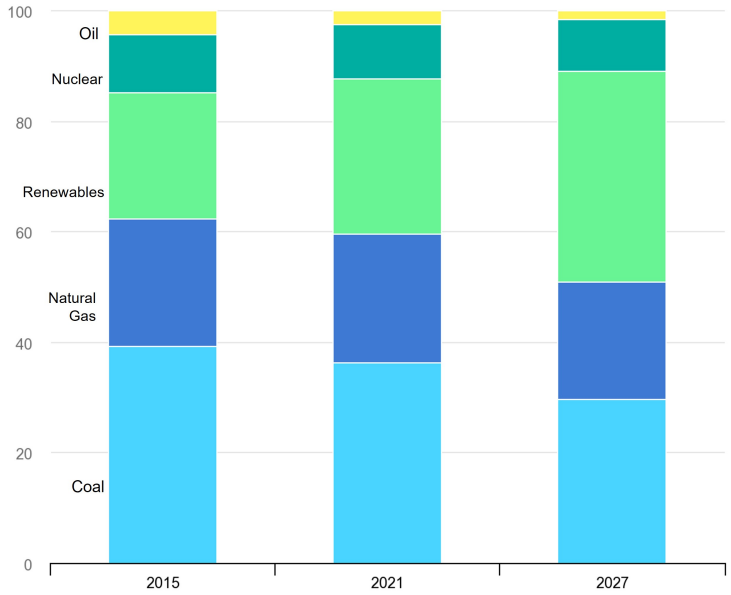



**Figure 1.2:** Global electricity generation by technology [3]

focused using a glass, was also used to start a fire. The use of solar energy to generate electricity was discovered only much later in 1893 when Edmond Macquerel discovered the *photovoltaic effect* (discussed in Section 2.2). Since then, efforts and experiments have been compiled to create working devices that can generate electricity from solar energy.
Solar PV generation has increased by 179 TWh in 2021, to exceed the total installed capacity to 1000TWh [4]. The annual production has increased by a factor of 9.7, from 2010 to 2021, with 93% coming from Asia alone in 2021 [5]. The cost of electricity generated from solar energy has dramatically reduced over the years [Figure 1.3], going from USD 0.417/kWh in 2010 to USD 0.048/kWh in 2021.

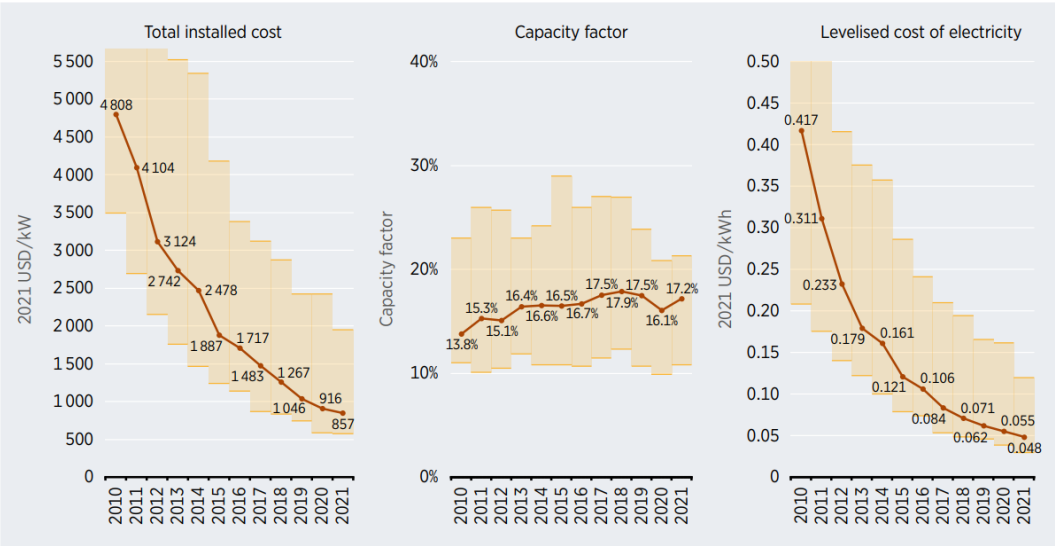



**Figure 1.3:** Global weighted average total installed costs, capacity factors, and LCOE for PV, 2010-2021 [6]

The main technologies in the market for Solar PV modules are as follows [7]:

1. First-generation solar cells: These include mono- and multi-crystalline silicon solar cells. Mono-crystalline silicon is a single crystalline solid with a continuous and unbroken crystal lattice and no grain boundary throughout. Multi-crystalline silicon has many small crystalline grains, arranged

in a random orientation. They currently occupy 90% of the solar PV market share [5]. Crystalline silicon (c-Si) is non-toxic, abundantly available, and has a stable efficiency. These properties make c-Si-based solar cells the most popular and most widely used. They are manufactured as wafers, from mono- and multi-crystalline silicon ingots. The c-Si solar cells are then designed using these wafers.

2. Second-generation solar cells: This category includes thin film solar cell devices made from the following:

   - Amorphous Silicon (a-Si)
   - Gallium Arsenide (GaAs)
   - Cadmium Tellurium (CdTe)
   - Copper Indium Gallium Selenide (CIGS)

   These films are created by the random nucleation reaction of individually condensing atoms/ions/-molecules on a substrate [8]. This opens up alternative deposition techniques for manufacturing, such as plasma deposition, evaporation, sputtering, etc. They are only a few nanometres to a micrometer thick, in contrast to c-Si solar cells which are around 200 micrometers [5], hence they are called *thin film devices*.

3. Third-generation solar cells: These solar cells have been fabricated with the intention to beat the thermodynamic limits of a solar cell [9]. The most common approaches to beat this limit are:

   - Spectral conversion in single junction solar cells using organic dyes, quantum dots, etc which can collect more than one electron-hole pair by altering the incident spectrum.
   - Multi-junction solar cells, that make use of multiple materials to facilitate more absorption of the incident solar spectrum.
   - Multi-exciton generation is a technique to generate more than one electron-hole pair from the incident solar spectrum.
   - Intermediate band-gap solar cells are used to create an artificial energy level in the solar cell, thus facilitating more electrons to be excited from the incoming photons.

   This approach aims to reach efficiencies beyond 30%, with the help of multiple energy threshold devices, although most of these approaches are still under the research phase.

Figure 1.4 represents the share of the above technologies in the market today.

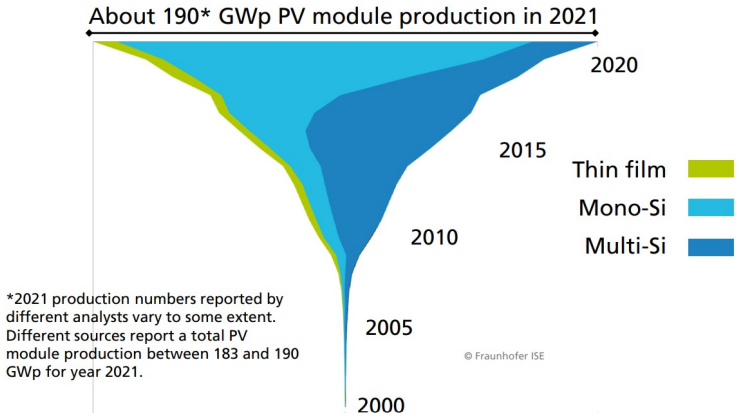



**Figure 1.4:** Annual PV production by technology [5]

## 1.2. HyET Solar: An overview

HyET Solar is a subsidiary of the HyET (High Yield Energy Technologies) Group, which manufactures flexible thin-film a-Si-based solar modules. Located in Arnhem, it was first known as Helianthos, a spin-off from Akzo Nobel, co-partnered with Shell from 2001 to 2006. In 2006, it was taken over by Nuon, Vattenfall. HyET Solar not only does research and development on thin-film solar cells on a

lab scale, but they also have a small production plant for roll-to-roll production of single-junction and multi-junction solar modules. This is done by using long aluminum foils as a temporary substrate for the modules. The final product has a thickness of <0.5mm and a surface density of 0.6 kg/m$^2$. Since it is flexible and lightweight, it can easily be integrated into a factory setup, thus avoiding the usage of additional support structures. This reduces the balance-of-system costs of such a module, bringing down its levelized cost of electricity (LCOE) such that it is 30% less than c-Si-based modules.
The Powerfoil is cost-effective, efficient, lightweight, easy to integrate, and sustainable [10]. The roll-to-roll production process at HyET is unique, due to the use of aluminum foil as the temporary substrate; giving the process homogeneity and the scope for scaling up. The processing is explained below:

1. Texturing of foil: The 350mm-wide aluminum foil is textured for better light trapping by creating crater-like structures through wet-chemical etching. Diluted NaOH is used for this purpose. After etching, the foil is cleaned in an acidic bath of $H_3PO_4$ to remove any precipitates.
2. Deposition of transparent conducting oxide (TCO): HyET uses fluorine-doped tin oxide (FTO) as the front TCO, as this is the most resistive compound to moisture and acid. This is deposited by atmospheric pressure chemical vapour deposition (APCVD) at 500$^o$C.
3. Deposition of silicon layers: The active layers are deposited in a single/multi pass route depending on the device architecture (single junction/tandem). This deposition is done via plasma-enhanced chemical vapour deposition at 200$^o$C using a RF frequency of 13.56MHz. The deposition machine has numerous zones, which deposits each layer one after the other on the roll.
4. Monolithic series connection: Laser scribing is used to define the active areas of the cell and isolate it from other cells, thus creating a series connection of multiple cells across the length of the foil.
5. Back contact deposition: Aluminum-doped zinc oxide and aluminum layers are sputtered after the scribing process.
6. Permanent carrier: The stack is then laminated on a permanent carrier foil, providing rigidity to the foil. The carrier is ideally a polymer substance that can bear the mechanical stresses of the foil.
7. Etching of Al substrate: The temporary aluminum substrate is etched away in a bath of NaOH, exposing the front TCO to light.
8. Encapsulation: To protect the foil from moisture, humidity, rain, wind, snow, etc, it is encapsulated from the front side. Finally, electrical connectors are added to complete the circuit.

## 1.3. Motivation

*Flexible, Lightweight, Advanced Materials in Next Generation of PhotoVoltaics* (FlamingoPV) is a joint initiative between TU Delft and HyET Solar to manufacture commercial solar modules with record efficiencies. The main objectives of this initiative are:

1. Lab-scale flexible a-Si:H/nc-Si:H devices (5 cm$^2$) and modules (5 $\times$ 5 cm$^2$) with 13% stabilized module efficiency
2. Roll to roll modules (30 $\times$ 30 cm$^2$) of 12% aperture area stabilized efficiency with 80% production yield.
3. Industry standard lifetime (>80 percent initial performance) convincingly proven for lifetime >35 years
4. Design and cost model for bottom cell PECVD tool with CAPEX < 0.2
5. Lab scale flexible a-Si:H/nc-Si:H/nc-Si:H PV Cell (5cm$^2$) and module (5 $\times$ 5 cm$^2$) with 14% stabilized module efficiency.

These objectives aim to deliver a state-of-the-art thin-film solar module, or *Powerfoil* that can compete with the existing c-Si-based solar modules.

**THE CHALLENGE**
Currently, the lab-scale devices on foil manufactured at HyET-TU Delft have not been meeting the target efficiency of 13%. Various reasons are being suspected for this drop in efficiency. This thesis is dedicated to investigating the cause of the low performance and low yield of devices on foil, by

performing a detailed root-cause analysis and developing a mitigation strategy to tackle the problem. A major focus is on the *low shunt resistance* of the lab devices, which appear to degrade the device performance greatly. At the same time, this thesis also explores ways to boost the performance of lab devices on foil, by using a novel, optimized device architecture on glass and translating it on the flexible foil. Through this, the aim is to reach the efficiencies specified in Objectve 1 of the FlamingoPV initiative.

## 1.4. Research Questions

The focus of this thesis is two-fold: to optimize the performance of single-junction a-Si devices on glass, and to demonstrate a proof-of-concept of a-Si/nc-Si tandem solar cells on Aluminium substrate. The following sub-questions are answered through this thesis:

1. Devices on Glass
    (a) **How is the device performance affected by the introduction of a-Si:H of different material properties?** This includes a series of experiments of tuning process parameters for bang-gap grading of a-Si:H.
    (b) **How much is the device performance degrading when exposed to light soaking?** This includes exposing the samples of 1a to light-soaking to see if band-gap grading influences the effect of light-induced degradation.
    (c) **Can the device performance be enhanced through improving the spectral utilization and collection of charge carriers?** This includes trial experiments to optimize the layers after the absorber layer.
2. Devices on Foil
    (a) **What are the possible casues of low shunt resistance in devices on foil?** This involves a deep root-cause analysis into the origin of low shunt resistances in devices on foil.
    (b) **Can the foils be processed with minimal mechanical manipulation?** This includes testing alternative methods for handling foils during the experiments at TU Delft and HyET Solar.
    (c) **Can the best-performing device-on-glass architecture of this thesis be duplicated on the foil?** This involves a comparison of the electrical performance of the novel, optimized device architecture on glass and foil.

The format of this thesis report is as follows: In Chapter 2, the fundamental principles of a solar cell are covered. In Chapter 3, the methodologies for device characterisation and fabrication are covered. Chapter 4 discusses studies for optimizing devices on glass, while Chapter 5 looks into the causes of low shunt resistances in devices on foil. In Chapter 6, the outcomes of the devices built on the aluminum substrate utilizing the best-performing device from the studies in Chapter 4 are examined. Chapter 7 wraps up the conclusions from all the experiments while also making recommendations for future study.

# 2

# The Solar Cell

This chapter discusses the physics behind the operation of a solar cell. First, silicon as a semiconductor is introduced in Section 2.1, followed by its working as a solar cell in Section 2.2. In Section 2.3, the thin-film silicon solar cell is studied which is followed by the device architecture in Section 2.4. Section 2.5 covers the parameters defining a solar cell, and Section 2.6 covers the common loss mechanisms in a solar cell. Most of the information in this chapter is taken from the book *Solar Energy* written by Smets et al [9]. It has not been cited everywhere in this chapter for brevity.

## 2.1. Silicon

Silicon belongs to group IV of the periodic table. It has four valence electrons, and forms covalent bonds with four other Si atoms. In a silicon crystal lattice, every atom is symmetrically bonded with the other four Si atoms, giving it a uniform tetrahedral look. This uniform structure is described as a structure with *long-range*. Amorphous silicon, on the other hand, has a lattice disorder. There is no periodic repetition, with deviations in bond angles and length making it lose its long-range order. This lack of order can break silicon bonds, resulting in nano-voids or *dangling bonds* (Figure 2.1).

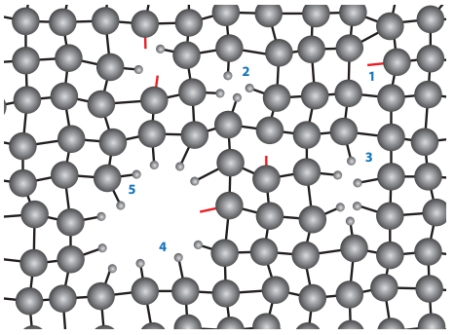



**Figure 2.1:** Atomic structure of amorphous silicon (1)mono-vacancies (2)di-vacancies (3)nano-sized voids (4)di-hydrides [9]

Pure a-Si has a very high defect concentration of $10^{19}$ $cm^{-3}$, which reduces its electrical properties drastically as compared to c-Si. To reduce the effect of dangling bonds, silicon prepared by glow discharge of silane ($SiH_4$) gas has better electrical properties due to the passivation of dangling bonds with hydrogen. From this point onwards, the abbreviation a-Si:H is used to indicate hydrogenated amorphous silicon. The random order of silicon atoms leads to a continuous distribution of energy states, consisting of tail states and defect states in between the extended band-gap states (Figure 2.2).

The mobility gap, or band gap of a-Si is 1.8 eV, which is higher than c-Si (1.1 eV). When translated to wavelength (Equation 2.1), a-Si:H corresponds to 750nm and c-Si corresponds to 1107nm. This means that a-Si:H can absorb all light upto 750nm, while c-Si can absorb all light upto 1107nm.

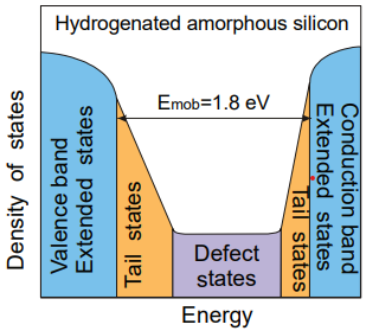



**Figure 2.2:** Band-gap states of amorphous silicon [9]

$$E_g = \frac{1240}{\lambda} \tag{2.1}$$

a-Si:H has a direct band gap, which means that the electrons require only the required energy to be excited from the valence to the conduction band. c-Si, on the other hand, is an indirect band-gap material, requiring both energy and momentum to be excited from the valence to the conduction band.

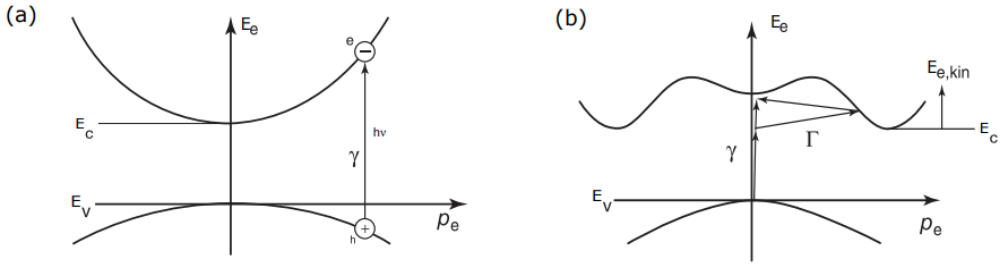



**Figure 2.3:** Comparison of the band-gaps of (a)a-Si and (b)c-Si [11]

a-Si:H thus has much higher absorptivity than c-Si. As observed from Figure 2.4, the absorption coefficient of a-Si is around two orders higher in the visible region (300-700nm), thus allowing a-Si:H films to be much thinner than c-Si in the same wavelength range. c-Si has better absorption of red and infrared wavelength light because of the lower band-gap value.
Hydrogenated silicon also exists in a *nanocrystalline* phase, which has a structure organization between the disordered a-Si:H and very organized c-Si. Their crystal size is around tens of nanometres big. The growth of nanocrystalline silicon (nc-Si) can be controlled by tuning the hydrogen flow rate during the plasma reaction of silane (Figure 2.5). Excess hydrogen in the plasma induces the transition to nc-Si. The band-gap of nc-Si is similar to that of c-Si (1.12 eV). It has better absorption than c-Si, as seen in Figure 2.4. These properties of nc-Si and a-Si:H make them ideal candidates to be used in combination to make thin-film solar cells, which will be discussed in the following sections.
To understand the effect of the nanostructural properties of a-Si:H on the band-gap, Smets et al [12] studied the relation between the a-Si:H nanostructure, tail states, and gap states created due to defects, on the band-gap of a-Si:H. Tail states refer to the localized electronic states present just adjacent to the conduction/valence band, arising due to the disorder in the lattice. Gap states, on the other hand, are states containing dangling bonds due to missing hydrogen atoms. The band-gap of a-Si:H can be increased by adding more hydrogen as a precursor gas in the matrix, which can decrease the mid-gap states. The volume deficiencies cause a volumetric compression of the silicon matrix, thus increasing the band-gap of a-Si:H. This makes high band-gap a-Si:H more porous than the low band-gap a-Si:H. Incorporating nano-sized voids can also increase the band-gap of a-Si, but this is countered by the formation of a highly porous a-Si with high metastable defect density. The trick here is then to modify the smallest open volume deficiency in such a way that nano-sized voids are not introduced in the matrix.

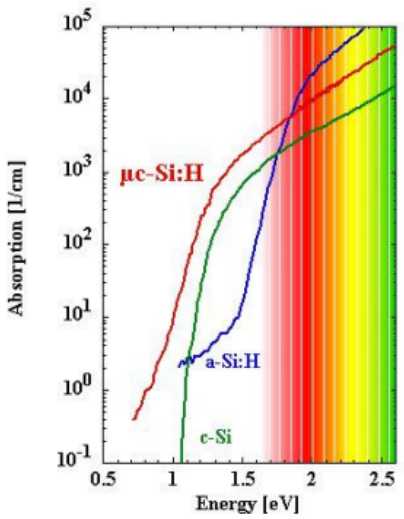



**Figure 2.4:** Relation between absorption spectra of silicon and wavelength of the incoming photon

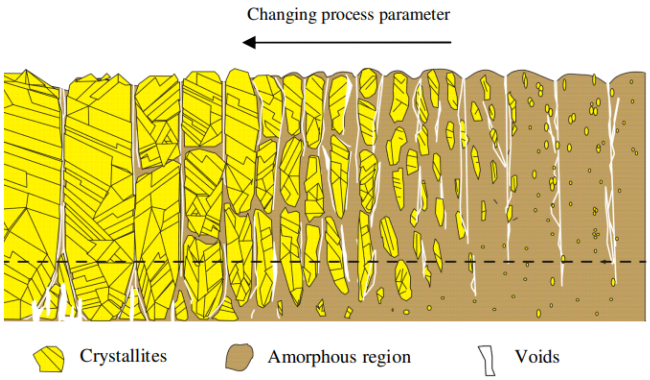



**Figure 2.5:** A cross-section view of the transition of crystal phase from amorphous to crystalline [9]

## 2.2. Working Principle

Solar cells are made from materials that are semiconductors in nature. These materials have conductivities between metals and non-metals. The principal mechanism behind electricity generation in these elements is the *Photovoltaic Effect*. This effect can be elaborated as follows:

1. Generation of electron-hole pair: A photon incident on a semiconductor can excite the *electrons* in it if the energy of the photon is equal to or greater than the energy required to excite the electrons. The electron in the valence band edge Ev, is excited to the energy level equal to the amount of energy it absorbs. It thus moves to the conduction band edge Ec. There does not exist any allowable energy state between Ec and Ev. So, the electrons need energy Ec - Ev, which is called the bandgap energy Eg, to be excited to the conduction band. This movement of an electron from the valence to the conduction band creates a void in the valence band, called the *hole*. This generation is depicted in Figure 2.6.
2. Separation of electron-hole pair: The electron-hole pair has the radiative energy of the photon stored as chemical energy. To make use of this energy, it is important to prevent recombination of the electron and hole. This can be facilitated by creating an external circuit for collection of the electrons at one membrane, and holes from the other.
3. Collection of photo-generated charge carriers: The charge carriers that are extracted from the solar cells convert their stored chemical energy to electrical energy in the external circuit. After this, they recombine.

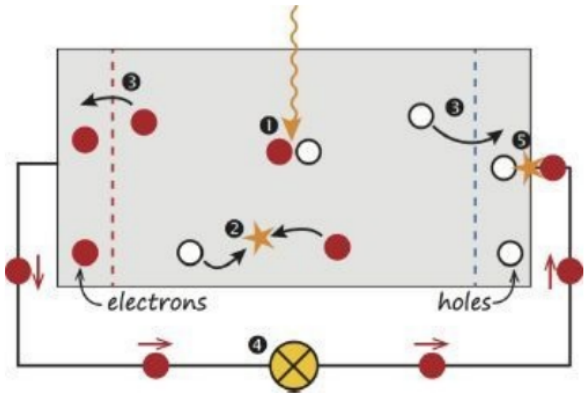



**Figure 2.6:** Schematic diagram of the working principle of a solar cell [9]

In its intrinsic, equilibrium state, silicon has the same number of electrons (n) and holes (p).

$$p = n = n_i \tag{2.2}$$

### 2.2.1. Doping of semiconductors

The concentration of electrons and holes in a semiconductor can be varied by adding other elements to replace Si in the crystal. Typical doping elements are Boron (3 valence electrons) and Phosphorus (5 valence electrons). When either is introduced to Si, the available electrons of the dopant bond with the 4 Si electrons. Adding boron results in an unbound Si electron, creating a hole, whereas adding phosphorus results in a free electron. Boron doping thus increases the hole concentration, making the crystal *acceptor* in nature (p-type), and phosphorus doping increases the electron concentration, making it *donor* in nature (n-type). For an n-type material, we can expect that the hole concentration is very low, which becomes lower with increasing the doping concentration. Assuming that n=$N_d$,

$$p = \frac{n_i^2}{n} = \frac{n_i^2}{N_d} \tag{2.3}$$

Similarly, for p-type material, assuming that p = $N_a$,

$$p = \frac{n_i^2}{p} = \frac{n_i^2}{N_a} \tag{2.4}$$

Inserting donor and acceptor ions into the lattice introduces allowable energy levels in the band gap, as shown in Figure 2.7. The red line represents the Fermi level, which is the average energy of electrons in a material.

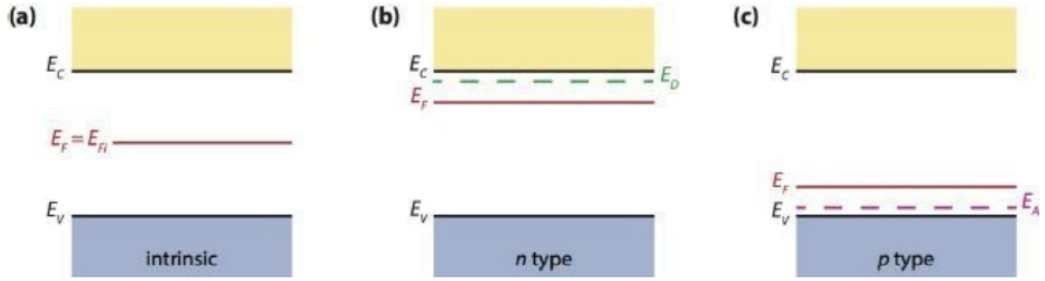



**Figure 2.7:** Effect of doping on the fermi-level of silicon [9]

On increasing the electron concentration (n-type), the Fermi level moves closer to the conduction band. In a p-type material, the Fermi level moves closer to the valence band.

### 2.2.2. Optics in solar cell interfaces

The thin film silicon devices in this thesis are essentially different layers stacked one upon the other, through which light passes. The rule of thumb is to design the device in such a way that all the light entering the device is absorbed by the i-a-Si, for maximum current generation. For this, it is important to understand the principles of optics involved. Any light wave incident on a surface is either reflected from it (R), transmitted through it (T) or absorbed in it (A), which is dependent on the properties of the two media through which the light travels. One such property is the refractive index *n*, which is the ratio of the speed of light in vacuum to the speed of light in that medium. The light incident on an interface at an angle $\theta_i$ is reflected at an angle $\theta_r$ and transmitted at an angle $\theta_t$. The angle of incidence is always equal to the angle of reflection,

$$\theta_i = \theta_r \tag{2.5}$$

whereas the angle of incidence and angle of transmittance bear a different relation via *Snell's law*.

$$n_1 sin\theta_i = n_2 sin\theta_t \tag{2.6}$$

For normal incidence, i.e. $\theta_i$=0, the amount of light reflected from surface 2 is given by Equation 2.7:

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \tag{2.7}$$

This relation is important while deciding which material is to be used in the device, depending on whether its purpose is to be completely transparent to all incoming light or to completely reflect all incident light. The layers in thin-film solar cells absorb the light incident on them, thus changing the dynamics of the reflectance properties. The electric field intensity (I) is known to attenuate exponentially when it travels through an absorptive media, which is given in Equation 2.8, known as the Lambert-Beer law.

$$I(z) = I_o(z) exp(-\alpha z) \tag{2.8}$$

where z is the distance the light travels through a layer, and $\alpha$ is the absorption coefficient of that layer.

## 2.3. The p-i-n junction

Unlike traditional c-Si cells which are designed using p-n junctions, thin film silicon-based solar cells are fabricated as p-i-n junctions. The high defect density in a-Si:H increases the rate of recombination in the layer, resulting in lower *diffusion length* of charge carriers, i.e. the charge carriers travel much lesser distance than they normally can before recombining. a-Si:H layers are thus much thinner (100-300nm) than c-Si. The intrinsic a-Si:H is sandwiched between two thin doped layers of a-Si;H, forming a p-i-n junction. In this junction, the band edges bend to form a uniform fermi-level as shown in Figure 2.8.

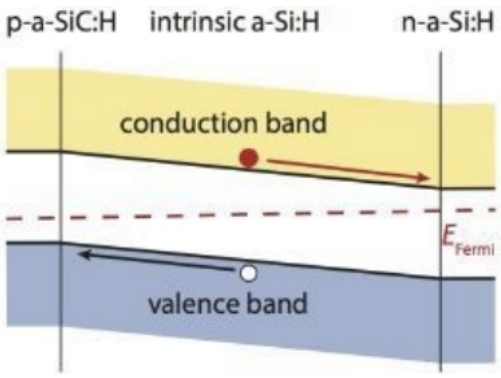



**Figure 2.8:** Schematic representation of the band diagram of a p-i-n junction [9]

This junction creates a slope across the electronic band. The doped p- and n- layers are not photo-active, but create an electric field across the intrinsic a-Si:H layer. Since diffusion length of the charge carriers in a-Si:H is small, the main transport mechanism is *drift* due to electric field generated by the p-

and n- layers. The electrons in the i-layer move towards the n-layer, whereas holes move toward the p-layer. These charge carriers are then collected in the external circuit. The i- layer has equal number of electrons and holes, that drift to their respective p- and n- layers. In the p- and n- layers, there is a concentration difference of the charge carriers, hence the transport mechanism in these layers is diffusion. Through diffusion, the charge carriers are collected at the other end of the p- and n- layers respectively.
nc-Si:H-based p-i-n junctions also work similarly to a-Si:H junctions. nc-Si:H can utilize the light of wavelength 700-1100nm, which is not utilized by a-Si:H. These i-layers are much thicker than a-Si:H i-layers (1800-2000nm) due to less defects in the crystal lattice. Using both these junctions in a solar cell can help us utilize the entire light spectrum from 300nm to 1200nm. Figure 2.9 represents the electronic band diagram of such a double junction, or *tandem* solar cell.

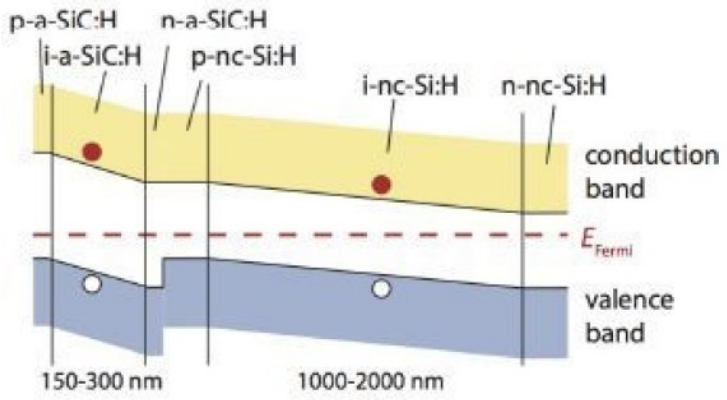



**Figure 2.9:** Schematic diagram of the band diagram of a thin-film tandem device [9]

The top sub-cell is a-Si:H, while the bottom sub-cell is nc-Si:H. This design is made so that the lower wavelength photons (300-700nm) are absorbed by the top cell and converted to electricity. The higher wavelength photons that are not absorbed by the top cell are transmitted and absorbed by the bottom cell. The holes generated in a-Si:H are collected at the top p-layer and the electrons generated in nc-Si:H are collected at the bottom n- layer. The electrons generated in a-Si:H, however, do not travel the entire bottom sub-cell to be collected at the bottom n-layer. Neither do the holes generated in nc-Si:H travel all the way to the top p-layer. These charge carriers, get recombined in the intermediate n- and p- layers, also called the *tunnel recombination junction* (TRJ). These n- and p- layers are deliberately made highly rich in defects to facilitate better recombination.

A major drawback of a-Si:H solar cells is that they degrade on prolonged exposure to high-intensity light. This phenomenon was first discovered by Staebler and Wronski in 1977 [13], who observed a drastic decrease in the photo-conductivity and dark conductivity of a-Si:H. This prolonged exposure is speculated to create excess dangling bonds in a-Si:H, which increased sites of recombination in the bulk of the solar cell. This phenomenon drastically reduced the efficiency by 10 percent of the initial efficiency. This effect is hypothesized to be a reversible effect, since the defects were *metastable* in nature. One way to recover this loss in efficiency is to anneal the samples at a high enough temperature for a specific amount of time, which is seen to recover the loss of efficiency and other electrical parameters of the solar cell [14].

## 2.4. Thin film device architecture

There are many layers built upon each other that form a complete solar cell device. These layers can be deposited in two configurations: *superstrate p-i-n* or *substrate n-i-p*, depending on the order of deposition. In superstrate configuration, the layer through which light passes first is deposited first, whereas in the substrate configuration, the layer through which light passes first is deposited in the end. In this thesis, all devices have been fabricated in the *superstrate configuration*. Based on the superstrate, two types of devices have been fabricated.

- Devices on glass have a **glass superstrate** (ASAHI VU glass and Corning glass).
- Devices on foil have **aluminium foil** as the superstrate.

The device looks as shown in Figure 2.10, with the deposition steps explained below:

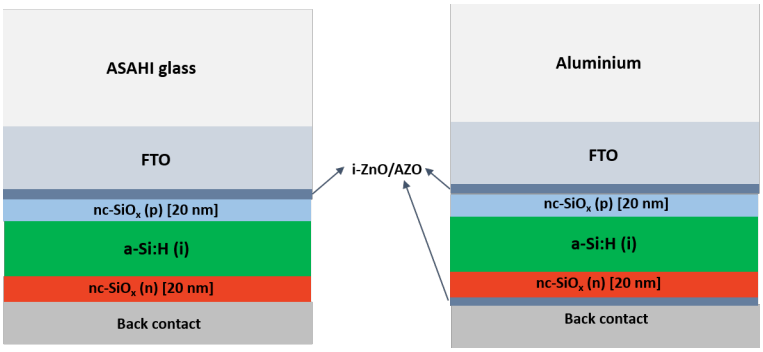



**Figure 2.10:** Device architecture

A *Transparent Conductive Oxide (TCO)* is deposited on this superstrate. This layer is responsible for the electrical front contact of the solar cell. It thus has to be highly conductive. Since it is also the first layer through which light passes, it has to be highly transparent. The bandgap of the TCO should be such that it allows the whole solar spectrum to transmit freely. This corresponds to around 3eV. [15]. The TCO should have good scattering properties of light to the absorber layer, which can be enhanced by *texturing* the superstrate. This gives the TCO layer crater-like or pyramidal structures, facilitating better light scattering. The TCO also should have favorable physicochemical properties for the growth of a-Si:H. Fluorine-doped Tin Oxide (FTO) works the best for the devices on foil since it is resistant to the etching solution used to remove the aluminum superstrate. This also gives a good comparison with devices on ASAHI glass as they come deposited with FTO from the supplier. Normally, the thickness of the TCO is around 750nm.
To protect the FTO from plasma processes of the absorber layers, a 20nm *buffer layer* of Aluminium-Zinc Oxide (AZO) or intrinsic Zinc Oxide (i-ZnO) is deposited on FTO.
After the buffer layer, the first p-i-n stack is deposited. The p-layer can be either boron-doped a-Si:H (p-a-Si:H) or oxides of silicon, doped with Boron (p-nc-$SiO_x$:H) using carbon dioxide ($CO_2$), silane ($SiH_4$) and hydrogen ($H_2$) as precursor gases. Silicon oxides are given a higher preference than p-a-Si since they have a higher band gap and reduced parasitic absorption in the blue part of the spectrum. Since their refractive index is tunable by varying the oxygen concentration, these silicon oxides can be used as anti-reflection layers to allow all the light into the absorber layer. Due to their filamentous growth, they have a higher top-to-bottom conductivity and a much lower in-plane conductivity [16]. The p-layer is around 20nm thick. Next, the i-a-Si:H absorber layer is deposited. The main gases used for this deposition are $SiH_4$ and $H_2$. The thickness of this layer is between 230 to 300nm. Next, the n-layer is deposited. The n-layer can be phosphorus-doped silicon oxide (n-nc-$SiO_x$:H) or phosphorus-doped a-Si (n-a-Si:H). Again, silicon oxides are preferred since the oxide is transparent and has a lower refractive index than a-Si:H, hence can also be used as a back reflector.
If tandem devices are to be made, the second p-i-n stack is deposited. The p- and n-layers can be the same as from the top cell, whereas the absorber layer is i-nc-Si:H, which is deposited using $SiH_4$ and $H_2$ as precursor gases.
Before depositing the metal back contact, a thin film of AZO (80nm) is deposited. This step is performed only for Devices on Foil from HyET, as AZO has proven to reduce diffusion of back contact aluminum into the n-layer which counter-dopes it to form a p-i-p architecture, causing leakage currents in the device [17] [18]. The last layer is the back contact to complete the electrical circuit. The back contacts used are either Silver-Chromium-Aluminium (300-20-500nm) or just Aluminium (500nm).

## 2.5. Solar cell parameters

There are various parameters that define the performance of a working solar cell. These are *short circuit current density*, *open circuit voltage*, *fill factor*, *power conversion efficiency* amd *external quantum efficiency*. Before understanding these parameters in detail, it is important to set a standard for

measuring these parameters. The *standard testing conditions (STC)* are 1000 W/m$^2$ solar irradiation impinging on the solar cell, at 25$^o$C. The impinging solar irradiation spectrum must also be the AM1.5 spectrum, which means that the radiation passes through the earth's atmosphere and is impinging on the solar cell at 37$^o$C.

### 2.5.1. Short circuit current density (J$_{sc}$)

This is the current per unit area flowing through the external circuit when the cell is short-circuited. This current $I_{sc}$ is dependent on the incident photon flux and the area of the solar cell.

### 2.5.2. Open circuit voltage (V$_{oc}$)

This is the voltage that develops across the solar cell when there is no current flowing through the external circuit. This is the maximum voltage that can be generated across the solar cell. This voltage is given as:

$$V_{oc} = \frac{k_b * T}{q} ln(\frac{J_{ph}}{J_0} + 1) \tag{2.9}$$

where k$_b$ is the Boltzmann constant, T is the temperature and q is charge, J$_{ph}$ is the photogenerated current density and J$_0$ is the saturation / dark current density. J$_0$ represents all the recombination mechanisms taking place in a semiconductor. It should thus be as small as possible. Since V$_{oc}$ is dependent on J$_0$, it indirectly hints at any recombinations taking place in the diode.
If the solar cell is assumed to behave ideally, the current-voltage relationship is defined by the Schottky equation:

$$J = J_0 * (exp(\frac{q * V}{k_b * T}) - 1) - J_{ph} \tag{2.10}$$

This corresponds to a J-V curve for every solar cell, which looks as follows:

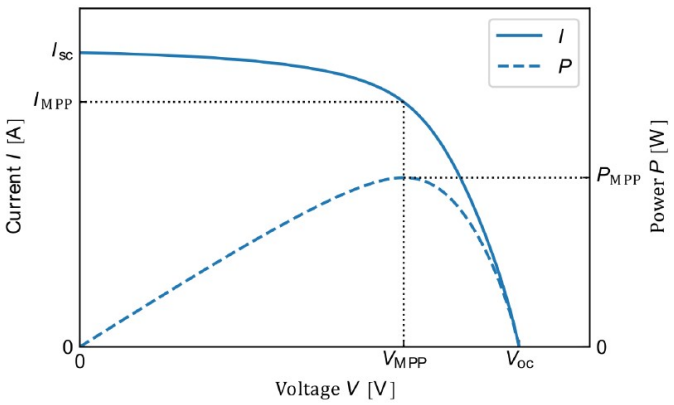



**Figure 2.11:** J-V curve and P-V curve of an ideal solar cell [9]

In real conditions, the solar cell does not operate at I$_{sc}$ and V$_{oc}$, but at I$_{mpp}$ and V$_{mpp}$, which is the *maximum power point* of the solar cell. At this point, the solar cell has the maximum power output.

### 2.5.3. Fill Factor (FF)

This parameter is the ratio between the *maximum power point* of the solar cell and the product of I$_{sc}$ and V$_{oc}$.

$$FF = \frac{I_{mpp} * V_{mpp}}{I_{sc} * V_{oc}} \tag{2.11}$$

### 2.5.4. Power Conversion Efficiency

The conversion efficiency determines what fraction of the incident solar radiation is converted into electricity.

$$\eta = \frac{P_{mpp}}{I_{in}} = \frac{I_{sc} * V_{oc} * FF}{I_{in}} \tag{2.12}$$

### 2.5.5. External Quantum Efficiency (EQE)

EQE is a measure of the ratio of successfully collected e-h pairs from the ones that are generated due to absorption of photons. The number of e-h pairs that are collected is dependent on the wavelength of the incident light.

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{e * \phi_{ph}(\lambda)} \tag{2.13}$$

where $I_{ph}(\lambda)$ is the wavelength-dependent photogenerated current, $\phi_{ph}(\lambda)$ is the wavelength-dependent photon flux coming from the sun and *e* is the charge of an electron ($1.6\times10^{-19}$). The EQE curve (EQE versus wavelength) gives insights into the optical and electrical losses in the cell. An ideal EQE curve for a tandem solar cell is shown in Figure 2.12. Any deviation from this curve helps us identify issues in device fabrication.

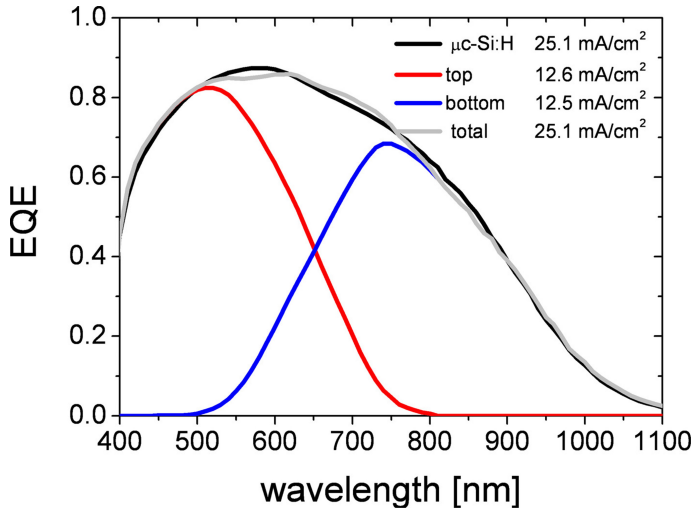



**Figure 2.12:** EQE of a tandem device [19]

## 2.6. Loss Mechanisms and limits

There are various mechanisms and limits that do not facilitate 100 percent conversion of incident solar energy to electricity. Solar cells can extract electricity from sunlight up to its theoretical efficiency limit. This limit is known as the *Shockley-Queisser limit*, discovered by Shockley and Queisser in 1960 [20]. They developed a detailed balance limit to calculate the highest theoretical efficiency of solar cells. An important assumption while calculating the efficiency is that the material undergoes only radiative recombination, i.e. the electrons recombine with the holes directly, without requiring a change in momentum. The various loss mechanisms are listed below:

### 2.6.1. Spectral mismatch losses

Also known as *thermalization loss*, this is the energy lost due to photons with energy greater than or less than $E_g$ of the absorber layer. The energy of the photon greater than $E_g$ is released as heat in the absorber layer, while the photons with energy less than $E_g$ do not generate charge carriers. The efficiency limited by this spectral mismatch is termed as *ultimate efficiency*. This efficiency ($\eta_{ult}$) is given by the formula:

$$\eta_{ult} = \frac{E_g * \int_0^{\lambda_g} \phi_{ph,\lambda} d\lambda}{\int_0^{\infty} \frac{hc}{\lambda} \phi_{ph,\lambda} d\lambda} \tag{2.14}$$

Where $\lambda_g$ is the wavelength of photons corresponding to $E_g$, $\phi_{ph,\lambda}$ is the photon flux at that wavelength, *h* is Planck's constant ($6.626\times10^{-34}$Js) and *c* is the speed of light in vacuum ($3\times10^{8}$ m/s).

### 2.6.2. Recombination Losses

These losses occur due to undesired recombination of electron-hole pairs, thus reducing the electrical performance of the device. **Shockley Read Hall Recombination** is based on the presence of trap

states in the band gap of a-Si [20]. Based on the charge of the trap state (positive/ negative), they can attract charge carriers to recombine. The energy released due to this recombination is lost as heat. **Auger Recombination** is a *three particle* process, wherein the energy and momentum of the recombining charge carrier is transferred to another electron/hole, which gets excited from its ground state. When the second excited carrier relaxes, it releases energy and heat in the lattice. **Surface Recombination** is more prominent at the surface, where there are many more dangling bonds present since valence electrons do not form covalent bonds.

### 2.6.3. Optical losses

Apart from defect-induced losses in the solar cell, there are some optical losses as well. *Reflection* of light from the top surface results in usable photons being lost. The metal electrodes on the top surface for collecting electrons decrease the active area of solar cells, called *shading loss*. Some part of the light that does enter the solar cell gets absorbed in the layers preceding the absorber layer, which does not generate charge carriers. This is known as *parasitic absorption*. The photons that have energy less than the $E_g$ of the absorber layer are transmitted to the back of the solar cell, known as *transmission loss*.

### 2.6.4. Fill Factor losses

Loss in fill factor is primarily due to the shunt and series resistances.

#### Series Resistance

For an ideal solar cell, we desire $R_s$ to be equal to 0. But there are numerous ways in which resistance can be developed in the bulk of the absorber layer, the contact resistance between the bulk layer and electrodes, and the resistance of the electrodes themselves. This increase in series resistance causes a dissipation of power in the device, thus reducing the voltage drop and fill factor of the solar cell.

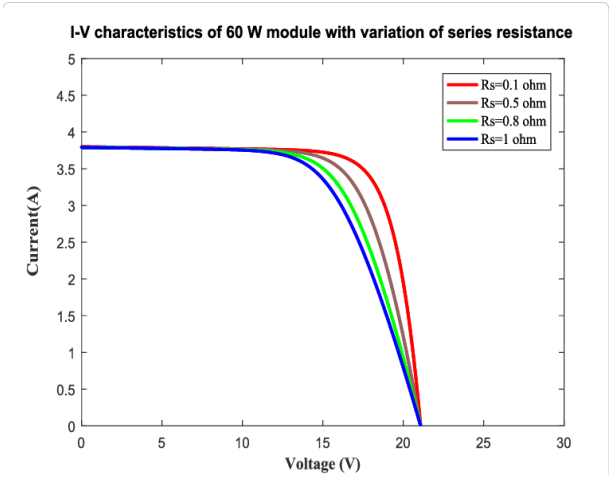



**Figure 2.13:** Effect of series resistance on solar cell parameters [21]

A key reason for high series resistance is the TCO used at the front and at the back. They have a *sheet resistance* ($\rho_s$) that can result in voltage drop across the solar cell. The dependence of FF depends on the sheet resistance of the TCO, through the following relation [22]:

$$\delta = \frac{\rho_s * L^2 * J_{sc}}{V_{oc}} \tag{2.15}$$

$\delta$ is a dimensionless parameter, that relates the fill factor to sheet resistance $\rho_s$ and the thickness of the TCO. The voltage drop across the TCO increases as the square of the thickness of the TCO, thus reducing the net generated current and thus power loss. These parameters are then used to relate $R_s$ to TCO properties as follows [22]:

$$R_s = \frac{\rho_s * L^2}{2} \tag{2.16}$$

### Shunt Resistance

An ideal solar cell should have an infinite *shunt resistance*. But due to defects in the fabrication or deposition, shunt or leakage paths can originate in the device. This results in a leakage current, reducing the collected current and thus the fill factor of the device. The origin of shunts has been broadly classified into two categories: *process-induced* and *material-induced* [23].

- Process-induced shunts [23]: These are shunts introduced during the fabrication of the device. *Linear edge shunts* are caused by bad edge isolation of the solar cells. They are detected using lock-in thermography, hinting towards being ohmic shunts. This leads to a leakage current through the edges. This is less prevalent now due to improved edge isolation techniques. *Non-linear edge shunts* on the other hand indicate recombination sites at the junctions. This results in a high ideality factor ($\tilde{3}$), indicating non-linear local shunts. Formation of *cracks and holes* during the deposition processes and *scratches* after the fabrication can cause severe ohmic and non-ohmic shunts. Contamination by *aluminum particles* in the intermediate layers, or at the surface, can result in a short circuit path, leading to leakage currents.
- Material-induced shunts [23]: *Strongly recombinative crystal defects* in the crystal lattice of Si can result in highly recombinative sites. Another possibility is the *inversion of p- and n- layers* caused by the presence of fixed positive charges at the corresponding grain boundaries.

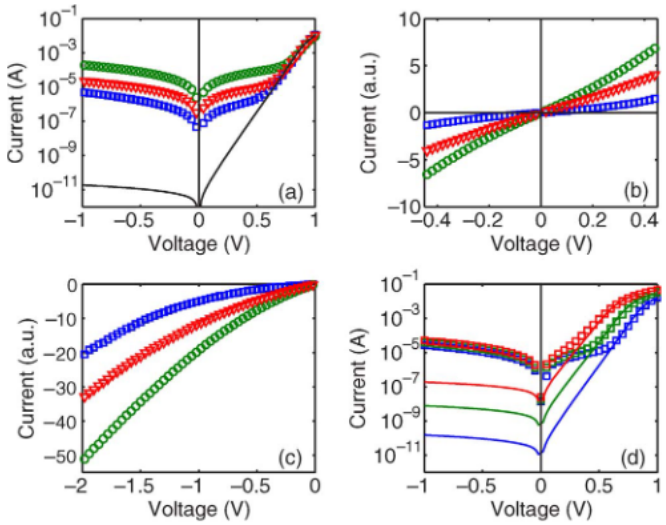



**Figure 2.14:** (a) Dark I-V curves of three identical cells (colored) versus a simulated I-V curve (solid black). (b) Symmetry around 0V. (c) non-linearity of leakage current. (d) Temperature dependence of I-V at 45$^o$C, 80$^o$C and 120$^o$C [24]

Dongaonkar et al [24] talk about the nature of shunt leakage current in large-area solar modules. They identify three phenomena from the dark I-V curve of p-i-n amorphous silicon samples.
As observed in figure 2.14, the first phenomenon is the deviation from ideality at V<0.5V. Much higher currents are observed in the voltage range between -1V and +0.5V. From (b), an unexpected symmetry is observed around 0V, which is not common for a rectifying p-i-n junction. This current in reverse bias is not linear, as can be seen in 2.14 (c). It can also be observed from (d) that at high forward bias, the dependence on temperature is exponential, whereas at low forward bias and reverse bias, there is no evident dependence on temperature. The effect of shunt resistance on the external parameters of the solar cell can be seen in Figure 2.15. The fill factor and efficiency drastically reduce.

## 2.7. The Equivalent Circuit

A solar cell that behaves ideally, can be modeled to be an electrical circuit based on the Schottky Equation.(2.10) The electric circuit can be visualized in Figure 2.16:
In reality however, the ideal diode behaviour of the solar cell is affected by the presence of a *series/ohmic resistance* $\mathbf{R}_s$ and a *parallel/shunt resistance* $\mathbf{R}_p$. These resistances represent losses in the solar cell, which result in a decrease in the FF and $\eta$ of the solar cell. By taking these resistances into account, the electrical model now looks as shown in Figure 2.17.

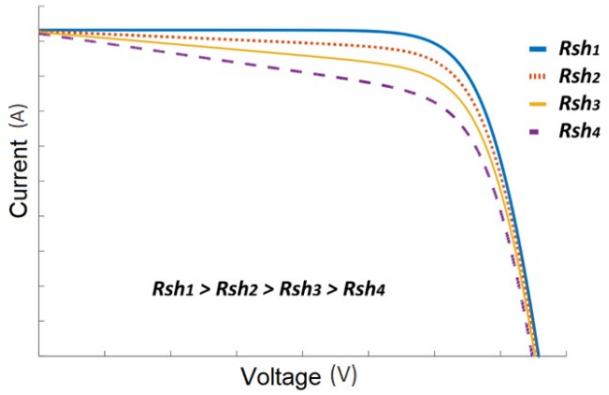



**Figure 2.15:** Effect of shunt resistance on solar cell parameters [25]

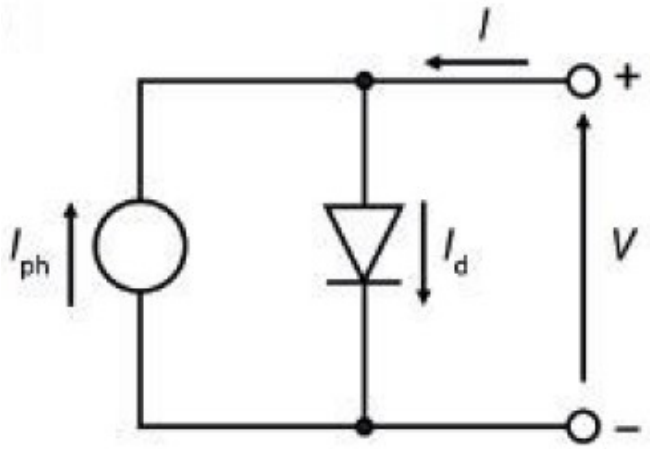



**Figure 2.16:** Electrical representation of an ideal diode [9]

The diode behaviour is now represented by the following equation:

$$J = J_0[exp\frac{q(V - AJR_s)}{k_bT} - 1] + \frac{V - AJR_s}{R_p} - J_{ph} \tag{2.17}$$

The dark J-V curve of an ideal solar cell (diode characteristics) and a non-ideal/shunted solar cell (resistor characteristics) is shown in Figure 2.18:
If the solar cell behaves like an ideal diode, it has a high shunt resistance (>10k$\Omega$.cm$^2$), and if the solar cell has any leakage current the shunt resistance value decreases (<1k$\Omega$.cm$^2$) thus behaving like a resistor.

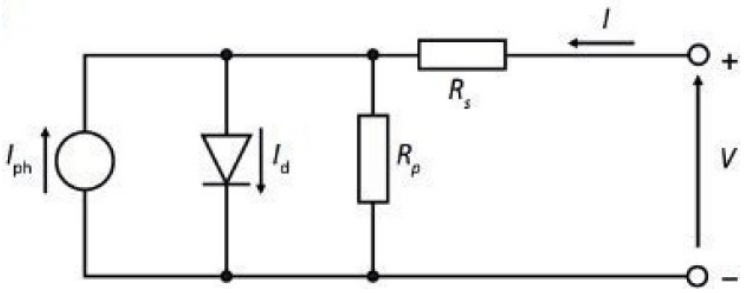



**Figure 2.17:** Electrical representation of a non-ideal diode [9]

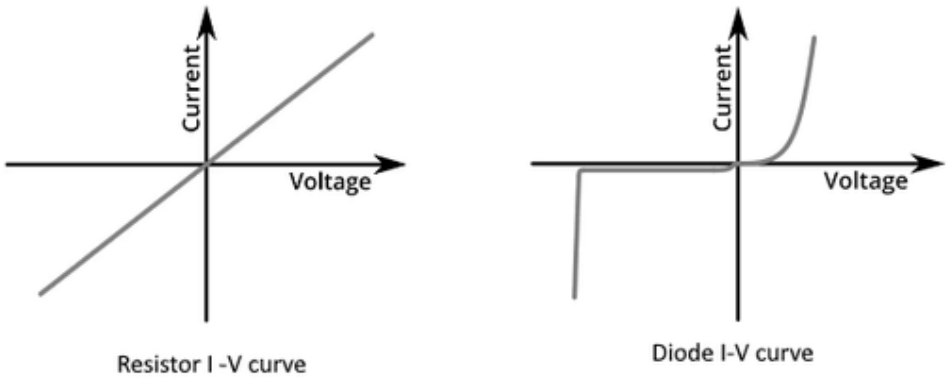



**Figure 2.18:** Dark J-V curve of a shunted solar cell (resistor curve) and an ideal diode

# 3

# Device Fabrication and Material Characterization

This chapter discusses the deposition techniques of thin film solar cells in Section 3.1, the fabrication steps on both on glass and aluminium superstrates in Section 3.2 and the various techniques to characterize these devices in Section 3.3.

## 3.1. Deposition Techniques

The different layers of a thin-film solar cell are deposited using different techniques, that are best suited for ideal growth of the film on the substrate.

### 3.1.1. Atmospheric Pressure Chemical Vapour Deposition (APCVD)

It is a synthesis method where the substrate is exposed to one or more volatile precursors at atmospheric pressure, which decompose on the surface to generate a film. In the CVD process, the desired elements of the film are introduced using appropriate precursor mixture during deposition [26]. For preparing FTO films tin tetra chloride (TTC), water, methanol and hydrogen fluoride (HF) are used as pre-cursor gases. Typical temperatures employed for this deposition are 500$^{o}$C. The key steps involved in this technique are shown in Figure (3.1):

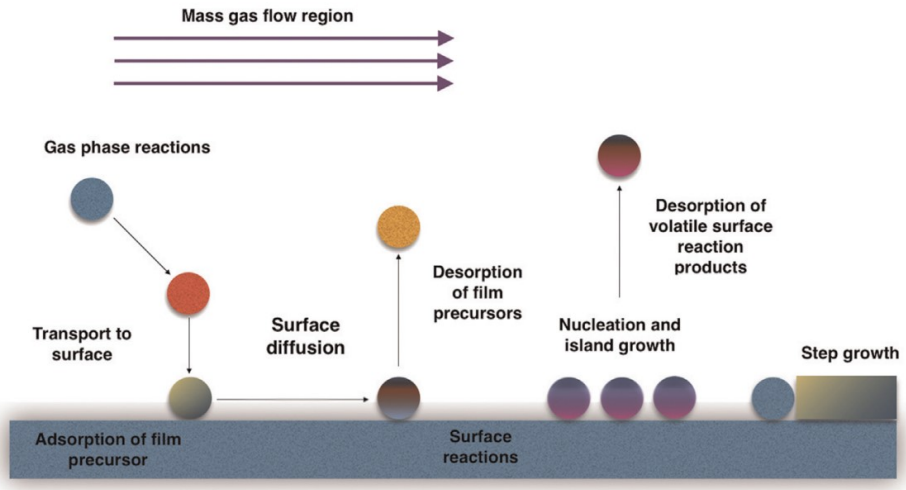



**Figure 3.1:** APCVD reaction processes [27]

### 3.1.2. Plasma-Enhanced Chemical Vapour Deposition (PECVD)

The thin-film silicon layers are deposited by this method. In this process, a bias voltage at radio-frequency or very-high frequency is applied to two electrodes. This generates a plasma, which dissociates the precursor gases in the chamber to deposit silicon films on the substrate. The precursor gases used are silane ($SiH_4$) and hydrogen for a-Si and nc-Si deposition. Diborane ($B_2H_6$) is used for p-doping and Phosphine ($PH_3$) is used for n-doping. Carbon Dioxide ($CO_2$) is used for making SiOx films. PECVD enables deposition at temperatures as low as 180$^o$C, giving uniform and high-quality films. Through ionization, dissociation and dissociative attachment reactions, the precuresor gas radicals/ions are diffused towards the electrodes, growing to form the layers.

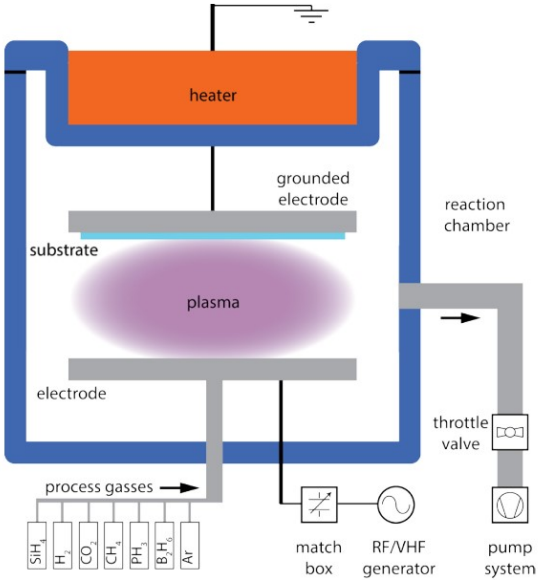



**Figure 3.2:** Schematic diagram of a PECVD process [9]

The PECVD tool at the Else Kooi Laboratory (EKL) at TU Delft is a multi-chamber tool manufactured by Elletorava, called AMIGO. There is minimal cross-contamination since different layers are processed in different chambers. The reaction chambers have two parallel electrodes, separated at a distance of 13mm.

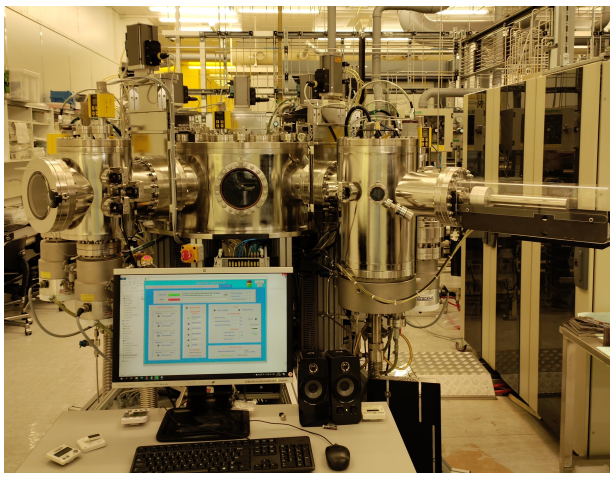


**Figure 3.3:** PECVD tool at EKL, TU Delft

The quality and properties of the layers can be controlled by varying the process parameters like temperature and pressure in the reaction chamber, gas compositions and flow rates, and plasma power.

### 3.1.3. Sputtering

Sputtering is a Physical Vapour Deposition (PVD) method used to deposit metal contacts like Aluminium, Silver, etc, or TCOs like AZO/ZnO/ITO. In this method, energy and momentum from the accelerated Argon ions are transferred to the surface of the target (cathode) to eject target atoms. These atoms then condense on the substrate (anode) to form a thin film of the target. Based on the material to be deposited, different sputtering techniques can be used: DC sputtering for aluminium, which uses a constant DC power and RF sputtering for AZO, which uses an oscillating power to generate the plasma.

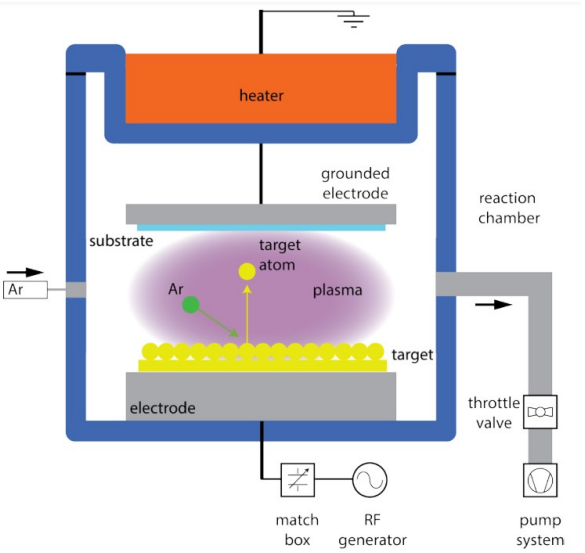



**Figure 3.4:** Schematic diagram of a sputtering process [9]

### 3.1.4. Evaporation

Evaporation is also a PVD technique used for depositing metal contacts of Aluminium, Chromium, Tin, Silver, etc. There are two main types of evaporation processes: resistive and electron beam. In the resistive evaporation process, the metal target is loaded in an open crucible, which is heated resistively by applying a high current. In an electron beam evaporation, the metallic target is placed in a water-cooled crucible and is irradiated by an intense electron beam that heats the source. The evaporation tool PROVAC500S at EKL employs both evapration techniques. The evaporation is performed under high vacuum conditions ($10^{-3}$ Pa to $10^{-6}$ Pa).

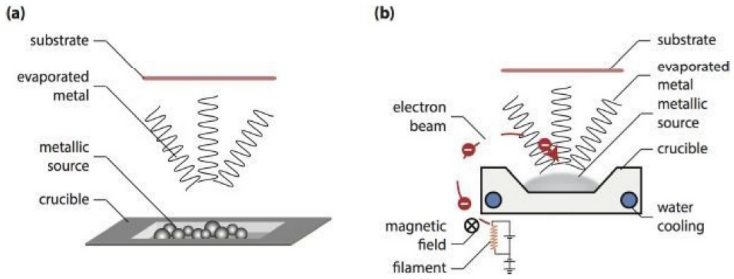



**Figure 3.5:** Schematic diagram for (a) Resistive evaporation (b) Electron beam evaporation [9]

## 3.2. Lab-Scale device fabrication

While the device fabrication processes on glass and foil have some steps in common, they are fabricated in very different ways. Hence they shall be discussed separately.

### 3.2.1. Devices on glass

The front TCO (FTO) on ASAHI glass (10 $\times$ 2.5 cm$^2$) already comes deposited and textured by the supplier. The following steps enlist the deposition process of devices on glass.

1. Before depositing any further layers, the glass samples need to be cleaned. This is done by dipping it in acetone ultrasonic bath for 5 minutes and iso-propyl alcohol (IPA) ultrasonic bath for 5 minutes.
2. The front contact is a 500nm strip of aluminium, which is deposited by evaporation at 180$^o$C in PROVAC using the appropriate mask.
3. A thin, 20nm buffer AZO/i-ZnO layer is sputtered in AMIGO, at 300$^o$C.
4. The p-i-n layers are deposited in dedicated chambers of the PECVD tool, in superstrate configuration. The deposition parameters are discussed in Chapter 4, depending on the exact layer properties desired.
5. The back contact, of 200nm Silver- 30nm Chromium- 300nm Aluminium is evaporated in PROVAC, using a mask of 30 square cells of 4$\times$4 mm$^2$.
6. Before performing any characterization, the samples are annealed at 180$^o$C for 30 minutes, to ensure good contact between all the layers and to reverse the effect of light-induced degradation.

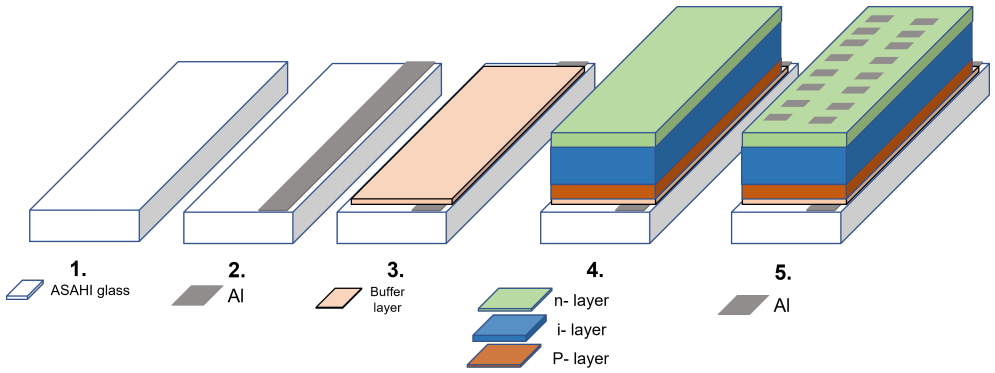



**Figure 3.6:** Schematic representation of deposition steps on ASAHI glass

### 3.2.2. Devices on Foil

Devices on foil are made by mimicking the roll-to-roll production process of solar modules at HyET Solar. Aluminium foil is used as a temporary superstrate, on which all layers are deposited. The step-by-step procedure for making lab-scale cells on foil is listed below:

1. The incoming foil from the supplier is textured by wet etching using diluted NaOH and cleaned in an acidic $H_3PO_4$ bath to remove any residues.
2. The front TCO (FTO) is deposited by APCVD, at 500$^o$C. The FTO layer is approximately 750nm thick.
3. 20nm buffer AZO layer is deposited by sputtering, to protect the FTO from hydrogen plasma during deposition of silicon layers.
4. The foil is then punched using a mechanical press, to cut it into 10$\times$10 cm$^2$ area.
5. The sample is then brought to EKL, where the silicon (p-i-n) layers are deposited in AMIGO in superstrate configuration. The deposition parameters are discussed in Chapter 4, depending on the exact layer properties desired.

After the silicon layers are deposited, the copper sulphate tests can be performed to analyze the layer properties. The post processing of the solar cells can be done in two ways: fabrication of Diodes on Foil and fabrication of superCells on Foil.

### Diodes on Foil

This processing route is to get quick feedback of the properties of the solar cell fabricated, especially the diode performance in the dark.

6. After the silicon layers are deposited, the cells can be completed either by sputtering AZO (80nm) and Al(300nm), or by evaporating Ag(200nm) + Cr(30nm) + Al(300nm). This is done by using masks that define an area of $4 \times 4$ mm$^2$.

The final device structure is shown in Figure 3.7.

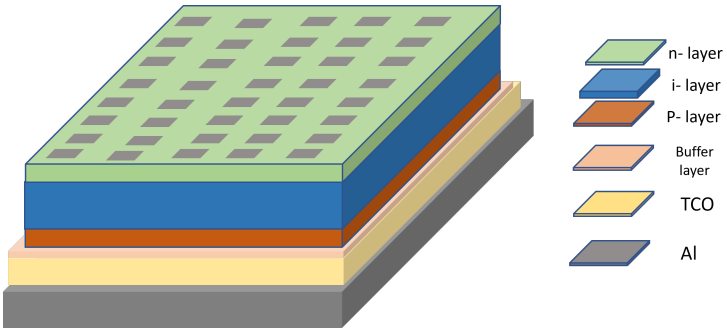



**Figure 3.7:** Device Architecture for Diode on Foil

### Super Cells on Foil (superCOF)

This processing route is developed to fabricate lab-scale solar cells, to study the optical and electical properties of the deposited device.

6. The back contacts AZO (80nm) and Al(200nm) are sputtered using masks that define the cell's active area. The masks are designed in a way that contacts can be created.

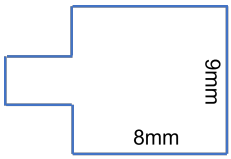



**Figure 3.8:** Back contact design for Super COF [28]

7. Copper tapes are connected to the back contact in such a way that they do not contact the aluminum on the edges. This is done by placing a plastic interleaf under the tape.
8. The sample is then encapsulated using a polyethylene nitrile (PEN) carrier. This is done in a vacuum press with a force of 18kN at 120$^o$C. Care is taken that no air bubbles are introduced in the encapsulant.
9. Etching is performed to remove the temporary aluminum superstrate. This is done using 1.2M NaOH bath at 70$^o$C, to remove around 80 micrometers of the superstrate.
10. Since etching can induce some mechanical stresses in the sample, it is annealed at 180$^o$C for 20 minutes. This prevents the FTO from cracking and the sample from bending.
11. A final etch is performed to remove the remaining temporary superstrate. To define the busbars, an etch-resistant tape is used.

The final device structure is shown in Figure 3.9.

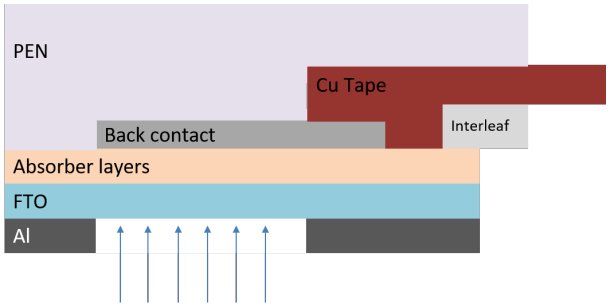



**Figure 3.9:** Schematic diagram of a superCOF structure [28]

## 3.3. Characterization Techniques

The fabricated devices have been characterized using various techniques, which shall be explained in this section.

### 3.3.1. Current-Voltage measurement

The current-voltage (J-V) curve of every sample is measured both in dark and illuminated conditions using a AAA class WACOM solar simulator. This measurement gives us important parameters of the cell like $V_{oc}$, $J_{sc}$, FF, Efficiency, $R_s$ and $R_p$. Another important parameter that can be extracted from the J-V curve is the third order of the parallel resistance, or $R_{ppp}$. This non-ohmic shunt resistance helps better understand the diode properties and can be extracted by simply fitting the J-V curve in the adapted non-ideal diode equation (3.1) [28].

$$J = J_0 exp\left[\frac{eV}{nk_bT} - 1\right] + \frac{V}{R_p} + \frac{V^3}{R_{ppp}} \tag{3.1}$$

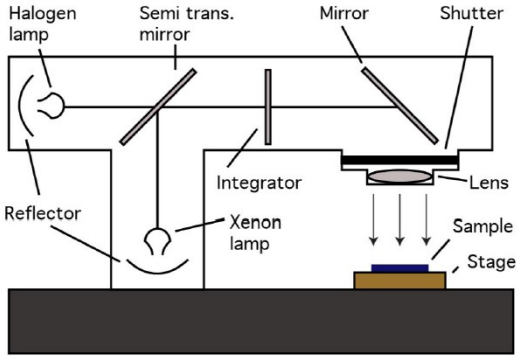



**Figure 3.10:** Schematic diagram of J-V measurement setup [29]

A schematic diagram of the J-V measurement setup is shown in Figure (3.10). For these measurements, the standard testing conditions are simulated by using the entire spectral range of a halogen and a xenon lamp.

### 3.3.2. External Quantum Efficiency (EQE)

The EQE setup as shown in Figure (3.11) is used to measure the EQE of the samples from 300nm to 1200nm, and subsequently the $J_{sc}$ of the device. The light from the lamp is chopped using an optical chopper, after which a single wavelength light is impinged on the solar cell with the help of a monochromator. The resulting current is measured, which gives the EQE and the $J_{sc}$ of the device. While measuring single junction devices, no bias light is used, whereas for measuring tandem devices, red and infrared bias light is used while measuring EQE of the top cell and blue and green bias lights are used while measuring the EQE of the bottom cell. The bias light is used to completely saturate the

sub-cell which is not being measured, to give an accurate spectral response of the measured sub-cell [30].

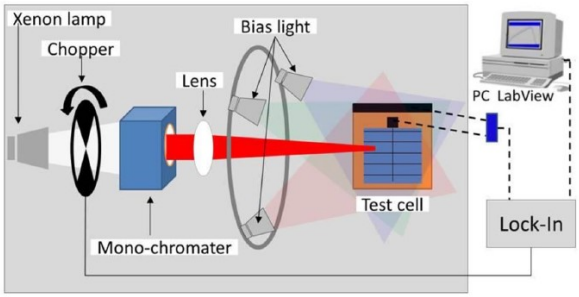



**Figure 3.11:** Schematic diagram of EQE measurement setup [29]

### 3.3.3. Reflectance and Transmittance (RT)

Transmittance and reflectance measurements can provide insights into the optical performance of the device. Through this data, one can determine where, if any optical losses, occur. These measurements are performed using the PerkinElmer Lambda 1050 UV/VIS Spectrophotometer. For doing reflectance measurements, the monochromatic light is focused on an integrating sphere consisting of InGaAs and PbS detectors. The sphere is made of spectralon, a highly reflective and scattering material. Calibration is performed to result 100% reflectance at each wavelength, after which the sample's reflectance values are measured. The sum of absorptance (A), reflectance (R) and transmittance (T) is 1. Assuming that no light is transmitted through the device due to metallic back contacts, **1-R**, or **A** values are calculated to check which part of the spectrum is absorbed in which layer of the device architecture.

### 3.3.4. Scanning Electron Microscopy (SEM)

SEM can provide important information on the surface topography, crystalline structure, chemical composition and electrical behaviour of a specimen. The SEM Hitachi Regulus 8230 uses a focused beam of electrons which is accelerated towards the sample surface. This then scans the surface, achieving large depth of fields and very high magnifications (nanometer level resolution) [31]. In this thesis, SEM images are used to observe possible shunt paths in the cells on foil.

### 3.3.5. Focused Ion Beam Scanning Electron Microscopy (FIB-SEM)

This is a technique similar to the SEM, but instead of using focused beam of electrons, a focused beam of ions is used. Gallium ions are most commonly used, which are accelerated to an energy of 1-50 keV and focused onto the sample using electrostatic lenses. The schematic diagram is shown in Figure 3.12

### 3.3.6. Confocal Microscopy

This analysis tool is used for sketching surface profiles. A point source of light is generated by the microscope, which penetrates deep into the surface, providing high-resolution images. The illumination and detection optics are focused on the same diffraction-limited spot, which is moved over the sample to build the complete image on the detector.

The surface roughness parameters of the aluminium foil is measured by this technique, to develop a correlation betewen foil quality and solar cell parameters. The following surface roughness parameters are used through confocal microscopy (z(x) is the sampling height in z direction) [33]:

1. Maximum profile peak height ($S_p$): This is the point along the sampling length at which the curve is the highest.
2. Maximum profile valley depth ($S_v$): This is the point along the sampling length at which the profile curve is the lowest.

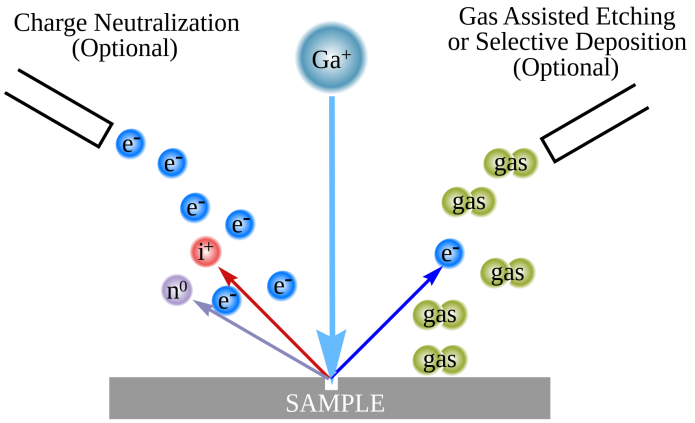



**Figure 3.12:** Schematic diagram of a FIB-SEM setup

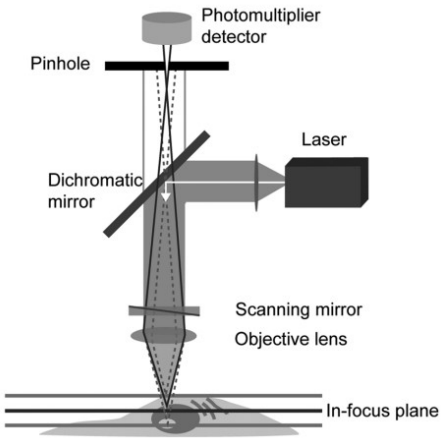



**Figure 3.13:** Schematic diagram of a confocal microscope [32]

3. Arithmetic mean peak curvature ($S_{pc}$): Represents the average curvature of the peaks in a given surface area. It essentially quantifies if the peak is rounded or sharp, as shown in Figure 3.14 (a).

$$S_{pc} = \frac{1}{2n} \sum_{k=1}^{n} \left( \frac{\partial^2 z(x,y)}{\partial x^2} + \frac{\partial^2 z(x,y)}{\partial y^2} \right) \tag{3.2}$$

   A smaller $S_{pc}$ value means that the peak is rounded, whereas a larger $S_{pc}$ means that the peak is pointed.

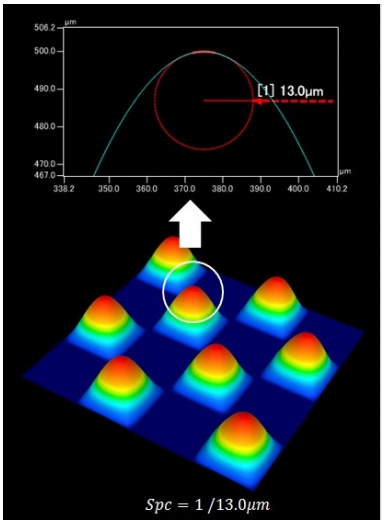
4. Kurtosis ($S_{ku}$): This parameter displays the dimensionless fourth power of the sampling length, giving an indication of the sharpness of the profile. A kurtosis value equal to 3, means that the height distribution is equally spiked and indented. If the value is less than 3, the surface has more indents than peaks and the other way around if the value is greater than 3. This is represented in Figure 3.14 (b).

$$S_{ku} = \frac{1}{S_q^4} \left[ \frac{1}{A} \iint_A Z^4(x,y) dx dy \right] \tag{3.3}$$

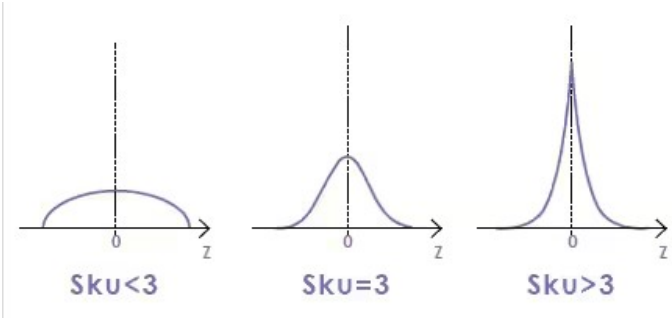
   Where $S_q$ is the root mean square deviation and $A$ is the area.

### 3.3.7. Copper Sulphate test

This test is used to determine presence of shunt paths in devices on foil. The processed sample is placed in a copper sulphate bath, acting as the negative electrode. A copper plate is also dipped in the bath, acting as the positive electrode. A voltage of 0.5V is supplied for 10 seconds, which dissociates




**(a)** Reference of Spc values




**(b)** Reference of kurtosis values

**Figure 3.14:** Surface roughness parameters

the solution to form copper ions. If there are any leakage paths present in the device architecture, the copper ions get deposited on the surface, which is indicated by the current measured by the multimeter.

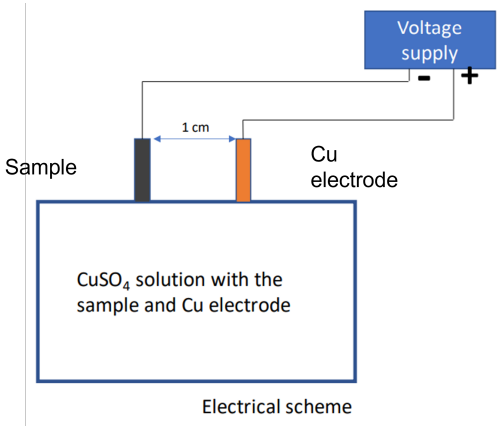



**Figure 3.15:** Schematic diagram of the Copper Sulphate test [28]

### 3.3.8. Light soaking setup

As mentioned in Section 2.1, a-Si:H solar cells undergo light-induced degradation when exposed to high-intensity light. To study this effect, a light soaker setup is used. This setup has multiple metal halide lamps for illuminating the samples which are placed on a stage. De-ionized water is used to keep the temperature constant. This is done by circulating the water in tubes to the stage. There are mirrors on each side of the stage to concentrate the light on the stage. The front open side of the setup is closed using a steel lid, which also has a mirror towards the inside. A highly sensitive spectroradiometer measures the power intensity of the lamps, which is around 700 $W/m^2$.

# 4

# Optimization of single junction a-Si devices on glass

The purpose of the experiments covered in this chapter is to test if the electrical performance of a single junction a-Si:H device can be maintained by reducing the absorber thickness from standard 300nm used uptil now at TU Delft. Section 4.1 gives a background of the a-Si:H devices and introduces the concept of band-gap profiling. In section 4.2, various configurations of the a-Si:H thicknesses are experimented, to observe the effect of a-Si:H band-gap profiling and thickness on device performance. Section 4.3 reports the effect of band-gap profiling on light-induced degradation. In Section 4.4, further experiments are conducted to improve the devices' spectral utilization and collection efficiency.

## 4.1. Background

As explained in Section 2.1, the band-gap of a-Si:H can be tuned through variation of the nano-structure by hydrogen dilution. Fischer et al [34] demonstrated a relation between the band-gap of a-Si:H, the deposition pressure and the $V_{oc}$ of the resulting device. At higher pressure regimes of deposition of a-Si:H, higher $V_{oc}$ can be attained. This is due to an increase in the size of the di-vacancies, which results in a volumetric compression of the Si matrix, thus increasing the band-gap of a-Si:H. This gives us room to improve the electrical performance of the solar cell.

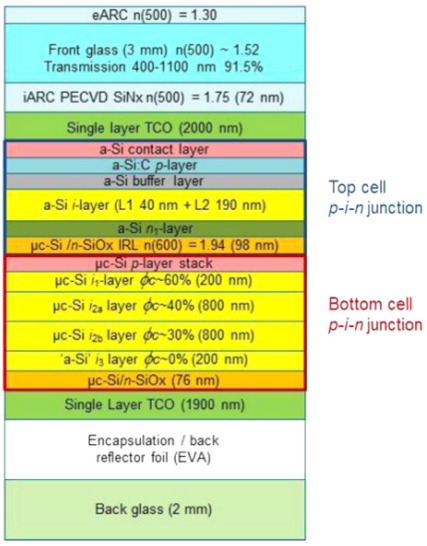
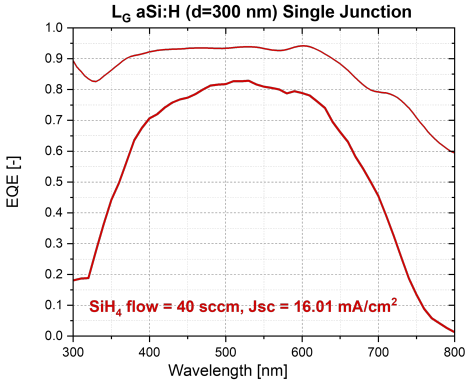



**Figure 4.1:** Device architecture used by TEL [35]

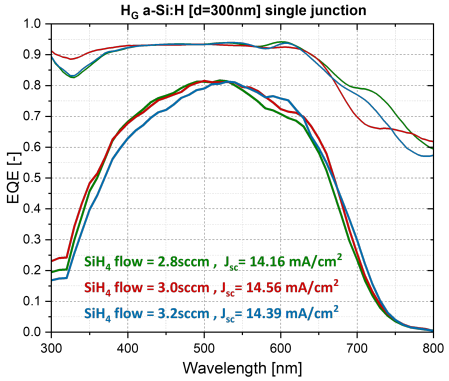
Cashmore et al [35] from TEL Solar AG developed a thin-film micromorph solar module in 2013, which

touched a record efficiency of 12.34% on a module area of 1.43m$^2$. The tandem structure shown in Figure 4.1, had an a-Si:H top cell, whose band gap was profiled in a way that an initial, high pressure a-Si:H layer (L1) of 40nm was deposited first. After this, 190nm of a-Si:H at a lower pressure is grown over the first layer (L2). By varying the pressures, it is expected that the band-gap of a-Si:H increases at higher pressure. Through this configuration and various light-trapping techniques, TEL achieved an initial $J_{sc}$ of 17.9mA/cm$^2$, initial $V_{oc}$ of 0.912V and a stabilized efficiency of 9.1% of the top cell. This architecture is used as an inspiration for the subsequent experiments in this chapter.

Tests conducted at TU Delft were aimed at optimizing the processing conditions for deposition of 300nm high band-gap a-Si:H and low band-gap a-Si:H. The results are shown in Figure 4.2.




**(a)** EQE for low band-gap a-Si:H




**(b)** EQE for high band-gap a-Si:H

| | |
|---|---|
| Voc [V]: | 0.855 |
| Jsc (mA/cm2) | 17.31 |
| Jsc-EQE | 16.01 |
| Rs [ohm·m²] | 13 |
| Rsh [ohm·m²] | 6187 |
| FF | 71.67 |
| η | 10.61 |
| $\eta_{EQE}$ | 9.81 |

**(c)** Electrical parameters for low band-gap a-Si:H

| | | | |
|---|---|---|---|
| Voc [V]: | 0.891 | 0.90 | 0.896 |
| Jsc (mA/cm2) | 16.18 | 16.30 | 16.28 |
| Jsc-EQE | 14.16 | 14.56 | 14.39 |
| Rs [ohm·m²] | 24 | 17 | 21 |
| Rsh [ohm·m²] | 5665 | 4742 | 5505 |
| FF | 0.67748 | 0.68019 | 0.694448 |
| η | 9.77 | 9.98 | 10.1 |
| $\eta_{EQE}$ | 8.54 | 8.94 | 8.95 |

**(d)** Electrical parameters for high band-gap a-Si:H

**Figure 4.2:** Variation of solar cell parameters based on L1-L2 thicknesses

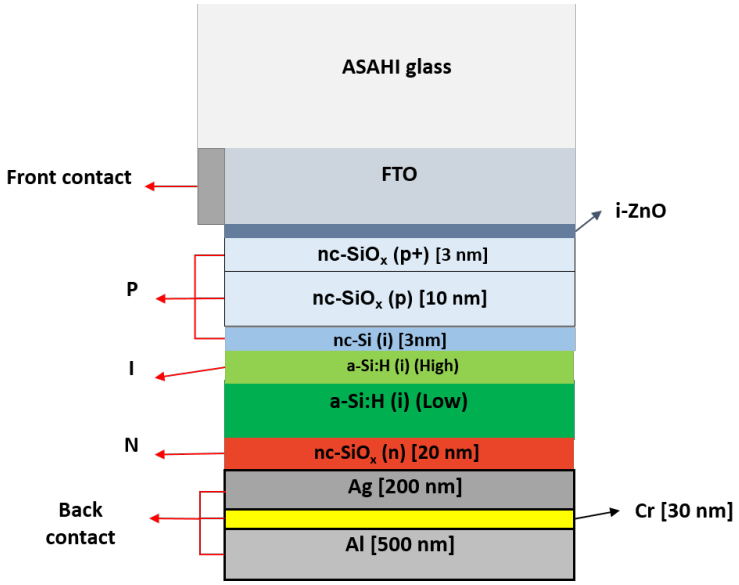
From Figures 4.2 (c) and (d), it can be seen that the low band-gap a-Si:H has a lower $V_{oc}$ due to more dangling bonds in the mid-gap state, whereas it has a higher $J_{sc}$ due to a higher response in the red spectrum than the high band-gap a-Si:H, as visible in the EQEs from Figures 4.2 (a) and (b). Looking at these results, the following experiments are tried in the subsequent sections:

1. Combination of high and low band-gap a-Si:H in one single absorber layer, varying the thickness of each layer (L1 and L2) and the total thickness of the absorber layer (230nm and 300nm). This is done to see if the electrical parameters can be boosted by i-layer grading and whether they can be maintained at a lower thickness.
2. Light-induced degradation of the samples with high band-gap a-Si:H to observe the effect of reduced mid-gap states on the Staebler-Wronski Effect (SWE).
3. Attempt to boost $V_{oc}$ by n-layer grading for improved charge carrier collection.
4. Attempt to boost red response through the addition of a back reflector.

## 4.2. Double i-layer series

In this section, we record two sets of experiments for making single junction a-Si:H devices as shown in Figure 4.3a:

- Varying the thicknesses of L1 and L2 to maintain a constant absorber layer thickness of 230nm.
- Using the L1 of the best-performing device above and increase absorber layer thickness.




**(a)** Figure 4.3: Device architecture

| | p+ nc-SiOx | p nc-SiOx | i-SiOx | High BG a-Si | Low BG a-Si | n nc-SiOx |
|---|---|---|---|---|---|---|
| **Pressure** | 2.2mbar | 2.2mbar | 2.2mbar | 10mbar | 0.7mbar | 1.5mbar |
| **Power** | 12W | 12W | 12W | 9W | 2.8W | 11W |
| **T (chamber)** | 300°C | 300°C | 300°C | 200°C | 300°C | 300°C |
| **$B_2H_6/H_2$** | 50 sccm | 10 sccm | - | - | - | - |
| **$CO_2$** | 1.2 sccm | 20 sccm | 2 sccm | - | - | 1.6 sccm |
| **$SiH_4$** | 0.8 sccm | 0.8 sccm | 0.8 sccm | 3 sccm | 40 sccm | 1 sccm |
| **$H_2$** | 170 sccm | 170 sccm | 170 sccm | 200 sccm | 0 sccm | 120 sccm |
| **$PH_3$** | - | - | - | - | - | 2 sccm |

**(b)** Table 4.0: Process parameters

These tests are done to see if the electrical parameters can be boosted by i-layer grading at a lower thickness and to compare the i-layer grading with increasing total absorber thickness. For both sets of experiments, an optimized triple p-layer recipe is used. The first p-layer (contact layer) is 3nm p-nc-$SiO_x$. This layer is heavily doped with boron, to ensure good ohmic contact with the front TCO. The second p-layer (window layer) is 10nm boron-doped p-nc-$SiO_x$, although this is much lesser doped than the contact layer. The buffer layer is 3nm intrinsic nc-$SiO_x$ deposited in the same chamber of AMIGO as the p-layers. This buffer layer ensures uniform growth of the subsequent a-Si:H layers, ensures better transport of the charge carriers at the p-i interface to prevent recombination, and prevents diffusion of boron into the i-layer [36]. Next, the absorber i-layers are deposited. A single, 20nm thick n-layer of nc-$SiO_x$ is deposited last. The process parameters are shown in Table 4.0.

### 4.2.1. L1:L2 ratio tuning to maintain total thickness of 230nm

In this experiment, the thicknesses of L1 and L2 are varied as shown in Table 4.1, and their effect on solar cell parameters is compared and studied.

#### Effect on solar cell parameters

The $J_{sc}$, $V_{oc}$, FF, efficiecny, $R_s$, $R_p$ and EQE values for each settings of L1-L2 are plotted.
As seen from Figure 4.4 (a), the $J_{sc}$ values do not vary drastically until sample 6, as the total thickness

| Sample | L1 (nm) | L2 (nm) |
|---|---|---|
| 1 | 0 | 230 |
| 2 | 3 | 227 |
| 3 | 10 | 220 |
| 4 | 20 | 210 |
| 5 | 30 | 200 |
| 6 | 40 | 190 |
| 7 | 60 | 170 |

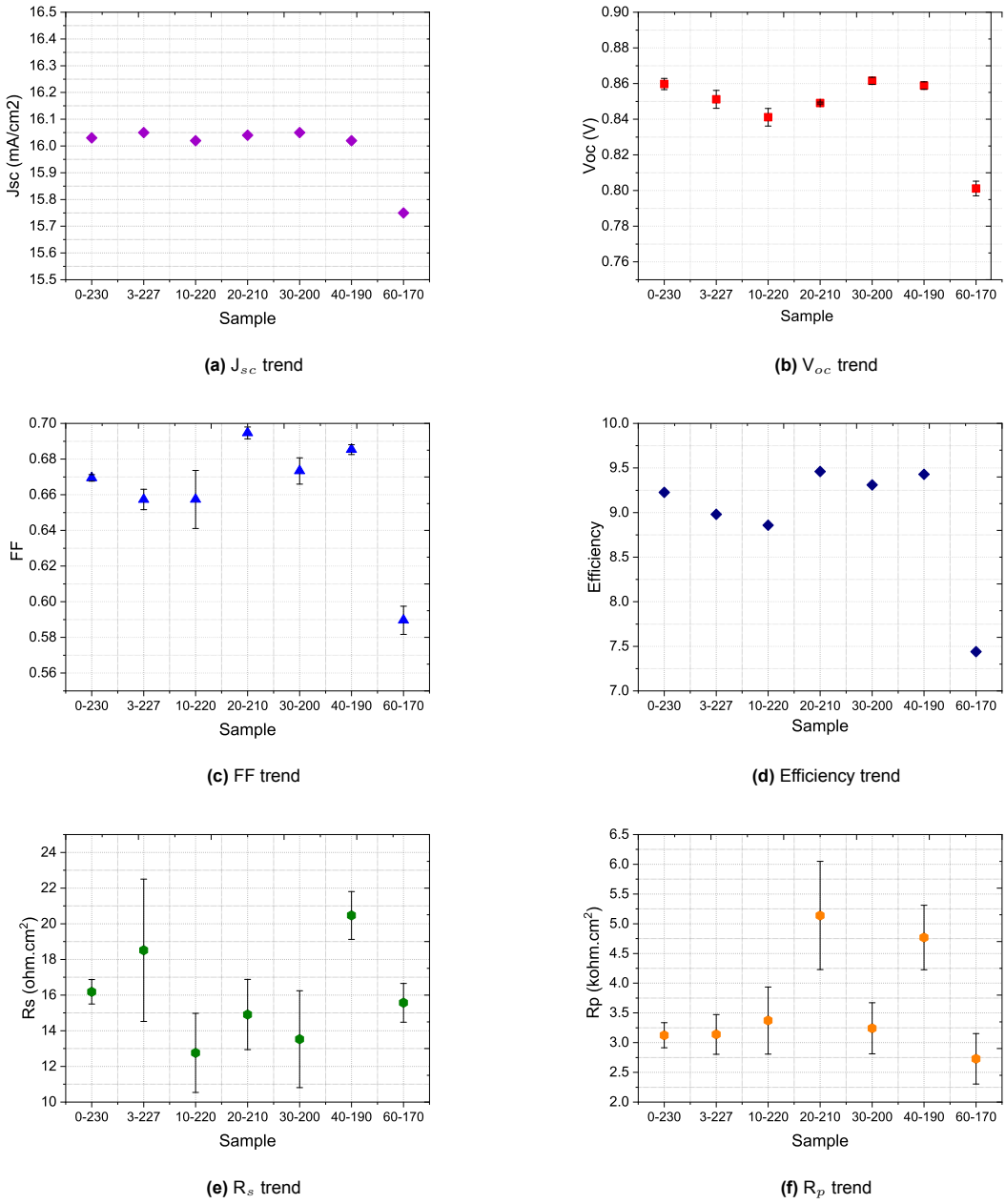
**Table 4.1:** Thicknesses of L1 and L2

of the absorber layer is constant at 230nm. The charge carriers generated, which depends on the thickness of the absorber layer, is approximately the same for all these devices, thus giving a similar $J_{sc}$ for all the devices. From Figure 4.4 (b), it is observed that with the addition of the high band-gap a-Si:H, the $V_{oc}$ of the devices is still in the range of 0.84V to 0.86V, while devices with similar configurations previously reached a $V_{oc}$ of 0.9V. This could be due to the following reasons:

1. Deposition of the very thin layers of the high band-gap a-Si:H (especially from 0nm to 10nm) is very sensitive to the plasma and chamber conditions. It could be possible that in the few seconds needed to deposit these layers, the desired plasma conditions are not reached due to start-up inertia and history of the chamber conditions.
2. The deposition of high band-gap a-Si:H is sensitive to the process parameters, especially the pressure. It is possible that at 10mbar pressure, more nano-voids are being introduced in the matrix, resulting in more defects and reducing the $V_{oc}$.
3. The triple p-layer deposition seems to vary from deposition to deposition, resulting in variation in the recombination losses in these layers. This requires a more critical analysis of the process parameters and chamber conditions for p- layer depositions.

Yet, the variation in $J_{sc}$ and $V_{oc}$ across the samples is not large enough to correlate the thickness of the high band-gap a-Si:H to the electrical properties. From Figure 4.4 (c) and (d), no particular trend in the fill factor or efficiency is seen. But it is worthwhile to notice that the sample with L1=20nm and L2= 210nm performed best in fill factor and efficiency, due to both low series resistance and high shunt resistance values as seen in Figures 4.4 (e) and (f), which is highly favorable. It is interesting to observe that Sample 7 has a lower $J_{sc}$, $V_{oc}$, FF and efficiency value than others. This is a trend that has been observed when this experiment was repeated. While one reason could be a deposition gone wrong, it is also possible that as the thickness of high band-gap a-Si:H is increased, the increased defect density results in higher recombination, thus reducing the electrical performance.
In Figure 4.5, the EQE of all the samples is plotted and observed. The blue response (350nm to 500nm) first increases after adding the high band-gap a-Si:H, but then falls back as the thickness of the high band-gap material is increased. This is not expected from the properties of a-Si:H, thus suggesting sample-to-sample variation in the deposition of the p-layers causing slight variations in the blue responses. The blue response can be higher (around 0.8), suggesting a parasitic absorption in the p-layers. It is interesting to note that the 'green' response (550nm to 650nm) for the device with the thickest high band-gap a-Si:H has drastically reduced, which is translating to a decrease in $J_{sc}$ of this device. This is also visible in the (1-R) fringe, of this particular device, which is much less than the others, indicating more optical losses in this particular device, probably arising from the thickness of the high band-gap material. The red response (650nm to 800nm) of the device without the high band-gap a-Si:H (black line) has a slightly higher red response (EQE at 700nm as reference) than the devices with increasing high band-gap thickness. On introducing the high band-gap a-Si:H, the device's performance is limited by the reduction in red response, as is visible from Figure 4.2. The reduction in red response could be attributed to the high band-gap a-Si:H (Equation 2.1). But the devices with the high band-gap a-Si:H have similar red responses. This is because the red response depends more on the light trapping by the layers after the intrinsic absorber layer, i.e. the n-layer, the back reflector, and metallic back contacts. Since all devices have the same layer after the absorber layer, the red response does not differ much, except for the slight sample-to-sample variation in deposition.

From the results of this experiment, it was concluded that the device with L1=20nm and L2=210nm




**(a)** $J_{sc}$ trend

**(b)** $V_{oc}$ trend

**(c)** FF trend

**(d)** Efficiency trend

**(e)** $R_s$ trend

**(f)** $R_p$ trend

**Figure 4.4:** Variation of solar cell parameters based on L1-L2 thicknesses

gave the best electrical performance. This configuration is used for the second experiment.

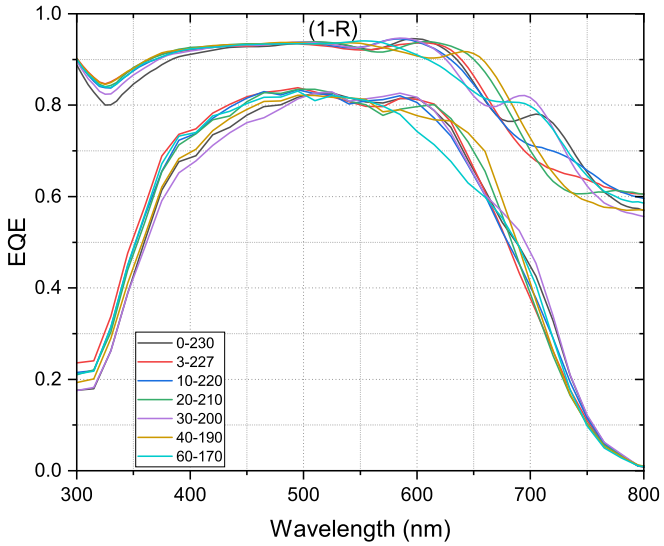



**Figure 4.5:** Variation of EQE based on L1-L2 thickness

### 4.2.2. Effect of increasing the absorber layer thickness

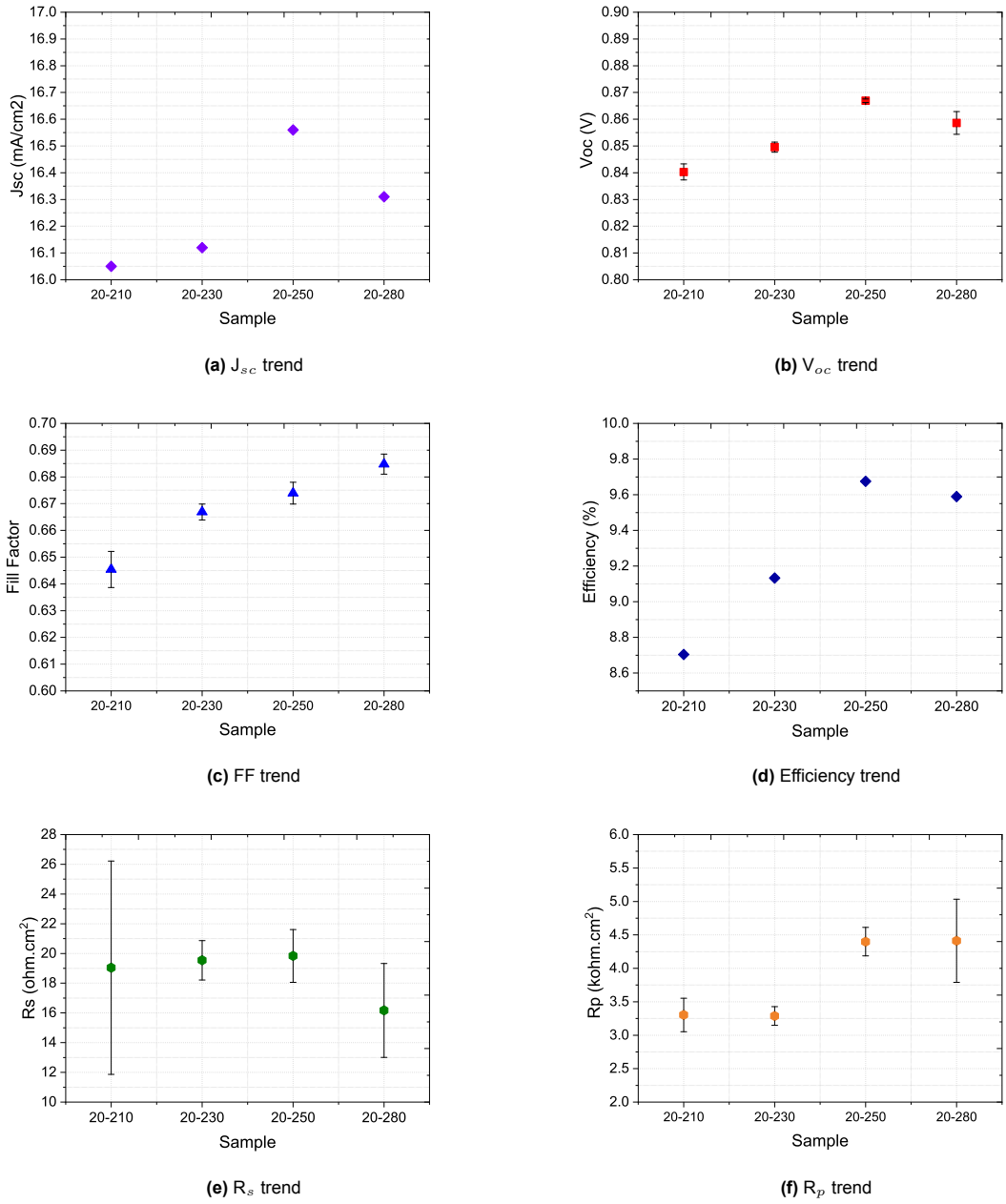
In this experiment, a constant 20nm high band-gap a-Si:H is used, and the thickness of the low band-gap a-Si:H is increased, to increase the total thickness of the absorber layer. This is to reach an optimum absorber layer thickness for maximum performance, which can also be translated to the devices on foil in the succeeding chapters. The device architecture is shown in Figure 4.3a, while the thickness series is shown in Table 4.2

| Sample | L1 (nm) | L2 (nm) |
|---|---|---|
| 1 | 20 | 210 |
| 2 | 20 | 230 |
| 3 | 20 | 250 |
| 4 | 20 | 280 |

**Table 4.2:** Thicknesses of L1 and L2

#### Effect on solar cell parameters

The $J_{sc}$, $V_{oc}$, FF, efficiency, $R_s$, $R_p$ and EQE values for each settings of L1-L2 are plotted below.




**(a)** $J_{sc}$ trend

**(b)** $V_{oc}$ trend

**(c)** FF trend

**(d)** Efficiency trend

**(e)** $R_s$ trend

**(f)** $R_p$ trend

**Figure 4.6:** Variation of solar cell parameters based on L1-L2 thicknesses

As seen from Figure 4.6 (a), the $J_{sc}$ values increase as the thickness of the absorber layer increases. This is because more charge carriers are available to be generated and collected at higher thickness of the absorber layer. The optimum $J_{sc}$ was reached at total aborber layer thickness of 270nm, since after a point, a thicker absorber layer also introduces more recombination sites, thus decreasing the $J_{sc}$. A similar reason results in the trend observed in $V_{oc}$ of these devices from Figure 4.6 (b). $V_{oc}$ is directly dependent (albeit a logarithmic relation) on the photogenerated current, as demonstrated in Equation 2.9. Since the photogenerated current increases with the thickness of the absorber layer, the $V_{oc}$ increases too, again until 270nm, after which the effect of increased recombination sites dominates. It is still counter-intuitive for $V_{oc}$ to increase with increasing thickness, since defect sites and saturation current density $J_0$ increase too. But the photogenerated current increase seems to be dominating the increase in saturation current density, resulting in an overall increase in $V_{oc}$. From Figure 4.6 (c), the fill factor is seen to increase as the thickness of the absorber layer increases. This is attributed to the reduction in series resistance and increase in shunt resistance as seen in Figures 4.6 (e) and (f), thus

boosting the operating point of the device. The increase in fill factor at 300nm thickness is counter-intuitive, which could be possible due to improved $R_p$ values at thicker layers, reducing sites of shunts and pin-holes. The efficiency also follows the trend of $J_{sc}$ and $V_{oc}$ as seen in Figure 4.6 (d), reaching an optimum at a total thickness of 270nm, and decreasing after.

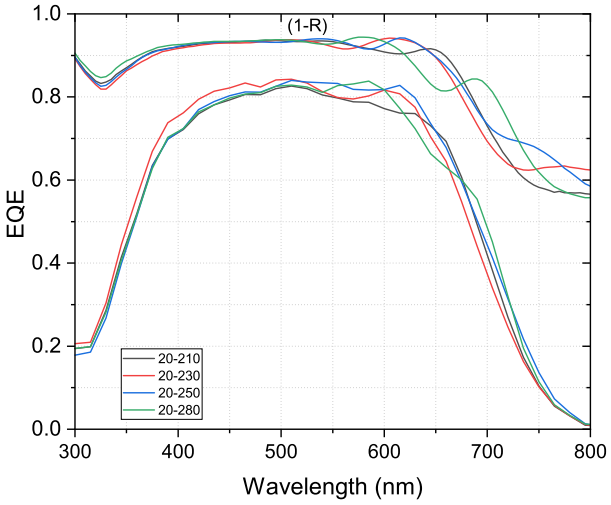


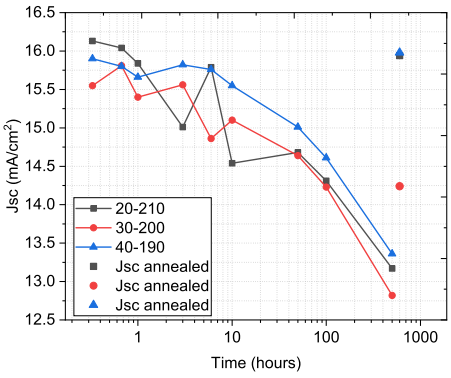

**Figure 4.7:** Variation of EQE based on L1-L2 thickness

From Figure 4.7, the blue response of all devices is seen to be the same, except for the device with 250nm thickness. These inconsistencies in the blue response suggest a non-reproducibility of p-layer depositions. The EQE is seen to increase as thickness increases in the wavelength range of 550nm to 650nm. This is because the optical path length of the green light is increased due to an increase in absorber layer thickness, thus facilitating more absorption in that wavelength region. The red response is not consistent across the devices; in principle, the red response should increase as the absorber layer thickness increases due to longer optical path lengths, which is not visible from the trend of these devices. This is also seen in the (1-R) curves of the devices. The device with 300nm absorber thickness (green line) seems to have a drastic reduction in the wavelength region 600nm to 700nm, which could be due to non-reproducibility in the n-layer depositions.
The electrical performance of the devices in the experiments conducted above is the 'initial' parameters. It is equally important to see at which point the device parameters stabilize, after being exposed to high-intensity light. This is discussed in the next section.

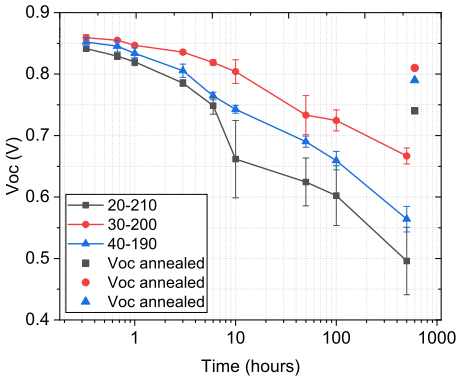
## 4.3. Study of light-induced degradation

In this experiment, the Staebler-Wronski Effect (SWE) on devices with a high-low band-gap configuration is studied. This is done to understand if the presence of high band-gap a-Si:H affects light-induced degradation in the device since it has more vacancies, but fewer dangling bonds. For this experiment, three devices from Experiment 4.2.1 have been chosen with the following L1-L2 configuration: 20-210nm; 30-200nm, and 40-190nm. These were the best performing cells of that experiment, and have been chosen to compare their stabilized parameters with the devices made by Cashmore et al [35]. They have been exposed to high-intensity white light of 700W/m$^2$ at 50$^o$C for 500 hours while measuring the electrical and optical performance at various times throughout the light-soaking. The results of the electrical parameters of the three devices are plotted.

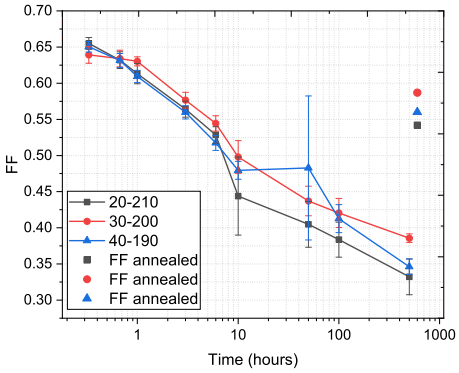
From the Figures 4.8 (a) to (f), the first observation is a drastic reduction in all the electrical parameters over the 500 hours of light soaking. We expect the degradation rate to reduce after 10 hours of exposure, which is not seen in this case. The parameters are degrading at the same rate for up to 500 hours and are expected to degrade even further, suggesting another cause for degradation apart from LID. Looking at the parameters of each device individually, the $J_{sc}$ of all three devices reduces at the same rate, reaching almost similar values at 500 hours. The $V_{oc}$ degradation for all three devices is different, with the sample having the thinnest high band-gap a-Si:H degrading the most. This is unexpected since a thinner layer of the porous material should have less degradation due to fewer vacancies. The $V_{oc}$ of the device with a 30nm high band-gap a-Si:H is higher than the device with a 40nm high band-gap a-Si:H, which is expected as explained above. The FF degradation is seen to follow the trend of the $V_{oc}$ of each device, with the device having a 30nm high band-gap a-Si:H degrading the least and the device having a 30nm high band-gap a-Si:H degrading the most. This can be correlated to the stabilized $R_s$ and $R_p$ values of each device. The $R_s$ values are seen to increase for each device, due to an increase in the recombination caused by the SWE, decreasing the mobility of the charge carriers and increasing the $R_s$ values. The $R_p$ values are all decreasing due to the degradation of the quality of a-Si:H. The final stabilized efficiency of each device shows a degradation of 65% to 75%, which is much higher than a typical SWE. To assess if this degradation is reversible or permanent, these samples are annealed for 30 minutes at 180$^o$C and the electrical parameters are measured (solid icons in each graph) It is seen that the $J_{sc}$ values of the devices with 20nm and 40nm high band-gap a-Si:H is completely recovered and not for the device with 30nm high band-gap a-Si:H. This can be explained better with EQE plots. The $V_{oc}$, FF, efficiency, $R_s$ and $R_p$ of the devices are not completely recovered, although the device with 30nm high band-gap a-Si:H has the highest recovery for all other parameters except $J_{sc}$. This indicates that the device with 30nm high band-gap a-Si:H is undergoing a permanent optical degradation apart from another chemical degradation. The optical performance (EQE) of the devices and the effect after annealing is shown in Figure 4.9. The EQE of all three devices is decreasing on exposure to light soaking, due to an increase in defects throughout the intrinsic layer and reducing the charge carrier collection. The effect of degradation is known to be most at the p-i interface due to maximum collection at this interface. But in these devices, the degradation is seen even at the i-n interface and the n-back contact interface, suggesting a degradation of the n-layers and the metal back contact as well. Investigating this further, it was noticed that the evaporation rate of the back contacts resulted in a less dense metal deposition, which could degrade more under light soaking than metals evaporated at a slower rate, giving much denser metal layers. To see if this effect is permanent, the EQE before and after annealing is plotted for each sample. It is seen that the EQE for devices with 20nm and 40nm high band-gap a-Si:H is completely recovered and not for the device with 30nm high band-gap a-Si:H. There seems to be a permanent degradation of the p-layers of this particular sample, which is causing a drop in the $J_{sc}$. All these results indicate a permanent degradation in the samples, which can be explored further, but is outside the scope of this thesis.



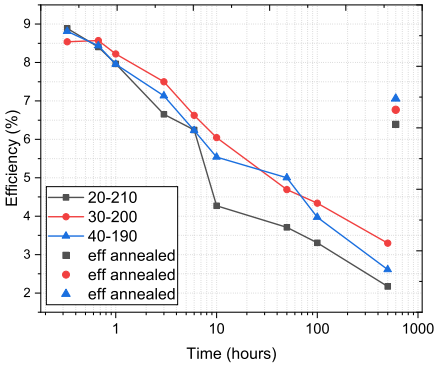

**(a)** $J_{sc}$ trend



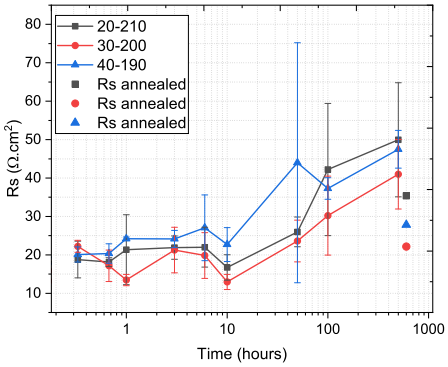

**(b)** $V_{oc}$ trend



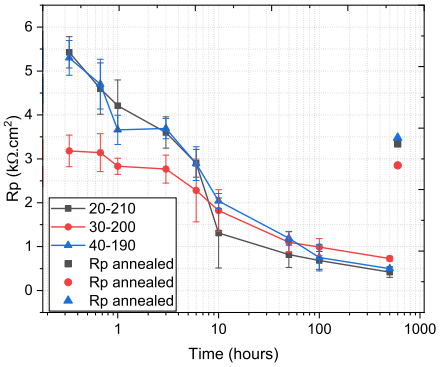

**(c)** FF trend




**(d)** Efficiency trend

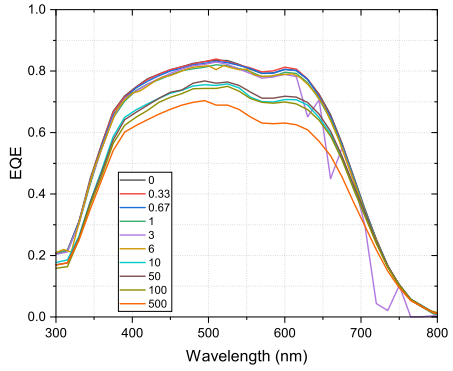



**(e)** $R_s$ trend

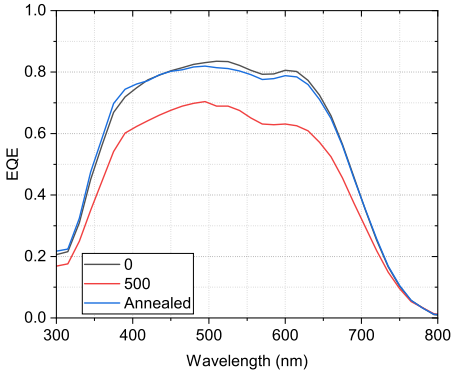



**(f)** $R_p$ trend

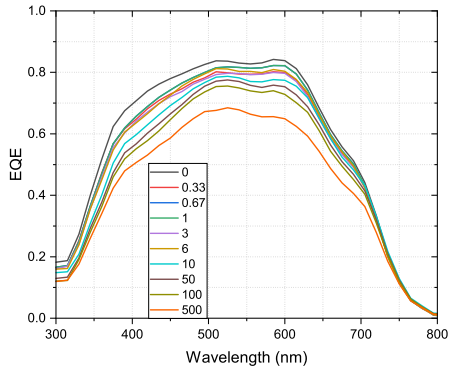
**Figure 4.8:** Variation of solar cell parameters on light soaking



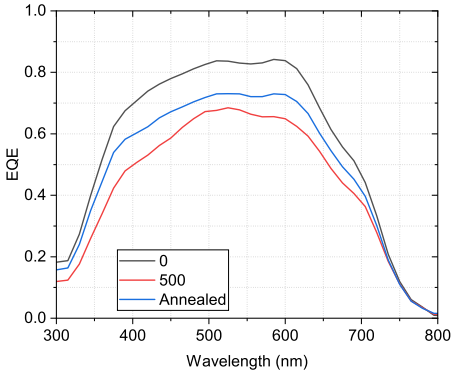

**(a)** EQE for sample 20-210 through LID



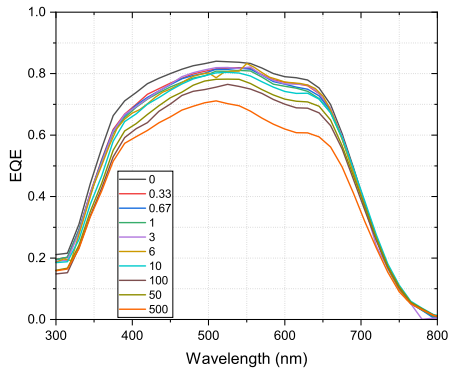

**(b)** EQE recovery for sample 20-210 after annealing



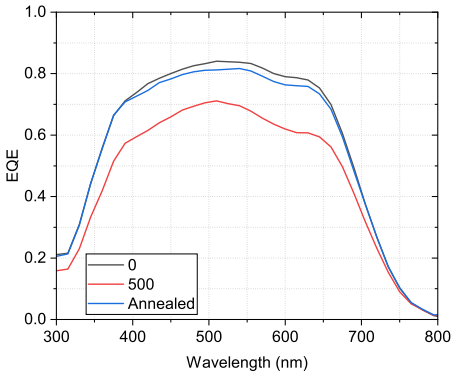

**(c)** EQE for sample 30-200 through LID




**(d)** EQE recovery for sample 30-200 after annealing




**(e)** EQE for sample 40-190 through LID




**(f)** EQE recovery for sample 40-190 after annealing

**Figure 4.9:** Effect of LID and annealing post LID, on EQE of the samples

## 4.4. Towards an improved spectral utilization and collection

From the experiments in Section 4.2, we have seen that there is still room for improvement in the device architecture, to attain record electrical parameters. One way is to enhance the charge carrier collection through the doped layers, to boost the $V_{oc}$. Another way is to boost absorption of the red light of the spectrum by incorporating some light management tricks to facilitate more absorption of red light. Ideally, the aim is to increase the optical path length of the photons, without increasing the absorber layer thickness. This can be done by reflecting the light back into the absorber layers, so they can generate electron-hole pairs. These experiments are discussed in the following subsections.

### 4.4.1. n-layer optimization

In this experiment, the aim is to improve the charge carrier collection, through manipulating the n-layers. The main n-layer, n-nc-SiOx, serves both as a n-layer for generating an electric field and as a back-reflector as it can reflect back light into the absorber layer. It has dominant properties over n-a-Si:H, having lesser parasitic absorption and higher transparency due to a higher bandgap. From Equation 2.7, it can be inferred that for the light to have maximum reflectivity, media 2 (n-ncSiOx) must have a much lower refractive index than media 1 (i-a-Si:H). The refractive index of a-Si:H deposited is 3.76, while the refractive index of n-nc-SiOx is around 2 at 900nm. Thus, the value of R from Equation 2.7 is high, meaning maximum light is reflected back into the absorber layer.
n-nc-SiOx has lower lateral conductivity and 2 orders higher transverse conductivity than n-a-Si:H, owing to columnar growth of SiOx [37]. The low lateral conductivity also prevents cause shunt paths by connecting to adjacent cells [38].
To boost the charge carrier collection at the back of the device, a triple n-layer is used similar to a triple p-layer. The three n-layers are as follows: first is a 5nm n-a-Si, preventing the diffusion of phosphorus into the bulk i-layer and to reduce recombination at the i-n interface, second is 20nm n-nc-SiOx and the third is 5nm, n-nc-Si, for facilitating better collection of charge carriers and good ohmic contact with the metals. The combination of n-nc-SiOx and n-nc-Si also facilitate better shunt resistances, with the n-nc-SiOx behaving as an interlayer, to reduce the sites of local current leakages [39].
Four devices are made, with the architecture as specified in Figure 4.10. Two devices have a single n-layer and two have a triple n-layer. For each n-layer configuration, the two L1-L2 settings are used: 20nm-210nm and 20nm-280nm. Through this, we aim to observe the effect of both triple n-layers on $V_{oc}$ and the increasing absorber layer thickness on the $J_{sc}$ and optical resposne of the devices.

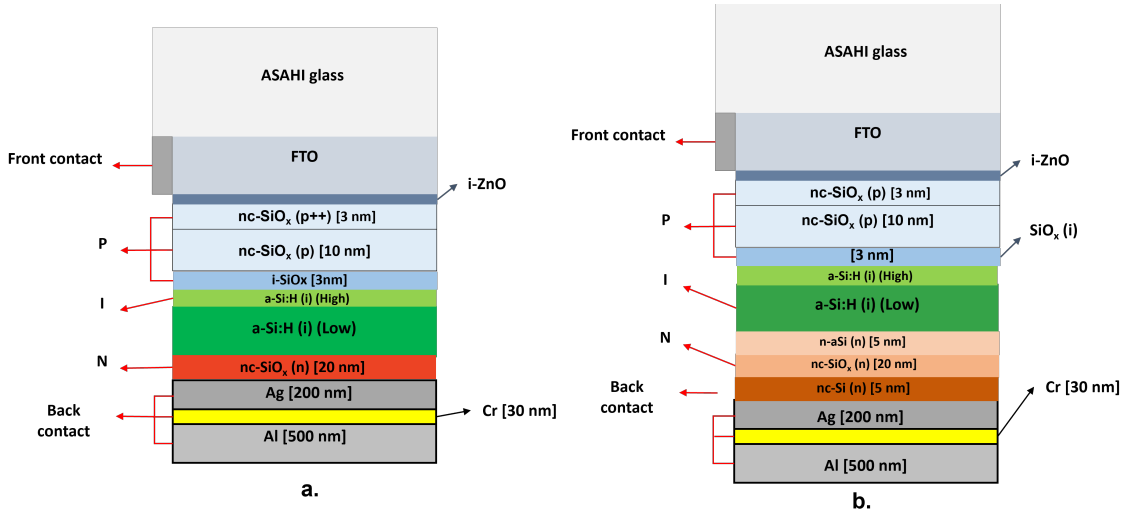
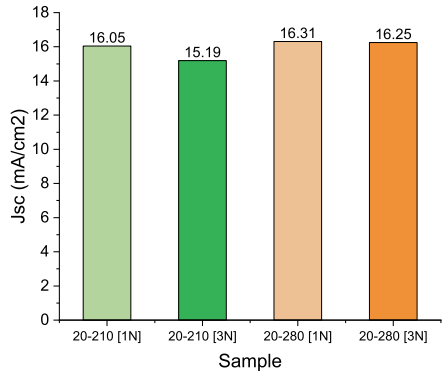



**Figure 4.10:** Device architecture for triple n-layer variations

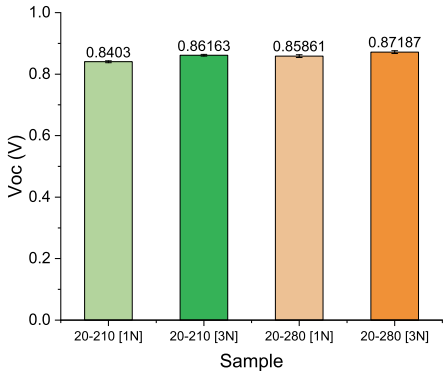
#### Effect on solar cell parameters

The $J_{sc}$, $V_{oc}$, FF, efficiency, JV and EQE of these devices are plotted in Figure 4.11
As expected, Figure 4.11 (a) shows that as absorber layer thickness increases from 230nm to 300nm, the $J_{sc}$ increases. But interesting is to note the effect of the triple n-layer. For both the L1-L2 settings, the $J_{sc}$ is seen to decrease slightly. This is counter to the effect desired, hinting towards parasitic absorption in the triple n-layers, possibly in n-a-Si. From Figure 4.11 (b), the $V_{oc}$ of the devices is seen to increase slightly with the addition of the triple n-layer. This variation is due to a reduced recombination by the addition of the buffer n-a-Si, which enhances the interface between the i- and n- layer, indicating a better layer growth from i-a-Si to n-a-Si to n-nc-Si. Also, since the ohmic contact between the n-layers and the metal is improved by using n-nc-Si, this improves the charge carrier collection and hence the $V_{oc}$. From Figure 4.11 (c), the fill factors are seen to improve as thickness increases, which is due to increased shunt resistance values at greater thicknesses. At higher thicknesses, the layers are more

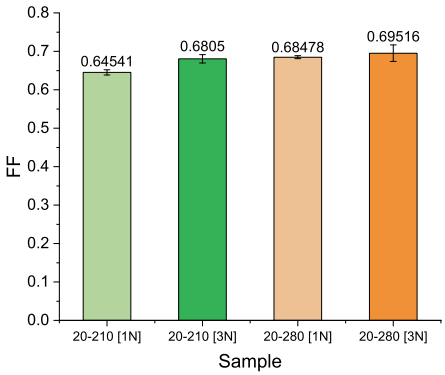
uniformly covering all possible shunt sites, hence are less prone to being damaged to cause shunts, which is reflected in Figure 4.11 (f). The increase in series resistance in Figure 4.11 (e) on adding the triple n-layer is expected due to increasing the number of contacting layers. But the effect of shunt resistance is seen to dominate over the effect of series resistance, thus increasing the fill factors. The combined effects of $J_{sc}$, $V_{oc}$ and FF is seen in the efficiency of the devices in Figure 4.11 (d), with the 20nm-280nm combination having the triple n-layer is seen to perform the best.
From Figure 4.12, the EQE performance of the devices is seen. It is interesting to note that the blue response for the device with 230nm absorber thickness and triple n-layer (black and red curve) is the same, even with different n-layers, showing that the additional n-layers is not boosting the blue response. This shows that all the blue light has been completely absorbed in the absorber layer before reaching the back reflector. But the red responses for these two devices is drastically different. The device with the triple n-layer (red curve) is losing a lot of red response (550nm to 750nm), hinting that the triple n-layer for this device is having more parasitic absorption of red light in the n-layers. This is also seen in the absorptance curves, with the light after 700nm being reflected from the n-layers but not being absorbed. On the other hand, for the devices with 300nm absorber layer thickness, the blue response for the device with triple n-layer (green curve) is much lower than the device with the single n-layer (blue curve). This could be due to inconsistencies in the p-layers, which is already known to vary from deposition to deposition. From the wavelength range of 550nm to 600nm, the device with single n-layer has slightly higher EQE and higher absorption than the device with the triple n-layers, indicating that some part of the green light is getting absorbed in the triple n-layers. Between 600nm and 700nm, the device with the triple n-layer has slightly higher EQE and absorptance than the device with single n- layer, indicating that the light is neither being absorbed enough in the first pass nor reflected in the device with the single n-layer. After 700nm, both devices have the same EQE, while the device with the triple n-layer has higher absorption, indicating that the red light is being parasitically absorbed in the n-layers, resulting in the same EQE.



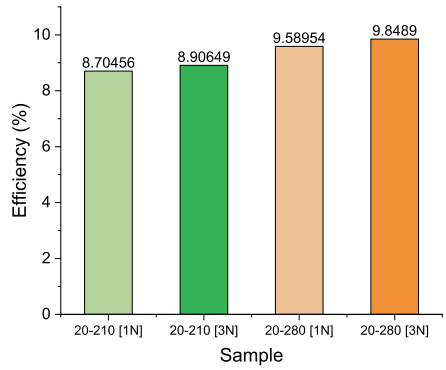

**(a)** $J_{sc}$ trend



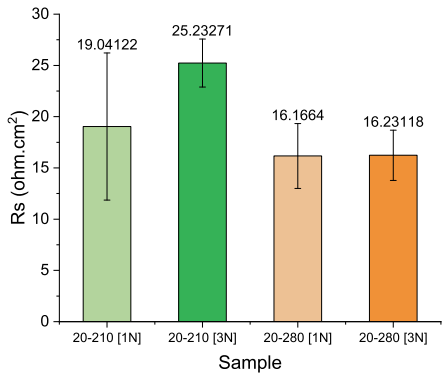

**(b)** $V_{oc}$ trend



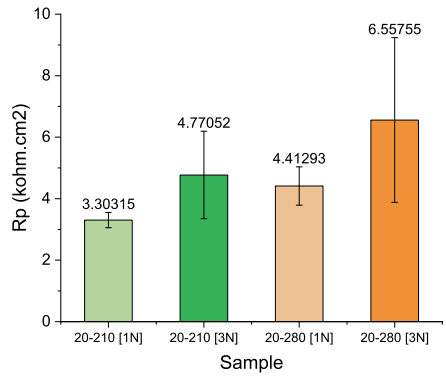

**(c)** FF trend




**(d)** Efficiency trend




**(e)** $R_s$ trend




**(f)** $R_p$ trend

**Figure 4.11:** Variation of solar cell parameters based on L1-L2 thicknesses

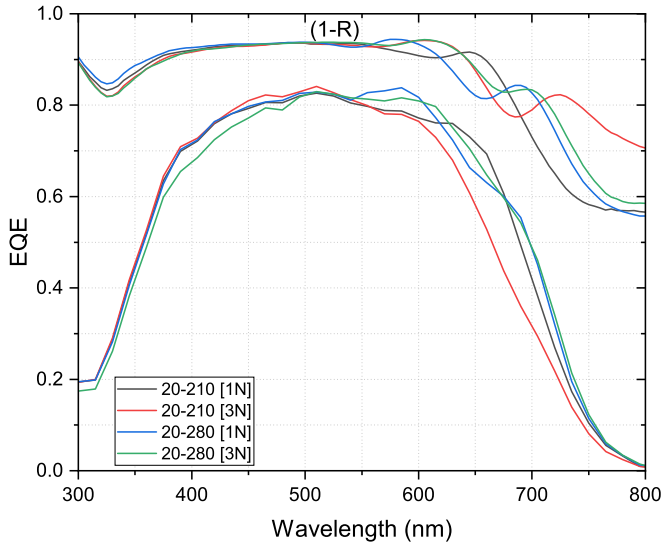



**Figure 4.12:** Variation of EQE with variation in n-layers

### 4.4.2. Addition of a back-TCO

We have seen from the previous experiment that the addition of multiple n-layers is hampering the optical response of the device. To try a different route, a back reflector is used instead of the multiple n-layers, to see if the red response can be boosted. In this experiment, intrinsic zinc oxide (i-ZnO) is used as a transparent layer at the back in the single junction device architecture. i-ZnO is a semiconductor with a band-gap of 3.37 eV. It is transparent in the visible region (reported transparency of 90%), so any light being reflected from the metal back contact is transmitted through the TCO back into the absorber layers. The crystals of i-ZnO grow predominantly in the vertical direction (002 orientation), thus facilitating good conductivity in the transverse directtion and minimal conductivity in the lateral direction [40] [41]. i-ZnO is highly abundant, economical, non-toxic, easy to produce, and is chemically and thermally stable. Another added advantage of i-ZnO is its ability as a local series resistance to inhibit shunts caused by spatial inhomogeneity in a-Si:H [42].

The experiment is performed as follows: two single junction devices are made, both with 30nm of high band-gap a-Si and 200nm of low band-gap a-Si. Both have a triple p- and single n- layer. To understand the effect of i-ZnO as back TCO, one device has i-ZnO deposited after the n-layer, while the other does not. 80nm i-ZnO is sputtered at 300$^{o}$C, using masks having 30 square dots of area 5$\times$5 mm$^2$. The device architecture is shown in Figure. The effect of the back reflector TCO on the electrical properties of the solar cell is discussed below.

#### Effect on solar cell parameters

The initial $J_{sc}$, $V_{oc}$, FF and efficiency values for each device are noted in Table 4.3.

| Parameter | Device without i-ZnO | Device with i-ZnO |
|---|---|---|
| $J_{sc}$ (mA/cm$^2$) | 16.64 | 16.51 |
| $V_{oc}$ (V) | 0.834 | 0.843 |
| FF | 65.68 | 56.27 |
| Efficiency (%) | 8.97 | 7.83 |
| $R_s$ ($\Omega$.cm$^2$) | 12.99 | 43.18 |
| $R_p$ (k$\Omega$.cm$^2$) | 3.32 | 4.21 |

**Table 4.3:** Electrical parameters of devices without and with i-ZnO

From Table 4.3, it is seen that the addition of a back-TCO did not enhance the electrical parameters of the device. To visualize this better, the J-V curve for both the devices is plotted in Figure 4.13.

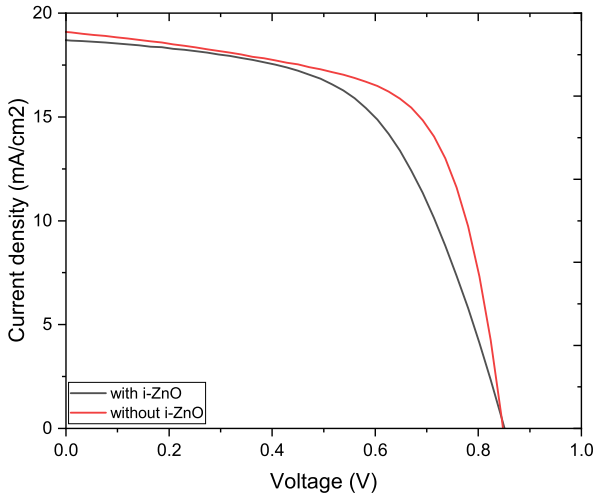



**Figure 4.13:** J-V curves of devices with and without i-ZnO back reflector

As seen from Figure 4.13, the effect of the back-TCO is clearly seen by a decrease in fill factor, due to an increased series resistance. The series resistance is originating from mismatch between the contact areas of the i-ZnO and the metal back contacts. While the i-ZnO dots are $5\times5$ mm$^2$ in size, the metal back contacts are $4\times4$ mm$^2$ in size. And since they are deposited in different equipments using different masks, there is a high probability of mis-alignment of the dots. This results in a lateral conduction of current in i-ZnO, also increasing the series resistance. This effect is visualized in Figure 4.14.

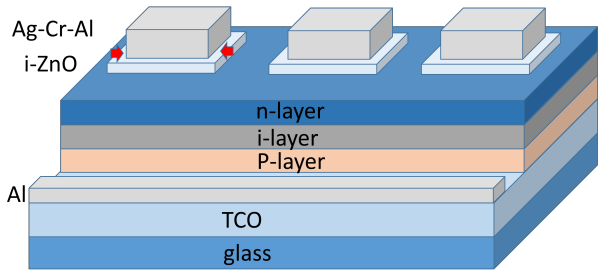



**Figure 4.14:** Schematic representation of misalignment of i-ZnO and metal back contact (Borrowed from Prof. Arno Smets)

The EQEs of both these devices are plotted in Figure 4.15 to see if there is any improvement in the red response. From Figure 4.15, it can be seen that there is no improvement in the red response, suggesting that the i-ZnO is not facilitating the red response boost as desired. This could be either due to the fact that since the band-gap of i-a-Si only absorbs light till 750nm it cannot absorb more red light than it already did, or there is some parasitic absorption in the n-layer or i-ZnO itself. It is interesting to note that the absotpance values of both devices differ after 650nm. The device without i-ZnO has a higher absorptance, which is not being reflected in the EQE, suggesting that there is a parasitic absorption in the n-layer.

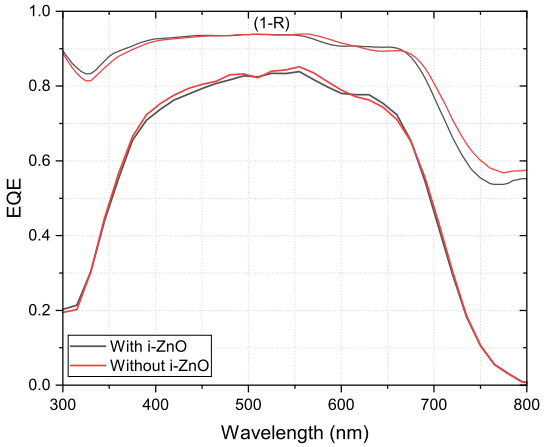



**Figure 4.15:** EQE and absorption of devices with and without i-ZnO

## 4.5. Key Take-Aways

From the experiments conducted above, the following important conclusions can be made:

1. At 230nm of i-absorber layer, we achieve almost similar electrical and optical parameters as 300nm of i-absorber layer.
2. The deposition of high band-gap a-Si:H is sensitive to the high-pressure. If this is not controlled or optimized, it can form more nano-voids, resulting in loss of $V_{oc}$ instead of the gain we require.
3. Increasing the absorber layer thickness gradually and slightly improves the electrical parameters, although with not much contribution from the high band-gap a-Si:H.
4. Thicker absorber layers are crucial to improving the shunt resistance values of the device.
5. The effect of high band-gap a-Si:H on light-induced degradation is still unclear. While it is expected that the device with thinnest high band-gap a-Si:H should degrade the least due to lesser nan-voids, this trend is not visible. Also, the device with 30nm high band-gap a-Si:H recovers the most, which does not follow any trend. This needs to be corroborated with more depositions with the same parameters to gain more statistics.
6. There is a permanent degradation in these devices, most probably of the metal back contact due to faster rates of evaporation.
7. Additon of multile n-layers to boost electrical and optical performance is seen to decrease $J_{sc}$ due to parasitic absorption in the extra layers, increase in $V_{oc}$ due to improved charge carrier collection in the triple n-layers, increase in fill factor due to improved $R_s$ and $R_p$ values and an overall increase in efficiency.
8. Addition of an internal back reflector TCO causes an increase in $R_s$ due to mismatch of the deposition areas of the TCO and metal back contact, thus decreasing the device's performance. No improvement in the optical response is oberved either.

# 5

# Shunt hunt- Devices on Foil

In the previous chapter, the devices with a combination of high-low band-gap a-Si:H have been fabricated on a glass substrate and optimized for improved performance. An attempt is made to translate the optimized device on the foil. While doing this, one major bottleneck was identified: a very low yield due to low shunt resistance values. Section 5.1 gives a short background on the history of shunt resistances in devices on foil. In the sections later, different possible causes for the low shunt resistances are investigated.

## 5.1. Background

As discussed in Section 2.7, low shunt resistances can immensely hamper the solar cell's performance. The shunt resistance values acceptable are of the order of 1 k$\Omega$.cm$^2$ and higher for single-junction devices and 10 k$\Omega$.cm$^2$ and higher for tandems (thicker layers are seen to have higher shunt resistances). The devices on foil processed in Delft since April 2021 suffered from low yield and low shunt resistances [43], with values reaching <$10^{-2}$ k$\Omega$.cm$^2$. Many possible causes were previously hypothesized, to identify the source of the shunts, which are listed below:

1. The sputtering and annealing processes of back contact were suspected to diffuse aluminum into the n-layer, resulting in a p-i-p device instead of a p-i-n device. This was explored by Papriwal et al [18] by using AZO before depositing aluminum. The AZO behaves both as an internal reflecting layer to trap more light and as a protective layer to prevent the diffusion of aluminum. The improvement in shunt resistance values is seen in Figure 5.1. This still does not give the best shunt resistance values, indicating some more causes of low shunt resistances.

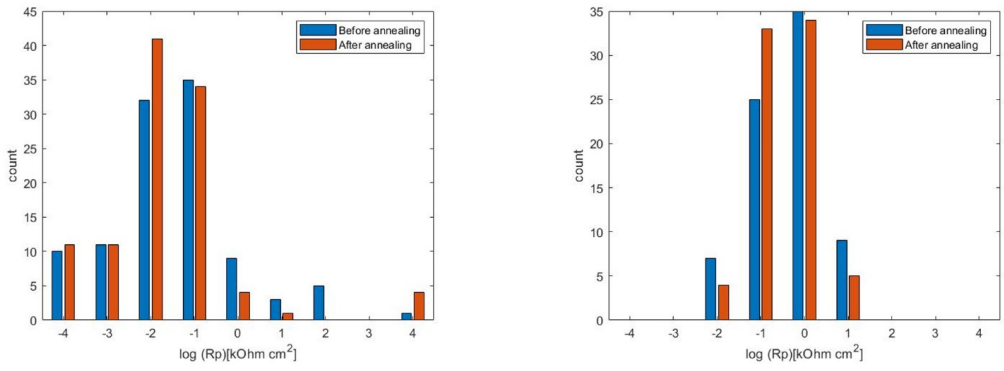



**Figure 5.1:** (a) $R_p$ values without back AZO (b) $R_p$ values with back AZO [18]

2. Nano-crystalline silicon bottom cell in the tandems was suspected to be current-leaking by Padmakumar et al [43]. If the quality of the i-nc-SiO$_x$ is poor or the doping of the tunnel recombination

junctions is too high, the layers could facilitate current flow in the lateral direction. EQE plots without bias light can help identify leaky sub-cells. As shown in Figure 5.2, a blue response of tandems in dark suggests a leaky bottom cell.

3. The scribing step (either P1 or P3), if not done correctly, can induce leakage currents. If the scribe is not completely opened, it does not isolate the active areas of the cell, creating a short circuit path for the current flow. can be created. This is shown in Figure 5.3.

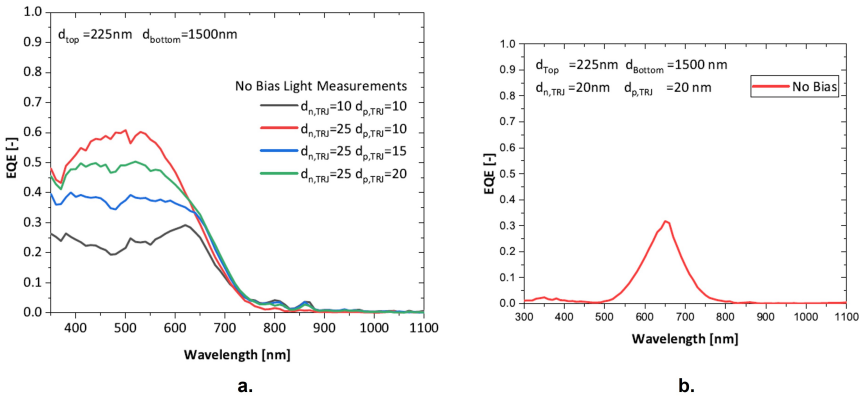



**Figure 5.2:** (a) Observed EQE of tandems (b) Desired EQE of tandems without bias light [43]

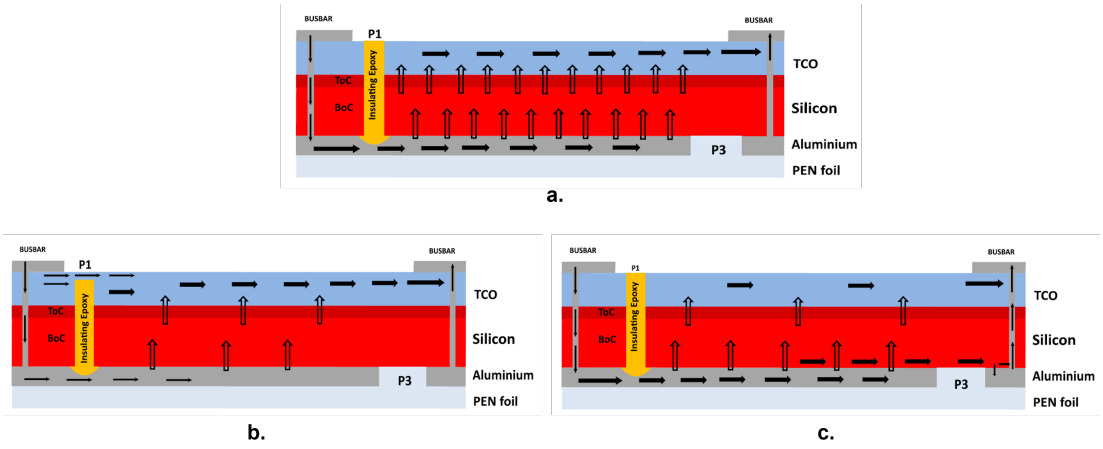



**Figure 5.3:** (a) Ideal path of current flow in a cell (b) and (c) Alternate current flow paths due to faulty device [43]

4. The samples have been observed to undergo severe bending after processing of the FTO and active layers. Every processing step after FTO deposition requires the sample to be stretched back. This could cause stresses in the sample, causing it to crack. These cracks can be sites of recombination or shunts.

In the subsequent sections, hypotheses 2,3 and 4 will be tested, and further hypotheses made along the way will be tested and proved.

## 5.2. Investigation of leaky n-layers

From the literature, nc-SiOx is known to grow as crystal-like filaments perpendicular to the substrate, making it more conductive in the transverse direction than in the lateral direction. But, from test layers deposited at TU Delft [43], it was observed that the n-nc-SiOx deposited is more conductive in the lateral direction than n-a-Si:H (Conductivity of n-nc-SiOx is 0.2 S/cm while the conductivity of n-a-Si:H is 0.02 S/cm). The higher lateral conductivity of n-nc-SiOx in the TRJ or bottom cell can create an alternate path for current to flow than in a transverse direction, connecting local shunt sites in the device and resulting in leakage currents. This can be significantly detrimental for devices when connected in series, which can have huge losses due to the leakage current. To test this theory, tandem devices (diodes and superCOFs) were made with variations in the n-layers in the TRJ and the bottom cell. This is shown in Figure 5.4. For brevity, these devices are called N1, N2, and N3 respectively.


**Figure 5.4:** Schematic diagram of samples with n-layer variations

Diodes are fabricated and characterized by measuring the J-V curves in the dark to extract $R_p$ values. Since each $10 \times 10$ cm$^2$ sample has 196 small area diodes, the J-V curves are not shown, and only the $R_p$ values are plotted in Figure 5.5.

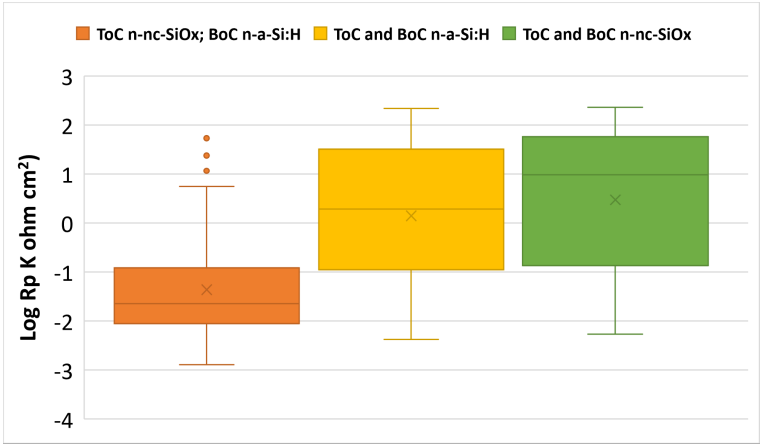
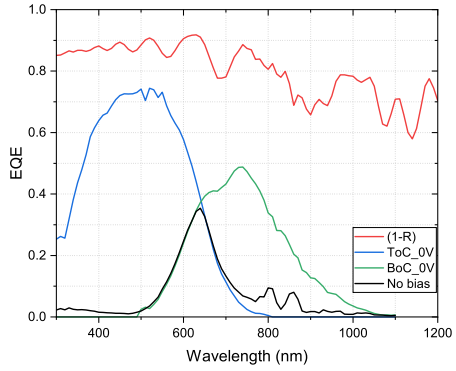
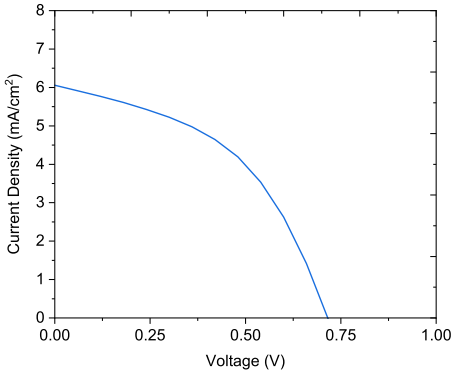



**Figure 5.5:** Comparison of log $R_p$ values for each n-layer variation

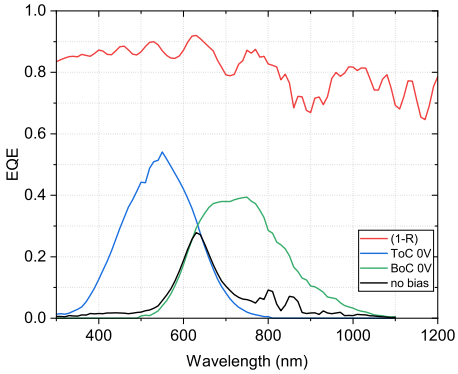
It can be seen that the diodes with different n-layers in the TRJ and bottom cell perform the worst, while the devices with the same n-layers in the TRJ and bottom cell performs the same, irrespective of the type of n-layer. The majority of $R_p$ values are still less than the desired 10 k$\Omega$.cm$^2$. It is unusual for the device with different n-layers to perform so drastically differently from the devices with the same n-layers. One reason could be that the conditioning in the n-layer chamber does not support two different layers being deposited in one run. Hence this effect is not seen in devices having the same n-layers. It could also be possible that this particular sample was subjected to more bending and stretching, which could have resulted in lesser shunt resistance values.



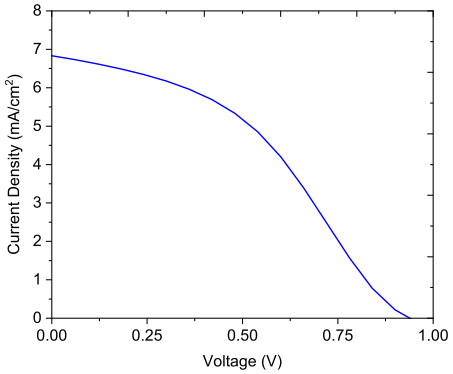

**(a)** EQE- device N1



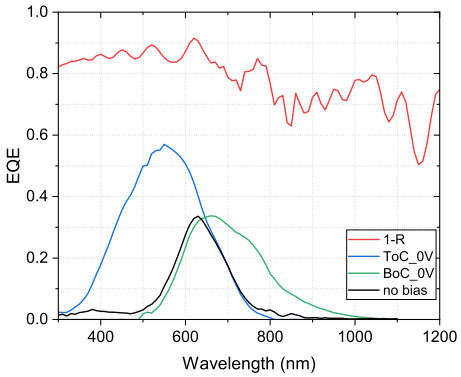

**(b)** JV- device N1



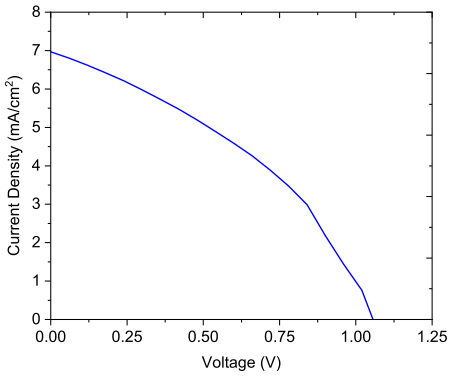

**(c)** EQE- device N2




**(d)** JV- device N2




**(e)** EQE- device N3




**(f)** JV- device N3

**Figure 5.6:** Comparison of EQE response and JV curve for each n-layer configuration

The superCOFs are used to compare the optical performance of the devices. The EQE of each configuration is measured and plotted in Figures 5.6. The device with different n-layers in the top cell and bottom cell has the best EQE (Figure 5.6 (a)), with no indication of the device being shunted and no visible capping in the blue response (top cell EQE). The no-bias EQE shows a near-perfect fit, with some fringes after 700nm, indicating a leaking top cell. The J-V curve shown in Figure 5.6 (b) shows a good solar cell performance, with a decent shunt resistance. But this performance does not correspond with the low shunt resistance values observed in Figure 5.5. While it is true that there are two separate samples used for making diodes and superCOFs which could cause a sample-to-sample variation in handling or deposition, it is very unlikely that a heavily shunted cell shows such an EQE response.

One possible explanation is that the characterization of diodes is not the most robust technique to give insights into the device's performance. $R_p$ measurement of diodes is done manually, where the probes contact with a very delicate foil, which could pierce through the diode. This is not the case for super-COFs that have the PEN foil lamination to reduce the pressure due to probing. The devices with the same n-layers (Figures 5.6 (c) and (e)). show poor optical performance which is contradictory to the diode performance seen in Figure 5.5. The J-V curve of N2 (Figure 5.6 (d)) shows a hint of the formation of a barrier at the TRJ, thus causing a drop in the $V_{oc}$ of the device. The J-V curve of N3 (Figure 5.6 (d)) shows a resistor-like behavior since the curve is almost a straight line. This also indicates slight variations in the depositiions for each sample. It is interesting to note that all three devices have very similar (1-R) values between 300nm and 500nm, indicating that the reflection from the top surface is the same. Even then, the EQE of the top cells of the three devices is strikingly different. This could indicate a parasitic absorption in the TCO, p-layers, or the i-layer, which seems unlikely as all three samples have the same deposition parameters for each layer and this drop in EQE is very much for it to be a parasitic absorption. If the bias light is not sufficient enough for the generation of charge carriers in the absorber layers, it could decrease the EQE response of the top cell in the 300nm to 500nm range, resulting in such lowered EQEs. It could also be an effect of the presence of shunts in the devices, which have an alternate path for the current to go through, thus not giving the EQE as expected by a p-i-n junction.
Looking at the bottom cell responses of the three devices, devices N1 and N2 are expected to have the same EQE response since they have the same configuration. Yet, this is not the case as there is a dip in the EQE of device N2 even though the (1-R) fringes are the same between 700nm and 800nm, which could be due to a parasitic absorption in the n-a-si:H of the top cell, or non-absorption due to a higher amorphous matrix in the bottom i-nc-Si:H layer. The bottom cell of N3 is then supposed to give a better EQE than N1 and N2, which is not the case, implying that the i-nc-Si:H regime could be more amorphous, thus not converting the lower energy photons to charge carriers. An important observation to be made is that the bottom cell response stops at 1100nm, indicating a very poor quality nc-Si:H. This can explain the reduced $V_{oc}$ of all the devices, due to increased recombination in around 2000nm of a-Si:H. This also explains the poor EQE of the top cells since the bottom cell does get completely saturated by the red bias light.
But since one of the three devices is giving an EQE as expected even when all three devices have the same deposition conditions, it could be possible that due to difference in handling of devices could create different shunting effects. This is explored in the next section.

## 5.3. Investigation of mechanical stresses in the foil

Throughout the fabrication of the lab devices on foil, it was observed that the foil which gave flexibility as an advantage to the Powerfoils, was causing difficulty in handling the samples. For every processing step, the sample has to be stretched, which could cause the thin films of the solar cell to crack or break. The deposition of FTO at 500$^o$C is the first step that curls the foil, due to the build-up of thermal stresses. The bent sample brought to TU Delft has to be straightened before the silicon layers are deposited at 200$^o$C. After this step, the samples get bent again. They have to be straightened once more for sputtering of back contact. These steps and the resultant curling is shown in Figure 5.7.

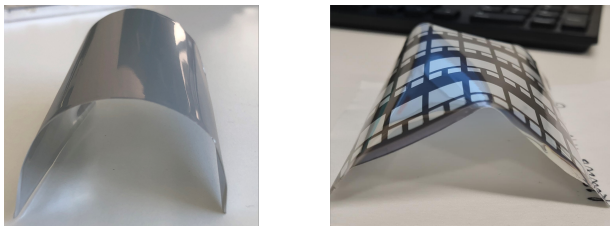


**Figure 5.7:** Foil after FTO deposition (left) and p-i-n-back contact deposition (right)

To minimise the bending in the foils for easier handling, two approaches are tried for fabricating the device:

1. Deposition of a sacrificial layer of nc-Si on the other side of the foil.
2. Attaching the foil to the substrate holder until the measurement step.

Deposition of a sacrificial layer of nc-Si on the other side of the foil

To counter the bending of the foil in the direction of the deposition of the layers of the solar cell, 1 $\mu$m thick layer of nc-Si is deposited on the other side of the foil. After this, two tandems were processed on the foil, one with n-a-Si:H in both sub-cells, and the other with n-nc-SiOx in both subcells (Figure 5.8). 0.16cm$^2$ area back contact of AZO(80nm) +Al(300nm) is sputtered to complete the diode.

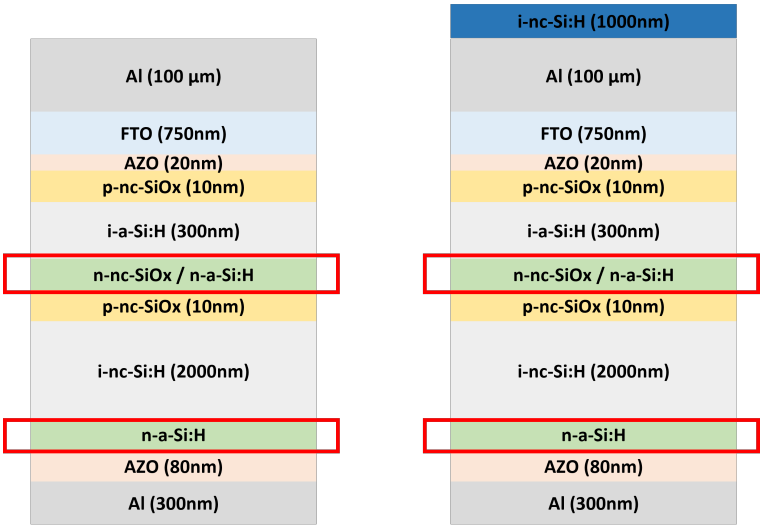



**Figure 5.8:** Device architecture to test effect of sacrificial layers on tandems

The shunt resistance values are plotted in Figure 5.9 for device with n-nc-SiOx in top cell and n-a-Si:H in bottom cell, and in Figure 5.9 for device with n-a-Si in both cells. The first stark observation is in Figure 5.9, with the similarity in the spread of $R_p$ value for both devices with and without the sacrificial layer, meaning that using different n-layers in the devices is creating a leakage path in the device. This is unexpected, as the difference in n-layers in the top and bottom cell should affect the EQE due to the difference in reflectance properties of the n-layers, and the $V_{oc}$ if the reverse electric field generated by the TRJ is different. But since it is also affecting the $R_p$ values, it could be possible that the band-bending due to different n-layers is creating localized leakage currents in the device architecture. To prove this, the device architecture can be modeled in semiconductor simulation software, which is outside the scope of this thesis. In Figure 5.10, both devices with and without the sacrificial layer have more spread towards the right, i.e. $R_p$ values > 1E-1 k$\Omega$.cm$^2$. But, the addition of a sacrificial layer is not giving a significant boost in the shunt resistance values for either device. It could either be that 1$\mu$m sacrificial layer is not thick enough to reduce stresses in the foil, or the shunt is originating due to some other reason.

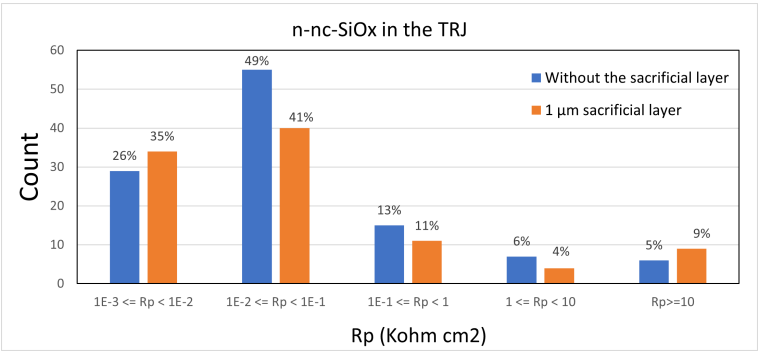



**Figure 5.9:** Spread of $R_p$ values with and without sacrificial layer for device with n-nc-SiOx and n-a-Si:H as n-layers

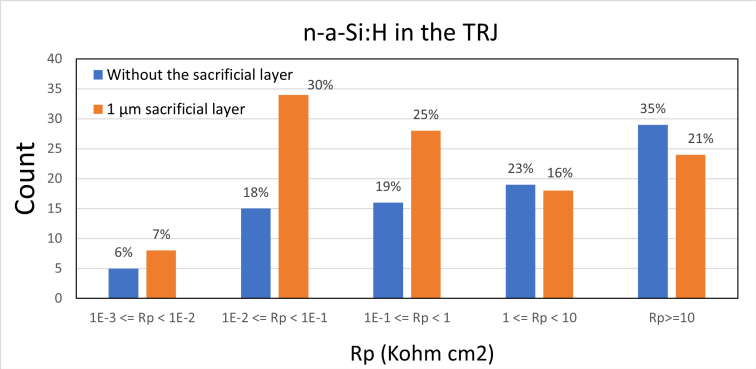



**Figure 5.10:** Spread of $R_p$ values with and without sacrificial layer for device with n-a-Si:H as n-layers

Another method is tried to reduce bending in the foils, which is explained below.

### Attaching the foil to the substrate holder

In this experiment, an attempt is made to attach the Al foil+TCO+AZO sample received from HyET, to the aluminum substrate holder of AMIGO, to provide sturdiness to the foils. This is depicted in Figure 5.11

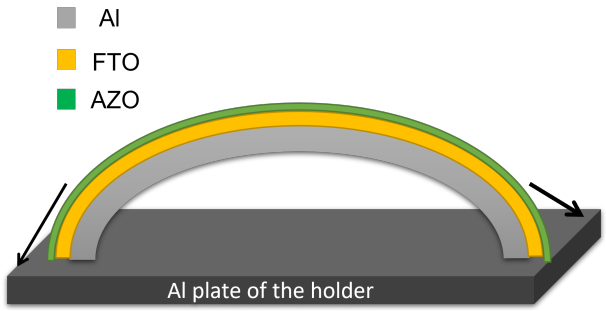



**Figure 5.11:** Schematic of attaching the foil sample to substrate holder

Two devices are made, one with the foil attached to the substrate holder, other without the substrate holder. On these foil samples, only the i-layer is deposited for even faster feedback. The device architecture is shown in Figure 5.12. Small area diodes of 0.16 $cm^2$ are made by evaporating Ag(300nm)+Cr(20nm)+Al(500nm) back contact using appropriate masks. The substrate holder is still kept attached in the evaporation step, so the foil does not undergo any bending or stretching. The shunt resistance values are then measured, during which the sample is still attached to the substrate. From Figure 5.13, it can be seen that the average of shunt resistances is the same and lower than 1k$\Omega$.$cm^2$, irrespective of the presence of the substrate holder. Although it is ot be noted that the devices with the holder has more diodes with $R_p$ greater than 1k$\Omega$.$cm^2$, which suggests some effect of the holder resulting in higher $R_p$ values. The shunt resistance values are still low, which leads us to believe that the origin of the shunts is from the material itself, which cannot be solved by reducing the bending in the foil. Hence, in the next section, we investigate the i-a-Si:H layer itself, to understand the layer properties and their effect on the shunt resistance values.

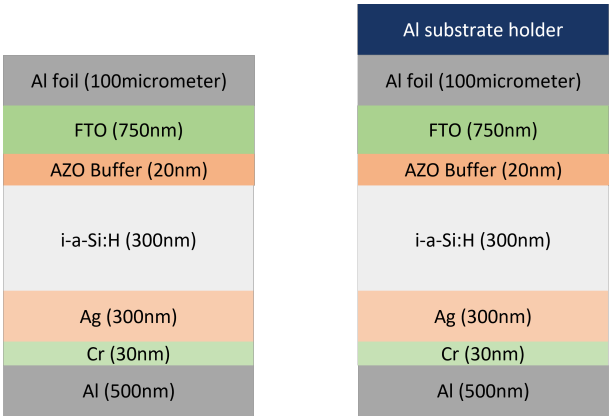



**Figure 5.12:** Device architecture for testing the effect of a substrate holder on device performance

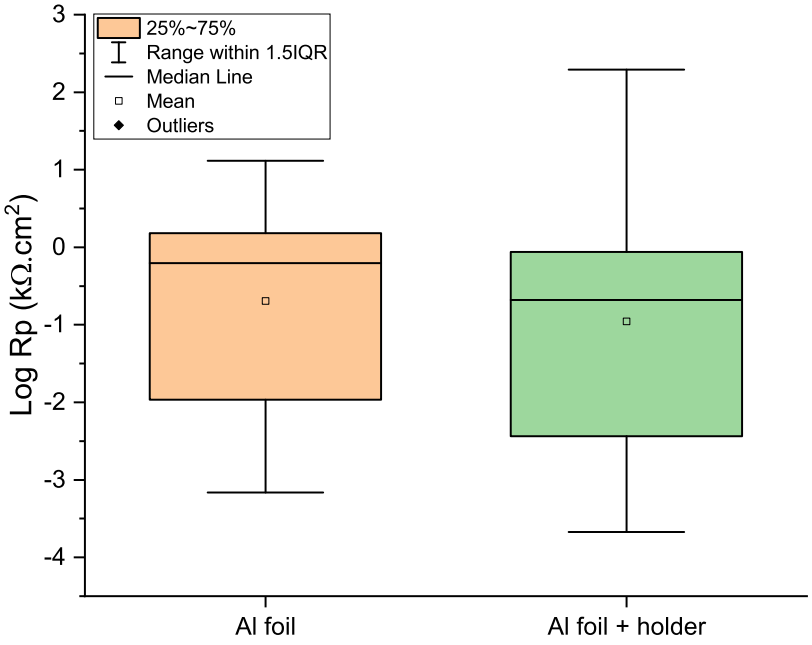



**Figure 5.13:** $R_p$ values of devices without and with the substrate holder

## 5.4. Investigation of i-layer quality

In this section, the deposition of the i-layers is studied in detail, to understand the layer quality and its effect on the shunt resistance of the resultant device. To test this, two devices are fabricated: one with just the i-a-Si:H layer on the Al+FTO+AZO stack from HyET, other with the p-i-n single junction on the Al+FTO+AZO stack from HyET (Figure 5.14). Both devices have only aluminum evaporated at the back to complete the electrical circuit, since AZO and Al cannot be deposited in the same equipment and the masks are not yet designed to be used in both AMIGO and PROVAC at TU Delft.


**Figure 5.14:** Device architecture i vs p-i-n to test silicon layers

On performing copper sulphate ($CuSO_4$) tests on both devices, it was observed that **0.02A/cm**$^2$ current flow was recorded for both devices. SEM analysis is done to visualize this stack at the microscopic level and to observe if the spots of copper (Cu) deposition correspond to any visible shunt sites. From SEM images of the device with just i-a-Si:H (Figure 5.15), very evident cracks can be seen and it is also visible that Cu ions gets deposited and collected in sites where the cracks are formed.

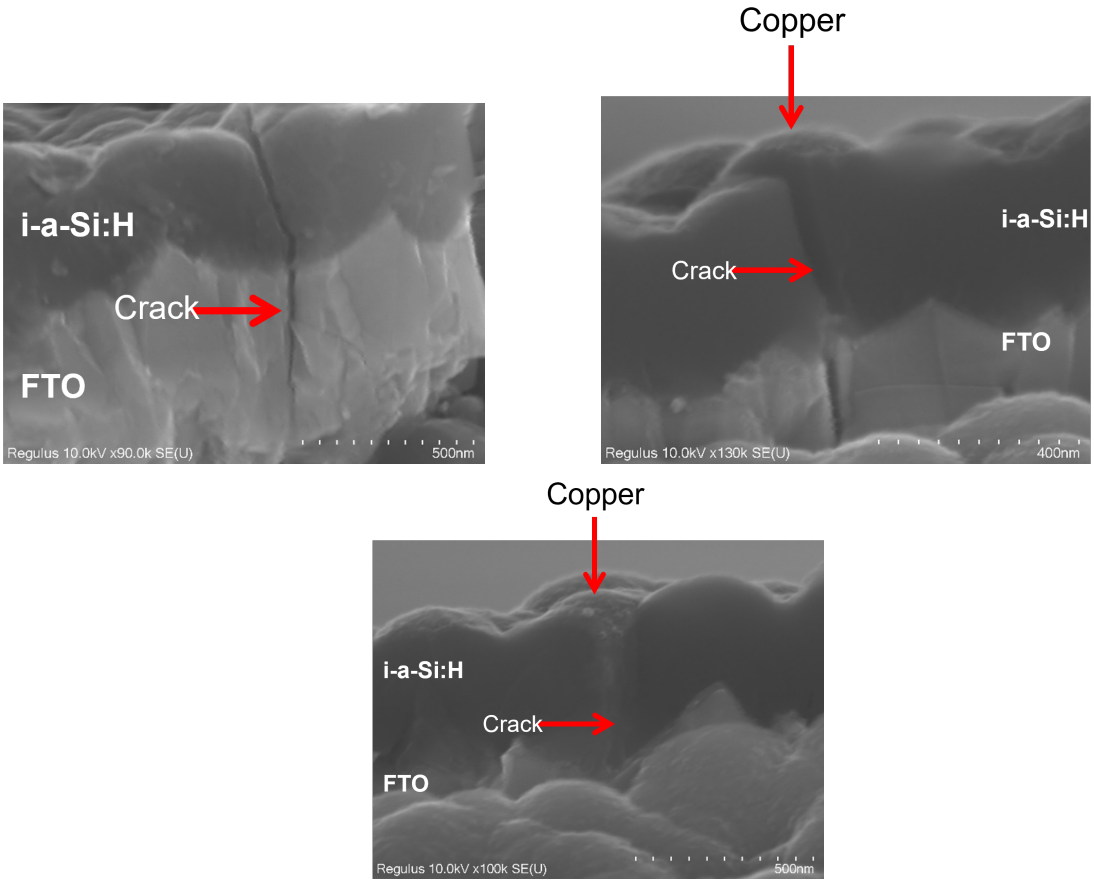



**Figure 5.15:** Cracks and copper depositions seen in device with i-a-Si:H

On looking at the SEM images of the device with the p-i-n stack, it was observed to be more uniform with

lesser cracks, although a few were visible as shown in Figure 5.16. No Cu depositions were seen, but it is possible that the wrong position was scanned. It is interesting to understand whether these cracks are being formed after the a-Si:H layers are being deposited, or whether they are already present in the TCO, which propagates to the subsequent layers as they are deposited.

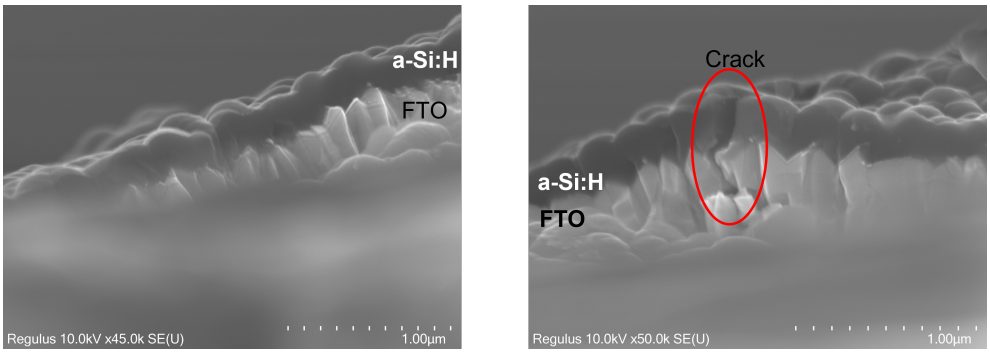



**Figure 5.16:** Cracks seen in device with p-i-n a-Si:H

The shunt resistance values for the diodes of devices are plotted in Figure 5.17. It is visible that the shunt resistance values do not vary much, although there is a very slight improvement in the device with the p-i-n junction. This is not very evident from the Cu depositions, but the SEM images do corroborate a better quality of the p-i-n stack than just the i-layer stack. At this point, it is imperative to question the i-layer stack itself. Since this is an intrinsic layer sandwiched between two metal-like compounds (FTO and Al), the stack behaves as a metal-semiconductor junction instead of a semiconductor-semiconductor junction. So it is worthwhile to question the actual behavior of this device and the expected resistance values. While it can be argued that the FTO can behave as an n-layer (due to electron-rich fluorine in FTO), and Al can behave as a p-layer (due to electron-deficiency as compared to i-a-Si:H), this is still counter-intuitive to the device architecture we actually want to study. And since it is not forming a diode, it cannot be expected to get a diode-like behavior and shunt resistance from this device architecture. It is also important to consider the possibility of Al diffusion into the i-layer. This can happen in evaporation processes at temperatures of 180 °C. This diffusion can make the intrinsic layer into a p-type a-Si:H layer, thus forming an n-p-n device. Nevertheless, if there is no source of leakage current in this architecture, the resistance measured should be equal to the resistance of the intrinsic a-Si:H, which is equal to $10^3$ k$\Omega$.cm$^2$ (log $R_p$ = 3). But since the resistance values are much lower, it is possible that the shunt sites are present somewhere in this stack.

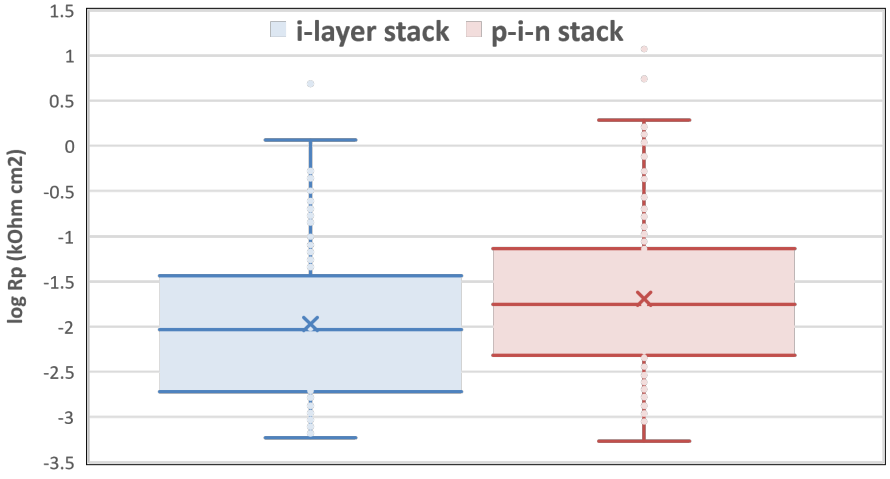



**Figure 5.17:** $R_p$ values for device with i-layer vs p-i-n stack

To test this, i-layers are deposited on ASAHI VU glass, Corning glass and the Al+FTO+AZO stack from HyET. This is done to see the difference of i-layer growth between FTO on ASAHI and FTO on HyET, while the Corning glass is used as a reference for comparing the quality of i-a-Si:H. The device architectures are shown in Figure 5.18. The devices are completed by evaporating a back contact of Ag(300nm) +Cr(20nm) +Al(500nm) to control the diffusion of aluminum into i-a-Si:H.

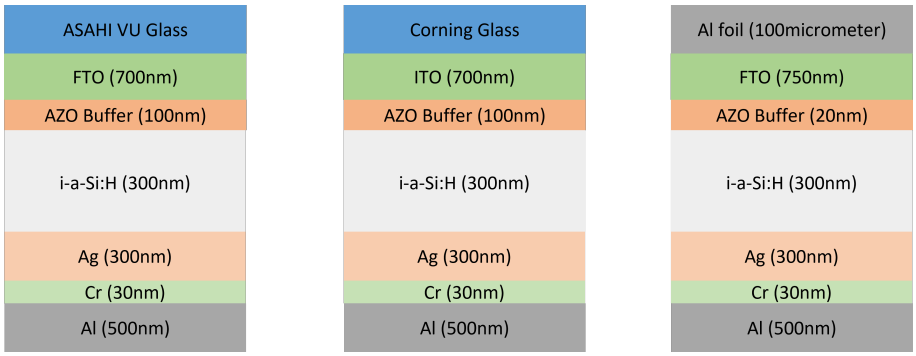



**Figure 5.18:** Device architecture for comparison of different substrates

The shunt resistance values of these devices are plotted in Figure 5.19. It can be seen that the devices made on ASAHI VU glass perform the best, while the device on Corning glass and Al foil have low shunt resistances. Although, the shunt resistance values for devices on glass is still one order lower than expected (Log Rp should be higher than 1), which means that the quality of the i-layer is not up to the mark. During the depositions, silicon dust particles were observed on the glass and foil sample holders, which could be a potential cause for the lowered shunt resistance values. This raises the question of purity of the chambers due to continuous depositions, which should be investigated further (This study is ongoing and the effect of cleaning the chambers on the device properties is being studied). At the same time, the quality of the TCO deposited at HyET is explored in the next section.

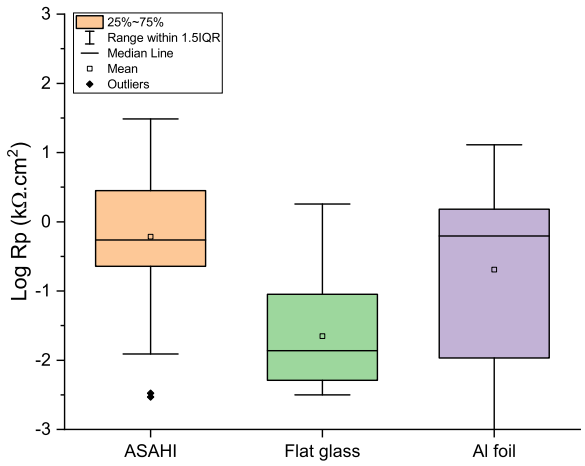
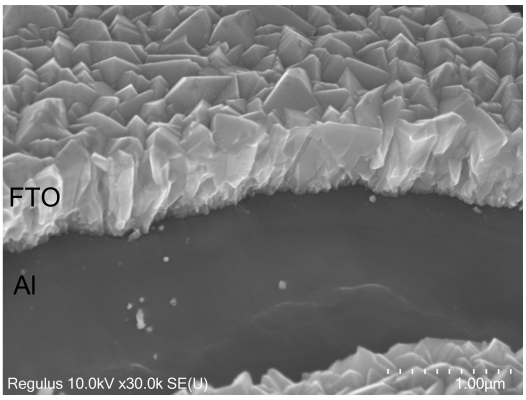


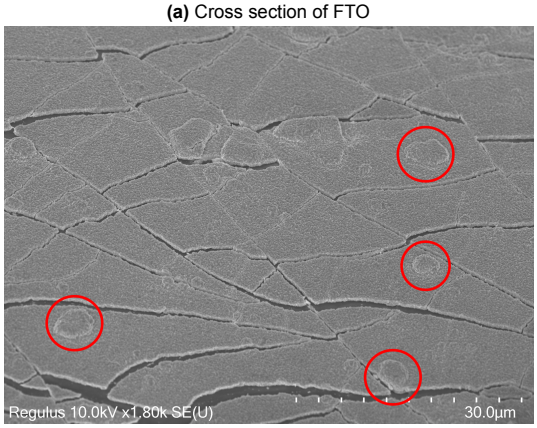

**Figure 5.19:** $R_p$ values of devices on different substrates

## 5.5. Investigation of TCO quality

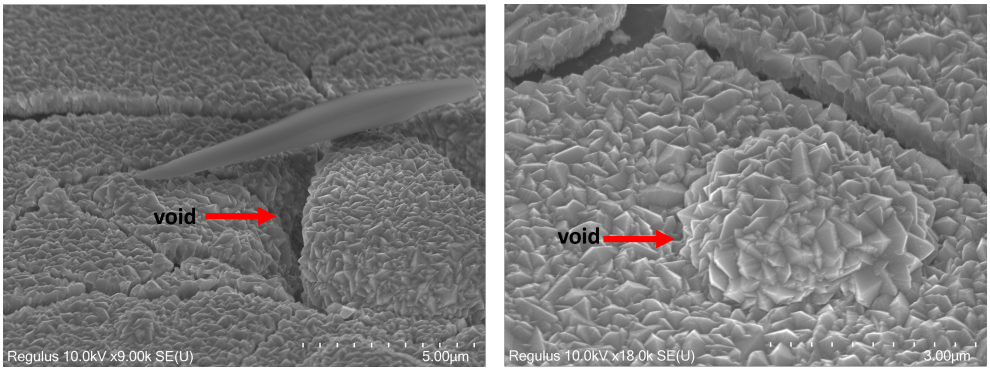
The FTO layer deposited at HyET is done via APCVD, which involves several gas phase reactions for the nucleation and growth of FTO crystals on the aluminum foil. SEM analysis is performed on the stack of 750nm FTO and 20nm AZO deposited on the aluminum foil to analyze the growth of FTO. These are shown in Figures 5.20. Blob-like features are visible in the top view of the FTO (Figures 5.20 b). These are unexpected features, which could be either some gas-phase particles spewed off during the chemical reactions of the FTO deposition or features on the foil on which the FTO is growing. The silicon layers might not grow conformally in the voids of these blobs, leading to shunt paths in the device (Figure 5.20 c).




**(a)** Cross section of FTO




**(b)** Blobs seen on top surface of FTO




**(c)** Voids seen near the blobs

**Figure 5.20:** Top view and cross-section view of FTO grown on Al foil using SEM

The samples in Section 5.5 (i and p-i-n devices) with Cu depositions are studied under a FIB-SEM, to see the individual layers at a higher resolution. These are shown in Figure 5.21 for the device with i-a-Si:H and Figure 5.22 for the device with p-i-n a-Si:H. A very interesting feature is observed in the aluminum foil- the presence of Iron-Silicon alloying elements. These are elements from the aluminum alloy, which stay in the foil due to the rolling process. it undergoes to be made into foils. The FTO is seen to grow conformally over these particles, wheras the growth of silicon layers on this FTO is not as conformal, as the layers around the blob are thinner, which could create voids, causing shunt paths. After performing the $CuSO_4$ test, the Cu ions seem to deposit in places where the alloying elements are present, thus providing a correlation between the alloying elements and the low shunt resistances. It thus becomes imperative to question whether these particles are present of the foil surface, or they appear after the foil is cleaned. This is studied in the next section.

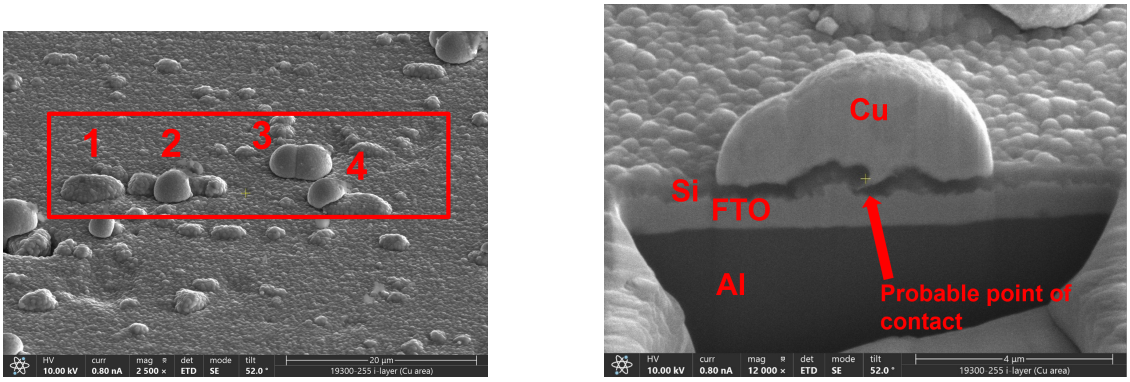



**Figure 5.21:** Cracks and copper depositions seen under FIB-SEM in device with i-a-Si:H

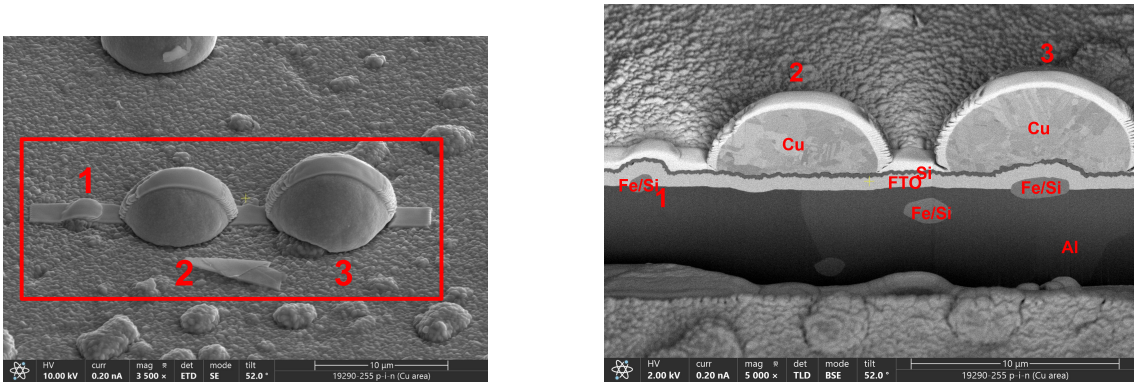


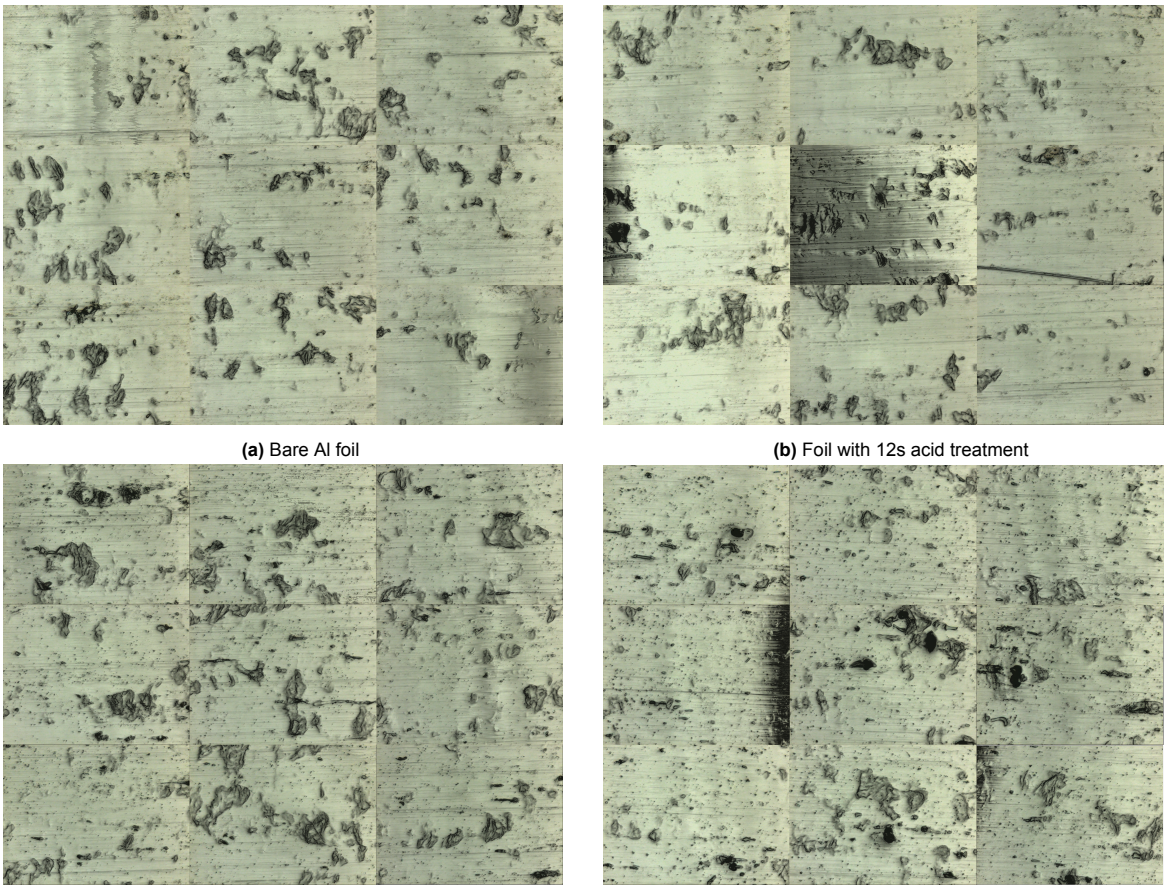

**Figure 5.22:** Cracks and copper depositions seen under FIB-SEM in device with p-i-n a-Si:H

## 5.6. Investigation of the effect of pre-treatment of foils

The incoming aluminum foil from the supplier has a thin layer of grease on it, which must be removed. For this, a wet chemical etching pre-treatment procedure is performed, where the foil is etched with 25% NaOH at 35$^o$C in a 1000L bath. The foil is then rinsed in warm water to remove the insolubles and precipitates from the etching process. The roll is then cleaned with 5% $H_3PO_4$ in a 240L bath [44]. This is the baseline texturing recipe, giving the foil randomized crater-like features for improved light trapping. While the craters are a desired feature on the foil, the etching process is hypothesized to expose possible unwanted features present in the foil, to the surface. This could be a potential shunt path in the device architecture. Different etching procedures are performed to investigate this and their effect on the device is assessed. At the same time, to eliminate the effect of the FTO on shunts, only AZO is used as front TCO. The different pre-treatment procedures are listed in Table 5.1.
These samples are first observed under a confocal microscope, shown in Figure 5.23.
In these images, we can observe the appearance of more features on the surface of the foil, as it is

| Sample | Base Treatment | Acid Treatment | remark |
|---|---|---|---|
| 1 | N/A | N/A | Untreated foil |
| 2 | N/A | 5% $H_3PO_4$, 12s | AT 12s |
| 3 | N/A | 5% $H_3PO_4$, 2min | AT 2mins |
| 4 | 25% NaOH at 35$^o$C, 12s | 5% $H_3PO_4$, 2min | Baseline texturing |

**Table 5.1:** Different texturing procedures on aluminum foil



**(a)** Bare Al foil

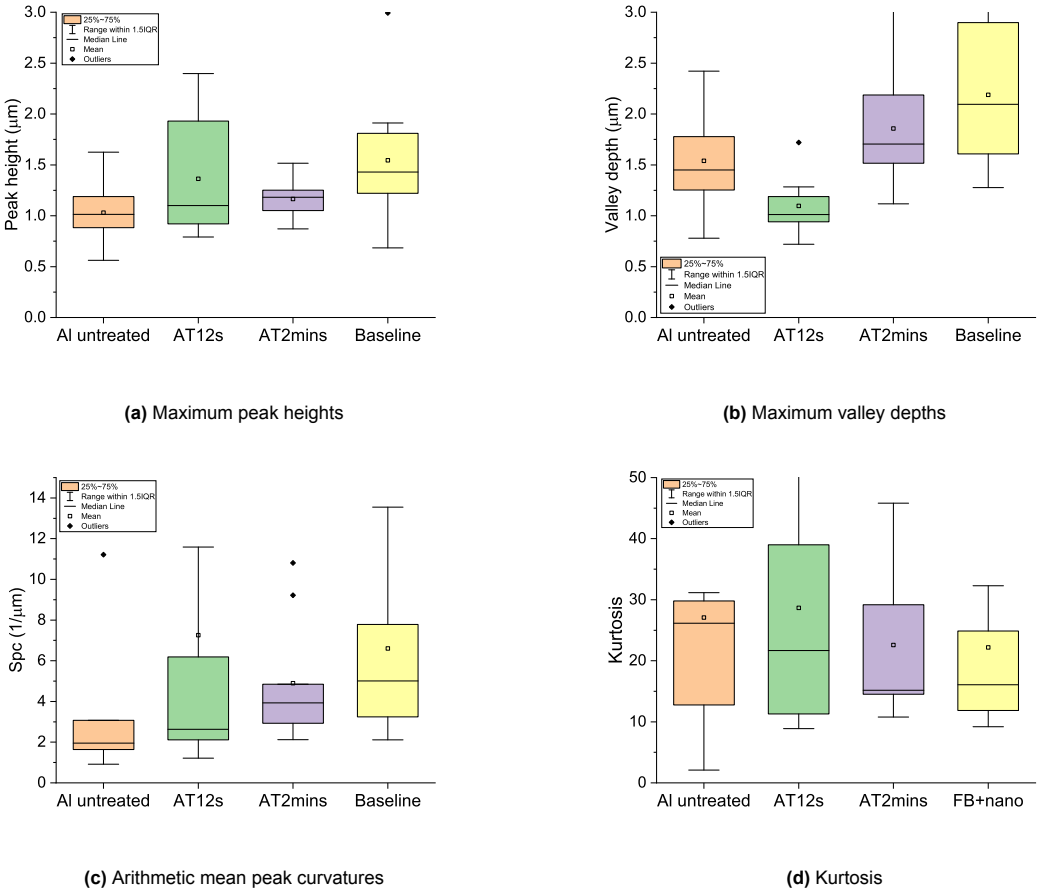
**(b)** Foil with 12s acid treatment

**(c)** Foil with 2mins acid treatment

**(d)** Foil with baseline texturing

**Figure 5.23:** Confocal Microscopy images for different foil treatments, at 150X magnification (9 points shown as a 3$\times$3 matrix)

exposed to more treatment. This is due to selective etching of the existing features, making them more prominent. To quantify these features, the surface roughness parameters are plotted for each foil.
From Figure 5.24 (a), it is observed that the peak heights of the foils is increasing as the treatment process is increased. This is because the randomized craters have more pointed features, thus increasing the peak heights. Peaks of height greater than 1 $\mu$m can already pierce through the subsequent layers, which are less than 500nm thick. From Figure 5.24 (b), the valley depths are also seen to increase, except for when the acid treatment is done for 12 seconds. This is again due to the formation of craters, which increases the depth of the existing features on the foil. From Figure 5.24 (d), we see a decrease in the kurtosis, meaning that the profile is getting lesser peaky due to etching. Yet, these values are much above the desired value of 3, meaning they are still very much spiked.
The parameters observed above indicate the presence of damaging features on the foil. To see their effect on the devices, 250nm i-a-Si is deposited on each foil. The device is completed by depositing AZO-Al as the back contact. The sputtering of back contact is done using masks that define devices of 0.16 cm$^2$ area. These devices are then tested for Cu deposition, and the current for each device is measured and tabulated in Table 5.2
It can be clearly seen that the untreated foil and the foil with very less exposure to acid treatment has




**(a)** Maximum peak heights

**(b)** Maximum valley depths

**(c)** Arithmetic mean peak curvatures

**(d)** Kurtosis

**Figure 5.24:** Surface roughness parameters for different foil treatments

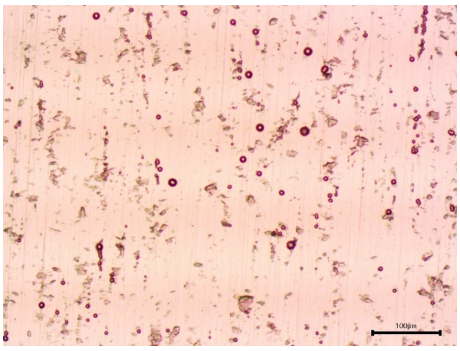
| Sample | Current measured |
|---|---|
| Untreated foil | 0.012 A/cm$^2$ |
| AT 12s | 0.012 A/cm$^2$ |
| AT 2mins | 0.024 A/cm$^2$ |
| Baseline texturing | 0.024 A/cm$^2$ |

**Table 5.2:** Current measurement for copper sulphate tests on each sample

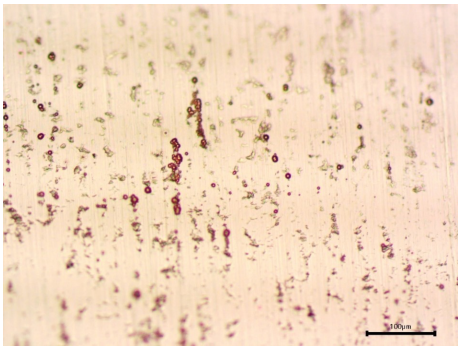
lesser current, i.e. lesser Cu accumulation, while the foils with more exposure to etching have more Cu deposited on it. To visualize this deposition, they are analyzed under a microscope. The microscope images are shown in Figure 5.25. It can be seen from these figures that the more you expose the foil to etching, the more Cu ions are being accumulated on the foil (bright dots), indicating more shunt paths in the foil.

The $R_p$ values of the diodes are plotted in Figure 5.26. From Figure 5.26, it is clear that irrespective of the kind of treatment done on the foil, the devices are still limited by low shunt resistances. It is important to remember here that these are again just i-layers and not diodes, so concluding a shunted device from the $R_p$ values might be incorrect. But at the same time, it is interesting to observe that the untreated foil has diodes with shunt resistance 2 orders higher than the ones with a treatment procedure involved. This corroborates the theory of etching causing the alloying elements to be exposed to the surface. The correlation between Cu deposition and shunt resistance values also need to be studied. The $R_p$ values indicate all shunted devices, while the Cu depositions vary as treatment is increased. This again corroborates a need for standardizing this test.

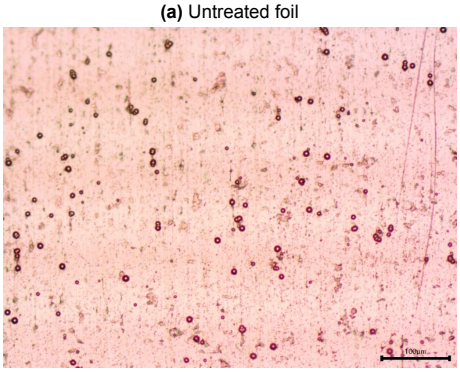
These results make it imperative to study the foil quality itself, which is discussed in the following section.



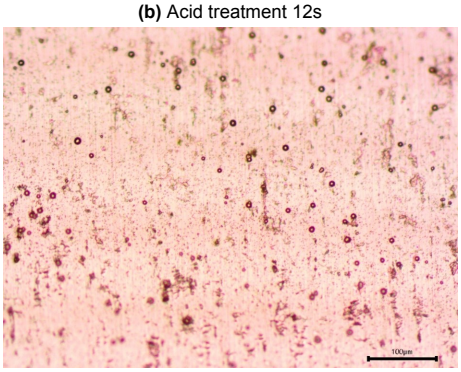
**(a)** Untreated foil



**(b)** Acid treatment 12s



**(c)** Acid treatment 2min



**(d)** Baseline texturing

**Figure 5.25:** Copper depositions for different texturings seen under a microscope

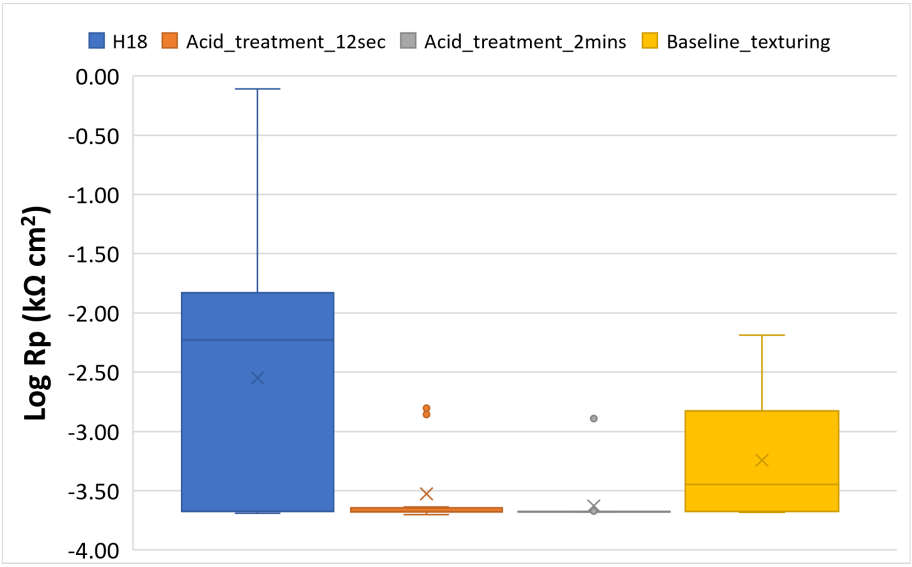
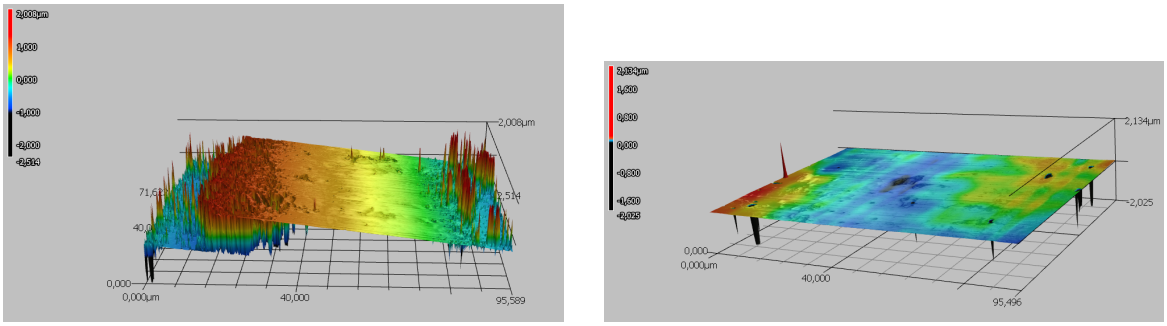



**Figure 5.26:** Variation of shunt resistance values with treatment on the foil

## 5.7. Investigation of foil quality based on hardness

The incoming aluminum foil has inherent material properties and features that seem to affect the device's properties. Hence, this must be investigated in more detail. One important parameter is the hardness of the foil, which represents the heat tempering done on the foil to give it specific mechanical properties. In this experiment, foils of two different hardness are studied: H18 and H19. H18 is work hardened to 100% hardness, while H19 is super work hardened temper, making it more tensile than H18 [45]. It is expected that the harder foil shall be less susceptible to bending and hence shall be less prone to cracks and shunts.



**(a)** Features H18 **(b)** Features H19

**Figure 5.27:** Surface features for different foil hardness

The surface of the foil is visualized using a confocal microscope, as shown in Figure 5.27. It can be seen that the surface of untreated H18 foil has more features than the H19 foil, which have more height as shown in the colour scale. Looking at the arithmetic mean peak curvature and kurtosis values in Figure 5.28, we can see from the $S_{pc}$ values that the H18 foil has much more pointed peaks than H19 foil, while from the kurtosis values, we can see that both are equally badly spiked. This indicates the H18 foil to have more damaging features than the H19 foil.

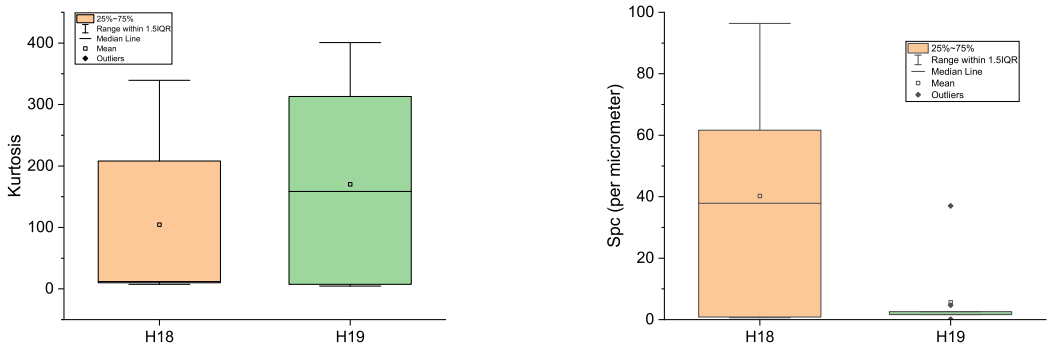
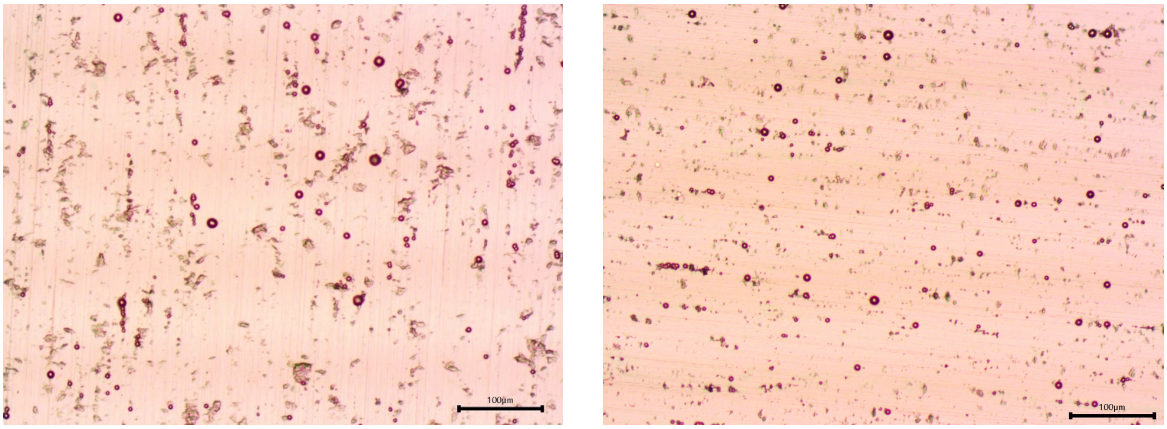



**Figure 5.28:** Surface roughness parameters for different foil hardness- Kurtosis (Left) and Spc (right)

To study the effect of foil hardness on the device, i-layers are deposited on the untreated Al+AZO stack from HyET, and measured for copper deposition and $R_p$ values.
The $CuSO_4$ test is done to analyze the presence of shunts. The current values for both the samples was observed to be **0.012A/cm**$^2$, on an area of 5cm$^2$. This test also bolsters the fact that the hardness of the foil is not altering the device's performance. To visualize the copper depositions, they are analyzed under a microscope. The microscope images are shown in Figure 5.29. It can be seen from these figures that both the foils have similar Cu deposition. An interesting observation is the features of the foil, which are much more prominent in the H18 foil than the H19 foil. Another observation to be noted is that the Cu ions seem to deposit at the spots where the foil features are, providing a correlation between the features of the foil, the alloying elements, and the shunts.
The $R_p$ values are plotted in Figure 5.30. It can be seen that there is not a lot of difference between the shunt resistance values of both devices, suggesting that the hardness of the foil is not really improving the device's performance. An interesting point to note is the current values in the previous texturing experiment and this hardness experiment. The $R_p$ values of all the texturing and hardness samples are in the same range of -2< log $R_p$< 0, while the current values are not the same. It is clear that the Cu depositions cannot directly correlate to the $R_p$ values. An extra measurement step might be causing more shunts in the device. Another possibility is that the Cu ions are larger than the small, localized shunt paths, hence can only detect large shunts, while the $R_p$ measurement gives insights about the presence of the smaller shunts.




**(a)** Copper deposition on H18 foil

**(b)** Copper deposition on H19 foil

**Figure 5.29:** Copper deposition on foils of different hardness

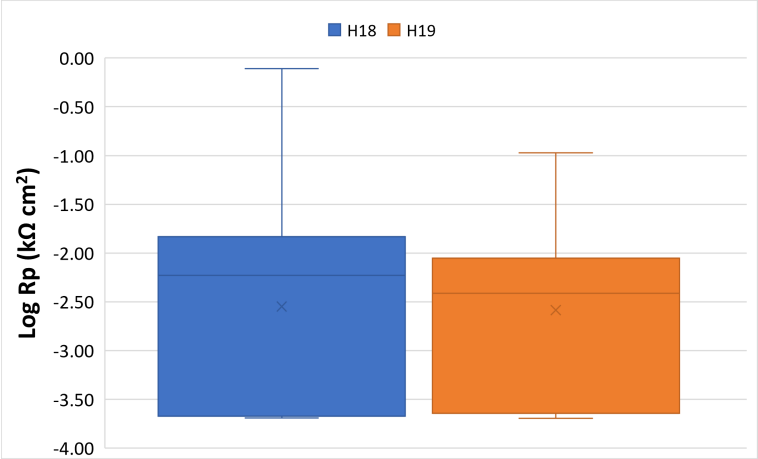



**Figure 5.30:** Shunt resistance values for foils with varying hardness

## 5.8. Key Take-Aways

From the experiments conducted above, the following important conclusions are made:

1. The devices with the same n-layers in the top and bottom cell have the same electrical and optical performance, indicating that the current flow is the same in the transverse direction irrespective of the n-layer being amorphous or nanocrystalline silicon. But, if the n-layers are different, the electrical performance degrades (lower $R_p$) while the optical performance enhances (better EQE). This is a counter-intuitive result, which needs to be studied in more detail, preferably through simulations.
2. Techniques for enhancing the sturdiness of the foils very slightly improve the $R_p$ values, but not enough to prove that the bending and mechanical manipulation of the foil is the main culprit of the shunts.
3. Changing to the hardness of the foil with improved surface morphology also does not have a significant improvement on the $R_p$ values of the devices.
4. The single junction devices in general have much lower $R_p$ values than tandems, indicating that thinner layers are more prone to shunting due to mechanical stresses. This is why even the addition of anti-stress layers is not improving the device's performance.
5. The SEM results showing the presence of cracks in the device cross-section and blob-like features on the FTO surface indicate undesirable features in the aluminum foil.
6. The FIB-SEM results confirm the presence of alloying elements in the foil, on which the TCO is seen to grow conformally, while the thin silicon layers do not fill the voids. If the silicon layers are

very thin (for example just the i-layer or single junction devices), the allowing elements can pierce through the layers, and even the slightest bending and stretching can amplify the cracks caused by these alloying elements.

7. The processing of diodes and subsequent measurement of $R_p$ values seems to reduce the shunt resistance values, which is probably why it does not correspond to the current values seen in the copper sulphate tests. The diode processing and copper sulphate tests need to be made more robust and a better correlation between the two needs to be developed.
8. Treating the foil for creating random craters exposes the alloying elements to the surface, thus damaging the device's performance.

The aluminum foil is thus identified to be a major reason for the low shunt resistances in the devices fabricated in the laboratory, which needs to be addressed with the Al foil supplier.

# 6

# A novel device on Foil

Having narrowed down all the possible causes for low shunt resistances and attempting to solve some of them in the process in Chapter 5, the optimized device architecture on glass from Chapter 4 is implemented on the flexible aluminum foil.

## 6.1. Putting it all together- a novel device on foil

For these experiments, a new Al roll is used. Two different TCO recipes are tested at HyET Solar. The difference between both the TCOs is the web speed of FTO deposition and the flow-rates of the pre-cursor gases. One foil has the baseline webspeed of 0.6m/min while the other has a webspeed of 0.9m/min. The precursor gas flow rates are ramped up at the same proportion as the web speed [46]. In more detailed study, it was also seen that the films at higher webspeed has lesser surface features (Appendix C).
On both these foils, the device architecture shown in Figure 6.1 is fabricated. In the same deposition run, the device is fabricated on ASAHI glass as well, for direct comparison.

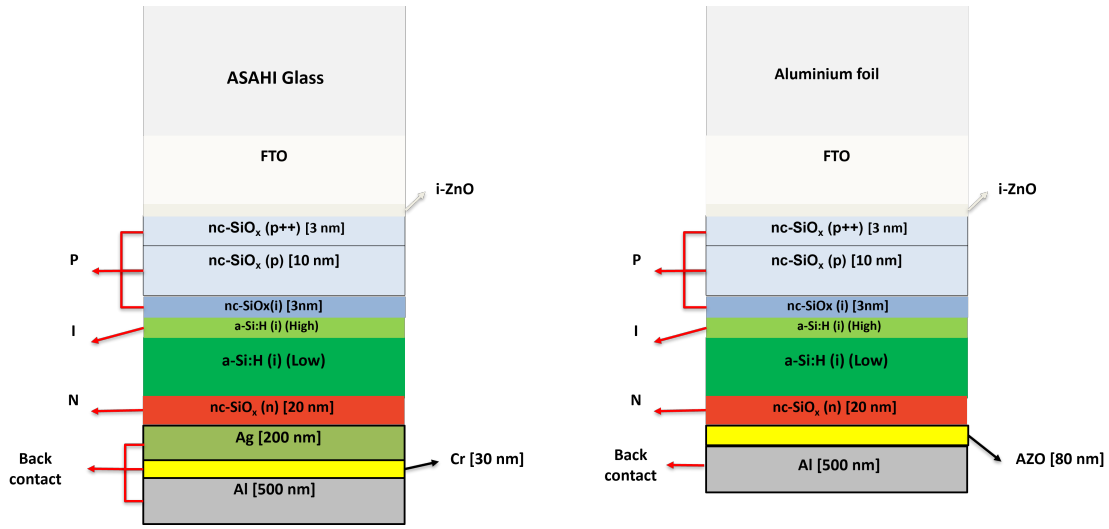



**Figure 6.1:** Device architecture glass versus foil

These devices are fabricated to be characterized as shown in Figure 6.2. It is important to note that the devices on glass do not have a different TCO recipe, these have been deposited only to study the difference in plasma mechanism and deposition between glass and foil.

| TCO 1x | TCO 1.5x | Characterization |
|---|---|---|
| F1 | F2 | CuSO4 tests, SEM |
| F3 | F4 | Small area diodes- Rp |
| | | |
| G1 | G2 | Dark JV, Light JV |

**Figure 6.2:** Characterization of devices on glass and foil

### Copper sulphate tests- Foil

The foil samples with the silicon layers are exposed to copper sulphate to check for copper deposition and the current values are reported in Table 6.1.

| Sample | Current measured |
|---|---|
| TCO 1x | 0.02 A/cm$^2$ |
| TCO 1.5x | 0.007 A/cm$^2$ |

**Table 6.1:** Current measurement for copper sulphate tests on each sample

Through these results we can conclude that the sample with the faster webspeed has lesser shunt sites, hence lesser copper ions are being deposited. This is probably arising from more uniform deposition at higher webspeeds, which could cover all the possible shunt sites in the device.

### Small area diodes- Glass

The results for $R_p$ values of the devices on glass are shown in Figure 6.3

G1- dark JV

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2.0E+5 | 0.471 | 2065.2 | 24.808 | 1.31 | 0.057 | Bad contact | 5.728 | Bad contact | 0.027 | 0.069 | 4.1E+5 | 4.6E+4 | 174.04 | Bad contact |
| 0.818 | 744.4 | 0.963 | 0.11 | 0.093 | 2.36 | 0.042 | 88.28 | 83.147 | 1.343 | 1.79 | 6.6E+5 | 4.5E+4 | 6.5E+4 | 3.6E+5 |

*Rp- kohm.cm2

G1- light JV

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bad contact | 0.372 | 3.077 | 2.42 | 0.189 | 0.057 | Bad contact | 2.13 | 0.064 | 0.025 | 0.071 | 3.1 | 2.62 | 2.417 | Bad contact |
| Bad contact | 2.8 | 0.67 | 0.045 | 0.075 | 1.15 | 0.044 | 2.5 | 3.2 | 1.14 | 1.41 | 2.4 | 2.293 | 2.751 | 2.56 |

G2- dark JV

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.186 | 0.129 | 0.063 | 0.061 | 0.088 | 3.0E+4 | Bad contact | 0.126 | 883.4 | 683.4 | 1.8E+5 | 603.76 | 2.4E+3 | 6.43 | Bad contact |
| 3.7 | 0.237 | 0.028 | 0.39 | 866.63 | 0.516 | 0.075 | 0.46 | 0.566 | 5.76 | 2.31E+4 | 2.25E+6 | 105.3 | 5.42E+4 | 28.85 |

G2- light JV

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.258 | 0.354 | 0.093 | 0.073 | 0.098 | 3.87 | Bad contact | 0.149 | 4.07 | 4.331 | 4.41 | 4.36 | 4.04 | 2.535 | Bad contact |
| 0.252 | 2.59 | 0.106 | 0.403 | 3.203 | 0.384 | 0.079 | 0.404 | 0.546 | 2.233 | 4.287 | 4.15 | 2.89 | 3.96 | 3.03 |

**Figure 6.3:** $R_p$ values of devices on glass (k$\Omega$.cm$^2$)

It is interesting to observe that only the left side of the device has lower $R_p$ values (denoted by yellow for 0.1 k$\Omega$.cm$^2$ < $R_p$ < 1k$\Omega$.cm$^2$ and red for $R_p$ < 0.1 k$\Omega$.cm$^2$), while the right side has all dots with

higher $R_p$ values (green for $R_p$ > 1 kΩohm.cm$^2$). This is a very strong indication of a measurement error in the J-V setup. The setup has 30 probes that automatically contact the 30 dots on the device to measure the electrical properties. It seems to be a case of either the probes piercing the contacts or that the probes are not aligned to contact the dots correctly. In either case, the circuit is getting shorted, resulting in a reduction in the $R_p$ values. But, since we also see one half of the device with good performance, we can conclusively say that the deposited layers are performing well as expected, with good diode properties. The measurement setup needs to be studied in more detail, which is out of the scope of this thesis.

### Small area diodes- Foil

The $R_p$ values of each small area diode on the foil is shown in Figures 6.4 and 6.5. The color scheme is green for $R_p$ > 1 kΩohm.cm$^2$, yellow for 0.1 kΩ.cm$^2$ < $R_p$ < 1kΩ.cm$^2$ and red for $R_p$ < 0.1 kΩ.cm$^2$.

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 4.18E-03 | 1.28E-02 | 1.08E-02 | 3.32E-03 | 5.67E-02 | 9.22E-04 | 9.73E-04 | 1.16E-03 | 2.08E-03 | 4.07E-03 | 1.45E-03 | 3.58E-03 |
| 2.36E-03 | 2.54E-03 | 4.41E-03 | 2.90E-03 | 2.72E-03 | 4.73E-03 | 4.88E-03 | 2.28E-03 | 1.73E-03 | 2.25E-03 | 1.05E-03 | 1.42E-03 |
| 1.46E-02 | 7.06E-03 | 5.38E-03 | 5.00E-03 | 2.43E-02 | 6.75E-03 | 6.81E-03 | 2.57E-03 | 1.07E-03 | 8.79E-04 | 1.35E-03 | 1.61E-03 |
| 1.65E-03 | 3.73E-03 | 1.91E-03 | 2.10E-03 | 1.31E-03 | 1.19E-03 | 9.60E-02 | 5.56E-03 | 3.08E-03 | 6.14E-02 | 3.05E-03 | 9.14E-03 |
| 2.54E-03 | 2.97E+00 | 3.73E-03 | 2.02E-03 | 2.17E-03 | 2.97E-03 | 4.91E-03 | 3.25E-03 | 1.71E-03 | 2.01E-03 | 3.45E-03 | 5.43E-03 |
| 5.42E-03 | 3.18E-01 | 3.89E-03 | 5.35E-03 | 5.71E-02 | 4.82E-03 | 1.94E-03 | 6.89E-03 | 5.62E-04 | 2.08E-01 | 1.80E-03 | 7.86E-04 |
| 9.33E-04 | 1.84E-03 | 5.49E-03 | 3.71E-03 | 2.89E-03 | 5.32E-03 | 1.46E-03 | 2.12E-03 | 1.74E-03 | 4.20E-03 | 1.22E-03 | 7.57E-03 |
| 8.71E-04 | 2.29E-04 | 8.85E-04 | 9.89E-04 | 1.35E-03 | 5.04E-03 | 6.33E-03 | 7.73E-01 | 2.19E-02 | 5.93E-03 | 4.53E-03 | 2.34E-03 |
| 1.40E-03 | 1.06E-03 | 1.82E-03 | 1.95E-03 | 1.27E-02 | 1.82E-02 | 3.11E-01 | 9.54E-01 | 2.24E-04 | 1.31E-02 | 1.92E-03 | 1.87E-03 |
| 2.03E-03 | 7.76E-03 | 2.83E-03 | 3.99E-03 | 3.27E-03 | 1.01E-03 | 9.36E-04 | 2.20E-03 | 3.97E-02 | 5.47E-04 | 5.41E-03 | 8.10E-04 |

**Figure 6.4:** $R_p$ values (kΩ.cm$^2$) of diodes on foil with FTO webspeed 0.6m/min

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6.73E-03 | 1.53E+00 | 3.24E-02 | 1.01E+01 | 4.02E-02 | 2.04E-01 | 1.74E-01 | 1.56E+00 | 9.14E-03 | 3.10E-02 | 4.39E-02 | 4.72E-02 | 4.86E-02 | 2.35E-03 |
| 2.43E-03 | 7.73E-03 | 1.53E-01 | 2.34E+00 | 4.10E-02 | 9.38E-03 | 7.53E-02 | 5.14E-02 | 1.97E-03 | 4.54E-02 | 4.70E+00 | 1.54E+00 | 4.20E-01 | 1.61E-02 |
| 6.40E-02 | 1.28E-02 | 6.86E-02 | 2.78E-01 | 7.04E-02 | 1.38E-02 | 4.99E-02 | 5.42E-02 | 9.73E-03 | 5.51E-01 | 2.26E-01 | 8.57E-01 | 4.61E-01 | 6.43E-03 |
| 5.16E-02 | 2.07E-03 | 6.23E-03 | 2.59E-03 | 2.12E-03 | 3.01E-02 | 2.39E-01 | 4.10E+00 | 1.28E-02 | 6.39E-03 | 2.93E-03 | 6.60E-03 | 2.94E-02 | 5.09E-02 |
| 1.76E-02 | 7.09E-02 | | | 7.05E-04 | 8.35E-04 | 9.41E-04 | 1.24E-03 | 1.63E-03 | 1.65E-03 | 1.20E-03 | 2.01E-03 | 8.27E-01 | 1.82E-03 |
| 3.34E+00 | 2.12E-03 | | | | | | | | | | 2.47E-03 | 1.90E-01 | 4.74E-02 |
| 2.29E-03 | 1.75E-03 | | | | | | | | | | 1.00E-02 | 5.55E-03 | 1.82E-02 |
| 2.09E-03 | 4.02E-03 | | | | | | | | | | 7.78E-02 | 6.35E-03 | 1.18E+00 |
| 2.92E-03 | 5.25E-03 | | | | | 1.07E-01 | 2.62E-02 | 9.41E-02 | 7.92E-03 | | | 1.62E-01 | 5.85E-02 |
| 2.63E-03 | 2.46E-03 | | | | | 4.95E-02 | 5.46E-03 | 5.19E-03 | 5.80E-03 | | | | |
| 4.09E-03 | 1.38E-03 | | | 4.00E-01 | 3.57E-03 | 1.50E-01 | 1.12E-01 | 1.74E+00 | 2.06E+00 | 2.42E-01 | 2.29E-03 | 2.22E-03 | 2.79E-02 |
| 2.77E-04 | 1.15E-02 | 1.06E-03 | 2.30E-03 | 7.08E-01 | 6.89E-01 | 3.41E-02 | 7.04E-02 | 2.58E-02 | 4.13E-02 | 1.02E-01 | 1.49E-02 | 1.25E-03 | 1.33E-03 |
| 3.20E-03 | 5.11E-02 | 3.53E-03 | 4.15E-03 | 1.71E-03 | 4.27E-01 | 9.19E-02 | 1.07E+00 | 2.01E-02 | 4.60E-01 | 8.64E-03 | 1.69E-01 | 1.32E-02 | 2.22E-02 |
| 4.70E-03 | 1.33E-02 | 3.23E-01 | 3.05E-02 | 4.94E-03 | 4.30E-03 | 3.79E-03 | 7.92E-03 | 2.84E-03 | 2.16E-03 | 1.77E-02 | 4.44E-03 | 3.07E-02 | 2.04E-04 |

**Figure 6.5:** $R_p$ values (kΩ.cm$^2$) of diodes on foil with FTO web speed 0.9m/min (grey cells represent bad contact)

It is clearly visible that both devices have a very poor diode behavior, although the device with the faster TCO web speed has slightly more dots with a diode-like behavior than the device with the baseline TCO recipe. This can be attributed to a more uniform TCO surface which was observed through SEM (Appendix). It is again noted that the $R_p$ of the devices are almost the same, while the copper deposition seen from Table 6.1 is very different which was indicating lesser shunts in the device with faster FTO deposition. This again indicates that the measurement technique for $R_p$ is not the most reliable and might be wrongfully indicating the presence of shunts in the device. There is also a stark difference between the device performance on the glass substrate and foil substrate. To inspect the cause behind this difference further, the plasma conditions during the deposition were studied in further detail.
Figure 6.6 shows the differences in reflected power and DC bias voltage during the i-layer deposition in the i-layer chamber of the PECVD tool. It is clearly visible from Figure 6.6 that the plasma conditions during high band-gap a-Si:H is not the same for glass and foil deposition. This difference was also visible by the very powdery samples after the layers were deposited (shown in Figure 6.7). This powder

| | High BG aSi-Glass | High BG aSi-Foil |
|---|---|---|
| DC bias | 2-2.8 V | 0.4-2 V |
| Reflected power | 1 – 2.5 W | 0.8 – 1 W |

| | Low BG aSi-Glass | Low BG aSi-Foil |
|---|---|---|
| DC bias | 4 V | 4V |
| Reflected power | 0.3 W | 0.3 W |

**Figure 6.6:** Plasma parameters during i-a-Si:H deposition

is of a-Si:H, indicating a dusty regime deposition of high band-gap a-Si:H. High band-gap a-Si:H is very sensitive to the pressure it is deposited at, and the history of the conditions of the chamber. While the deposition seems to be stable on an insulator glass substrate, it does not seem to be the case on a conductive aluminum substrate. It is possible that at 10mbar pressure on a conductive aluminum substrate, the a-Si:H is being deposited as dust in the chamber, which is being accumulated on the substrate. This dust is suspected to be the cause for poor device performance on the foil.

**Figure 6.7:** i-a-Si powder seen on aluminum holders with the foil samples

## 6.2. Key Take-Aways

From the experiments conducted above, the following important conclusions are made:

1. The TCO deposited at higher webspeed seems to decrease the shunting in the device, visible from both the copper sulphate tests and the $R_p$ values of the diodes.
2. The plasma conditions for deposition of high band-gap i-a-Si:H is not the same during deposition on glass and deposition on foil. This could be due to the effect of the conductive Al substrate. This could also be the case for the p-layers, which are the most sensitive to deposition parameters.
3. The deposition chambers are getting increasingly dusty after every deposition, especially when the Al foil is used as a substrate, reducing the yield of the devices fabricated. The conductive Al substrate is visually seen to attract more dust on the sample than the glass substrate, causing potential shunt paths in the device architecture.

The generation and accumulation of silicon dust in AMIGO is identified to be another major source of shunts in the devices fabricated.

# 7

# Conclusions and Future Outlook

This chapter concludes the findings of this thesis in Section 7.1, by answering the research questions proposed in Chapter 1. Then, recommendations for further studies is provided in Section 7.2.

## 7.1. Answering the research questions

The primary goals of this thesis were to optimize single junction a-Si:H devices on glass, to improve the optical and electrical performance, and to demonstrate a proof-of-concept of single junction and tandem a-Si:H based solar cells on flexible aluminum substrate. For this purpose, six research questions were developed; the first three to optimize devices on glass and the last three to develop single junction and tandem a-Si:H based solar cells on flexible aluminum substrate. These are all answered below:

### 7.1.1. Optimization and improvement- Devices on Glass

1. **How is the device performance affected by the introduction of a-Si:H of different material properties?**

   a-Si:H is deposited at high pressure and high power, with the aim to increase $V_{oc}$ of the device by increasing band-gap of the a-Si:H. From the experiments conducted in Section 4.2.1, the desired $V_{oc}$ boost was not seen, which could be possible due to numerous reasons. One reason could be the high band-gap itself. The thickness of this layer is varied from 0nm to 60nm in steps. The deposition of these very thin layers (especially from 0nm to 10nm) is very sensitive to the plasma and chamber conditions. It could be possible that in the few seconds needed to deposit these layers, the desired plasma conditions are not reached due to start-up inertia. It could also be possible that if the layers are deposited at the optimum process conditions, the pressure regime is creating more nano-voids in the matrix, thus decreasing the $V_{oc}$. Another possibility is that the p-layers are causing more recombination due to improper deposition, thus reducing the $V_{oc}$. Looking at all other electrical parameters, there is no improvement in the $J_{sc}$ of the devices, which is expected and seen clearly in the EQE's of each device. Due to sample-to-sample variation in deposition of each layer, losses in the p-layers are seen to be compensated by the variation in the red response. The FF and efficiency follow the same trend as the $V_{oc}$ for the same reason. The $R_s$ and $R_p$ values also do not follow any particular trend, bolstering a sample-to-sample variation in the depositions. But, comparing the results of this experiment to the 300nm layers of high band-gap and low band-gap a-Si:H, it is seen that the electrical and optical parameters are almost similar, thus concluding that we can make thinner layers and retain the electrical and optical properties of the device by reducing raw material usage by 23%.

   The experiment of Section 4.2.2 with increasing the absorber layer also corroborates the fact that the difference between 230nm thickness and 300nm thickness is improving the device performance by less than 10%. This improvement can be tried to achieve at 230nm, by improving light management and charge carrier collection.
2. **How much is the device performance degrading when exposed to light soaking?**

LID experiments were performed to understand if the high band-gap a-Si:H degrades more due to presence of more divacancies and nano-voids or degrades less due to the dangling bonds being passivated by hydrogen. But from the results of the LID experiment, a permanent degradation of the devices was seen apart from the metastable reversible defects discovered by Staebler-Wronski. Hence the SWE of high band-gap a-Si:H is not clearly understood. The permanent degradation can be attributed to the degradation of the metal back contacts which have a fast rate of evaporation. This is visible in the EQE of the devices, where the red response is seen to degrade as severely as the blue response. This is probably why the degradation does not slow down after 10 hours, as it is expected to. The SWE degradation is temporary, which is seen by approximately 80% recovery of the electrical and optical parameters of the devices. The device with 30nm high band-gap a-Si:H is seen to stabilize at the highest value of the electrical parameters and recovers the most, while it degrades the most and does not recover optically.

3. **Can the device performance be enhanced through improving the specctral utilization and collection of charge carriers?**

   As seen from experiments in Section 4.2.2, the device performance at 230nm is only about 10% lesser than the device performance at 300nm. To increase the charge carrier collection, a triple n-layer is used. The n-layers are graded in a way that the i-n interface is more uniform and has less defects, and the ohmic contact with the metal is improved. The results from the experiments in Section 4.4.1 shows an improvement in the charge carrier collection , i.e. $V_{oc}$ of the devices with the triple n-layer, although this induces parasitic absorption thus decreasing the $J_{sc}$. Yet, the devices with 300nm absorber layer thickness perform slightly better than the devices with 230nm absorber layer thickness.

   To improve the spectral utilization, a back-reflector is used after the n-layer in the device. i-ZnO is used as a back-reflector TCO, which has a high band-gap hence lower parasitic absorption, and a refractive index which facilitates maximum reflection from the surface. But, the desired EQE boost was not achieved. This is mainly because the red light reflected back by i-ZnO is not absorbed in the i-layer more than it already is, due to the band-gap of the absorber layer limiting the absorption of the red light. The i-ZnO back reflector also reduces the electrical performance since i-ZnO and metal back contacts are deposited in two different equipments using different masks of different sizes. This causes a misalignment of the layers, resulting in additional lateral current flow, thus increasing the series resistance of the device. This reduces the electrical performance of the device, while not improving the spectral red respone. Use of a back-reflector in single junction a-Si:H devices will thus not serve the purpose of boosting the red response.

### 7.1.2. Proof of concept- Devices on Foil

1. **What are the possible casues of low shunt resistance in devices on foil?**

   A structured root-cause analysis was performed to identify the major cultprits for the lowered shunt resistances for devices on foil. Starting with the suspicion of leaky n-layers in a tandem device due to a more conductive n-nc-SiOx, it was observed that having two different n-layers in the top and bottom cell reduced the shunt resistance values. The reason is still unclear, as this is an unexpected trend to occur. Then, the i-a-Si:H layer is studied in deep detail. The tests from i-layer depositions show the presence of numerous cracks in the device, which can be a path for the leakage currents. An even deeper analysis into the TCO layers shows blob-like features on the TCO surface, which was found to be alloying elements (Fe-Si) present in the foil. These alloying elements are exposed to the surface when the foil is etched to create craters for improved light scattering.

   A few more important findings are noticed from these tests. First is the inconsistency between the copper sulphate tests and $R_p$ measurement method to identify shunts in the device. It seems that while the copper depositions vary according to the actual presence of shunt paths in the device, this is not reflected in the $R_p$ values, which are in the same range even if the copper deposited is lesser. This indicates that the diode fabrication and subsequent $R_p$ measurement is inducing more shunts in the device than actually present. Second observation is the drastic reduction in the shunt resistance values as the total thickness of the device decreases. The tandems have at least 2 orders higher $R_p$ values than the single junction devices and the i-layers. This means that

thinner layers are more prone to shunting on a flexible foil, which undergoes a lot of bending and stretching.

2. **Can the foils be processed with minimal mechanical manipulation?**

   The flexibility of the foils has made manually handling the samples very tricky. For every fabrication step starting from TCO deposition to the measurement, the sample undergoes multiple bending and stretching due to release of thermal stress. To decrease the bending, the foil was mechanically manipulated. One way was to deposit a 1$\mu$m thick nc-Si layer on the reverse side of the foil, and the other way was to attach the foil to the substrate holder throughout the depositions until the measurement step. While this did make handling the foils a bit easier, this did not help with improving the $R_p$ values. Only a very slight increase in the $R_p$ values was observed.

3. **Can the best-performing device-on-glass architecture of this thesis be duplicated on the foil?**

   The stack of triple p-layer, 20nm high band-gap a-Si:H, 210nm low band-gap a-Si:H and single n-layer is deposited on the Al+TCO+FTO stack from HyET Solar. After the silicon depositions, it was observed that the sample holders having the Al foil came out very dusty, which was not seen on the sample holders having the glass substrate. This was identified to arise from the high-pressure deposition of high band-gap a-Si:H, which deposited a more dusty silicon. And since the aluminum substrate is more conductive than glass, it appears to change the plasma conditions in the chamber and attracts the silicon dust onto the substrate, thus reducing the quality of the devices.

## 7.2. Recommendations for future research

The experiments conducted in the last nine months are far from conclusive. This leaves room for continued research to improve the performance of devices on both glass and aluminum substrates.

For understanding the contribution of high band-gap a-Si:H better, it is important to understand the deposition parameters of this particular layer; both individually and in combination with low band-gap a-Si:H. Thicker high band-gap a-Si:H layers can be tested (100nm to 300nm series), combined with low band-gap a-Si:H (200nm to 0nm series). This will give more insights into the possibility of $V_{oc}$ gain by the use of high band-gap a-Si:H.
To understand the degradation of metal back contacts, a series of experiments can be conducted with varying evaporation rates, to see which rate has the best and the worst light-induced degradation.
To improve the charge carrier collection using triple n-layers, a series of experiments can be conducted with increasing thickness of the window n-layer and variation in the doping of the window and contact n-layer. This will help to determine the optimum triple n-layer to obtain the best red response and charge carrier collection.
Since using a back-reflector will not improve the red response as required, the spectral response can be tried to improve by use of an anti-reflection coating at the front, to boost the blue response of the devices.

For the devices on foil, it is best to shift back to the basics and make simple layers. This is to be done until the shunt problem is solved, after which the triple p-layer, high band-gap a-Si:H layer, and triple n-layer can be tested on the foil for attaining record performances. It is becoming more clear that the deposition chamber needs to be in pristine condition before making devices, to maintain efficiency and yield. Hence, it is suggested to clean the equipment before every deposition.
The n-layer combinations for tandems can be repeated again, for statistical purposes. If the same trend repeats, this particular stack can be modeled on the semiconductor simulation softwares, to understand the mechanism of charge collection throughout the device.
To make the copper sulphate tests more robust, the test can be performed on i-a-Si:H, single junction and tandem cells deposited on glass. This will be a good standard to compare the copper depositions on the foil to.
To make the $R_p$ measurements on diodes more robust, the device architecture can be first simulated to get a good reference. Then, the measurement technique itself can be improved by improvising the diode fabrication. One possibility is to develop the silver epoxy strategy, where the sample is cured to a metal plate with conductive silver epoxy paste, thus giving more sturdiness and improved charge carrier

collection and measurement of the devices. Also, the WACOM measurement setup and software for measuring the parameters of the devices on the foil can be improved. The $R_p$ values were noticed to be inaccurately calculated by the software, which needs to be corrected.
To reduce dependency on the equipments at HyET for post processing, a new lab-route can be developed to get faster results and feedback. First, a new holder can be designed that can hold the sample in both the PECVD tool and evaporation tool, thus reducing the manual handling of the foils. Second, FTO sputtering can be explored internally, to eliminate the FTO deposition at HyET as a cause for low shunt resistances, and reduce dependency on the production tool for R&D purposes. More brainstorming needs to be done on the possibilities of lamination and encapsulation at TU Delft.

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# A

# JV Curves

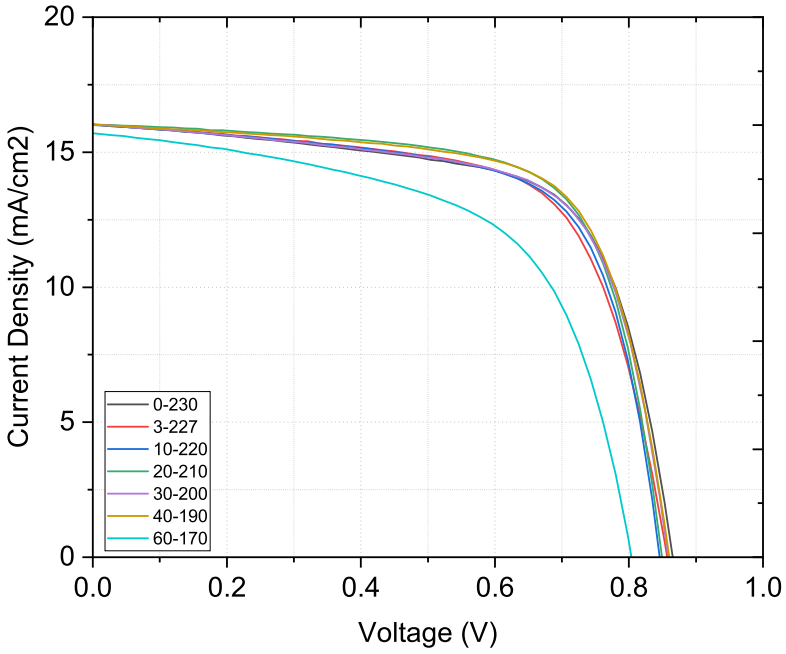



**Figure A.1:** JV curves of devices Experiment 4.1.1

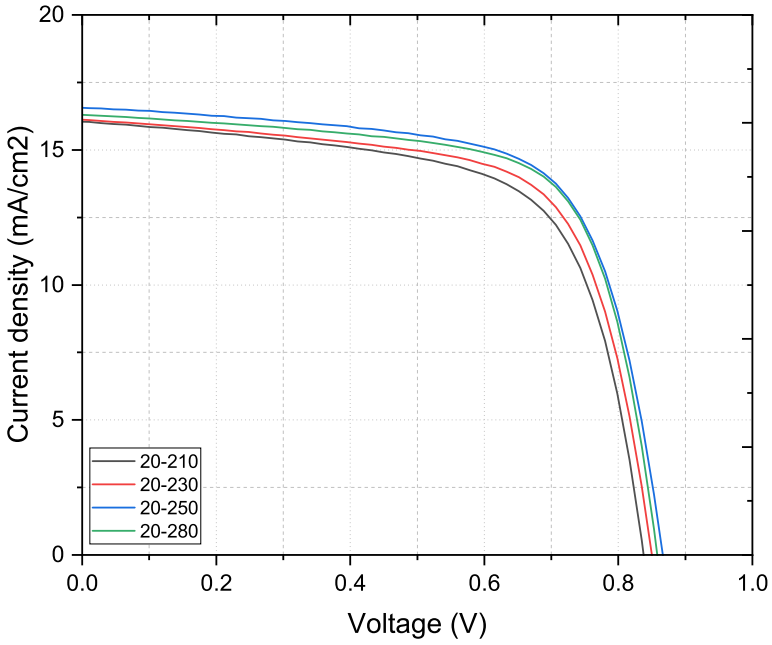



**Figure A.2:** JV curves of devices Experiment 4.1.2

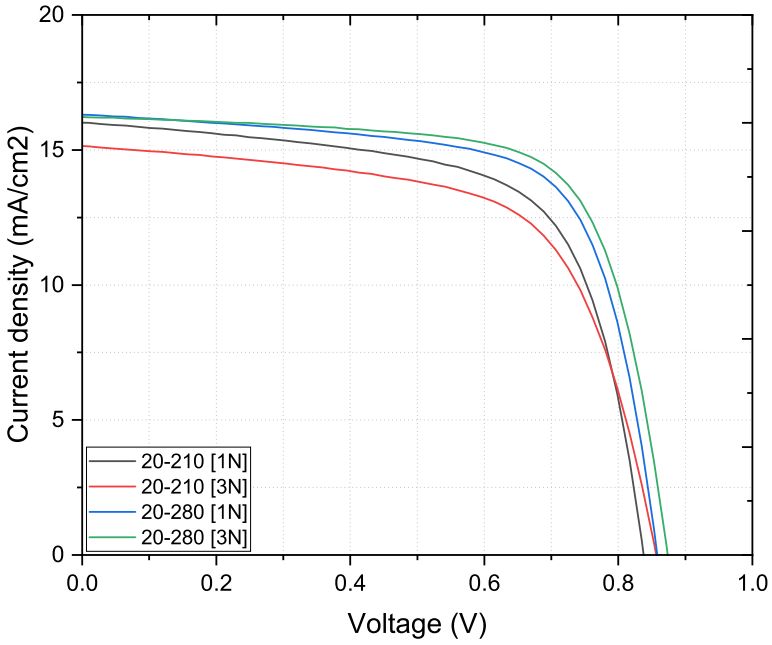



**Figure A.3:** JV curves of devices Experiment 4.4.1

# B

# Absorber thickness series with i-ZnO

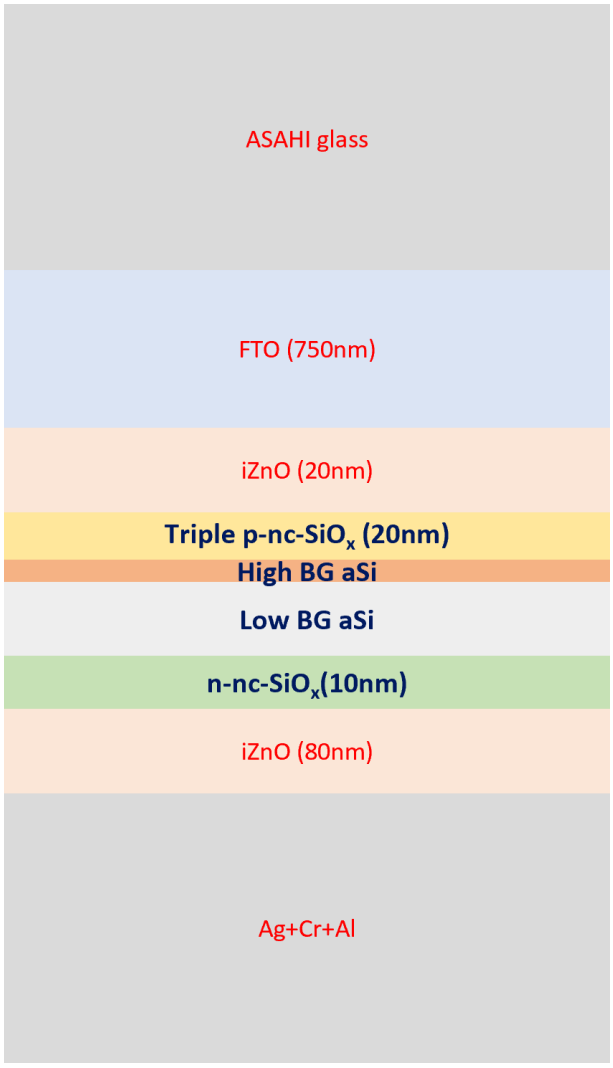
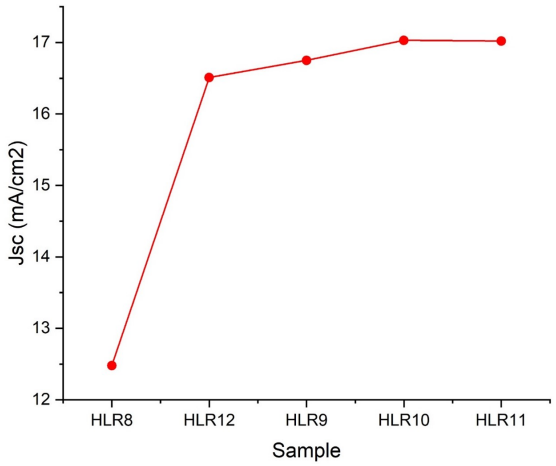


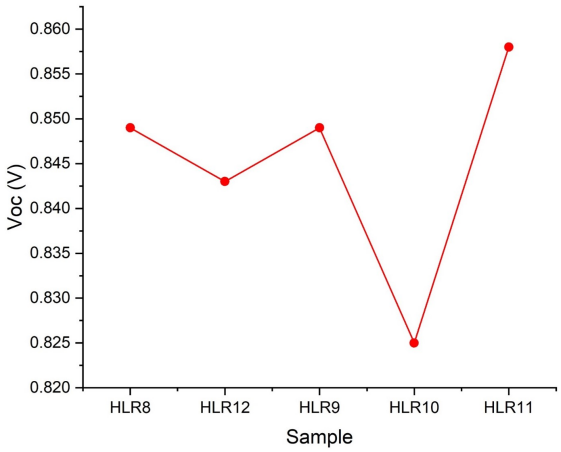

**Figure B.1:** Device architecture

| SAMPLE | texture | High Thickness | Low thickness | P | N | HaSi power | Low asi power |
|---|---|---|---|---|---|---|---|
| HLR8 | Asahi | 30 | 150 | 3P---- 3+10+3 | N NCsloX | 9 | 2.8 |
| HLR12 | Asahi | 30 | 200 | 3P---- 3+10+3 | N NCsloX | 9 | 2.8 |
| HLR9 | Asahi | 30 | 220 | 3P---- 3+10+3 | N NCsloX | 9 | 2.8 |
| HLR10 | Asahi | 30 | 250 | 3P---- 3+10+3 | N NCsloX | 9 | 2.8 |
| HLR11 | Asahi | 30 | 270 | 3P---- 3+10+3 | N NCsloX | 9 | 2.8 |

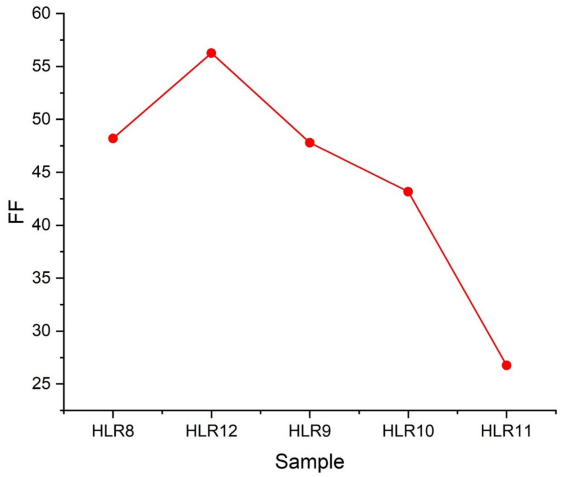
**Figure B.2:** Devices prepared



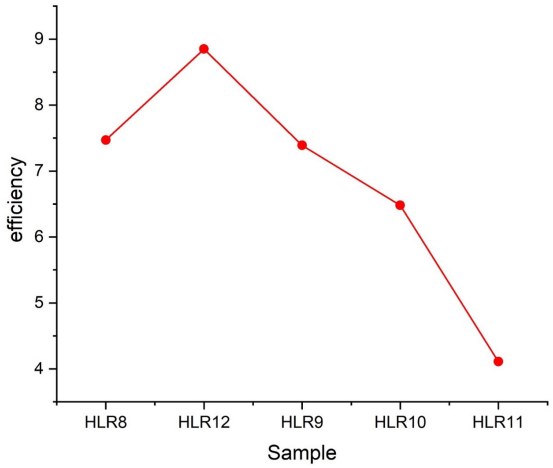

**(a)** $J_{sc}$ variation




**(b)** $V_{oc}$ variation




**(c)** FF variation




**(d)** Efficiency variation

# C

# SEM Images new TCO

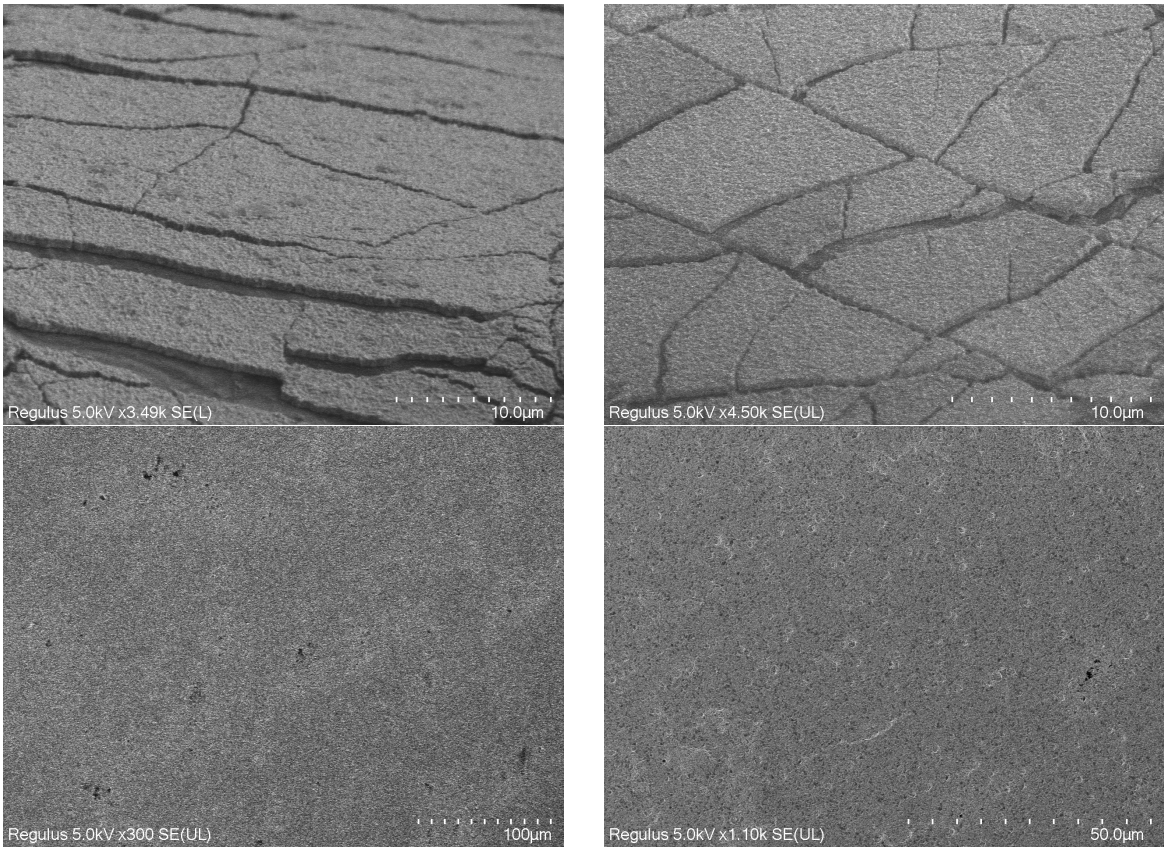



**Figure C.1:** SEM images of the TCO at higher webspeed