Improving packaging and increasing the level of integration in power electronics

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PROEFSCHRIFT

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To Mum and Dad

Mami i tati

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Table of contents

List of symbols

Latin letters

A	Surface area	[m^2]
a	Construction technology alternative	
a	Evaluation criteria	
A_c	Core cross section	[m^2]
a^{norm}	Normalized criteria	
B	Magnetic flux density	[T]
C	Capacitance	[F]
C_{iss}	MOSFET's input capacitance	[F]
D	Duty ratio	[%]
d_{in}	Inner diameter	[m]
d_{out}	Outer diameter	[m]
d_w	Track width	[m]
ESR	Equivalent Series Resistance	[Ω]
f_s	Switching frequency	[Hz]
I	Current	[A]
I_{driver}	Gate drive current	[A]
I_{out}	Output current	[A]
J	Current density	[A/m^2]
K_I	Functional elements integration level	
K_i	Wheeler constant (i = 1,2)	
K_P	Packaging elements integration level	
k	Thermal conductivity	[W/m°C]
k_w	Winding window utilization factor	
L	Inductance	[H]
N_{FE}	Number of functional elements	
N_{FEv}	Number of virtual functional elements	

N_{PE}	Number of packaging elements	
N_{PEv}	Number of virtual packaging elements	
N_{comp}	Number of components	
N_{layers}	Number of layers	
N_{total}	Total number of parts	
N_{turns}	Number of turns	
P	Power	[W]
P_{Qi}	Losses in MOSFET i	[W]
P_{core}	Losses in core	[W]
P_{ind}	Losses in inductor	[W]
P_{loss}	Power dissipation	[W]
P_{rated}	Rated power	[W]
Q_{gd}	Gate drain charge	[C]
Q_{rr}	Reverse recovery charge	[C]
R_{dr}	Internal resistance of gate driver	[Ω]
R_{ds_on}	MOSFET's on-resistance	[Ω]
R_{gate}	Gate resistance	[Ω]
R_m	Magnetic resistance	[Ω]
Rth	Thermal resistance	[°C/W]
Rth_{c_hs}	Thermal resistance case-to-heat sink	[°C/W]
Rth_{j_c}	Thermal resistance junction-to-case	[°C/W]
T	Temperature	[°C]
T_{hs}	Heat sink temperature	[°C]
Tj_{Qi}	Junction temperature of MOSFET i	[°C]
TDR	Thermal design rating	[%]
TMLD	Thermal management loss density	[W/m^3]
t	Thickness	[m]
t_{cond}	MOSFET's body diode conduction time	[s]
t_{fi}	Current fall time	[s]
t_{fv}	Voltage fall time	[s]
t_{ri}	Current rise time	[s]
t_{rr}	Reverse recovery time	[s]
t_{rv}	Voltage rise time	[s]

V	Voltage	[V]
V_{FE}	Volume of functional elements	[m^3]
V_{GG}	Gate drive voltage	[V]
V_{conv}	Converter's volume	[m^3]
V_{plt}	Plateau voltage	[V]
V_{th}	MOSFET's threshold voltage	[V]
v	Construction technology value function	
w	Weighting factor	

Greek letters

ΔI	Peak-to-peak current ripple	[A]
ΔV	Peak-to-peak voltage ripple	[V]
$\tan(\delta)$	Loss factor of magnetic material	
η	Electrical efficiency	[%]
η_v	Volumetric packaging effectiveness	[%]
μ_r	Relative magnetic permeability	

Acronyms

COB	Chip-On-Board
DBC	Direct Bond Copper
DP	Design parameter
emPCB	PCB Embedded Converter
FE	Functional element
FOM	Figure of merit
FR	Functional requirement
HDI	High Density Interconnects
HCC	Heat Conductor Converter
HTCC	High Temperature Co-fired Ceramic
IMS	Insulated Metal Substrate
LF	Lead Frame Converter
LTCC	Low Temperature Co-fired Ceramic
MCM	Multi-Chip Modules
MID	Moulded Interconnect Device

MIM	Metal Injection Moulding
PCB	Printer Circuit Board
PCC	Power Chip Capacitor
PE	Packaging element

Chapter 1: Introduction

1.1 Power electronics applications growth

The present revolution of power electronics has resulted in cost reduction, performance improvement and widespread applications of electrical systems. The use of power electronics is growing in industrial, commercial, residential, aerospace and military environments for applications such as heating and lighting control, ac and dc power supplies, machine drives, electrical welding, etc [Bos92].

An important role of power electronics is energy saving through the controlled and more efficient use of electrical energy. At present, more than 40% of the electric power generated in the US is being reprocessed through some form of power electronics [CPE]. It is predicted that the application of efficient and cost-effective power electronics technology would result in a 25% - 35% reduction in the global consumption of electrical energy. By 2010, it is expected that up to 80% of the generated power will be processed by power electronics systems. This will depend on whether power electronics succeeds in fulfilling the requirements of potential applications.

Some broad estimates state that, at present, around 25% of the global electric power consumption [Lid99], 30% of the EU consumption [Eva] and 55% of the US electrical power consumption [CPE] is consumed by the motor drives industry, 21% by the lighting industry and 13% by the Internet infrastructure. Let us consider where the potential applications of power electronics are in these areas and what the main requirements they impose on power electronics are.

Automotive

The automotive industry is undergoing a revolution in the design of the electrical system in cars. The introduction of new, electrically controlled functions and electrification of the existing ones has increased the demand for electric power. This has resulted in a replacement of the current 14 V bus with the 42 V electrical bus. Due to the complexity of automotive systems, this transition goes through an intermediate step of having a dual 14 V and 42 V power net [Neu00]. The most important enabling technology for this transition is power electronics. Two architectures for the dual power net system are being considered at present. Both of them require a dc-dc converter to tie the 14 V and 42 V subsystems together [Kas01].

Some examples of new electrical loads or electrified present loads are: electromechanical valves, electrical active suspension, power steering, water pump, integrated starter/alternator

etc. All of these loads require an application of power electronics. Some of these features such as electromechanical engine valves will demand both the conversion and sophisticated control at power levels in the 2 kW to 10 kW range. For e.g. in the case of electromechanical valves, no matter what electromechanical mechanism is used, it will be controlled by power electronics according to a complex algorithm with inputs engine speed, load, exhaust gas conditions, temperature and injection dynamics.

Furthermore, due to the advantages of electric and hybrid cars such as high performance, low fuel consumption and low emissions, these vehicles are becoming a major growth area within the automotive industry. The first hybrid car from a major car manufacturer was Toyota Prius, introduced in 1997 with a quantity of 2000 units. By 2002, the annual sales of the Prius reached 12 000 worldwide and in 2004, 50 000 cars were sold in the USA alone [Jon03a][Hyb]. The electrical system in these cars is dominated by power electronics that controls the power flow between motors, batteries and brakes including battery charging system, dc/dc and dc/ac converters for auxiliary devices and appliances etc.

All of these trends are promising to create an important market for power electronics. However, the environment in today's automobiles presents a big challenge for power electronics. The maximum underhood ambient temperature is specified by different manufacturers as between 125 °C and 150 °C depending on underhood packaging philosophy, while the minimum operating ambient temperature is -40 °C. Another significant challenge that power electronics faces, as it penetrates the automotive market, is cost. In many cases the cost of the power electronics determines whether new functions are going to be introduced or not. For e.g. in case of the integrated starter/alternator, the real challenge is not the mechanical integration of the machine with the transmission but the power electronics cost. Some predictions are that the cost of the power electronics is 5-8 times the machine cost [Kas00]. Reducing the cost is a big challenge for the power electronics industry and will determine the future of power electronics in the automotive market.

Computer and Telecommunication

In the computer and telecommunication domain, power electronics is influenced by the consequences of Moore's Law [Mor04]. As the number of transistors in CMOS chips increase, they require lower voltages and higher currents. Since the distribution of high currents at low voltages is very difficult with the centralized architecture, these trends have encouraged the introduction of distributed power architectures instead of traditional centralized systems. Distributed power systems (DPS) are used primarily in telecommunications and high-end enterprise server systems and they generally have a high system cost. A reduction in the cost of the DPS will result in the introduction of this architecture into lower performance systems.

Computers are still the largest market for ac-dc power supplies [PSM]. While dc-dc converter sales are driven by changes in voltages, ac-dc power supply sales are driven by the increasing power requirements of systems. As systems move into higher power ranges, the market shifts as well. At present, the largest market for ac-dc power supplies is the 100 W – 300 W power range, including applications such as desktop PCs, wireless networking etc. The 300 W – 500

W segment is growing fast, particularly due to emerging technologies such as Intel's Balanced Technology Extended (BTX) form factor and Power-over-Ethernet (POE).

All of these trends are highly cost driven. To make the DPS approach more attractive, the manufacturing costs have to be reduced [Tab92]. One possible way of doing this is modularity and standardization of manufacturing processes. Furthermore, the point-of-load dc-dc converters in distributed architecture will have to be lower profiles and have higher power densities. New packaging technologies and advanced thermal management are necessary to achieve these requirements. For non-isolated dc-dc converters (under 200 W) the cost is targeted to drop from 0.15 \$/A – 1 \$/A as it is at present to 0.1 \$/A – 0.5 \$/A in the next five years [PSM]. At the same time, the rated current per unit volume is expected to increase from 50 A/in^3 to 75 A/in^3. For ac-dc front ends, cost is expected to drop from 0.1 \$/W – 0.2 \$/W to 0.08 \$/W – 0.14 \$/W also in the next five years. The power density is targeted to increase from 3-10 W/in^3 to 10-25 W/in^3.

Motor drives

More than one quarter of the world's electricity is used to drive motors. In industrial drives, new generations of gate-controlled power switches have improved the performance and cost-effectiveness of ac drives. The development of solid-state power semiconductors during the second half of the 20th century made it possible to use ac induction and synchronous machines in rail traction drives that eliminated the need for mechanical commutators [Jah01]. By upgrading fixed-speed industrial process equipment to adjustable-speed equipment, significant cost and efficiency improvements can be achieved. Since motor controls make motors much more efficient it is expected that in the next ten years over one billion motors will convert to speed control. This will save the world approximately 100 GW of power [Lid97].

In order to satisfy high volume markets the cost of power electronics in motor drives has to be reduced. This will depend on the advancement of both semiconductor devices and packaging techniques. New packaging techniques are expected to reduce the cost significantly by modularizing the power electronics and automating its manufacturing.

Lighting

Lighting technology is changing rapidly and power electronics is one of the enablers of this change [PEL]. Compact fluorescent lamps, high-intensity discharge (HID) lighting, and high brightness LEDs are some examples of the applications of power electronics to lighting. It is being predicted that in the next ten years, over five billion light bulbs will be replaced with energy-saving electronically ballasted lights. Lighting uses nearly one quarter of all the power generated in the world and converting just five billion bulbs now in use would save the world around 200 GW of power [Lid97]. In the automotive environment one of the emerging applications is the HID lamp used as more efficient headlights. These lamps have much higher efficiencies, white light and a very long lifetime. The disadvantage is complex and costly power electronics, which makes these lamps usable only in high class automobiles. If the cost of the power electronics could be reduced these lamps will find their market in lower-class automobiles as well.

1.2 Meeting the requirements of the future applications

It is shown in Section 1.1 that the range of potential applications for power electronics is very broad. The ultimate goal is to make the power electronics in these systems as transparent to the final user as possible, which means little extra cost, use of existing space and little or no extra thermal management components. This sets very stringent requirements on power electronics concerning electrical and thermal performance, cost and size. In the following sections, the main barriers and frontiers for fulfilling these requirements in present power electronic technology will be discussed.

Electrical and thermal performance

In the past few decades, power electronic converter technology was driven mostly by power semiconductors device technology [Wyk00]. The reduction in power semiconductor devices switching times made it possible to increase operation frequencies from 50Hz to the megahertz region. This has resulted in tremendous improvements in converters' performance, size and cost. On the other hand, packaging technology remained almost unchanged. Power semiconductor devices in discrete form or in form of power modules still use wire bonds and leads for electrical interconnections. Parasitic inductances associated with this technology combined with short switching times severely limit the electrical performance of the device and whole converter. This is especially critical in applications that require fast delivery of large currents in small time intervals such as high-speed microprocessors. For example, the parasitic inductance of the D2PAK power package that comes from wire bonds and leads is 5nH [Pav03]. This inductance combined with large di/dt values causes voltage overshoot across switching devices, electromagnetic noise and switching energy loss [Eva01]. The parasitic resistance value of the same package is 2mΩ compared to the device's on-resistance that can be as low as 4.5mΩ (for low voltage MOSFETs) [IRF]. Wire bonds are also prone to detaching from the semiconductor die due to electrical and thermal fatigue which significantly affects converter reliability. Interconnect inductances of bus capacitors in converters can cause dissipative ringing with output capacitance of power switches which increases voltage stress on the switches.

Furthermore, the conventional converter design process starts with electrical properties of discrete components and concerns only electrical design captured in the circuit schematic. This phase is followed by the converter packaging phase. In this phase, the chosen pre-packaged discrete components have to be packaged together to make the converter assembly, by engineering issues such as electrical connections, mechanical integrity and heat management. This results in a cut-and-trial approach to thermal management where the thermal issues are engineered at the final hardware implementation stage. Each packaging level in the heat path from the heat dissipating component to the heat exchanger contributes with its thermal resistance to the total thermal resistance of the heat path limiting the thermal performance of the system. This is especially critical in high temperature applications (such as automotive) where the maximum allowed thermal resistances that ensure the components' operation within their allowed temperature ranges are rather small. Since thermal behaviour is strongly

dependent on physical implementation, it is necessary to include the physical implementation of the converter into the design process.

Cost

Cost is often a critical parameter in determining whether power electronics is going to find its place in a new application or not. In the past, the cost of power electronics was mainly dominated by the cost of semiconductor devices. As the semiconductor device technology developed further, the overall construction of the converter became more dominant in the total cost. The present construction technology of power electronic converters has matured to such an extent that it becomes extremely difficult to reduce the cost. The present practice is mainly based on assembling pre-manufactured discrete components. During the past few decades, components manufacturers have worked towards reducing the cost of these components. The manufacturers of circuit components such as capacitors, resistors, wire-wound components and even semiconductor components are operating at small profit margins and they cannot afford to spend much on research and development. As a result the technologies are driven deeper into maturity and fractions of a cent become important when the profit margin is calculated [Fer03].

In analyzing the physical construction of a typical converter, one notices that each component in the assembly consists of a number of construction parts. Besides the main electrical part, each component is provided with parts for electrical interconnection, protection and thermal management. Furthermore, the converter assembly includes parts for electrical interconnection of the components, their mechanical support and assembly protection. If all converter parts are added up, one can end up with a total number of parts that could be five or ten times more than the number of components in the circuit assembly. All of these parts have to be manufactured and assembled which makes the total cost of manufacturing a converter high. Figure 1-1 shows a breakdown of the total material cost in an off-line power supply for consumer applications [Phi02]. It can be seen from the figure that the packaging cost represents a significant part of the total material cost. In addition, the level of automation in manufacturing power electronic converters is rather low, which makes the assembling process labour-intensive and thus costly.

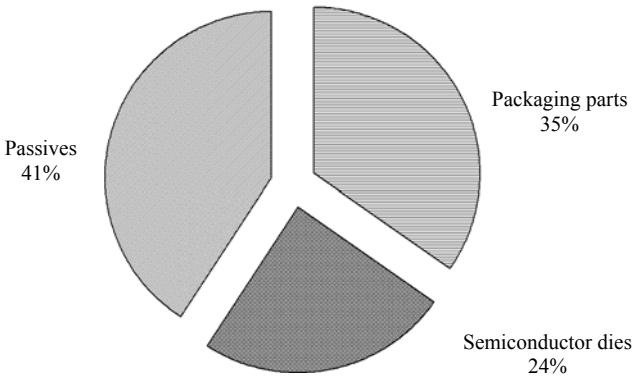

Figure 1-1 Material cost breakdown in a low power off-line power supply for consumer applications

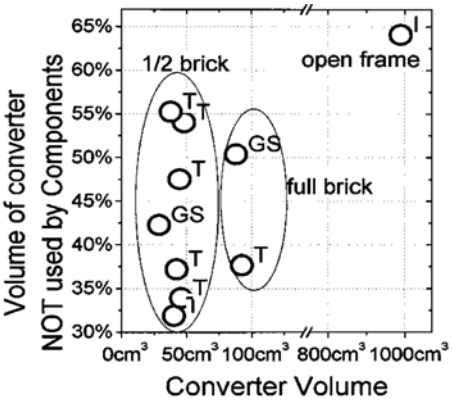

Figure 1-2 Percentage of the converter volume occupied by air – survey [Che02]
(T – telecommunication, GS – government and space, I – industrial power supplies)

Power density

Power density has become a widely used indicator of converter performance since it describes the capacity to process a certain amount of power in a certain volume. Power density is directly dependent on the thermal management and volume of the converter. At present, thermal management in power electronic converters is based on discrete components. High heat density components, such as power semiconductors, are packaged as discrete devices or in a power module and mounted onto the heat sink. The heat they dissipate is transferred in one direction only, from the die(s) through the substrate to the heat sink. Low heat density components, such as energy storage passive components, are cooled individually, each having its separate heat management embedded in the component itself. This results in an inefficient, bulky heat management structure that does not allow for high power densities.

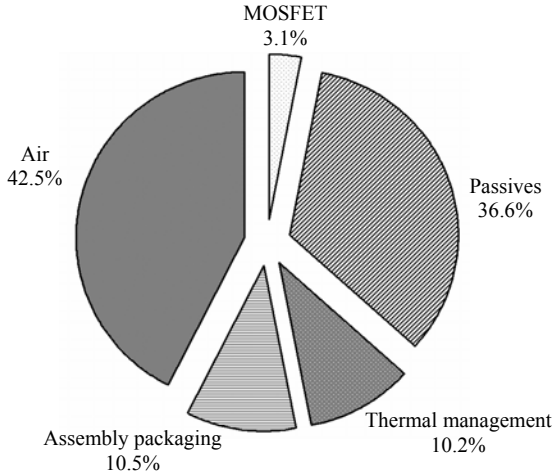

Figure 1-3 Volumetric breakdown of an off-line laptop power supply built in conventional technology

Concerning the volume of power electronic converters, the size of power semiconductors has been reduced to the level where it is not the main limiting factor in achieving high power densities [Wyk00]. It is rather the spatial design of the passive components and converter in total as well as the volume of the converter's packaging structure that occupy the most converter volume. [Che02] shows that a significant percentage of volume in commercial dc-dc converters, in some cases as high as 65%, is occupied by air (Figure 1-2). One of the reasons is the use of conventional pre-manufactured discrete components that are not designed for the application they are going to be used in, neither spatially nor to suit the packaging and interconnection technology. Figure 1-3 shows the volumetric breakdown of a commercial off-line laptop power supply built using conventional technology [Jon03b]. It can be seen that the power semiconductors occupy the minor part of the total volume while the most volume is occupied by air, packaging material and bulky thermal management.

1.3 Problem description

The foregoing discussions on performance, cost and power density of power electronic converters bring us to the conclusion that it is the physical construction including integration, packaging, thermal management and spatial design rather than power semiconductor devices or converter topology that are the main frontiers in the future growth of power electronic applications. A new approach to physical realization of power electronic converters is needed to reduce the cost of power electronic assemblies. The physical construction and world of modelling and simulations have to come closer in order to fulfil the system demands. Since physical realization of power electronic converters is a multidisciplinary technology, this poses a significant challenge for a power electronics engineer.

Physical construction technology involves material technology, layout technology, interconnections technology, component technology etc. All of these issues that are not part of conventional electrical design are sometimes being referred to as packaging [Hop98]. On the other hand, packaging is sometimes restricted to power semiconductors packaging which is inherited from microelectronics and not suitable in power electronics given that passive components represent a significant part in a typical converter. Other terms related to physical construction, such as integration, are also loosely used to suit certain applications and their meanings exhibit a lack of preciseness and general applicability. One of the objectives of this thesis is to approach the construction technology of power electronic converters in a systematic way and to introduce precise terminology that will support improvements in this field and ease communication of ideas and concepts among power electronics engineers.

In order to develop better ways of constructing power electronic converters, it is essential to analyze the present philosophy of construction and identify its main drawbacks. It is important to identify the origins of the large number of constructional parts and manufacturing processes in converters and to consider prospects and bottlenecks that prevent power electronics from achieving a similar breakthrough similar to that in information processing due to silicon monolithic integration technology.

The central objective of the thesis is to investigate how the construction of power electronic

converters can be improved through reducing the number of construction parts by means of integrating the functionality of several parts into one. This includes not only the multifunctionality of electrical parts but also of non-electrical parts since they represent a large portion of the total number of parts in the converter assembly. One of the objectives of the thesis is to devise formal methods to assist power electronics designers in increasing the level of integration by implementing these ideas in actual converters. These methods need to be placed in the total design process in order to form the backbone of the design of the converter's physical implementation. This approach is also intended to make the physical implementation of converters more systematic than it is at present.

Since power electronic converters of the future will have to meet a number of criteria simultaneously, it is important to be able to compare different construction technology options based on all the important criteria in order to choose the optimal solution for the particular application. Many concepts and technologies are emerging in both the industry and academic field and there is a need for tools that allow one to compare them to each other. Therefore, the last objective is to develop a method to evaluate different construction technology options that come out as a result of the developed design process in order to choose the optimal solution for the particular application. This method must allow for industry involvement from the early stages in the design. Such a method could lead to standardization of a technology base for implementing power electronic converters intended for similar applications.

Thesis objectives

Considering the foregoing problem description, four main objectives of the thesis are identified:

- Analyzing the present practice of constructing power electronic converters and identifying its main drawbacks;
- Introducing a systematic approach to construction technology of power electronic converters with the accent on integration and packaging;
- Increasing the level of integration in power electronic converters by:
  - Developing formal methods for achieving higher levels of integration by multifunctional use of construction parts;
  - Identifying technologies that can be used to embody the integration methods;
  - Devising a design algorithm that merges the integration methods and technologies in the process of the mapping of the design of fundamental functions (electrical and thermal) onto the design of physical parts;
- Developing a method for evaluating construction technology of power electronic converters on the basis of a number of criteria such as cost, power density, electrical performance etc.

1.4 Thesis outline

In *Chapter 2* the main characteristics of the present practice of designing and constructing power electronic converters are presented. The main drawbacks regarding manufacturing and assembly issues and converters' performance are identified. Furthermore, an overview of the

current methods used to construct power electronic converters is presented. The overview covers various power ranges and is split up into two parts: components technologies (power semiconductors, passive components and control components) and assembly technologies (interconnection technology, mechanical support technology and heat management technologies). The main focus is on construction parts and manufacturing processes and their influence on the converter performance and cost.

Chapter 3 introduces an approach that defines important terms about power electronic converter construction. The theory is based on a breakdown of the converter's physical construction on basic parts according to the functions that they perform. Two groups of functions are identified: fundamental functions (electrical, thermal and electromagnetic) and packaging functions (electrical interconnection and insulation, mechanical support and protection and thermal interconnection). The foundations of the novel design approach based on functional and packaging elements and integral electrical, thermal and spatial design are introduced. Furthermore, the relationship between two important aspects of power electronic converter construction namely packaging and integration is discussed. Two types of integration – functional elements integration and packaging elements integration – are identified. Some similarities and differences of integration in power electronics and microelectronics are discussed.

Based on the types of integration identified in Chapter 3, two quantities that describe the level of integration in both types are introduced in *Chapter 4*. Furthermore, the formal methods to increase the level of functional and packaging elements integration are developed. Some issues regarding the influence of increasing the level of integration on the converter's electrical and thermal performance are considered. Finally, some limits on increasing the level of integration and the need for circuit partitioning as a consequence of these limits are discussed.

The implementation of the methods presented in Chapter 4 is enabled by the use of various technologies. In *Chapter 5*, an overview of existing and emerging integration technologies is presented. For each technology, the potential to embody the methods for increasing the level of packaging and functional elements integration is discussed.

Chapter 6 deals with a method for evaluating construction technology concepts on the basis of a number of criteria and choosing the optimal among a number of construction technology options. The chapter starts with an introduction to the mathematical techniques referred to as Decision Theory and the basic elements of this theory. This is followed by an identification of these elements in the converter construction: evaluation criteria – figures of merit for converter construction and construction technology value function – function that combines all the criteria by means of suitable weighting factors. The evaluation process is applied to two case studies: PCB power supplies and power modules. For each case study two construction technology concepts are given. The weighting factors for the criteria in both cases are obtained from the preferences of the industry experts in the field.

Chapter 7 explains how the element-based integral design approach outlined in Chapter 3 is implemented by means of the integration methods introduced in Chapter 4 and integration technologies from Chapter 5. This is formalized in a design algorithm whose inputs are library of technology platforms and outputs of the fundamental functions design phase. The algorithm outputs are a number of construction technology options. The options are then evaluated as shown in Chapter 6 and the optimal solution can be chosen for the particular case. This process is implemented in a case study of a dc-dc 42 V/ 14 V converter for dual powernet automotive applications. The design process results in three different construction technology options.

The three construction technology options for the dc-dc 42 V/ 14 V converter case study from Chapter 7 are manufactured and tested. The practical results of the converters' electrical and thermal performance are presented in *Chapter 8* and compared to a benchmark converter constructed in conventional technology. Furthermore, some manufacturing and technology issues and trade-offs regarding the implementation of the concepts are discussed.

In *Chapter 9*, the main conclusions reached in the thesis are drawn and some suggestions for future research are given.

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Chapter 2: State-of-the-art power electronics converters construction technology

2.1 Introduction

The major potential applications for power electronics were identified in Chapter 1. The main requirements that these applications impose on power electronics – in particular, cost, performance and power density – were discussed. The main drawbacks of the present practice of constructing power electronic converters that prevent it from satisfying these requirements were also identified.

In this chapter, the state-of-the-art power electronic converters construction technology is discussed. Section 2.2 starts off the chapter with a historical background of electronic assemblies. Section 2.3 discusses the current practice of constructing and designing power electronic converters. Section 2.4 and Section 2.5 deal with the construction technology of discrete components and the circuit packaging phase, respectively. In both Section 2.4 and Section 2.5, the accent is put on construction parts and their functions.

The chapter is summarized in Section 2.6.

2.2 Evolution of electronic assemblies

In order to understand the way that power electronic circuits are constructed nowadays, one must delve into the history and evolution behind it. The inception of discrete assemblies begins with origins of electrical components [Dar58], i.e. with discoveries of phenomena such as electrical charge storage, electromagnetic induction etc. Electrical circuits are traditionally built around these components using circuit theory for modelling and design. The decoupled approach between design and physical realization or manufacturing over years has resulted in a one-to-one relation between symbols in the electrical circuit diagram and components. This means that each circuit symbol is realized by one physical component. Furthermore, electrical interconnections in the circuit schematic and physical wires also had one-to-one relation.

The increased demand for electronic circuits in radio communication systems some six decades ago had forced the electronic industry to seek a better way of interconnecting components than the slow, error-prone and labour-intensive point-to-point wiring practice. The efforts had resulted in the invention of printed wiring which made it possible to implement electrical interconnections with metallization patterns produced in one manufacturing process. This had brought large cost savings through automatization of the process and prompted the industry to look for ways to eliminate the one-to-one relationship between circuit symbols and components

through manufacturing a number of parts in one integral process on a multifunctional insulating supporting plate [Sar47].

The invention of the Integrated Circuit made it possible to build the whole electronic circuit in one physical component. In microelectronics, an enormous cost, size and performance improvement was achieved by monolithic integration. Voltage, current and energy storage levels in microelectronic circuits are much lower than those in power electronics, and this allows for the integration of all the circuit functions in one chip. However, even in microelectronic systems the number of discrete components is still high. This is due to a number of factors, cost often being the most dominant.

The level of integration in power electronics assemblies is still rather low. Assemblies of discrete components make up the vast majority of power electronics circuits. Monolithic integration of the whole circuits is only feasible at very low power levels due to the higher voltage and current ratings that power electronic circuits handle [Wyk00]. Enclosing a number of power semiconductor devices into one package is referred to as a power module and was introduced a few decades ago [Sto00]. It has become the state-of-the-art in the medium power range (up to a few kilowatts). On the other hand, passive components integration is still in its infancy. In lower power ranges, technologies that integrate passive components into the circuit carrier are emerging [Waf02]. In medium power ranges, the electromagnetic integration of passives is realized by ceramic based planar technologies [Wyk03].

2.3 Present practice of designing and constructing power electronics converters

As discussed in the previous section, power electronic converters to date are mainly constructed as assemblies of discrete components. The electrical parameters of discrete components mostly found in manufacturers' data sheets are used as input parameters for the electrical design, as illustrated in Figure 2-1 [Pop03]. The design of the circuit electrical function is represented by an electrical circuit schematic. The outcome of this phase is electron flow paths. This is followed by the circuit packaging phase, where the electron flow paths are mapped onto physical electrical interconnections. In order to ensure the proper functioning of the converter, additional issues such as mechanical integrity (including mechanical support and protection) and heat management are engineered in this phase. This is done by arranging the discrete components and necessary additional parts into electrical, thermal and mechanical structures.

2.3.1. Large number of construction parts

Each discrete component used in a power electronic converter assembly consists of a number of parts. Besides the part that performs the main electrical function, each component contains a number of parts that ensure the component's integrity. These include parts for electrical interconnection with the outside world, for environmental protection, mechanical support, heat removal etc. Such components are fully packaged and self-standing.

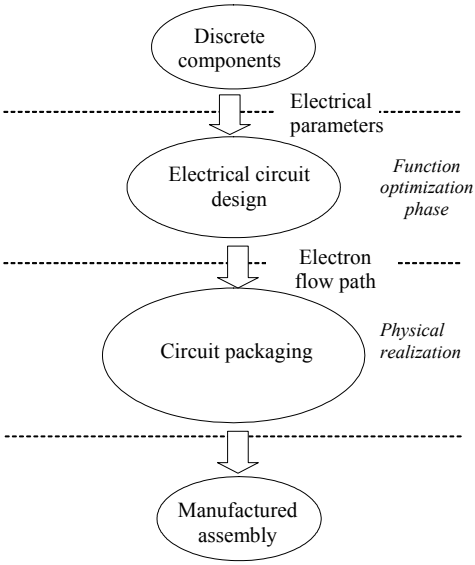
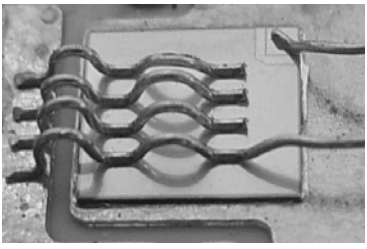
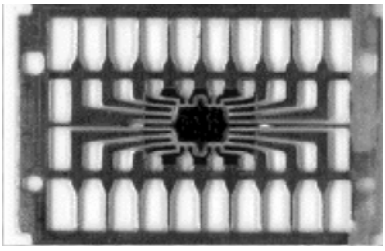
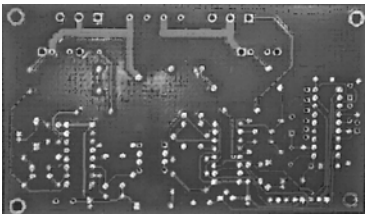


Figure 2-1 Conventional construction of power electronic converters

The circuit packaging phase requires additional parts and assembly processes to ensure the proper functioning of the converter: to electrically interconnect the components with each other and the assembly to the outside system, to provide mechanical support and protection from the environment, to perform the exchange of the heat dissipated by the converter's components with the environment etc.


wire bonds


lead frame


PCB tracks


connectors

Figure 2-2 Electrical interconnection parts

This sequential approach combined with the use of discrete components results in a large total number of construction parts in a converter. A large number of parts in a typical power

electronics assembly can be illustrated with the number of parts that provide electrical interconnections in the converter, shown in Figure 2-2. The first level is the component level, which includes leads and lead frames that connect the component to the outside world and wire bonds that connect the basic electrical part of the component to the component leads. The next level of interconnections is the circuit level, mostly implemented in the form of tracks in the metallization of the circuit carrier. The third level is connecting the circuit to the system by means of connectors or metal terminals. The situation is similar with the parts that provide the heat removal. On the component level, components contain parts intended for heat removal, such as metal slugs in the case of power semiconductors. Additional parts are added on the assembly level, such as thermal interface materials, thermally conductive substrates, etc. The third level thermal management parts are normally heat exchangers, such as heat sinks in order to convey the heat dissipated by the converter components to the ambient.

Manufacturing and assembly issues

The efforts to include manufacturing and assembly concerns in early stages of the product design in order to achieve a cost-effective product were formalized into the Design for Manufacture and Assembly (DFMA) techniques by G. Boothroyd [Boo94]. In this reference, “to manufacture” refers to the manufacturing of the individual parts of a product or an assembly and “to assemble” refers to the addition or joining of parts to form the completed product. This notation will also be used in this book.

According to the main principles of DFMA, *reducing the number of parts* in an assembly is the most powerful way of reducing the assembly cost [Shi91]. As previously discussed, the number of parts in typical power electronic assemblies is large. If all the constructional parts in a power electronic converter are added up, one can end up with a number that is several times larger than the number of symbols in the electrical circuit schematic. Each of these parts has to be manufactured and connected to the rest of the assembly which makes the total cost of the converter – including material, manufacturing, assembling and overhead costs – high.

Another DFMA principle is *multifunctionality* of construction parts. Regarding multifunctionality or the lack thereof in a power electronics assembly, each discrete component contains parts that serve only that one component. Examples are component cases, leads etc. Furthermore, these parts often perform only one function, e.g. electrical interconnection or heat conduction etc. The functionality of basic electrical parts is low too since the electrical part of a discrete component implements only one circuit schematic symbol.

The next DFMA concern is *standardization* of parts in an assembly. The need for standardization of component parts had been recognized together with the need for automation in electronic circuits [Pos58]. In a typical power electronic converter a large diversity of components is used. These components have been optimized by their manufacturers over years in order to reduce their cost and size. Various types of components have followed different development paths. This has resulted in a number of incompatible technologies that can be found in a typical power electronic converter. There are parts in different components that perform the same function but are incompatible with each other from the manufacturing

viewpoint and thus present a barrier to prospective manufacturing of converter parts and assembling them together in one manufacturing line.

Modularization is another DFMA technique. The use of modular construction during manufacturing permits a large and complex unit to be broken down into small and often repetitive subassemblies that can be manufactured efficiently [Ans58]. It also makes failure repair simpler because the failed module rather than the whole assembly, can be replaced. In information processing, two basic modules are standardized: switching module (CMOS inverter) and information storage module (DRAM cell) [Bor05]. In power electronics, modularization is present only in the form of power modules, where a number of semiconductor dies connected according to the most common topologies are placed in a single package.

Finally, minimizing the *assembly time* is another concern of DFMA. Power electronic equipment is often labour-intensive due to the assembling of parts that do not lend themselves to automated assembly.

Converter's electrical, thermal and spatial performance

The large number of parts in power electronic assemblies also affects the converter's electrical, electromagnetic and thermal performance. The multilevel packaging hierarchy adds parasitic effects such as electrical inductance, capacitance and resistance, due to the electrical interconnect paths and impedance mismatch between packaging levels or components [Lia04]. These parasitic elements cause propagation distortion of the electromagnetic energy flow. Parasitic inductances of these parts in components limit the electrical performance of the switching devices. Parasitic resistances cause additional conduction losses in the component or assembly. Parasitic capacitances of these parts combined with large dv/dt values cause common mode electromagnetic noise.

Furthermore, each part in the heat path from the heat dissipating component to the ambient contributes with its thermal resistance and capacitance to the total thermal impedance of the heat path affecting the thermal performance of the converter.

Finally, the large number of construction parts negatively influences the total volume of the converter, since each construction part takes up a certain volume.

2.3.2. Non-optimized electromagnetic, thermal and spatial issues

Besides the existence of a large number of parts and problems that it causes (discussed above), the present design approach from Figure 2-1 has another significant drawback. The function optimization phase deals with the optimization of the electrical function only and electromagnetic, thermal and spatial issues are engineered in the circuit packaging phase. This approach was acceptable in the past since converters operated at lower switching frequencies, components were larger and spread apart, surface areas for heat removal were larger, electromagnetic coupling between components could be neglected and the size of power electronic systems was not critical.

With the recent advances in power switching devices (MOSFETs, IGBTs) operating switching frequencies are constantly being increased, and this has resulted in size reductions of passive components and power electronic converters on the whole. This in turn results in an increase of loss power densities in components. Furthermore, the ever-increasing need for smaller volumes and higher power densities has brought components in close vicinity to each other, influencing each other's operating temperature. This poses more stringent requirements on the heat management of power electronic converters. As the thermal behaviour is considered one of the main reliability issues in power electronics it is crucial to ensure that all the components work in their allowed temperature ranges.

The electromagnetic behaviour of power electronic converters is another issue that became important with the increase of switching frequencies and power densities. Fast switching of power devices, combined with parasitic elements of the devices and layout, generates the electromagnetic noise. Electromagnetic compatibility has become an important issue in power electronics and standards introduced to control electromagnetic noise levels have to be met in future converters.

Furthermore, the need for a size reduction brings components closer together and leads to their physical integration [Fer01]. This results in electromagnetic coupling of these parts.

In the conventional approach from Figure 2-1, both thermal and electromagnetic issues are engineered in the circuit assembly phase. These issues are often conducted by means of the "cut-and-try" approach by performing EMI and thermal measurements on the hardware and if satisfactory results are not achieved, a time-consuming redesign and additional hardware are necessary. This results in penalties in size and cost.

2.4 Construction of power electronics components

As mentioned in the previous section, a large diversity of components is found in power electronic converters. In the following sections, the construction technology of components typically used in power electronics are described with the accent on the construction parts and functions they perform.

2.4.1. Power semiconductors construction

Figure 2-3 shows the cross-section of a typical leaded discrete power semiconductor component. The back side of the power semiconductor die is attached to a copper alloy lead frame by means of a die attach material such as soft solder. This part of the lead frame provides the electrical connection between the drain (collector) pad and the outside world, mechanical support for the die and a heat path for the heat dissipated by the die. The rest of the electrical connections between the die pads and the lead frame leads are provided by means of wire bonding. Finally, the die is encapsulated for protection with a mould compound such as epoxy resin. The lead frame leads protrude from the edges of the package. They can be designed to make different types of packages. A package can be through-hole (Figure 2-4a), designed to be plugged into a circuit carrier (such as printed circuit board) by inserting the leads through

holes. It can also be surface mount (Figure 2-4b) where the component is soldered onto the circuit carrier.

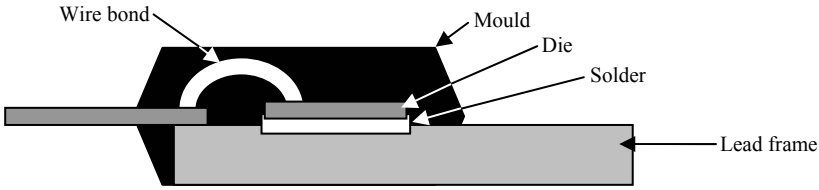
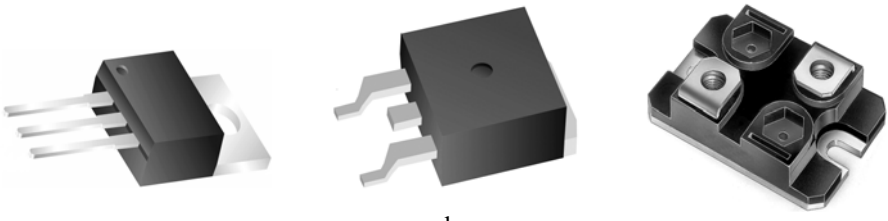


Figure 2-3 Power semiconductors conventional package – cross-section

Some applications require electrical isolation from the mounting surface (heat sink). In this case, a power semiconductor die is soldered (or glued) to an insulating substrate. This substrate is mounted onto a metal base plate (Figure 2-4c). As this is the main heat path, substrates with a high thermal conductivity, such as ceramic substrates, are the most suitable. The same construction method is used when several power semiconductors are mounted into one package which is referred to as a power module.

The conventional packaging methods described above have a number of drawbacks. The interconnection technology, wire bonding, degrades the electrical performance by increasing the parasitic inductance and resistance, affects reliability and intrinsically limits the device's thermal management to single-sided cooling. Furthermore, the packaging levels in the device's heat path increase its thermal resistance, thus limiting the power capability of the package. Also, the size of the package is three or more times larger than the die size [Eva01], thus influencing the power density. Finally, the package cost contributes approximately one third of the total cost of the power semiconductor device.

In order to deal with these issues, a number of packaging techniques with advanced interconnection methods and heat management are emerging. Some of them employ advanced interconnection technologies such as flip-chip instead of wire bonding combined with chip-scale packaging (FlipFET [IRF], MOSFET BGA [Fai]). Others provide double-sided cooling by means of a special die design to provide solderable gate and drain pads on the bottom side of the device while the top drain pad is attached to the copper housing that extends on the sides and makes the drain connection (DirectFET [IRF]). Power semiconductors can also be used in the non-packaged die form, thus eliminating the packaging levels and improving the electrical and thermal performance.



a. b. c.

Figure 2-4 Power semiconductors packages: a. through-hole, b. surface-mount, c. electrically isolated

2.4.2. Passive components construction

Capacitors

The need to obtain high capacitance values in small volumes and to control other parameters has enforced the use of many materials, both for electrodes and for dielectrics. Different materials used for dielectrics, electrodes and package, and different manufacturing processes and construction types result in capacitors with various characteristics. The main difference is in the dielectric type, which primarily determines the application of the capacitor. Power electronics makes large use of capacitors for a number of functions such as energy storage, filtering, decoupling, timing, etc. In order to perform a specific function, requirements imposed on a capacitor may vary, hence capacitors made in different technologies and packaging techniques are used. There are three major capacitor technologies: ceramic, metal film and electrolytic. Since they use different dielectric types their overall construction technologies also differ.

Ceramic capacitors - The ceramic dielectrics are made of a variety of titanates (titanium oxide (TiO_2), barium titanate ($BaTiO_3$)), and oxides. Common ingredients include titanium dioxide, barium titanate, and strontium titanate. Initially, the dielectric was implemented by a single layer of ceramic. A metal layer is screen-printed on both sides of the ceramic disc and fired to make capacitor electrodes. Hairpin wires that provide electrical interconnections are soldered onto it and the capacitor is coated with epoxy for protection. The whole process is automated and these capacitors are inexpensive. However, capacitance values that can be achieved with this technology are limited to lower values, such as 0.01μF.

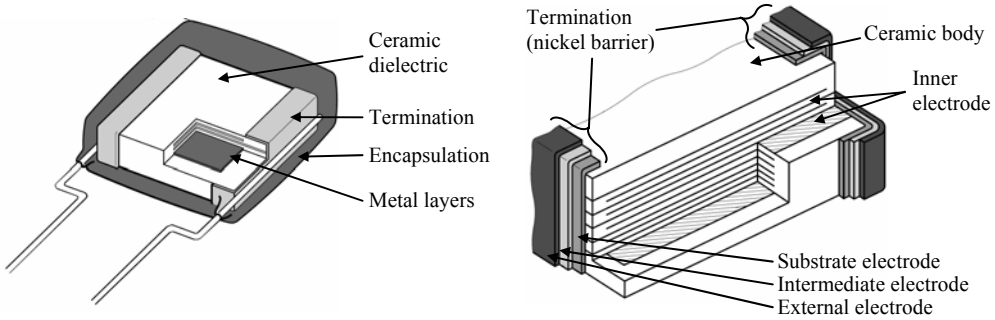


Figure 2-5 Multilayer ceramic capacitor: a. leaded b. SMT [Epc]

In order to achieve higher capacitance values, multilayer ceramic capacitor technology is employed. A number of very thin unfired ceramic tiles are screen-printed with gold, palladium, platinum, and silver alloy to implement capacitor electrodes. Once the ink is dry, the tiles are stacked on top of each other. The screen-printed electrodes are arranged so that alternate electrodes exit from opposite ends. The top- and bottom-most layers do not have screen-printed electrodes. The laminated layers are then compressed and fired, which sinters them into one monolithic structure. Next, the ends are terminated, often with silver. Electrical connections are realized either in the form of wires that are soldered onto the ends, which results in leaded

capacitors (Figure 2-5a), or the terminations can be covered with tin for direct soldering onto the PCB, which results in so-called chip capacitors (Figure 2-5b). The whole capacitor may be covered with lacquer or encapsulated in plastic for protection. Capacitance values of these capacitors range from several pico farads to several micro farads.

Metal film capacitors – These capacitors are based on a dielectric film on which a very thin layer of metal is vacuum-deposited. The thickness of the metal layer is in the range 80-300 Å. Metals used are aluminium, zinc, silver, or combinations of these metals, as well as a variety of proprietary alloys. Dielectrics used are polyester, polypropylene, and polycarbonate. The metallized films are cut and wound into capacitors (Figure 2-6). Another way is to stack the foils and insulator in alternating flat layers instead of winding them. This makes for a compact form-factor and low inductance. Lead wires for electrical interconnections are attached to the metallized film electrodes by first spraying layers of high-purity metal (melted with an electric arc) on each end of the capacitor and then welding the wires onto the sprayed layers. The capacitor is then encapsulated for protection. These capacitors also come in an uncoated form such as Silver Caps [Epc] or in an uncoated, unleaded form such as the Power Capacitor Chip (PCC) [Epc]. Such designs have smaller volumes and allow for advanced spatial designs thus achieving higher power densities. Capacitors for use in applications with commutating high reactive power and with high peak current load are implemented with polypropylene dielectric film and an electrode of double-sided metallized paper [Epc].

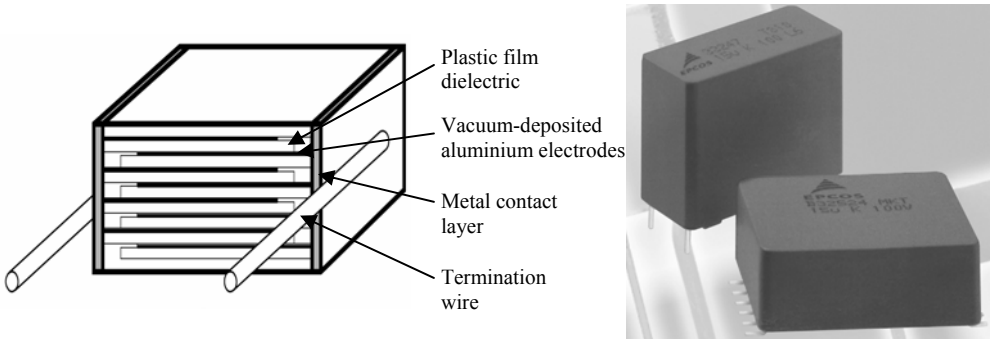


Figure 2-6 Metal film capacitor a. construction [Wim] b. encapsulated capacitor [Epc]

Electrolytic capacitors – Most electrolytic capacitors today are aluminium electrolytic capacitors. The manufacturing process of these capacitors is mostly automated and consists of several steps. A sheet of aluminium foil which has been etched in acid represents the anode electrode of the capacitor. The etching process significantly increases the effective surface area. The capacitor dielectric consists of a thin oxide, Al_2O_3, grown on the etched aluminium foil. The second electrode is a sheet of paper saturated with a liquid or a gel electrolyte. The electrolyte forms an intimate contact with the outside of the dielectric on the roughened aluminium foil. A second sheet of aluminium foil, which is usually not etched, forms the contact to the liquid or gel electrode. Metal leads are attached to the two aluminium sheets for electrical interconnection, the layers are rolled up, and the structure is encased into a metal can

for protection. The winding construction of an aluminium electrolytic capacitor is shown in Figure 2-7a while the package cross-section is shown in Figure 2-7b.

In place of liquid electrolytes, solid electrolytes can be used, such as manganese dioxide in solid tantalum capacitors or organic semiconductor capacitors (Os-Con capacitors [Vis]) – the latter having a very high electrical conductivity and thus low ESR. The construction principle is similar to the one used in aluminium electrolytic capacitors.

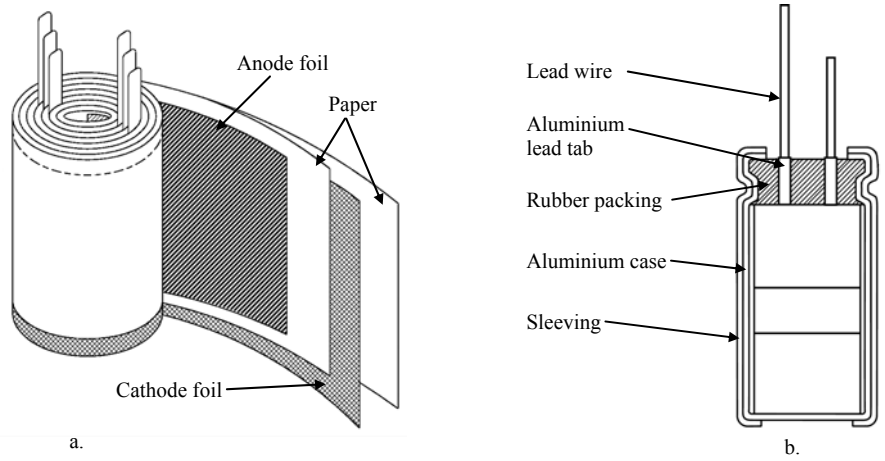


Figure 2-7 Aluminium electrolytic capacitor construction a. winding construction [Epc] b. package cross section [Nic]

Magnetic components

Magnetic components in power electronics are used for a broad range of functions such as energy storage, filtering, isolation, level-shifting etc. To date these components are mostly custom designed with the exception of low power through-hole and surface-mount inductors, which are provided by a number of manufacturers. Their manufacturing process is often labour- intensive and makes up a significant percentage of the total assembly cost.

Magnetic components construction is very diverse. There are a number of materials used for magnetic cores and a variety of winding technologies. The four main types of magnetic materials are laminated polycrystalline metallic alloys, polycrystalline metal powder, ferrite and amorphous cores. Each of these materials has its niche applications depending on the design requirements such as operating frequency, saturation flux density, thermal environment etc.

Magnetic components construction and assembly process is mainly determined by the winding technology. The most widely used winding technologies are wire-wound technology (solid and litz wire), foil winding and planar winding technology.

Wire-wound technology – This is the most mature winding technology (Figure 2-8a). The insulated solid wire or litz wire (a number of individually insulated strands of very small round

wire that have been woven or braided together – a more expansive alternative to solid wires) is wounded on a plastic coil former (bobbin) which provides the mechanical support and electrical interconnections.

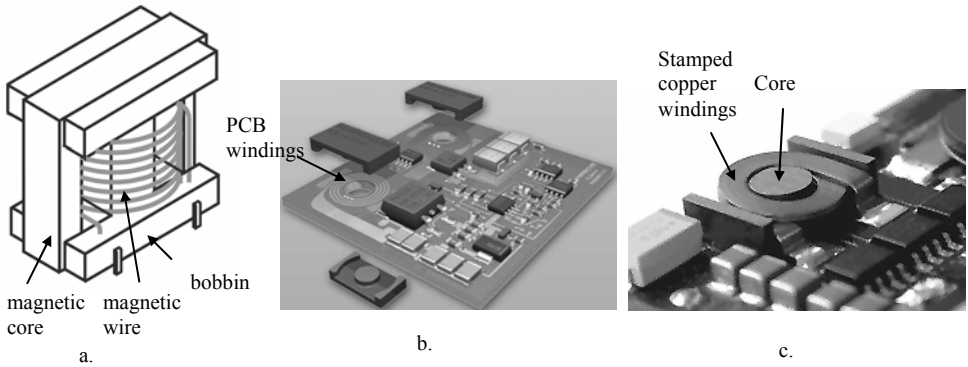


Figure 2-8 Magnetic components winding technologies a. wire-wound b. planar PCB [Fer] c. planar stamped copper [Hil04]

Foil winding technology – This type of winding is made mostly from an un-insulated copper foil slightly narrower than the winding window wound on a coil. Each turn forms one winding layer. Insulation between the windings is provided by inserted layers of Kapton or similar material between the turns as the foil is wound. Making the foil winding is often a manual process. Furthermore, making the terminating electrical connections is always a challenge.

Planar technology – Various technologies can be used to implement the planar windings. The most widely used are Printed Circuit Board (PCB), flex circuit and stamped copper [Qui01]. Windings fabricated in thick film and Low Temperature Co-fired Ceramic technologies are used in low power applications. Printed circuit board technology offers a highly repeatable and manufacturable way of producing planar windings. The windings can be implemented in the main circuit carrier, thus simplifying assembly process (Figure 2-8b). The disadvantage is a low window utilization factor due to the thickness of the PCB laminates. This can be improved by using a flexible substrate with a very low dielectric thickness. Stamped copper windings are manufactured by means of the stamping process that cuts the winding out of an un-insulated copper foil (Figure 2-8c). Resulting lead frame windings have to be insulated by inserting additional insulating layers. The lead frames are self-supporting foil conductors which are shaped to fit the core as a single turn. Creating multi-turn windings is more difficult, hence the windings created using this technology are mostly limited in number of turns. Also, the winding turns have to be mutually electrically interconnected by means of metal interconnection techniques such as welding. They are therefore suitable for relatively low voltage high current applications.

2.4.3. Control components construction

In this section, the main characteristics of the construction technology of control integrated circuits, resistors, capacitors and inductors used in the control part of the circuitry will be presented.

Control ICs

Figure 2-9a shows a cross-section of a typical package of a controller in power electronic converters. The silicon die is epoxy attached to a copper-alloy lead frame for mechanical support. The electrical connections between the die and the lead frame are realized by means of wire bonding. The component is then encapsulated in injection-moulded plastic for protection. The heat is dissipated through the encapsulation and the lead frame pins. Depending on the way the lead frame is formed, they come in through-hole or surface-mount packages (Figure 2-9b).

In some cases, circuits to drive power semiconductors are integrated in the same die with the control IC. These ICs have higher heat density (dissipate more heat per unit area) and hence require improved thermal management compared to standard ICs. For this reason, the die is mounted on the lead frame pad that is exposed at the back side of the package establishing a low thermal resistance heat path from the die, through the lead frame pad to the circuit carrier (Figure 2-9c).

Resistors – Resistors used in control circuitry are mostly in the surface mount form. Alternatively, they can be integrated on the substrate in thick-film or thin-film technologies on ceramic substrates [Tar96]. There are two main types of rectangular surface mount resistors: thick film and thin film. Thick film surface mount resistors are constructed by screening resistive film (ruthenium dioxide based paste or similar material) on a flat high purity alumina substrate surface that serves as mechanical support for the resistive film. The resistance value is obtained by varying the composition of resistive paste before screening and laser trimming the film after screening. Figure 2-10 shows the construction of a thick film resistor.

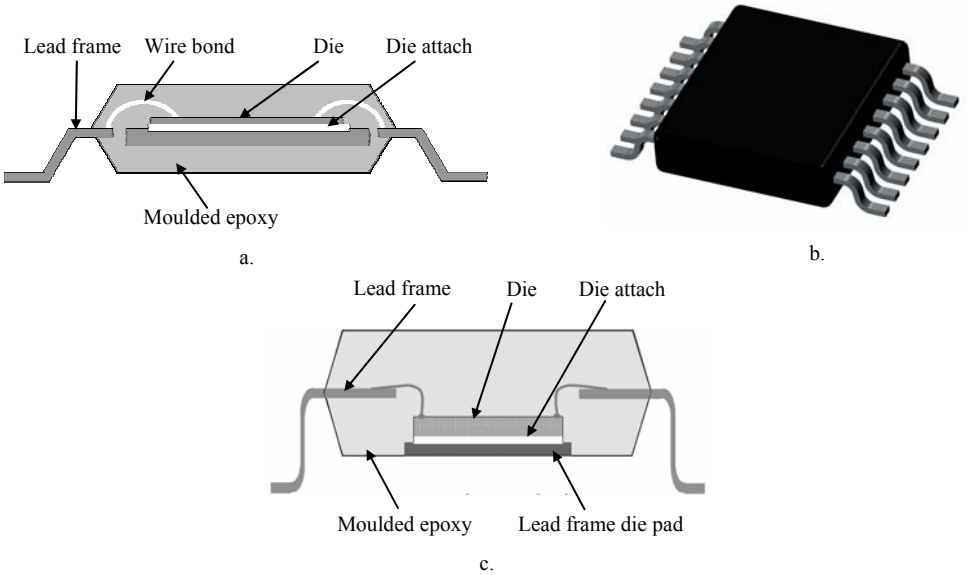


Figure 2-9 Control IC construction a. standard package cross section b. surface mount IC package c. thermally enhanced package [Tex]

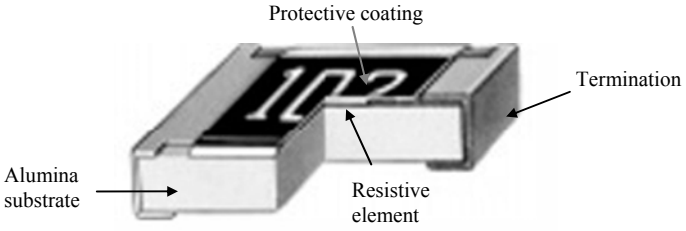


Figure 2-10 Surface mount thick film resistor [Pan]

In thin film resistors, the resistive element is nichrome film, which is sputtered on the ceramic substrate instead of being screened on. Both thick and thin film resistors are protected by protective coating (glass passivation). Electrical connections are provided by several layers of metallization. The terminations have an adhesion layer (silver deposited as thick film paste) on the ceramic substrate, and nickel barrier underplating followed by either dipped or plated solder coating. The nickel barrier is very important in preserving the solderability of terminations because it prevents leaching (dissolution) of the silver or gold electrode during soldering.

Capacitors – Ceramic multilayer surface mount chip capacitors (shown in Figure 2-5b) are mostly used in the control part of the circuitry. If the control circuit carrier is designed in thick film technology, dielectric pastes and metallized layers for electrodes can be screen-printed directly on the substrate.

Inductors – A monolithic chip inductor is shown in Figure 2-11. Such an inductor is constructed by layering the coil windings between layers of core material (ferrite or ceramic core). The inductance value can be made larger by adding additional layers for a given spiral pattern.

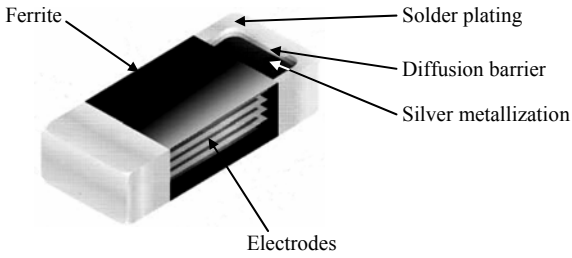


Figure 2-11 Multilayer surface mount inductor [Koa]

2.5 Circuit packaging technology

The circuit packaging phase in Figure 2-1 involves connecting manufactured components into the final product by using parts and processes necessary to provide the following:

- Completing the electrical circuit by providing low resistance paths for current flow and providing electrical isolation;
- Mechanical integrity including mechanical support and environmental protection;

- Paths for removal of the heat generated by power dissipation of components.

The input converter specifications set requirements on circuit packaging technology. Current levels and the operating environment determine the thermal management requirements. Voltage levels impose requirements on insulation materials and techniques. The specifications related to the operating environment (humidity, dust, vibrations) determine protection needs.

In the following text, an overview of the circuit packaging technologies for power electronic converters classified on the power level basis is given. Five power levels are distinguished:

- Very low power level (< a few Watts);
- Low power level (a few Watts to a few hundreds of Watts);
- Medium power level (a few hundreds of Watts up to a few kW);
- High power level (a few kW up to 100 kW);
- Very high power level (> 100 kW).

These boundaries are not strict, as there are converters that belong to one defined power level but use technologies associated with the other power levels. Furthermore, technologies for implementing converters of the same power rating but different current and voltage ratings could differ. The classification is intended to cover the most widely used circuit packaging technologies in today's power electronic assemblies.

2.5.1. Very low power level

Monolithic integrated assemblies

Monolithic integration of power switches, driver and protection circuit and in some cases the whole converter is limited to the very low power range [Mus05]. In this technology, all circuit schematic symbols and electrical interconnections are implemented in silicon. The circuit packaging technology in this case comes down to packaging of a conventional IC as described in Section 2.4.3.

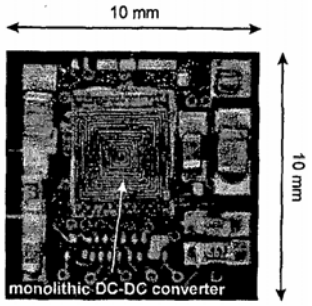


Figure 2-12 Monolithic 1W DC-DC converter with thin-film inductor fabricated on the chip [Sug00]

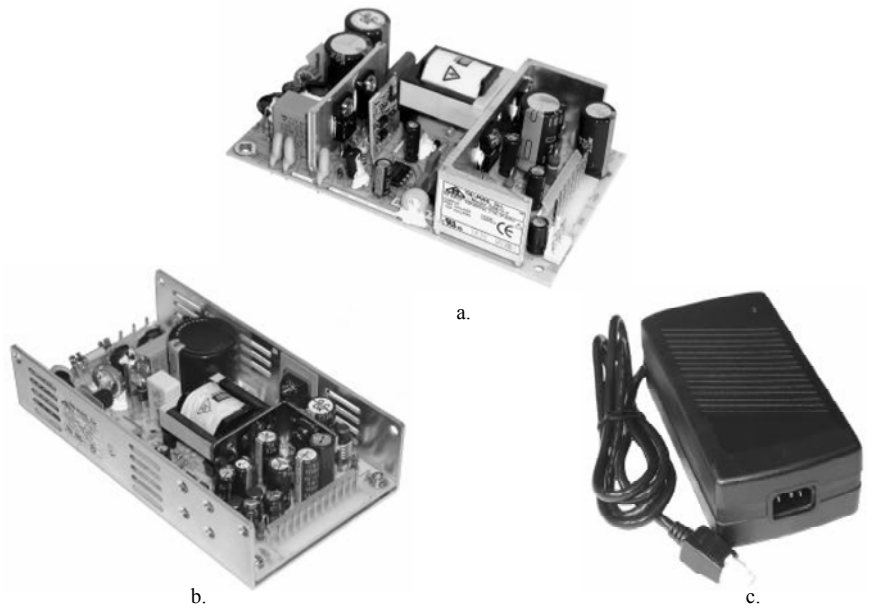
One of the limitations of this technology is that is not economical to process power semiconductor devices through all the mask steps necessary for control semiconductors processing. Also, these switches are capable of blocking relatively small voltages. Monolithic integration of passive components is also limited due to the unsuitable dielectric and magnetic properties of silicon. Even in very low power converters, the electrical performance of the passive components, especially inductors realized in CMOS technology, is poor. Therefore,

various techniques of manufacturing inductors on the chip with micro-fabrication techniques, such as thin-film [Sug00] (Figure 2-12) or micro-electro-mechanical systems (MEMS) technologies [Mus05] are used. Furthermore, only part of the conductive function can be realized inside the semiconductor material; the rest have to be implemented by metallized structures [Wyk00]. Furthermore, heat sinking cannot be readily realized in monolithic technology.

2.5.2. Low power level

Printed Circuit Board assemblies

The vast majority of power electronic converters in this power range use printed circuit board for electrical interconnections and mechanical support. Typical off-line PCB power supplies are shown in Figure 2-13. The PCB manufacturing process is mature and inexpensive. Standard, discrete components are mostly used, both for power semiconductors and passive components. These components are soldered onto the PCB. The PCB tracks together with the components leads and wire bonds provide the electrical interconnections. Depending on the power dissipation level, the power semiconductors are attached to a heat sink by means of thermal interface materials (thermal grease, insulating tapes etc.). The heat sink can be a stand-alone metal block, a metal block connected to the system housing or the system housing itself [Che02]. The rest of the components are mainly cooled by means of convection (natural or forced). Depending on the operating environment, the whole assembly can be enclosed in a metal box (Figure 2-13b) for mechanical protection and electromagnetic shielding or potted using silicone-based materials or epoxies (Figure 2-13c) for protection.



a. b. c.

Figure 2-13 PCB power supply assembly [Tri] a. open frame (75 W) b. in metal box (200 W) c. encapsulated (120 W)

2.5.3. Medium power level

Injection moulded lead frame power modules

For applications up to a few kW, power semiconductors, gate drives and protection circuit can be enclosed in one package as shown in Figure 2-14 [Sch03]. The bare power dies and the gate drive integrated circuits are assembled on a lead frame that provides electrical interconnection, mechanical support and a heat path. The electrical interconnections between the chips and the lead frame are made by means of wire bonding. Depending on the power rating of the module, a block of aluminium can be inserted to conduct the heat from the power dies through the lead frame and a thin layer of thermally conductive epoxy formed on the aluminium block to the heat sink surface of the module. For lower power levels, the lead frame with the layer of epoxy on it is bent, allowing good heat transfer. The whole module is encapsulated by injection moulding to provide environmental protection and hold the assembly together.

The rest of the circuitry, such as passive components, auxiliary power supply, high level control and other electronics, is assembled in PCB technology (Figure 2-14c).

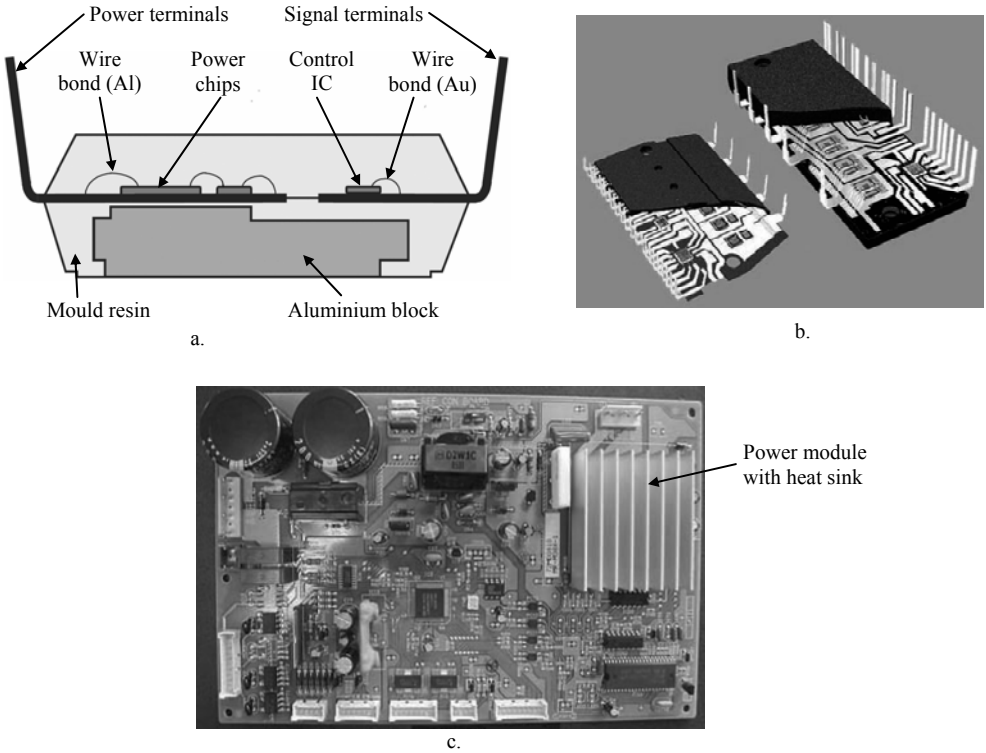


Figure 2-14 Power module on lead frame [Don02] a. Package construction b. Power module c. Complete converter

Insulated metal substrate assemblies

As the power level increases, the dissipation of power components increases, which increases the working temperature of the components. Hence, the standard PCB is replaced with carriers with higher values of thermal conductivity such as Insulated Metal Substrate (IMS) [Ber]. An IMS substrate consists of a copper layer for the circuit's interconnections, thin dielectric layer (75 μm -150 μm) for electric insulation and metal layer (1.6 mm thickness) for heat spreading and mechanical support. The standard construction of an IMS is shown in Figure 2-15a. The insulation layer is a ceramic-polymer blend or FR4 laminate with low thickness, which allows for low thermal resistance of the heat path through the board. The IMS can be mounted onto a metal base plate or directly onto a heat sink. Components in the SMD form are soldered onto the substrate. To reduce the thermal resistance of the heat path, power semiconductors can be mounted in the bare die form directly to the substrate.

Since an IMS substrate is suitable for component mounting on one side only, the component density is low. The IMS substrate is also more expensive than a standard PCB. Therefore, a two substrate solution is usually utilized, where the power part of the circuitry, mainly power semiconductor components, is mounted on the IMS substrate (Figure 2-15b) while the rest of the circuitry is assembled on the PCB (Figure 2-15c). This PCB is mounted on top of the IMS substrate and the two boards are electrically and mechanically connected through a number of pins. The converter can be encased in a plastic cover and potted for protection (Figure 2-15d).

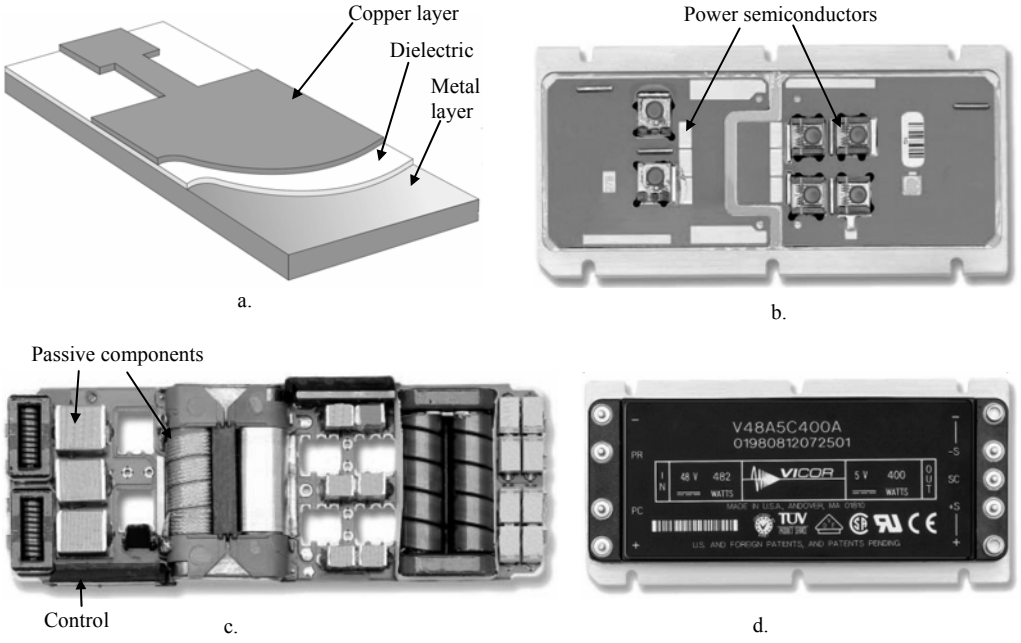


Figure 2-15 Power converter assembly on IMS a. IMS carrier cross-section [Ber] b. IMS with power part of circuitry [Vic] c. PCB with passive and control components d. encapsulated converter

Thick film hybrid assemblies

The thick film process is an additive process by which conductive, resistive and dielectric (insulating) patterns in the form of a viscous paste are screen-printed, dried and fired onto a ceramic substrate (such as Alumina (Al_2O_3)) at an elevated temperature to promote the adhesion of the film. In this manner, by depositing successive layers, multilayer interconnection structures can be formed, which may contain integrated resistors, capacitors or inductors. This is a mature technology, applied in the electronics industry for over five decades. By screen-printing multiple conductor layers, the current handling capability can be significantly increased.

Figure 2-16 Thick film dc-dc power converters [XPM]

The assembly process starts with the manufacturing of the carrier, which includes screen-printing of conductor paste (silver-palladium alloy or copper paste), resistive paste (ceramic/metal alloys) and dielectric paste (barium titanate) on the ceramic substrate. This is followed by the attachment of the semiconductor dies and other components onto the substrate by means of soldering or epoxy attachment. Next, the substrate is soldered onto the base plate. Then, the electrical interconnections from the semiconductors to the substrate tracks and from the substrate to the input and output terminals are established by means of wire bonding. The case is then encapsulated or hermetically sealed by means of welding the lid to the case (Figure 2-16).

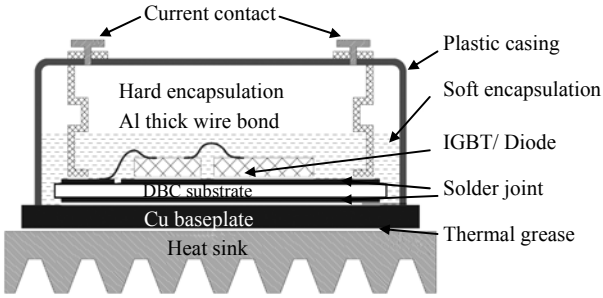
2.5.4. High power level

Direct bonded copper assemblies

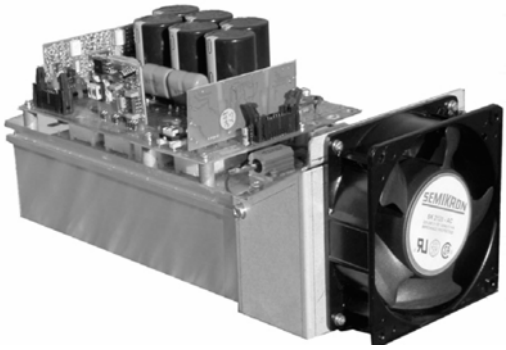
For even higher power levels, highly thermally conductive Direct Bonded Copper (DBC) substrates are employed. DBC consists of a ceramic isolator, Al_2O_3 (Alumina) or AlN (Aluminium-Nitride), onto which solid copper is bonded in a high temperature melting/diffusion process.

Figure 2-17a shows a cross-section of a power semiconductor module built using this technology. The power semiconductor dies are soldered onto the substrate and the substrate is soldered to the base plate. Power terminals are either moulded into the case sides or inserted

after the case is moulded. The next step is interconnecting the circuitry by means of wire bonding. The module is encapsulated with the silicon gel for the purposes of protection. The assembly is finished by inserting a plastic cover. The module's base plate is mounted on the heat sink. The rest of the circuitry, including the passive components, gate drives, control, auxiliary power supplies etc. are implemented on a PCB and mounted on top of the power module (Figure 2-17b.



a.



b.

Figure 2-17 Power converter assembled in DBC technology a. Cross section [Cur] b. complete converter (15 kW) [Sem]

2.5.5. Very high power level

For power converters in the hundreds of kilowatts power range, power modules described in Section 2.5.4 are connected in parallel and series to achieve desired current and power ratings. The power modules are mounted onto a liquid (water or oil) cooled heat sink. Passive components in the discrete form are electrically interconnected to the power semiconductor modules by means of bus bars (Figure 2-18b) or wires. The bus bars can also provide the mechanical support structure for the passive components. The passive components are then mounted on top of the power semiconductor modules or in a cabinet rack for mechanical support (Figure 2-18b). Control electronics, gate drives and auxiliary power supplies are assembled on a number of PCBs and placed in the vicinity of the corresponding power module.

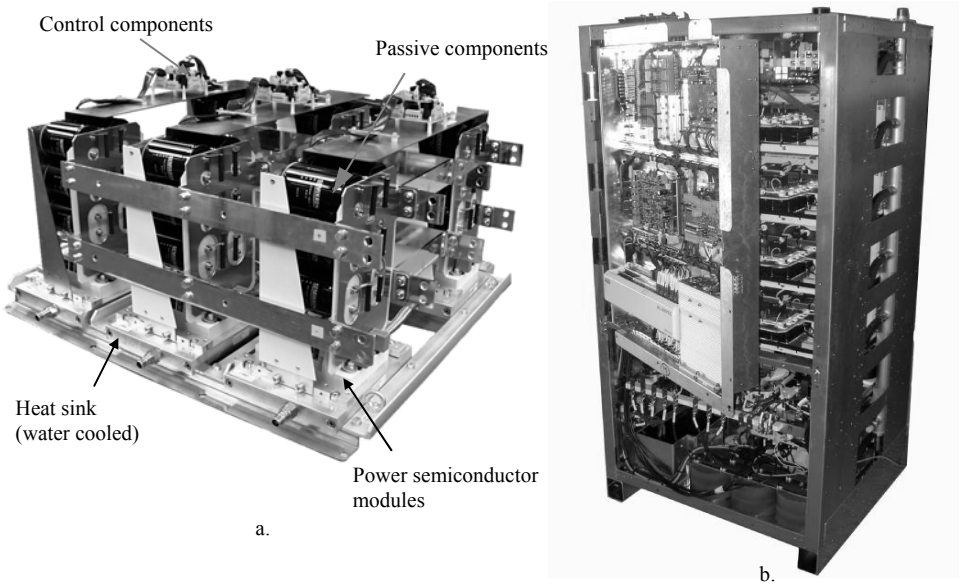


Figure 2-18 Very high power converter assemblies a. Power converter for UPS systems (~ a few hundreds of kW) [Sem], b. Converter for rail vehicles (1 MW) [ABB]

2.6 Summary and conclusions

In this chapter, the main characteristics of the state-of-the-art construction technology of power electronic converters were presented. Section 2.2 discussed some aspects concerning the evolution of the construction technology of electronic assemblies. In Section 2.3, the current approach in designing and constructing power electronic converters was outlined. The main drawbacks of this approach were identified, particularly the large number of construction parts and a design practice that does not optimize thermal and electromagnetic issues.

In Sections 2.4 and 2.5, power electronic components and assemblies were taken apart and their construction parts were identified. The power level of converters was used as the basis for the classification of the circuit packaging technologies. The main point of this breakdown is to show that a typical power electronic converter consists of a large number of constructional parts and requires various manufacturing processes. Some of these parts are components constituents; others are added in the circuit packaging phase. Assemblies with numerous, non-standardized and low functional parts do not satisfy the main principles of design for manufacturing and affect the performance and size of the power electronics converter.

In Chapter 3, a theory that deals with these matters will be presented and an approach to improve the construction of power electronic converters will be introduced.

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Chapter 3: An approach to improving the construction technology of power electronic converters

3.1 Introduction

In Chapter 2, the salient features of the present practice of constructing power electronic converters were described. An overview of components and circuit packaging technologies was also given. The main drawbacks of the present construction technology concerning the ever more demanding requirements of the potential applications on power electronics were identified.

In this chapter, an approach to a better practice of constructing power electronic converters is presented. The large number of construction parts was identified in Chapter 2 as one of the main weaknesses of the present construction technology. Hence, this approach is based on a breakdown of a converter to its construction parts according to the functions they perform. This breakdown is introduced in Section 3.2.

Another drawback identified in Chapter 2 is the existing design practice. Electrical circuit design and converter construction are decoupled and thermal, electromagnetic and spatial issues are engineered in the circuit packaging phase and therefore are not optimized. A new design approach based on elements instead of discrete components and including integral electrical, thermal, electromagnetic and spatial design is introduced in Section 3.3.

In Section 3.4, two important aspects of the construction technology of power electronic converters, integration and packaging, are presented in light of the introduced breakdown and design approach. Some analogies and differences between these two issues in microelectronics and power electronics are discussed.

The chapter is summarized in Section 3.5.

3.2 Converter construction breakdown

In order to deal with the problem of having a large number of construction parts in power electronic converters one has to look deeper than the discrete components that power electronic converters are normally assembled from. In order to achieve this, a power electronics converter is stripped down to its construction parts according to the functions that they perform. Firstly, the functions performed in power electronic converters will be identified.

3.2.1. Fundamental and packaging functions

The main functionality of a power electronic converter is embodied in the following functions [Kre98][Wyk00]:

- Switching function – controls the flow of electromagnetic energy through the converter;
- Electromagnetic energy storage function – provides the continuity of energy when interrupted by the switching function;
- Heat exchange function – provides the exchange of the heat dissipated in the converter with the environment;
- Control/information function – enables the required relationship among the previous functions.

In this thesis, these functions will be referred to as fundamental functions.

On the other hand, there are functions necessary to provide the integrity of the fundamental functions of the converter – i.e. to ensure the proper functioning of the converter. These functions are classified in three categories:

- Functions that provide electrical integrity:
  - Electrical interconnection (providing electrical path for power and signals);
  - Electrical insulation (providing integrity of electrical signals);
- Function that provides thermal integrity – provides heat paths for the dissipated heat from the dissipated part to the heat exchanger in order to ensure that these parts operate in their allowed temperature range;
- Functions that provide mechanical integrity:
  - Mechanical support (provides mechanical support, rigidity, ductility);
  - Environmental protection (provides protection of the parts and assembly from damaging due to handling and environmental effects, especially moisture).

These functions will be referred to as packaging functions.

3.2.2. Functional and packaging elements

Based on the above introduced classification, construction parts in a converter are classified in two categories:

- Functional elements (FEs) – parts that perform one or more fundamental functions;
- Packaging elements (PEs) – parts that perform one or more packaging functions.

Some examples of functional elements are: power semiconductor dies as switching functional elements, IC semiconductor dies as control functional elements, metallized film roll as a capacitive functional element, wire or planar copper conductors and magnetic core as magnetic functional elements. Examples of packaging elements are: semiconductors lead frames and components leads as electrical interconnection packaging elements; encapsulation and housings as protection packaging elements, carrier dielectric as insulation packaging elements, bobbin and lead frames as mechanical support, thermal adhesives as thermal packaging elements etc.

Table 3-1 Typical functional elements

Fundamental function	Functional elements
Switching	power semiconductor die (MOSFET, IGBT, diodes)
Control/information	control semiconductor die
Electromagnetic energy storage	magnetic core magnetic wire and planar copper conductors metallized film foil metallized ceramic layer
Heat exchange	heat sink heat pipes

Table 3-2 Typical packaging elements

Packaging function		Packaging elements	
Electrical integrity	Interconnection	Component level	wire bonds semiconductor lead frames bobbin (pins) leads
		Assembly level	copper tracks via holes copper bus bars pins
	Insulation	Component level	wire insulation
		Assembly level	dielectric carrier (PCB dielectric, ceramic) dielectric tapes, adhesives
Mechanical integrity	Mechanical support	Component level	leads and lead frames bobbin
		Assembly level	circuit carrier base plate bus bars
	Protection	Component level	polymer case (moulded plastic, epoxy coating)
		Assembly level	silicone gel metal housing
Thermal integrity		Component level	cases lead frames
		Assembly level	thermally conductive circuit carrier thermal interface materials

In some cases, determining all the functions that an element performs is not a straightforward process. For e.g. wire bonds perform the electrical interconnection function but they also conduct the heat dissipated by the die and thus contribute to the thermal packaging function. In the case of power semiconductors, the amount of heat that the wire bonds conduct is negligible compared to the heat removed through the main heat path, from the back side of the die through the lead frame or other substrate to the heat sink. However, in signal processing integrated circuits this contribution might be comparable to the other heat paths [NIS]. Hence, when assigning functions to elements, it will be assumed that an element performs a function if the contribution of that element to the function is substantial. The relevance of this condition

will become clear in later chapters, when the evaluation of the level of functionality of elements in a converter is done.
Packaging elements can be classified in packaging levels according to their physical location. The extensive classification of packaging levels can be found in conventional literature on electronic packaging [Bla00]. In this thesis, only two packaging levels will be distinguished:

- Component packaging level – includes packaging elements that are physically part of a self-standing component;
- Assembly packaging level – other packaging elements in a converter.

Wire bonds and lead frames are examples of component level electrical interconnection packaging elements while circuit carrier metallization is an assembly level packaging element. In the case of the mechanical protection function for e.g., polymer coatings and cases are component level packaging elements while the converter's housing is an assembly level packaging element.

Table 3-1 and Table 3-2 give functional and packaging elements on the component and assembly packaging level that are typically found in power electronic converters. In the next section, functional and packaging elements of a power electronic converter case study will be identified.

3.2.3. Functional and packaging elements in a power electronic converter – Case study

Figure 3-1 shows the electrical circuit schematic of a power converter that consists of parts that perform the switching function, control function, electromagnetic energy storage function and heat exchange function. Such a circuit, containing the parts that perform all the fundamental functions, and constructed in the conventional construction technology described in Chapter 2, is chosen to illustrate the introduced construction breakdown [Fer03].

Figure 3-2 shows the functional elements in the converter marked with the corresponding circuit schematic symbols. It should be noticed that each schematic symbol from the circuit diagram is realized in one FE (except for the inductor, which consists of the wire and core). In other words, there are no FEs that implement more than one schematic symbol.

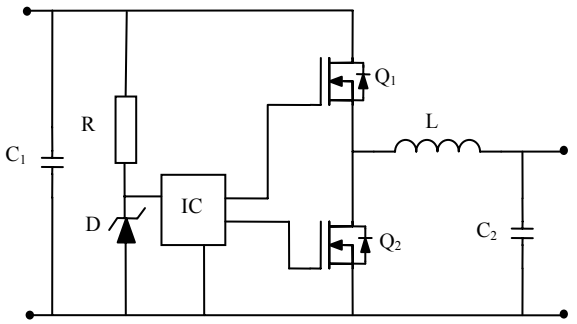

Figure 3-1 Circuit diagram of a power converter

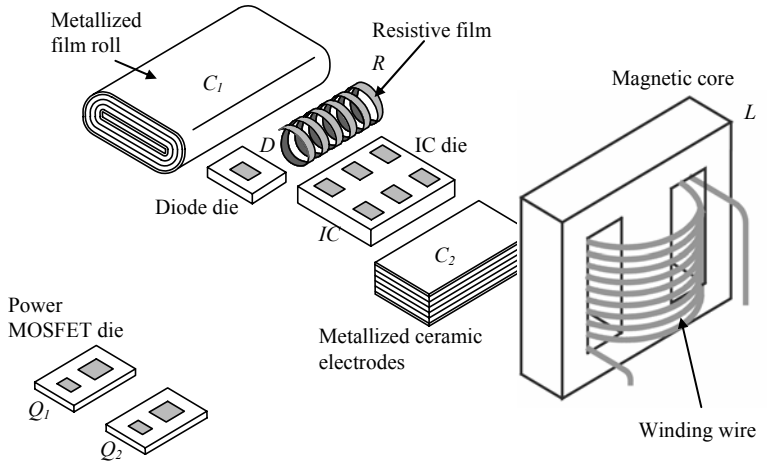

Figure 3-2 Functional elements in the converter

Figure 3-3 shows the fully packaged discrete components consisting of the FEs together with their component level PEs. It can be noticed that all these components, regardless of the function they fulfil, have certain PEs in common. Most of the components make use of leads or solder plated copper wires for electrical interconnection, mechanical support and heat removal. Some sort of polymer coating (epoxy resin, moulded plastic) is used in all the components except the inductor for protection and heat removal. Furthermore, the electrical interconnection between the FEs and the leads is performed by a metal interface (copper plated steel cap, sprayed metal). The mechanical support and insulating function in the inductor is carried out by the plastic winding supporting spool (bobbin). The electrical interconnection between the inductor wire as a functional element and the rest of the circuitry is performed by the bobbin's metal pins. For insulation purposes, the winding wire is coated with polymer. In the control IC case, the interconnection function is performed by metal wire bonds and etched or stamped supporting copper sheet (lead frame), which also gives the mechanical support and serves as a heat removal path.

It will be assumed that the power level of the converter is such that the circuit packaging technology described in Chapter 2, Section 2.5.4 is employed. The components are split up in two groups according to the amount of heat that they produce. Thus, the high loss density power MOSFET dies with the heat sink and highly thermally conductive Direct Bonded Copper (DBC) ceramic substrate, which performs the electrical interconnection, heat removal, insulation and mechanical support functions, represent one sub-assembly (Figure 3-4). The rest of the functional elements in the form of discrete components are assembled on a low thermal conductivity standard epoxy-based PCB for interconnection, insulation and mechanical functions. These two sub-assemblies are connected with the pins for electrical interconnection and mechanical support, protruding from DBC to PCB to make the complete circuitry as shown in Figure 3-5.

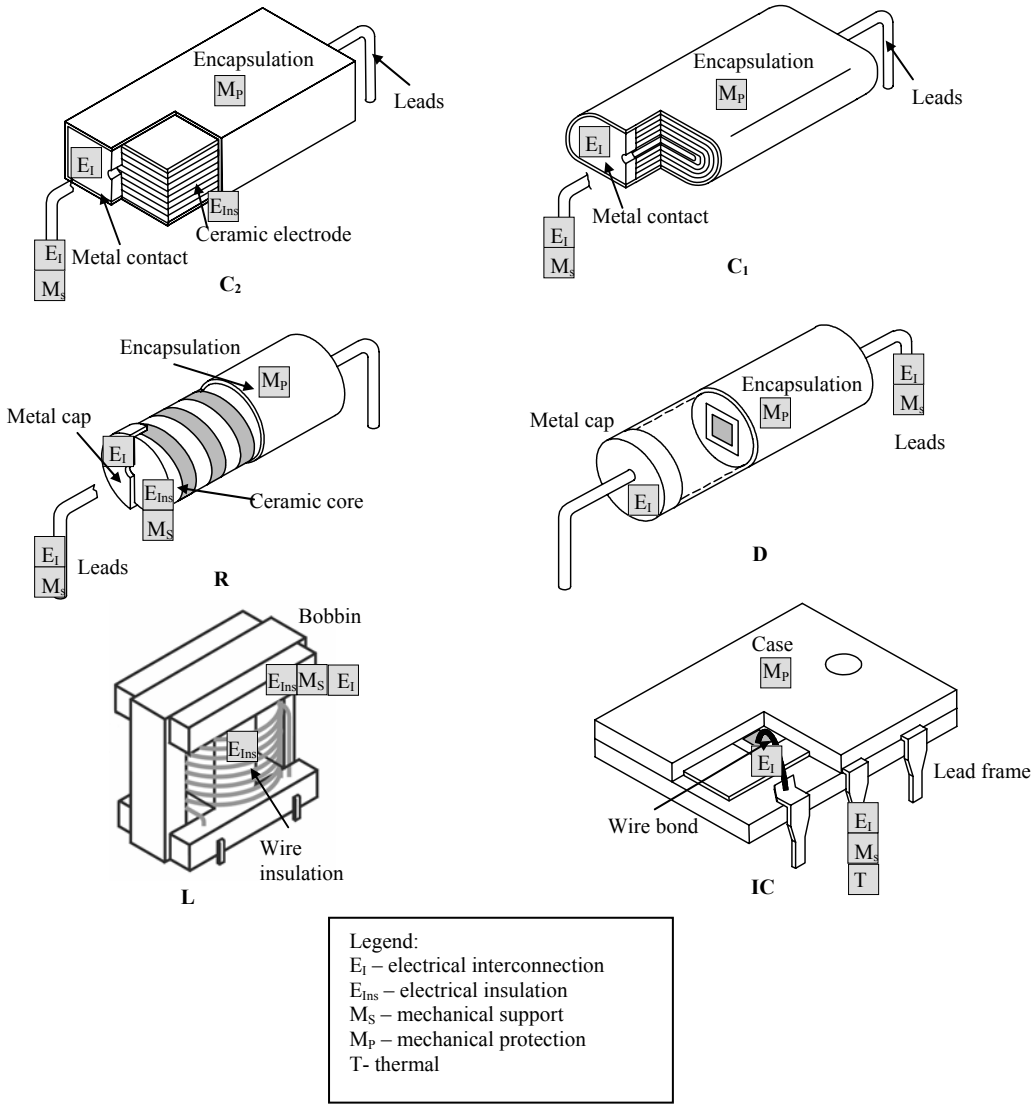

Figure 3-3 Packaging elements of the converter's discrete components

It can be noticed that the power semiconductors are used in the bare form, which significantly reduces the number of their PEs compared to the fully packaged discrete components. All the packaging functions are carried out on the assembly level by packaging elements (ceramic substrate for e.g.) that are multifunctional (insulating, mechanical support, interconnection function) and shared among a number of FEs (in this case two). On the other side, each of the fully packaged discrete components used in the control and energy storage parts has its own PEs for each packaging function. For example, the control circuit IC's – power MOSFET gate electrical interconnection function is performed by the whole sequence of packaging elements:

IC's wire bonds, lead frame, copper tracks on the PCB, pins, copper conductors on DBC and finally power MOSFET's wire bonds.

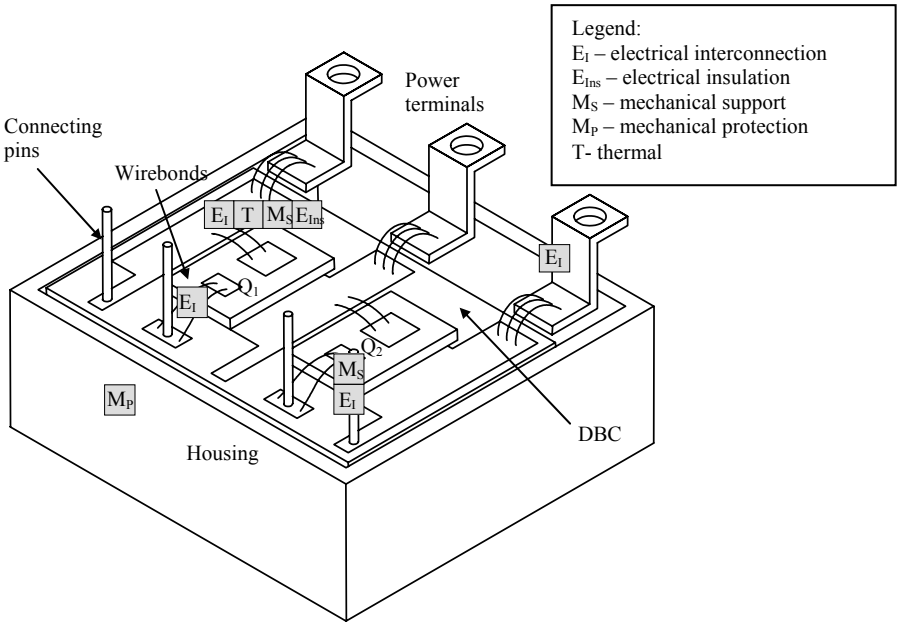

Figure 3-4 Power module packaging elements

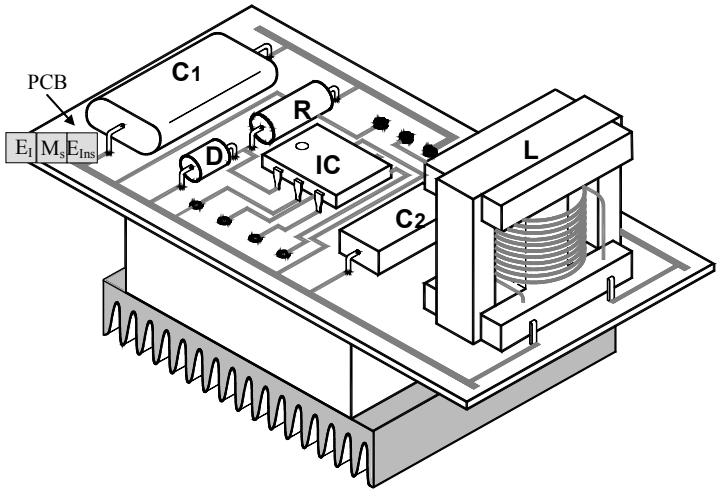

Figure 3-5 Complete assembly

The total number of FEs in the converter is 9: metallized ceramic electrodes, metallized film roll, winding wire, magnetic core, resistive film, diode die, IC die and two MOSFET dies. The total number of packaging elements is 24. The PEs on the component level are the capacitor's C_2 encapsulation, leads and metal contact; capacitor's C_1 leads, metallization and

encapsulation; winding wire insulation, bobbin, resistor's ceramic core, encapsulation, metal cap and leads; diode's encapsulation, metal cap and leads; IC's case, lead frame and wire bonds. The PEs on the assembly level are the DBC carrier, pins, wire bonds, power terminals and power module housing and PCB carrier.

3.3 Element based integral design approach

It was pointed out in Chapter 2 that the conventional design approach shown in Figure 3-6 does not deal with the thermal and electromagnetic issues in the function optimization phase. Also, the spatial design, important for minimizing the volume and achieving high power densities, is not dealt with in this phase. Furthermore, the large number of parts was identified as a drawback concerning both manufacturing and assembly issues and electrical, thermal, electromagnetic and spatial performance.

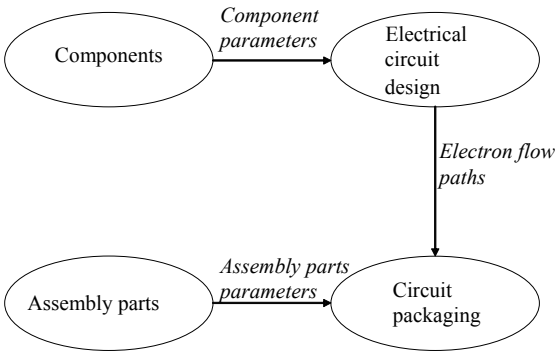

Figure 3-6 Conventional design of power electronic converters

A modified design approach based on functional and packaging elements instead of discrete components and including electromagnetic, thermal and spatial design in the function optimization is shown in Figure 3-7. Two domains can be identified in the figure: functional domain (fundamental and packaging functions design) and physical domain (FEs and PEs).

FEs and fundamental functions design are linked by electrical, thermal, electromagnetic and spatial parameters of FEs in one direction and the fundamental functions design outputs (electrical circuit schematic, heat paths, electromagnetic field distribution, spatial design) in the other direction. PEs and packaging functions are linked by PEs parameters (electrical, thermal, mechanical) and the packaging functions design outputs that are derived from the fundamental functions design outputs and input specifications of the converter (mechanical, environmental etc.).

Integral fundamental functions design

Electrical, thermal, electromagnetic and spatial parameters of functional elements are inputs in the fundamental function optimization phase. Figure 3-7 shows this phase as an interlinked electrical, thermal, electromagnetic and spatial design. [Ger05] delves into interdependencies between electrical, thermal and spatial design and shows that in order to achieve high power

densities at high operating temperatures, a power electronic converter must be designed in an integral manner. The choice of the circuit's electrical design, such as the topology, switching method and component number, determines the losses in the converter. On the other hand, the losses in the converter and the heat exchange function design influence the spatial design of the converter. The storage of electromagnetic energy requires volume and thus affects the spatial design.

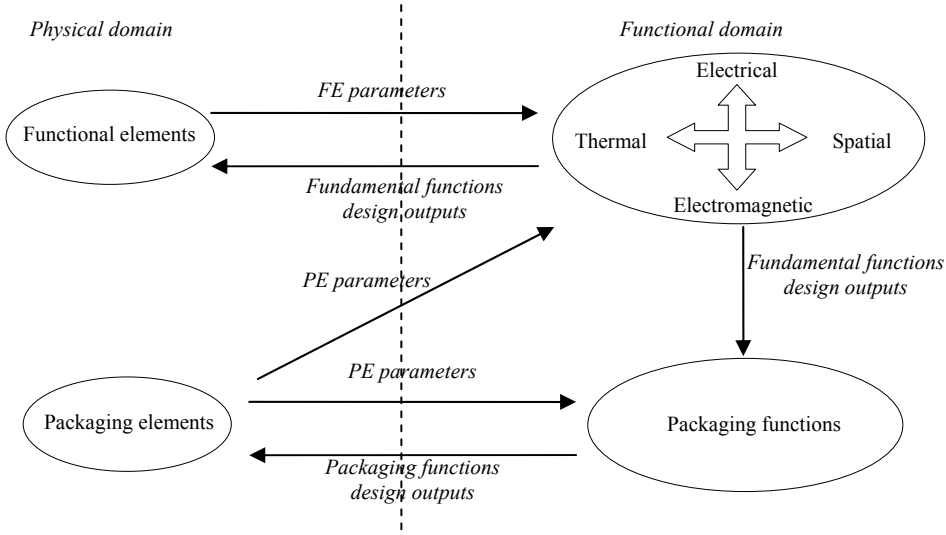

Figure 3-7 Element based integral design approach

In a manner similar to that used for the optimization of the electrical circuit, the *thermal circuit* can be designed and optimized. Powerful CAD software implementing various methods for thermal analysis such as closed form Fourier series solution, thermal network method, finite difference and finite element simulations [Bar93] can be used for thermal circuit analysis and optimization. Furthermore, electrical and thermal circuit optimization can be performed simultaneously using the electro-thermal network method [Hef93]. This method combines electrical and thermal circuit network, implementing the thermal circuit network in already existing electrical circuit simulators, allowing for an interactive electrical and thermal circuit design.

[Fer89] shows how *electromagnetic modelling* and optimization of electromagnetic energy flow can be performed using energy flux or Poynting vector theory. In this reference, an algorithm to model structural impedances of electrical interconnections in converters is derived. In order to analyze the conducted EMI performance of the converter it is essential to model parasitic elements in the circuit [Zha98]. Finite element analysis or Partial Element Equivalent Circuit (PEEC) methods are used to extract circuit parasitic elements and circuit theory software tools (such as Saber) are used to simulate the conducted EMI performance.

By including *spatial design* in the function optimization phase, smaller volumes of FEs, PEs and the converter as a whole can be achieved for the same performance [Ger02].

The integral design methods are generally performed by iterative software interactions among the separate function designs and are beyond the scope of this thesis. The initial efforts including integral electrical, thermal and spatial design of power electronic converters are documented in literature [Che01] [Ger05].

Links between the functional domain and physical domain

The outputs of the functional domain are physically realized by means of FEs and PEs. The implementation of FEs and PEs makes use of a number of disciplines, such as component technology, material technology, manufacturing technology etc. While in the conventional design approach the function optimization and physical construction phase were decoupled, the functional and physical domain in the new approach continuously interact with each other throughout the converter design.

Thermal function and physical domain: Contrary to the electrical function where electrical interconnection PEs are generally not included in the electrical function optimization phase, thermal interconnection PEs have to be dealt with in the thermal function optimization. Thermal management is largely dependent on material properties and interfaces of thermal PEs, geometrical design variable and layout [Fer02]. The reason for this, expressed in electrical and thermal network terminology, is that thermal PEs exhibit much higher thermal resistance relative to electrical resistance of their electrical packaging counterparts. This results in considerable temperature-drops over thermal PEs. Furthermore, due to the differences in orders of magnitude in “insulation” and “conduction” in the electrical and thermal world, the heat flow is much less one-dimensional than the electrical current flow [Ros97] hence there is often more than one heat flow path that has to be taken into account.

Electromagnetic function and physical domain: For an optimal design concerning circuit parasitic elements and electromagnetic interference (EMI) issues, electrical interconnection PEs, being an important issue in power converters especially as the operating switching frequency increases, must be included in the function optimization. They are strongly dependent on the converter spatial layout and physical realization. Due to the nature of the effects they cause, they represent part of electromagnetic function optimization.

Furthermore, electromagnetic modelling and simulations can be used to optimize the electromagnetic energy storage FEs reducing the FEs volume by integrating more functions into the same volume, which in turn reduces the volume of the electrical interconnection PEs. This is especially important when their relative volume increase with frequency [Fer01] is taken into account. The electromagnetic models of the FEs are related to the geometrical design variable, which again brings the physical domain and function optimization together.
Given the above reasoning, the physical and functional domain in the converter design can not be decoupled and treated sequentially. This is even more pronounced when an integral electrical, thermal and electromagnetic design is undertaken and when it is considered that FEs and PEs are not necessarily off-the-shelf pre-manufactured elements but can be designed to suit the application.

In the following section, the important aspects of construction technology, integration and packaging will be approached in terms of the presented design approach and construction breakdown.

3.4 Packaging and integration

Packaging and integration are recognized as two important aspects of power electronics technology. Both exhibit a lack of preciseness in the used terminology in literature. As they will be used extensively in this thesis, let us first clarify and define them in terms of the proposed construction breakdown and design approach.

3.4.1. Packaging in power electronics

The term "packaging" is often loosely used in power electronics. Packaging mostly refers to connecting semiconductor devices to the outside world, a meaning which is inherited from microelectronics packaging and must be modified in the power electronics world given that a power electronic converter typically contains a large diversity of components of which passive components present a significant part.

Let us start from the commonly accepted definition of electronic packaging [Har93]:
"Electronic packaging is the engineering discipline that combines the engineering and manufacturing technologies required to convert an electrical circuit into a manufactured assembly".
This definition corresponds to the conventional design approach explained in Section 3.1. In this approach, packaging is performed on two levels. The first level is packaging of discrete components. This packaging level is described in Chapter 2. It is not distinguished as a separate phase in Figure 3-6 since it is performed by component manufacturers and generally not accessible by a power electronics engineer. The second level is designated as circuit packaging and includes using assembly parts, interconnection and layout technologies to convert a group of discrete components into a power electronic converter according to the output of the function optimization phase, which is, as already noted, a circuit schematic diagram.

Following the new design approach that includes thermal and electromagnetic design into the function optimization phase, the above definition can be modified to suit better the nature of power electronics [Pop05]:
"Power electronics packaging is the combination of engineering and manufacturing technologies required to convert an electrical and thermal circuit as well as electromagnetic design into a manufactured assembly".

In this approach, packaging is performed on the assembly level and includes using PEs to convert the FEs set into a power electronic converter according to the outputs of the fundamental function optimization (electrical circuit schematic, thermal circuit schematic and electromagnetic energy flow).

In Figure 3-7, packaging deals with the PEs in the physical domain, packaging functions in the functional domain in the following ways:

- Choosing technologies for implementing PEs that will perform packaging functions according to the outputs of fundamental functions design;
- Analyzing the behaviour of the PEs that influence fundamental functions and designing them accordingly;
- Analyzing the packaging functions performance and designing the PEs accordingly.

Packaging generally does not change or modify functional elements except in certain cases that will be discussed in later chapters.

The packaging functionality can be illustrated in the example of realizing the electrical interconnections in a power electronic converter. The output of the electrical function design is an electrical circuit schematic. Next, electrical interconnection packaging elements are chosen in a technology that suits the converter specifications – for e.g. PCB tracks for low to medium power level. Afterwards, the layout parasitic parameters for the EMI behaviour as well as the thermal behaviour, such as heat spreading in the PCB tracks and heat paths to the ambient or heat sink, should be analyzed in the electromagnetic and thermal fundamental functions domain. Then the packaging functions are analyzed and additional PEs are added, for e.g. the whole converter can be encapsulated for protection.

The foregoing procedure is iterative rather than sequential, since, as already discussed and illustrated in Figure 3-7, the fundamental functions are dependent on each other, the packaging functions influence the fundamental functions and the functional domain as a whole is strongly related to the physical domain. For example, by modifying the spatial layout in order to optimize the EMI behaviour, the thermal behaviour will change. If the change in the thermal behaviour results in a situation where the FEs and PEs do not operate in their allowed temperature range, the layout and/or material properties have to be modified, which in turn affects the EMI behaviour. Furthermore, concerning the mechanical protection function, the physical properties of the PE (encapsulation for e.g.) such as permittivity, permeability and thermal conductivity might influence the EMI and thermal behaviour of the assembly.

3.4.2. Integration in power electronics

As described in Section 3.2, the proposed converter construction breakdown and design approach are based on construction parts of a power electronic converter and the functions that they perform. Based on this breakdown we can translate integration of functions into physical structures. By integrating functions of two or more parts into one part, reduction in cost and size is expected due to less material used, fewer manufacturing processes and simplified assembly [Suh90]. Following Figure 3-7, integration occurs in two domains [Pop05]: integration in the physical domain and integration in the functional domain.

Integration in physical domain

In the physical domain, integration can be classified, according to the type of elements that are the subjects of integration, in two groups – *functional elements integration* and *packaging elements integration*.

Functional elements integration

Functional elements integration occurs when a number of functional elements are substituted with one that performs the same fundamental functions. [Waf02] classifies this type of integration in two groups – integration technologies where a number of discrete devices are made in one process and integrated devices, where different functions are integrated into one device.

Examples of functional elements integration are:

- Integrated devices:
  - Monolithic integration where the whole circuit is integrated into one device;
  - Electromagnetic integration of passives [Hof00] where passive components, such as inductor, capacitor and transformer are integrated into one device (Figure 3-8a);
- Integration technologies:
  - PCB embedded passives technology where passive components such as resistors, capacitors and magnetic components are realized in laminates that can be laminated in the standard multilayer PCB process with the rest of the circuitry as in Figure 3-8b;
  - Thick film and Low Temperature Co-fired Ceramic (LTCC) technology where passive components such as resistors and capacitors are manufactured by means of screen printing on a ceramic substrate.

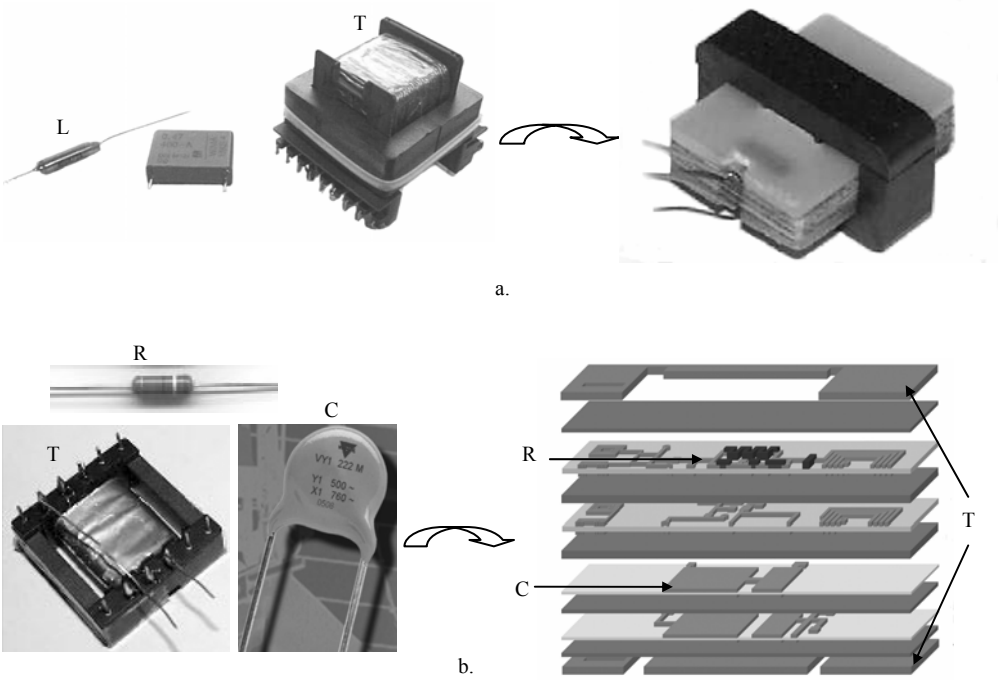

Figure 3-8 Functional elements integration a) integrated device b) integration technologies [Waf02]

The potential benefits of functional elements integration are:

- Reduction of the number of parts, not only FEs but also PEs since there are fewer functional elements to serve;
- Fewer manufacturing processes since there are fewer parts to fabricate;
- Fewer assembly steps since there are fewer parts to connect;
- Size reduction;
- Better performance due to lower parasitic values.

Packaging elements integration

Packaging elements integration occurs when a number of packaging elements are substituted with one that performs the same packaging functions. It can be implemented by integrating a number of FEs in one package, where they share the same packaging elements, such as the housing, mechanical support, thermal paths etc. This type of PEs integration is found in Multichip Modules (MCM), power modules, integrated resistive networks etc.

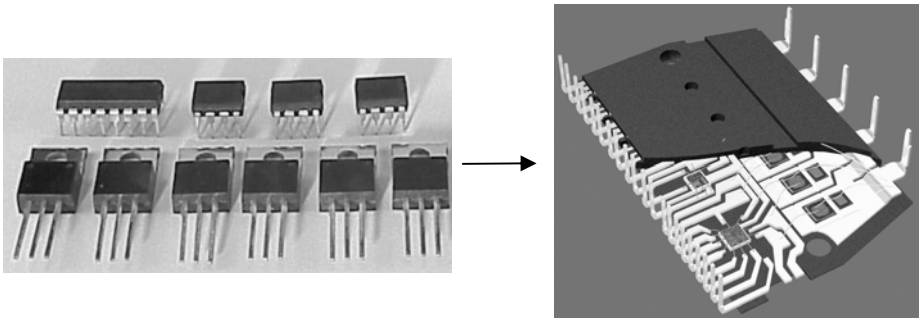

Figure 3-9 Packaging elements integration – power module on lead frame [Iwa01]

Figure 3-9 shows a power module that includes a number of power semiconductors and control integrated circuits assembled on a common lead frame [Iwa01]. In this case, the electrical interconnection, and thermal and mechanical support PEs of the discrete components are integrated into one – the lead frame. Furthermore, the protection PEs of the discrete components are integrated into the injection-moulded encapsulation in the power module.

The potential benefits of packaging elements integration are:

- Reduction of the number of parts, primarily PEs, since PEs integration generally does not influence FEs;
- Fewer manufacturing processes since there are fewer parts to fabricate;
- Fewer assembly steps since there are fewer parts to connect;
- Size reduction;
- Better performance due to lower parasitic values.

Figure 3-10 illustrates the two types of integration. FEs are represented by patterned rectangles. Different patterns in FEs represent different manufacturing processes involved in manufacturing of the part. PEs are represented by hollow rectangles. The conventional approach, as already discussed, uses discrete components that each consists of one FEs and a

number of PEs. In the case of packaging elements integration, the number of FEs remains the same but benefits are in the reduction of the number of PEs. As for functional elements integration, integration technologies still have discrete FEs but these FEs are made in the same manufacturing process. Finally, integration of devices results in one functional element.

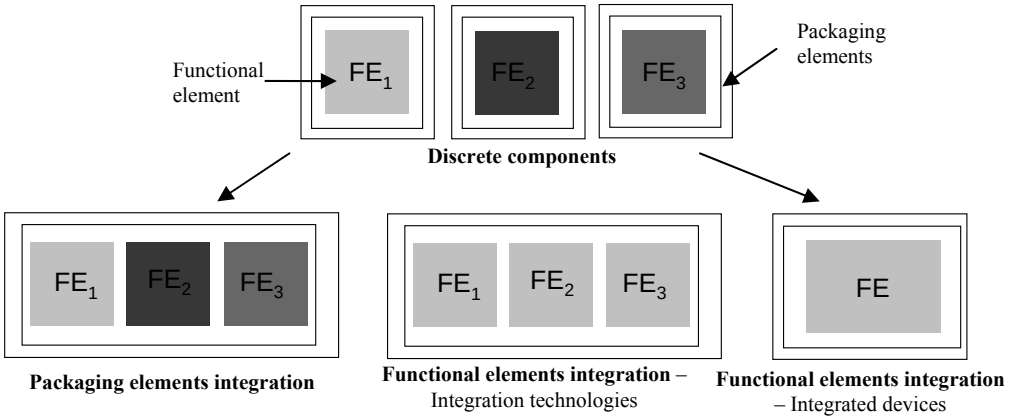

Figure 3-10 Functional elements integration vs. Packaging elements integration

Integration in functional domain

In the functional domain, integration can be classified on the basis of the fundamental function that is the subject of integration: electronic circuit integration, electromagnetic integration and thermal circuit integration.

Electronic circuit integration

Electronic circuit integration implies integration of FEs that perform switching and/or control and information functions. Monolithic integrated control circuits (Figure 3-11a) have been used in power electronics for decades. Control circuits and low power semiconductor devices can be integrated in one monolithic integrated circuit, mostly referred to as "smart power" (Figure 3-11b) [Bal91][Inf].

Electrical interconnection PEs can also be integrated, as in the case of the power module on a lead frame in Figure 3-9.

Electromagnetic integration

Electromagnetic integration implies the integration of FEs that perform the electromagnetic energy exchange function [Hof00]. An example of this type of integration is shown in Figure 3-8, where an inductor, capacitor and transformer are integrated into a single component.

PEs that serve electromagnetic FEs can also be integrated so that a number of FEs are packaged into a single housing. [Ger02] shows how the volume of a low pass filter can be reduced if the inductor and capacitors share the packaging elements for mechanical support, electrical interconnection and heat removal.

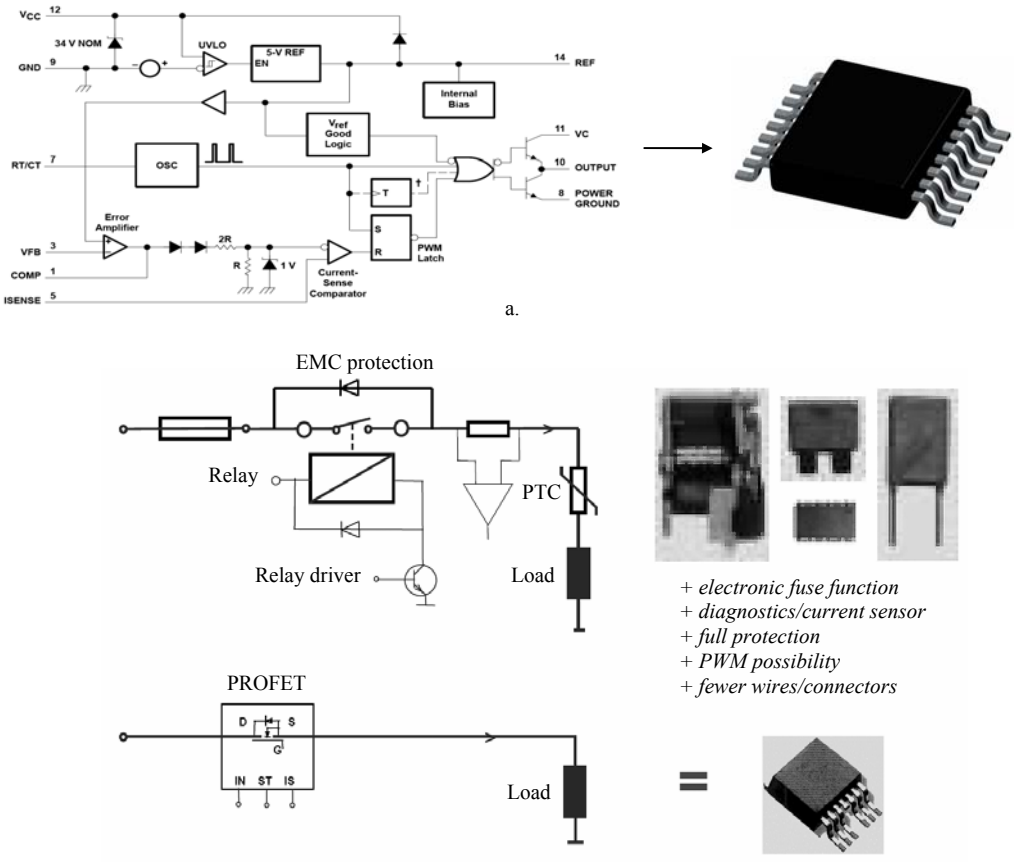

Figure 3-11 Electronic integration: a. PWM controller [Tex] b. Integrated switching, control and information circuit [Inf]

Thermal circuit integration

Thermal circuit integration implies integration of FEs that perform the heat exchange function. In microelectronics this may be done by monolithic integration of a micro-channel heat sink in a silicon device [Per98]. This is not feasible for power devices since both sides of a silicon die are metallized for electrical connections. Hence, a power device is brazed onto a micro-machined heat sink [Gil99]. Furthermore, common thermal FEs (heat sinks, fluid heat exchangers) can be used for cooling of both the power electronic converter and other sub-systems (e.g. electrical machines) achieving integration on a higher, system level.

Furthermore, instead of using separate thermal PEs for each component, thermal PEs can be integrated into a structure that serves more than one FE in the same way that a lead frame serves to connect multiple semiconductor FEs to the outside world. [Fer02] shows how this concept can be used to package both passive and active FEs in order to achieve high power densities in DC/DC converters for automotive applications (Figure 3-12).

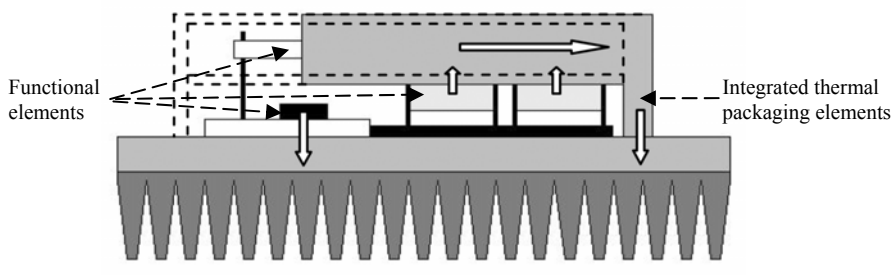

Figure 3-12 Thermal circuit integration of packaging elements [Fer02]

3.4.3. Microelectronics vs. power electronics integration and packaging

The invention of the Integrated Circuit some five decades ago revolutionized the world of electronics. It became possible to implement the whole electronic circuit, consisting of transistors, resistors, capacitors and the connecting wiring onto a single crystal made of semiconductor material. The cost of electronic functions was reduced by a million to one. Integrated circuit technology made possible the integration of CPU, memory and input and output controls onto a single chip, thus making the first microprocessor. The number of transistors on a single chip has been increasing exponentially over the years, following Moore's law [Moo65]. Modern microprocessors hold a few hundred million transistors [Int].

Despite this enormous revolution in electronics that allowed for the implementation of entire electronic circuits onto a single sliver of semiconductor, in today's products there is still a large number of discrete components present next to integrated analogue and digital circuits. There are a number of reasons why the whole microelectronic systems, including analogue, digital and RF circuits, are not realized on a single piece of silicon (or other material). One of the most important reasons is the increased cost due to the increased design complexity, the setting up of a new production line and the long time to production that is often unacceptable for fast-changing markets. The processes of manufacturing some types of integrated circuits are more costly than the others, for e.g. cache memory built into a processor is much more expensive then the RAM memory chips. Another reason is the poor performance of passive components integrated in silicon, especially in RF and high-speed applications. Electrical interconnections implemented on silicone chips represent one of the limits on the chip's performance as the chip's functionality increases [Key01]. Furthermore, individual characteristics of different functional blocks in a system, such as the physical size of optic lenses or RF transmitters, preclude them from being integrated on a single chip [Hub02].

In general, fully integrated solutions are superior in terms of size, reliability, assembly cost and speed. A recent trend in microelectronics, in which analogue, digital and RF circuits are implemented on a single chip, is referred to as System-on-Chip (SoC). However, for all the abovementioned reasons, integrating the whole system on one chip might not be the optimal solution for some cases. In those cases, a number of separate dies (and surface-mounted passive components) are packaged together in a single package, using advanced, often three-

dimensional (3D) stacking techniques, where chips are mounted on top of each other and electrically interconnected. This packaging technique is referred to as System-in-Package (SiP). It offers more freedom in design, faster time to market and often a cheaper manufacturing process of separate dies compared to the single-die solution. These benefits come with the price of a more complex assembly process.

The main difference between power electronics and signal electronics is that power electronics processes energy with high efficiency while signal electronics processes information with minimum amount of energy. However, they have a number of common attributes [Lee02]: fundamental electromagnetic limits, thermo-mechanical limits, material limits and the ever-increasing demand for lower cost. The question that naturally arises is why power electronics has not seen size and cost reductions and performance improvements on the scale seen in microelectronics with the invention of the integrated circuit.

While microelectronics by integration and miniaturization achieved a reduction of energy needed per logic operation by several orders of magnitude in the past few decades [Key01], the levels of energy that power electronics converters have to process have constantly been increasing due to the increased power demand of power electronics loads. This poses different requirements on construction technologies of power electronic and microelectronics circuits.

The limits on integration are even more pronounced in power electronics then in microelectronics. Considering the fundamental functions of a power electronic converter, some requirements regarding functional elements can be derived. For the electromagnetic energy storage function, a certain volume of functional elements is needed together with dielectric and magnetic properties of the materials. Considering the switching function, functional elements with controllable impedances are needed. For the control/information function, functional elements capable of signal processing are required. For the heat exchange function, functional elements with high thermal conductivity are needed. Therefore, monolithic silicon integration technology that has revolutionized microelectronics is not suitable for realizing all the fundamental functions in power electronics.

However, the same principle of balance between integration and packaging that is observed in microelectronics can be applied to power electronics. In microelectronics, integration is pushed as far as feasible, while various constraints such as fundamental limits, performance and cost have to be taken into account. Once these limits are reached, when it is not feasible to integrate more functionality onto a single chip, a number of chips and passive components are packaged together into a single package. In power electronics, expressed in the introduced terminology, functional elements integration should be pushed as far as possible, taking into account requirements of different functions and partitioning the circuitry accordingly. When fundamental, material, manufacturing or economic limits of functional elements integration are reached, packaging elements integration takes over. By designing PEs in a smarter way so that they perform more functions and are shared among a number of FEs, the total number of parts and assembly processes in the converter can be significantly reduced.

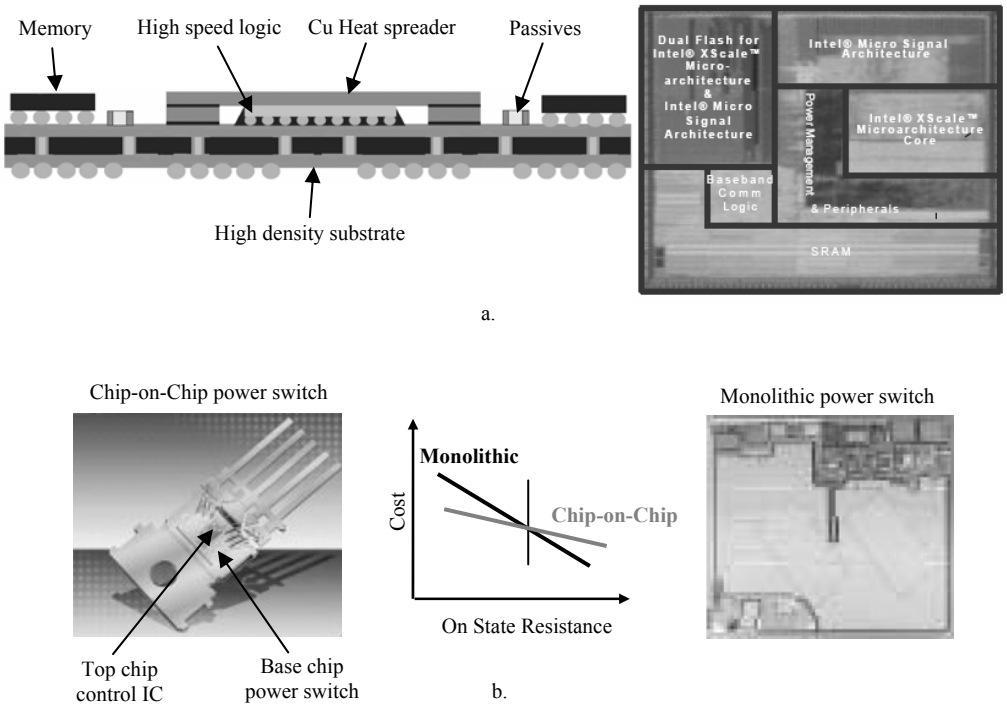

Figure 3-13 a. System in Package vs. System on Chip (Cellular processor) [Amk] [Int] b. "Chip on chip" vs. Monolithic power switch [Inf]

Figure 3-13 illustrates this analogy. Figure 3-13a shows a system-in-package that includes ASIC, memory chip and passive SMD components in one package and a system-on-chip processor for cell phones where the whole functionality is integrated in one chip. Figure 3-13b shows a counterpart example in power electronics, a "smart" power switch, i.e. power switch with some control and diagnostic electronics implemented in two ways [Inf]. The first is a monolithically integrated chip where all the circuit symbols are implemented in one FE (FE integration). The second option is "chip-on-chip" where the logic chip, realized in complex CDMOS technology, is stacked on top of the power switch, realized in inexpensive DMOS technology, in a single package. This is an example of PEs integration since PEs are shared between two discrete chips. Figure 3-13b also shows the cross point in the on-resistance value of the MOSFET where the cost of the monolithic option becomes more expensive than the "chip-on-chip" option since the size of the chip becomes larger and the whole chip is implemented in the expensive CDMOS technology. This cross point is where FEs integration reaches its limits and PEs integration takes over.

3.5 Summary

In this chapter, an approach to improving the construction technology of power electronic converters was introduced. In Section 3.2 power electronic converters were taken apart down to their construction parts on the basis of the functions they perform. In order to satisfy the

requirements set for power electronics by the system level, a new design approach based on functional elements and packaging elements instead of discrete components and integral electrical, electromagnetic, thermal and spatial design was proposed in Section 3.3. The relationship between the physical domain and functional domain in this approach was also discussed in this section. In Section 3.4, two important aspects of construction technology, packaging and integration were presented in light of the construction breakdown and new design approach. Packaging deals with PEs and packaging functions, while integration deals with increasing the functionality of both FEs and PEs. Some analogies between integration and packaging in microelectronics and power electronics were drawn in Section 3.4.3 and the balance between FEs integration and PEs integration was discussed.

In Chapter 4, the level of FE integration and PE integration in power electronic converters will be evaluated by means of two quantities that will be introduced: FE integration level and PE integration level. Formal methods that allow for increasing the level of integration will be derived from these quantities. These methods will then be embodied by using integration technologies that will be presented in Chapter 5. The means to merge the methods with integration technologies into a design process whose bases are laid out in this chapter in order to implement them in actual converters will be presented in Chapter 7. This chapter introduces an approach that will be used as the basis for improving the construction of power electronic converters, something that will be described in the chapters that follow.

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Chapter 4: Increasing the level of integration in power electronic converters

4.1 Introduction

In Chapter 3, a breakdown of the physical construction of power electronic converters was introduced. Two types of converter construction parts were identified on the basis of the function they perform: functional elements and packaging elements. Based on this breakdown, two types of integration were classified: functional elements integration and packaging elements integration.

In this chapter, methods to increase the level of integration in power electronic converters are devised. Section 4.2 starts off the chapter with the discussion on integration level. The definitions of corresponding quantities in microelectronics related to monolithic and hybrid integration are given. This is followed by the introduction of two quantities that evaluate the level of functional and packaging elements integration in power electronics. In Section 4.3 and Section 4.4, a number of methods to increase the level of functional elements integration and packaging elements integration, respectively, are introduced and illustrated with examples. Section 4.5 shows how these methods can be combined with each other to further increase the level of integration.

In Section 4.6, some limits in increasing both level of integration are discussed. Circuit partitioning as a means of achieving an optimal level of integration is discussed. Furthermore, the consequence of partitioning on the level of integration is considered.

The chapter is summarized in Section 4.7.

4.2 Integration level

Since integration brings the benefits discussed in Chapter 3, the term “level of integration” is widely used in characterising electronic systems to emphasize their advantages. Yet, this term is used to reflect different phenomena for different types of integration. In order to derive quantities that will quantify the level of functional and packaging elements integration in power electronics, the commonly used definitions of integration level in different areas in microelectronics are reviewed first.

4.2.1. Integration level in microelectronics

There are two main types of integration in microelectronics: monolithic integration and hybrid integration. Let us take a look at the definitions of integration level related to these two integration types.

Monolithic integration level

Monolithic Integrated Circuit is defined as a combination of interconnected circuit elements formed in situ upon or within a semiconductor substrate with at least one of the elements formed within the substrate [Mei67].

Integration level in monolithic integration is defined as the number of transistors per chip or per area unit. Since the invention of the Integrated Circuit, this level has been following a trend of doubling every couple of years, commonly referred to as Moore's law, illustrated in Figure 4-1 [Moo65]. In the latest generation of computer processors, this level has risen to around a few hundred million transistors in a chip.

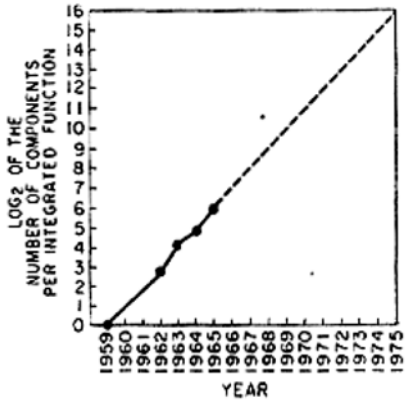


Figure 4-1 Integration level in microelectronics (Moore's law) [Moo65]

Hybrid integration level

A Hybrid Integrated Circuit is defined as a combination of interconnected circuit elements inseparably associated on a common substrate consisting of two or more integrated circuit types or one integrated circuit type and a discrete element [Mei67]. The most widely used hybrid integration technologies are thick film and thin film technologies.

In the case of hybrid integration, integration level is defined as the number of unpackaged components in a hybrid microcircuit package or per area unit.

4.2.2. Functional and packaging elements integration level

From the two definitions presented above it can be concluded that both monolithic and hybrid integration levels represent the number of electrical circuit schematic symbols implemented in one functional element or one package.

Following the same reasoning, two quantities to describe and evaluate the level of functional and packaging elements integration in power electronic converters are defined in the next subsections [Pop05a]. The quantity that describes the level of functional elements integration is referred to as the *functional elements integration level* whereas the quantity that evaluates the level of packaging elements integration is referred to as the *packaging elements integration level*.

Functional elements integration level

Let us first introduce the term *virtual functional element*. In the discrete approach, each electrical circuit schematic symbol in the functional domain is represented by one functional element in the physical domain. The basic idea behind integration is to implement more functions or in this case more circuit schematic symbols into one element. Hence, a functional element that contributes to the physical realization of *n* circuit symbols is "worth" *n* virtual functional elements.

In order to evaluate the level of multifunctionality of FEs in a complete converter or sub-assembly, a quantity *Functional elements integration level* (K_I) is defined as:

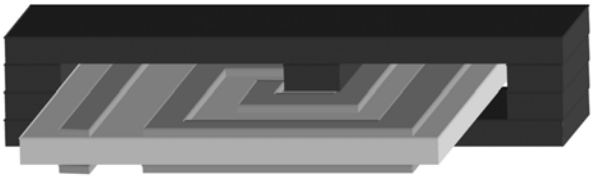
$$K_I = \frac{\sum_i N_{FEv_i}}{N_{FE}} = \frac{N_{FEv}}{N_{FE}} \tag{4.1}$$

where N_{FE} is the total number of functional elements in the sub-assembly, while N_{FEvi} is the number of virtual functional elements that the functional element *i* is worth. N_{FEv} is the total number of virtual functional elements in the converter.

Figure 4-2 illustrates the meaning of this quantity on an example of a planar integrated LC structure. The metallized ceramic dielectric in this structure represents one functional element (Figure 4-2) but it takes part in two circuit schematic symbols: inductance (windings) and capacitance (electrodes and dielectric), hence this element is worth two virtual functional elements.

In order to obtain the value of the functional element integration level of the whole sub-assembly, the other functional elements have to be taken into account, in this case the ferrite core. The magnetic core performs the magnetic field shaping and contributes to the inductance circuit symbol only, hence its number of virtual functional elements is 1. By substituting these values into (4.1) the value of the functional elements integration level in the sub-assembly can be obtained:

$$K_I = \frac{N_{FEv}}{N_{FE}} = \frac{N_{FEv}\langle metallized\ ceramic\rangle + N_{FEv}\langle core\rangle}{N_{FE}} = \frac{2+1}{2} = 1.5$$

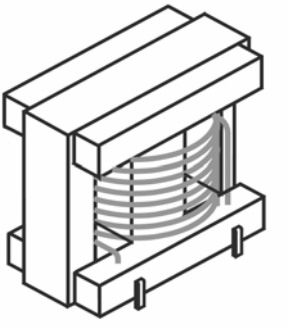


$N_{FE\,met\_ceramic} = 1$

$N_{FEv\,met\_ceramic} = 2$

Inductor windings
Capacitor

a.



$N_{FE1} = 2$

$N_{FEv1} = 2$

$N_{FE2} = 1$

$N_{FEv2} = 1$

b.

Figure 4-2 Virtual functional elements a. integrated LC structure [Waf02] b. discrete L and C components

In a discrete components assembly, each functional element participates in only one schematic symbol, which gives N_{FEv} equal to N_{FE} and the functional elements integration level K_I equal to 1. Figure 4-2b shows two discrete components, an inductor and a capacitor. The capacitor contains one functional element, and the inductor contains two functional elements: the magnetic wire and core. Each of these elements performs only one function, hence the level of integration is equal to 1.

$$K_I = \frac{N_{FEv}}{N_{FE}} = \frac{N_{FEv}\langle inductor\rangle + N_{FEv}\langle capacitor\rangle}{N_{FE}} = \frac{2+1}{3} = 1$$

In the case of monolithic integration for e.g., N_{FE} is equal to 1 as we have one chip, while N_{FEv} is equal to the number of elements in the schematic representation of the chip. The K_I value then corresponds to the definition of integration level in terms of monolithic integration.

Furthermore, it is possible that a packaging element performs a fundamental function, in which case that packaging element does not contribute to the total number of functional elements N_{FE}, but represents one (or more) virtual functional elements and thus increases the integration level value. This will be explained in more detail later on.

Packaging elements integration level

Analogous to functional elements and virtual functional elements, a packaging element that performs *n* packaging functions is "worth" *n* virtual packaging elements. A quantity that evaluates the level of packaging elements multifunctionality in a sub-assembly, *packaging elements integration level* (K_P), is defined as:

$$K_P = \frac{\sum_j N_{PEv_j}}{N_{PE}} = \frac{N_{PEv}}{N_{PE}} \tag{4.2}$$

where N_{PE} is the total number of packaging elements in the converter while N_{PEvj} is the number of virtual packaging elements that the packaging element *j* is worth.

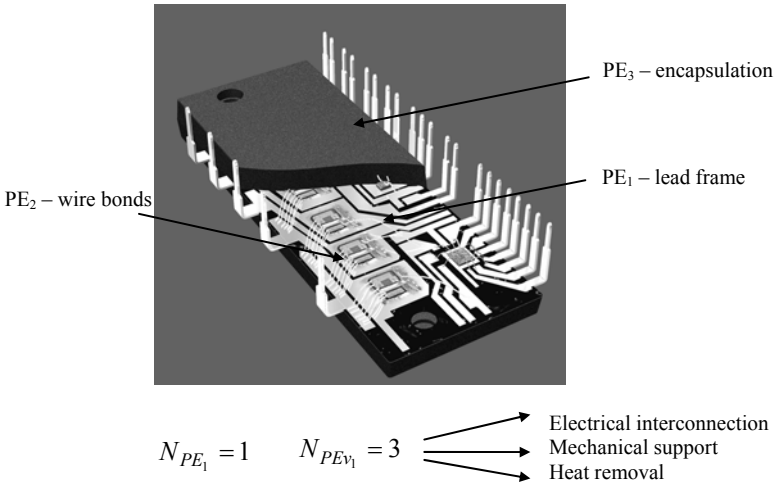


Figure 4-3 Virtual packaging elements [Iwa01]

For example, the lead frame in a power module, shown in Figure 4-3 represents one packaging element. Since it provides the electrical interconnections, heat path and mechanical support, it is worth three virtual packaging elements, i.e. N_{PEv} of the lead frame is 3. On the other hand, the wire bonds provide only electrical interconnections, hence the number of virtual packaging elements is one. The last packaging element is the assembly encapsulation that provides environmental protection and mechanical support as it holds the whole assembly together. The level of packaging elements integration of this power module is:

$$K_P = \frac{N_{PEv}}{N_{PE}} = \frac{N_{PEv}\langle leadframe\rangle + N_{PEv}\langle wirebonds\rangle + N_{PEv}\langle encapsulation\rangle}{N_{PE}} = \frac{3+1+2}{3} = 2$$

As discussed in Chapter 3, the wire bonds in the above power module also conduct the heat dissipated by the power semiconductor dies but their contribution is very small compared to the

main heat path through the lead frame and hence this function is not attributed to this packaging element.

4.3 Increasing level of functional elements integration

In Chapter 3, three fundamental functions of a power electronic converter were identified: electrical, thermal and electromagnetic function. Consequently, the functional domain of the converter design includes the design of these three functions. In Section 4.2.2, the term "circuit symbol" is used to define the level of functional elements integration. In this context, "circuit symbol" implies part of the representation of the fundamental function design, captured in the electrical circuit schematic, thermal circuit or electromagnetic energy flow. In this connotation, functional domain is represented by *circuit schematic symbols* while physical domain is represented by *functional elements* and *packaging elements*.

The number of virtual functional elements is equal to or larger than the number of circuit symbols. Each circuit symbol in the functional domain (electrical, thermal and electromagnetic design) is performed by at least one virtual functional element. The case where these two quantities are equal is intuitive and clear from the definition of virtual packaging element. The number of virtual functional elements is larger then the number of circuit elements when two or more functional elements contribute to the same circuit symbol. For example, the circuit element magnetic field shaping can in the same sub-assembly be implemented in two functional elements, a high permeability ferrite core and low permeability magnetic sheet.

By analysing the definition of functional elements integration level, K_I, given by (4.1), it can be concluded that this quantity increases if the total number of functional elements N_{FE} decreases or if the total number of virtual functional elements N_{FEv} increases. Let us investigate methods that can be implemented to increase the level of functional elements integration in power electronic sub-assemblies.

4.3.1. Multifunctional functional elements

By designing one functional element to implement several circuit symbols, the total number of functional elements in the sub-assembly can be reduced and the level of functional elements integration can be increased.

Let us assume a sub-assembly with the level of functional elements integration K_I. Let us analyze two functional elements, FE_m and FE_n, and let N_{FEvm} and N_{FEvn} be the numbers of virtual functional elements that these two functional elements are worth. If the element FE_m is redesigned to implement the additional N_{FEvn} circuit symbols, its number of virtual functional elements will increase from N_{FEvm} to $N_{FEvm}+ N_{FEvn}$. This redesigned functional element will be designated as FE_m' and the number of virtual functional elements that this element is worth is $N_{FEvm}'= N_{FEvm}+ N_{FEvn}$. The element FE_n can then be omitted and the level of functional elements integration of the modified sub-assembly, K_I', becomes:

$$K_I' = \frac{N_{FEv}'}{N_{FE}'} = \frac{\sum_{j=1}^{N_{FE}-1} N_{FEv_j}'}{N_{FE}-1} = \frac{\sum_{i=1,i\neq m,n}^{N_{FE}} N_{FEv_i} + N_{FEv_m}'}{N_{FE}-1} = \frac{\sum_{i=1,i\neq m,n}^{N_{FE}} N_{FEv_i} + N_{FEv_m} + N_{FEv_n}}{N_{FE}-1} = \frac{\sum_{i=1}^{N_{FE}} N_{FEv_i}}{N_{FE}-1} = \frac{N_{FEv}}{N_{FE}-1} = K_I \cdot \frac{N_{FE}}{N_{FE}-1} > K_I \tag{4.3}$$

Figure 4-4 schematically shows this method. Each solid rectangle represents one functional element and different shades indicate that functional elements are implemented in different construction technology.

It is assumed for the sake of simplicity that the element FE_m alone took over the functionality of the element FE_n. In practice, the functionality of the element FE_n can be divided among the rest of the functional elements. Furthermore, a completely new element can be introduced to replace the functionality of the element FE_m and FE_n, instead of increasing the functionality of the existing elements.

Some examples of implementation of this method for increasing the level of functional elements integration are:

- Monolithic semiconductor integration – the functionality of a single functional element, semiconductor sliver, replaces the functionality of a large number of discrete functional elements.
- Electromagnetic integration of passives – the functionality of ceramic dielectric is increased to perform the capacitive and inductive functional element (as shown in Figure 4-2).

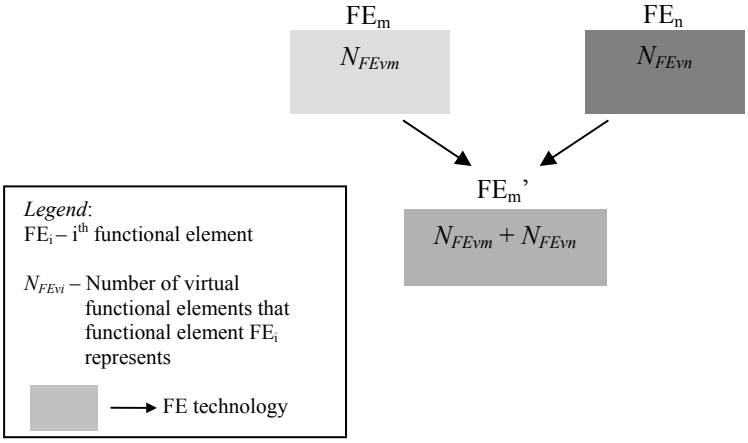


Figure 4-4 Multifunctional functional elements

4.3.2. Reducing the number of functional elements by using integrated processes

The second approach to increase the level of functional elements integration in a sub-assembly, K_I, is to reduce the number of functional elements by implementing a number of circuit symbols in the same process, which is then considered as one functional element. In this case the number of virtual functional elements remains the same.

Figure 4-5 illustrates this method schematically. By using the same notation as in the previous method, if two functional elements FE_m and FE_n are made in one integrated process, they are considered as one functional element FE_m'. The total number of functional elements decreases by one, while the number of virtual functional elements remains the same. Hence, the new value of functional elements integration level, K_I', becomes:

$$K_I' = \frac{N_{FEv}'}{N_{FE}'} = \frac{N_{FEv}}{N_{FE}-1} = K_I \cdot \frac{N_{FE}}{N_{FE}-1} > K_I \tag{4.4}$$

Examples of this method are:

- Hybrid integration technologies such as thick film and thin film, where a number of passive circuit elements is implemented in the same process. Figure 4-6 shows such a sub-assembly of two capacitors and one resistor implemented in thick film technology.
- Passive components embedded into the Printed Circuit Board – this technology allows for implementing a number of passive components in the form of laminates (resistors, capacitors) in standard PCB manufacturing process.

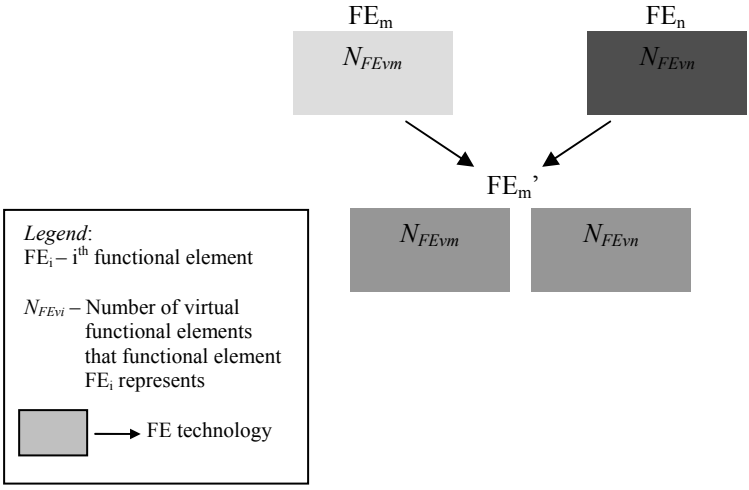


Figure 4-5 Reduction of functional elements number by using integrated processes

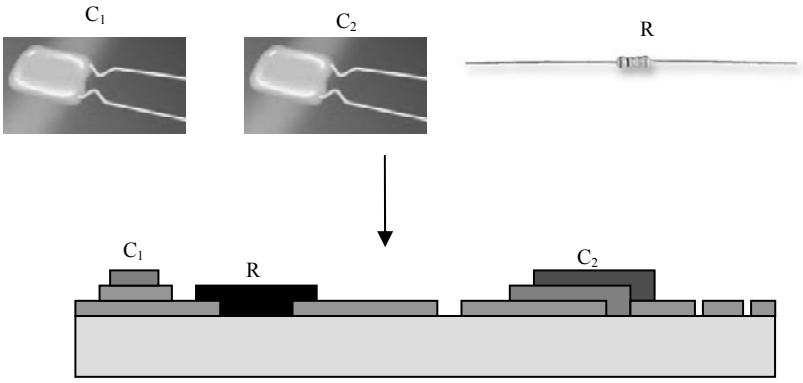


Figure 4-6 Using integrated processes (thick film) to reduce the number of functional elements

4.3.3. Packaging elements as functional elements

The level of functional elements integration, K_I, can also be increased if a packaging element is designed to implement one or more circuit symbols – i.e. to act as one or more virtual functional elements.

Let us assume that the packaging element PE_i is redesigned to implement the circuit symbols that the functional element FE_m implements, i.e. the number of virtual functional elements that come from PE_i is equal to the number of virtual functional elements that the functional element FE_m was worth, i.e. $N_{FEvi} = N_{FEvm}$. This allows for omitting the functional element FE_m which decreases the total number of functional elements by one. The new value of functional elements integration level, K_I', becomes:

$$K_I' = \frac{N_{FEv}'}{N_{FE}'} = \frac{\sum_{i,i\neq m} N_{FEv_i} + N_{FEvi}}{N_{FE}-1} = \frac{\sum_{i,i\neq m} N_{FEv_i} + N_{FEvm}}{N_{FE}-1} = \frac{\sum_{i} N_{FEv_i}}{N_{FE}-1} = K_I \cdot \frac{N_{FE}}{N_{FE}-1} > K_I \qquad (4.5)$$

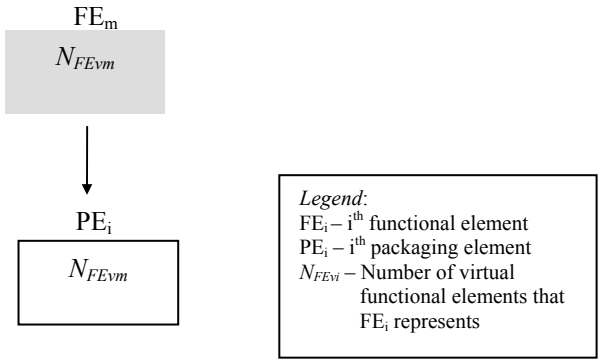


Figure 4-7 Packaging elements as functional elements

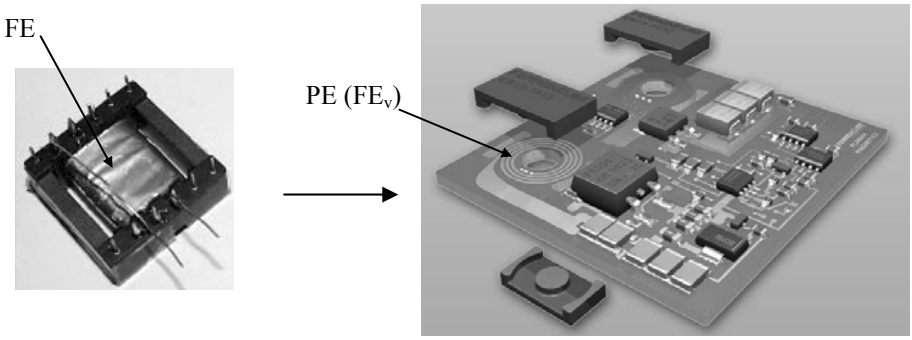


Figure 4-8 Packaging elements as functional elements – Planar PCB transformer [Fer]

The method is schematically illustrated in Figure 4-7. The functional element is represented by a solid rectangle, while the packaging element is represented by a hollow rectangle.

Some examples of implementing this method to increase the level of functional elements integration are:

- Using PCB layers with enhanced dielectric and magnetic properties as capacitive or magnetic elements;
- Using electrical interconnections (copper tracks on Printed Circuit Boards) to implement inductor windings (Figure 4-8);
- Using electrical interconnection elements for tailoring of energy flow [Cro92].

4.4 Increasing level of Packaging elements integration

By analysing the definition of packaging elements integration level K_P, given by (4.2), it can be concluded that this quantity increases if the total number of packaging elements N_{PE} decreases or if the total number of virtual packaging elements N_{PEv} increases.

It is logical that if the number of functional elements N_{FE} decreases by means of one of the methods derived in Section 4.3 that the number of packaging elements will also decrease since there are fewer functional elements to "serve". For this reason, in the following sections it will be assumed that N_{FE} is fixed. Under this assumption, let us investigate methods that can be implemented to increase the level of packaging elements integration in power electronic sub-assemblies.

4.4.1. Multifunctional packaging elements

In order to perform a packaging function, a packaging element must have certain physical properties determined by the function, such as electrical or thermal conductivity, mechanical strength, moisture absorption etc. By designing a packaging element in a way that it fulfils several requirements one can make use of one packaging element for more than one packaging function.

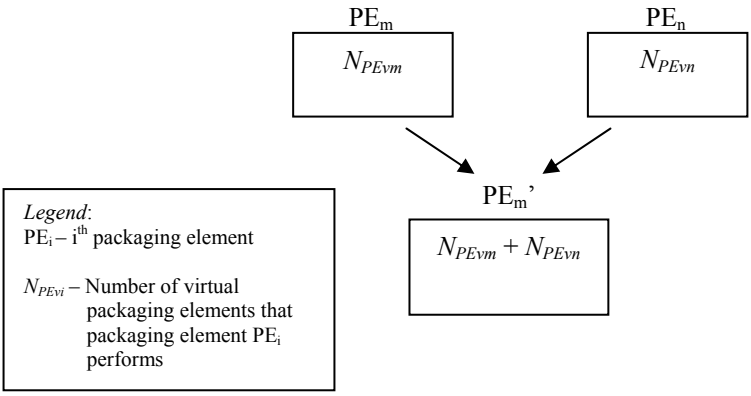


Figure 4-9 Multifunctional packaging elements

Let us consider a sub-assembly with a level of packaging elements integration K_P. Let PE_m and PE_n be two packaging elements, and N_{PEvm} and N_{PEvn} be the numbers of virtual functional elements that these two packaging elements perform (Figure 4-9). If the element PE_m is redesigned to perform the additional N_{FEvn} functions, the number of virtual packaging elements of this packaging element (now designated as PE_m') increases from N_{FEvm} to $N_{PEvm}+ N_{PEvn}$, then the element PE_n can be omitted and the level of packaging elements integration K_P' becomes:

$$K_P' = \frac{N_{PEv}'}{N_{PE}'} = \frac{\sum_{j=1}^{N_{FE}-1} N_{PEv_j}'}{N_{PE}-1} = \frac{\sum_{i=1,i\neq m,n}^{N_{FE}} N_{PEv_i} + N_{PEv_m}'}{N_{PE}-1} = \frac{\sum_{i=1,i\neq m,n}^{N_{FE}} N_{PEv_i} + N_{PEv_m} + N_{PEv_n}}{N_{PE}-1} = \frac{\sum_{i=1}^{N_{FE}} N_{PEv_i}}{N_{PE}-1} = \frac{N_{PEv}}{N_{PE}-1} = K_P \cdot \frac{N_{PE}}{N_{PE}-1} > K_P \tag{4.6}$$

An example of this method for increasing the level of packaging elements integration is shown in Figure 4-10 [Ger02]. An integrated housing is used as a heat path for passive components, mechanical support and since it is made of metal, it can also be used for electrical interconnection.

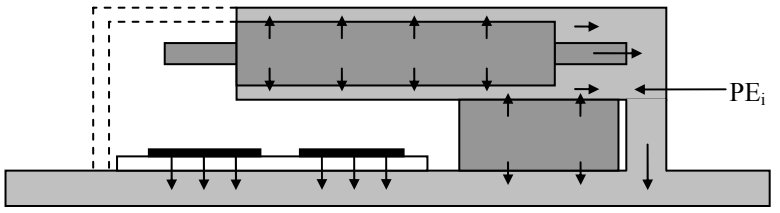


Figure 4-10 Multifunctional packaging element (thermal integration) – housing, heat path, electrical connection [Ger02]

4.4.2. Sharing packaging elements

When using discrete components, the packaging elements that belong to these components serve only one functional element. If more functional elements share one packaging element (housing, mechanical support, heat paths) the number of total virtual packaging elements N_{PEv} remains the same and the total number of packaging element N_{PE} decreases.

Let us assume that two packaging elements, PE_m and PE_n related to the functional elements FE_m and FE_n are replaced by one PE_m' that is shared between two functional elements. This is illustrated in Figure 4-11. The same notation as in the illustrations of the previous methods is used, i.e. the solid rectangles represent functional elements while hollow rectangles represent packaging elements. The total number of packaging elements decreases by one and the new value of packaging elements integration level, K_P', becomes:

$$K_P' = \frac{N_{PEv}'}{N_{PE}'} = \frac{N_{PEv}}{N_{PE}-1} = K_P \cdot \frac{N_{PE}}{N_{PE}-1} > K_P \tag{4.7}$$

Figure 4-12 shows an example of this method on a power module assembled on a lead frame. This example was already mentioned with introducing packaging elements integration in Chapter 3. Figure 4-12 shows how the packaging element PE_1' (housing) is shared among 10 functional elements and thus replaces the packaging elements PE_1 to PE_{10}. The same stands for the lead frames instead of a separate lead frame for each die one lead frame is used for the whole module.

Other examples of this method are:

- Thermal packaging elements integration (the heat path is common for a number of functional elements) [Ger02] (Figure 4-10);
- Multichip modules (MCM), where a number of semiconductor dies are mounted on a common ceramic substrate.

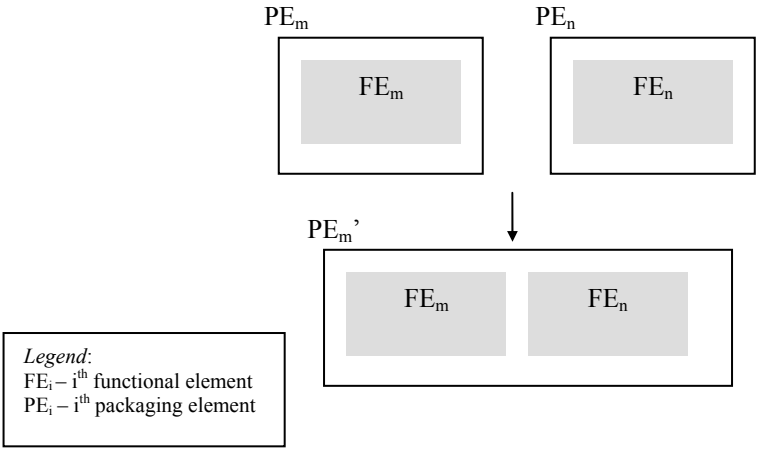


Figure 4-11 Shared packaging elements

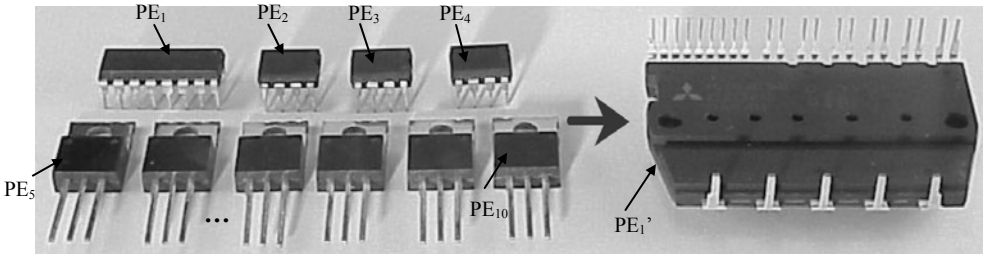


Figure 4-12 Shared packaging elements (lead frame power module) [Iwa01]

4.4.3. Reducing the number of packaging levels

In conventional literature on microelectronic packaging [Bla00][Tum97] a number of packaging levels in an electronic system are identified:

- Component level – chip is extracted from the wafer and placed into an individual package;
- Board level – mounting and interconnecting several components on a board such as Printed Circuit Board (PCB);
- Board to board level – assembly of an array of boards, interconnected by means of a motherboard;
- Complete system level – assembly of the complete system.

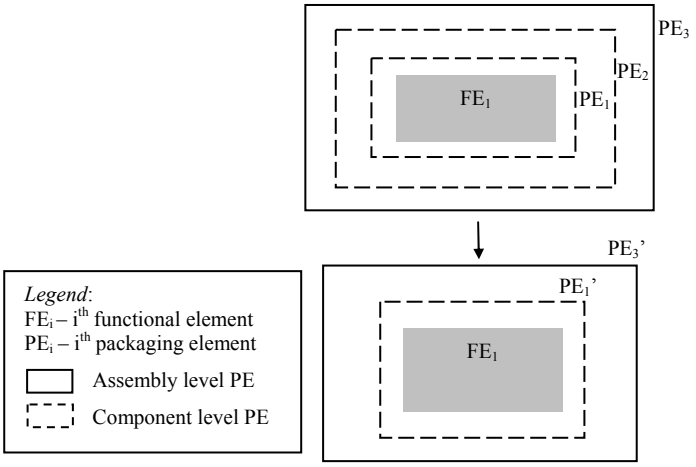


Figure 4-13 Reducing the number of packaging levels

The packaging hierarchy in power electronics is different to some extent. The higher packaging levels, above the component level are not always based on assembling components on PCBs and interconnecting the PCBs by means of a motherboard. Therefore, only two packaging levels were distinguished in Chapter 3: component level and assembly level. Discrete components are provided with connections, mechanical support, protection and their own heat sinking. On the assembly level, these components are interconnected electrically, thermally and

mechanically. By transferring some of the packaging functions from the component level to the assembly level the total number of packaging elements, N_{PE}, can be reduced, which increases the level of packaging elements integration, K_P.

Figure 4-13 schematically illustrates this method. The solid rectangles represent functional elements, hollow solid line rectangles assembly level packaging elements and hollow dashed line rectangles represent component level packaging elements. Let us assume that the component level packaging elements PE_1 and PE_2 are replaced by an assembly level packaging element PE_1'. Since the functions are only transferred to the assembly level, the number of virtual packaging elements remains the same. The new value of packaging elements integration level, K_P', is:

$$K_P' = \frac{N_{PEv}'}{N_{PE}'} = \frac{N_{PEv}}{N_{PE} - 1} = K_P \cdot \frac{N_{PE}}{N_{PE} - 1} > K_P \tag{4.8}$$

An example of this method is Chip-On-Board technology, shown in Figure 4-14, where bare semiconductor dies are directly attached to laminate printed circuit boards [Asp]. This allows for the omission of separate packaging elements for mechanical support, protection and electrical interconnections for each functional element.

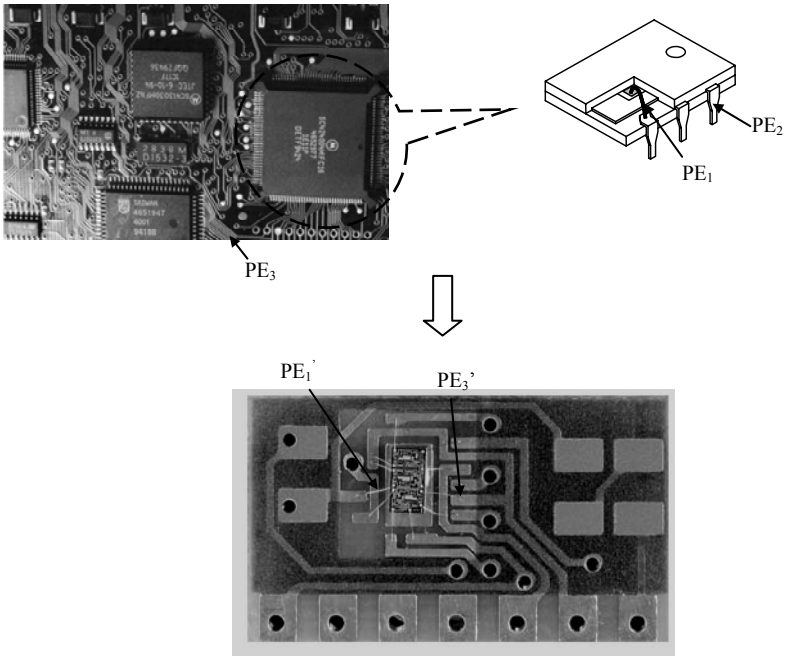


Figure 4-14 Reducing number of packaging levels (Chip-On-Board technology) [Asp]

4.4.4. Functional elements as packaging elements

Analogous to using packaging elements to implement circuit symbols in order to increase the level of functional elements integration, a functional element can be designed to perform one or more packaging functions in order to increase the level of packaging elements integration. In this case, a functional element is designed to perform one or more packaging functions. This obviates the need for one or more packaging elements, which means that the total number of packaging elements N_{PE} can be reduced.

Let us assume that the functionality of the packaging element PE_m, represented by N_{PEvm} virtual packaging elements, is performed by the functional element FE_i (Figure 4-15). In that case, the number of virtual packaging elements represented by FE_i, N_{PEvi}, is equal to N_{PEvm} and the packaging element PE_m can be omitted. By substituting this into (4.2) the packaging elements integration level value K_P' of the modified sub-assembly becomes:

$$K_P' = \frac{N_{PEv}'}{N_{PE}'} = \frac{\sum_{i,i\neq m} N_{PEv_i} + N_{PEv\,p}}{N_{PE}-1} = \frac{\sum_{i,i\neq m} N_{PEv_i} + N_{PEvm}}{N_{PE}-1} = \frac{\sum_{i} N_{PEv_i}}{N_{PE}-1} = K_P \cdot \frac{N_{PE}}{N_{PE}-1} > K_P \quad (4.9)$$

An example of implementation of this method to increase the level of packaging elements integration is using a magnetic core to enclose the whole circuit and for the heat removal [Hof95]. Another example is using a capacitive functional element as the circuit substrate, providing mechanical support for the other functional elements [Per04] (Figure 4-16).

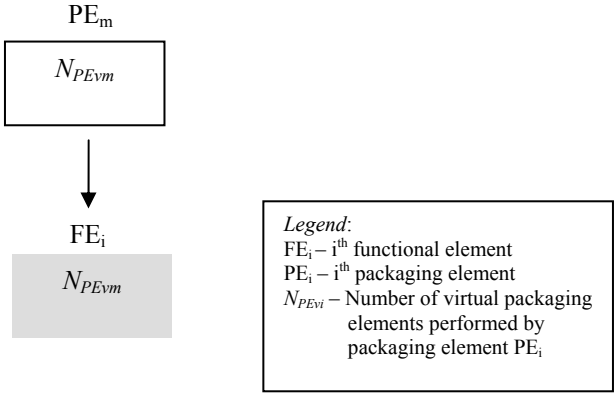


Figure 4-15 Functional elements as packaging elements

4.5 Combination of methods for increasing integration level

By combining the methods for increasing the level of functional and packaging elements integration presented in the previous sections, the level of integration in a sub-assembly can be increased even further. It is possible to combine the methods from the same group as well as to combine the methods for increasing K_I and methods for increasing K_P.

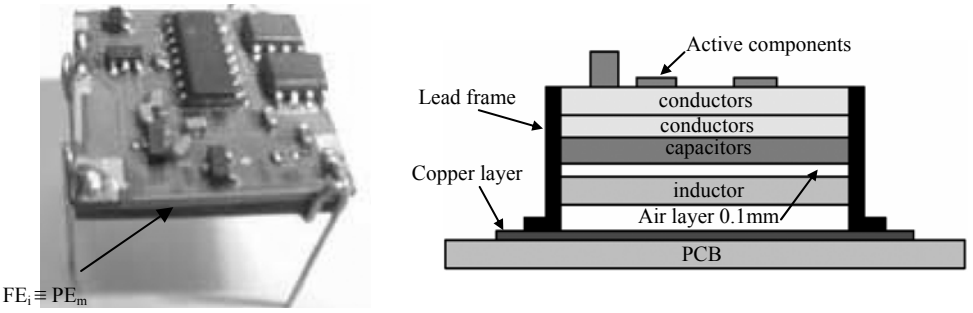


Figure 4-16 Functional elements as packaging elements (capacitor module as circuit substrate) [Per04]

Figure 4-17 shows the methods from both groups and a few examples of such combinations. One example is embedded passive integrated circuits (emPIC) technology [Waf02], where planar electromagnetically integrated passive functional elements are embedded into the PCB. In this technology, the following methods are employed:

- Packaging elements are designed to perform as functional elements (enhanced PCB layers perform capacitive and magnetic functions) – Section 4.3.3.
- The functional elements perform more fundamental functions (capacitive and magnetic) – Section 4.3.1.
- The functional elements are manufactured in an integrated process (multilayer PCB lamination process) – Section 4.3.2.

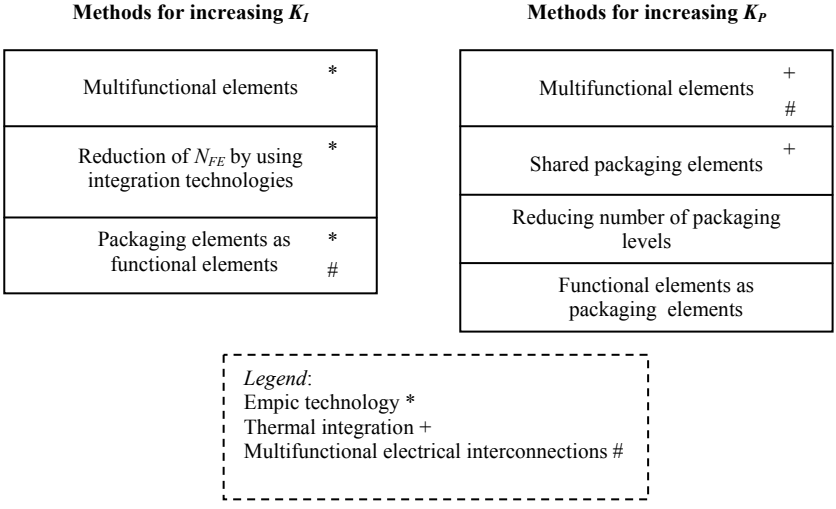


Figure 4-17 Combining methods for increasing level of integration

Another example is the case of thermal integration shown in Figure 4-10. In this case, two methods are combined:

- Sharing packaging elements among all passive functional elements – Section 4.4.2;

- Multifunctionality of packaging elements – Section 4.4.1.

Since the packaging elements that perform electrical interconnections are implemented in electrically conductive materials, such as metals, these materials are also thermally conductive, which means that such elements can be used for heat removal. Furthermore, such elements can also be used to implement functional elements such as inductor windings or capacitive electrodes. In this case three methods are combined:

- Multifunctionality of packaging elements – Section 4.4.1;
- Packaging elements perform as functional elements – Section 4.3.3.

4.6 Integration limits – need for circuit partitioning

In Section 3.4.3, the relationship between functional and packaging elements integration was discussed. It was pointed out that although the fully integrated solution, where the whole circuit is implemented in a single functional element is superior in terms of size, reliability, and assembly cost, this is not always the most optimal or possible solution, due to various factors including fundamental limits, manufacturing cost and performance. Hence, when these limits are reached and increasing the level of functional elements integration by means of the methods from Section 4.3 is no longer feasible, packaging elements integration takes over.

On the other hand, packaging elements integration also has its limits. Although it might be possible to further increase the level of packaging elements integration by implementing the methods from Section 4.4, this might not be the most cost- and performance-effective solution. For example, following the method of packaging elements sharing presented in Section 4.4.2, the whole power electronic converter should be assembled on a single carrier. Due to the presence of functional elements with a high heat density such as power semiconductors, this needs to be a substrate with high thermal performance such as ceramic-based Direct Bonded Copper substrate (DBC). This would result in a higher level of packaging elements integration and lower number of parts, but DBC substrates are expensive and fragile. Furthermore, a considerable number of functional elements in a typical power electronic converter have a low heat density, which implies that a high thermal performance substrate might not be necessary for their thermal management.

For the above discussed reasons, increasing integration level, both functional and packaging, should be done in combination with a suitable partitioning of the circuitry. The methods from Section 4.3 and Section 4.4 are then applied to increase the level of functional and packaging elements integration within the partitions.

4.6.1. Circuit partitioning criteria

There are a number of criteria that influence the way that the circuit is partitioned. Let us discuss the most prominent factors.

Performed function

Since the function (fundamental, packaging) that an element performs determines the

technology that can be used (material properties, manufacturing processes etc.) this is one of the most important criteria for creating partitions. For example, high value energy storage functional elements such as capacitive and magnetic elements cannot be implemented in silicon due to its magnetic and dielectric properties.

Function level

Even if a group of elements perform the same function, implementing them in different technologies might be more efficient if the level of performed function varies significantly.

For example, capacitive and magnetic functional elements with low values of capacitance and inductance can be implemented in monolithic integration technology. On the other hand, high value energy storage capacitive and magnetic functional elements cannot be implemented in this manufacturing process due to the unsuitable magnetic and dielectric properties of silicon.

Another example is choosing thermal packaging elements based on the level of heat that the corresponding functional elements dissipate. If this level is comparable among the functional elements, it is feasible to implement the whole circuitry on one substrate, such as printed circuit board for low heat density dissipating functional elements or thermally conductive circuit carriers such as DBC for high heat dissipating functional elements.

Cost

The importance of cost for a wide application of power electronics was discussed in Chapter 1. In Chapter 3, cost was recognized as one of the main drivers and at the same time restrainers of integration. Higher levels of integration bring fewer manufacturing processes, which brings the total cost down provided that it does not require an expensive manufacturing process that would cancel out the benefits of the reduction of the number of manufacturing processes. Therefore, partitions are normally chosen so that each partition can be effectively manufactured using technologies that allow for minimal number of parts and manufacturing and assembly processes.

4.6.2. Two approaches to circuit partitioning

[Fer05] distinguishes two approaches to circuit partitioning. The first approach is based on the function and achievement level of the function. [Lee02] outlines the research program of Centre for Power Electronic Systems (CPES) that implements this approach by partitioning power electronic converters on active and passive sub-assemblies referred to as Integrated Power Electronic Modules (IPEM). These two types of sub-assemblies are implemented in different technologies suited for their characteristics. This approach is also pursued by the European Centre for Power Electronics (ECPE) [Fer05], where the circuit is partitioned into the planar IPEM and three-dimensional IPEM, based on the characteristics of the functional elements (heat density, cost per volume etc) and each IPEM is constructed in the most suitable technology. [Jac00] uses this approach for circuit partitioning by combining various packaging technologies applied to a 2.2 kW motor drive.

The second approach is based on partitioning the circuit into a number of equal sub-circuits with the lower level of function (power level, heat density) and implementing the sub-circuits using cost-effective technologies that are generally suitable for low power ranges [Pop05b]. This practically means that the complete converter consists of a number of equal building blocks with a lower power rating, which are stacked in parallel in order to achieve the desired power level. Furthermore, in order to reduce the component stresses, these modules can be interleaved in time [Cha95].

4.6.3. Integration level of a partitioned sub-circuit

Let us analyze how the functional and packaging elements integration level changes with the partitioning of a sub-circuit. Let N_{FEv} be the total number of virtual functional elements, N_{FE} the total number of functional elements and K_I the level of functional elements integration in the initial, non-partitioned sub-circuit.

Let us assume that the sub-circuit is partitioned into n partitions according to the discussion explained in the previous sections. Let N_{FEvi} be the number of virtual functional elements and N_{FEi} the number of functional elements in the i^{th} partition. The number of virtual functional elements remains the same. The level of functional elements integration of the partitioned sub-circuit K_{Ip} is:

$$K_{Ip} = \frac{N_{FEvp}}{N_{FEp}} = \frac{\sum_{i=1}^{n} N_{FEv_i}}{\sum_{i=1}^{n} N_{FE_i}} = \frac{N_{FEv}}{\sum_{i=1}^{n} N_{FE_i}} \geq \frac{N_{FEv}}{N_{FE}} = K_I \tag{4.10}$$

where equality holds if there is no functional elements integration in the partitions.

A similar reasoning can be followed for the level of packaging elements integration. Let us assume that the sub-circuit is partitioned into n partitions according to the discussion explained in the previous section. Let N_{PEvi} be the number of virtual packaging elements and N_{PEi} the number of packaging elements in the i^{th} partition. The number of virtual packaging elements remains the same. The level of packaging elements integration of the partitioned sub-circuit K_{Pp} is:

$$K_{Pp} = \frac{N_{PEvp}}{N_{PEp}} = \frac{\sum_{i=1}^{n} N_{PEv_i}}{\sum_{i=1}^{n} N_{PE_i}} = \frac{N_{PEv}}{\sum_{i=1}^{n} N_{PE_i}} \geq \frac{N_{PEv}}{N_{PE}} = K_P \tag{4.11}$$

Equality holds if there is no packaging elements integration in the partitions.

4.7 Summary

This chapter deals with defining quantities to evaluate the level of integration in power electronic assemblies, both functional and packaging elements integration and developing formal methods to increase these quantities.

In Section 4.2.1, the definitions of integration level in microelectronics, in the case of monolithic and hybrid integration, were given. Both levels of integration represent the number of electrical circuit elements integrated in one functional element or one package. In Section 4.2.2, the quantities for evaluating the level of integration in power electronic converters, namely functional elements integration level, K_I, and packaging elements integration level, K_P, were introduced. By analyzing the level of multifunctionality of FEs and PEs in a sub-assembly, the integration level was evaluated.

Based on these quantities, the methods for increasing the level of integration were developed, for FEs integration in Section 4.3 and PEs integration in Section 4.4. The methods were illustrated on examples that already exist in power electronics or microelectronics construction technology. The methods are summarized in Table 4-1. Some examples of combining these two methods were presented in Section 4.5.

Table 4-1 Methods for increasing the level of FEs and PEs integration

Method		Description
FE integration	*Method 4.3.1*	Multifunctional FE
	Method 4.3.2	Reduction of the number of FE by using integrated processes
	Method 4.3.3	PE as FE
PE integration	*Method 4.4.1*	Multifunctional PE
	Method 4.4.2	Sharing PE
	Method 4.4.3	Reduction of the number of packaging levels
	Method 4.4.4	FE as PE

In Section 4.6, circuit partitioning as a means to deal with limits of integration was discussed. Two approaches to circuit partitioning were identified. The first approach partitions the circuit into different sub-circuits based on the function and level of function of the circuit symbols. The second approach partitions the circuit into equal sub-circuits with lower function level that can be implemented in cost-effective technologies.

The methods for increasing the level of integration presented in this chapter, together with the integration technologies from Chapter 5 and the design approach foundations introduced in Chapter 3, will be used in Chapter 7 to formalize a design algorithm that allows for physical implementation of power electronic converters with higher level of integration.

The introduced quantities, functional elements integration level (K_I) and packaging elements integration level (K_P), will be used as one of criteria for the evaluation of construction technologies for power electronic converters that will be presented in Chapter 6.

4.8 References

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Chapter 5: Technologies for integration in power electronics converters

5.1 Introduction

In Chapter 3, two types of integration were identified: functional elements integration and packaging elements integration. In Chapter 4, the methods for increasing the integration level, in relation to both functional and packaging elements integration were introduced. In this chapter the technologies that allow for the implementation of these methods are presented. Descriptions of the technologies are given together with the methods from Chapter 4 that can be embodied in the technology to increase the level of functional and packaging elements integration. Furthermore, the application boundaries for each technology are also discussed.

For convenience, the methods for increasing the level of integration are designated on the basis of the section of Chapter 4 that they were introduced in, as shown in Table 4-1 in Chapter 4.

The presented technologies are classified according to the primary function they implement in power electronic converters:

- Substrate technologies – technologies that provide electrical interconnections, mechanical support and insulation (ceramic-based substrates are described in Section 5.2 and organic-based substrates are described in Section 5.3);
- Interconnection technologies – technologies that provide electrical interconnections not attached to substrates (Section 5.4);
- Environmental protection technologies – technologies for providing environmental protection of functional elements such as encapsulation and housing technologies (Section 5.5);
- Functional elements technologies – technologies for constructing and spatial arrangement of functional elements (Section 5.6).

Some of these technologies were already mentioned in Chapter 2, when state of the art of constructing power electronic assemblies was presented. In this chapter, however, the accent is on their potential for implementing the integration methods.

In this chapter, the term "technology" has a broader meaning than materials and manufacturing processes, as usually considered. Especially in Section 5.6 that deals with FEs integration technologies, not only materials and processes but underlying integration principles are presented.

The chapter is summarized in Section 5.7.

5.2 Ceramic-based substrate technologies

Ceramics are inorganic non-metallic materials that consist of metallic and non-metallic elements bonded together by ionic and/or covalent bonds. They are crystalline in nature, with a dearth of free electrons. Ceramics are attractive for application as substrates in electronic circuits due to their electrical, thermal, mechanical and chemical properties. They have a high electrical resistivity, are very stable, chemically and thermally, and have a high melting point. Compared to plastic-based substrates, they also have relatively high thermal conductivity.

Ceramics exist as oxides, nitrides, carbides, or siliicides. Ceramic substrates used in electronics generally include aluminium oxide (Al_2O_3 – Alumina), beryllium oxide (BeO – beryllia), aluminium nitride (AlN), boron nitride (BN), diamond (C), and silicon carbide (SiC). The most widely used are alumina due to its low cost and aluminium nitride due to its exceptional electrical and thermal characteristics. The others are used less often due to their characteristics, such as the high cost of diamond, the toxicity of beryllia etc.

Ceramic interconnection technologies differ in metallization technique, manufacturing processes, maximum number of layers, conductive materials used etc. The selection of a metallization technique depends on both the application and the compatibility with the substrate material. In the following sections, ceramic substrate technologies and their metallization techniques that allow for implementing the methods for increasing the level of integration will be presented.

5.2.1. Thick film technology

Technology description, materials and processes

Thick film technology has been used in the electronics industry for over five decades for constructing hybrid circuits. The thick film process is an additive process by which conductive, resistive and dielectric (insulating) patterns in the form of a viscous paste are screen-printed, dried and fired onto a ceramic substrate at an elevated temperature to promote the adhesion of the film [IMA]. In this manner, by depositing successive layers, multilayer interconnection structures can be formed which may contain integrated resistors, capacitors or inductors. The active element within the paste dictates the electrical properties of the fired film. If the active element is a metal, the fired film will be a conductor, if it is a conductive metal oxide, a resistor, and if it is an insulator the fired film will be a dielectric. The main steps in the thick film manufacturing process are shown in Figure 5-1. This process is mature and can be automated for cost-effective, high-volume production.

Potential for increasing level of integration

Thick film technology is an integration technology that allows for the manufacturing of a number of passive FEs in an integral process. By using pastes with different characteristics, FEs such as resistors, capacitors and inductors can be produced in an integrated process. By adding other passive elements and discrete semiconductor devices, either as chips or as prefabricated and separately surface-mounted devices a hybrid thick-film circuit is produced.

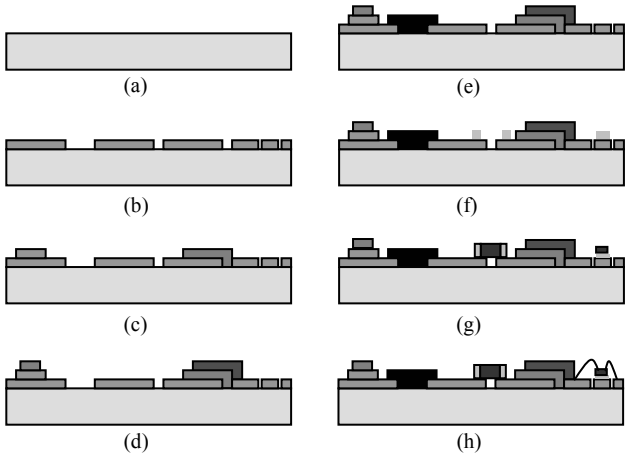


Figure 5-1 Thick film manufacturing process

This means that *Method 4.3.2* of constructing a number of FEs in one integrated process can be implemented for increasing the level of FEs integration.

Concerning PEs integration, thick film technology is used as a substrate technology in packages that contain several integrated circuits referred to as Multichip modules (MCM) and packages that contain several power semiconductor dies referred to as power modules. This is an implementation of the method of sharing PEs (*Method 4.4.2*), in this case the substrate, among several FEs.

Application boundaries

The thickness of conductive pastes used in screen-printing is usually between 0.3 mils to 2 mils (7.6 μm – 50 μm). For higher currents, thicker conductors can be produced by multilayer printing of conductive tracks, which results in high current-carrying connection suitable for power applications. This can be combined with fine-line geometries to enable substrates for combined power and control circuits. Thick film technology is used for producing power hybrid circuits in the low to medium power range, up to about 2 kW [Wel][Tyc][XPM].

Concerning capacitors produced in this integral manner, a capacitance of 1000pF with a dielectric that meets X7R characteristics can be implemented in the footprint of a 0805 chip capacitor. The dielectric strength of thick film capacitors depends on the type of the dielectric paste used, with typical values being around 20-30 V/μm [Gup03]. Thick film screen-printed resistor technology offers tolerances to <0.5 % in ranges from milliohms to megaohms.

5.2.2. Thin film technology

Technology description, materials and processes

Thin film technology is a subtractive technology where the entire substrate is coated with several layers of metallization and the unwanted material is etched away in a succession of selective photo-etching processes [IMA]. The use of photolithographic processes to form the patterns enables much finer and more well-defined lines than can be formed by the thick film process. This feature promotes the use of thin film technology for high interconnection densities and high frequency applications.

Thin film circuits are composed of films between 50 Å and 20 000 Å (5 nm – 2 μm) thick. Thin film materials are deposited by vacuum deposition (evaporation, sputtering, chemical vapour deposition), spin coating and plating (electro and electroless plating). The patterns are formed by means of photolithography and etching. With the exception of electroplating, in which the conductor may be plated in the desired pattern, the deposited layer must be patterned by means of photolithography and wet chemical etching. Patterning of thin film interconnects is very similar to semiconductor fabrication. The deposited film is coated with photoresist, and the photoresist is soft-baked, exposed through a mask, developed and hard-baked. The underlying film is etched through openings in the photoresist, and then the photoresist is stripped. As in the case of thick film technology, adding other passive elements and discrete semiconductor devices, either as chips or as prefabricated and separately surface mounted devices produces a hybrid thin-film circuit.

Potential for increasing level of integration

By using different materials for films, thin film technology allows for implementing resistive, capacitive and inductive elements in an integrated process. Hence, like thick film technology, it allows for implementing *Method 4.3.2* of manufacturing several FEs in an integral manufacturing process.

Thin film technology is used for manufacturing High Density Interconnection substrates (HDI) for Multi-chip Modules (MCMs). Again, as in the case of thick film, this technology allows for applying the method of sharing PEs *Method 4.4.2* in the form of common substrate for a number of FEs.

Application boundaries

Since the conductor thicknesses that can be achieved in this technology are lower then those in thick film technology (<5 μm), the current levels that circuits manufactured in this technology can handle are also much lower. Hence, this technology is mainly used in low current applications where the circuit size and density of interconnections are the major issues, such as microwave and HDI substrates [Aer][Nan]. The dielectric strength of thin film capacitors depends on the type of the film, with the value of most used material, evaporated silicon monoxide, being around 200 V/μm [Gup03].

Capacitor values that can be achieved in thin film technology are lower than in thick film technology. Standard values are 0.5 pF to 500 pF and capacitance densities are 8.5 pF/mm^2 to 230 pF/mm^2.

5.2.3. Low Temperature Co-fired Ceramic (LTCC) technology

Technology description, materials and processes

Low Temperature Co-fired Ceramic (LTCC) [LTC] technology can be defined as a thick film-based multilayer technology where single unfired tapes (green sheets) with printed conductor lines on the surface are laminated on top of each other and fired all together in one step. A big advantage of LTCC technology is that the firing temperature is much lower (850 °C – 1050 °C) than those of more mature High Temperature Co-fired Ceramic (HTCC) technology. This presents the possibility of using low resistivity conductors like silver, gold, copper and alloys with palladium and platinum instead of tungsten and molybdenum that are used in HTCC technology. The low firing temperature enables the use of precious metals in the conducting layers and the metallization is gold-based or silver-based thick film formulated to be compatible with LTCC material. One advantage that LTCC has over other multilayer technologies is the ability to print and fire resistors. It is also possible to bury printed capacitors of small values. The manufacturing process of LTCC is shown in Figure 5-2. This technology has its primary applications in telecommunications (RF and optical), the automotive industry, data processing, high reliability space and medical applications etc.

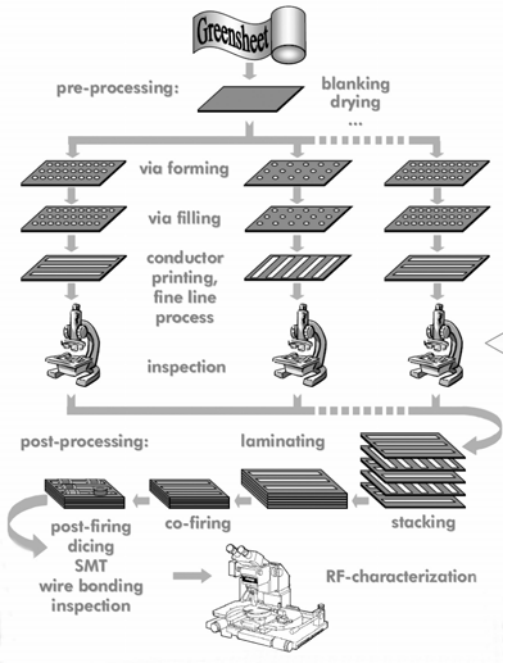


Figure 5-2 Low Temperature Co-fired Ceramic (LTCC) manufacturing process [LTC]

A variation of LTCC technology is Low Temperature Co-fired Ceramic on Metal core (LTCC-M) [DLI]. The individual layers are appropriately prepared and then laminated to a metal core. The metal core provides an excellent RF ground, a very high rate of thermal dissipation and a means of constraining the XY shrinkage that occurs in the production of LTCC and HTCC packages. This technology combines the benefits of Low Temperature Co-fired Ceramic processing and low cost thick film materials with a metal core to provide superior electrical and thermal performance.

Potential for increasing level of integration

LTCC technology combines the properties of thick film with the advantage of the multilayer tape based dielectric. Hence, similar to thick film, this technology also allows for implementing the *Method 4.3.2* of manufacturing FEs such as resistive, capacitive and inductive elements in an integrated manner as shown in Figure 5-3. Furthermore, magnetic FEs such as windings of inductors and transformers can be implemented in the layers' metallization, which increases the level of FEs integration by means of *Method 4.3.3*. The same method is implemented by using tapes with enhanced permeability (ferrite tapes) or permittivity (dielectric tapes) in order to realize inductive or capacitive FEs.

Concerning PEs integration, this technology allows for implementation of *Method 4.4.2* of sharing PEs in MCMs, like thick and thin film technologies. Furthermore, the green tapes serve as mechanical support and protection for the FEs realized within inner layers, thus implementing *Method 4.4.1* of increasing the functionality of PEs.

Application boundaries

LTCC technology is mainly used in RF applications up to a few watts. Due to its improved thermal properties LTCC-M can be used in applications up to about 150 W. Hence, in power applications this technology is suitable for low power converters and implementation of control circuits in higher power converters.

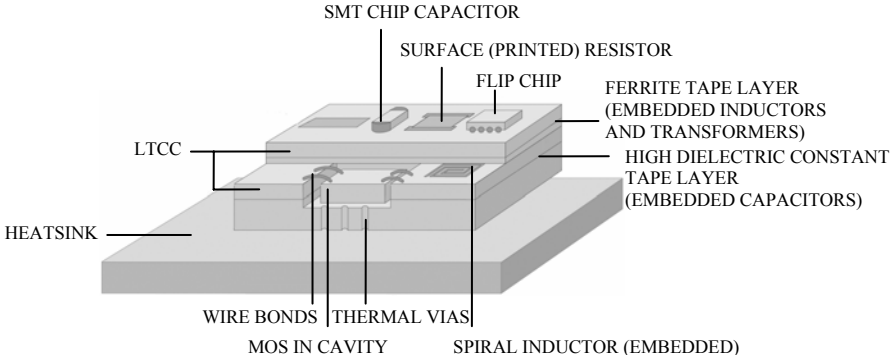


Figure 5-3 Integration in LTCC technology [Cma]

Regarding integral capacitors achievable in LTCC technology, [Del99] shows that a fabrication capability of 7.8 nF/cm^2 was achieved. Typical capacitance values found in LTCC circuit are low, up to 3000 pF [Cma].

5.2.4. Direct Bond Copper (DBC)

Technology description, materials and processes

A Direct Bond Copper (DBC) substrate consists of a ceramic isolator, Al_2O_3 (Alumina) or AlN (Aluminium-Nitride), onto which solid copper is bonded in a high temperature melting/diffusion process. This process runs at about 1075 °C in an inert atmosphere using eutectic melting of a very thin copper oxide layer, which forms a very strong bond of the copper to the ceramic base (Figure 5-4) [Cur].

The thickness of the copper foils that are bonded onto the ceramic substrate is between 0.125 mm – 0.7 mm. The patterning of the copper is done by a technology similar to processing conventional PCBs. The thick copper conductors provide excellent current-carrying capability and heat-spreading of power dies attached onto it. The strong adhesion of the copper to ceramic bond reduces the coefficient of thermal expansion (CTE) in the plane to values only slightly higher than those of the ceramic itself (7.2 - 7.6 x 10-6). This allows direct die attachment of large dies without using CTE controlling layers.

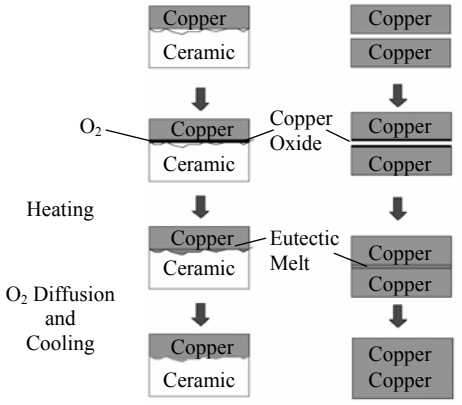


Figure 5-4 Manufacturing process of DBC substrates [Cur]

Potential for increasing level of integration

In contrast to the above presented ceramic based technologies, DBC technology does not allow for integration of passive FEs such as resistive, capacitive and magnetic elements in an integral manufacturing process.

The main advantage of DBC is its high current capability due to the thickness of the copper metallization. Hence DBC is the primary technology choice for high power MCMs for power applications (Figure 5-5a) [Cur]. Power semiconductor FEs are soldered to the DBC substrate

at the top and the DBC is in turn soldered onto a base plate at the bottom side. This is an implementation of *Method 4.4.2* of shared PEs, in this case the DBC substrate.

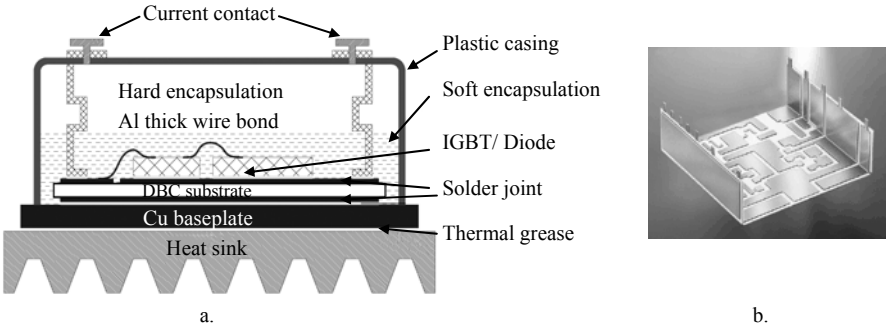


Figure 5-5 Integration potentials of DBC [Cur] a. Power Multi-Chip Module b. Three dimensional DBC

Another characteristic of DBC that is taken advantage of in power modules is high thermal conductivities of ceramic substrates (24 W/mK – thermal conductivity of Alumina and 180 W/mK – thermal conductivity of Aluminium Nitrid); hence the substrate is used as the main thermal path from the power semiconductors to the heat sink. This is an implementation of *Method 4.4.1* of multifunctionality of PEs.

Using a process of laser scribing the backside of the DBC substrate, this substrate can be bent as shown in Figure 5-5b, creating a quasi 3D structure. The control part of the circuitry can be assembled on the side parts of the DBC while the power part is assembled on the bottom part that is mounted onto the heat sink. This allows for increasing the level of PEs integration by applying *Method 4.4.2* of sharing PEs – in this case the substrate between the control and power FEs, which results in a reduction of the number of PEs.

Application boundaries

Due to its high current capability, DBC is used for power electronic converters in high power levels, from a few kilowatts up to tens of kilowatts. However, due to its mechanical characteristics and high cost, it is mainly used only for FEs with high loss density such as power semiconductors.

5.3 Organic substrate technologies

5.3.1. Printed circuit board (PCB) technology

Technology description, materials and processes

Polymer-based substrates, such as the conventional Printed Circuit Board (PCB), have been used in electronics for decades as a cheaper and easier to process alternative to ceramic substrates. The substrate is a composite material consisting of epoxy (resin) and glass fibres (base material). A composite structure is advantageous because it combines the favourable properties of its ingredients. For instance, glass fibres are strong, and this gives the laminate its

structural ability. However, it breaks easily when bent. Forming a composite of the brittle glass and a tough resin gives better ductility to the composite because the glass fibres absorb most of the stress during bending.

PCBs are manufactured by laminating layers of core and prepreg alternately. Core is a layer of dielectric (woven glass fibre or paper) impregnated with resin, cured and coated with copper foil by means of rolling or electro-deposition. Prepreg is uncured fibreglass epoxy resin that will harden during lamination. The conductive patterns of the inner layers are produced by means of photolithography. This is followed by aligning the layers, pinning them between two metal plates and heating them in a hydraulic press for a few hours. Electrical interconnections between layers are provided by means of electroplated via holes. Vias can be through-hole, which means that they are drilled through the whole PCB, or blind and buried, which means that they span between two inner layers or an inner layer and an outer layer.

Potential for increasing level of integration

PCBs are traditionally used for electrical interconnection and mechanical support of electronic circuits. However, in the past few years, PCB functionality was increased by embedding passive components such as capacitors, inductors and resistors into the PCB as shown in Figure 5-6. This is done by using layers with enhanced dielectric and magnetic properties such as capacitive and magnetic laminates and laminating them together with the conventional PCB layers in the same manufacturing process. For resistive elements printing of resistors with resistive pastes is employed or special laminates for resistive elements such as the Ohmega Ply process [Fer02][Waf02].

In the case of capacitive and magnetic laminates, they can be regarded as PCB laminates since they are laminated in one process with the rest of the PCB layers (provided that they are compatible with the PCB manufacturing process). Also, magnetic windings and capacitive electrodes are implemented in the PCB layers' metallization. Hence they are PEs that perform fundamental functions, which is an embodiment of increasing the level of FEs integration by applying *Method 4.3.3*. Furthermore, several passive FEs can be manufactured in one manufacturing process, which is an implementation of *Method 4.3.2*.

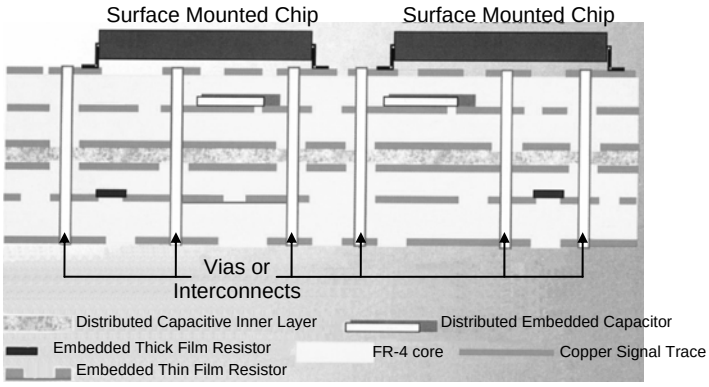


Figure 5-6 Embedding passive FEs into PCB [Bor01]

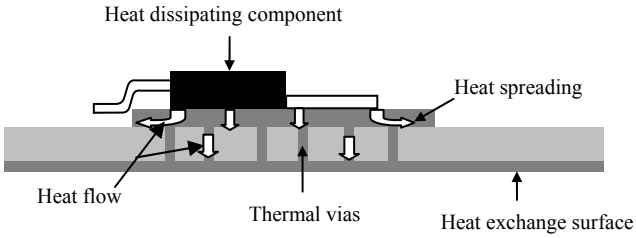


Figure 5-7 Multifunctional PEs in PCB – heat-spreading and thermal vias

Copper metallization on PCB layers is traditionally used for electrical interconnections. If heat-dissipating FEs are mounted on a copper pad larger than their footprint, the heat that they produce is first spread over the larger area and then conducted through the PCB, which decreases the thermal resistance of the heat path through the PCB (Figure 5-7). This is especially important given the low thermal conductivity of PCB (< 1 W/mK). If through-hole vias normally used for electrical interconnection between the layers are used in parallel with this heat path, the thermal resistance can be decreased even more [Kee91]. These are two implementations of *Method 4.4.1* which allows for increasing the level of PEs integration by using multifunctional PEs.

Application boundaries

Due to the limited copper thickness (< 300 μm) and low thermal conductivity, PCB substrates are mostly limited to the low power range, up to a few hundred watts. In the higher power range, they are widely used for implementing control, sensor and protection circuits, auxiliary power supplies etc.

Concerning the values of passive FEs that can be integrated in the PCB, capacitance values of about 0.2 nF/cm^2 [Iso] can be achieved with the capacitive laminates compatible with the standard multilayer process, while capacitance values of up to 4.6 nF/cm^2 can be achieved by using very thin laminates [3M] that require a sequential build-up PCB manufacturing process.

The main limiting factors of magnetic laminates are their low permeability (μ_r~ 20) and high losses (about 10 times higher than the values of sintered ferrites).

The resistor values that can be achieved are in the region of 25-1000 Ω/□ for OhmegaPly and 10 Ω – 1MΩ in paste printing technology.

5.3.2. Insulated metal substrate (IMS)

Technology description, materials and processes

An Insulated Metal Substrate (IMS) consists of a metal base, mostly made of aluminium or copper, a dielectric insulation layer and a metallization copper layer. The standard construction of an IMS is shown in Figure 5-8 [Ber]. The insulation layer is a thin ceramic-polymer blend layer or a low thickness printed circuit board FR4 laminate, which allows for low thermal

resistance of this layer. Standard thicknesses of the copper layer are between 35 μm – 350 μm, of the dielectric layer between 75 μm – 150 μm and of the metal base 0.5 mm – 3.2 mm. Multilayer constructions are also possible.

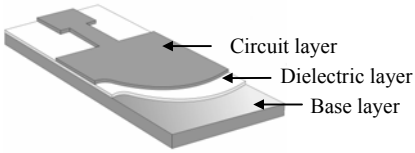


Figure 5-8 Insulated metal substrate – construction [Ber]

Potentials for increasing level of integration

The main advantage of IMS is its thermal capability, which comes from the thin dielectric and metal base that give the low value of the thermal resistance through the substrate. The main heat path is through the substrate, which makes the substrate multifunctional, i.e. increases the level of PEs integration by applying *Method 4.4.1*. Decreasing the thermal resistance by means of thermal vias and heat-spreading (discussed in the PCB technology) can also be implemented in IMS. For lower power level the metal base acts as the heat sink and the external heat sink is not necessary. This means that the PE, in this case the substrate, acts as a thermal FE, which is an implementation of the *Method 4.3.3*.

Furthermore, IMS allows for the direct die attachment, i.e. assembling bare semiconductor dies on the substrate. This allows for skipping one packaging level for electrical interconnection elements, which increases the level of PEs integration by implementing *Method 4.4.3*.

Application boundaries

The available copper thicknesses and good thermal properties of the substrate make IMS the substrate of choice for power electronic converters in the medium power level (2 kW – 10 kW) [Sch03]. In this range IMS is a cost-effective and more mechanically durable alternative to brittle DBC substrates.

5.4 Interconnection technologies

The main function of an electrical interconnection technology is to implement PEs that provide electrical interconnections among FEs. For different applications, different technologies will be used, depending on the current levels, type of FEs and their interfaces etc.

In the previous section, a number of interconnection technologies that are inseparable part of the circuit carrier were presented. The following interconnection technologies that are not part of the carrier and allow for implementing the methods for increasing the level of integration will be presented in this section:

- Planar metallization technologies (used mostly for interconnecting semiconductor FEs with the rest of the circuitry);

- Laminated bus bar technology (used mostly for electrical interconnections of passive FEs and for interconnections on the assembly level);
- Lead frame technology (used mostly for electrical interconnections of semiconductor FEs and for interconnections on the assembly level).

5.4.1. Planar metallization technologies

As discussed in Chapter 2, electrical interconnections in conventional power electronic converters are based on interconnecting discrete components, where each component is provided with its own PEs for electrical interconnections (wire bonds, lead frames, leads etc.). In power modules, electrical interconnection PEs on the component level are omitted and bare dies are interconnected by means of wire bonding. This interconnection technology, although mature, has a number of drawbacks. One concern is the reliability of wire bonds, since they are often the cause of failures. The other drawback is that this technology limits the spatial design of FEs to two dimensions while the third dimension is very important in achieving high power densities. Furthermore, the wire bonding process is intrinsically costly since it performs one wire at a time.

For the above reasons, novel interconnection technologies that allow for metallization of all interconnects at the same time, three-dimensional spatial layout and improved reliability are being introduced [Lee02]. These technologies are mainly planar and in the form of thin film, analogous to interconnection technologies in monolithic integrated circuits and HDI substrates. Planar metallization technologies have been demonstrated to have the highest interconnections density and integrity. Two variants of this technology, employed for microelectronics and power electronics purposes and their integration potentials will be described in the following sections.

Dies embedded in polymer

This technology embeds semiconductor chips into laminated build-up dielectric layers and realizes interconnections using PCB technologies such as galvanic copper metallization and laser drilling of vias [HID]. Figure 5-9 shows the main principle of this technology and the steps in the manufacturing process of fabricating a sub-circuit in this technology.

Integration potential: This technology allows for increasing the level of PEs integration by omitting the component packaging level such as electrical interconnections on the component level (*Method 4.4.3*) and using an integrated metallization process shared among all embedded FEs (*Method 4.4.2*). Furthermore, this technology can be combined with other means of increasing integration level in PCB technologies presented in Section 5.3.1, such as embedded passive FEs, thermal management by means of heat-spreading and thermal vias etc.

Application boundaries: Since this technology is based on PCB technology, similar limits on power levels apply here as well. Furthermore, since the main heat path from the power semiconductor FEs is through the PCB, the amount of heat produced by these elements will be the limiting factor in the use of this technology.

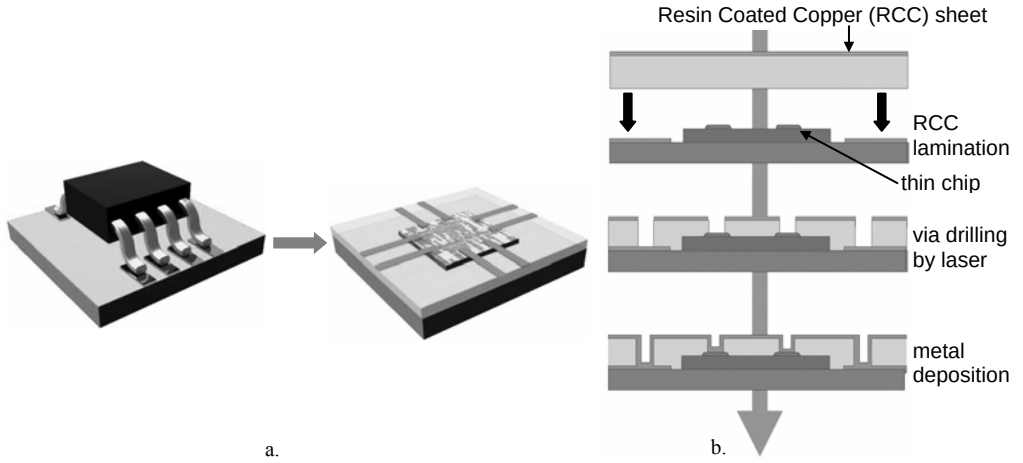


Figure 5-9 Semiconductor dies embedded in printed circuit board [HID] a. principle b. manufacturing process

Embedded power [Lia04]

This technology utilizes planar interconnection technologies in the form of sputtering and electroplating for electrical interconnections of power semiconductor FEs. Semiconductor dies and capacitor chips are embedded in the openings of a ceramic frame and coated with a dielectric layer for planarization and chip protection with via holes on the aluminium pads of the dies. This is followed by metallization, which is done in two steps. The first step is an interface metallization performed by sputtering of Al-Ti-Cu or Al-Cr-Cu metals. The purpose of this layer is to provide a base layer for the second metallization layer, which is implemented by electroplating of a thick copper layer (> 3 mils).

In order to build a power module, this "embedded power" stage is soldered onto a patterned DBC substrate in order to provide remaining electrical connections and thermal paths. Other FEs, mostly in surface-mount technology, are mounted on the ceramic frame. The construction principle and a power module built in this technology are shown in Figure 5-10.

Integration potential: Integration potential of this technology is mainly in the domain of PEs integration. Firstly, an integrated process is employed for electrical interconnection of all FEs and the ceramic frame is shared among a number of FEs (*Method 4.4.2*). Also, the component packaging level for semiconductors and some passive FEs (such as capacitive chips, C-chips in Figure 5-10) is skipped (*Method 4.4.3*). Furthermore, the dielectric layer is multifunctional: it protects the chips and provides insulation, which increases the level of PEs integration by applying *Method 4.4.1*.

Application boundaries: Since the main heat path of semiconductor power FEs is through the DBC substrate, boundaries similar to those described in Section 5.2.4 apply.

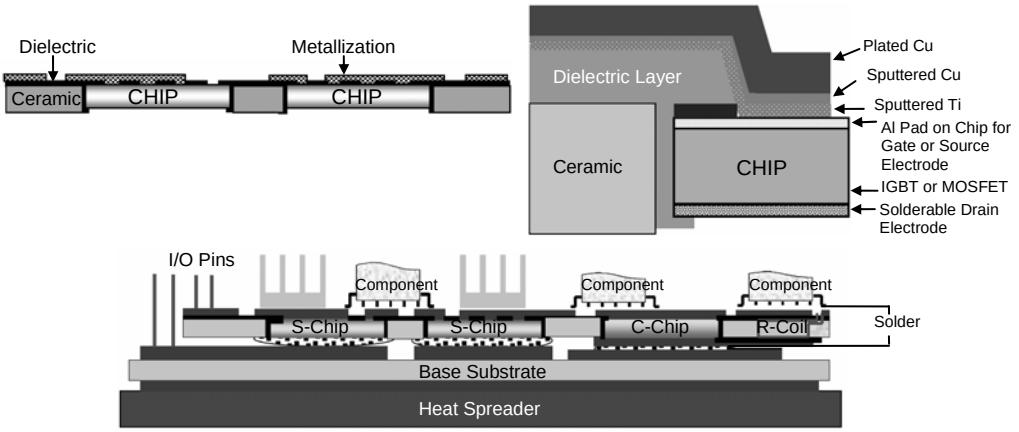


Figure 5-10 Cross-section of a power assembly in embedded power technology [Lia04]

5.4.2. Laminated bus bar technologies

Technology description, materials and processes

Laminated bus bars are made of layers of insulated copper sheet, where each layer is a conductor and can distribute power at a different voltage, can be neutral, ground, act as EMI shield or transmit signals [FCI] as shown in Figure 5-11a. A polymer such as epoxy is used to glue together thick conductor bars and provide electrical insulation. Vias between layers are metal posts or fasteners placed through drilled or stamped holes. Laminated bus bars can handle very high currents and can accommodate very large components.

Potential for increasing level of integration

The bars can be free-floating laminated interconnects or, if sufficiently thick, provide mechanical support in the form of a metal carrier, as shown on a motor drive inverter assembled on a bus bar structure (Figure 5-11b). This increases the level of PEs integration by implementing the method of multifunctionality of PEs (*Method 4.4.1*).

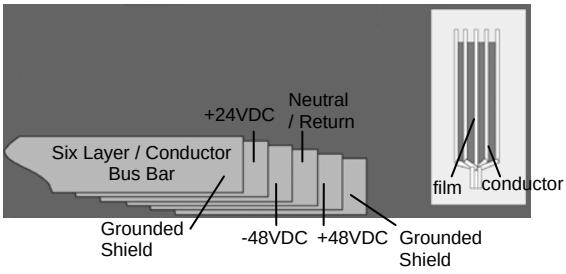
Furthermore, laminated bus bars can be used to implement FEs such as magnetic windings or capacitive electrodes. Figure 5-11c shows an example of a transformer winding implemented in this technology. This increases the level of FEs integration by applying the method of using PEs as FEs (*Method 4.3.3*).

Another implementation of *Method 4.3.3* is using bus bars to implement high frequency EMI filters. By introducing higher resistivity materials into areas of high frequency current crowding caused by the skin and proximity effects, the high frequency resistance of the conductor can be significantly increased. In case of a single conductor, the bus bars consist of an inside part made of a low resistive material (such as copper) and an outside part made of a higher resistive material (such as nickel). At high frequencies, due to skin effect, the current

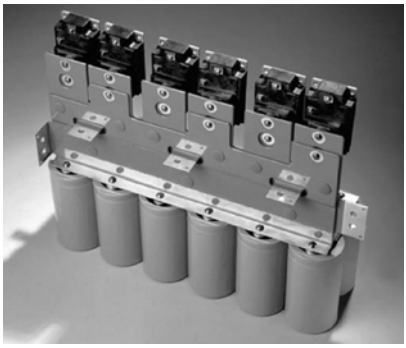
concentrates in the higher resistivity region (outside part) providing high frequency attenuation [Wol02].

Application boundaries

Laminated bus bars are the most suitable for high current, high power applications.



a.



b.

c.

Figure 5-11 Laminated bus bar technology a. construction principle [FCI] b. motor drive inverter assembly c. transformer winding implemented in bus bar technology [Eld]

5.4.3. Lead frame technologies

Technology description, materials and processes

Lead frame has been used extensively in semiconductor packages for decades as a thin layer of metal that connects the wiring from small electrical terminals on the semiconductor surface to the large-scale circuitry.

Lead frames are mostly made out of copper-based alloys. They are manufactured from flat sheet metal by stamping or etching. Etching is a more expensive process than stamping, hence lead frames with small number of leads are stamped, while those with larger number are etched. Stamping is a highly automated mechanical process that employs die and punch sets to progressively achieve the intended lead frame structure through a series of stamping/punching steps. Etching consists of selectively covering the sheet metal with photoresist in accordance with the pattern of the lead frame. The sheet metal is then exposed to chemical etchants that

remove areas not covered by photoresist. After the etching process, the etched frames are singulated into strips. After stamping or etching, the lead frame is then finished with cleaning, silver-plating and taping steps. Silver-plating is done on the bonding fingers and die pad to improve wire bond and die attach quality. Taping consists of putting a lead lock tape over the leads to prevent lead deformation. The manufacturing process flow and typical lead frames for integrated circuits are shown in Figure 5-12.

Potential for increasing level of integration

In conventional packages for integrated circuits, lead frame is used to mechanically support the die and electrically connect the wire bond terminals to the outside circuitry. The lead frame also contributes to the heat removal.

The lead frame can also be used as a carrier for more FEs or even the whole converters, such as power modules for lower power range [Iwa01], "integrated power train" (a power module that contains two MOSFETs and the driver IC for synchronous buck phases) [Rut05] (Figure 5-13a) or low power DC/DC converters (Figure 5-13b) [CD]. The lead frame technology is employed in combination with moulding technologies, which allows for the use of mature processes of manufacturing IC packages in power electronics. Using the lead frame as the circuit carrier shared among several FEs increases the level of PEs integration according to *Method 4.4.2*.

Furthermore, since it is made of electrically conductive materials, lead frames can be used to implement FEs such as magnetic inductor windings or capacitive electrodes. In this manner, the level of FEs integration can be increased by applying *Method 4.3.3*. Such an implementation, where a thick copper lead frame implements the transformer and inductor windings as well as heat sink for the semiconductor FEs, thus implementing *Method 4.3.3* for increasing the level of FEs integration and *Method 4.4.1* for increasing the level of PEs integration, is presented in [Wan04].

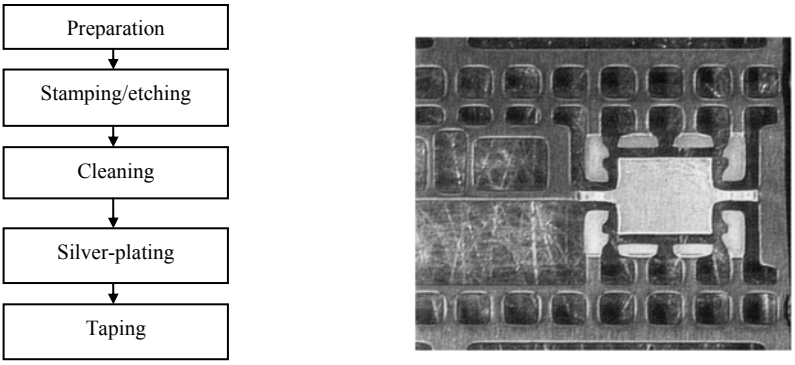
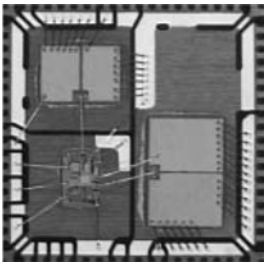
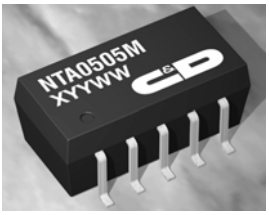


Figure 5-12 Lead frame technology a. manufacturing process b. lead frame [Agi]



a.



b.

Figure 5-13 Lead frame as circuit carrier a. integrated power train [Rut05] b. 1W DC/DC converter [CD]

Application boundaries

Depending of its thickness, a lead frame can handle a wide range of current levels from low to high currents. The main drawback of lead frame technology is that it is mainly used in combination with wire bonding for electrical interconnection between semiconductor FEs and lead frame pads. The main drawbacks of this interconnection technology were already discussed.

Furthermore, the manufacturing process of encapsulating the lead frame assembly restricts the use of this technology to the low to medium power levels due to the limited heat dissipation capabilities.

5.5 Environmental protection technologies

In conventional discrete components and assemblies, each functional element has its own packaging elements for environmental protection, in the form of housing, coating or encapsulation.

In the following sections, technologies for protection of FEs are presented that allow for increasing the integration level by means of:

- Encapsulating several FEs in one process (Chip-on-board (COB) technology);
- Performing functions other than protection (Moulded Interconnect Device (MID) and metal housing technology).

5.5.1. Chip-on-board encapsulation technologies

Chip-on-board (COB) technology allows for attaching bare semiconductor FEs onto laminate substrates such as PCBs. Various encapsulation technologies, such as liquid encapsulation or transfer moulding, are used to protect he dies. For high-volume applications and applications that can be fit into standardized mould cavities, transfer moulding provides a low-cost alternative. Larger modules and die mounted to large mixed technology substrates generally demand liquid encapsulation. Liquid encapsulants come in two types: silicone or epoxy-based. Silicone systems offer excellent moisture resistance and high compliance, but are difficult to

mark and difficult to handle. Epoxy systems provide improved adhesion and marking relative to silicone as well as more consistent appearance and require smaller “keep outs” or die spacing specifications. The most widely used encapsulation method is Glob Top, which is simply the process of depositing the encapsulant on top of the component (Figure 5-14). An alternative method is dam-and-fill, which is a two-step process where the first step is dispensing a high viscosity dam around the component and the second the filling of the dam with a low-viscosity filler material.

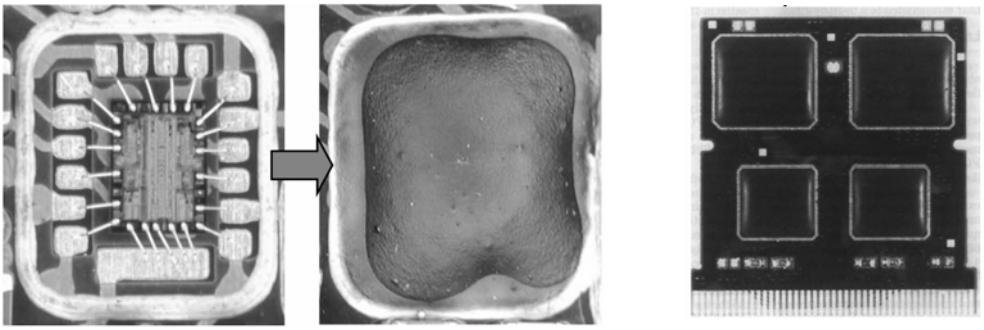


Figure 5-14 Encapsulation in COB technology [Nat] [DPC]

Potential for increasing level of integration

In this technology several dies can be encapsulated in the same process, thus increasing the level of PEs integration by skipping the component packaging level (*Method 4.4.3*). Other techniques for increasing the level of integration related to PCB technologies described in Section 5.3.1 can also be utilized.

Application boundaries

This technology is based on PCB technology, hence limits similar to those presented in Section 5.3.1 apply. The main heat path is through the PCB, which limits the amount of dissipated heat that can be removed.

5.5.2. Moulded interconnect device (MID) technology

Technology description, materials and processes

Moulded Interconnect Device (MID) is defined as [MID]: “An injection moulded plastic substrate which incorporates a conductive circuit pattern, and integrates both mechanical and electrical functions. An MID may be either two or three dimensional, and a variety of methods may be used to apply the conductors”.

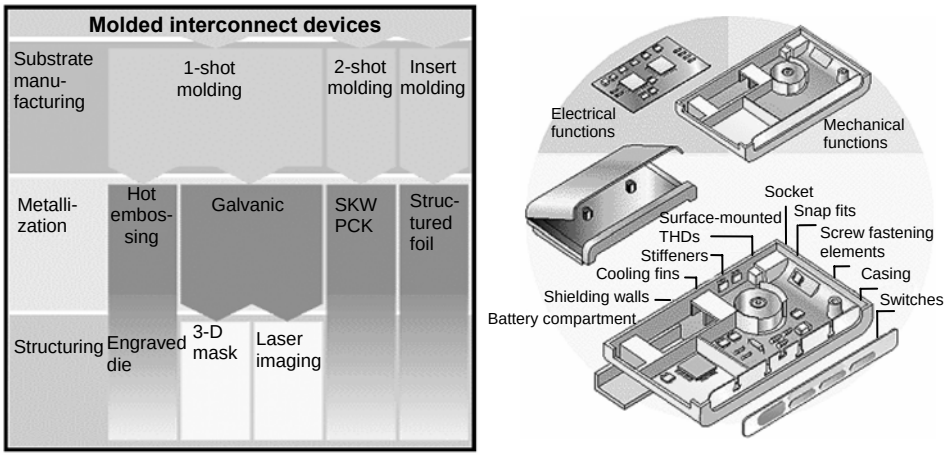
MIDs can be produced in a number of ways depending on the application requirements. The most common methods of manufacturing include (Figure 5-15):

- Single-shot injection moulding – In the case of single-shot injection moulding, the moulding process is followed by a series of metallizing steps that are very similar to those employed for conventional printed circuitry.
- Two-shot moulding – This process uses two separate moulding cycles and usually different polymers to form the component. It requires the construction of different mould cavities for each shot.
- Film techniques (Capture process, Transfer process, Hot stamping) – These processes have in common the fact that the conducting material starts out as a separate flexible film and is subsequently attached to an injection moulded plastic substrate. The conductors are usually formed from copper laminate, foil or silver conductive inks on a carrier.

For metallization patterns a range of conductive materials are used, such as copper, tin, nickel, silver and carbon inks etc. Metallization patterns can have thicknesses between 12 μm and 125 μm.

Potential for increasing level of integration

The most prominent benefit of MIDs arises from their ability to integrate electrical and mechanical functions into a single part. In this way, the plastic part, traditionally used as housing for protection, also serves as the circuit substrate, providing mechanical support and integrity. Furthermore, MIDs can integrate other parts such as integrated connectors, buttons and switches. This reduces the total number of parts and increases the level of PEs integration applying the method of multifunctionality of PEs (*Method 4.4.1*).



a. b.

Figure 5-15 Moulded interconnect devices (MID) technology [Poh97] a. manufacturing process b. MID product

Furthermore, windings of magnetic FEs can be implemented in MID metallization, which allows for increasing the level of FEs integration by applying *Method 4.3.3*, where PEs provide some functions of FEs.

Application boundaries

The major limitation of MID technology is its relatively low circuit density. MID technology cannot replace the layered circuitry in traditional boards, and unlike mutilayer PCBs, which can have as high as 32 layers, MIDs typically have two layers only, on the front and back of the plastic substrate.

5.5.3. Metal-based protection technologies

Technology description, materials and processes

Technologies involved in the manufacturing of metal housings are general purpose technologies for metal processing such as extrusion, machining, punching, stamping, bending etc [Kal01]. More recent technologies such as Metal Injection Moulding (MIM), which allow for more complex shapes of smaller parts, can also be used.

Potential for increasing level of integration

In Section 5.5.1 and Section 5.5.2 it was shown how PEs manufactured in plastic-based protection technologies can be used to perform multiple functions. This can also be done if a metal housing is used for protection.

a. b.

Figure 5-16 Metal housing as the heat path [Ger04] for a. inductor b. section of a dc-dc converter

Since metal is thermally conductive, it can be spatially designed to act as a heat collector from different components to the place where the heat is exchanged with the ambient. Figure 5-16a shows an implementation of this principle on an inductor enclosed in an aluminium housing where the heat is collected from the windings and the core and delivered to the heat sink [Ger04]. This increases the functionality of the housing as PE, which results in the increase of the level of PEs integration according to *Method 4.4.1*.

Furthermore, a metal housing can be used as a heat path for a number of FEs, which increases the level of PEs integration according to *Method 4.4.2*. Figure 5-16b shows several FEs

(inductors, capacitors) in a dc-dc converter enclosed in a metal housing that acts as a heat path for all the elements.

Metal is electrically conductive as well, which means that a metal housing can be designed so that its part performs electrical interconnection. This increases the functionality of the housing as PE, which results in the increase of the level of PEs integration according to *Method 4.4.1*.

Parts of a metal housing can be structured to implement magnetic windings FEs and capacitive electrodes. This increases the level of FEs integration by applying *Method 4.3.3*.

Furthermore, metal housing structures can be used to provide mechanical support and protection for a number of FEs, thus increasing the level of PEs integration by means of *Method 4.4.2*.

Application boundaries

Since metal housings are generally more expensive and heavier protection alternatives than plastic encapsulation techniques, they are mostly used in applications where robustness, heat removal capabilities and electromagnetic shielding are more important than the weight and cost.

5.6 Functional elements technologies

The technologies presented above concern mostly packaging elements and thus primarily increase the level of packaging elements integration. Some of them also allow for integration of functional element integration, particularly substrate technologies that can implement functional elements integration in an integral manufacturing process as part of the substrate.

In this section, technologies related to primarily FEs will be considered. These technologies allow for increasing the level of FEs integration by means of *Method 4.3.1, Method 4.3.2* and *Method 4.3.3*. Some of them allow for increasing the level of PEs integration as well.

These technologies are presented as classified into three categories:

- Monolithic semiconductor integration (technologies that implement FEs that perform switching and control functions)
- Electromagnetic integration (technologies for integration of FEs that perform electromagnetic function)
- Spatial (technologies for spatial arrangement of FEs)

5.6.1. Monolithic integration

Technology description, materials and processes

The process flow of manufacturing a monolithic integrated circuit is shown in Figure 5-17. The process is based on photolithography. A high-energy UV light is shone through a mask onto a slice of silicon covered with a photosensitive film. The mask describes the parts of the chip and

the UV light only affects the areas not covered by the mask. When the film is developed, the areas affected by light are removed. Now the chip has unprotected and protected areas forming a pattern, and this is the first step to the final components of the chip. Next, the unprotected areas are processed by doping so their electrical properties change. A new layer of material is added, and the entire process is then repeated to build the circuit, layer by layer. When all the components have been made and the circuit is complete, a layer of metal is added. As in the previous steps, a layer of photosensitive film is applied and exposed through a mask. However, in this case the mask used describes the layout of the wires connecting all the parts of the chip.

Potential for increasing level of integration

Monolithic semiconductor integration is the most favourable as regards the level of integration since a large number of electrical circuit symbols is implemented in one FE, thus implementing *Method 4.3.1*.

Application boundaries

Power electronics did not benefit from monolithic integration to the extent that microelectronics did since silicon is not suitable for realizing all fundamental functions in power electronics (energy storage, heat removal). This was already discussed in Chapter 3. In power electronics, monolithic integration is mostly employed in integrated circuits for control.

As discussed in Chapter 2, in very low power levels the whole converter can be realized in monolithic technology. This is done by integrating magnetic components directly onto silicon substrates. In Chapter 3, an example of a monolithic 1 W dc-dc converter, where the magnetic component, power switches and control devices were integrated on a single chip, was given.

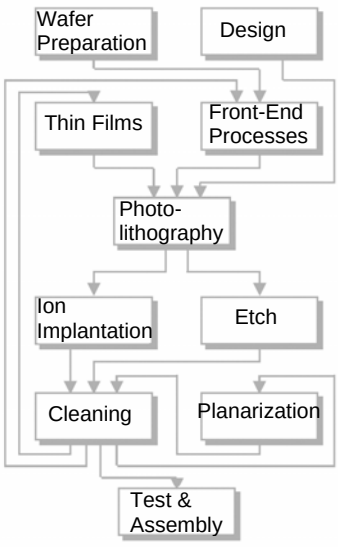


Figure 5-17 Semiconductor manufacturing process

Furthermore, low power semiconductor devices can be integrated in one monolithic integrated circuit with some control, protective and diagnostic circuits. This technology is mostly referred to as "smart power" [Bal91] (discussed in Chapter 3). The manufacturing processes of power and control semiconductor devices differ in a number of factors such as material thicknesses, complexity and number of masks, which presents the main barrier in extensive exploitation of this type of integration.

5.6.2. Electromagnetic integration

In a similar way similar to that in which monolithic semiconductor integration allows for integration of a number of FEs (mostly active) into a single sliver of silicon, electromagnetic integration allows for integrating more then one FE (mostly passive) into one FE.

Potential for increasing level of integration

Integrated magnetic FEs: As described in Chapter 2, magnetic circuit elements (inductors, transformers) in power electronics are traditionally constructed using magnetic wires for current path and magnetic core for magnetic flux path. If there are more magnetic components in the circuit schematic, they are traditionally constructed as separate components.

Under certain conditions related to the operating behaviour of the magnetic circuit elements, namely their voltages have to be proportional during all switching intervals, several magnetic can be implemented in one magnetic core and multiple windings [Ćuk83]. Figure 5-18 shows the principle of such an integrated magnetic FE where three magnetic cores are replaced with one. A procedure for deriving switching mode power converters that can make use of implementing magnetic integration technology is presented in [Kha95].

The technology used to implement such an FE is the same as conventional magnetic components presented in Chapter 2.

By doing so, the magnetic core performs the functions of several magnetic circuit elements and allows for increasing the level of integration by applying *Method 4.3.1*.

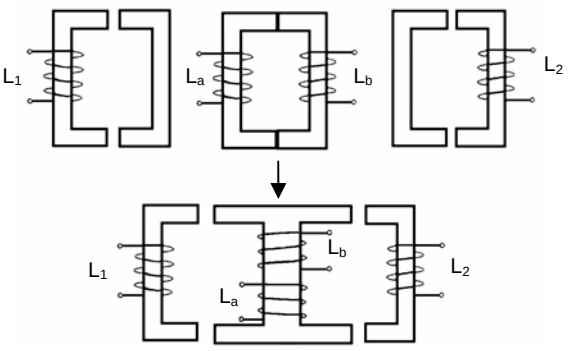
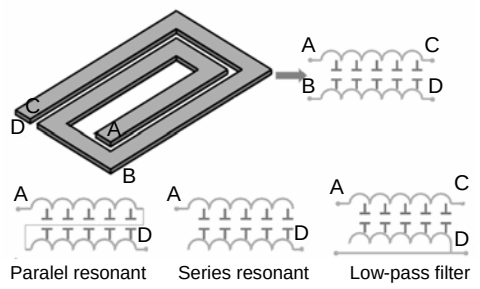
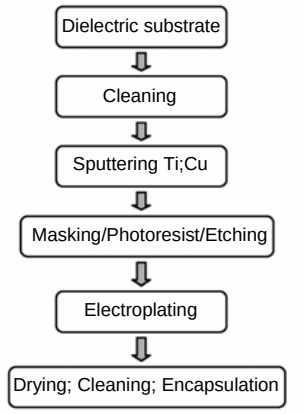


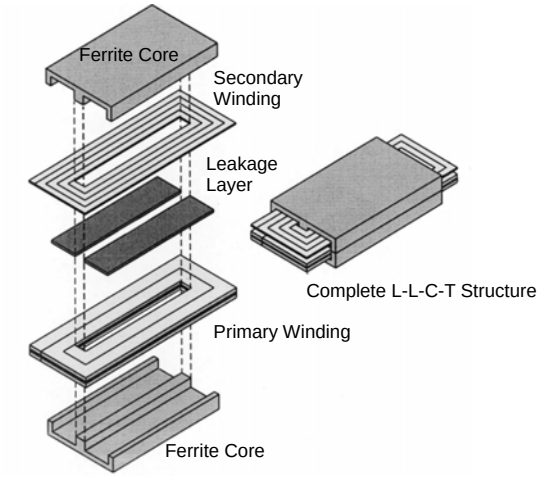
Figure 5-18 Integration of magnetic functional elements [Ćuk83]



a.



b.



c.

Figure 5-19 Electromagnetic integration of reactive FEs a. Planar integrated LC component b. manufacturing steps in ceramic processing c. Planar integrated LLCT component [Che03] [Wyk05]

Integrated reactive functional elements: In Chapter 2, construction technologies for discrete capacitive and magnetic components were described. However, integration of several reactive FEs (inductors, transformers and capacitors) can be achieved by enhancing the capacitance in windings by inserting a dielectric layer between wound conductors (capacitive elements) or adjusting the reluctance between the primary and secondary winding by a layer with a low permeability [Ehs93][Fer02].

The copper tracks implement the inductor windings and capacitive electrodes. The capacitor dielectric is implemented by a dielectric layer inserted between the windings. [Mar95] discusses various technologies that can be used to implement integrated LC components such as electrolytic, planar and polypropylene. Figure 5-19a shows an example of an integrated LC structure implemented in planar technology. The dielectric layer is normally made of ceramic, such as barium titanate ($BaTiO_3$). The steps in manufacturing such a layer are outlined in Figure 5-19b. A magnetic core can be added to enhance the inductance. The equivalent circuit schematic is also shown. Another technology suitable for implementing planar

electromagnetically integrated FEs is PCB technology, where enhanced laminates are used as capacitive and magnetic FEs in the integrated structure. The capacitance values that can be achieved are lower than in ceramic technology, due to the lower permittivity of capacitive laminates compared to ceramic layers.

Electrolytic integrated LC structure is barrel-wound around a ferrite core. The aluminium foils in electrolytic capacitor construction are used to implement windings. In the case of the polypropylene integrated LC structure, the polypropylene metallized film is wound around a ferrite core in a manner similar to that used in the electrolytic integrated structure. In both cases, the insulation between windings has to be provided by means of low permittivity dielectric layers, such as polyimide.

Figure 5-19c shows the exploded view of a planar integrated LLCT component. The ferrite core couples the primary and secondary windings to realize the transformer. The main core is air-gapped to realize the magnetizing inductance. The resonant inductance is implemented through the leakage layer made of low permeability material between the primary and secondary windings. The secondary windings are implemented in copper foil. The resonant capacitance is realized by means of the primary winding conductors and dielectric layer in between two conductive layers. The insulation among the primary and secondary windings, core and leakage layers is accomplished by using layers of low permittivity dielectric, such as polyimide (Kapton).

This technology allows for the implementation of more circuit symbols into one FE. The metallized ceramic layer implements the inductor windings, capacitor electrodes and transformer windings. This increases the level of functional elements integration by applying *Method 4.3.1*.

5.6.3. Spatial packaging of functional elements

In the discrete approach to construction of power electronic converters presented in Chapter 2, components are designed by different manufacturers and optimized to have the best performance for the smallest volume and lowest cost. This means that each component is spatially optimized independently of other components, which results in a lot of unused volume in power electronic assemblies since the components have to be packaged next to each other while the components' shapes are not made to complement each other.

If components are stripped down to their FEs and these FEs spatially designed and packaged together this will result in lower volume, which is crucial in achieving high power densities. Furthermore, this will result in fewer PEs that are shared among a number of FEs thus increasing the level of PEs integration by applying *Method 4.4.2.* Furthermore, one FE can be designed to provide mechanical support or heat removal for another FE, which increases the level of PEs integration by applying *Method 4.4.4.* However, this might involve geometrical reshaping of FEs, which has to be done in the manufacturing phase of the particular FE.

Technologies for spatial packaging of passive functional elements

This technique is especially fruitful when it comes to passive FEs, since they take up a large portion of the total volume.

Concerning capacitive FEs, metallized film capacitive technology allows for manufacturing capacitive FEs in custom shapes and sizes due to the flexibility of the manufacturing process that is employed (Figure 5-20). The former used to roll the metallized film on can be manufactured in different shapes allowing for different shapes of the final capacitive FE.

[Ger02] implements this idea by using spatial packaging of a low pass filter, where the conventional construction that consists of two components, inductor and capacitor is replaced by an implementation where metal film capacitors are reshaped into a "square donut" shape to complement the inductor shape (Figure 5-21). In this case, the inductor serves as mechanical support for the capacitors.

Electrolytic capacitive FEs are generally manufactured in barrel-wound technology, although novel stacked concepts are emerging [Tak04]. These concepts would be more suitable for the effective spatial packaging, similar to stacked metallized film capacitors.

Ceramic capacitive technology is mostly used to implement high frequency capacitive FEs which are normally low in capacitance value and volume. The shape of these FEs is only limited by manufacturing limits of ceramic processing.

Concerning magnetic FEs, the shape of core FEs is limited by the manufacturing technology of ceramic magnetic materials. Before sintering, virtually any shape can be produced. Cores can also be processed after sintering by means of machining and grinding but with less flexibility since sintered cores are brittle. As discussed in Chapter 2, winding FEs can be implemented in a variety of technologies, such as being implemented in rigid or flex PCBs, which gives a large freedom in the shape of the windings. The shape of windings implemented in copper foils or lead frames is limited only by the limits of metal processing techniques such as stamping, punching, bending etc.

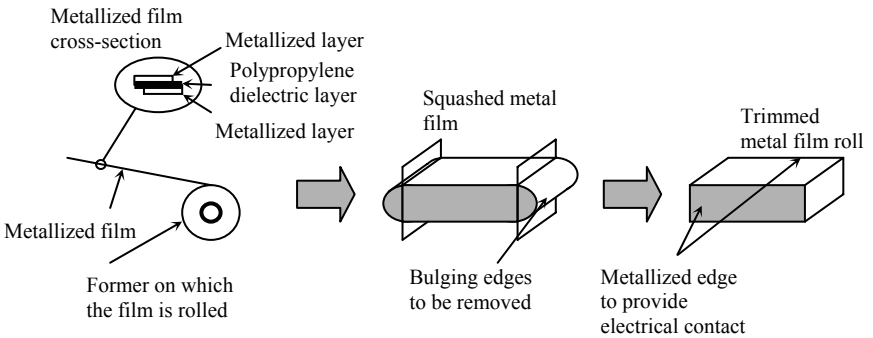


Figure 5-20 Metal film capacitors manufacturing process

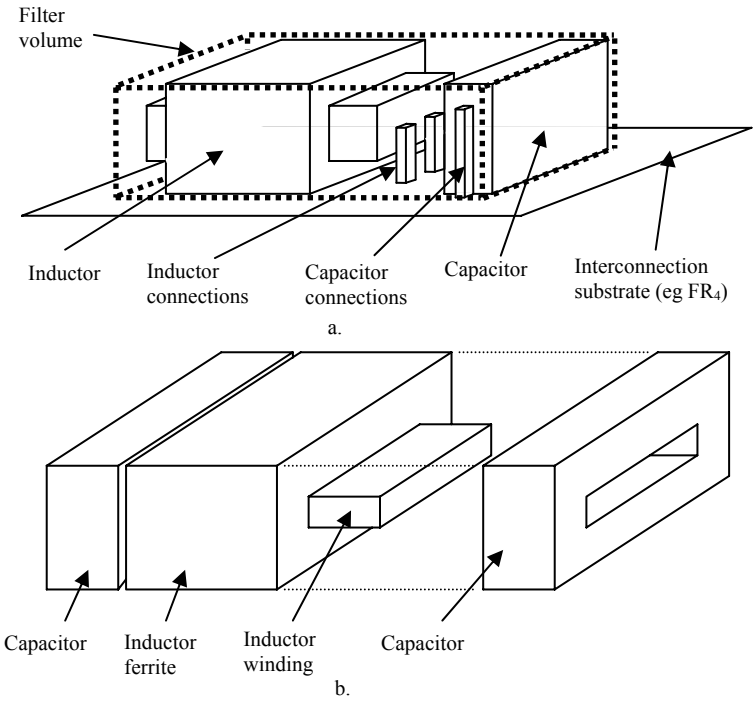


Figure 5-21 Spatial reshaping of capacitors in a low pass filter [Ger02] a. conventional construction b. geometrically packaged

[Fer00] implements the spatial packaging technique by shaping the magnetic core to enclose the whole converter, providing protection and electromagnetic shielding.

5.7 Summary

In this chapter technologies that can be used to increase the level of functional and PEs integration in power electronic converters were presented. Technologies were classified and presented according to the primary function that they implement in power electronic converters. Section 5.2 and Section 5.3 presented the integration potential of substrate technologies, ceramic and organic substrates respectively. Section 5.4 described the integration potential of interconnection technologies while Section 5.5 dealt with protection technologies. Finally, Section 5.6 dealt with technologies that implement FEs and the integration potential thereof.

For each technology the basic principle, manufacturing processes and materials were described. The intention was not to provide detailed descriptions of processes and materials involved but rather to present them in the light of the integration methods from Chapter 4 (Table 4-1).

Table 5-1 shows the list of technologies and the integration methods that they implement. As already pointed out in the chapter, the technologies that allow for integration of FEs consequently lead to integration of PEs but this is not explicitly shown in the table.

Technologies presented here certainly do not cover all the available technologies that can be used for integration in power electronics. The purpose of this chapter is to present the most prominent technologies and their integration potentials and illustrate what merits of a technology can be exploited in order to achieve a higher level of integration. This can lead to identifying needs and developing new technologies to fulfil these needs. More importantly, this can assist in identifying integration potentials in existing, commercially available technologies.

Table 5-1 Integration technologies and corresponding methods

Method / Technology		FEs integration			PEs integration			
		Method 4.3.1	***Method 4.3.2***	***Method 4.3.3***	***Method 4.4.1***	***Method 4.4.2***	***Method 4.4.3***	***Method 4.4.4***
Ceramic substrate technologies	Thick film		X			X		
	Thin film		X			X		
	LTCC		X	X	X	X		
	DBC				X	X		
Organic substrate technologies	PCB		X	X	X			
	IMS				X		X	
Interconnect. technologies	Planar metallization				X	X	X	
	Laminated bus bar			X	X			
	Lead frame			X	X	X		
Protection technologies	Chip-on-board						X	
	MID			X	X			
	Metal housing			X	X	X		
Functional elements integration technologies	Monolithic integration	X						
	Electromagnetic integration	X						
	Spatial packaging					X		X

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Chapter 6: Evaluating the construction technologies of power electronic converters

6.1 Introduction

In Chapter 3, an approach to improving the construction technology of power electronic converters by increasing the level of integration was introduced. The formal methods for increasing the level of integration were developed in Chapter 4 and technologies that allow for embodying these methods were reviewed in Chapter 5. Implementing the integration methods in different technologies will result in different construction technology concepts. A method of evaluating the different options according to a number of criteria in order to choose the best solution for the particular application is presented in this chapter.

The method is based on the set of mathematical techniques referred to as decision theory. The basic terms used in decision theory and their counterparts in the construction technology of power electronic converters will be outlined in Section 6.2.

Section 6.3 introduces the criteria that will be used for the evaluation of construction technology options. This section reviews the conventional packaging figures of merit and introduces some other figures of merit. Section 6.4 shows how all the criteria are weighted and included into a single function. The hierarchy tree of objectives obtained from the breakdown of the ultimate cost-effectiveness objective is given in Section 6.5. The means to obtain weighting factors from the preferences of decision-makers are discussed in Section 6.6.

Section 6.7 implements the evaluation method in two case studies: off-line commercial PCB power supplies and power modules. For each case study, two construction technology options are evaluated: the conventional one and the more advanced, integrated option.

The chapter is summarized in Section 6.8.

6.2 Multi-objective evaluation of construction technology of power electronic converters

Let us assume that a number of construction technology options are under consideration for the physical realization of a power electronic converter or a sub-circuit thereof. By the term "construction technology option" a set of fully described aspects of construction technology discussed in Chapter 3 is assumed. This includes both functional and packaging elements technologies and their assembly process in order to make the sub-circuit. These options can

include the conventional discrete approach with each component fully packaged and interconnected on a PCB, bare functional elements that share common packaging elements as seen in power modules, or fully integrated solutions as seen in integrated circuits, resulting in fewer, preferably only one functional element.

Naturally, the question arises which of these options is optimal for the particular application. Each option has its pros and cons and hardly ever can one give an immediate answer. Due to the complex and multidisciplinary nature of power electronic converters construction technology combined with the often contradictory requirements of the application, evaluating construction technology options is a difficult task. A number of evaluation criteria have to be taken into account in order to get to an objective result. For example, the advantage of the discrete approach is its maturity and wide commercial availability, while integrated solutions offer a size reduction and potential for cost reduction due to fewer parts and common manufacturing processes. Also, for different applications, different criteria are more important. For example, in consumer applications, the cost criteria will be crucial, while in the case of military or space applications, criteria such as reliability and size constraints will be predominant.

In order to choose the optimal solution, all these criteria must be taken into account while including the level of their importance for the particular application. A set of analytical techniques collectively called *decision theory* [Fre88] deals with these types of problems; hence its methods will be used to deal with the problem of choosing the optimal construction technology among a number of alternatives for the specific application. Let us first introduce the terminology used in decision theory and apply this terminology to our case.

Introduction to Decision Theory

When faced with a number of possible options for a particular problem, decision theory refers to these options as *alternatives*. In order to compare them and choose the optimal one, the alternatives are represented by a vector of levels against a number of important factors. These factors are referred to as *criteria* or *decision rules*. An *objective* is a dimension together with an indication of the "good and bad" ends of the dimension. For example, "minimise product cost" is an objective that indicates that low costs are preferred. Objectives are often competitive – i.e. an improvement in one of them leads to a deterioration in another. This occurs either because of limited resources, physical limitations or other constraints. Expressed in this terminology, the task of decision theory techniques is to rank the alternatives by using criteria that are consistent with decision-makers' objectives and preferences. Since there is more than one criterion, the technique is referred to as multi-criteria decision-making or multi-objective decision-making.

Decision theory techniques are used in a very broad range of engineering applications, such as problems of transmission and distribution of electrical power [Che98], traffic assignment [Tze93], electromagnetic design problems [Dia02], induction motor design problems [Liu03] etc. [Qis03] presents an application of multi-objective optimization in optimal selection of number of signal layers in Printed Circuit Boards concerning cost, electrical performance and

reliability criteria. [Que98] presents a methodology for optimal placement of convectively cooled electronic components on Printed Circuit Boards concerning thermal behaviour and total wiring length on the PCB.

Decision theory terms in construction technology of power electronic converters

Let us translate the decision theory terminology into terms used in the power electronics construction technology domain. *Construction technology options* as introduced at the beginning of this section represent *alternatives*. In this chapter these options will be treated as given inputs. The means of obtaining them through the design algorithm will be presented in Chapter 7. *Objectives* are low cost, high performance, small volume etc. The *figures of merit* used in the benchmarking of packaging of power electronic converters such as power density, thermal density, component density and the quantities that will be introduced in the next section represent decision *criteria*. The means of choosing the optimal alternative by weighting all the criteria with corresponding coefficients into a single value function will be shown in Section 6.4.

6.3 Evaluation criteria – Construction technology figures of merit

In few decision problems is there a natural structuring of the alternatives as vectors of criteria levels. Hence, the decision-makers must use their insight into the actual problem to achieve this. This is certainly the case in the problems of choosing optimal construction technology. As in most situations, the ultimate objective in this case is cost-effectiveness, which means obtaining an effective solution to the given problem for the lowest possible cost. As this objective is rather intangible, the next challenge is to break this objective into a number of criteria that reflect the ultimate objective.

This ultimate objective will be broken down into only the criteria that are influenced by the construction technology choice. For example, the choice of topology in designing a power electronic converter has a significant impact on its performance and cost, but this is not directly related to the construction technology since the same topology can be realized in a number of construction technology options. Another example is potential changes in the power electronics market caused by changes in systems where power electronics is to be used. These changes largely affect both cost and performance of power electronics converters but do not come from construction technologies and hence will not be taken into account.

Furthermore, in the process of breaking down the cost-effectiveness objective some criteria might appear that are qualitative in their nature or difficult to quantify. However, these effects must be quantified in order to include them into the final value function. The method of quantifying such fairly nebulous effects by means of *proxy variable*, which one expects to be highly correlated with the effect, is common in decision theory.

Before we move on to breaking the ultimate objective into criteria, let us look at the already existing criteria used in the literature to benchmark physical realization of power electronics

converters. Afterwards, some non-conventional criteria will be introduced in order to cover all the evaluation aspects.

6.3.1. Conventional packaging figures of merit

From the time when the importance of the physical realization of power converters was recognized as an important constituent in power electronics technology, a few benchmarking studies have been conducted in order to determine the current status of construction technology in power electronics [Che02][Mat04]. This is accomplished by evaluating a considerable number of case studies based on several figures of merit (FOMs). Furthermore, these FOMs are used for the evaluation of novel integration and packaging concepts [Str03][Fer02]. In the following text, the FOMs used in these studies and in the literature in general are presented.

Power density

Power density of a power electronic converter is defined as the ration of the rated power (P_{rated}) of the converter to the converter volume (V_{conv}):

$$Power\ density = \frac{P_{rated}}{V_{conv}}\ [\mathrm{W/m^3}] \tag{6.1}$$

This FOM is frequently used in benchmarking power electronic converters, in particular dc-dc converters.

In certain cases, such as power modules, a variation of this FOM expressed as the rated power of the module per its base plate area, A_{base_plate}, is used [Sem]:

$$Power\ density = \frac{P_{rated}}{A_{base\_pl}}\ [\mathrm{W/m^2}] \tag{6.2}$$

However, when comparing two converters, this FOM does not give any information about the operating conditions of the converter, such as the temperature of the heat exchanger (base plate in the case of power modules, ambient temperature in the case of natural convection-cooled PCB power converters etc.). This is an important drawback since the power level that the converter can handle is mostly limited by the maximum operating temperatures of the components.

Thermal density

In order to overcome the shortcomings of power density, another FOM is used. Thermal density is defined as the converter's power dissipation (P_{loss}) related to its base plate area (A_{base_pl}):

$$Thermal\ density = \frac{P_{loss}}{A_{base\_pl}}\ [\mathrm{W/m^2}] \tag{6.3}$$

This FOM, as defined in (6.3), is applicable to cases where it can be assumed that all the heat dissipated by the converter is conducted through the base plate and then exchanged to the environment.

Component density

Component density is defined as number of components (N_{comp}) related to the converter area (A_{conv}):

$$Component\ density = \frac{N_{comp}}{A_{conv}}\ [\mathrm{m}^{-2}] \tag{6.4}$$

where the converter area is the size of the PCB for low power converters assembled on a PCB or the base plate area for the power modules. This FOM, as defined, is inherited from the PCB metrics where it is desired to place the discrete components as close to each other as possible in order to reduce the size of the circuit. However, with integration, the number of "components" will decrease and this FOM loses its meaning.

6.3.2. Other figures of merit

Volumetric packaging effectiveness

Since high power densities have become a high priority objective in emerging power electronic applications, it is desirable to have the "non-functional" volume in a converter reduced to minimum or to package the functional elements as effectively as possible. *Packaging efficiency* in microelectronic packaging is introduced as percentage of area in an interconnection substrate that is occupied by silicon. Analogous to this definition and taking into account the specific nature of power electronics, including the variety of components including passive components and the importance of the third dimension or volume for power processing, *Volumetric packaging effectiveness* can be introduced as percentage of volume in a converter that is occupied by functional elements [Pop03]:

$$\eta_v = \frac{V_{FE}}{V_{conv}} \tag{6.5}$$

where V_{FE} is the volume occupied by functional elements and V_{conv} is the total converter volume.

Thermal management effectiveness

In contrast to the well-established FOMs for electrical performance, the thermal performance of power electronic converters is usually expressed in temperature profile combined with power and thermal density. In [Jon04], this problem is addressed, and two FOMs are introduced in order to evaluate the thermal performance of power electronic converters: *thermal management loss density* (TMLD) and *thermal design rating* (TDR). Thermal

management loss density is defined as the ratio of the total electrical losses and volume that participates in thermal transport and is intended to show how intensive the thermal management is functioning. The second FOM, thermal design rating, is defined as a function that evaluates how close the components in the converter operate to their thermal optimum.

6.4 Construction technology value function

In a multi-attribute decision-making process, the problem consists in choosing an alternative (or a number of them) from among a set of alternatives that optimizes the vector of objectives. Each alternative is represented by a vector of levels against criteria:

$$\mathbf{a} = (a_1(\mathbf{a}), a_2(\mathbf{a}), ..., a_k(\mathbf{a})) \tag{6.6}$$

The goal of the decision process can be expressed as finding the alternative **a** that satisfies the following condition:

$$\max_{\mathbf{a} \in S} a_1, a_2, ..., a_k \tag{6.7}$$

where S is the set of alternatives, while a_i are the criteria expressed in numbers. It can be noticed that it is assumed in (6.7) that all the criteria should be maximized. If the criteria i should be minimized instead, this can be translated into max (- a_i), hence there is no loss of generality. An ideal solution would be an alternative $\mathbf{a}^* \in S$ such that

$$a_i(\mathbf{a}) \le a_i(\mathbf{a}^*) \quad \forall i \in \{1, ... k\} \quad \forall \mathbf{a} \in S \tag{6.8}$$

which means that the alternative $\mathbf{a}^*$ is superior to the other alternatives for all the criteria. However, this rarely happens in practice since the evaluation criteria are often competitive or in conflict with each other.

There are a number of approaches in the literature for solving this type of problem. They range from methods where consequences of each alternative are known (decision under certainty) such as Pareto optimality, methods where consequences of the alternatives are known with certain probability (decision under risk) such as multi-attribute utility analysis [Fre88] to methods where probability distributions of consequences are unknown (decision under uncertainty).

For an alternative to be optimal, it has to fulfil the requirement of being a Pareto undominated set. An alternative $\mathbf{a}^*$ is Pareto undominated if no $\mathbf{a} \in S$ exists such that:

$$a_i(\mathbf{a}) \ge a_i(\mathbf{a}^*), \quad \forall i \in \{1, ..., k\} \tag{6.9}$$

and

$$a_j(\mathbf{a}) < a_j(\mathbf{a}^*) \tag{6.10}$$

for at least one index $j \in \{1, 2, ..., k\}$.

The most frequently used method is based on a single utility function which summarizes the different criteria into a single objective function, referred to as *ordinal value function*. One of the methods that belong to this group is the weighting method. In this method, the ordinal value function is defined as:

$$v(\mathbf{a}) = w_1 \cdot a_1^{norm}(\mathbf{a}) + w_2 \cdot a_2^{norm}(\mathbf{a}) + ... + w_k \cdot a_k^{norm}(\mathbf{a}) \tag{6.11}$$

where criteria $a_i^{norm}(\mathbf{a})$ are criteria $a_i(\mathbf{a})$ normalized by the normalization formulas:

$$a_i^{norm}(\mathbf{a}) = \frac{a_i(\mathbf{a}) - a_i^{\min}}{a_i^{\max} - a_i^{\min}} \text{ if the criteria } a_i \text{ needs to be maximized and} \tag{6.12}$$

$$a_i^{norm}(\mathbf{a}) = \frac{a_i^{\max} - a_i(\mathbf{a})}{a_i^{\max} - a_i^{\min}} \text{ if the criteria } a_i \text{ needs to be minimized,} \tag{6.13}$$

while w_i are the weighting factors of the criteria i, while a_i^{max} and a_i^{min} are the maximum and minimum values of the criteria a_i in the chosen set of alternatives. In further text, this function will be referred to as *construction technology value function.* The sum of the weighting factors equals one

$$w_1 + w_2 + ... + w_k = 1 \tag{6.14}$$

Substituting $w_k = 1 - w_1 - w_2 - \ldots - w_k$, for $k = 3$, thus if there are three evaluating criteria, (6.11) becomes:

$$v(\mathbf{a}) = w_1 \cdot a_1^{norm}(\mathbf{a}) + w_2 \cdot a_2^{norm}(\mathbf{a}) + (1 - w_1 - w_2) \cdot a_3^{norm}(\mathbf{a}) \tag{6.15}$$

The value function is calculated for all the alternatives and represented on a 2-D diagram with the weighting factors w_1 and w_2 on the axes and the areas for optimal alternatives. The results of such an example are shown in Figure 6-1. It can be seen that the alternative $\mathbf{a_1}$ is the optimal alternative for the largest range of the weighting factor values, followed by the alternatives $\mathbf{a_2}$ and $\mathbf{a_4}$, while the alternative $\mathbf{a_6}$ is the optimal alternative in only a small range of the weighting factors. Such a small optimality area shows that the optimal solution is very sensitive to the weighting factors selection. In other words, small changes in the weighting factors might change the optimal solution. On the other hand, if the optimality area is large, the optimal solution is stable in given ranges of the weighting factors. Furthermore, it can be noticed that the alternatives $\mathbf{a_3}$ and $\mathbf{a_5}$ are not the optimal alternatives for any range of the weighting factors,

which means that they are dominated alternatives or that they do not belong to the Pareto-optimal set of alternatives.

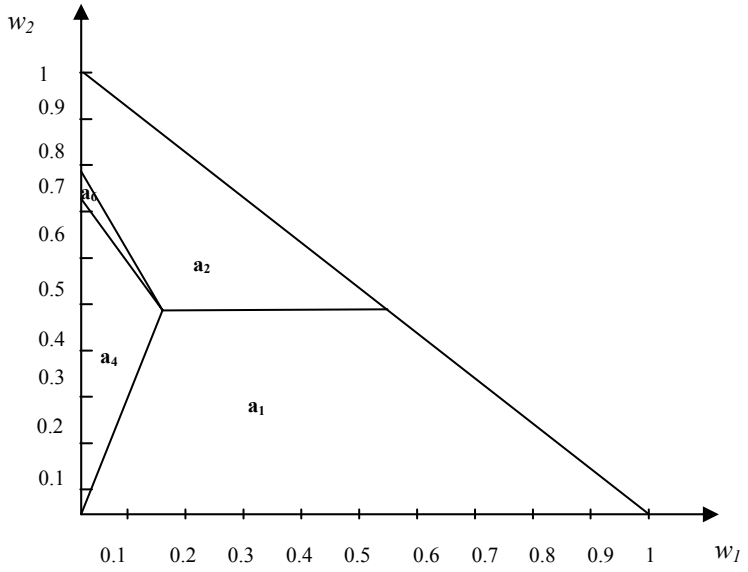


Figure 6-1 Optimal alternatives vs. weighting factors

6.5 A breakdown of objectives

As mentioned in Section 6.3, the ultimate objective cost-effectiveness is intangible by itself and has to be broken down into quantifiable criteria that the decision-maker can deal with. Creating such a breakdown is not an easy task in real applications [Poy98]. It should include all relevant aspects and yet still be as simple as possible. The criteria should be independent of each other in order to apply the linear methods (such as the weighting method). The criteria tree should also represent the opinion of the decision-makers. Figure 6-2 shows a possible hierarchy tree of objectives, starting from the ultimate cost-effectiveness to the final evaluation criteria that can be quantified. The cost-effectiveness objective is split up into two objectives: cost and performance.

Cost

Conventional methods used to describe the costs associated with a product usually deal with manufacturing costs incurred in the form of either labour or material [Bro99]. These costs are usually classified as being direct or indirect. Direct labour is the cost of all “hands-on” activities associated with the manufacture of the product. Typical direct labour activities include fabrication procedures, assembly, testing/troubleshooting, inspection and rework/repair efforts. Similarly, direct material costs consist of the costs of all the materials that are included in the end product that is being produced. Examples include PCBs, passive and active

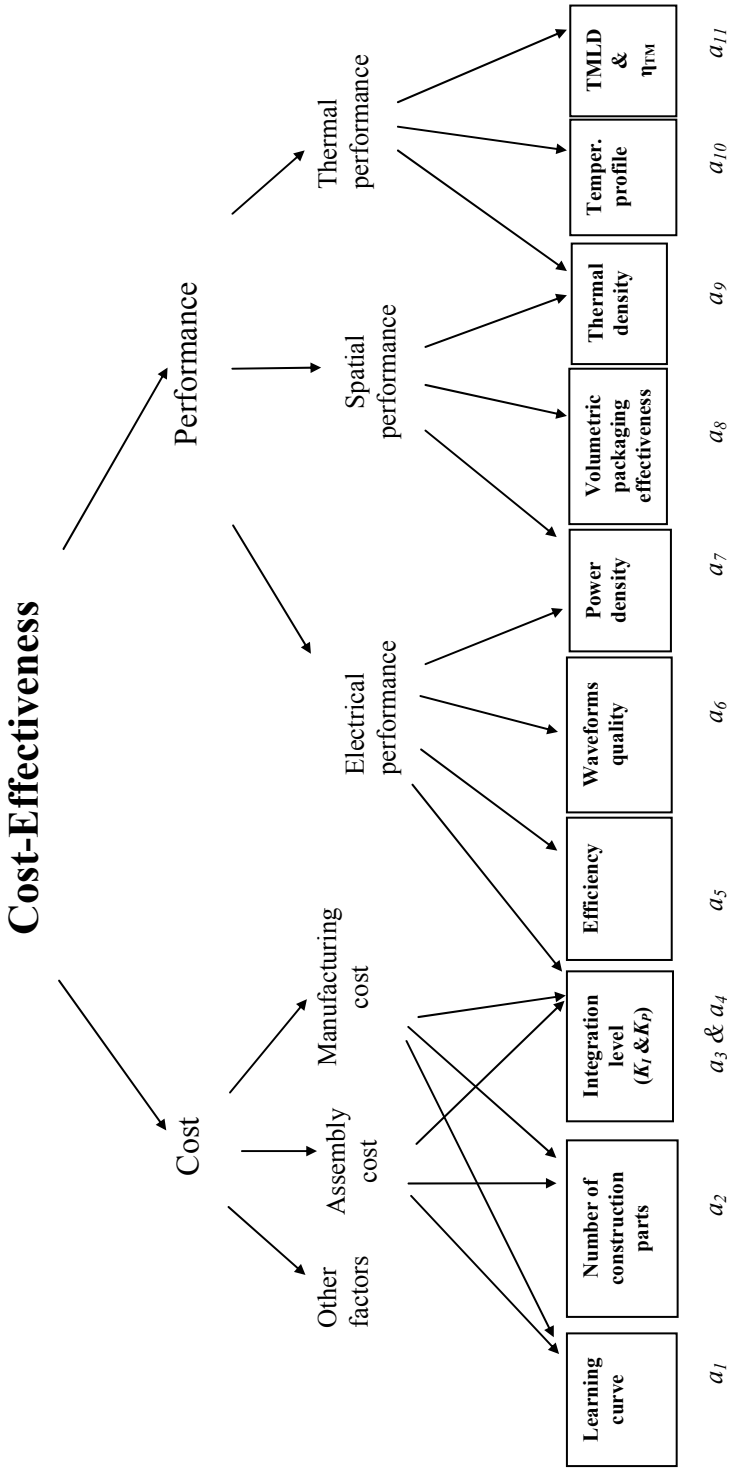


Figure 6-2 A hierarchy tree of objectives

components, and materials used in placing components on PCB. Indirect labour is all the labour that is not direct. Examples include costs for management/supervision, accounting, engineering, labour costs to support clean room facilities, etc. Indirect labour is an integral part of what most organizations consider to be manufacturing overhead. Other components of overhead costs include building and equipment depreciation, insurance, utility costs, etc. For our purposes, the total cost is classified into three groups:

- Manufacturing costs – costs resulting from manufacturing converter parts, both material and processing costs;
- Assembling costs – costs originating from joining of parts to form the complete product, including both assembly materials and processes;
- Other factors (overhead, production line setup and maintenance etc.).

Apart from the requirement that the evaluation criteria are quantifiable, it is important that they are available to the decision-maker. Hence, although certain criteria such as manufacturing cost and assembling cost are essentially quantifiable (expressed in currency units) they are rarely known to the decision-maker or designer. There are two main reasons for this: one is that these values depend on a large number of factors (production quantity, market trends, technology learning curve etc.). The second reason is that the decision is to be made in the converter design phase, before the actual converter is constructed. Therefore, these criteria are represented by other, more tangible criteria: number of construction parts and level of integration (functional and packaging). The importance of the number of construction parts in the converter realization was discussed in Chapter 3.

Performance

Based on the requirements that the system level products impose on power electronics converters, the performance objective is split up into three criteria: electrical performance, thermal performance and spatial performance.

The electrical performance objective is split up into a number of widely used quantitative criteria that describe electrical behaviour of power electronic converters, such as electrical efficiency, waveforms quality (input/output voltage ripple, over/under shoot), transient response, etc. [Moh03][Che02][Mat04].

The thermal performance objective is split up into the FOMs introduced in Section 6.3, such as thermal density, thermal management effectiveness FOMs, temperature profile etc.

The spatial performance criterion is further split up into power density and volumetric packaging efficiency. For a converter implemented in two different construction technology options, the power density values show how converters' volumes compare to each other for the same power rating, while the volumetric packaging effectiveness values indicate how effectively the converter volume is utilized by its functional elements.

Furthermore, integration level (both functional and packaging elements) is chosen as a criterion that will represent both manufacturing and assembling cost and electrical performance. The

benefits of integration from these two factors' viewpoints were already discussed in Chapter 4. In a nutshell, if a number of parts (functional or packaging elements) are integrated into one, fewer parts will be used, which results in reduced manufacturing costs, since there are fewer parts to fabricate and lower assembly costs since there are fewer parts to connect. Also, the electrical performance is expected to improve due to the reduction in parasitic elements values, reduced losses etc, hence the levels of FEs and PEs integration are chosen as the electrical performance FOMs as well.

6.6 Methods for obtaining weighting factors

As given in (6.14), the sum of the weighting factors is equal to one. The motivation for this is that the decision-maker is usually asked to divide the 100% importance between the different criteria. These percentages are then selected as weights. The problem arises from the fact that the decision-maker as a rule does not have a quantifiable opinion about the relative importance of the different criteria [Tok98]. In that case, a sensitivity analysis has to be performed in order to see how the solution depends on the particular weight selection (as shown in Figure 6-1).

There are a number of methods available for obtaining weighting factors. The most frequently used methods will be briefly described here. The more detailed descriptions are available in the literature on decision theory [Poy98][Fre88][Kee76]. The weighting factors are elicited either by weighting all the lowest level criteria simultaneously (non-hierarchical weighting) or by weighting criteria within one branch at a time and multiplying the local values through the value tree (hierarchical weighting) (Figure 6-3). With non-hierarchical weighting, the decision-maker does not have to weight the mid-level criteria, but the problems occur in real applications when the number of criteria is large.

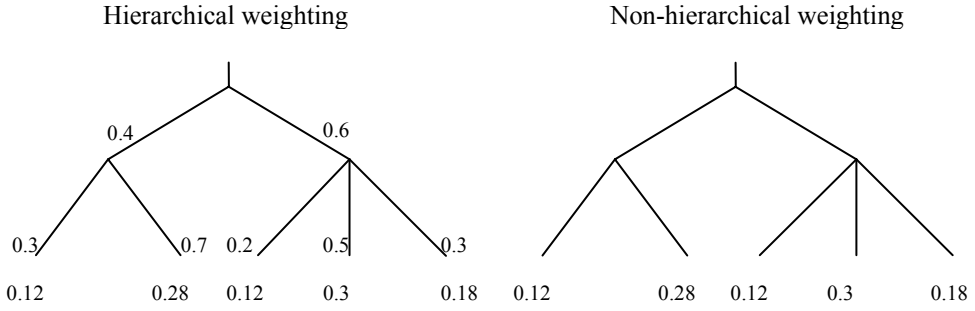


Figure 6-3 Hierarchical and non-hierarchical weighting methods

The most frequently used methods are: Simple Multi-attribute Rating Technique (SMART), SWING, Analytic Hierarchy Process (AHP), TRADEOFF etc. All these weighting methods are based on comparing two criteria at a time. In the SMART method, the weighting factors are obtained in two steps: rank the importance of the changes in the criteria from the worst criteria level to the best and then make ratio estimates of the relative importance of each criteria relative to the one ranked lowest in importance. The decision-maker is asked to assign 10

points to the least important criteria. The importance of the other criteria is evaluated by giving them points from 10 upwards.

In SWING, the decision-maker is asked to consider a situation where he faces a hypothetical alternative that all the criteria are at their worst levels. First, the decision-maker is asked to move one attribute to its best level and assign it 100 points. Next, he is asked to choose an attribute change from the worst to the best level which he considers to be the second most desirable improvement and to assign points less than 100 to that attribute. This procedure is continued with all the remaining attributes.

In the TRADEOFF method, the decision-maker compares two hypothetical alternatives that differ in two criteria only. The other criteria are kept on the same, fixed levels. The decision maker is asked to consider two hypothetical alternatives, $\mathbf{a_1}$ and $\mathbf{a_2}$, and to adjust one of the attributes until the alternatives become equally preferred. That results in:

$$w_1 \cdot a_1^{norm}(\mathbf{a}_1) + w_2 \cdot a_2^{norm}(\mathbf{a}_1) = w_1 \cdot a_1^{norm}(\mathbf{a}_2) + w_2 \cdot a_2^{norm}(\mathbf{a}_2) \tag{6.16}$$

This procedure is repeated for the rest of the criteria, which results in k-1 equations. This combined with the (6.14) gives the total of k equations, which is sufficient for obtaining k weighting factors.

The AHP procedure is based on estimates of weight ratios similarly to SMART and SWING. The decision-maker is asked to compare the importance of two attributes at a time by determining which one is more important and how many times. The decision-maker gives weight ratios to indicate the strength of their preferences by using integers from 1 to 9.

[Poy98] shows that all the weighting methods are equally applicable to practical implementation and no preferred method has been established yet. However, all the methods are subject to certain phenomena that occur due to the features of the weighting procedures. These are referred to as behavioural biases. These include influences of changes in structuring the criteria tree on weighting factors. This means that the weighting factors change if certain criteria are split up into sub-criteria, which theoretically should not occur.

The weighting procedures can be implemented in a computer program in order to accelerate and simplify obtaining results. There are a number of software packages available [SAL]. For our purposes, web-based software decision analytic problem structuring, multi-criteria evaluation and prioritization Web-Hipre [Mus00] will be used. The program supports the following weighting methods: direct weighting (non-hierarchical weighting), SMART, SWING, SMARTER (successor of SMART) and AHP. Furthermore, it is possible to combine these methods, i.e. to use different weighting methods on different criteria levels.

6.7 Case studies

The method presented in the previous sections will be implemented in two case studies. Two categories of power electronic converters are chosen: commercial off-line PCB power supplies and power modules. In both categories two construction technology alternatives will be analysed: a conventional, state-of-the-art construction technology option and a more advanced integrated solution.

6.7.1. PCB power supplies

The salient features of PCB-assembled power supplies were discussed in Chapter 2. These assemblies are mostly found in the low power level range (up to a few hundred watts) in commercial applications. In these applications, the cost criterion is crucial and the size is also important since the space allocated for the power electronics in applications such as DVD players, set-top boxes etc. is limited. On the other hand, the ambient temperature is normally around 50 °C, hence the margins in which components are supposed to operate are in general larger.

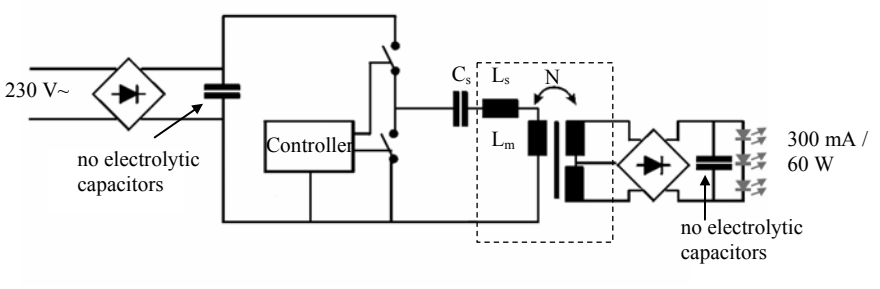


Figure 6-4 PCB power supply circuit schematic [Neu04]

The circuit to be implemented is a power supply for the background lighting of flat screen monitors by means of light emitting diodes in the form of wide lamps LALS (Large Area Light Source Lamp) [Neu04]. The converter is implemented in an off-line series resonant topology with mains insulation (Figure 6-4), with the following specifications:

- Input voltage: $280V < V_{in} < 360V$;
- Output current: $I_{out} = 300mA$;
- Output voltage: $V_{out} = 200V$.

The application allows propagation of line harmonics, hence large input and output filter capacitors (electrolytic capacitors are mostly used) are not required.

Two possible construction technologies for this circuit are considered: conventional discrete technology and Embedded Passive Integrated Circuit (EmPIC) technology [Waf02]. Firstly, short descriptions of each technology are given. This is followed by adjusting the objectives tree from Figure 6-2 for this application based on the fact that the values of all the criteria for both alternatives have to be known for the evaluation to be performed. Then, both modules are presented as vectors of chosen criteria, i.e. the values of all the criteria are calculated for both

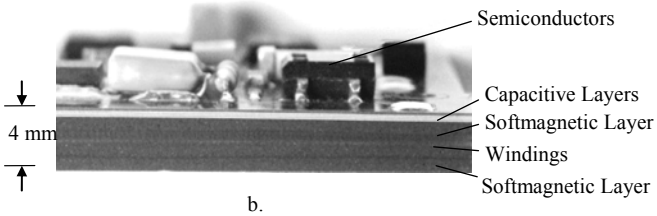
alternatives. This is followed by performing the procedure to elicit the weighting factors for the chosen criteria. The procedure is based on a set of preferences obtained from an expert in this field. Finally, the values of the value function for both alternatives are calculated. Furthermore, a sensitivity analysis is performed in order to investigate how the variations in the weighting factors affect the decision result.

Technology descriptions

Conventional technology: The circuit from Figure 6-4 is conceptually designed with discrete through-hole active components (switches and diodes), through-hole capacitors, and a wire-wound transformer and discrete leaded inductor. The circuit is implemented on a conventional printed circuit board. This construction technology was discussed in Chapter 2.

EmPIC technology: EmPIC technology was discussed in Chapter 5 in relation to the integration potential of printed circuit boards. This technology aims to increase the functionality of printed circuit boards in power electronic converters by integrating layers of materials with enhanced dielectric and magnetic properties into the PCB [Waf02]. This allows for integrating capacitive and magnetic FEs into the PCB. Resistive elements can also be embedded. The circuit from Figure 6-4 is implemented in this technology by integrating the transformer, resonant inductor and 11 capacitors. Beside the resonant capacitor (C_s), the timing and decoupling capacitors (not shown in Figure 6-4) are also integrated into the PCB [Neu04]. The ferrite polymer compound MagLam [Iso] ($\mu_r = 17$, $B_{sat} = 300$ mT) is used to implement the transformer and inductor. The capacitive laminates C-Lam [Iso] (capacitance per area ~ 243 pF/cm^2) are used to implement the capacitors. Figure 6-5 shows the complete assembly and the cross-section of the assembly. As can be seen from the figure, the majority of the components that are not integrated into the PCB (with the exception of the output diodes, two capacitors and a few control components) are implemented in the SMD form.

a.



b.

Figure 6-5 EmPIC construction technology [Neu04] a. complete converter b. cross-section

A hierarchy criteria tree

Figure 6-2 gives us the starting point in creating the hierarchy objective tree. As mentioned in Section 6.5, when a tree of objectives is being created, it is important to keep in mind that the values of the final, lowest-level criteria for each alternative have to be accessible to the decision-maker. Since the analysis is based on the conceptual design of the conventional converter rather than the actual prototype, the waveforms quality, temperature profile and thermal management effectiveness criteria are not available and are therefore omitted from the criteria tree. The modified criteria tree is given in Figure 6-6.

Criteria values for alternatives

Table 6-1 shows the criteria values for both converters. Since only the EmPIC converter was built and tested, the efficiency value of the conventional converter is calculated on the basis of the results of the EmPIC converter. It is assumed that all the components are the same except for the integrated magnetics and capacitors. Hence, the efficiency is calculated as the losses in the EmPIC converter minus the losses in the integrated magnetics and capacitors. The estimated design value of the losses in the discrete components is added to this value. A similar procedure is used to determine the volume and surface area of the conventional converter. The detailed procedure of obtaining the values from Table 6-1 including the calculations of virtual functional and packaging elements is given in Appendix A.

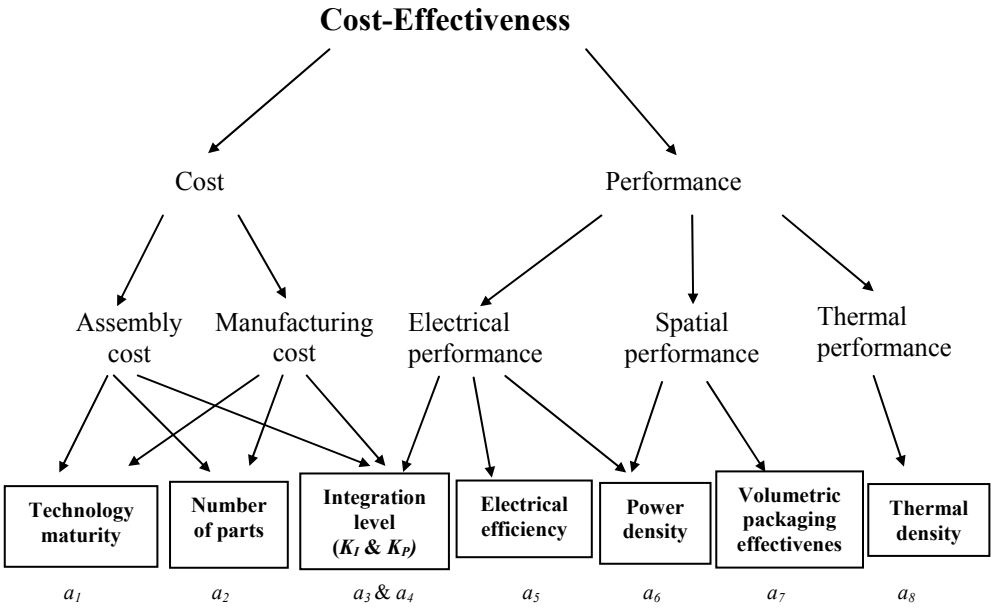


Figure 6-6 A hierarchy criteria tree for PCB power supplies

Table 6-1 PCB power supplies criteria values

Criteria			Conventional converter	EmPIC converter
a_1	Technology maturity		1	0.5
a_2	Number of parts		80	59
a_3	Integration level	K_I	1	2.27
a_4		K_P	1.49	1.58
a_5	Efficiency [%]		91.5	80
a_6	Power density [W/in^3]		11.2	34.4
a_7	Volumetric packaging effectiveness [%]		3.6	34.2
a_8	Thermal density [W/cm^2]		0.12	0.34

It can be seen that the efficiency of the conventional converter is considerably higher than that of the EmPIC converter. This is mainly due to the high losses in the ferrite polymer compound magnetic layers. These materials are in general still in the research phase [Epc][Iso] and one of the main drawbacks is their high losses.

Concerning the integration level, not all the components from the detailed circuit schematic are taken into account. The components that form the main sub-circuit from Figure 6-4 and the capacitors integrated into the PCB in the EmPIC converter are considered. Therefore, the level of functional integration in Table 6-1 will be lower if the whole circuitry is taken into account. The level of functional elements integration is significantly higher in the EmPIC converter due to the multifunctionality of the magnetic and capacitive layers integrated into the PCB. The level of packaging elements integration is also higher in EmPIC converter but not considerably, since there are still a lot of discrete components (MOSFETs, diodes, capacitors, controller and driver) in the considered sub-circuit that contain large numbers of packaging elements.

It can be noticed that the volumetric packaging effectiveness value of the EmPIC converter is ten times larger than that of the conventional one. One of the reasons is the low profile of the EmPIC converter and consequently the smaller total volume. Furthermore, a large percentage of the PCB volume is occupied by the magnetic material, which contributes to the volume of the functional elements.

Weighting factors

Based on the preferences of a PCB power supply expert [Hor05], the weighting factors shown in Figure 6-7 are derived. Depending on the way that the preferences are expressed, three weighting methods are used: SWING, direct rating and mostly AHP. The intermediate steps in determining the weighting factors for the final criteria level (level 3) are also presented. The detailed procedure is given in Appendix A.

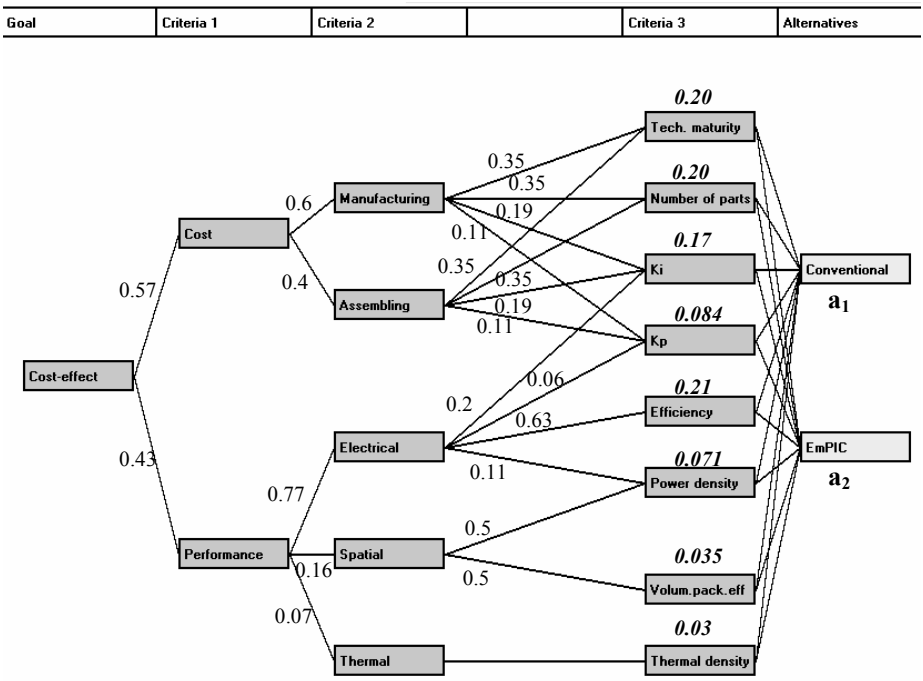
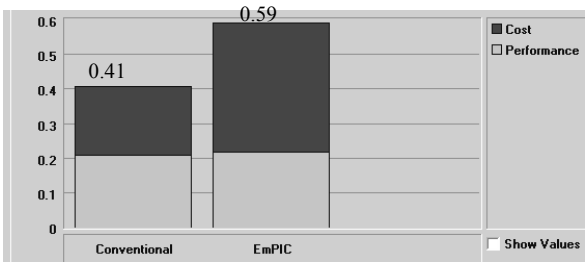


Figure 6-7 Weighting factors for PCB power supplies evaluation

Evaluation results

The criteria values for both alternatives and the weighting factors are substituted in (6.11) by means of Web-Hipre software. Figure 6-8 shows the construction technology value function values for both the conventional and EmPIC implementation. The figure shows the breakdown of this value on all three criteria levels. From Figure 6-8 can be seen that the value of the construction technology value function of the EmPIC implementation ($v(\mathbf{a}_2)$= 0.59) is higher than that of the conventional implementation ($v(\mathbf{a}_1)$= 0.41). Furthermore, from the breakdown in Figure 6-8a it can be noticed that the total performance achievement is comparable between the two alternatives although the EmPIC converter, as can be seen from Table 6-1, has higher values for all the criteria related to performance except for the efficiency criteria. The main reason is the high value of the weighting factor of this criterion and the fact that the efficiency of the conventional converter is considerably larger than that of its more integrated counterpart.

The results presented above stand for the given values of the criteria and weighting factors. However, both of these sets of values can vary. The weighting factors depend on decision-makers' preferences, which are subject to various types of biases as already mentioned. Also, as the criteria values are obtained from the current design, it is expected that if certain aspects of the design are optimized the criteria values may change. For example, using soft magnetic materials with lower losses will increase the EmPIC converter's efficiency. Therefore, before concluding that one alternative is preferred above the other, it is important to analyze how the results will change if the weighting factors and/or criteria values change.



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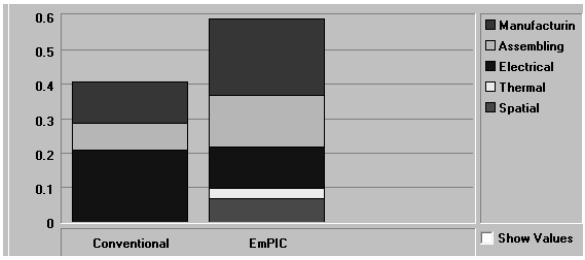

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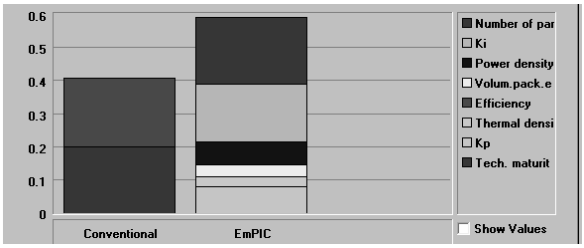
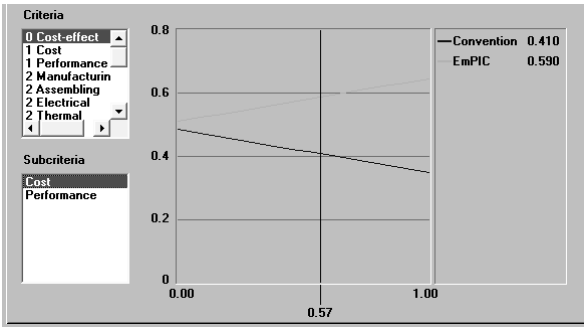


c.

Figure 6-8 Construction technology value function – breakdown on a. criteria level 1 b. criteria level 2 c. criteria level 3

Figure 6-9a shows the sensitivity of the result on the weighting factors for the first-level criteria, more specifically the cost criteria. It can be seen that if the weighting factor for the cost criteria is placed anywhere in the whole range between 0 and 1 the final results remains the same, i.e. the EmPIC converter remains superior to the conventional alternative.

On the other hand, Figure 6-9b shows the sensitivity of the result on the weighting factors for one of the second-level criteria, more specifically the electrical performance criteria. It can be seen from the figure that if the weighting factor for the efficiency criteria varies in the range between 0 and 0.9, the result remains the same. However, if the value of this criteria is larger than 0.9 the conventional alternative becomes more preferred. Since the chosen weighting factor for this intermediate criterion is 0.63, the margin is large enough and the result can be considered stable with regard to this criterion.



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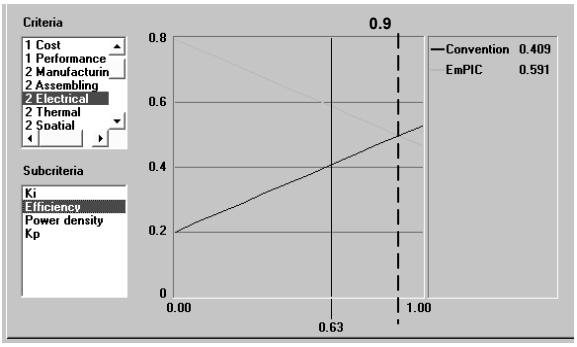


b.

Figure 6-9 Sensitivity analysis a. weighting factors for cost-effectiveness b. weighting factors for electrical performance

Similar analyses are performed for the rest of the weighting factors and the criteria values and it can be concluded that the result of this decision analysis is stable and that the EmPIC construction technology is in this case preferred above the conventional technology.

6.7.2. Power modules

In a power module several power semiconductors (MOSFET or IGBT chips and diode chips) which are electrically isolated from the mounting surface (heat sink) are integrated into a common housing. Various construction technologies of power modules were discussed in Chapter 2.

Two power modules from the same manufacturer [Sem] that implement two different construction technologies are considered: SEMITRANS and MiniSKiiP. The modules have the same sub-circuit configuration (IGBT three phase bridge inverter shown in Figure 6-10) and the same electrical ratings (V_{CES}= 1200V, I_C = 75A).

Like the PCB power supplies case studies, the descriptions of the two implementations will be given first. This will be followed by a multi-objective evaluation of the two alternatives.

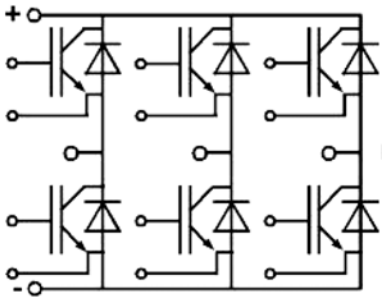


Figure 6-10 Power module circuit schematic [Sem]

Furthermore, a sensitivity analysis is performed in order to investigate how the variations in the weighting factors and criteria values affect the evaluation results.

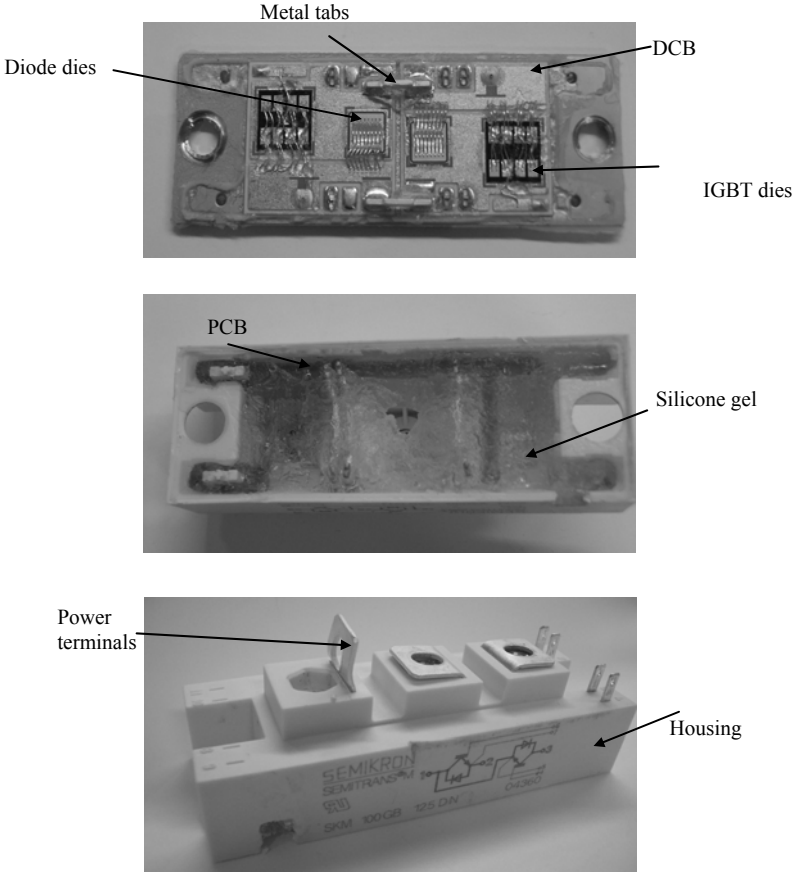


Figure 6-11 SEMITRANS construction technology [Sem]

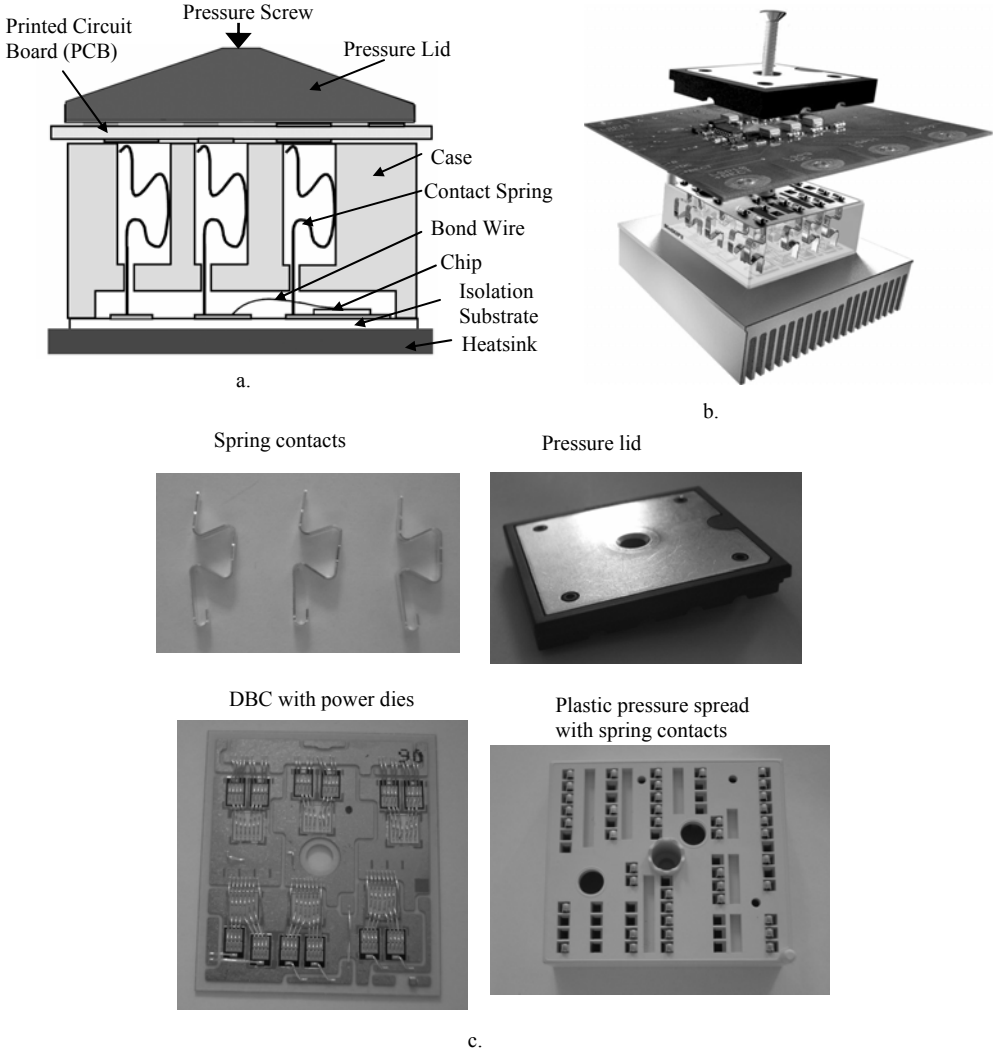


Figure 6-12 MiniSKiiP construction technology [Sem] a. construction principle b. assembly with PCB and heat sink c. module construction parts

Technology description

SEMITRANS technology employs the conventional power module technology, where bare semiconductor dies are soldered onto a DBC substrate. The DBC electrical connections are realized by means of wire bonding. The DBC is then soldered onto a metal base plate for heat-spreading and mechanical support. The power and signal terminals are soldered onto the DBC. Since ceramic substrates are fragile, the circuitry is often realized on two or more DBCs in which case the separate DBCs are connected by means of metal tabs. A PCB that realizes internal electrical connections is also mounted. The assembly is completed by the insertion of a plastic housing onto the module. The module is encapsulated with silicone gel for protection

purposes. The module is then mounted onto the heat sink. The basic parts and construction. principle of power modules in this technology are shown in Figure 6-11 (the module on the figure is a half bridge configuration and is used only to illustrate the construction technology, while for the evaluation a 3-phase bridge "six-pack" is used).

MiniSKiiP technology is based on pressure contact technology. The principle of this technology is illustrated in Figure 6-12. In contrast to conventional transistor modules (including SEMITRANS), the DBC substrates carrying the IGBT and diode chips are not soldered onto a base plate, but are pressed almost with the complete surface directly to the heat sink by means of a plastic pressure spread. The electrical connection of the DCB to the electrical terminals is made by pressure spring contacts that are integrated into the plastic pressure spread. The module is closed with a plastic pressure lid. A metal inlay and pressure cylinders in the lid provide even pressure to the module. As shown in Figure 6-12a and Figure 6-12b, the open space on the underside of the pressure lid can be used to mount SMD components on a PCB that interconnects the module with the outside system. The basic parts and construction principle are shown in Figure 6-12c.

A hierarchy criteria tree

Following the same procedure as in Section 6.7.1, the starting point is Figure 6-2. As mentioned in Section 6.5, when creating an objectives tree, it is important to keep in mind that the values of the final, lowest-level criteria for each alternative have to be accessible to the decision-maker. Also, it is important to establish whether the choice of construction technology affects certain criteria.

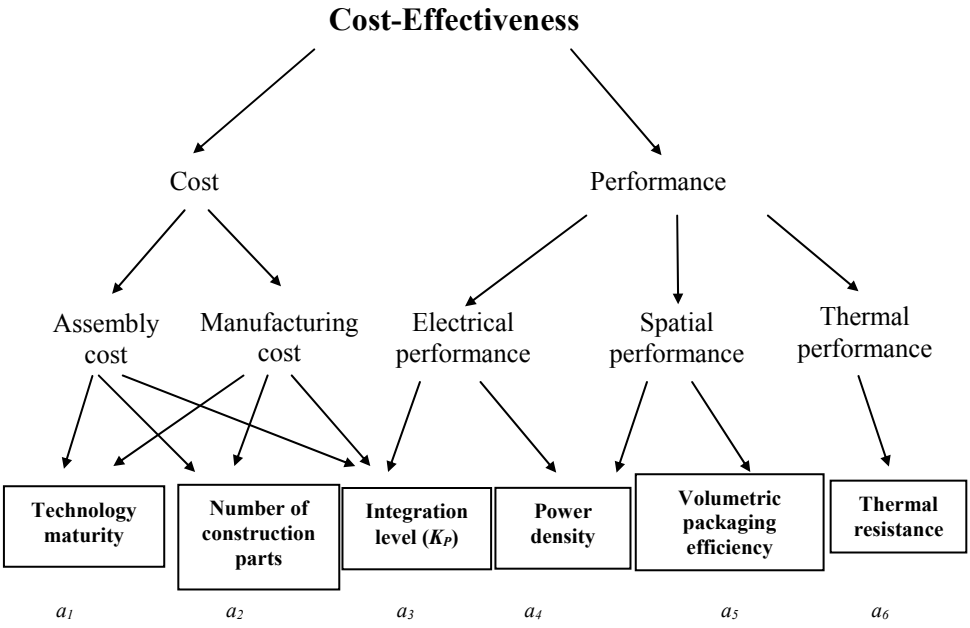


Figure 6-13 A hierarchy criteria tree for power modules

Since the power modules' efficiency in this case is mainly affected by the characteristics of the devices (IGBTs in this case) used in the modules rather than the construction technology, this criterion is omitted. Furthermore, since the temperature profile is not known at this stage, the thermal resistance value that is available from the modules' data sheets is used to indicate the thermal performance of the modules. Also, the parasitic parameters that depend on the layout are not known from the devices' data sheets. Furthermore, since power modules consist of discrete power dies, their level of functional elements integration is equal to 1, and the K_I criteria will not be considered. Taking these considerations into account, the objectives tree from Figure 6-2 is modified to a tree shown in Figure 6-13.

Criteria values for alternatives

Table 6-2 shows the values of all six criteria for both SEMITRANS and MiniSKiiP. It can be noticed that the number of parts in MiniSKiiP is lower than in SEMITRANS. Furthermore, the MiniSKiiP's PEs are more functional, and this results in a higher level of PEs integration. Since discrete IGBT and diode dies are used in both modules, the level of functional elements integration is equal to one in both cases.

Furthermore, the volumetric utilization of both modules is very low – i.e. the functional elements, in this case IGBTs and diodes, occupy less than one percent of the total volume of the module. Power density is calculated as processed power per unit area [Sem]. The detailed procedure of obtaining the values from Table 6-2 is given in Appendix A.

Table 6-2 Criteria values of power modules

Criteria			SEMITRANS	MiniSKiiP
a_1	Technology maturity		1	0.7
a_2	Number of construction parts		30	25
a_3	Integration level	K_I	1	1
		K_P	1.33	1.71
a_4	Power density [W/mm^2]		19.1	29.1
a_5	Volumetric packaging effectiveness [%]		0.14	0.21
a_6	Thermal resistance $R_{th\,(j\text{-}s)}$ [°C/W]		0.37	0.5

Weighting factors

Based on the preferences of a power module expert [Tur05], the weighting factors shown in Figure 6-14 are derived. The AHP weighting method is used for all the criteria levels. The intermediate steps in determining the weighting factors for the final criteria level (criteria 3) are also presented. The detailed procedure is given in Appendix A.

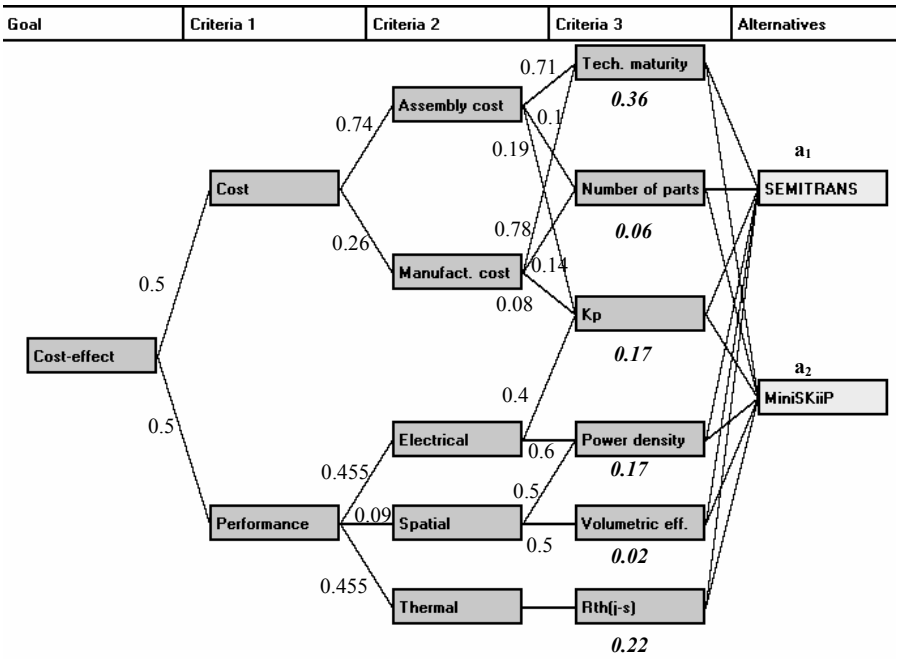


Figure 6-14 Weighting factors for power modules evaluation

Evaluation results

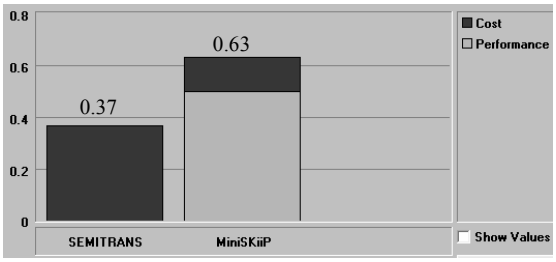
The criteria values for both alternatives and the weighting factors are substituted in (6.11) by means of Web-Hipre. Figure 6-15 shows the values of the construction technology value function for both SEMITRANS and MiniSKiiP modules. The figure shows the breakdown of this value on all three criteria levels. From Figure 6-15 can be seen that the value of the construction technology value function of the MiniSKiiP implementation ($v(\mathbf{a_2})$= 0.63) is higher than that of the conventional implementation ($v(\mathbf{a_1})$= 0.37). Furthermore, the breakdown in Figure 6-15a shows that MiniSKiiP is superior, performance-wise, to the SEMITRANS alternative. This is expected, since MiniSKiiP has higher values in all the criteria related to performance. From Table 6-2 can be seen that SEMITRANS is superior to MiniSKiiP in relation to only one criterion, technology maturity, which is reflected in the breakdown of the value function on the criteria level 2 presented in Figure 6-15b.

As with the procedure with the PCB power supplies, before concluding that one alternative is preferred above the other, it is important to perform a sensitivity analysis to see how the results will change if the weighting factors and/or criteria values change.

Figure 6-16a shows the sensitivity of the result on the weighting factors for the first-level criteria, more specifically the cost criteria. It can be seen that if the weighting factor for the cost criteria is chosen in the range between 0 and 0.68, the final result remains the same, i.e. MiniSKiiP remains superior to the conventional alternative, SEMITRANS. The value of the weighting factor that is obtained from the decision-makers' preferences is 0.5, so if this value

changes with the margin of 0.18, the result remains stable. Figure 6-16b shows how the value of the construction technology value function changes with the change of the weighting factor for the technology maturity criteria. It can be seen that the result is stable over the whole range of possible criteria values.

Similar analyses were performed for the rest of the weighting factors and the criteria values and it emerged that the evaluation result is stable over the whole range of weighting factors and criteria values. From this analysis it can be concluded that the result of this decision analysis is stable within the given margin and that MiniSKiiP construction technology is in this case preferred to the conventional SEMITRANS technology.



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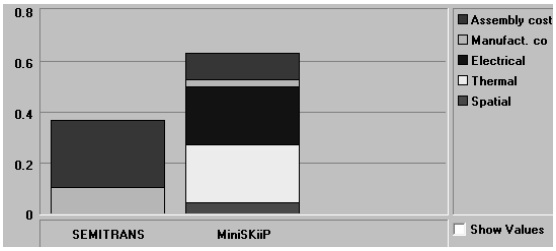

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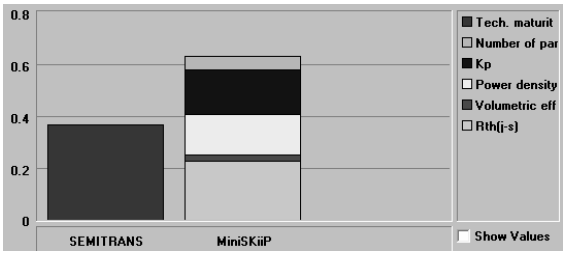
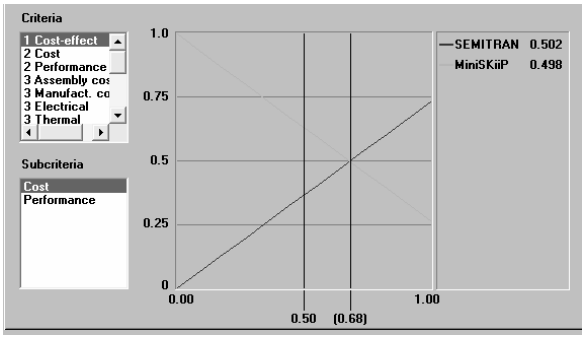


c.

Figure 6-15 Construction technology value function – breakdown on a. criteria level 1 b. criteria level 2 c. criteria level 3



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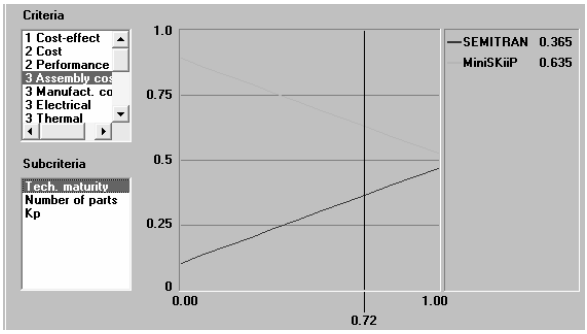

b.

Figure 6-16 Sensitivity analysis a. cost criteria weighting factor b. assembly cost weighting factor

6.8 Summary

In this chapter, a method of evaluating construction technologies of power electronic converters was presented. This method is based on the set of analytical techniques known as decision theory. These techniques allow for the selection of an optimal alternative among a number of alternatives with respect to a number of criteria. The criteria are conventional FOMs such as power density, thermal density, electrical efficiency etc, combined with non-conventional FOMs such as volumetric packaging effectiveness and thermal management effectiveness. The criteria values for each alternative are weighted according to the preferences of the decision-makers and combined into a single function, referred to as the construction technology value function. The methods of extracting weighting factors from the decision-makers' preferences were reviewed. Performing a sensitivity analysis of the evaluation result on variations in weighting factors and criteria values is important since decision-makers' preferences are prone to biases and inconsistencies and criteria values in final products may vary from design values.

The evaluation method was illustrated in relation to two case studies: PCB power supplies and power modules. The weighting factors for the criteria are different in these two cases, based on the preferences of the decision-makers that express the differences between two types of applications. In both cases, the alternatives that use integration technologies were evaluated to

be superior to the conventional alternatives. The procedure is general and can be extended to any application, regardless of its specific nature.

As was shown in Chapter 4 and Chapter 5, there are many possibilities for integration in power electronics. The method presented in this chapter allows for evaluating these possibilities and choosing the optimal one for the particular application. Furthermore, it allows for the direct involvement of the industry, which is expressed in their preferences concerning the importance of different criteria for their application. In this way, the presented method can support the process of converging to a common technology base for similar applications.

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Chapter 7: Design process to increase the level of integration

7.1 Introduction

In Chapter 3, two types of integration were distinguished: functional and packaging elements integration. The quantities that evaluate both levels of integration, functional and packaging elements integration level, were introduced and the formal methods for increasing both integration levels were derived in Chapter 4. Technologies that allow for implementation of these methods in actual converters were reviewed in Chapter 5.

In this chapter, an algorithm that merges the methods from Chapter 4 and integration technologies from Chapter 5 in order to implement them in actual converters is presented.

It was recognized in Chapter 3 that the novel design approach needs to be based on the continuous link between the functional domain represented by the electrical circuit, thermal circuit and electromagnetic design and the physical domain represented by FEs and PEs, throughout the whole design process. In this chapter the means to implement this design approach through the introduced algorithm will be described. In order to position this algorithm in the complete process of the design of a power electronic converter, 7.2 deals with all the steps in the converter design. In Section 7.2.1, the basic principles of design in general are given. This is followed by an identification of the steps in the design of a power electronic converter in Section 7.2.2.

The central part of the chapter is the mapping of the functional domain onto the physical domain and is addressed in Section 7.3. Some considerations regarding the choice of a technology platform for a specific application are given in Section 7.3.1. Once the technology platform is chosen, the design algorithm for exploiting the functionality of the technology base is applied. This algorithm is the subject of Section 7.3.2.

Section 7.4 implements this design process in a case study of a dc-dc converter for automotive applications. Several technology platforms for this application are selected in Section 7.4.2 and the design algorithm is applied to this case study in Section 7.4.3.

The chapter is summarized in Section 7.5.

7.2 Power electronic converters design

7.2.1. Fundamentals of design

Design is often approached as a rather unsystematic process of implementing designer's fundamental knowledge and experience to realize a product that satisfies perceived needs. In [Suh90], a more systematic approach to design applicable to any engineering field is introduced. In its broadest sense, design involves continuous interface between what needs to be achieved and how it can be achieved. The objective of design is stated in the functional domain while the physical solution is generated in the physical domain. The design procedure interlinks these two domains at every level of the design process.

The design's objectives are specific requirements, referred to as functional requirements (FRs). To satisfy these requirements, a physical embodiment characterised in terms of design parameters (DPs) is created. The design process relates the FRs of the functional domain to the DPs of the physical domain. Expressed in these terms, design may be formally defined as "the creation of synthesized solutions in the form of products, processes or systems that satisfy perceived needs through the mapping between the FRs in the functional domain and the design parameters of the physical domain" [Suh90]. The design outputs are in the form of drawings, circuits, software and/or equations that describe the transformation process. From these examples it is clear that the physical and functional domains in this sense should not be mistaken with the physical and functional domains as introduced in Chapter 3. In Chapter 3, these two domains represent literally the domain of physical implementation and the domain of modelling and analysis respectively, while in this design theory connotation the functional domain represents the set of requirements and the physical domain represents the parameters embodiment of these requirements which could be software, drawings etc. In order to avoid misinterpretations, in the following text the terms functional and physical domain will be used in the sense used in Chapter 3.

In addition to FRs, designers often have to take into account certain constraints. There can be many different kinds of constraints such as cost, size or weight and appearance or aesthetic quality. Constraints differ from FRs in that, as long as the product does not exceed the constraints, then the solution is acceptable, whereas a specific range of design values must be maintained for each FR at all times. In other words, the resultant design must be such that constraints can be dependent both on other constraints and on FRs, whereas FRs must be fulfilled regardless of other FRs.

Furthermore, FRs and DPs are hierarchical in nature. This means that FRs cannot be decomposed into the next level of the FR hierarchy without first going over to the physical domain and developing a solution that satisfies the current level of FRs with the corresponding DPs.

Design involves four distinct aspects of engineering and scientific effort:

- Problem definition;
- Creative process of devising physical embodiment;

- Analytical process of determining whether the proposed solution is correct or rational;
- Ultimate check if the designed product satisfies the perceived needs.

The problem definition aspect involves stating the design problem to be solved on the basis of the perceived needs of the system. The creative process depends on the specific knowledge possessed by the designer and the designer's ability to integrate knowledge into synthesizing new solutions. The analytical process complements the creative process by verifying the proposed concepts. The ultimate check provides the verification of whether the designed product meets the original needs.

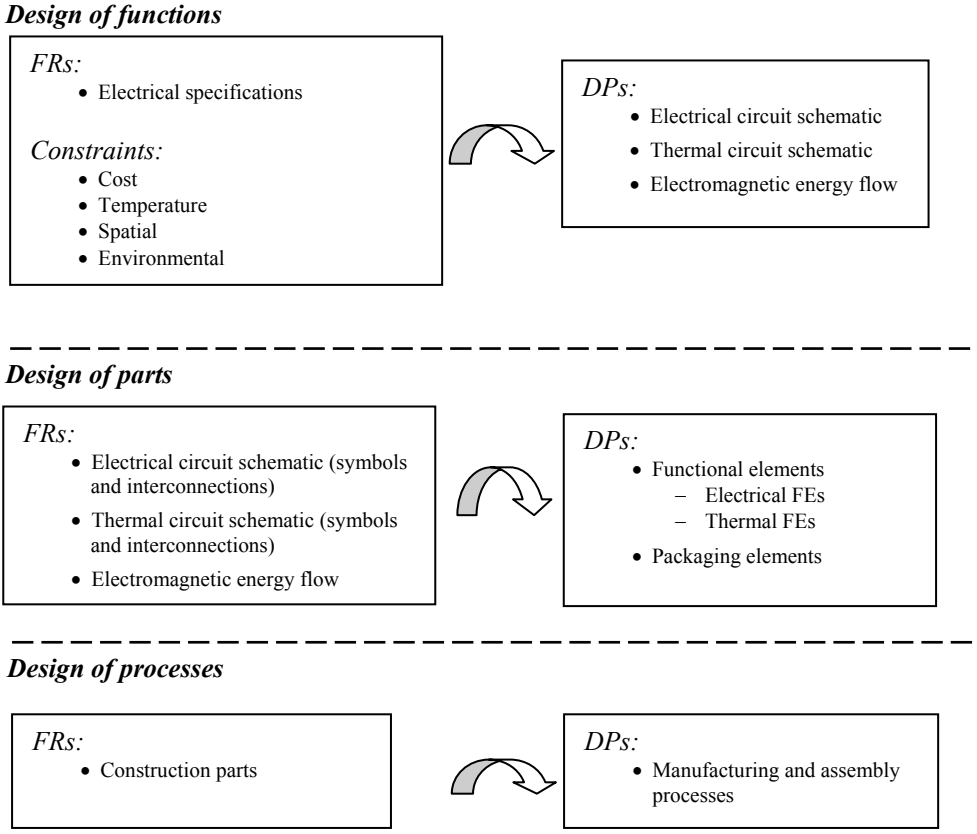


Figure 7-1 Phases in converter design

7.2.2. Phases in the design of a power electronic converter

In the design terms introduced above, the design of a power electronic converter involves linking the input specifications of the converter as its FRs and information about final, manufactured product as its DPs. Design of power electronic converters is also hierarchical in nature. The process of designing a power electronic converter from its input specifications to the final, manufactured product can be broken down into three phases (Figure 7-1):

- Design of functions (electrical circuit, thermal circuit and electromagnetic design);
- Design of parts (design of FEs and PEs that implement circuit symbols);

- Design of manufacturing process (design of processes that allow for manufacturing of converter parts).

Each phase links its FRs to DPs. Furthermore, each phase involves four design aspects outlined in the previous section. Let us consider each phase in more details by analyzing the link between its FRs and DPs.

Design of functions

Design-of-functions includes what is traditionally meant under "design of a power electronic converter". The functional requirements are the electrical specifications describing the required energy conversion form, such as input/output voltages and currents, waveform quality etc. The possible constraints are shown in Figure 7-1 and include cost, temperature constraints (such as temperature of the environment or cooling surface etc.), spatial constraints (maximum volume or dimension), environmental constraints (EMC standards, mechanical requirements) etc.

One set of DPs of this phase is embodied in the electrical circuit schematic. The creative aspect in this phase is in choosing the most suitable circuit topology while keeping in mind the functional requirements. The analysis aspect is performed through modelling of the circuit behaviour. It verifies the topology choice and gives the values or characteristics of the electric circuit symbols as the output.

The second set of DPs is embodied in the thermal circuit schematic. From the electrical circuit schematic, the heat dissipation associated with the electrical circuit symbols can be estimated or the suitable model derived. Taking into account the input temperature constraints, maximum thermal resistances of the heat paths coupled with the circuit symbols can be derived.

The third set of DPs is embodied in the outputs of the electromagnetic design. This includes the electromagnetic field coupling within the converter parts (including effects on losses) and the behaviour of the electromagnetic field at the converter boundaries, which concerns the EMI behaviour of the converter.

In order to get to an optimal solution, the electrical characteristics of the circuit symbols should be specified as a range of values that fulfil the input requirements, rather than as a single value, since the chosen construction technology might limit values that can be realized. This can be expressed in mathematical relationships between two or more circuit symbols.

Design of parts

This design phase includes mapping of this phase's FRs, which are circuit schematic symbols, onto DPs, which are converter construction parts. This phase will be the main focus of this chapter and it is in this phase that the combination of integration technologies and methods for increasing the level of integration is applied.

The outputs of the design-of-functions phase are the inputs to this phase. The FEs are to be implemented to fulfil the requirements of these inputs. Similarly, the PEs are to be realized to

provide the packaging functions. Some packaging functions are specified in the outputs of the first phase – such as electrical interconnections and insulation or thermal interconnection elements. The rest of the packaging functions, protection and support come from the initial mechanical constraints.

The creative part of this design phase consists of choosing technologies for both FEs and PEs, envisaging their 3D realization and mutual spatial arrangement. The analysis part of the phase involves modelling and optimization of the FEs and PEs in order to ensure that they fulfil the functional requirements and satisfy the initial constraints. This aspect is essentially carried out in the functional domain and represents an embodiment of the continuous link between the physical and functional domain as required in Chapter 3.

Design of processes

The inputs to this phase are the construction parts and their spatial arrangement obtained in the design-of-parts phase. This design phase deals with mapping of the construction parts to the processes that will be used to manufacture the parts and assemble them into the final product. The outputs of this phase are embodied in either specifications of existing processes or providing data required to carry out the new process.

7.3 Design of parts – Mapping of functional domain onto physical domain

7.3.1. Selecting a technology platform

This phase starts with selecting technology platforms to implement the FEs and PEs. By the term “technology platform” is meant the technology (or technologies) that is the basis of the circuit construction. For e.g. in the world of integrated circuits, the technology platform is monolithic semiconductor integration; in most low-cost, low-power electronic circuits the technology platform is the Printed Circuit Board and through-hole or surface-mount components etc. A number of technology platforms were presented in Chapter 6.

In order to choose the optimal technology platform (or a library of platforms) for the specific application, the designer has to possess a broad knowledge of available technologies not only in the power electronics domain but also in other engineering fields. Most emerging technologies in power electronics are technologies that originate from other electronic disciplines, since power electronics is rarely a technology driver. The technology platform is chosen based on:

- Functional requirements of the design-of-parts phase:
  - Electrical circuit schematic – the voltage levels determine the required breakdown voltage, the current levels determine the interconnection technology such as conductor width and thickness;
  - Thermal circuit schematic – the maximum thermal resistances of the heat paths determines the technologies used for implementing the heat paths;
- Input constraints:

- Environmental – required mechanical strength, temperature, humidity conditions, vibrations etc;
- Cost – in most applications the cost factor will rule out a technology platform even if it is suitable from the other factors' viewpoints.

7.3.2. Design algorithm for increasing the level of integration in the converter

Figure 7-2 shows the design algorithm for the design-of-parts phase of design [Pop05]. The algorithm consists of four sub-phases:

- Sub-phase 0: Technology platform selection (discussed in the previous section);
- Sub-phase 1: Functional elements integration;
- Sub-phase 2: Packaging elements integration;
- Sub-phase 3: Choosing the best option.

Let us assume that *n* technology platforms suitable for the particular application are chosen. The inputs in the next phase are the chosen technology platforms and the outputs of the design-of-functions phase. The sub-phases 1 and 2 are performed for each technology platform.

Sub-phase 1: Functional elements integration

This sub-phase deals with functional elements integration. As Chapter 5 demonstrated, there are three methods for FEs integration: integration technologies, multifunctional FEs and PEs that act as FEs.

The first step is to identify if there are integration technologies compatible with this technology platform. For example, in ceramic-based technology platforms, thick film printing technologies are an option for the implementation of passive FEs in an integral process. If the answer is positive, the next step is to identify FEs from the circuit schematics that can be realized in this technology. This is again done on the basis of the outputs of the design-of-functions phase, such as current/voltage levels for electrical FEs or thermal resistance for thermal FEs. For the previous example of a ceramic technology platform, FEs suitable for implementation in this technology would be low current, low voltage electrical control passive FEs.

The next step is to envisage the implementation of the rest of the FEs on the basis of the outputs of the design-of-functions phase. Selecting technologies for functional parts belongs to the component technology discipline, including power switch technology, passive component technology and control circuit technology. The outputs of the design-of-functions phase, such as the capacitance or inductance value of the passive component circuit symbol together with design values of currents and voltages or design operating frequency and rated voltages and currents of power semiconductors, are used as the inputs to the FEs manufacturer's database. Furthermore, the chosen FE technologies and technology platform have to be compatible with each other. For example, PCBs cannot accommodate large power components or the thick bus bars are not suitable for small surface-mount components. On the other hand, for low-current, low-voltage electrical FEs (such as control FEs) surface-mount technology might be used.

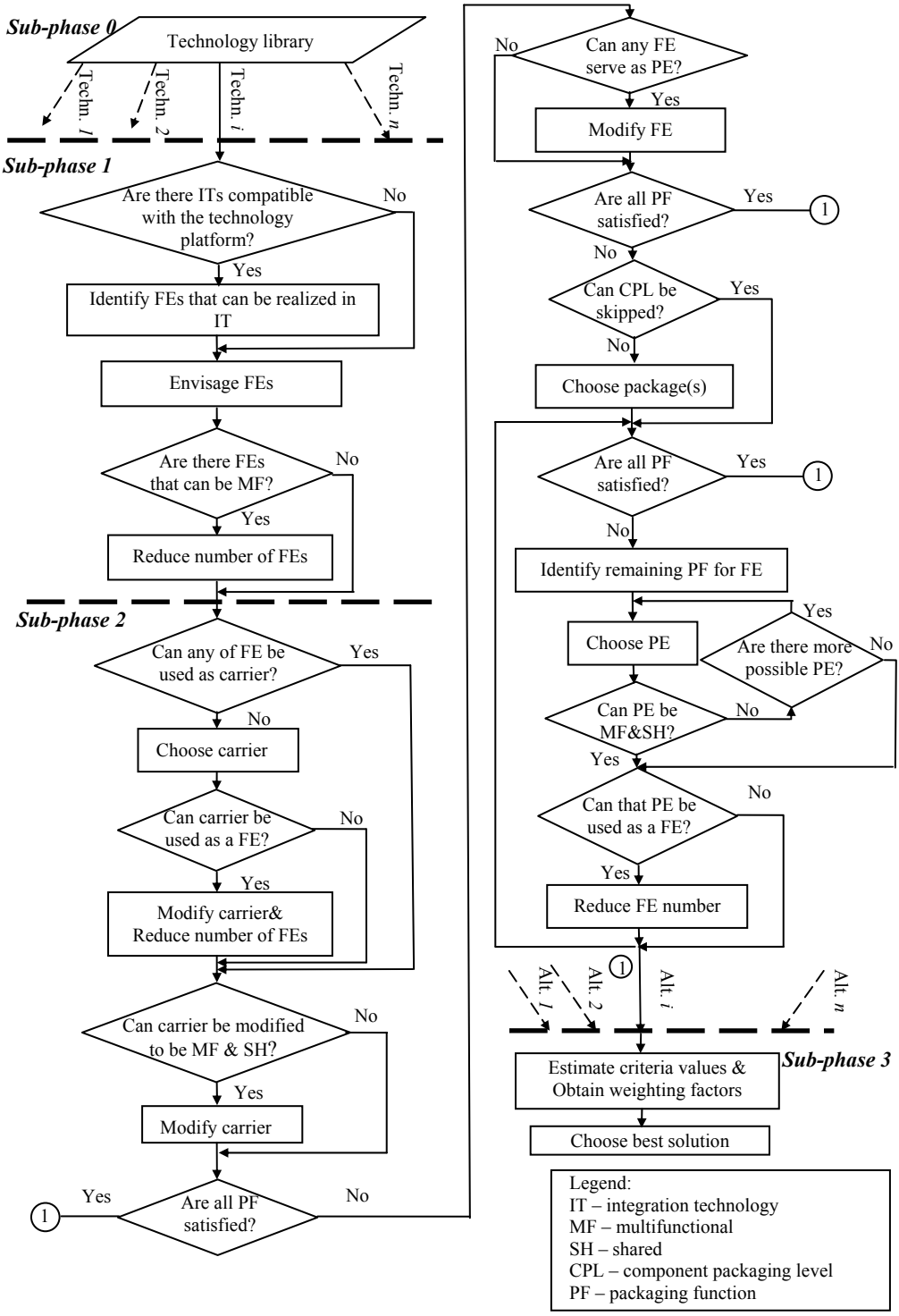


Figure 7-2 Design-of-parts algorithm

Once the FEs implementation is envisaged, the next step is to check if there are FEs that can be modified to implement the functions of two or more FEs, i.e. to be multifunctional. This is again done on the basis of the requirements from the design-of-functions phase and the material properties of the FEs. If there are elements that can be modified to be multifunctional, then the initial set of FEs is reduced.

Each processing block of the algorithm consists of both creative and analysis aspects. The creative aspect involves envisaging the solution while the analysis aspect involves verification of the feasibility of the solution. This may include electrical, electromagnetic, thermal and spatial modelling. For example, for a magnetic FE, the creative part is envisaging the technology and spatial arrangement of the element while the analysis part is performed through FEM modelling or simplified design formulas for checking the feasibility and obtaining the dimensions of the element.

The outputs of this sub-phase are FEs specified by technologies and initial spatial design.

Sub-phase 2: Packaging elements integration

This sub-phase deals with the realization of the packaging elements. The inputs (or FRs) to this phase are:

- Outputs of design-of-functions phase;
- Outputs of functional elements integration sub-phase (FEs design);
- Input design constraints.

The first few steps in this sub-phase deal with the carrier for the circuit. The term “carrier” is very broad and generally represents a PE (or several PEs) that a group of FEs is mechanically attached to. The carrier is mostly determined by the chosen technology platform. In some cases, an FE can act as a carrier for the other FEs. Although the carrier is normally associated with mechanical support and electrical interconnections, its functionality can be enhanced to perform more functions. Some carriers or parts thereof can perform some fundamental functions thus replacing one or more FEs from the initial set of FEs. A typical example would be using PCB copper metallization to implement the windings of a magnetic FE. Therefore, the next step in the algorithm is to explore the possibilities of enhancing the functionality of the carrier to replace one or more FEs. If it is possible, the initial set of FEs is reduced. If the carrier is already defined by the technology platform, this step can be performed even earlier, in the FE integration sub-phase.

Furthermore, in some cases, the functionality of the carrier can be increased by using it for other packaging functions. For example, some carriers allow for mounting bare FEs onto it, hence no extra PEs are needed for electrical interconnection and mechanical support. In that case, only one additional step, such as encapsulation, might be required for protection of the bare FEs.

The next step is to check if all the packaging functions are fulfilled – i.e. if the concept satisfies the FRs of this phase. Some packaging functions are specified in the outputs of the design-of-

functions phase – electrical interconnections and insulation are specified in the electrical circuit schematic and thermal interconnection elements are specified in thermal circuit schematic. The mechanical packaging functions, protection and support come from the initial mechanical constraints. This conditional step is performed after adding every PE.

If not, it is checked if any of FE can be modified to perform some packaging functions.

If all the packaging functions are not satisfied yet, the next step is to check if the component packaging level can be skipped, i.e. if bare FEs can be used. This depends on the type of the carrier, technology platform and initial constraints. If it cannot be skipped, the type of FEs packaging is chosen (surface-mount, through-hole etc.).

If the packaging functions are not yet satisfied, additional PEs are to be chosen. They are first envisaged and then it is investigated whether some of them can be multifunctional and/or shared among several FEs. If the answer is positive, the initial set of PEs can be reduced.

In some cases, PEs can perform fundamental functions, i.e. they can be used as FEs. The set of PEs is checked for this possibility. If the answer is positive then the set of FEs is reduced.

As with the FEs integration sub-phase, each block in this sub-phase consists of both creative and analysis aspects. The creative aspect of this phase involves envisaging PEs implementation and a possible 3D spatial layout of parts. By employing spatial design of the converter as a whole, i.e. including FEs and PEs together, less material can be used, and the unused volume (usually occupied by air) can be reduced, which will lead to higher power densities. The analysis aspect may contain modelling in 3D mechanical design software, thermal modelling and electromagnetic modelling (for EMI behaviour).

The outputs of this sub-phase are the PEs and converter's spatial layout.

Sub-phase 3: Choosing the best option

The inputs to this sub-phase are the design outputs from the previous phase, of all *n* technology alternatives. As described in Chapter 4, the criteria values for all the alternatives are calculated and weighting factors obtained from the decision-maker's preferences. This will give the values of the construction technology value function for each alternative. The alternatives can then be compared and the best alternative chosen. It is important to analyze the sensitivity of the result on variations in the criteria values and weighting factors since for some criteria the manufactured product will most likely have different values from the concept.

It is important to note that this design algorithm not only uses the available technologies but can also indicate the need for new technologies, processes or materials throughout the algorithm steps. For example, for enhancing the functionality of a FE or PE, a new process or material might be needed. Also, for the specific spatial layout, the need for new interconnection technologies might arise.

7.4 Case study: Dc-Dc converter for automotive applications

In this section, the presented design algorithm will be implemented in a concrete example. A dc-dc converter for automotive dual 14 V/ 42 V power net has been chosen as a case study. The automotive market is highly cost-driven, and this sets limits on technologies that can be used. Therefore, high performance, high cost technologies are to be avoided. On the other hand, the power electronics is to be used in the engine compartment, which poses stringent temperature and volumetric constraints. It is desirable that the engine cooling system is used for cooling the power electronics, which implies high operating temperatures (nominal temperature is 85 °C, maximum temperature can go as high as 120 °C). Furthermore, the volume available for the power electronics is rather limited, hence high power densities are a necessity.

The contradictory requirements of the automotive environment make this application a suitable case study, since all the phases of the design algorithm have to come together in order for an optimal solution to be devised. This starts from the technology platform selection for cost-effectiveness, and includes functional and packaging elements integration sub-phases, which are important for reducing the number of parts and achieving high power densities.

7.4.1. Design of functions

The inputs to the design-of-functions phase are the converter's electrical specifications and constraints imposed by the environment.

The electrical specifications of the converter are as follows:

- Input voltage 30 V< V_{42} < 48 V;
- Output voltage V_{14} = 14 V, output voltage ripple ΔV_{14} (peak-to-peak) is 2% of the nominal voltage value;
- Output current I_{out} = 10 A.

The environmental constraints are:

- Nominal heat sink temperature T_{nom} = 85 °C;
- Electrical insulation from the heat sink required.

Figure 7-3 shows the chosen electrical circuit topology. The buck topology is selected because of the low number of circuit symbols and its robustness. The synchronous rectification technique is utilized in order to reduce the conduction losses of the rectifier. A synchronous buck controller (TPS40051) with integrated gate drives for both high and low side MOSFETs is selected for the converter control. The values of some passive control circuit symbols necessary for the controller's functioning are determined by the data sheet specifications of the controller, while the other symbols (compensation passives, resistor for switching frequency setting etc.) depend on the values of the output filter's inductance, capacitance and the duty ratio of the switches.

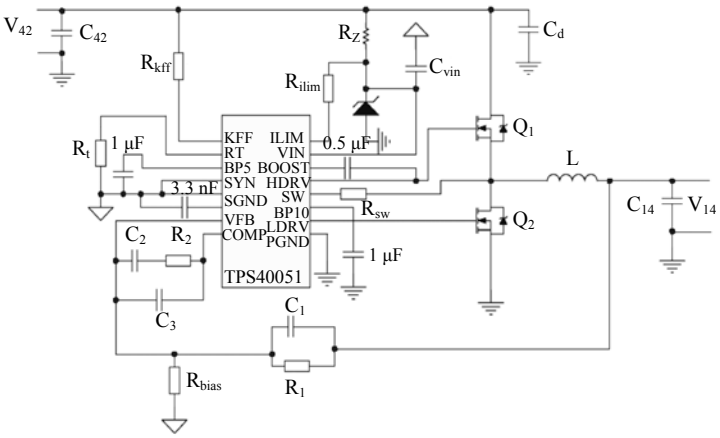


Figure 7-3 Electrical circuit schematic

The relationships between the values of the inductance L, capacitance C_{14} and C_{42} and the switching frequency, input and output voltage ripple and current are derived from the electrical circuit design and are given by the following expressions [Eri97]:

$$L = \frac{V_{14} \cdot (1 - D_{14})}{f_s \cdot \Delta I_{out}} \tag{7.1}$$

$$C_{14} = \frac{\Delta I_{out}}{8 \cdot f_s \cdot \Delta V_{14}} \tag{7.2}$$

$$C_{42} = \frac{I_{42\max} \cdot D_{42\max}}{f_s \cdot \Delta V_{42}} \tag{7.3}$$

In the next phase, design-of-parts, these relationships will be used to couple the characteristics of technologies to the electrical circuit design.

Based on the circuit's switching waveforms and characteristics of the power MOSFETs, the model for the losses in the power MOSFETs (P_{Q1} and P_{Q2}) is developed (Appendix B). A thermal circuit such as that shown in Figure 7-4 is used to determine maximum thermal resistances from the MOSFETs' and controller's junctions to the heat sink, given the maximum allowed operating temperature of the MOSFETs (Tj_{max}) and controller (Tj_{contr_max}) and the heat sink's operating temperature (T_{hs}). This will be used as one of the inputs to the design-of-parts phase, in order to ensure that the thermal resistances of the physical heat paths do not exceed these values.

Such an analysis has to be performed for the other FEs in the converter, such as the inductor and capacitors, but this will be done in the next phase when the physical implementations of their circuit symbols are known.

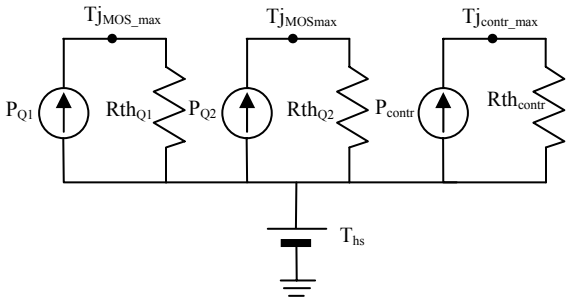


Figure 7-4 Thermal circuit schematic

The detailed electromagnetic design is beyond the scope of the thesis and will not be performed here. However, some considerations regarding the electromagnetic issues in different construction technology alternatives will be discussed in the section that deals with the design-of-parts phase since these issues are largely dependent on the physical implementation, as discussed in Chapter 3.

7.4.2. Technology platforms selection

In Chapter 5, two types of modular approach were distinguished. The first approach partitions the circuit into groups according to characteristics of the circuit symbols and implements each partition in the most suitable technology. The second approach is where the circuit is partitioned into a number of circuits with the same topology but lower power level. These circuits are implemented in a low cost technology and used as building blocks for achieving the desired power level. As already discussed, the automotive market is highly cost-driven, hence the low cost technology platforms are the preferred choice for this application. Therefore, the second modular approach will be employed. This explains the chosen low value of the output current in the converter's input specifications while the required power that needs to be processed is considerably higher [Kas01].

Three technology platforms will be considered: organic-based PCB technology, ceramic-based technology and metal-based lead frame technology. These technologies were discussed in Chapter 6 and their main characteristics will be repeated here.

PCB technology platform

Printed circuit board (PCB) technology has been used in electronics for decades, as a circuit carrier, providing electrical interconnection and mechanical support for electronic components. It is a mature and cost-effective technology.

As discussed in Chapter 6, PCB technology is normally used with packaged through-hole or surface-mount components. The copper metallization thickness ranges from 18 μm for low power circuits to 150 μm for large currents. Laminates of various thicknesses can be used, depending on the required mechanical strength, size of the components etc.

Ceramic technology platform

Ceramic substrate technology is widely used in electronics for implementing carriers of hybrid circuits, power modules etc. Its thermal conductivity is higher than that of organic-based substrates making them suitable for an effective thermal management of high heat density dissipating devices.

Different metallization techniques make ceramic technology suitable for versatile applications. Multilayer thick film metallization of ceramic substrates offers the possibility of implementing the whole circuit, including not only the power components but also the control circuit, on a single substrate. Possible metallization thicknesses of ~70 μm make it suitable for this current level. Ceramic substrates are generally used with surface-mount components or bare semiconductor dies. Small passive components such as resistors, capacitors and inductors can be implemented on a thick film metallized substrate in an integrated process.

Lead frame technology platform

Lead frame technology is extensively used in electronics, for electrical interconnection of the semiconductor dies terminals to the outside world in semiconductor packages. It is also used in low power range power modules as a cheaper alternative to ceramic substrates.

As discussed in Chapter 5, lead frame is normally manufactured by stamping or etching and can be produced in a wide range of thicknesses. A lead frame with sufficient thickness can perform the function of a carrier for the circuit. Power semiconductors in the surface mount or bare die form can be soldered directly onto the lead frame.

7.4.3. Design of parts

Ceramic technology-based building block

Sub-phase 1 – Functional elements integration: According to the algorithm in Figure 7-2, the first step is to check if there are integration technologies compatible with this technology platform. This depends on the type of ceramic metallization used. In this case, for the specified power level, thick film metallization is suitable. As described in Chapter 5, this technology platform allows for integrating capacitive and resistive FEs in an integration process. The capacitance values that can be integrated are < 1000 pF. Thick film screen-printed resistor technology offers tolerances to < 0.5 % in ranges from milliohms to megaohms. The values for some control passive components are determined by the data sheet of the chip itself, while the others depend on the switching frequency and values of the filter components and as such will be specified at the later stage. Furthermore, the inductor winding of the inductance circuit symbol can be realized in the substrate metallization.

The next step is to envisage the physical implementation of the remaining circuit symbols in the form of FEs. The power switches will be realized in the form of power MOSFETs, as already specified in the design-of-functions phase. The control chip TPS40051 contains the

integrated controller and gate drives. The magnetic core is realized in the form of a low profile planar ferrite core.

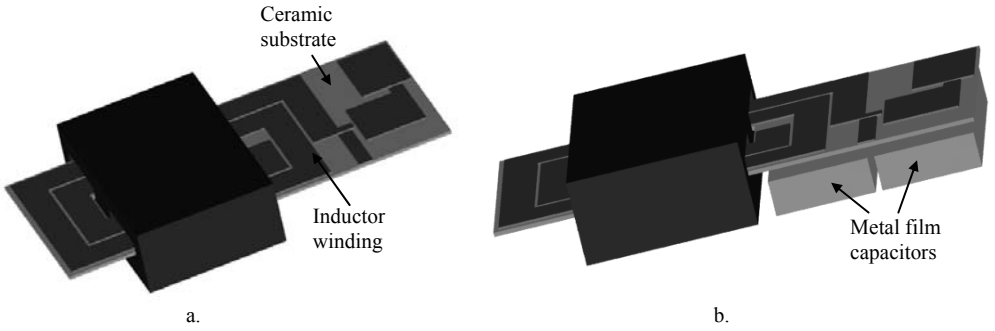


Figure 7-5 Physical implementation of FEs a. inductor b. capacitors

According to (7.3), the switching frequency would have to be larger than 10 MHz in order to implement C_{42} in this technology. Similarly, according to (7.1) and (7.2) either the switching frequency in tens of megahertz or a very large inductance would be required to implement C_{14} in this technology. This implies that the input and output capacitors will be implemented as separate FEs.

A possible implementation of the converter's FEs is shown in Figure 7-5. The space underneath the ceramic can be used to implement the capacitive FEs C_{14} and C_{42}. As discussed in Chapter 5, metal film capacitors can be manufactured in the rectangular shape, can achieve the necessary capacitance values and are able to handle the current ripple requirements.

Sub-phase 2 – Packaging elements integration: The first step is choosing the carrier, which is the ceramic substrate in this case. The thick film metallization of the carrier will be used for the electrical interconnections between the FEs. The ceramic substrate will also provide mechanical support. As indicated in the previous phase, the carrier can be structured to implement an FE, namely the inductor windings.

The next step is to check if all the packaging functions are fulfilled. The means to provide the electrical interconnections from the FEs to the ceramic metallization are not identified yet. No FEs can provide these functions. The next step is to check if the component packaging level can be skipped. If the control capacitors and resistors are implemented in the integrated thick film process, the MOSFETs and controller can be mounted in the bare die form and wire-bonded to the metallization pads. In this case, the MOSFETs and controller are not protected and would have to be encapsulated or the whole converter encased. An alternative is to use the control and switching FEs in surface-mount packages (Figure 7-6a), which would take care of the interconnections and protect the FEs. This alternative will be considered further. The capacitive FEs can be used in their bare form (such as Power Chip Capacitors (PCC) [Epc_b]). Their interconnections are provided by means of metal bus bars as shown in Figure 7-6a. These bus bars can be structured to provide the converter's input and output terminals. The bus bars are connected to the ceramic metallization by means of solder tabs.

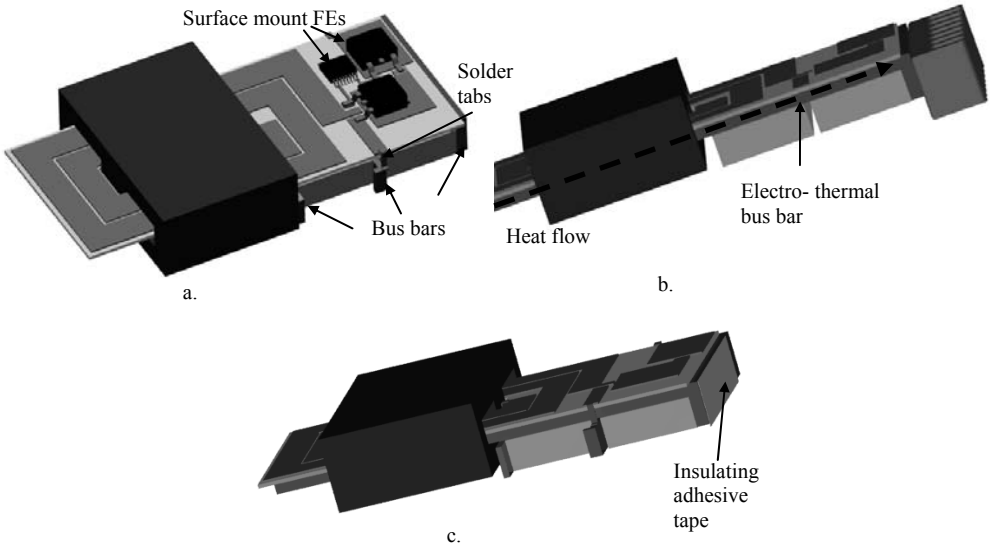


Figure 7-6 Physical implementation of PEs a. surface mount packages b. heat conductor bus bar c. electrically insulating thermally conducting adhesive tape

The thermal conduction function is not fulfilled yet, i.e. it is not specified how the heat is transferred from the dissipating FEs to the heat sink. A metal bus bar can be used on the bottom side of the ceramic to take the heat from all the FEs to the heat sink, as shown in Figure 7-6b. Since this bus bar is made of metal, such as copper, it can be used as one turn of the inductor winding. It can also be used as an electrical interconnection for the C_{14} capacitor and the output terminal. This bus bar needs to be mechanically attached to the ceramic, which can be done by means of thermally conductive glue. On the other side, the bus bar has to be mounted onto the heat sink, which can be implemented with a thermally conductive double sided adhesive tape (Figure 7-6c). This tape can also be electrically insulating, which provides electrical insulation between the heat sink and the converter.

Now that the physical implementation of the FEs and PEs is envisaged, it is necessary to perform the analysis part of this sub-phase in order to finalize the design. In order to achieve a high power density, it is desirable to reduce the volume of the FEs and the assembly in total. Reduction of passive FEs volume by means of increasing switching frequency is well known. However, the switching losses in the MOSFETs will increase proportionally with the frequency increase. For a fixed thermal management structure, this results in higher operating temperatures of the FEs. Furthermore, the FEs have to fulfil the electrical requirements from the design-of-functions phase. In order to achieve a high power density while keeping all the FEs in their operating range, an integral electrical, thermal and spatial design procedure is employed.

Firstly, an inductor parameter, namely the core size (only commercially available planar E-I combinations are considered), is selected. The width of the converter is primarily determined by the core size. The initial value of the current density in the part of the inductor winding

implemented in the ceramic metallization is chosen. This, together with the winding window size, determines the number of turns in the part of the winding that is implemented in the ceramic metallization (as described earlier in the text the total number of turns is this number plus one turn that comes from the electro-thermal bus bar). The switching frequency is chosen on the basis of the design criteria of energy requirement in the inductor [Moh01]. The heat conductor geometry is then derived and the losses in the converter calculated (Appendix B).

Finally, the FEM thermal simulation is performed on that geometry in order to obtain the temperature distribution in the converter. It is assumed that the heat sink temperature is T_{hs}= 85°C and that the conduction is the only heat transfer mechanism. This is justified by the concept of using a number of these modules tightly packaged together, which allows us to neglect the convection and radiation heat removal mechanisms. The simulation results show whether all the FEs operate in the allowed temperature range. If their temperature is too high, the next larger core is chosen which leads to the reduction in switching frequency and lower losses in the MOSFETs. On the other hand, the result might be that the FEs operate far below their temperature ratings, i.e. the converter is "over-designed". In that case, the next smaller core is chosen. Table 7-1 shows the results of this procedure.

Table 7-1 Electrical and thermal design procedure

Core size	**ELP 38/8/25**	**ELP 32/6/20**	**ELP 22/6/16**
f_s **[kHz]**	150	300	450
ΔI_{out} **[A]**	3.5	4	6
L **[µH]**	17.8	7.8	3.5
P_{Q1} **[W]**	5.36	10.35	14.41
P_{Q2} **[W]**	1.86	3.07	3.44
Tj_{Q1} **[°C]**	101.7	127.2	145.6
Tj_{Q2} **[°C]**	96.2	108.9	128.8
Power density [W/in^3]	56.6	75.6	110.1

The planar E-I 32/6/20 core is chosen due to the acceptable temperatures of the MOSFETs and the high power density. Figure 7-7 shows the simulated temperature profile of the whole assembly. Furthermore, the thickness of the electro-thermal bus bar can be varied according to the available space in the winding window of the core. As this is the main heat path from the MOSFETs to the heat sink, increasing the thickness of the bus bar will mean that its thermal resistance will decrease. The results shown in Table 7-1 are obtained for t_{busbar} = 2 mm. For t_{busbar} = 1 mm and the same core, the junction temperature of the high side MOSFET is Tj_{Q1} = 132.1 °C. However, the thickness of the bus bar is limited by the height of the winding window of the core half.

For the design value of inductance and ripple current, for fulfilling the output voltage ripple value requirement given by the input specifications, the capacitance value is determined according to the following expression:

$$\Delta V_{out} = \sqrt{(\frac{\Delta I_{out}}{8 \cdot f_s \cdot C_{14}})^2 + (\Delta I_{out} \cdot ESR(C_{14}))^2} \tag{7.4}$$

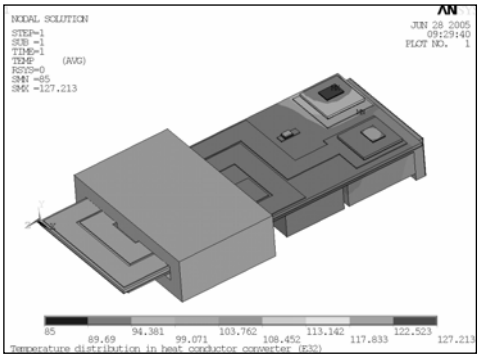


Figure 7-7 Integral converter design – simulated temperature profile

According to this expression, the value of at least 20 μF is needed to satisfy the output voltage ripple requirement. According to the volumetric capacitance density of PCC capacitors [Epc_b], this value can be implemented in a PCC capacitor with the dimensions 30 mm X 15 mm X 5 mm. These dimensions suit the concept from Figure 7-5 since the ELP 32/6/20 core width is 31.7 mm and the ceramic length outside the core of approximately 30 mm is needed for the MOSFETs and control circuit.

Let us consider some electromagnetic issues in this building block. Since the magnetic field shaper of the inductor is made of a high permeability ferrite, the level of field coupling between the inductor and the rest of the circuit is expected to be fairly low. Concerning the EMI behaviour, the interwinding capacitance of the inductor between the winding turns implemented in the copper metallization and the turn implemented in the bus bar combined with the large *dv/dt* will be a source of the differential mode noise. Furthermore, due to the bus bar interconnections arrangement, the parasitic inductance of the loop that carries the switching current (Q_1, Q_2 and C_{42}) is expected to be rather large, which, combined with the large *di/dt*, is another source of the differential mode noise. The switching waveforms of the MOSFETs will be affected by the high frequency noise, which will result in a change in the MOSFET losses, which in turn will influence the MOSFETs' thermal behaviour.

With the analysis part performed, the feasibility of the concept is confirmed and the design parameters for the FEs and PEs determined. The salient features of this concept are:

- Multifunctional bus bar – thermal, electrical and mechanical function;
- Shared thermal management for both power semiconductors and passive components;
- Both power and signal circuitry assembled on a single ceramic substrate;
- Inductor winding implemented in the substrate conductor pattern;
- Capacitors bus bars are used as power terminals.

PCB technology-based building block

Sub-phase 1 – Functional elements integration: This sub-phase starts with an investigation of the possible integration technologies compatible with this technology platform. In Chapter 6, PCB-embedded passives technology was discussed. Passive FEs are implemented by means of layers of capacitive and magnetic material that are laminated with conventional PCB materials in an integral manufacturing process. This brings a number of benefits, including low profile assemblies, better performance, fewer manufacturing processes etc. Looking at the circuit schematic from Figure 7-3, circuit symbols that are potential candidates to be realized in this technology are input filter capacitor C_{14}, output filter inductor L and output filter capacitor C_{14} and the control circuit's capacitors. For the capacitors, capacitive laminates will be used to implement the dielectric while the copper metallization of these layers will provide capacitive electrodes. For the inductor, magnetic laminates will be used for magnetic field shaping while copper metallization will be utilized to implement the windings. The next step is to check if there are FEs that can perform more functions. Copper metallization used for the capacitor electrodes can be used to implement the inductor windings as well, provided it is structured in the correct pattern.

This is followed by the analysis step, in order to ensure that the envisaged solution is feasible, taking into account the technology characteristics and the outputs of the design-of-functions phase. Let us start with considerations about integration of capacitors. As shown in Chapter 6, there are two types of capacitive materials available at present. The first type is FR4-like laminates enhanced with the dielectric powder. These materials are compatible with the standard PCB multilayer manufacturing process. Typical capacitances of these materials are in the 0.2 nF/cm^2 - 0.5 nF/cm^2 range. The second type is based on resin-coated copper foils that are laminated together. The dielectric layers of these materials are very thin, and this results in higher capacitance values. However, they require more expensive, sequential build-up processing.

The converter circuit schematic contains 11 capacitors (including the input filter capacitor) of which only three capacitors have capacitance values lower than 20 nF (the required PCB area for capacitors above 20 nF is > 40 cm^2) and can be considered feasible for integrating into the PCB.

As regards magnetic laminates, two types of materials are considered. Soft magnetic metal sheets (NiFe for e.g.) are one option. They have very high permeability (μ_r > 1000) but are electrically conducting, which results in very high core losses. For this reason, thin cores must be used thus reducing the flux density capability. The second option is polymer-like laminates filled with the ferrite powder, such as MagLam by Isola [Iso] or Ferrite Polymer Composite (FPC) materials by EPCOS [Epc_a]. The permeability of these materials is rather low (μ_r < 20).

Let us analyze if integration of the output LC filter is feasible in this case. Taking into account the given capacitance values of the capacitive laminates (0.2 nF/cm^2 - 0.5 nF/cm^2), for a PCB area of 50 cm^2 and assuming three capacitive layers, the capacitance value that can be obtained

will be approximately C_{14} = 35 nF. For this capacitance value and a peak-to-peak output voltage ripple of ΔV_{out} = 2 % of the nominal voltage value, the necessary inductance value is a function of the switching frequency according to the following expression, obtained by combining (7.1) and (7.2):

$$L = \frac{V_{14} \cdot (1 - D)}{8 \cdot f_s^{\,2} \cdot C_{14} \cdot \Delta V_{14}} \tag{7.5}$$

This relationship is plotted in Figure 7-8. It can be seen from the figure that either the switching frequency should be in the megahertz region or an inductance value of more than 0.2 mH is necessary for this capacitance value. Since this is a hard switching topology and the converter is operating in the continuous conduction mode, such high operating frequencies would result in very large losses in the MOSFETs. On the other hand, due to the limited relative permeability of magnetic laminates ($\mu_r < 20$), such large values of inductance cannot be realized in acceptable size.

From the discussion above is clear that, in this case, both the output capacitance and inductance cannot be integrated in the PCB at the same time. Either the output filter capacitance can be embedded into the PCB and the inductor realized in the discrete form, or the inductor can be integrated and the capacitor implemented as a separate component. If the capacitor is integrated, the inductance value for the switching frequency of f_s = 300 kHz (the frequency used in the ceramic technology building block) is 1.2 mH. The smallest commercially available magnetic core that this inductance value can be realized with, for the output current of 10 A and assumed current density of 6 A/mm^2, is E65/32/27 with the volume of 78.6 cm^3 (Appendix B). If the inductor is integrated, according to the FEM analysis the inductance value that can be achieved is in the region of 5 μH, the output capacitance needed is > 30 μF (according to the expression (7.4)), which for the output capacitor can be realized in a much smaller volume – e.g. a commercially available metal film capacitor of this capacitance and voltage rating has the volume of 7.6 cm^3. Therefore, it is volumetrically more feasible to implement the inductance rather than capacitance circuit symbol in this integration technology. Figure 7-9a shows the conceptual implementation of the inductor.

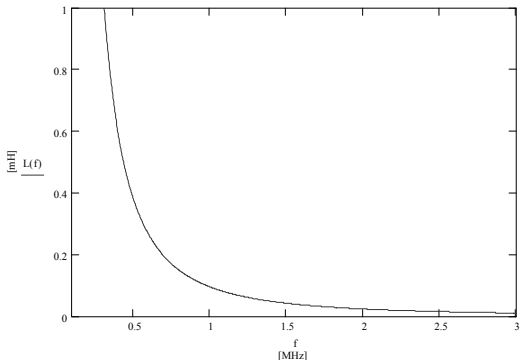


Figure 7-8 Inductance vs. switching frequency of integrated LC filter

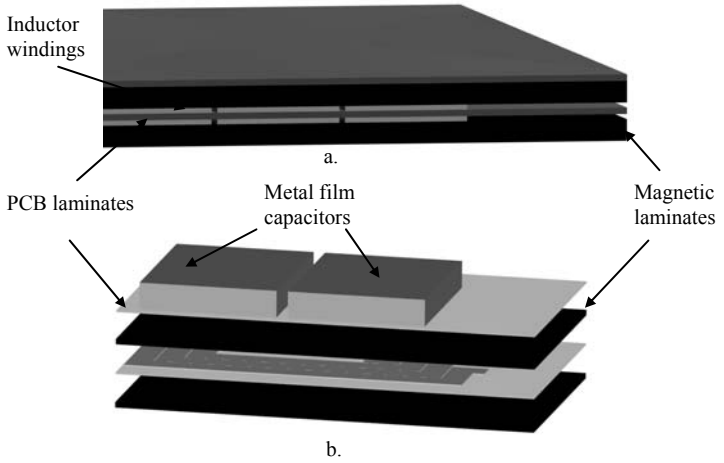


Figure 7-9 Physical implementation of FEs a. PCB embedded inductor b. low profile capacitors above inductor

The next step is to envisage the implementation of the rest of the circuit symbols in the form of FEs. The remaining circuit symbols are the power switches Q_1 and Q_2, control chip, capacitors C_{14}, C_{42} and the control circuit capacitors, the values of which are not suitable for integration and resistors from the control circuit.

As in the ceramic technology building block, the power switches will be realized in the form of power MOSFETs. The same controller chip TPS40051 will be used. These FEs and control circuit passive FEs will be implemented as separate FEs, in the surface-mount or through-hole form.

Since the way the inductor is implemented implies a large surface area, capacitors with low profile that will be mounted on the PCB above the inductor are desired. This combined with the capacitance and current ripple handling requirements brings us to an option of using metal film capacitors that fulfil these electrical requirements from the design-of-phase outputs and can be manufactured in the desired profile (such as PCC capacitors). Figure 7-9b shows the conceptual implementation of the capacitors and inductor FEs.

The next step is to analyze the feasibility of this concept. This implies investigating whether it is possible to implement the L, C_{14} and C_{42} as proposed so that they suit the requirements from the design-of-functions given by the expressions (7.1), (7.2) and (7.3). The switching frequency is kept the same as for the ceramic technology building block, f_s = 300 kHz.

Since magnetic laminates are generally lossy materials and are embedded into the PCB, the thermal behaviour has to be included in the inductor design. An iterative, integral electrical-thermal inductor design procedure is shown in Figure 7-10. The procedure inputs are the magnetic material characteristics (permeability and relative loss factor), minimum desired inductance value and the circuit geometry, which is mostly determined by the dimensions of PCC capacitors as shown in Figure 7-9. Then, the thickness of the magnetic material and

number of turns are chosen. The inductance value of the structure is then obtained by the electromagnetic FEM simulation. If the inductance value of the structure is lower than the input value, the number of turns and/or material thickness is increased. Afterwards, the losses in the inductor, both winding losses (dc and high frequency losses) and losses in the magnetic material ("core"), are calculated. The high frequency winding losses are obtained by means of FEM simulation, while the core losses are obtained from the data sheet value of relative loss factor ($\tan\delta$ / μ_i) for the given excitation (Appendix B). In this case, the parameters of the FPC C303 material (μ_r = 24 ± 20 %) [Epc_a] are used for design.

These values are the inputs to the thermal FEM simulation in order to obtain the temperature profile of the inductor. If the temperature of the magnetic material and the PCB layer that carries the winding is higher then the maximum allowed operating temperature of these materials, a new set of values for the material thickness and/or number of turns is chosen and the procedure is repeated.

Table 7-2 shows the results of the procedure. The minimum inductance value is chosen to be L_{min} = 3 μH, which at switching frequency f_s = 300 kHz corresponds to the peak-to-peak value of the inductor current ripple ΔI_{out} = 10 A. Larger values of the current ripple would increase losses in the input and output capacitors. The thickness of the magnetic material is selected to be 1 mm for all cases. The widths of the tracks are obtained from the spatial constraint of the PCC capacitor length, which is chosen to be 50 mm. For this value of inductance, according to the expression (7.4), the capacitance value of 35 μF is needed. This value can be achieved in the PCC capacitor with dimensions 15 mm X 50 mm X 5 mm, which geometrically suits the concept presented in Figure 7-9.

Table 7-2 Design procedure results

N_{turns}		5	6	7	6
N_{layers}		1	1	1	2
L [μH]		2.05	2.84	3.49	4.45
P_{ind} [W]	P_{dc}			7.58	4.1
	P_{ac}			0.49	0.27
	P_{core}			0.84	0.71
T [°C]				111.65	102.13

According to Table 7-2, the optimal design values are: six turns arranged in two layers, three turns per layer. Figure 7-10b shows the simulated temperature profile of the inductor for the chosen design values. It can be seen from the figure that all the materials are within their allowed temperature range.

Sub-phase 2 - Packaging elements integration phase: The selection of the carrier in this technology is straightforward since printed circuit boards are normally used as circuit carriers. It has already been established in the previous phase that magnetic laminates can be used to shape the magnetic field, capacitive laminates as capacitance dielectric and that copper tracks can be used as inductance windings and capacitive electrodes.

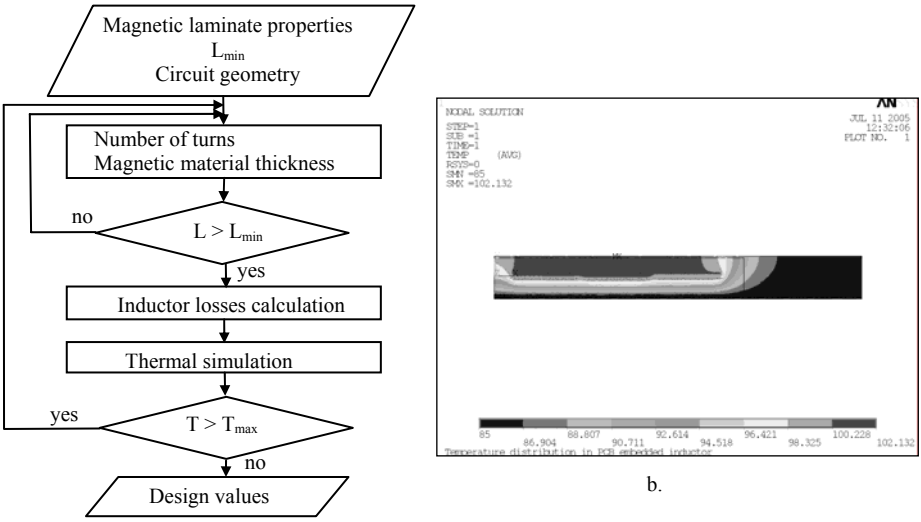


Figure 7-10 Inductor design a. design procedure b. temperature profile

Considering multifunctionality of the PCB, its electroplated vias, originally intended for electrical interconnections in multilayer PCBs, can be used to conduct the heat from the dissipating FEs through the PCB to the heat sink. Furthermore, copper pads that the FEs are mounted on can be structured to spread the heat produced by the FEs over a larger surface area, thus reducing the thermal resistance of the heat path through the PCB.

The next step is to check if all the packaging functions are satisfied. The means of attaching FEs to the PCB and electrical interconnections from the FEs terminals to the PCB are not yet identified. In the selected set of FEs, there are no FEs that can perform any packaging function. The electrical interconnection from the FEs terminals to the PCB could be done either by a common process that interconnects all the FEs at the same time or by using separate PEs on the component packaging level, which is more compatible with the PCB carrier due to its mechanical properties. In order to keep the bottom surface of the PCB flat so that it can be mounted onto the heat sink, the power MOSFETs, control integrated circuit and control passive components will be implemented in surface-mount technology and attached to the PCB by means of a reflow soldering process. The metal film capacitors will be used in their bare form (PCC capacitors) and soldered onto the PCB.

Again, it is checked if all the packaging functions are satisfied. The means of insulation between the converter and the heat sink and the electrical connections to the outside are not identified yet. A double-sided adhesive tape can be used to mechanically attach the converter onto the heat sink. Furthermore, this PE can also perform the electrical insulation function, between the converter and the heat sink. The electrical interconnections with the outside can be implemented by means of surface-mount connectors.

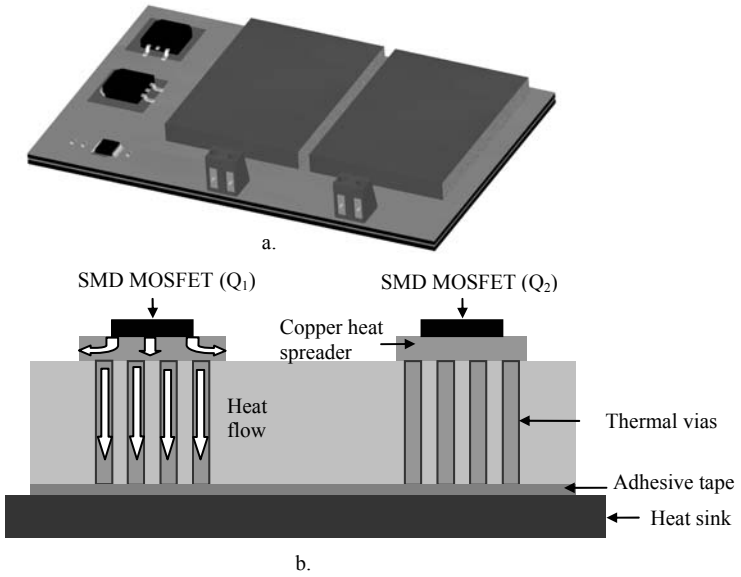


Figure 7-11 Physical implementation of converter a. whole assembly b. cross-section

Figure 7-11a and Figure 7-11b show the whole converter assembly and the vertical cross-section.

It is necessary to analyze if this thermal management concept fulfils the outputs of the design-of-functions phase, more specifically the maximum thermal resistance of the heat path from the MOSFETs to the heat sink. The thermal resistance of the heat path from the MOSFETs case to the heat sink Rth_{c_hs}, is calculated according to the expression:

$$Rth_{c-hs} = \frac{1}{k_{Cu}} \cdot \frac{t_{PCB}}{A_{via}} \cdot \frac{1}{N_{via}} + \frac{1}{k_{ins}} \cdot \frac{t_{ins}}{A_{pad}} \tag{7.6}$$

where t_{PCB} is the thickness of the PCB, A_{via} is the surface area of one via, A_{pad} the surface area of the MOSFET's drain pad and k_{ins} and t_{ins} are the thermal conductivity and thickness of the insulation layer.

The junction temperatures of the MOSFETs are calculated according to the following formula:

$$Tj_{Qi} = P_{Qi} \cdot Rth_{j\_a} + T_{hs} = P_{Qi} \cdot (Rth_{j\_c} + Rth_{c\_hs}) + T_{hs} \tag{7.7}$$

where P_{Qi} is the heat dissipation of the MOSFET i, Rth_{j_c} junction-to-case thermal resistance as specified in the data sheet and T_{hs} is the temperature of the heat sink. The obtained values for the MOSFETs junction temperatures are Tj_{Q1} = 132.5 °C and Tj_{Q2} = 103.4 °C. This is considerably lower the maximum operating junction temperature of these devices specified in the devices' data sheets (Tj_{max} = 175 °C).

Thermal vias are also used to conduct the heat dissipated by the controller. The controller's package has an exposed copper pad at the bottom side that allows for the cooling on the bottom side. The power dissipation of the chip is 0.3 W. The equivalent thermal resistance of the heat path from the copper pad to the heat sink is Rth_{c_hs}= 30.6 °C/W. The junction temperature of the chip is calculated in the same way as for the MOSFETs. The obtained value is Tj_{IC}= 94.2 °C, which is again lower than the maximum operating junction temperature of this device (Tj_{max}= 125 °C).

Let us take a look at the electromagnetic issues in this building block. Due to the spatial arrangement of the capacitors being in close proximity to the inductor and the low permeability of the C303 material, a leakage magnetic field will induce eddy currents in the capacitors, which will result in the increased losses in the capacitors. As for the layout parasitics, in order to minimize the parasitic inductance of the loop that carries the high frequency switching current that causes the differential mode noise, C_{42} should be placed closer to the MOSFETs. On the other hand, for the control feedback signal it is desirable to place the C_{14} capacitor closer to the control circuit. Again, the high frequency switching noise will cause the losses in the MOSFETs to differ from those calculated using the model presented in Appendix B, which will influence the thermal behaviour of the MOSFETs. Possibly, a larger drain pad area would be needed to accommodate more thermal vias, which would increase the common mode capacitance between the switching node and ground.

With the analysis part performed, the feasibility of the concept is confirmed and the design parameters for the FEs and PEs determined. The main characteristics of this concept are:

- Multifunctional PCB – electrical interconnection, mechanical support, heat conduction, integrated magnetic FE;
- No extra parts for heat sinking due to an integrated thermal management into the PCB;
- Low profile.

Lead frame technology based building block

Sub-phase 1 - Functional elements integration: As in the previous two cases, this sub-phase starts with exploring possible integration technologies compatible with this technology. The inductor windings can be realized as part of the lead frame. There are no other integration technologies compatible with this technology platform.

Figure 7-12 shows the inductor implementation. It is necessary to analyze if this implementation is feasible, i.e. if the inductance value that can be obtained in this way satisfies the outputs of the design-of-functions phase given by the expressions (7.1), (7.2) and (7.3). The area inside the inductor can be used to place the MOSFETs and the control circuit. An area of 30 mm X 30 mm is assumed to be occupied by these FEs. This assumption will be substituted with final values in the next phase, when the PEs for these FEs have been identified. The switching frequency is the same as in the previous two cases, f_s = 300 kHz.

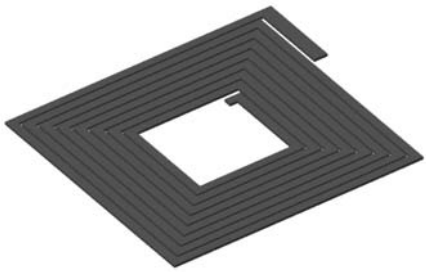


Figure 7-12 Lead frame air-core inductor

As in the previous two cases, the minimum inductance value is L_{min} = 3 μH. Let us analyze what size the air core inductor would have to be in order to achieve this inductance value. The inductance value can be enhanced by the use of sheets of composite ferrite to shape the magnetic field as shown in Figure 7-13. Table 7-3 shows the inductance values of a square air core inductor calculated by the methods presented in [Moh99][Gro62] (Appendix B) and an inductor with top and bottom layers of a composite material made of VITROPERM flakes and epoxy (μ_r = 20-35, B_s ~ 0.7 T) [Vac] obtained by FEM simulations. The option of N_{turns} = 7 gives the inductance value larger than the minimum value but the size of the inductor is rather large. By adding two sheets of the composite ferrite polymer material, the inductance value increases, and for N_{turns} = 6, the desired value is achieved (L = 4.65 μH). All these values are obtained for square inductors with the inner dimensions of 30 mm X 30 mm (d_{out_1} and d_{out_2} are the outer diameters of the inductor).

Table 7-3 Lead frame inductance values

	N_{turns}	L[μH]	d_{out_1} [mm] X d_{out_2} [mm]
Air core	5	1.73	52 X 52
	6	2.48	57 X 57
	7	3.38	62 X 62
Enhanced (sheets of composite Vitroperm)	5	3	52 X 52
	6	4.65	57 X 57

The next step is to envisage the FEs to implement the rest of the remaining circuit symbols. As in the previous cases, the power switches will be realized in the form of power MOSFETs. The control passive circuit symbols will be realized as discrete FEs, in the surface-mount or through-hole form. The capacitive symbols could be implemented in the form of PCC metal film capacitors as shown in Figure 7-13, to use the available space above the inductor.

According to the expression (7.4), the capacitance value needed for this inductance value is 33 μF. If the capacitance length is taken to be 57 mm (the same as the output diameter of the inductor) and the height 5 mm (the same as the height of the capacitor samples available at the time of the design), the width of a PCC capacitor needed to implement the value given above is 13.2 mm. Given that the inside diameter of the inductor is 30 mm, and the outside diameter 57 mm, the space available for one PCC is 13.5 mm. Therefore it can be concluded that this spatial concept satisfies the input requirements.

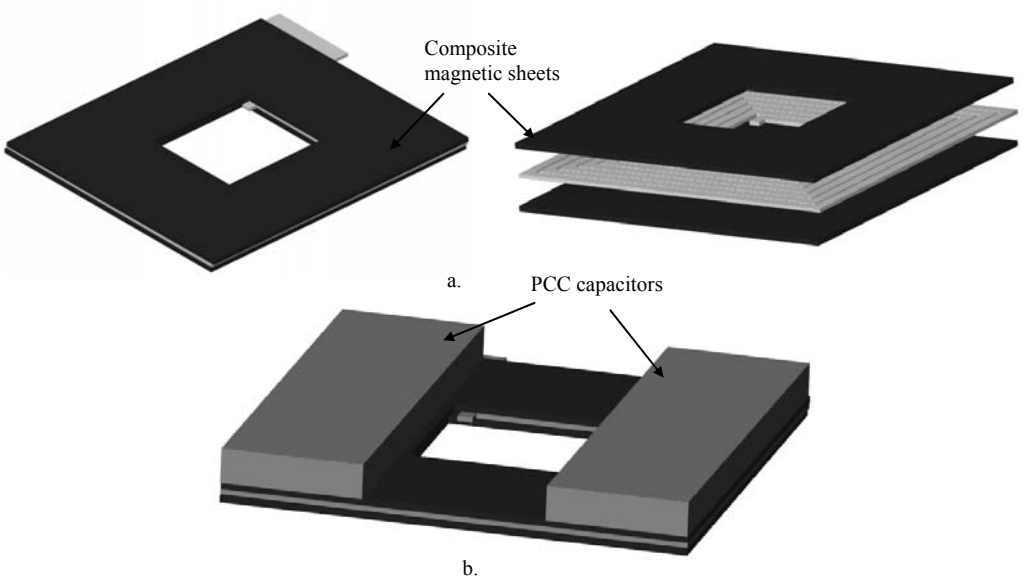


Figure 7-13 a. Lead frame air core inductor – enhanced with composite magnetic sheets b. PCC capacitors' spatial arrangement

Sub-phase 2 - Packaging elements integration: The carrier for the power circuit symbols and the controller is the lead frame itself. The carrier is multifunctional, i.e. it provides electrical interconnection, mechanical support for the FEs and can serve as a thermal conductive element. The lead frame can also implement the converter's electrical input and output terminals. For the control passive components, the carrier can be a PCB or a ceramic substrate.

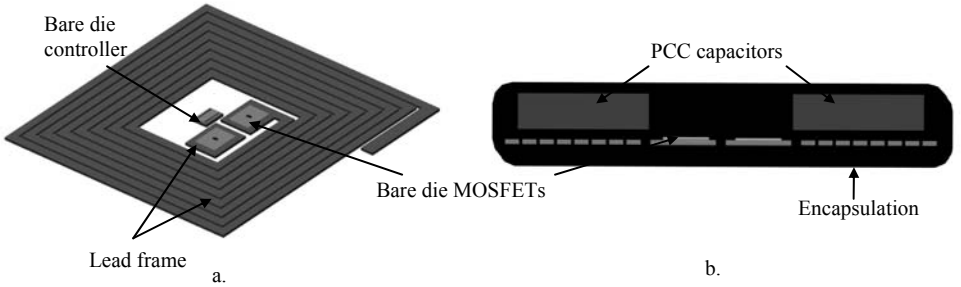


Figure 7-14 Lead frame assembly a. FEs b. encapsulation

The component packaging level for the MOSFETs and control chip can be skipped and they can be mounted in the bare die form onto the lead frame (Figure 7-14a). The next step is to check if all the packaging functions are satisfied. Electrical interconnections between the MOSFET and control chip terminals and the lead frame are not yet implemented. Wire bonds can be used to implement these interconnections. Furthermore, the MOSFETs are not protected and there is nothing to hold the loose pieces of the lead frame together. This can be provided by encapsulating the whole assembly. This part can serve as an FE, i.e. as part of the moulding process: a composite ferrite polymer is moulded around the inductor in order to enhance the

inductance, which can reduce the number of FEs (Figure 7-15a). The inductance value of an inductor with 6 turns and the same dimensions as in Table 7-3 moulded with the FPC C302 material (μ_r = 17 ± 20 %, B_s = 330 mT), 1 mm thickness on both sides of the inductor winding, obtained by FEM modelling is 5.44 µH.

Again, it is checked if all the packaging functions are satisfied. Figure 7-15b shows the cross-section of the converter up to this point. The thermal resistance of the MOSFETs' heat path is 12.9 W/°C. This results in the high side MOSFET's Q_2 junction temperature of 212.9 °C, which is above the maximum allowed operating temperature of the MOSFET. In order to reduce the thermal resistance of the heat path so that it satisfies the thermal conduction packaging function, an additional PE, a copper block is added. The MOSFETs' and control chip's lead frame pads are mounted on this block by means of a double-sided adhesive tape that also provides electrical insulation (Figure 7-15c). The bottom of this metal block is exposed after moulding for the direct contact with the heat sink.

Let us check if adding these PEs means that the requirements from the design-of-functions phase are fulfilled. The heat path from the MOSFETs to the heat sink is shown in Figure 7-16a. The thermal resistances of the heat paths are calculated as the sums of the thermal resistances of the layers and the resulting values are Rth_{j_c} = 4.1 °C/W for the MOSFETs and Rth_{j_c} = 18.7 °C/W for the controller chip. This gives the MOSFETs junction temperatures Tj_{Q1} = 125.3 °C and Tj_{Q2} = 97.5 °C at full power while the temperature of the controller chip is Tj_{IC} = 91.7 °C. These values are well below the maximum operating temperatures given in the FEs data sheets. Furthermore, the thermal behaviour of the inductor was analyzed by means of thermal FEM simulations and the result is presented in Figure 7-16b. It can be seen that the inductor materials operate within their allowed temperature range.

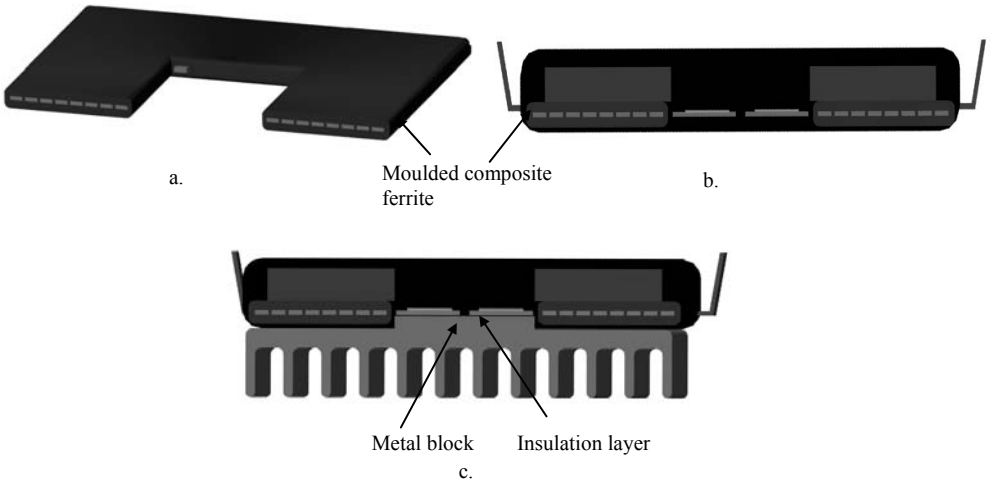


Figure 7-15 PEs implementation a. inductance enhancement as part of encapsulation process b. cross-section c. heat conduction path

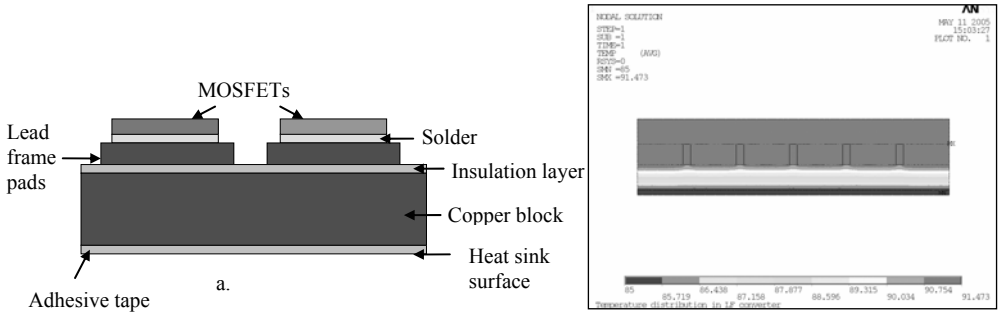


Figure 7-16 Thermal management structure a. MOSFETs and controller b. inductor

Let us take a look at the electromagnetic issues in this building block. As in the case of the PCB-embedded building block, due to the spatial arrangement of the capacitors being placed above the inductor and the low permeability of the composite VITROPERM-epoxy material, there will be a leakage magnetic field coupled with the capacitors. This field will induce eddy currents in the capacitors, which will result in the increased losses. Furthermore, the MOSFETs and the control circuit are positioned inside the lead frame. The inductor's magnetic field lines will pass through this area, which might influence the operation of these FEs. Concerning the EMI behaviour, the common mode capacitance between the drain pad and heat sink is expected to be considerably large since the insulation layer is very thin, which, combined with the large *dv/dt* of the switching node, will be a source of the common mode noise. Furthermore, due to the chosen interconnections arrangement, the parasitic inductance of the loop that carries the high frequency switching current is expected to be significant, contributing to the differential mode noise. Again, the high frequency noise in the switching waveforms will result in the deviations of the MOSFET losses from the calculated values and consequently altered thermal behaviour.

With the analysis part performed, the feasibility of the concept is confirmed and the design parameters for the FEs and PEs determined. The salient features of this concept are:

- Low number of parts;
- Multifunctional lead frame – thermal, electrical and mechanical function;
- Inductor winding implemented in the lead frame;
- Magnetic field shaper implemented as part of the encapsulation process
- Low profile

Sub-phase 3: Choosing the best option

In Chapter 6, the procedure for evaluating construction technology options and choosing the best option for the particular application was presented. This procedure will be used here to find the best among the three presented options.

Firstly, a hierarchy tree of objectives for this application is to be created. As described in Chapter 6, a hierarchy tree of objectives starts with the ultimate cost-effectiveness objective, which is branched down to the criteria that can be quantified. It is necessary that the values of

the final criteria for all the options are available at the time of decision-making. Based on this condition, an objective tree for this case is derived from the tree presented in Chapter 6. The tree is shown in Figure 7-17. There are eight final criteria that represent performance (electrical, thermal and spatial) and cost (assembly and manufacturing cost).

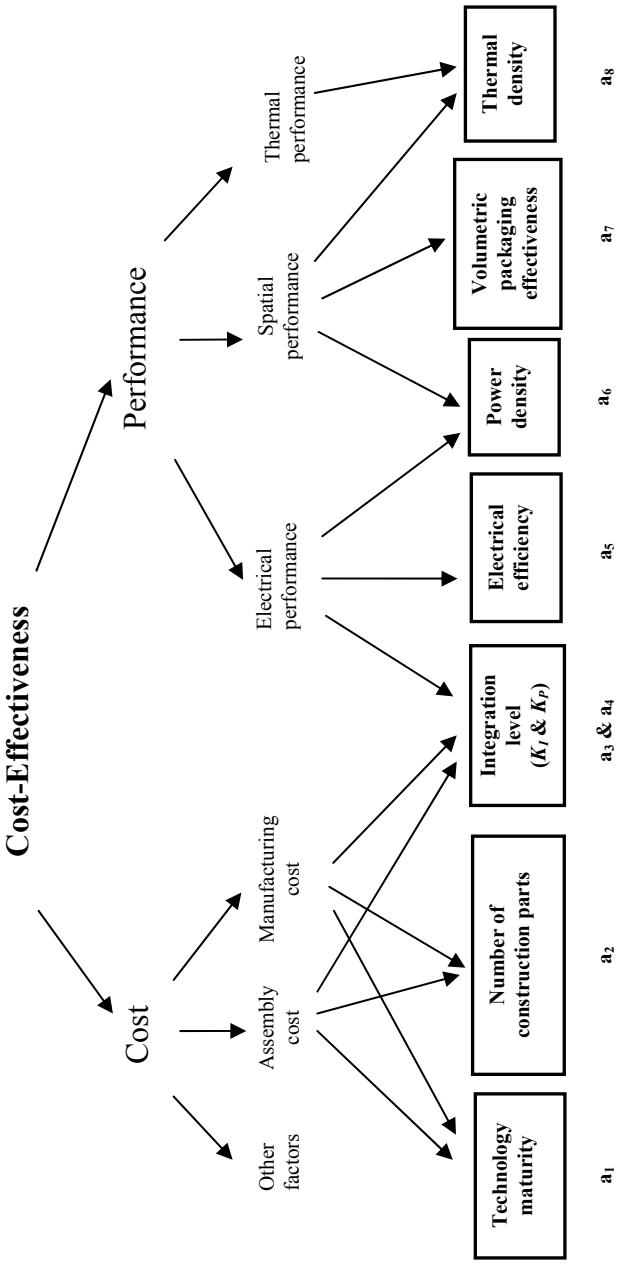


Figure 7-17 Hierarchy tree of objectives

Criteria values: Table 7-4 shows the criteria values of the three construction technology options. The building blocks are named by their most prominent feature: the ceramic technology building block will be referred to as the Heat Conductor Converter, the PCB technology building block as the PCB Embedded Converter and the lead frame technology building block as the Lead Frame Converter. In order to compare the proposed concepts with conventional technology, a discrete converter with conventional components, wire-wound inductor and discrete heat sinking was designed.

Table 7-4 Criteria values of construction options

Criteria / Alternative	Number of parts	K_I	K_P	Techn. maturity	Electrical efficiency [%]	Power density [W/in^3]	Thermal density [W/cm^2]	Volumetric efficiency [%]
Benchmark	42	1	1.15	1	89.9	9.7	0.34	10
HCC	25	1.17	1.53	0.7	90.4	75.6	5.88	45.9
LF	10	1.4	2	0.6	89.7	75.8	0.48	44.5
emPCB	18	2	1.85	0.6	88.8	83.3	0.54	44.8

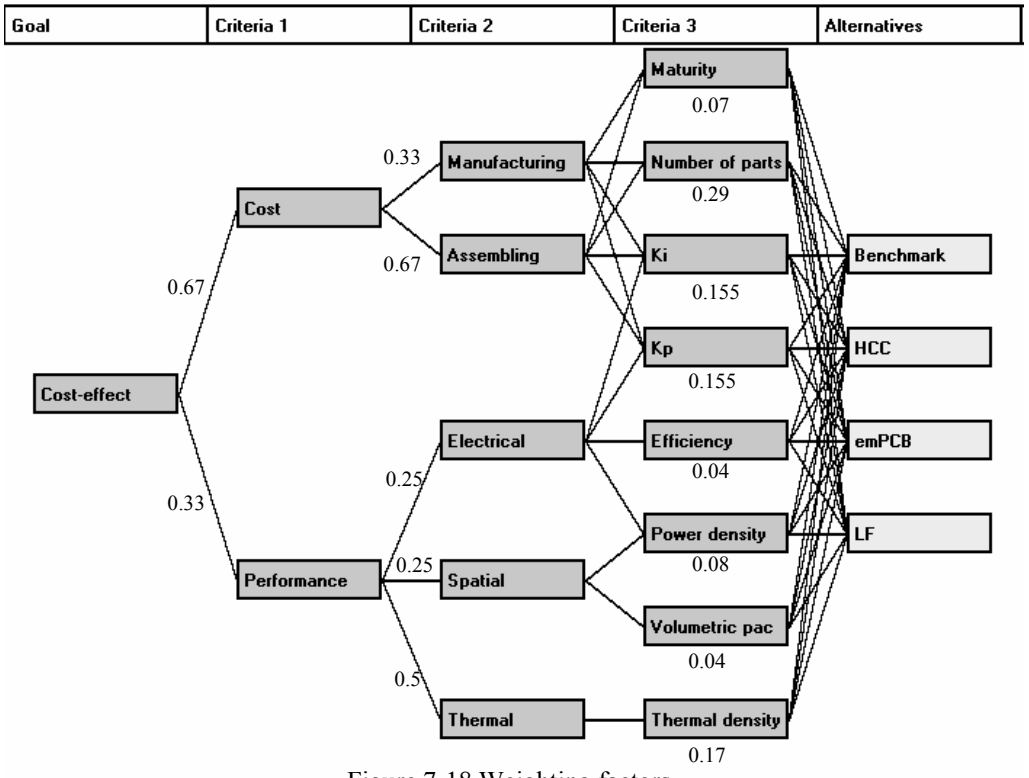
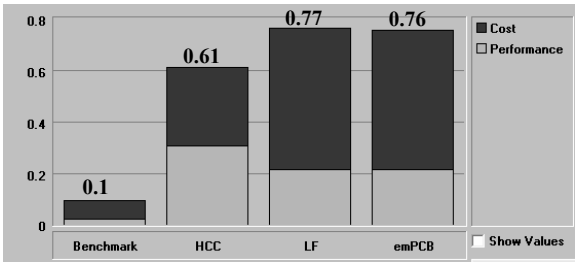


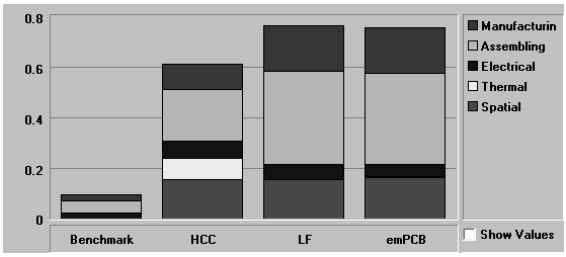
Figure 7-18 Weighting factors

The detailed calculations of the criteria values are shown in Appendix B. The values are calculated according to the design presented in the previous section. The highest value of each criterion is shaded. The Lead Frame Converter has the lowest number of parts and the highest level of PE integration due to its simple construction and multifunctionality of the lead frame. The PCB Embedded Converter has the highest value of FE integration due to the embedded capacitance and inductance. The Heat Conductor Converter has a higher electrical efficiency than the Lead Frame Converter and PCB Embedded Converter since the latter make use of lossy magnetic materials. It can be seen no alternative is inferior to any other alternative in all the criteria, i.e. there are no dominated alternatives.

Weighting factors: The weighting factors are determined by the AHP (Analytic Hierarchy Process) method outlined in Chapter 6. Figure 7-18 shows the weighting factors for the first two levels and the final weighting factors. The preferences that lead to these factors are shown in Appendix B.



a.



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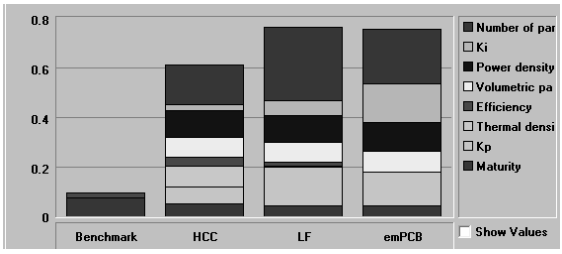


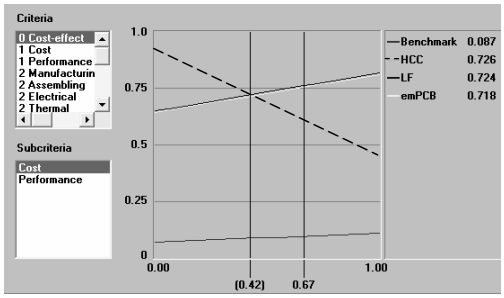
c.

Figure 7-19 Construction technology value function results a. First-level criteria b. Second-level criteria c. Final criteria

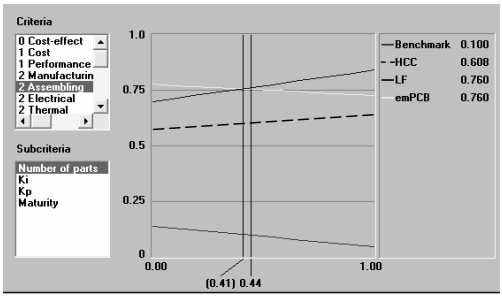
Evaluation results: Following the same procedure used in Chapter 6 to evaluate the various construction technology options for power modules and PCB power supplies, the weighting

factors and criteria values are inserted into the decision software Web-Hipre model. The results are shown in Figure 7-19. Figure 7-19a, Figure 7-19b and Figure 7-19c show the construction technology value function broken down to the first-, second- and third-level criteria, respectively. Figure 7-19a also shows the total values of the function. The Lead Frame Converter scores the highest, closely followed by the PCB Embedded Converter. It is important to notice that all three options score much higher than the conventional discrete option.

Sensitivity analysis: As described in Chapter 6, it is important to analyze the sensitivity of the evaluation results on variations in weighting factors and criteria values. This is especially important in this case considering the very close values of the construction technology value function for all the three converters and given that the criteria values are calculated in the design phase, before the actual converters are manufactured and tested.



a.



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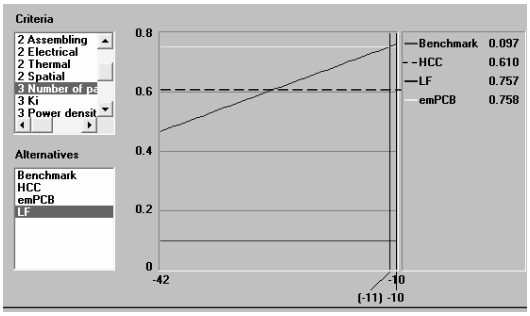

c.

Figure 7-20 Sensitivity analysis a. Weighting factors – First-level criteria b. Weighting factors – Second-level criteria c. Final criteria values

The sensitivity analysis is performed in the same decision software as in Chapter 6 and the most sensitive weighting factors and criteria values are shown in Figure 7-20. Regarding the weighting factors of the first-level criteria (Figure 7-20a), the cross point is 0.42 for the cost criteria (0.58 for the performance criteria). If the weighting factor is below 0.42, the Heat Conductor Converter becomes superior above the Lead Frame Converter. Figure 7-20b shows the sensitivity of the results on the weighting factors of the second-level criteria. If the weighting factor of the number of parts criteria is lower than 0.41 (cross point), the function value of the PCB Embedded Converter becomes higher than that of the Lead Frame Converter.

The current weighting factor of this criterion is 0.44, which means that a small variation in preferences would result in a different evaluation result.

As regards the sensitivity of the result on variations in the criteria values, Figure 7-20c shows that the cross point for the number of parts for the Lead Frame Converter is 11. If the number of parts in this converter is higher than this value, the Heat Conductor Converter would be the option of choice. Again, a small variation (the current value is 10) would result in a change in the evaluation outcome. The rest of the sensitivity analysis results are shown in Appendix B.

7.4.4. Design of processes

For the manufacturing of construction parts and the assembling of the three proposed concepts, mostly standard processes used in power electronic assemblies are employed.

Heat conductor converter

The ceramic carrier is manufactured by standard ceramic processing, and the hole for the centre leg of the magnetic core is formed by laser cutting. The heat conductor, the rest of the other bus bars and solder tabs are manufactured by metal forming and shaping processes such as stamping or machining.

The processes for manufacturing the rest of the parts and assembling them are standard. The MOSFETs, controller and soldering tabs are soldered onto the ceramic carrier. The heat conductor bus bar is glued onto the bottom side of the carrier. This is followed by the ferrite core placing. The two halves are clamped together. The PCC capacitors are soldered onto the ground and 42 V bus bars into one sub-assembly. This assembly is then soldered onto the heat conductor converter as the 14 V connection. The assembly is finished by soldering the solder tabs onto the bus bars.

PCB embedded converter

The capacitive laminates used in this concept are manufactured by processes used for manufacturing FR4 fibreglass reinforced epoxy laminates filled with inorganic fillers (ceramic powder) such as mixing, impregnating with resin, drying and pressing together with the copper sheets. The magnetic laminates are manufactured as composite polymers, with ferrite powder in a polymer matrix. These materials are laminated together with FR4 laminates in the standard multilayer PCB process.

The manufacturing of the PCB is followed by the soldering of all the surface-mount FEs and PCC capacitors in one reflow process.

Lead frame converter

The lead frame carrier in this concept is manufactured by stamping. The bare die MOSFETs and controller are soldered onto the appropriate lead frame pads and these pads are mounted onto the copper block by means of the adhesive tape. The control PCB is manufactured and the surface-mount control FEs are soldered onto the PCB. Afterwards, the wire bonding step is

performed. This is followed by placing the PCC capacitors on the lead frame and soldering their terminals onto the respective lead frame terminals. Finally, the assembly is finished by encapsulation, which is manufactured by a two-step insert injection moulding process, the first step for the ferrite composite moulding material and the second for plastic encapsulation.

7.4.5. Other technology bases

Besides the three chosen technology platforms, other technologies presented in Chapter 5 could be applied to increase the level of integration.

The large number of parts in discrete heat sinking can be reduced by using Insulated Metal Substrates (IMS). This substrate also allows for bare die attachment of power semiconductors further reducing a number of total packaging elements. Due to its cost lead over ceramic substrates and mechanical ruggedness it allows for an implementation of both power and control circuitry on a single substrate. Since IMS is a polymer substrate on a metal base, the advantage over standard PCB is easier mounting onto the heat sink.

Concerning other plastic-based technologies, Moulded Interconnect Devices is a version of lead frame technology. Since the principle is the same, they would differ in the manner that the metallization pattern is produced and perhaps three-dimensional layout, since MID offers more freedom in 3D design.

Considering other ceramic technologies, Direct Bond Copper allows for higher power levels, which would make it possible to implement building blocks with a higher power rating. However, the disadvantage is higher cost and the inability to integrate passive components on the same substrate. Advanced planar interconnection technologies, such as Embedded Power, Flip-chip on Flex, and Dimple Array, allow for double-sided cooling, 3D spatial integration and higher power densities. On the other side, high interconnection density ceramic technologies such as Low Temperature Co-fired Ceramic (LTCC) allow for the integration of small control passive components, thus increasing the level of functional elements integration.

7.5 Summary

This chapter merges the formal methods for increasing the level of integration derived in Chapter 4 and technologies for integration presented in Chapter 5 into a design procedure for increasing the level of integration in power electronic converters.

In Section 7.2, the complete process of designing a power electronic converter from the input specifications to the manufactured product was approached in a systematic manner. The design process was split up into three phases: design-of-functions, design-of-parts and design-of-processes. The functional requirements and design parameters of each phase were identified. The *design-of-functions* phase involves mapping input specifications and constraints onto electrical and thermal circuit schematics. The *design-of-parts* phase deals with mapping the electrical and thermal circuits onto physical construction parts, FEs and PEs. The *design-of-*

processes phase deals with processes for manufacturing of the parts and assembling them into the final product.

The design procedure for increasing the level of integration was presented in Section 7.3. The procedure belongs to the design-of-parts phase. It was presented in the form of an algorithm, and explores the possibilities of increasing the functionality of the FEs and PEs by embodying the formal integration methods by means of the integration technologies.

The presented design approach has several advantages above the conventional design approach presented in Chapter 2. Firstly, this approach includes integral electrical, thermal and spatial design, and this allows for the fulfilment of multidisciplinary and often contradictory requirements. Secondly, it continuously links the physical and functional domain throughout the whole design process, allowing for an optimized physical implementation of the converter, with higher level of integration and fewer parts and processes. Thirdly, the design is approached in a systematic way, as compared with the rather unsystematic current design practice.

In Section 7.4, the complete design process was illustrated by way of a case study of a dc-dc converter for dual powernet automotive applications. Three concepts based on different technology platforms, namely ceramic, PCB and lead frame technology platforms, were designed according to the design algorithm. Furthermore, the concepts were evaluated on the basis of a number of criteria through the process presented in Chapter 4 and the best option was selected.

The presented algorithm is general and can be applied to any power electronic converter regardless of the specific nature of the concrete example.

7.6 References

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Chapter 8: Manufacturing and assembly, electrical and thermal performance of the building blocks

8.1 Introduction

In Chapter 7, an algorithm for increasing the level of integration in power electronic converters was introduced and set in the whole design process. This algorithm was implemented in a case study of a dc-dc 42 V/ 14 V converter for automotive applications. The converter is implemented in three technology platforms: ceramic, PCB and lead frame. Since these three technology platforms are limited in power level they can handle, a modular approach is to be employed. Therefore, these converters can be used as building blocks that are connected in parallel in order to achieve the desired power rating. In Chapter 7, the physical implementation of the converters was designed, including FEs, PEs and their spatial arrangement, according to the outputs of the design of the electrical and thermal functions.

In this chapter, the manufacturing of the converter parts and assembling them to make the final converter is described for each building block. Some materials and technology issues that are encountered during the physical implementation are addressed. The building blocks were tested and the results of the electrical and thermal measurements are presented and compared to the design values. In Section 8.2 the converter parts and assembly steps of the Heat Conductor Converter are presented, followed by the results of the experimental evaluation of the electrical and thermal performance. Section 8.3 and Section 8.4 deal with the same aspects concerning the PCB Embedded Converter and Lead Frame Converter respectively.

In Section 8.5, the three building blocks are compared to each other and the benchmark converter built in conventional discrete technology. The comparison is based on their ease of assembly, the electrical and thermal performance and ease of implementing a modular approach based on each block.

The chapter is summarized in Section 8.6.

8.2 Heat Conductor Converter

Figure 8-1 summarizes the conceptual design of the Heat Conductor Converter presented in Chapter 7. The circuit carrier is a ceramic substrate metallized in thick film technology. The power MOSFETs Q_1 and Q_2 and the control circuitry FEs in the SMD form are soldered onto the circuit carrier. The bottom side of the ceramic carrier is attached to a copper bus bar that serves as the heat path from all the FEs to the heat sink, implements one inductor winding, provides the mechanical support and 14 V terminal. The magnetic core is implemented as a

low profile planar core. The input and output filter capacitive FEs are implemented as bare metal film Power Chip Capacitors (PCC).

8.2.1. Materials and technology issues

The Heat Conductor Converter design presented in Chapter 7 is based on an assumption that some FEs, in particular input and output capacitive FEs, can be obtained in custom size. However, as these capacitors are still in the experimental phase, only a limited range of capacitor sizes was available. Hence, in the final converter, the capacitors with the capacitance value of 70 μF and size 50 mm X 30 mm X 5 mm were used. Therefore, instead of placing them next to each other underneath the thermal bus bar as shown in Figure 8-1, the capacitors are stacked on top of each other. It was shown in Chapter 7 that the capacitance value of 20 μF would be satisfactory. The size of the capacitors with this capacitance value would allow for the arrangement from Figure 8-1, which would result in a lower profile and therefore higher power density of the converter.

Furthermore, double-sided metallization of the ceramic substrate would allow for attaching the thermal bus bar onto the bottom side of the ceramic by means of soldering rather than gluing. Since the thermal conductivity of solder is ~ 40 W/mK while the thermal conductivity of the electrically conductive silver epoxy is ~ 1.5 W/mK, this would result in a significant reduction of the thermal resistance of the main heat path, which would allow for managing more heat and therefore handling a higher output current.

The maximum operating junction temperature of the controller with integrated gate drives TPS40051 specified in the data sheet is $Tjmax_{IC}$ = 125 °C, which is a limiting factor in increasing the power level of the converter since the main heat path for the dissipated heat is through the ceramic. The same device with higher maximum operating temperature ($Tjmax_{IC}$ = 150 °C), specifically intended for automotive applications, is supplied by the manufacturer but was not available from the component supplier at the time of the design.

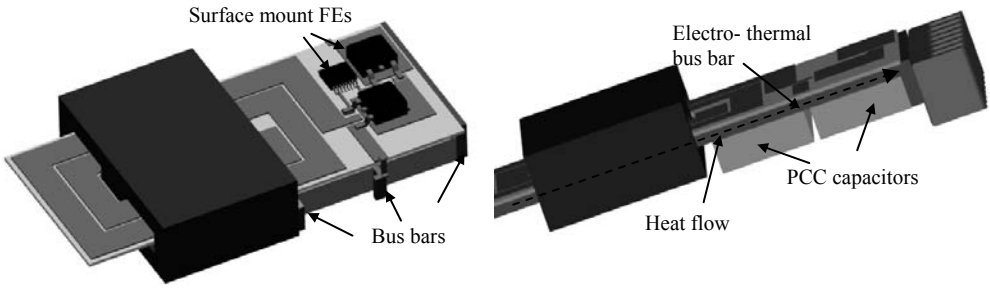

Figure 8-1 Heat Conductor Converter – construction technology concept

8.2.2. Construction parts and assembly steps

Figure 8-2 shows the construction parts of the Heat Conductor Converter. Figure 8-2a shows the power MOSFETs, controller, control passive FEs, PCC capacitor and the E and I halves of the magnetic core.

Figure 8-2b shows the ceramic substrate, which is made of Alumina (Al_2O_3) and has the thickness of 0.635 mm. The ceramic metallization is single-sided. The conductor pattern is printed in two layers. The first layer is printed with a platinum-silver composition [Dup] and has the thickness of 10 µm - 12 µm. This layer implements the complete conductor pattern and the second layer is printed with a silver composition [Dup], has the thickness of 55 µm and is only printed on the power tracks. The thick film metallization is protected with a dielectric coating to prevent silver migration.

Figure 8-2c shows the electro-thermal bus bar and the rest of the bus bars. They are made of copper and manufactured by the machining process.

Figure 8-3 shows the sequence of assembling the converter parts. The MOSFETs and control circuit FEs are attached onto the ceramic carrier by means of reflow soldering (Figure 8-3a). The next step is gluing the electro-thermal bus bar onto the ceramic carrier (Figure 8-3b). This is followed by assembling the ferrite core (Figure 8-3c). The PCC capacitors are stacked on top of each other and insulated by a layer of polyimide film Kapton [Dup] (Figure 8-3d). The bus bars are soldered onto the capacitor stack and this sub-assembly is soldered onto the electro-thermal bus bar (Figure 8-3e).

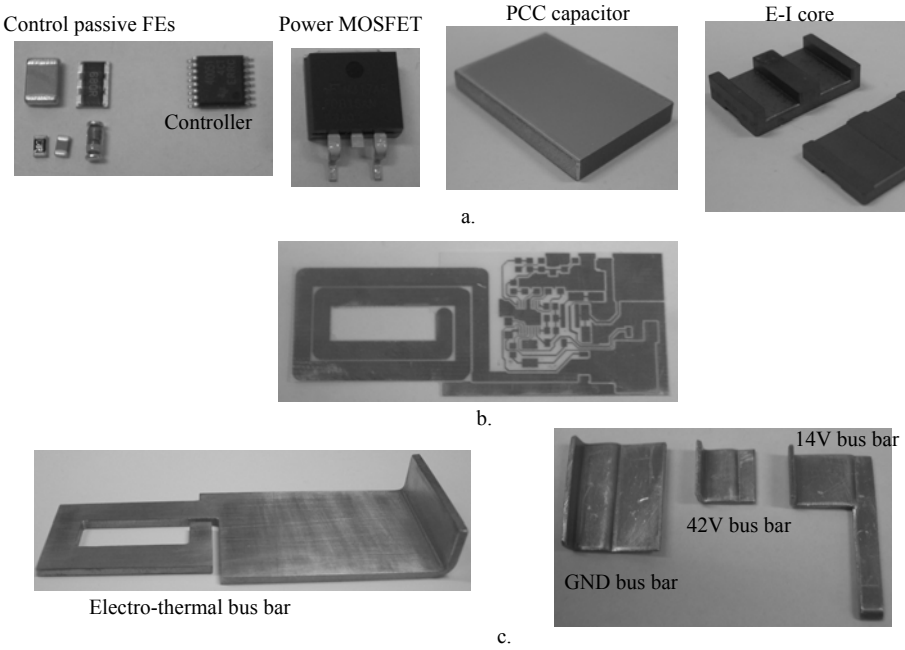

Figure 8-2 Heat Conductor Converter – construction parts

The electrical interconnections between the ceramic substrate and the bus bars are provided by means of solder tabs. These tabs can be soldered onto the ceramic substrate together with the MOSFET and control circuitry in one soldering process. The assembly process is completed by attaching the electro-thermal bus bar to the heat sink surface by means of thermally conductive (k_{resin} = 0.8 W/mK) double-sided adhesive tape Bond-Ply 100 [Ber] (Figure 8-3f). This tape also provides the electrical insulation between the MOSFETs and the heat sink.

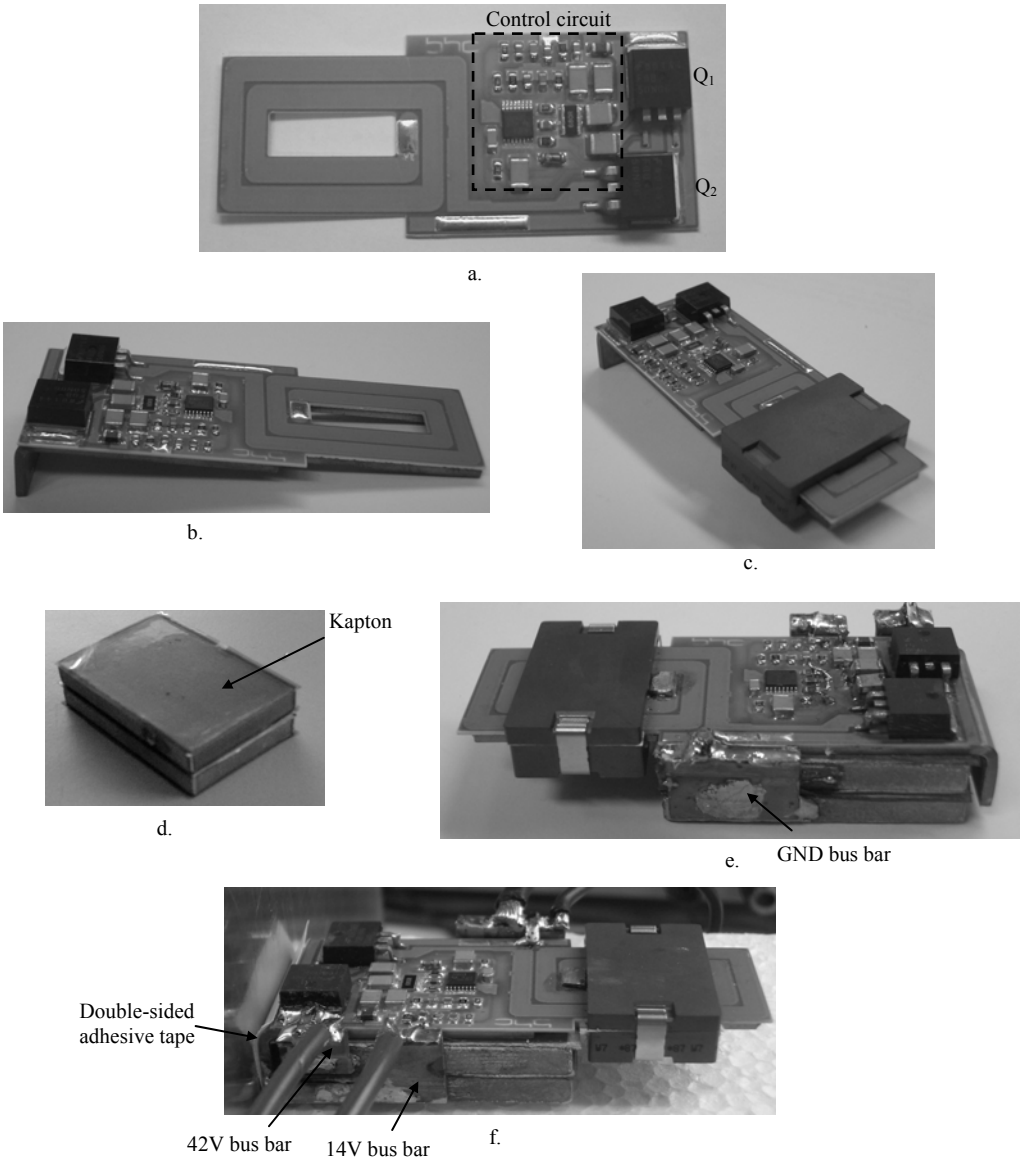

Figure 8-3 Heat Conductor Converter – assembly process

8.2.3. Electrical and thermal performance

In order to test the converter at the conditions as close as possible to those in the automotive environment, the converter is mounted onto an oil-cooled heat sink the temperature of which can be controlled between -20 °C and 150 °C with an accuracy of 0.1 °C.

The converter's electrical efficiency was measured at four heat sink temperatures 25 °C, 40 °C, 60 °C and 85 °C. The results are shown in Figure 8-4. The obtained efficiency values are between 90.3% and 95.2% over the power range from 40 W to 140 W (full power) and the heat sink temperature range.

The losses in all FEs are estimated in Appendix B. The estimated values for the losses in the 14V capacitor are P_{C14} = 0.1 W, in the 42 V capacitor P_{C42} = 0.43 W, in the inductor winding (dc and ac losses) P_{wind} = 1.76 W and in the core P_{core} = 0.32 W. If the MOSFETs losses are added up, the total losses in the converter (at 25 °C) are P_{loss} = 14.99 W, while the measured losses in the converter at full power at 25 °C are P_{loss_meas} = 13.9 W.

The MOSFETs and controller's temperatures were measured by means of thermocouples. Figure 8-5 shows the measured MOSFETs and controller's temperatures over the whole power range at the heat sink's temperature T_{hs} = 85 °C. The obtained values for the temperatures of the MOSFETs cases at full power and T_{hs} = 85 °C are Tc_{Q1} = 125.9 °C and Tc_{Q2} = 110.3 °C and the measured controller's case temperature is Tc_{IC} = 105.2 °C. The junction temperatures of the MOSFET Q_i and controller are calculated according to the expression:

$$Tj_{Qi} = Tc_{Qi} + Rth_{j\_c} \cdot P_{loss\_Qi} \tag{8.1}$$

The obtained values of the junction temperatures of the MOSFETs are Tj_{Q1} = 137.3 °C and Tj_{Q2} = 113.7 °C and the controller Tj_{IC} = 105.8 °C. The values correspond within 8% with the simulated design values (Tj_{Q1} = 127.2 °C, Tj_{Q2} = 108.9 °C and Tj_{IC} = 108.9 °C) presented in Chapter 7.

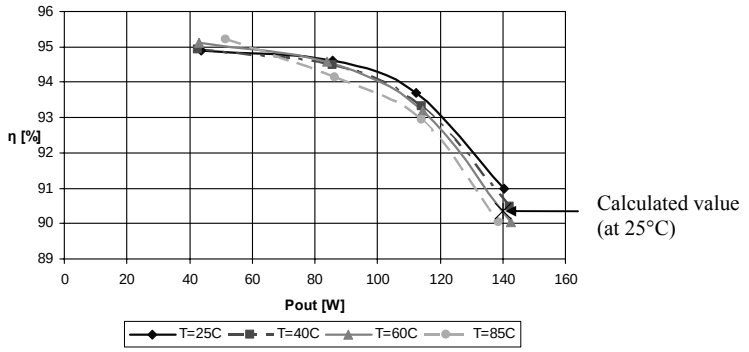

Figure 8-4 Electrical efficiency measurements of Heat Conductor Converter

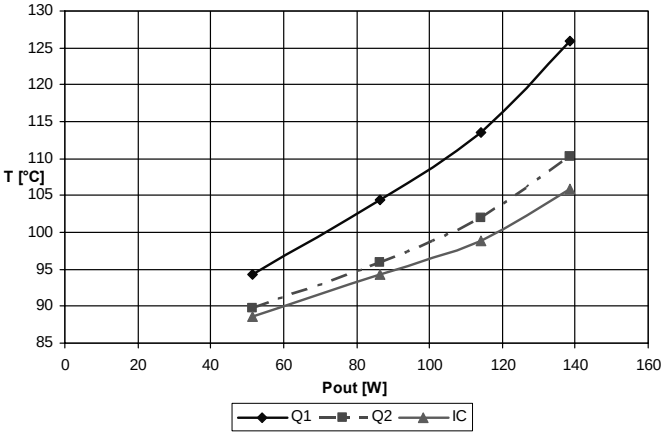

Figure 8-5 Heat Conductor Converter's temperature measurements at T_{hs} = 85 °C (case temperatures)

The dimensions of the Heat Conductor Converter are 34 mm X 82 mm X 16 mm and power density is 51.4 W/in3.

8.3 PCB Embedded Converter

Figure 8-6 shows the physical implementation concept of the PCB Embedded Converter. The inductance FE is embedded in the PCB by means of magnetic laminates, the capacitive FEs are realized in low profile bare metal film capacitors and the rest of the FEs are implemented in the SMD form on the top side of the PCB. The bottom side of the PCB is mounted onto the heat sink by means of a double-sided adhesive tape. The heat dissipated by the MOSFETs and the integrated controller is spread over the copper pads and then conducted through the thermal vias to the heat sink.

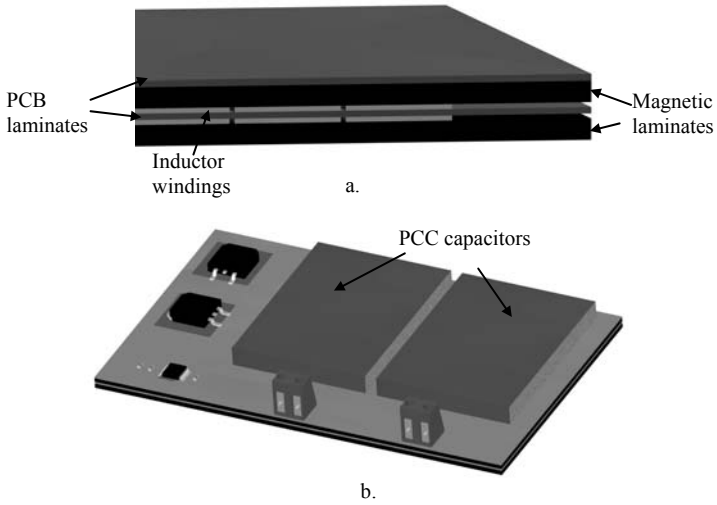

Figure 8-6 PCB Embedded Converter – construction concept

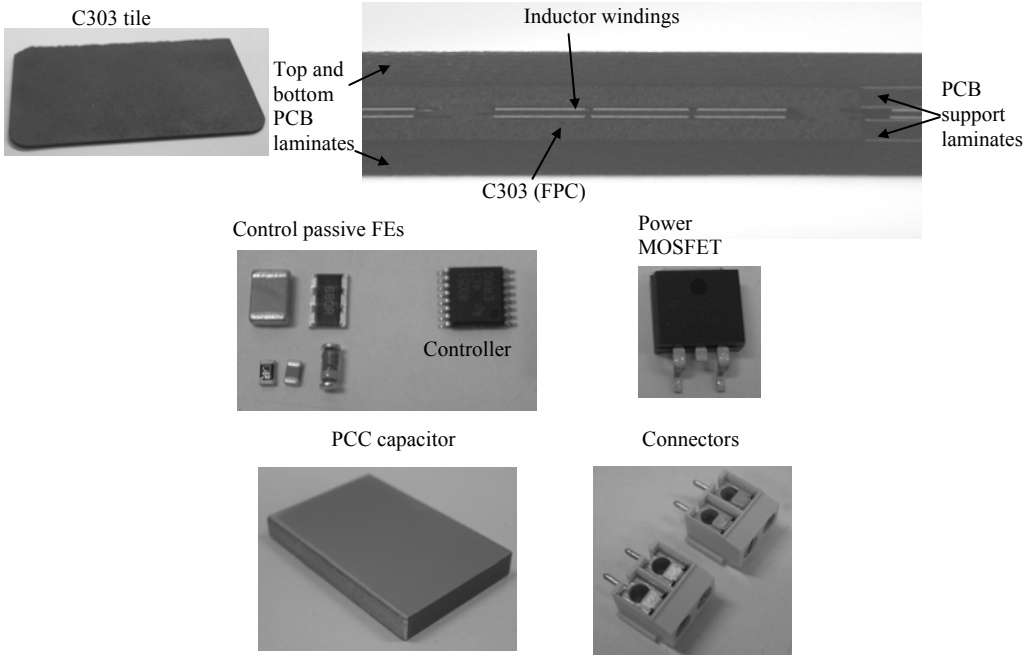

Figure 8-7 PCB Embedded Converter – parts

8.3.1. Materials and technology issues

As discussed in Chapter 7, polymer like laminates filled with ferrite powder, such as MagLam by Isola [Iso] or Ferrite Polymer Composite (FPC) materials by EPCOS [Epc], are suitable for implementing magnetic FEs in this construction technology option. One of the issues regarding these materials is their rather low permeability (< 20). Another issue is the availability of these materials. MagLam was successfully used in the realization of a 60 W off-line converter presented in [Waf05]. However, at the time of the design of this technology demonstrator it was not possible for the author to obtain this material. The situation was similar with the FPC material C351. The only available material was dye pressing material C303 [Epc] and the design presented in Chapter 7 was based on this material.

As with the Heat Conductor Converter, the capacitance values (70 μF) of the PCC capacitors used in manufacturing the PCB Embedded Converter are based on the availability of these capacitors rather than the design values. As shown in Chapter 7, the value needed to satisfy the output voltage ripple requirements, for the inductance value given in Chapter 7, is 35 μF, which means that capacitors of half the size could be used, which would result in an overall size reduction of the converter.

8.3.2. Construction parts and assembly steps

Figure 8-7 shows the construction parts of the PCB Embedded Converter. Since the C303 material is not in the form of a laminate but dye pressed tiles, the inductor was embedded in the PCB by means of PCB support layers as shown in Figure 8-7a. The PCB is made of five PCB laminates. The middle laminate is double-sided metallized with the copper thickness of 70 μm and carries the inductor windings. The two C303 tiles are embedded in two support laminates. Finally, the top and bottom laminates metallized single-sided (copper thickness 70 μm) carry the circuitry tracks. The inductance value is measured with an impedance analyzer and the obtained value is L_{meas} = 4.37 μH. This value corresponds well with the design value given in Chapter 7 (L_{design} = 4.45 μH). The rest of the PCB Embedded Converter parts, SMD MOSFETs and control circuit FEs, PCC capacitor and connectors are also shown in Figure 8-7.

The assembling process of the converter starts with the manufacturing of the PCB. Firstly, the tracks of the inner layer that carries the inductor windings are structured by means of etching or in this case milling with a PCB manufacturing prototyping machine. The inner layer, two support PCB layers with the embedded C303 tiles on top and bottom of the inner layer and the top and bottom layers are laminated together. This is followed by drilling and plating the vias for electrical interconnections and heat conduction. The top and bottom PCB layers are then milled (or etched) to obtain the desired conductor pattern. The top side of the manufactured PCB is shown in Figure 8-8a.

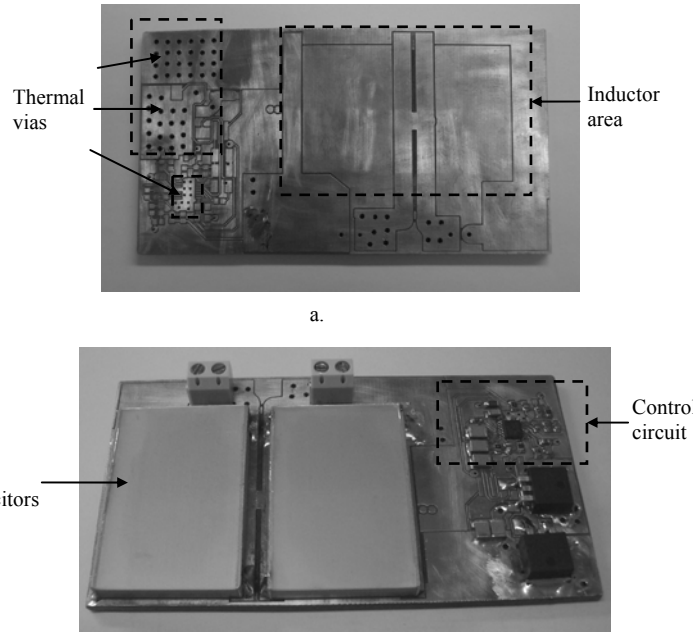

Figure 8-8 PCB Embedded Converter – assembly steps

This is followed by soldering the SMD components, PCC capacitors and input and output connectors onto the PCB (Figure 8-8b). The assembling process is finished by attaching the

bottom side of the converter onto the heat sink by using the same double-sided adhesive tape as used to attach the Heat Conductor Converter to the heat sink.

8.3.3. Electrical and thermal performance

The converter's electrical efficiency was measured over the whole power range at four heat sink temperatures: 25 °C, 40 °C, 60 °C and 85 °C. The results are shown in Figure 8-9. As can be seen from the figure, the achieved efficiency is between 87% and 89% over the whole power range and the heat sink temperature range.

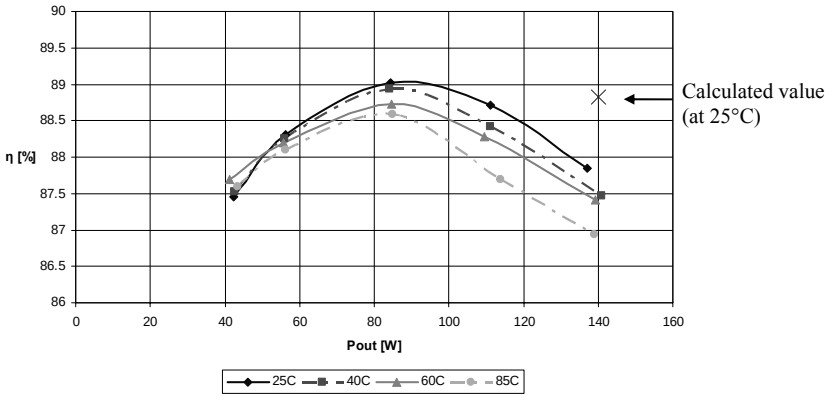

Figure 8-9 Electrical efficiency measurements of PCB Embedded Converter

The losses in all FEs are estimated in Appendix B. The estimated values for the losses in the 14V capacitor are P_{C14} = 0.31 W, in the 42 V capacitor P_{C42} = 0.45 W, in the inductor winding P_{wind} = 4.35 W and in the core P_{core} = 0.71 W. If the MOSFET losses are added up, the total losses in the converter are P_{loss} = 17.62 W, while the measured losses are P_{loss_meas} = 18.96 W.

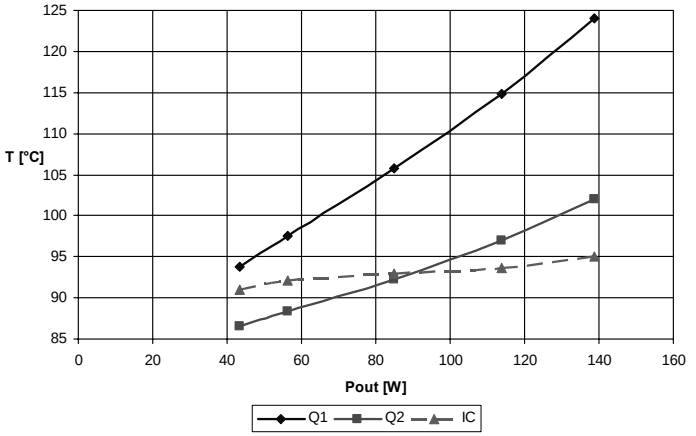

Figure 8-10 PCB Embedded Converter temperature measurements at T_{hs} = 85 °C (case temperatures)

The MOSFETs and controller's case temperatures were measured at the four heat sink temperatures over the whole power range. The results at T_{hs} = 85 °C are shown in Figure 8-10.

The measured temperatures of the MOSFETs cases at full power and the heat sink temperature T_{hs} = 85 °C are Tc_{Q1} = 124 °C and Tc_{Q2} = 102 °C and the measured controller's temperature is Tc_{IC} = 95 °C. The junction temperature of the MOSFET Q_i is calculated according to (8.1) and the values obtained are: Tj_{Q1} = 134.7 °C and Tj_{Q2} = 105.4 °C and Tj_{IC} = 95.6 °C and the values correspond within 2% with the design values presented in Chapter 7 (Tj_{Q1} = 132.5 °C, Tj_{Q2} = 103.4 °C and Tj_{IC} = 94.2 °C).

The dimensions of the PCB Embedded Converter are 61.5 mm X 101.8 mm X 8.5 mm, which gives the power density value of 43.1 W/in^3.

8.4 Lead Frame Converter

Figure 8-11 shows the physical implementation concept of the Lead Frame Converter. The lead frame provides the carrier for the bare die power MOSFETs and controller, implements the inductor winding and provides the mechanical support for the bare metal film capacitive FEs. The electrical interconnections between the MOSFETs and controller and the lead frame are provided by means of wire bonding. The control passive FEs are implemented on a separate carrier, PCB or ceramic. The whole converter is encapsulated by means of insert moulding for protection and for holding the assembly together. As part of the moulding process, the injection moulding composite ferrite material is inserted around the lead frame inductor winding to provide an inductance enhancement. The heat dissipated by the MOSFETs and controller is conducted through a metal block to the heat sink. The electrical insulation between the MOSFETs and the heat sink is provided by means of the double-sided adhesive tape Bond-Ply 100 that is used for attaching the MOSFET pads onto the copper block.

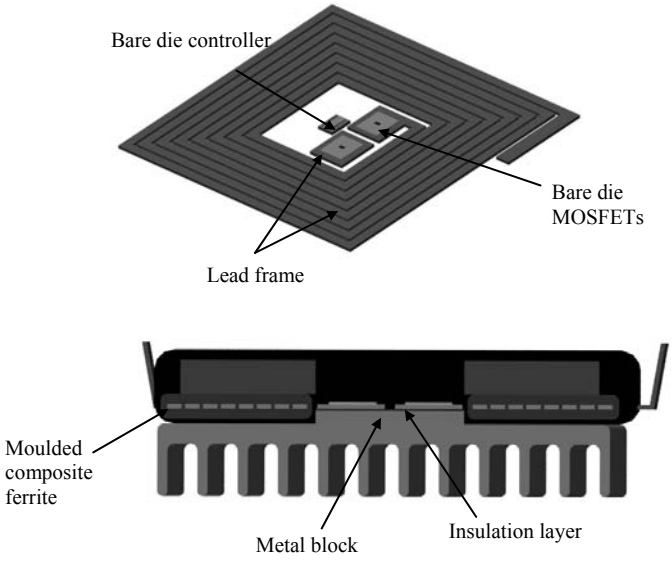

Figure 8-11 Lead Frame Converter – construction concept

8.4.1. Materials and technology issues

The design of the inductance enhancement in Chapter 7 is based on the ferrite polymer composite material C302, which is suitable for injection moulding. However, at the time of manufacturing of the converter, it was not possible for the author to obtain this material from the manufacturer. Therefore, the inductance enhancement was achieved by placing two sheets of the composite VITROPERM-epoxy material on the top and bottom of the inductor winding.

Also, the facilities necessary to carry out the wire bonding process were not available at the time of the converter manufacturing: hence the MOSFETs and controller in the SMD form are used.

In the same way as for the Heat Conductor Converter and PCB Embedded Converter, the capacitance values (70 μF) of the PCC capacitors used in manufactured the Lead Frame Converter are based on the availability of these capacitors rather than the design values. In Chapter 7 was shown that the value needed to satisfy the output voltage ripple requirements for the achieved inductor value is 33 μF, which means that capacitors of half the size could be used, which would result in an overall size reduction of the converter.

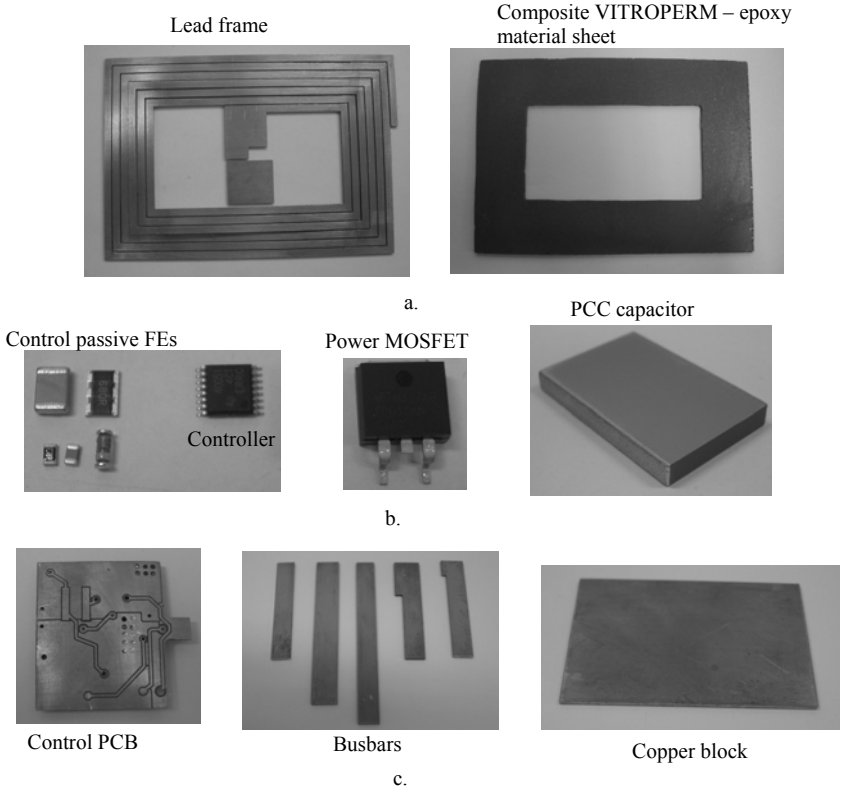

Figure 8-12 Lead Frame Converter – converter parts

8.4.2. Converter parts and assembly steps

Since the construction concept presented in Figure 8-11 has to accommodate the input and output capacitors with specific dimensions, the inductor dimensions and shape presented in Chapter 7 had to be modified. The inductor is rectangular, with the inner dimensions 27 mm X 50 mm and outer dimensions 54 mm X 77 mm. The inductance value of the modified inductor obtained by FEM simulation is L_{sim} = 5.65 μH. The inductance value is measured by an impedance analyzer and the obtained value is L_{meas} = 5.03 μH.

Figure 8-12 shows the Lead Frame Converter's construction parts. The lead frame and magnetic material sheet cut to fit the inductor winding are shown in Figure 8-12a. The SMD power MOSFETs, control FEs and PCC capacitors (Figure 8-12b) are the same as in the previous two building blocks. The control substrate (Figure 8-12c) is a double-sided 1 mm thick PCB. The copper block, bus bars and the lead frame are manufactured by the machining process. The encapsulation is provided by a thermally conductive epoxy resin (k_{th_resin} = 1 W/mK).

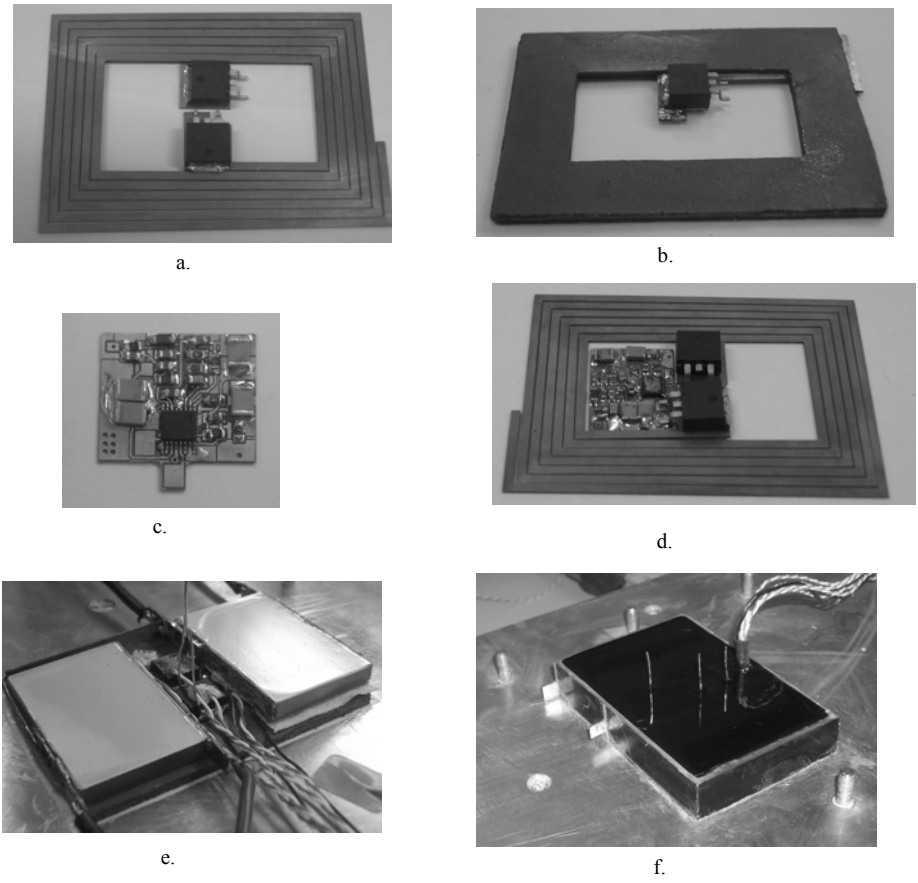

Figure 8-13 Lead Frame Converter – assembly steps

Figure 8-13 outlines the process of assembling the Lead Frame Converter. Firstly, the MOSFETs are soldered onto the corresponding lead frame pads (Figure 8-13a). This is followed by gluing the composite VITROPERM-epoxy sheets on top and bottom of the inductor (Figure 8-13b). The control board is populated with the control circuitry FEs in the SMD packages (Figure 8-13c). The control board and the MOSFET pads (Figure 8-13d) are mounted onto the heat conducting copper block by means of the Bond-Ply 100 tape, described in the previous sections. This is followed by placing the capacitors with pre-soldered bus bars onto the lead frame and soldering the bus bars to their corresponding locations (Figure 8-13e). The assembly is finished by encapsulating the whole converter with the epoxy resin (Figure 8-13f).

8.4.3. Electrical and thermal performance

The electrical efficiency of the Lead Frame Converter was measured over the whole power range at four heat sink temperatures: 25 °C, 40 °C, 60 °C and 85 °C. The results are shown in Figure 8-14. It can be seen from the figure that the converter's efficiency varies from 81.5% at low power to 89% in the region of 100 W.

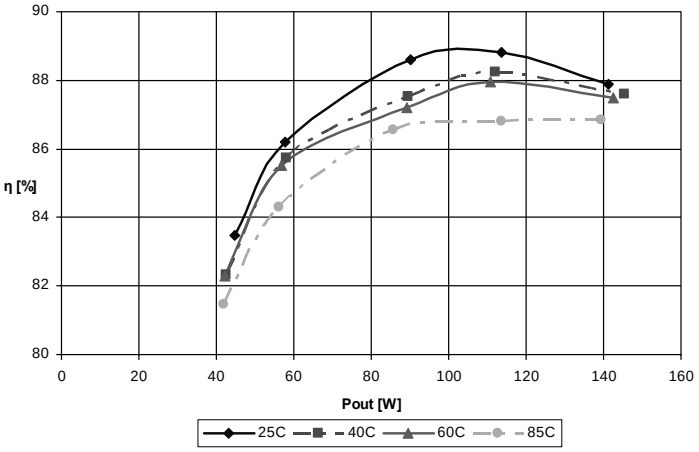

Figure 8-14 Lead frame converter efficiency measurements

The losses in the converter's FEs are estimated in Appendix B. The estimated values for the losses in the 14V capacitor are P_{C14} = 0.23 W, in the 42 V capacitor P_{C42} = 0.44 W, in the inductor winding P_{wind} = 2.54 W. The core losses are not estimated since the loss factor of the composite VITROPERM-epoxy material is not known. If the MOSFET losses are added up, the losses in the converter excluding the losses in the magnetic material at full power and T_{hs} = 85 °C are P_{loss} = 15.3 W, while the total measured losses are P_{loss_meas}= 19.5 W.

In Chapter 7, the thermal design of the MOSFETs and controller is based on the assumption that the FEs in the bare die form will be used. If the SMD packages are used the thermal resistance of the heat paths will change, especially the heat path of the controller since the controller is mounted on the PCB and the heat path is through the PCB. In order to reduce the thermal resistance through the PCB, thermal vias are employed. The junction temperatures of

the MOSFETs and controller are calculated by means of the thermal resistance network method and the obtained values are Tj_{Q1} = 125.9 °C, Tj_{Q2} = 97.7 °C and Tj_{IC} = 97.7 °C.

The MOSFETs and controller's case temperatures were measured by means of thermocouples at the four heat sink temperatures over the whole power range. The results for the heat sink temperature T_{hs} = 85 °C are shown in Figure 8-15. The measured temperatures of the MOSFETs and controller cases at full power and T_{hs} = 85 °C are Tc_{Q1} = 109.9 °C, Tc_{Q2} = 96.2 °C and Tc_{IC} = 99.3 °C. The junction temperatures of the MOSFETs and controller are calculated according to (8.1) and the values obtained are: Tj_{Q1} = 120.91 °C and Tj_{Q2} = 99.7 °C and Tj_{IC} = 99.9 °C. These values correspond within 5% with the design values.

The dimensions of the Lead Frame Converter are 57 mm X 85 mm X 9 mm and the power density is 52.6 W/in^3.

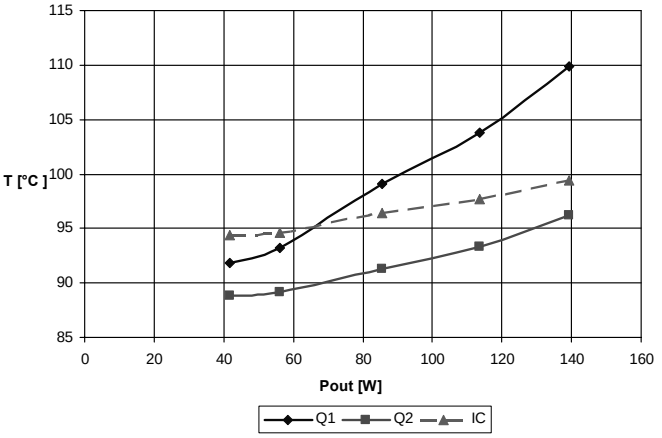

Figure 8-15 Lead Frame Converter's temperature measurements at T_{hs} = 85 °C (case temperatures)

8.5 Comparisons

Electrical and thermal performance

Figure 8-16 shows the comparison of the electrical efficiency of the three converters and benchmark converter over the whole power range at T_{hs} = 25 °C. The difference between the efficiency in the Heat Conductor Converter and the benchmark converter comes from the losses in the capacitors since in the benchmark converter the electrolytic capacitors with higher ESR were used. One of the reasons that the Heat Conductor Converter shows the highest efficiency of the three integrated converters throughout the whole power range are the high losses in the magnetic materials used in the Lead Frame Converter and the PCB Embedded Converter. The difference is the largest at low power levels since in this range the losses in the magnetic material represent a significant percentage of the total losses.

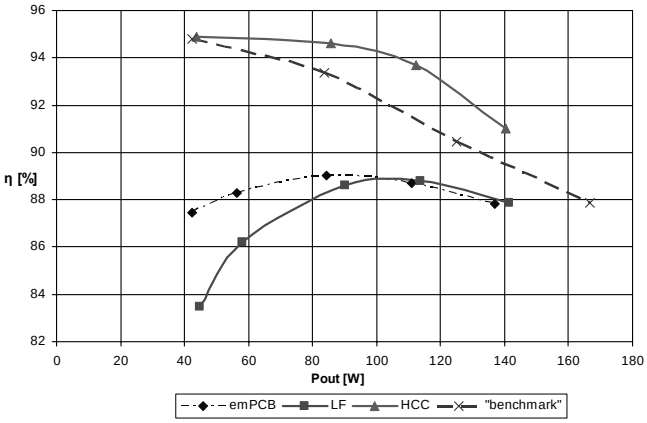

Figure 8-16 Electrical efficiency comparison at T_{hs} = 25 °C

Furthermore, the dc losses in the inductor windings of the PCB Embedded Converter and the Lead Frame Converter are larger than in the inductor winding of the Heat Conductor Converter. The dc losses in the PCB Embedded Converter are the largest of the three, which is the reason that the efficiency of the Lead Frame Converter reaches and even becomes slightly higher than the PCB Embedded Converter efficiency at higher power levels. As for the losses in the MOSFETs, the losses in the low side MOSFET are the same in all three converters. As for the high side MOSFET losses, the largest value of the three is in the Heat Conductor Converter, since the switching losses in this MOSFET during the turn-on are proportional to the turn-on current, which is equal to the difference between the mean value of the inductor current and half of the current ripple value (Appendix B). The value of the inductor current ripple of the Heat Conductor Converter is the lowest of the three.

The losses in the output capacitor C_{14} depend on the value of the inductor current ripple, and since the inductance value and thus the current ripple differ among the building blocks, the losses in this capacitor also vary. They are the largest in the PCB Embedded Converter since the value of the inductor current ripple is the highest. However, the losses in this capacitor are low: the estimated value in the PCB Embedded Converter is only 0.31 W, which is only 5% of the total losses at the lowest measured operating point (I_{14} = 3 A) and less than 2% at full power. The losses in the input capacitor C_{42} do not differ significantly with changes in the inductor current ripple.

Since the losses of all the FEs except the magnetic laminate FEs at low power in the PCB Embedded Converter are very close to or larger than those in the Lead Frame Converter, it can be concluded that the losses in the magnetic material in the Lead Frame Converter make up a significant portion of the total losses in this converter. The difference between the estimated and measured losses is another indication thereof.

Figure 8-17 shows the measured temperatures of the high side MOSFET Q_1 for all three converters at T_{hs} = 85 °C over the whole power range. The temperature of the high side MOSFET in the Lead Frame Converter is the lowest, which is expected due to the lowest

thermal resistance heat path to the heat sink. Regarding the integrated controller, the lowest temperature rise is achieved in the PCB Embedded Converter since the thermal path of the heat dissipated by the controller is through the thermal vias and is decoupled from the MOSFETs' heat paths. In case of the Heat Conductor Converter, the controller uses the same heat path as the MOSFETs, which causes the heat coupling and higher operating temperature. In case of the Lead Frame Converter, the controller's and MOSFETs' heat paths are coupled through the copper block. It was already mentioned Section 8.2.1 that if the same heat path is used for all the FEs that the controller rather than MOSFETs might pose a limit on the current level that the converter can handle.

Power density

In Chapter 7, power density was one of the criteria that the building blocks were evaluated on. The values of power density were calculated on the basis of the design parameters and shown in Table 7-4. The power density values of the manufactured converters are 51.4 W/in^3 for the Heat Conductor Converter, 43.1 W/in^3 for the PCB Embedded Converter and 52.6 W/in^3 for the Lead Frame Converter. The values are lower than the design values due to the modified size and spatial arrangement of the PCC capacitors.

Manufacturing and assembly

The Heat Conductor Converter and PCB Embedded Converter have the advantage of having only one circuit carrier, for both control and power FEs. The Lead Frame Converter utilizes the lead frame for the power FEs and a separate PCB for the control circuit FEs. Except for the more complex process of manufacturing of the PCB due to the utilization of the tiles instead of laminates, the PCB Embedded Converter has the simplest assembly process: it consists of soldering the SMD components and PCC capacitors onto the PCB.

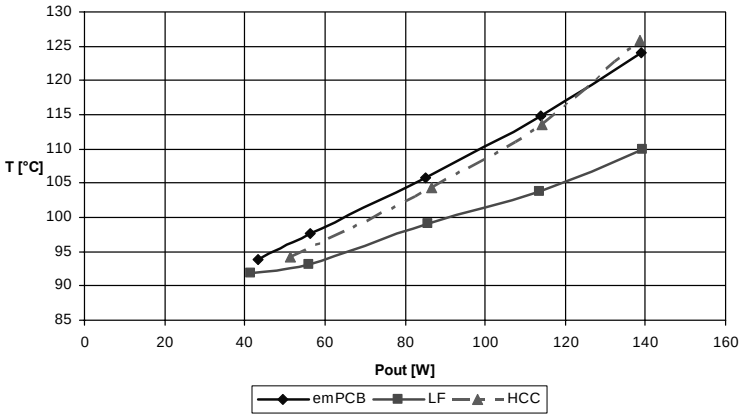

Figure 8-17 High side MOSFET's temperature comparison of in three building blocks

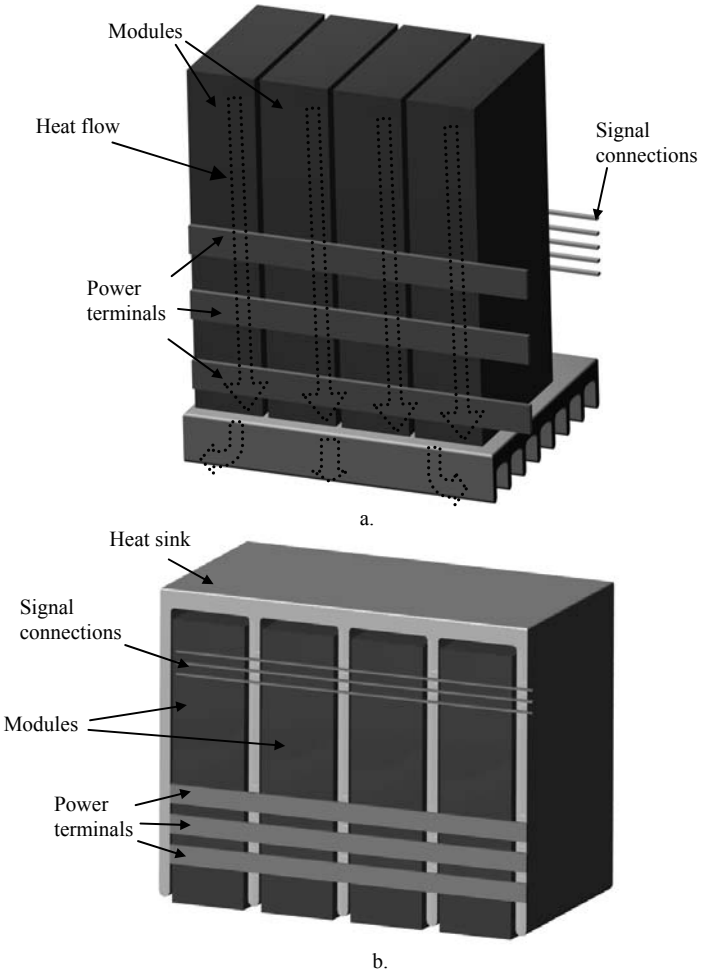

Figure 8-18 Possible modular arrangements a. Heat Conductor Converter building blocks b. Lead Frame Converter and PCB Embedded Converter building blocks

Modular arrangement

It was mentioned in Chapter 7 that due to the fact that the chosen technology platforms are limited to low power levels, a modular approach can be applied in order to reach desired power levels.

Figure 8-18a shows a possible modular arrangement for the Heat Conductor building blocks. The building blocks are stacked next to each other and connected with the power and signal connections for the higher level control. The heat dissipated by the FEs in each building block is conducted via the electro-thermal bus bar to the heat sink as indicated in the figure.

The situation is somewhat different for the PCB Embedded Converter and Lead Frame Converter, since they are to be mounted with the whole converter bottom surface to the heat sink. An arrangement with heat sink flanges that the building blocks are to be mounted on, such as shown in Figure 8-18b, is to be employed.

8.6 Summary

The three building blocks designed in Chapter 7 were experimentally evaluated in this chapter. The results of the electrical and thermal measurements for the Heat Conductor Converter, PCB Embedded Converter and Lead Frame Converter were presented.

The construction parts and assembling steps necessary to construct each converter were presented. Some modifications of the original designs presented in Chapter 7 had to be made due to the availability of certain materials and processes. These technology issues were also discussed for each converter.

The results of the electrical efficiency measurements performed at four heat sink temperatures and over the whole power range were presented for each converter. A set of thermal measurements was performed on each building block and the results obtained were also presented. The results of experimentally evaluated electrical and thermal performance of the converters were compared to the design values. Good correlations between designed and measured values are found.

Finally, the building blocks were compared to each other, including experimentally evaluated electrical and thermal performance, achieved power density, ease of assembly and suitability for being implemented in a modular arrangement.

8.7 References

[Ber] Bergquist company, www.bergquistcompany.com.

[Dup] QS171 Platinum Silver Conductor and 7740 Silver Conductor, DuPont Electronic Materials, www.dupont.com.

[Epc] Ferrite Polymer Composite (FPC) Film, available at: http://www.epcos.com/inf/80/ap/e0001000.htm.

[Iso] Isola, www.isola.de.

[Waf05] E. Waffenschmidt, B. Ackermann, J.A. Ferreira, “Design method and material technologies for passives in printed circuit Board Embedded circuits”; in *IEEE Transactions on Power Electronics*, May 2005, Volume 20, Issue 3, Page(s): 576 – 584.

Chapter 9: Conclusions and recommendations

The thesis deals with improving the physical implementation of power electronic converters by increasing the level of integration.

Chapter 1 identifies the requirements imposed on power electronics by the emerging applications and the role of construction technology of power electronic converters in fulfilling these requirements.

Chapter 2 analyses the present practice of constructing power electronic converters. The large number of parts in power electronic converters together with the design approach that in the phase of modelling and simulations deals with electrical circuit design only and decouples this optimization phase from the physical implementation of the converter are identified as the main drawbacks of the current practice.

In Chapter 3, an approach to dealing with the construction technology of power electronic converters based on a breakdown of the converter into its physical construction parts based on the functions that they perform is introduced. These parts form the basis of an integral design approach. Packaging and integration as two aspects of construction technology are discussed in light of this approach and some parallels between these aspects in power electronics and microelectronics are drawn.

Two quantities that evaluate the level of functional and packaging elements integration are introduced in Chapter 4. The formal methods for increasing the level of integration based on these quantities are also developed in this chapter. Chapter 5 gives an overview of technologies that allow for implementing these methods in actual converters.

A method for evaluating different construction technology options in order to choose the optimal solution for the particular application based on a number of relevant figures of merit is presented in Chapter 6.

Chapter 7 merges the methods devised in Chapter 4, technologies presented in Chapter 5 and foundations of the element-based integral design approach from Chapter 3 into a design algorithm for construction technology with a higher level of integration. Chapter 8 implements this algorithm in a case study of a dc-dc converter for the automotive dual power net applications. This application is suitable as a case study due to the thermally and volumetrically demanding operating environment and a highly cost-driven market.

9.1 Conclusions

The conclusions drawn from this thesis are classified into four categories, based on the objectives presented in Chapter 1:

- To analyze the present philosophy of construction practice and identify its main drawbacks;
- To introduce a systematic approach to construction technology, including integration and packaging;
- To investigate means of improving the construction of power electronic converters by increasing the level of integration through the multifunctionality of parts;
- To develop a method to compare different construction technology options based on a number of important criteria.

Present practice of construction technology in power electronic converters

In the current design approach, electrical parameters of discrete components are inputs to the function optimization phase. This phase deals with only the electrical circuit optimization. The thermal, electromagnetic issues and spatial layout are engineered in the circuit packaging phase, where the electrical circuit is translated into the physical construction. This sequential design practice, where the function optimization phase deals with the electrical circuit design only and where the physical implementation is decoupled from the modelling and simulations phase, does not allow for satisfying the stringent requirements of emerging power electronic applications concerning operating temperature, electromagnetic compatibility and volumetric requirements.

The present way of constructing power electronic converters does not comply with the principles of good design practice that take into account manufacturing and assembly issues, summarized in design for manufacture and assembly (DFMA):

- Number of parts – according to DFMA, a low number of parts in an assembly is an effective way of keeping the assembly cost low. The present design approach based on assembling with discrete components results in a large number of parts in power electronic assemblies.
- Multifunctionality of parts – the functionality of parts in power electronic assemblies is low: one FE mostly implements only one electrical circuit schematic symbol and one PE performs one packaging function for one FE.
- Standardization – according to DFMA, by standardizing parts in an assembly, the cost of the assembly can be kept down due to using the same manufacturing processes and the same production line. In power electronic assemblies, a large diversity of components and parts is found.
- Modularization – according to DFMA, the use of modular construction permits a large unit to be broken down into small units that can be manufactured repetitively and efficiently. In power electronics, modularization is present only in the form of power modules.

Concerning the large number of parts, the number of packaging elements in a typical power electronic converter is normally a few times larger than the number of functional elements. This implies that in order to improve the construction technology, PEs have to be dealt with as well, as opposed to the present design practice where only electrical FEs are dealt with in the function optimization phase.

Furthermore, the large number of parts negatively affects the electrical, thermal, electromagnetic and spatial performance of the converter. This is manifested in a number of effects:

- Electrical parasitic effects of packaging elements – electrical resistance, capacitance and inductance affect the electrical performance and EMI aspect.
- Each part contributes with its thermal resistance to the total thermal resistances of the heat path, thus influencing the heat removal potential.
- Each part takes up volume, which contributes to the total volume of the assembly and limits the power density.

Systematic approach to construction technology, including integration and packaging

As the large number of parts is identified as one of the main shortcomings of the present construction technology practice, the construction technology is to be approached on the basis of the construction parts and functions they perform. Since the thermal and electromagnetic behaviour are fundamentally dependent on the physical implementation of the converter, the integral electrical, thermal, electromagnetic and spatial design approach requires the coupling of the functional domain (design of functions) and the physical domain (design of parts) performed through continuous design interactions.

The integral design approach (electrical, thermal, electromagnetic and spatial) coupled with the physical domain is essentially more complex and time-consuming than the electrical design alone. This can be justified by achieving:

- Higher functionality of parts, both functional elements and packaging elements. This leads to the reduction of the number of parts.
- Modularization and standardization. The breakdown can be performed in two ways:
  - The circuit is partitioned into sub-circuits based on the parameters of the circuit symbols (function they perform and achievement level of function) and each sub-circuit is implemented in the most suitable technology.
  - The circuit is partitioned into a number of equal sub-circuits rated for the low power range. This sub-circuit is implemented in low cost technologies that lend themselves to mass production.

  In both cases, these smaller units can be standardized and used for a number of applications.

The relationship between integration and packaging is translated into the relationship between functional elements integration and packaging elements integration. Functional elements integration transcends packaging elements integration since by means of FEs integration both the number of FEs and PEs can be reduced while by means of PEs integration only the number

of PEs can be reduced. Therefore, possibilities of FE integration in a converter should be exploited first and when the limits of this type of integration are reached, PE integration takes over.

Increasing the level of integration by increasing functionality of converter functional and packaging elements and implementing it in design process

The level of integration can be expressed by the level of multifunctionality of functional and packaging elements. Two quantities, FE integration level and PE integration level, represent the average functionality of FEs and PEs respectively. The FE integration level (K_I) of an assembly shows how many circuit symbols one FE implements on average, while the PE integration level (K_P) of the assembly shows how many packaging functions one PE performs on average. The level of FE integration is low in power electronic converters since mostly discrete components are employed where one FE corresponds to one electrical circuit schematic symbol. The PE integration is also low, and it is only applied through circuit carriers and in power modules.

Since power electronics is a technology follower rather than driver, technologies for increasing the level of integration are generally inherited from microelectronics and mostly suited for the low power range. The second modularization approach can then be applied to utilize these technologies and increase the level of integration. This is illustrated in this thesis by using three low power technologies (ceramic, PCB and lead frame) as the technology platforms for implementing a case study of dc/dc converter for dual power net automotive applications.

The methods for increasing the level of integration can be embodied by means of integration technologies into a design algorithm for physical implementation of power electronic converters with a higher integration level. It is shown in this thesis that the complete design of a power electronic converter can be approached in a more systematic way, including integral design of functions (electrical and thermal) and the continuous interaction between the physical and functional domain. The algorithm for increasing the level of integration is continuously supported with analysis, i.e. design-of-functions modelling and simulation tools. The links between the design-of-functions and design-of-parts are embodied through the electrical, thermal and spatial parameters of parts in one direction and electrical circuit schematic, thermal circuit schematic and spatial modelling in the other direction. These two aspects have to be kept in continuous interaction, since simple analysis of the conceptual design can eliminate an unviable solution.

Evaluating the construction technology based on a number of criteria

Several construction technology options emerge from the process of implementing the design algorithm for increasing the level of integration presented in this thesis. There is a need for a quantitative method for comparing these options to each other in order to find the optimal solution for the particular application. The requirements imposed on power electronic systems in modern applications are multidisciplinary, including electrical performance, thermal behaviour, power density, cost etc. Therefore a method that takes into account all these requirements is needed.

A method for multi-objective evaluation of construction technology based on analytical techniques of decision theory is presented in this thesis. The level of importance of the figures of merit varies from application to application: for example, in military and space applications reliability and performance are the most important, while in low cost consumer applications cost is often the crucial factor. The presented method allows for the industry involvement through the weighting factors derived from the preferences of the decision-maker.

It was shown in the literature that the expressed preferences often show some inconsistency, which will result in weighting factors that do not represent the standpoint of the industry completely and credibly. Also, the predicted criteria values in the design phase might be different from the values of the final product. The sensitivity analysis provides a means for investigating the margin in which the best solution is the best, with respect to the variations in weighting factors and criteria values.

Furthermore, a lot of novel integration concepts have already been presented by the academics and industry. The evaluation method presented in the thesis can be used to evaluate these concepts, given the particular application they are to be used in.

Since standardization is one of the means of reducing the assembly cost through the large volume production, this evaluation method can also assist in the process of arriving at a common technology base for a group of similar applications.

9.2 Recommendations for further research

The recommendations for further work are grouped into three categories: possible research directions concerning increasing the level of integration, recommendations related to the element-based integral design approach and those related to the multi-objective evaluation method.

Increasing the level of integration

In this thesis, an overview of integration technologies is given. This overview could form the initial step in building comprehensive technology libraries with well-defined characteristics of each technology, including characteristics related to both fundamental and packaging functions. This should include electrical, thermal and mechanical properties and could be accomplished in the form of databases similar to those of discrete components manufacturers. This would assist the designer in implementing the presented design algorithm for the implementation of functional and packaging elements by choosing suitable technologies as opposed to the often arbitrary choice of technologies encountered in the present practice.

Furthermore, it might be useful to make a technology survey of technologies emerging in microelectronics and investigate the integration potential of these technologies based on the presented integration methods and the modifications of these technologies that will be required in order for them to be applied in power electronics. This could be useful in pointing the technology movements in power electronics in the right direction.

Establishing common technology platform for power electronic assemblies intended for similar applications and power level would be useful as it would lead to standardization and cost-reduction through large volume production. This could be done by using the inputs from the technology libraries, performing the design algorithm for increasing the level of integration, which will result in a number of construction technology options, and then applying the evaluation method to choose the best option. If this is performed for each cluster of applications, the result will be few technology bases that cover the whole power electronics domain.

In this thesis, two methods of circuit partitioning that exploit the modular approach are presented. The second approach was applied in the design of the case study since it was assumed that the second approach is suited for a cost reduction since it allows for using low power level, low cost technologies. However, in the first approach, each sub-circuit is manufactured in for it the most suitable technology and can be optimized to take full advantage of that technology, which leads to a better electrical and thermal performance. It may be useful to further investigate the benefits and drawbacks of these two modular approaches and possibly find the most suitable applications for each approach.

Concerning the introduced quantities that evaluate the level of FEs and PEs integration, K_I and K_P, some issues have still to be resolved. In this thesis, for calculation of K_P, the number of interconnections made in one process, is considered as one construction part – for e.g. the wire bonds in a power module are counted as one part. Since the large number of interconnections in a sub-assembly is an important issue in reliability and cost, it may be interesting to find a way to include this number in the calculation of K_P. Furthermore, in this thesis a distinction is not made between having two identical components and two different components in the assembly. Since standardization brings a cost reduction, it would be useful to find a way to include this issue in the definition of K_P.

Element-based integral design approach

Design and analysis of electrical circuits rely on well-developed modelling and simulation software based on circuit theory. Thermal design is performed by thermal circuit network modelling of finite element method software packages, electromagnetic design by software for parasitic parameters extraction and circuit theory software and spatial design by means of various 3D CAD software packages. The element-based integral design approach presented in this thesis would benefit significantly from a software tool that allows for the data transfer among these different software packages and the technology libraries for extracting parameters of FEs and PEs.

The presented design algorithm for achieving a higher level of integration was only tested on one case study in this thesis. It would be useful to implement this algorithm on a range of case studies for different applications and use experienced observations to verify and further develop the algorithm. Furthermore, in this thesis, the choice of electrical circuit topology was assumed to be made in the design-of-functions phase and not influenced by the physical implementation. Since some technology platforms are more suited for implementing specific

circuit symbols above others, practical application of this algorithm should allow for the design-of-parts phase to influence the choice of topology.

Multi-objective evaluation method

Concerning the hierarchy tree of objectives, in this thesis the cost criterion was represented by the indirect criteria such as technology maturity, the number of construction parts and level of integration. Since cost is often one of the crucial criteria in deciding whether power electronics is going to be implemented in a new application or not, the evaluation method would benefit from a closer collaboration with industry concerning the cost-related data, both material and overhead costs. Furthermore, since reliability has become a major issue in power electronic assemblies, criteria that represent reliability should be included in the hierarchy tree of objectives.

It was shown that a variety of weighting methods used to extract preferences of decision-makers exist in decision theory. In this thesis, the AHP weighting method is primarily used. An investigation of the impact of different weighting methods on the outcome of the evaluation results at the hand of concrete case studies is recommended.

Since the preferences of decision-makers are often inconsistent and might not fully reflect the reality of the industry standpoint, it is desirable that the evaluation be based on the preferences of a group of decision-makers rather than a single expert in the field. The decision-making software package used in this thesis supports this option.

Appendix A: Criteria values and weighting factors for multiobjective evaluation of case studies

A.1 Introduction

In Chapter 6, the multiobjective evaluation of two groups of case studies was presented: off-line PCB power supplies and power modules. Each case study is implemented in two construction technologies, the conventional technology and more advanced integrated option.

In this appendix, the procedures for obtaining the values of the criteria for both case studies and for deriving the weighting factors based on the preferences of the experts in the field are presented in Section A.2 and Section A.3, respectively.

A.2 Criteria values

A.2.1. PCB power supplies

Maturity

The estimation of the technology maturity is chosen to be 1 for the conventional construction, as this technology has been used in industry for decades, while the EmPIC technology is fairly new and capacitive and magnetic laminates are still in the development phase. The used value for EmPIC technology should not be treated as absolute and hence the sensitivity analysis based on this criteria will be presented later on in this appendix.

Number of parts

The number of parts in the conventional option is 80, out of which the number of functional elements is N_{FE} = 25 and number of packaging elements N_{PE} = 55. The number of parts in the EmPIC solution is 59, out of which the number of functional elements is N_{FE} = 11 and number of packaging elements N_{PE} = 48.

Integration level

The number of virtual functional elements in the conventional option is N_{FEv} = 25, which according to the equation (4.1) gives the level of functional elements integration K_I = 1. The number of virtual functional elements in the EmPIC solution is N_{FEv} = 25, which according to the equation (4.1) gives the level of functional elements integration K_I = 2.27.

The number of virtual packaging elements in the conventional option is N_{PEv} = 85, which according to the equation (4.2) gives the level of packaging elements integration K_P = 1.49.

The number of virtual packaging elements in the EmPIC solution is N_{FEv} = 76, which according to the equation (4.2) gives the level of packaging elements integration K_P = 1.58.

Electrical efficiency

The electrical efficiency of the EmPIC solution was measured and presented in [Neu04]. Furthermore, the breakdown of the estimated values of the losses in all the components is given in this reference. Assuming that the losses in the rest of the FEs are the same in both converters, the electrical efficiency of the conventional solution was derived by subtracting the estimated losses in the magnetic laminates (6 W) and windings (5 W) in the EmPIC converter from the total losses and adding the estimated losses (1.5 W) in the discrete transformer. The losses in the capacitive laminates are estimated to be low comparable to the magnetic laminates and hence were not included in the calculation of the efficiency of the conventional converter.

Power density

The rated power of both converters is the same P_{rated} = 60 W. The volume of the conventional solution is 87 cm^3 which gives the power density value of 11.2 W/in^3. The volume of the EmPIC solution is 28.6 cm^3 which results in the power density of 34.4 W/in^3.

Thermal density

The surface area of the EmPIC converter is 44 cm^2 which gives the thermal density value of 0.12 W/cm^2. The surface area of the conventional converter is estimated by adding the surface area of the discrete transformer and inductor to the surface area of the EmPIC converter and the obtained value is 48 cm^2. This is only an approximation since this value in the real converter would be different, due to a different layout and discrete instead of integrated capacitors. This results in the thermal density value of 0.34 W/cm^2.

Volumetric packaging effectiveness

The volume of the functional elements in the EmPIC solution is estimated based on the list of components that is presented in [Neu04]. The obtained value is 9.8 cm^3 which results in the value of η_v = 34.2 %. The volume of the functional elements in the conventional solution is estimated based on the EmPIC functional elements volume and modified to account for the discrete inductor and transformer. The obtained value is 3.2 cm^3 which results in the value of η_v = 3.61 %.

A.2.2. Power modules

Technology maturity

The criteria values for the technology maturity criteria are chosen somewhat arbitrarily, as in the case of the PCB power supplies case study. It is assumed that the construction technology of the SEMITRANS module is mature since it has been utilized for a few decades. The pressure technology is newer but extensive testing has been performed by [Sem] and the value assigned is 0.7, which is higher than the value for the EmPIC technology compared to the conventional PCB technology.

Number of parts

The number of parts in the SEMITRANS module is 30, where the number of functional elements is N_{FE} = 18 (12 IGBTs and 6 diodes) and packaging elements N_{PE} = 12. The calculation only takes into account the power module itself, not the external interconnection means (bus bars, etc.) The number of parts in the MiniSKiiP module is 25, out of which the number of functional elements is N_{FE} = 18 and number of packaging elements N_{PE} = 7.

Integration level

The functional elements integration level in both SEMITRANS and MiniSKiiP module is K_I = 1, if the sub-circuit schematic in Figure 6-12 is modified to consist of two IGBTs circuit symbols in parallel for each IGBT in each phase arms. If it is considered that it consist of only one, then effectively two IGBTs implement one circuit symbol which means that the number of virtual functional elements is N_{FEv}=12 which gives the level of functional elements integration K_I = 0.67.

The number of virtual packaging elements in the SEMITRANS module is N_{PEv} = 16, which according to the equation (4.2) gives the level of packaging elements integration K_P = 1.33. The number of virtual packaging elements in the MiniSKiiP module is N_{FEv} = 12, which according to the equation (4.2) gives the level of packaging elements integration K_P = 1.71.

Power density

The rated power of both power modules is the same P_{rated} = 90 kW. The base plate area of the SEMITRANS module is 47.3 cm^2, which gives the power density value of 19.1 W/mm^2 (as defined in Section 6.3.1, for power modules). The volume of the MiniSKiiP module is 30.1 cm^2, which results in the power density of 29.1 W/mm^2.

Volumetric packaging effectiveness

The estimated value of the functional elements in the SEMITRANS module and MiniSKiiP module is the same, 153 mm^3. The volume of the SEMITRANS module is $V_{SEMITRANS}$ = 113.4 cm^3 which results in the volumetric packaging effectiveness value of $\eta_{v\_SEMITRANS}$ = 0.14 %. The volume of the MiniSKiiP module is $V_{MiniSKiiP}$ = 71.4 cm^3 which results in the value of $\eta_{v\_MiniSKiiP}$ = 0.21 %.

Thermal resistance

The thermal resistance values are taken from the manufacturer's data sheets of the modules.

A.3 Weighting factors

A.3.1. PCB power supplies

Decision maker's preferences

The preferences of the decision maker are obtained through the following questions and expressed in the following answers:

1. Which criteria is more important: cost or performance? How many times (scale 1 to 9) where 1 is equally preferred, 3 slightly preferred, 5 strongly preferred, 7 very strongly preferred and 9 extremely preferred?
On a scale of 1 to 9: 8 for cost and 5 for performance.

2. Which criteria is more important manufacturing or assembling costs? How many times?
Manufacturing and assembling costs can't be split up since we buy all materials (components, PCB, etc.) and assemble them together.

3. Electrical or thermal performance? How many times?
Electrical performance is more important. 9 times.

4. Thermal or spatial performance? How many times?
Spatial performance is more important. 7 times.

5. Electrical or spatial performance? How many times?
Electrical performance is more important. 9 times.

6. Efficiency or power density? How many times?
Efficiency is more important. 6 times.

Extracting weighting factors

Looking at the above expressed preferences, a few points can be noticed. Firstly, it can be seen that not all the criteria from the hierarchy tree are dealt with. One of the reasons is that the criteria such as integration level and volumetric packaging efficiency are new and not yet widely used by industry. For these criteria, the author's opinion was used. Secondly, for the preferences concerning manufacturing and assembling costs, the decision maker could not express the preference since the cost data that this industry handles is normally in the cost of discrete components and assembly rather than the cost of parts manufacturing and assembling. Hence, for this breakdown, the author's preferences were also used.

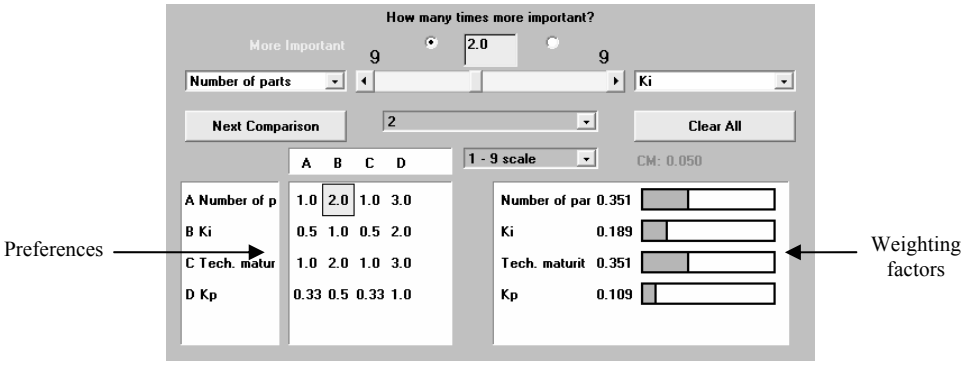

Figure A-1 Weighting factors for manufacturing and assembling cost criteria for PCB power supplies

It can also be noticed that there is inconsistency between the preferences regarding the electrical, thermal and spatial performance. The electrical performance is valued to be 9 times more important than both spatial and thermal performance, while the spatial performance is

valued to be 7 times more important than the thermal performance. From the first two preferences would be expected that thermal and spatial performance are equally preferred. The preferences were modified to compensate for this inconsistency. The electrical performance is kept to be 9 times more important than the thermal performance and 6 times more important than the spatial performance, while the spatial performance is 3 times more important than the thermal performance.

Figure A-1 shows the author's preferences concerning the manufacturing and assembly cost breakdown that lead to the weighting factors.

A.3.2. Power modules

The preferences of the decision maker are obtained through the following questions and expressed in the following answers:

1. Which criteria is more important: cost or performance? How many times (scale 1 to 9)?
Cost and performance are equally preferred (performance is not even discussed ever more)

2. Which criteria is more important manufacturing or assembling costs? How many times?
Assembling cost preferred (3)

3. Number of construction parts or technology maturity (scale 1 to 9)?
Technology maturity is preferred (7)

4. Electrical or thermal performance? How many times (scale 1 to 9)?
No difference (1)

5. Thermal or spatial performance? How many times (scale 1 to 9)?
Thermal performance (5)

6. Electrical or spatial performance? How many times (scale 1 to 9)?
Electrical performance (5)

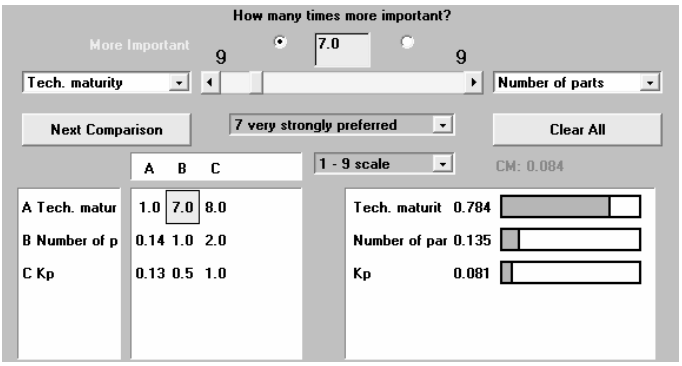

Figure A-2 Weighting factors for manufacturing and assembling cost criteria for power modules

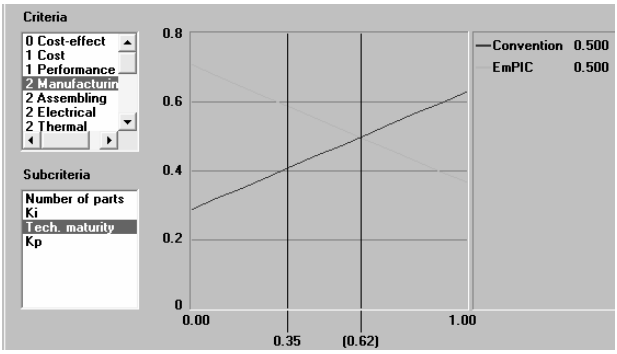

Figure A-3 Weighting factor for technology maturity criteria – sensitivity analysis

The same reasoning as discussed in the case of PCB power supplies concerning the non-conventional FOMs applies here. For the K_P, and η_v criteria, the author's preferences are used to derive the weighting factors.

Figure A-2 shows the author's preferences concerning the manufacturing and assembly cost breakdown that lead to the weighting factors.

A.4 Sensitivity analysis

A.4.1. PCB power supplies

The sensitivity analysis related to the weighting factor of the efficiency criteria in the electrical performance breakdown was presented in Section 6.7.1.

Figure A-3 shows the influence of the technology maturity weighting factor in the manufacturing criteria breakdown on the evaluation result. It can be seen that if this weighting factor is higher than 0.62, the conventional approach becomes more preferred. However, if the technology maturity criteria value of the EmPIC technology changes anywhere between 0.5 and 1, the EmPIC converter will still be preferred. The result is less sensitive on variations in all other weighting factors and criteria values.

A.4.2. Power modules

The sensitivity analysis related to the weighting factors of the cost-performance breakdown was presented in Section 6.7.2. The result is less sensitive on variations in other weighting factors and criteria values.

A.5 References

[Neu04] *Aufbau eines Schaltnetzteils mit passiven integrierten Komponenten für einen Flachmonitor*" T. Neubert, Diplomarbeit, RWTH-ISEA Aachen, 2004.

[Sem] Semikron International, www.semikron.com.

Appendix B: Design and experimental evaluation of the building blocks

B.1 Introduction

In Chapter 7, three dc-dc 42 V/ 14 V building blocks were designed in an integral manner, linking the function design and physical implementation. These three building blocks were also compared to each other, using the evaluation method presented in Chapter 6.

In this appendix, the procedures used in the design, including losses calculations, inductance calculations etc. are given. Furthermore, the criteria values, weighting factors and sensitivity analysis for the evaluation method are presented.

B.2 Building blocks design and loss estimations

In this section, some design issues and losses calculations for all the three building blocks will be presented. Firstly, the losses in MOSFETs will be presented followed by the design and losses calculations in the three building blocks.

B.2.1. MOSFET losses

There are three main categories in the total losses in the MOSFETs: Q_1 and Q_2 switching losses, conduction losses and body diode losses [Mit97][Fai].

Switching losses

As the body diode of Q_2 is conducting before Q_2 switches on and off, this MOSFET operates in zero voltage switching mode and its switching losses can be neglected. The switching losses in the high side MOSFET (Q_1) consist of turn-on and turn-off losses.

Turn-off losses: The turn-off time of Q_1 can be split up into two intervals (Figure B-4): the voltage rise time and current fall time. These intervals are given by the following expressions [Moh01][Mit97][Fai]:

$$t_{rv} = \frac{Q_{gd}}{I_{driver(H-L)}} \tag{B.1}$$

and

$$t_{fi} = (R_{dr\_pulldown} + R_{gate}) \cdot C_{iss} \cdot \ln(\frac{V_{GG} - V_{th}}{V_{GG} - V_{plt}}) \tag{B.2}$$

where $I_{driver(H-L)} = \dfrac{V_{GG} - V_{plt}}{R_{dr\_pulldown} + R_{gate}}$

$R_{dr\text{-}pulldown}$ is the internal resistance of the gate driver at turn-off extracted from the integrated gate drive's data sheet
R_{gate} is the resistance in series with the gate
C_{iss} is the MOSFETs input capacitance
V_{GG}, V_{th}, V_{plt} are the gate drive voltage, MOSFET's threshold voltage and plateau voltage respectively
Q_{gd} is the gate drain charge from the MOSFET's data sheet
and $I_{driver(H-L)}$ is the gate drive current at turn-off

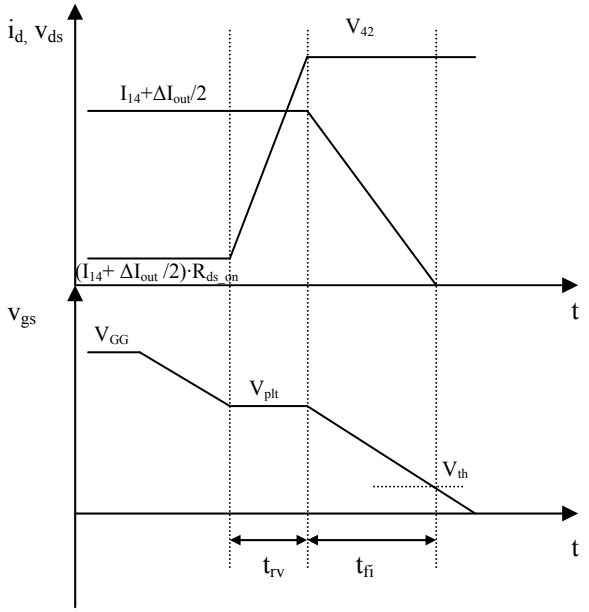

Figure B-4 Turn-off switching waveforms of Q_1

The total turn-off switching losses in Q_1 are given by:

$$P_{sw\_Q_1(off)} = \frac{V_{42} \cdot (I_{14} + \dfrac{\Delta I_{out}}{2}) \cdot (t_{rv} + t_{fi}) \cdot f_s}{2} \tag{B.3}$$

where V_{42} is the input voltage
I_{14} mean value of the inductor current,
ΔI_{out} is the peak-to-peak value of the inductor current ripple
f_s is the switching frequency
and t_{fi} is current fall time and t_{rv} voltage rise time

Turn-on losses: The turn-on time of Q_1 can be split up into three intervals as shown (Figure B-5): the current rise time, reverse recovery time and voltage fall time. These intervals are given by the following expressions:

$$t_{ri} = (R_{dr\_pullup} + R_{gate}) \cdot C_{iss} \cdot \ln(\frac{V_{GG} - V_{th}}{V_{GG} - V_{plt}}) \quad \text{(B.4)}$$

$$t_{fv} = \frac{Q_{gd}}{I_{driver(L-H)}} \quad \text{(B.5)}$$

$$t_{rr} = 2.8 \cdot 10^{-6} \cdot BV_{BD} \sqrt{\frac{I_{14} - \frac{\Delta I_{out}}{2}}{di/dt}} \quad \text{(B.6)}$$

where $I_{driver(L-H)} = \dfrac{V_{GG} - V_{plt}}{R_{dr\_pullup} + R_{gate}}$

$$di/dt = \frac{I_{14} - \frac{\Delta I_{out}}{2}}{t_{ri}}$$

and $R_{dr\text{-}pullup}$ is the internal resistance of the gate driver at turn-off extracted from the integrated gate drive's data sheet.

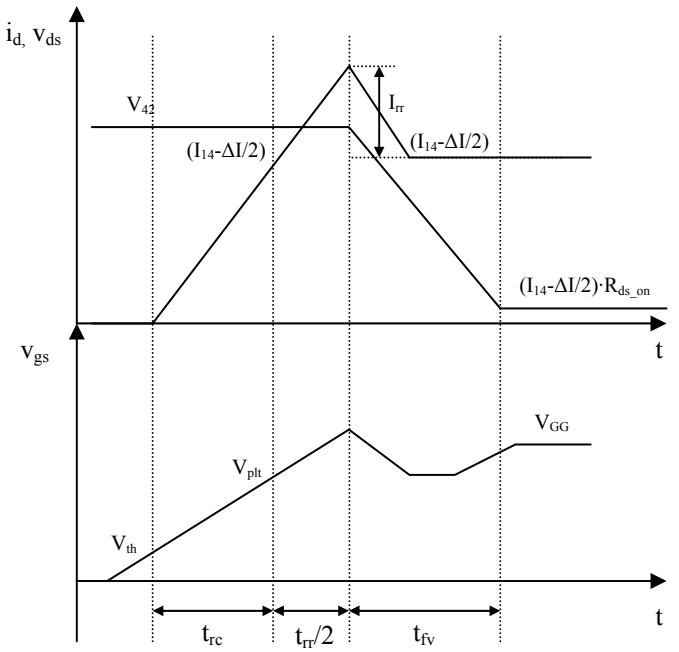

Figure B-5 Turn-on switching waveforms of Q_1

The total turn-off switching losses in Q_1 are given by:

$$P_{sw\_Q_1(on)} = \frac{V_{42} \cdot (I_{14} - \frac{I_{ripple}}{2}) \cdot (t_{ri} + t_{vi}) \cdot f_s}{2} + \frac{V_{42} \cdot t_{rr} \cdot f_s}{2} [(I_{14} - \frac{I_{ripple}}{2}) + \frac{I_{rr}}{2}] \quad \text{(B.7)}$$

Conduction losses

The conduction losses in both MOSFETs are given in the following equations:

$$P_{cond\_Q_1} = I_{14}^2 \cdot R_{ds\_on} \cdot D \tag{B.8}$$

$$P_{cond\_Q_2} = I_{14}^2 \cdot R_{ds\_on} \cdot (1-D) \tag{B.9}$$

where R_{ds_on} is the MOSFETs on resistance
and D is the duty cycle of the high side MOSFET.

Body diode losses

The losses in the body diode consist of the reverse recovery losses and diode conduction losses. The body diode conducts during the transition periods of the MOSFETs Q_1 and Q_2 in order to prevent both of them conducting at the same time. Both losses components are given in the following equations:

$$P_{rr} = \frac{1}{2} Q_{rr} \cdot V_{42} \cdot f_s \tag{B.10}$$

$$P_{con\_diode} = I_{14} \cdot V_{fw} \cdot t_{con} \cdot f_s \tag{B.11}$$

where Q_{rr} is the reverse recovery charge
and t_{cond} is the diode's conduction time.

B.2.2. Heat Conductor Converter design

Optimization procedure

As presented in Chapter 7, the inductor core size (only commercially available planar E-I combinations are considered) is chosen first. The width of the converter is primarily determined by the core size. The initial value of the current density in the conductors is chosen. This, together with the winding window size determines the number of turns in the part of the winding that is implemented in the ceramic metallization. The maximum number of turns is the number of turns in the ceramic metallization plus one turn of the electro-thermal bus bar:

$$n_{\max}(core) = \frac{k_w \cdot w(core)}{d_w} + 1 \tag{B.12}$$

where k_w is the winding window utilization factor
w is the width of the core's winding window
and d_w is the conductor width

The switching frequency is chosen based on the design criteria of energy requirement in the inductor (Figure B-6) [Moh01]:

$$L \cdot I_{\max} = N \cdot B_{\max} \cdot A_c \tag{B.13}$$

$$C_{input}(f, I_{ripple}) = L(f, I_{ripple}) \cdot I_{\max}(I_{ripple}) \cdot I_{rms} \tag{B.14}$$

$$C_{core}(ferrite, core) = B_{\max}(ferrite) \cdot A_c(core) \cdot [(k_w \cdot w(core) \cdot t_{con} \cdot J_{rms}) + I_{rms}] \tag{B.15}$$

where I_{max} is the maximum value of the inductor current
B_{max} is the maximum value of flux density in the core
A_c is the core cross section
I_{rms} is the rms value of the inductor current
J_{rms} is the rms value of the current density
and t_{con} is the conductor thickness.

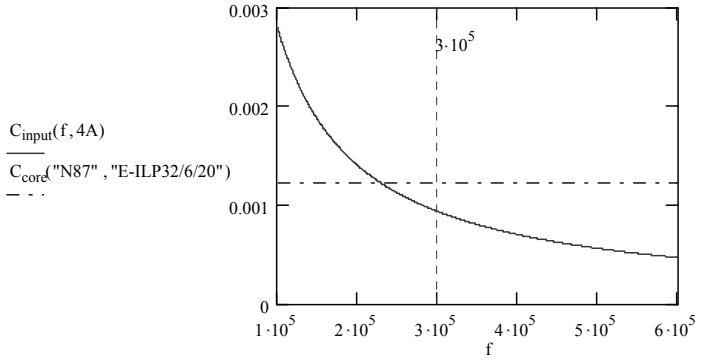

Figure B-6 Energy requirement for the inductor design

MOSFET losses

Based on the model presented in Section B.2.1, the obtained values for the MOSFET losses are P_{Q1} = 10.01 W and P_{Q2} = 2.38 W.

Capacitor losses

The RMS currents in the capacitors C_{14} and C_{42} are calculated according to the following expressions [Ger03]:

$$I_{C14rms}(\Delta I_{out}) = \frac{\Delta I_{out}}{\sqrt{3}} \tag{B.16}$$

$$I_{C42rms}(\Delta I_{out}) = \sqrt{\frac{D}{3}\cdot[(I_{14}-\frac{\Delta I_{out}}{2}-I_{42})^2+(I_{14}-\frac{\Delta I_{out}}{2}-I_{42})\cdot(I_{14}+\frac{\Delta I_{out}}{2}-I_{42})+(I_{14}+\frac{\Delta I_{out}}{2}-I_{42})^2]+(1-D)\cdot I_{42}^2} \tag{B.17}$$

and the expression for the losses in the capacitors is given by:

$$P_{C14}(\Delta I_{out}) = (I_{C14rms}(\Delta I_{out}))^2 \cdot ESR \tag{B.18}$$

$$P_{C42}(\Delta I_{out}) = (I_{C42rms}(\Delta I_{out}))^2 \cdot ESR \tag{B.19}$$

where ESR is the equivalent series resistance of the capacitor, obtained by measurements.

According to the above expressions, the losses in the capacitors are P_{C14} = 0.1 W and P_{C42} = 0.43 W.

Inductor losses

The dc losses in the part of the inductor winding implemented in the ceramic metallization are 1.68 W and in the bus bar 0.01 W, which gives the total dc losses in the inductor P_{dc} = 1.69 W. The eddy current losses in the inductor, obtained through an FEM simulation, are P_{ac} = 0.07 W. Based on the core ac excitation (B_{ac} = 80 mT) and the N87 material properties taken from the data sheet, the core losses are estimated to be P_{core} = 0.32 W.

The total losses in the converter are obtained by adding up the losses in all the FEs. The obtained value is P_{tot} = 14.99 W which gives the efficiency of 90.4%.

B.2.3. PCB Embedded Converter design

Integrated capacitances and discrete inductor vs. discrete capacitances and integrated inductor

As shown in Section 7.4.3 in Chapter 7, the capacitance value that can be achieved by means of capacitive laminates is approximately C_{14} = 35 nF. It was also shown in this section that in order to satisfy the peak-to-peak output voltage ripple requirements ΔV_{out} given by the expression:

$$L = \frac{V_{out} \cdot (1 - D)}{8 \cdot f_s^{\,2} \cdot C_{14} \cdot \Delta V_{out}} \tag{B.20}$$

the minimum inductance value needed at 300 kHz is 1.2 mH.

According to the inductor design energy equation [Moh01]:

$$L \cdot I_{\max} \cdot I_{rms} = k_{Cu} \cdot J_{rms} \cdot B_{\max} \cdot A_w \cdot A_{core} \tag{B.21}$$

the smallest commercially available core size that satisfies the above expression is E65/32/27. The volume of this core is 78.6 cm^3.

If the inductor is integrated, the values that can be achieved are obtained by means of FEM simulation and are in the region of 5 μH, which according to the expression for the output voltage ripple:

$$\Delta V_{out} = \sqrt{\left(\frac{\Delta I_{out}}{8 \cdot f_s \cdot C_{14}}\right)^2 + \left(\Delta I_{out} \cdot ESR(C_{14})\right)^2} \tag{B.22}$$

results in the needed output capacitance of C_{14} > 30 μF. If a volumetric capacitance density value of 3.9 μF/cm^3 is taken (derived from the metal film capacitors commercially available by [Epc], the volume needed for implementing this capacitance is 7.6 cm^3.

MOSFET losses

Based on the model presented in Section B.2.1, the obtained values for the MOSFET losses are P_{Q1} = 9.42 W and P_{Q2} = 2.38 W.

Capacitor losses

Using the expressions (B.16) to (B.19), the losses in C_{14} and C_{42} are calculated. The obtained values are P_{C14} = 0.31 W and P_{C42} = 0.45 W.

Inductor losses

The calculated value for the dc resistance of the inductor winding is 40 mΩ which gives the dc losses value of P_{ind_dc} = 4.1 W. The ac losses were estimated by means of FEM simulation and the obtained values is P_{ind_ac} = 0.27 W and the core losses are calculated by means of the following expressions [Epc]:

$$R_m(f) = L \cdot 2 \cdot \pi \cdot f \cdot \tan\delta \tag{B.23}$$

$$P_{core} = \sum_i R_m(i \cdot f_s) \cdot I_{amp}{}^2(i \cdot f_s) \tag{B.24}$$

where $\tan(\delta)$ is the loss factor of the magnetic material,
R_m is the magnetic resistance
and $I_{amp}(i{\cdot}f)$ amplitude of the i^{th} harmonic of the inductor current.
The obtained value for the core losses is P_{core} = 0.71 W.

The total losses in the converter are obtained by adding up the losses in all the FEs. The obtained value is P_{tot} = 17.62 W which results in the converter efficiency of 88.8%.

B.2.4. Lead Frame Converter design

Air core inductance calculation

The inductance value of a square air core inductor (as shown in Figure B-7) is calculated according to the following expression [Moh99]:

$$L_{air}(N, d_{in}) = K_1 \cdot \mu_0 \cdot \frac{N^2 \cdot \frac{d_{in} + d_{out}}{2}}{1 + K_2 \cdot \frac{d_{out} - d_{in}}{d_{out} + d_{in}}} \tag{B.25}$$

where K_1 and K_2 are constants referred to as Wheeler's constants
N is the number of turns
and d_{in} and d_{out} are the inner and outer diameter of the inductor
Wheeler's constants are dependent on the layout, i.e. whether the inductor is square, hexagonal or octagonal. For a square inductor, these values are K_1 = 2.34 and K_2 = 2.75. The inner and outer diameter of the inductor d_{in} and d_{out} are linked by the following expression:

$$d_{out} = d_{in} + 2 \cdot N \cdot d_w + 2 \cdot (N - 1) \cdot s_w \tag{B.26}$$

where d_w and s_w are the conductor width and gap between conductors respectively.

Converter losses

MOSFET losses: Based on the model presented in Section B.2.1, the obtained values for the MOSFET losses are P_{Q1} = 9.69 W and P_{Q2} = 2.38 W.

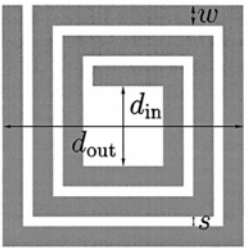

Figure B-7 Geometry of a square air core inductor

Inductor losses: The dc resistance of the inductor winding is 13.4 mΩ which results in the dc losses value of 1.34 W. The ac losses in the inductor are calculated by means of FEM simulations and the obtained value is 1.2 W.

Capacitor losses: Using the expressions (B.16) to (B.19), the losses in C_{14} and C_{42} are calculated. The obtained values are P_{C14} = 0.2 W and P_{C42} = 0.44 W.

The total losses in the converter are obtained by adding up the losses in all the FEs. The obtained value is P_{tot} = 16 W which results in the converter efficiency of 89.7%.

B.3 Evaluation

In this section, the calculations of the criteria values for each building block will be shown. The preferences used for extracting the weighting factors are also given. Finally, the rest of the results of the sensitivity analysis that were not presented in Chapter 7 will be given here.

B.3.1. Criteria values

Technology maturity

The estimation of the technology maturity criteria value is 1 for the conventional construction, as this technology has been used in industry for decades, 0.7 for the Heat Conductor Converter since it uses mature thick film technology while issues such as gluing the thermal bus bar, attaching the converter to the heat sink by means of an adhesive tape, the electrical interconnections between bus bars and ceramic etc. have to be tackled yet. The Lead Frame Converter and PCB Embedded Converter were assigned a somewhat lower value (0.6) due to the use of novel magnetic materials in both converters. The used values should not be treated as absolute and hence a sensitivity analysis based on this criteria will be presented later in this appendix.

Number of parts and integration level

Table B-1 shows the number of FEs and PEs, number of virtual FEs and PEs, total number of parts and FE and PE integration level values for the three building blocks and benchmark converter.

Table B-1 Number of parts and integration level of building blocks

	N_{FE}	N_{FEv}	N_{PE}	N_{PEv}	N_{total}	K_I	K_P
Benchmark	9	9	33	38	42	1	1.15
HCC	6	7	19	29	25	1.17	1.53
LF	5	7	5	10	10	1.4	2
PCB embedded	5	10	13	24	18	2	1.85

Power density

The dimensions of the Heat Conductor Converter are estimated based on the spatial design. The width of the converter is determined by the core width, the length of the converter by the inductor length increased by the estimated area for the control circuit and MOSFETs and the thickness is the sum of the thicknesses of the ceramic substrate, magnetic core, electro-thermal bus bar and PCC capacitor. The obtained values are 85 mm X 31.75 mm X 11.25 mm which results in the power density value of 75.6 W/in^3.

The dimensions of the PCB converter are estimated based on the inductor dimensions increased by the estimated area for the control circuit and MOSFETs. The obtained values are of the PCB embedded converter are 90 mm X 36 mm X 8.5 mm. This gives the power density value of 83.3 W/in^3.

The length and width of the Lead Frame Converter are determined by the inductor dimensions increased for the thickness of the electrical interconnection bus bars. The height is obtained as the sum of the thicknesses of the lead frame, moulded ferrite and PCC capacitor. The obtained values are 58 mm X 58 mm X 9 mm which gives the power density value of 75.8 W/in^3.

The volume of the discrete converter is 235 cm^3 which results in the power density value of 9.7 W/in^3.

Volumetric packaging effectiveness

The volume in the discrete benchmark converter taken up by the FEs is 23 cm^3 which results in the volumetric packaging effectiveness value of 10%.

The FEs volume in the Heat Conductor Converter is 13.9 cm^3 which gives the volumetric packaging effectiveness of 45.9%.

The volume in the PCB Embedded Converter taken up by the FEs is 21.3 cm^3 which gives the volumetric packaging effectiveness value of 44.8%.

The volume in the Lead Frame Converter taken up by the FEs is 13.5 cm^3 which gives the volumetric packaging effectiveness value of 44.5%.

Thermal density

Using the converter losses values from the Section B.2 and the heat exchange surface area for each converter (in the case of the Heat Conductor Converter that is the surface area of the thermal bus bar that is mounted onto the heat sink while in the case of the PCB Embedded Converter and Lead Frame Converter these are the surfaces areas of the converters) the thermal density values of: 5.88 W/cm^2 for the Heat Conductor Converter, 0.54 W/cm^2 for the PCB Embedded Converter and 0.48 W/cm^2 for the Lead Frame Converter.

B.3.2. Preferences for weighting factors

The following preferences reflect the opinion of the author and colleagues, not an official standpoint of automotive industry.

Criteria level 1

1. Which criteria is more important: cost or performance? How many times (on scale 1 to 9)?
Cost preferred (2)

Criteria level 2

2. Manufacturing or assembling costs?
Assembling cost preferred (2)

4. Electrical or thermal performance?
No difference (1)

5. Thermal or spatial performance?
Spatial performance (2)

6. Electrical or spatial performance?
Spatial performance (2)

Criteria level 3 (Manufacturing and Assembling)

7. Number of parts or K_I?
Number of parts (2)

8. Number of parts or K_P?
Number of parts (2)

9. Number of parts or technology maturity?
Number of parts (4)

10. K_I or technology maturity?
K_I (2)

11. K_P or technology maturity?
K_p (2)

12. K_I or K_P?
Equal

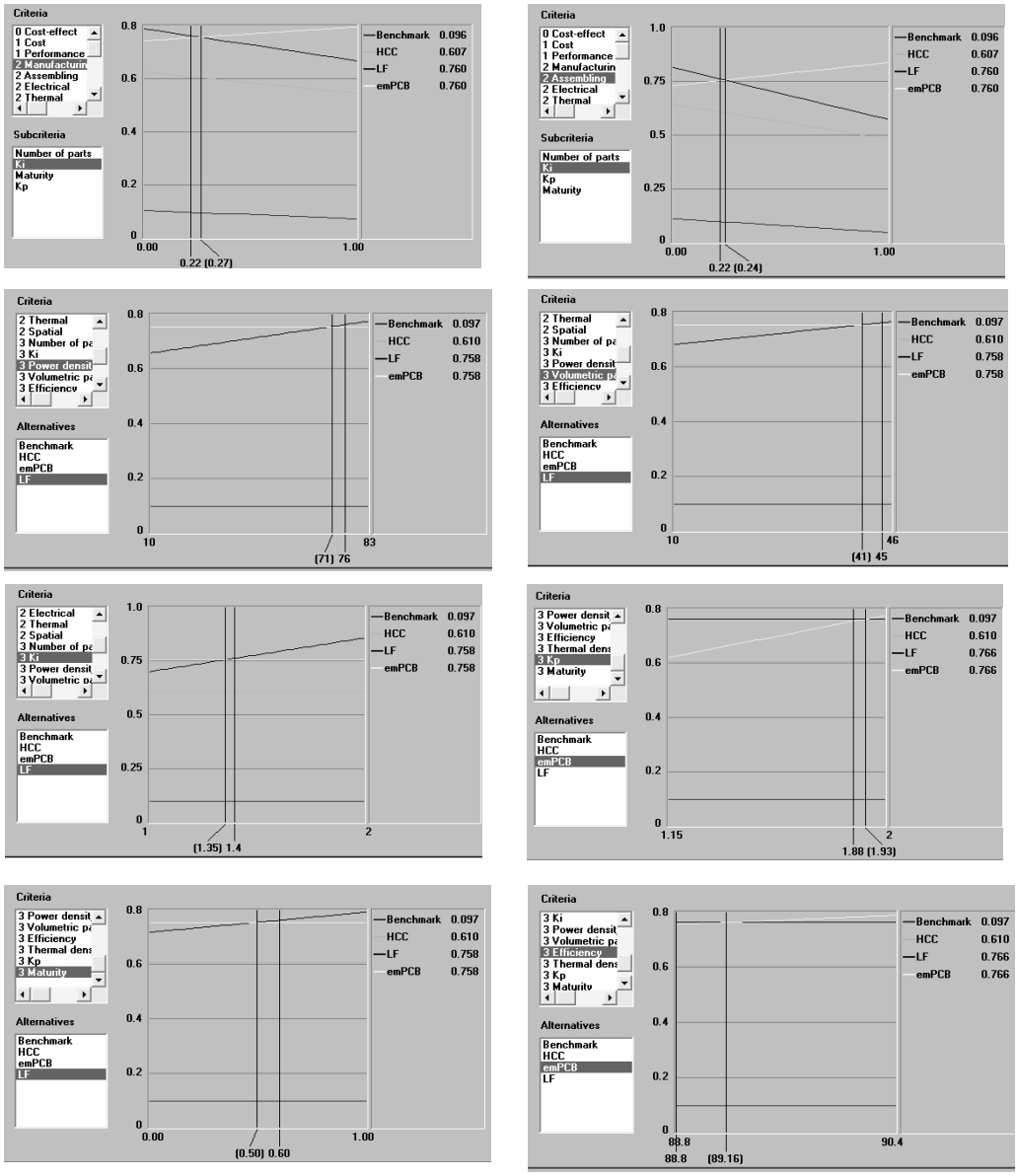

Figure B-8 Sensitivity analysis - results

Criteria level 3 (Electrical performance)

13. K_I or electrical efficiency?
Electrical efficiency (4)

14. K_I or power density?
Power density (4)

15. K_I or K_P?
Equal

16. Power density or electrical efficiency?
Equal

17. K_P or electrical efficiency?
Electrical efficiency (4)

18. K_P or power density?
Power density (4)

Criteria level 3 (Spatial performance)
19. Volumetric packaging effectiveness or power density?
Equal

By inserting these preferences in the Web-Hipre model, the weighting factors are derived and presented in Chapter 7.

B.3.3. Sensitivity analysis

As presented in Chapter 7, the Lead frame converter has the highest value of the construction technology value function. However, this chapter also presented the results of the sensitivity analysis, that show that for small variations of the weighting factors and criteria values (the outcome of the evaluation process will be changed.

Figure B-8 shows the rest of the sensitivity analysis results. It can be seen that for small variations in the weighting factors of FE integration level and criteria values of power density, volumetric packaging effectiveness, FE and PE integration level, electrical efficiency and technology maturity, the evaluation result will be different.

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Summary

Improving packaging and increasing the level of integration in power electronics

PhD thesis
by Jelena Popović

The use of power electronics is growing extensively in applications such as the automotive field, lighting, power supplies, motor drives, etc. The ultimate goal is to make power electronics as transparent to the final user as possible, which means little extra cost, use of existing space and little or no extra thermal management. This sets very stringent requirements on power electronics concerning performance, cost and size. It has been recognized that the physical construction of power electronic converters represents one of the main frontiers in fulfilling these ever-increasing requirements. This thesis deals with improving the physical implementation of power electronic converters by increasing the level of integration through the use of multifunctional parts.

Analysis of the present practice of constructing power electronic converters

In order to develop a better approach to the construction of power electronic converters, one of the objectives of the thesis is to analyze the present construction technology and identify the main drawbacks.

To date, power electronic converters are mainly constructed as assemblies of discrete components. Each component consists of a number of construction parts. Besides the electrical part, each component is provided with parts for electrical interconnection, protection and thermal management. Furthermore, the converter assembly includes parts for electrical interconnection of the components, their mechanical support and assembly protection. If all converter parts are added up, one can end up with a total number of parts that could be five or ten times more than the number of components in the circuit assembly. This practice does not comply with the Design for Manufacture and Assembly (DFMA) principles of good design that take into account manufacturing and assembly issues. All of these parts have to be manufactured and assembled, and this makes the cost and size of converters large. In this thesis, the origins of the large number of construction parts and manufacturing processes in converters are identified and some prospects and bottlenecks that prevent power electronics from achieving a breakthrough similar to that achieved in information processing due to monolithic silicon integration technology are considered.

Systematic approach to construction technology of power electronic converters, including integration and packaging

Physical construction of power electronic converters is a multidisciplinary technology and involves material technology, layout technology, interconnection technology, component technology etc. All these issues that are not part of conventional electrical design are often being referred to as packaging. On the other side, packaging is sometimes restricted to the packaging of semiconductor components, which is inherited from microelectronics and not suitable in power electronics, given that passive components represent a significant part of a typical converter. Other terms related to physical construction, such as integration, are also loosely used, and their meanings exhibit a lack of preciseness and general applicability.

One of the objectives of this thesis is to approach the construction technology of power electronic converters in a systematic way and to introduce terminology that will enable improvements in this field and ease communication of ideas and concepts among power electronics engineers. In order to improve the construction of power electronic converters, this thesis looks deeper than discrete components that power electronic converters are generally assembled with. A power electronic converter is stripped down to its basic construction parts on the basis of the functions that these parts perform. The number of construction parts in the converter can be reduced by integrating the functionality of several parts into one. This includes not only electrical (functional) parts but also non-electrical (packaging) parts, since packaging parts represent a large portion of the total number of parts in the converter assembly.

Increasing the level of integration by increasing the functionality of converter functional and packaging elements

The central part of the thesis deals with the ways of increasing the level of functionality of construction parts. Two quantities that evaluate the level of integration in power electronics are introduced: functional elements integration level (K_I) and packaging elements integration level (K_P). These quantities represent the average functionality of functional elements and packaging elements, respectively.

Formal methods to assist the power electronic designer in increasing the level of functional and packaging elements integration are devised in the thesis. Furthermore, a comprehensive overview of integration technologies that can be used to implement these methods in actual converters is given. The integration methods and technologies are merged into an algorithm that maps the design of fundamental functions (electrical and thermal) onto the design of physical parts. The algorithm is placed into the design process as the whole, which is intended to make the physical implementation of converters more systematic than it is at present. Another important advantage of this algorithm, compared to the conventional design practice, is that the domain of simulations and modelling and the physical domain are continuously interacted through the whole design process, which allows for an optimal physical implementation of converters.

This design process is implemented in a case study of a dc-dc 42V/14V converter for dual power net automotive applications. The design process results in three technology

demonstrators which are based on the Printed Circuit Board, thick film ceramic and lead frame technology platforms.

Evaluating the construction technology according to a number of criteria

Since power electronic converters of the future will have to meet a number of criteria simultaneously (cost, power density, electrical and thermal performance), it is important to be able to compare different construction technology options based on all the important criteria in order to choose the optimal option for a particular application. Many concepts and technologies are emerging in both the industry and academic field – hence there is a need for a means that allows for comparing these concepts among each other.

Therefore, the last objective of this thesis is to develop a tool to evaluate different construction technology options, devised in the introduced design algorithm, in order to choose the optimal solution. The evaluation criteria for each option are calculated and weighted on the basis of the preferences of decision makers which allows for the industry involvement in the early stage of the design. Furthermore, such a method could assist in standardizing the technology base for power electronic converters in the same power range and for similar applications.

Samenvatting

Het verbeteren van de *packaging* en het verhogen van het niveau van integratie van vermogenselektronica

Proefschrift
van Jelena Popović

Het gebruik van vermogenselektronica in auto's, verlichting, voedingen, motoraandrijvingen, etc., groeit sterk. Het ultieme doel is om vermogenselektronica onzichtbaar te maken voor de eindgebruiker. Dit betekent weinig extra kosten, gebruik maken van de bestaande ruimte en weinig tot geen extra warmtebehandeling. Dit stelt aan de vermogenselektronica zeer strenge eisen met betrekking tot de prestatie, de kosten en de afmetingen. Het bouwproces van de vermogenselektronische omvormer vormt één van de belangrijkste begrenzingen om aan deze continu hoger wordende eisen te kunnen voldoen. Dit proefschrift gaat over het verbeteren van de fysieke implementatie van vermogenselektronische omvormers middels het verhogen van het niveau van integratie door het gebruik van multifunctionele onderdelen.

Analyse van de huidige praktijk voor het bouwen van vermogenselektronische omvormers

Om een betere methode voor de bouw van vermogenselektronische omvormer te ontwikkelen, is een van de doelen van dit proefschrift het analyseren van de huidige bouwtechniek en het identificeren van de belangrijkste nadelen.

Vandaag de dag worden vermogenselektronische omvormers meestal opgebouwd uit discrete componenten. Elke component bestaat uit een aantal onderdelen. Naast het elektrische gedeelte is iedere component voorzien van mechanische onderdelen voor elektrische verbinding, beveiliging en koeling. Verder bevat ook de omvormer als geheel onderdelen voor de elektrische verbinding van de componenten, hun mechanische ondersteuning en beveiliging. Als alle onderdelen van de omvormer opgeteld worden, komt men veelal op een totaal aantal onderdelen dat vijf tot tien keer zo groot kan zijn dan het aantal componenten in het elektrische circuit. Dit komt niet overeen met het *Design for Manufacture and Assembly* (DFMA) principe voor goed ontwerp, dat rekening houdt met fabricage en montage kwesties. Al deze onderdelen moeten gefabriceerd en in elkaar gezet worden en dat zorgt voor hoge kosten en grote afmetingen van de omvormer. In dit proefschrift wordt de oorsprong van het grote aantal onderdelen en fabricage processen in omvormers geïdentificeerd. Verder worden een aantal vooruitzichten beschouwd, alsmede de knelpunten die belemmeren dat er in de

vermogenselektronica een doorbraak komt die vergelijkbaar is aan de doorbraak in de micro-elektronica, door de integratietechnieken van monolytisch silicium.

Systematische benadering van de realisatie van vermogenselektronische omvormers, inclusief integratie en *packaging*

De realisatie van vermogenselektronische omvormers is een multidisciplinaire techniek en omvat materiaaltechniek, ontwerptechniek, verbindingstechniek, componenttechniek, etc. Al deze kwesties, die niet tot het conventionele elektrische ontwerp behoren, worden *packaging* (verpakking) genoemd. Aan de andere kant is *packaging* soms beperkt tot de verpakking van halfgeleidercomponenten. Dit komt uit de micro-elektronica en is niet toepasbaar in de vermogenselektronica, vanwege het feit dat passieve componenten een flink deel van een typische omvormer uitmaken. Andere termen die gerelateerd zijn aan de fysieke bouw, zoals integratie, worden vaak onterecht gebruikt, en de betekenis vertoont een gebrek aan precisie en algemene toepasbaarheid.

Eén van de doelstellingen van dit proefschrift is om het bouwen van vermogenselektronische omvormers op een systematische manier te benaderen. Veder is het de bedoeling om een terminologie te introduceren die verbeteringen op dit vlak mogelijk maakt en die de communicatie van ideeën en concepten tussen vermogenselektronici mogelijk maakt. Om het bouwproces van vermogenselektronische omvormers te verbeteren, kijkt dit proefschrift dieper dan de discrete componenten waaruit vermogenselektronische omvormers meestal zijn opgebouwd. Een vermogenselektronische omvormer is gereduceerd tot zijn basisonderdelen op basis van de functies die deze onderdelen vervullen. Het aantal constructieonderdelen in de omvormer kan gereduceerd worden door de functionaliteit van verschillende onderdelen te integreren in één onderdeel. Dit omvat niet alleen elektrische (functionele) onderdelen, maar ook niet-elektrische (*packaging*) onderdelen, aangezien onderdelen voor *packaging* een groot gedeelte van het totale aantal onderdelen van een omvormer uitmaken.

Het verhogen van het niveau van integrale middels het verhogen van de functionaliteit van de functionele en de *packaging* elementen van een omvormer

Het centrale deel van het proefschrift gaat over de manier waarop het aantal functionaliteiten van de constructieonderdelen vergroot kan worden. Er worden twee grootheden geïntroduceerd die het niveau van integratie evalueren: het niveau van integratie van functionele elementen (K_I) en het niveau van integratie van verpakkings elementen (K_P). Deze grootheden representeren de gemiddelde functionaliteit van respectievelijk de functionele elementen en de elementen voor *packaging*.

In het proefschrift zijn formele methoden afgeleid die de ontwerper van vermogenselektronica kunnen helpen bij het verhogen van het niveau van integratie van de functionele en e *packaging* elementen. Verder wordt er een uitgebreid overzicht gegeven van integratietechnieken die gebruikt kunnen worden om deze methodes in de huidige omvormers te implementeren. De integratiemethoden en –technieken zijn samengevoegd in een algoritme dat het ontwerp van de functionele elementen (elektrisch en thermisch) afbeeldt op het ontwerp van de fysieke onderdelen. Het algoritme is opgenomen in het ontwerpproces als

geheel. Dit is bedoeld om het bouwen van omvormers systematischer te maken dan die nu is. Een ander belangrijk voordeel van dit algoritme, vergeleken met de conventionele ontwerppraktijk, is dat het simulatie- en modelleringsdomein en het fysieke domein elkaar gedurende het hele ontwerpproces beïnvloeden. Dit maakt een optimale realisatie van de omvormer mogelijk.

Dit ontwerpproces is toegepast in een studie met een 42V/14V dc-dc omvormer voor toepassing in een dubbel vermogensnet dat toegepast wordt in auto's. Het ontwerpproces resulteert in drie *technology demonstrators*, die gebaseerd zijn op de *Printed Circuit Board*, *thick film ceramic* en *lead frame* technologie.

Het evalueren van de bouwtechnieken aan de hand van een aantal criteria

De vermogenselektronische omvormers van de toekomst zullen gelijktijdig aan een aantal criteria (kosten, vermogensdichtheid, elektrische en thermische prestatie) moeten voldoen. Daarom is het belangrijk om, gebaseerd op al de belangrijke criteria, de verschillende opties voor het bouwproces te kunnen vergelijken, om zodoende de optimale optie voor een specifieke toepassing te kunnen kiezen. Zowel in de industrie als binnen de academische wereld worden veel , veel concepten en technieken voorgesteld. Daarom is er een middel nodig dat het mogelijk maakt om de verschillende concepten met elkaar te vergelijken.

Daarom is het laatste doel van dit proefschrift om gereedschap te ontwikkelen dat gebruikt kan worden om de optimale oplossing te kiezen uit de verschillende opties voor het bouwproces die bedacht zijn in de geïntroduceerde ontwerpalgoritmes. De evaluatiecriteria voor elke optie zijn berekend en gewogen op basis van de voorkeuren van de personen die de beslissingen nemen. Dit maakt de betrokkenheid van de industrie in een vroeg stadium van het ontwerp mogelijk. Verder kan zo'n methode helpen bij het standaardiseren van de technologie voor vermogenselektronische omvormers in hetzelfde vermogensbereik en voor vergelijkbare toepassingen.

Curriculum Vitae

Jelena Popović was born in Tuzla, Yugoslavia on September 2, 1977. In 2001, she received the Dipl. Ing. degree cum laude from the Faculty of Electrical Engineering, Department of Electronics, Telecommunications and Control, University of Belgrade, Yugoslavia.

In October 2001, she started working towards the PhD degree at the Delft University of Technology in The Netherlands. The thesis is the result of this research, done in the Electrical Power Processing group of the Faculty of Electrical Engineering, Mathematics and Computer Science. During the course of this research, she was involved in a project on miniaturization of consumer power supplies in cooperation with Philips Power Solutions, Eindhoven, The Netherlands.

Her research interests include integration and packaging in power electronics.

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