A PNP-based temperature sensor with an energy-efficient current-voltage mirror biased front-end.

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by

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Abstract

This thesis presents a PNP-based temperature sensor that employs an energy-efficient current–voltage-mirror (CVM) front-end. In contrast to prior PNP-based designs that rely on a low-noise but power-hungry bias amplifier[1], the proposed architecture replaces the amplifier with a symmetrically matched CVM, substantially reducing power consumption while preserving comparable noise performance. The PTAT voltage is generated using an emitter-area ratio rather than a current ratio, further improving energy efficiency.

To suppress mismatch, flicker noise, and offset-related errors, several dynamic techniques—including bitstream-controlled DEM, chopping, and resistor-ratio calibration—are incorporated into the system. Simulated in a 0.18-μm CMOS process, the design achieves a resolution FoM of $\mathbf{0.558}$ pJ·K$^{\mathbf{2}}$, with a resolution of $\mathbf{1.97}$ mK at a $\mathbf{38.4}$ ms conversion time. It attains an inaccuracy of $\mathbf{0.1}^\circ$C ($\mathbf{3}\sigma$) over the -55°C to 125°C temperature range after one-point trimming, while consuming only $\mathbf{3.75}$ $^{-}$W. These results demonstrate that CVM-biased front-ends provide a promising direction for next-generation ultra-low-power PNP temperature sensors.

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Contents

1

Introduction

High-accuracy temperature sensors play a critical role in a wide range of modern applications, including environmental monitoring, industrial process control, and precision instrumentation. With the continuous scaling of CMOS technology, integrated circuit (IC) temperature sensors have become increasingly attractive due to their compact size, compatibility with standard digital systems, and potential for low-cost mass production. Compared to discrete solutions, CMOS-based sensors offer improved integration with on-chip analog and digital circuitry, enabling efficient system-on-chip (SoC) designs. However, achieving high accuracy across a wide temperature range presents significant challenges, as it requires careful circuit design and compensation techniques to minimize process variations, supply sensitivity, and nonlinearity. Furthermore, to be competitive in practical applications, such sensors must achieve excellent energy efficiency and resolution within limited conversion times, while minimizing the need for costly multi-point calibration.

1.1. Types of CMOS temperature sensors

Several types of temperature sensors can be implemented in modern CMOS technologies, each with distinct advantages and limitations in terms of accuracy, energy efficiency, and calibration requirements. The energy efficiency can be expressed in terms of a resolution Figure-of-Merit (FoM)[2], which is defined as the energy consumed per conversion multiplied by the square of the achieved resolution.

$$\text{FoM} = E \cdot \sigma^2$$

where E is the energy consumed per conversion and σ is the resolution expressed in °C. A lower FoM indicates that a sensor can achieve finer resolution with lower energy cost, making it a key benchmark for comparing different architectures.

BJT-based temperature sensors exploit the well-defined temperature dependence of the base-emitter voltage of bipolar junction transistors (BJTs). Specifically, the base-emitter voltage (V_{BE}) of a BJT exhibits a complementary-to-absolute-temperature (CTAT) behavior, while the difference in base-emitter

voltages (ΔV_{BE}) between two BJTs biased at different current densities is proportional-to-absolute-temperature (PTAT). By combining these signals, accurate temperature information can be extracted. Although the low ΔV_{BE} sensitivity limits energy efficiency, BJT-based sensors can achieve state-of-the-art accuracy ($< 0.1\,^{\circ}\mathrm{C}$) across a wide temperature range with only a single-point calibration, making them highly attractive for precision applications [3].

Resistor-based temperature sensors exploit the temperature coefficient of resistance (TCR) of on-chip resistors. Their relatively high temperature sensitivity—up to $0.4\%/^{\circ}\mathrm{C}$ for high-TCR materials, compared to about $0.25\%/^{\circ}\mathrm{C}$ for BJTs [1]—allows them to achieve energy efficiencies typically 7–10 times higher than those of BJT-based sensors [3]. However, due to process-induced variations in resistor values, two-point calibration is generally required to ensure accuracy, increasing production cost and limiting their use in cost-sensitive applications [2].

MOSFET-based temperature sensors operate in the subthreshold region, where the exponential I–V characteristic resembles that of BJTs. Benefiting from this behavior, they can achieve very low supply voltages (typically 0.6–0.9 V) and excellent energy efficiency [3]. For example, subthreshold-oscillator-based sensors have demonstrated resolution FoMs in the range of $0.3\text{–}1\ \mathrm{pJ \cdot K^2}$ [4], [5]. However, their accuracy is generally limited by process variations in threshold voltage and subthreshold slope, which introduce significant spread. As a result, even the best reported designs typically achieve $0.1\ ^{\circ}\mathrm{C}$ (3σ) inaccuracy after at least a two-point calibration [5], [3], making them less suitable for precision applications requiring $< 0.1\ ^{\circ}\mathrm{C}$ accuracy.

Electro-Thermal Filter (ETF) sensors determine temperature by measuring the thermal diffusivity of silicon, a material property with a well-defined temperature dependence. Thanks to its physical robustness, ETF sensors can achieve excellent accuracy with minimal calibration; recent designs report untrimmed inaccuracies of $0.2\ ^{\circ}\mathrm{C}$ (3σ) and resolution FoMs below $7.5\ \mu J \cdot K^2$ [6], [3]. However, these sensors require an on-chip heater to stimulate thermal diffusion, which leads to substantial power consumption.

In summary, each sensor type offers a different trade-off between accuracy, energy efficiency, and calibration requirements. Among them, BJT-based temperature sensors remain the most widely used solution for high-accuracy applications, since they offer an excellent balance between accuracy and cost while being compatible with digital CMOS technologies. Recent research has demonstrated inaccuracies as low as $\pm 60\,\mathrm{mK}$ from $-70\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ after a single-point calibration [7].

1.2. Working principle of BJT-based temperature sensors

The operation of BJT-based temperature sensors relies on the well-defined temperature dependence of the base–emitter voltage (V_{BE}) of a bipolar junction transistor, as shown in Figure 1.1. According to the ideal diode equation, the collector current of a BJT is given by

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) - I_S, \tag{1.1}$$

where I_S is the saturation current, and $V_T = \frac{kT}{q}$ is the thermal voltage, with k denoting the Boltzmann constant, q the electron charge, and T the absolute temperature. Rearranging this expression and assuming that $I_{CTAT} \gg I_S$ yields

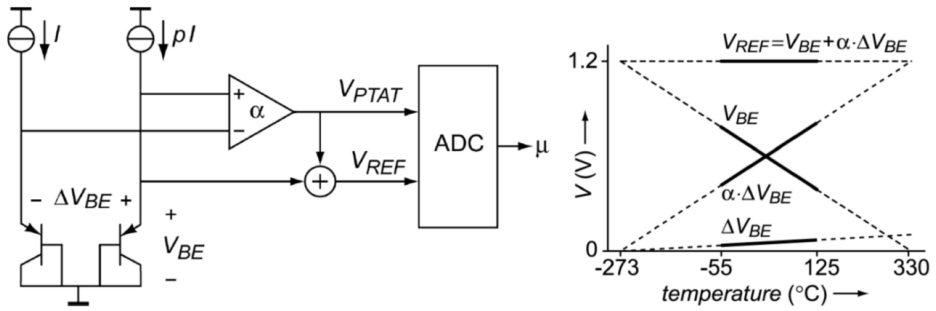

Figure 1.1: Working principle of BJT-based temperature sensor [2]

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right). \tag{1.2}$$

Since the saturation current I_S increases exponentially with temperature, V_{BE} decreases approximately linearly as temperature rises, exhibiting a complementary-to-absolute-temperature (CTAT) characteristic. This voltage therefore serves as a stable reference in many analog circuits.

To extract accurate temperature information, the difference between the base–emitter voltages of two BJTs operating at different collector current densities is often used:

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{J_1}{J_2}\right), \tag{1.3}$$

where J_1 and J_2 are the collector current densities of the two transistors. While both V_{BE} and ΔV_{BE} are temperature-dependent, the temperature coefficient (TC) of ΔV_{BE} is solely determined by the thermal voltage V_T, making it a proportional-to-absolute-temperature (PTAT) quantity.

In practical BJT-based temperature sensors, V_{BE} provides the CTAT reference, whereas ΔV_{BE} supplies the PTAT signal. By processing their ratio, a temperature-dependent digital output is obtained, ensuring compatibility with modern mixed-signal systems.

1.3. Prior-art of BJT-based temperature sensors

BJT-based temperature sensors can be realized using either PNP or NPN front-ends. NPN transistors generally offer higher current gain and lower base resistance, which contribute to superior noise performance. However, these advantages come at the expense of increased sensitivity to packaging-induced mechanical stress, leading to undesired V_{BE} offsets and requiring additional calibration. This extra calibration effort reduces the overall cost benefit of NPN-based designs. In contrast, PNP transistors are more readily available in standard single-well CMOS processes, making PNP-based implementations particularly attractive for achieving low-cost and high-accuracy temperature sensing.

Yousefzadeh et al. [7] presented a precision BJT-based temperature-to-digital converter (TDC) that achieves an inaccuracy of ± 60 mK (3σ) from -55°C to 125°C after a single room-temperature trim. The design employs a PTAT/R biasing scheme, as shown in Figure 1.2, to establish well-defined and reproducible PNP bias currents across process batches. As a result, variations in the saturation current

I_S become the dominant error source and can be effectively corrected by digital PTAT trimming. To suppress process-induced mismatch and low-frequency noise, the design employs several dynamic error-cancellation techniques, including DEM of current ratios, dynamic swapping of current-mirror devices, and a chopped folded-cascode amplifier for offset and $1/f$-noise reduction. In addition, a dedicated β-monitor allows the current gain of the sensing PNPs to be measured on-chip, enabling accurate characterization and compensation of β-related errors. Fabricated in 0.16-µm CMOS, the sensor achieves an inaccuracy of ± 60 mK (3σ) from -55 °C to 125 °C after single-point trimming, with a power consumption of 4.6 µA, a resolution of 15 mK_{rms}, and a resolution FoM of 7.8 $\text{pJ} \cdot ^\circ\text{C}^2$.

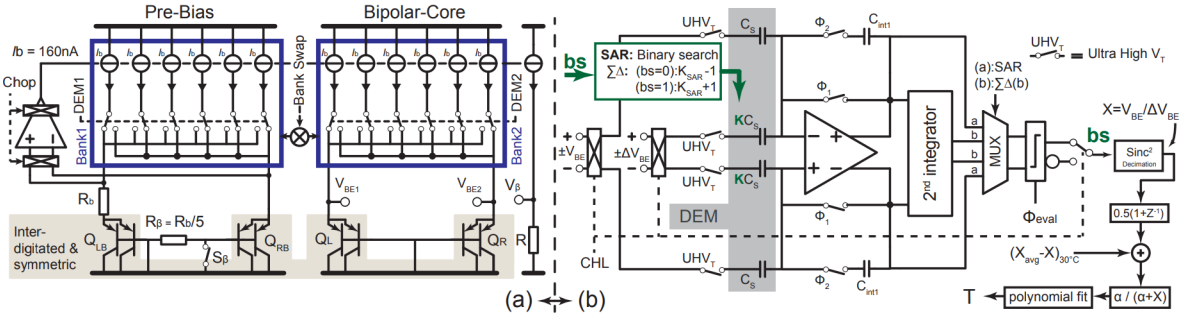

Figure 1.2: The PNP based front-end of Bahman 2017 [7]

Toth et al. [1] proposed a continuous-time (CT) current-mode readout architecture that achieves significantly improved energy efficiency. The front-end employs a PTAT/Resistance (PTAT/R) biasing scheme that is optimized for supply voltage, bias current, and noise, thereby providing a low-power and low-noise bias condition for the readout. As shown in Figure 1.3, the design converts V_{BE} and ΔV_{BE} into currents and digitizes them using a continuous-time $\Delta\Sigma$ modulator (CTDSM), effectively eliminating the kT/C noise limitation inherent to discrete-time implementations. The CTDSM consists of a continuous-time first-stage integrator followed by a switched-capacitor (SC) second stage; since the first-stage gain attenuates the kT/C noise of the SC integrator, the latter can be implemented with minimal area overhead. The resulting sensor achieves a competitive figure of merit (FoM) of 0.85 $\text{pJ} \cdot \text{K}^2$ and an inaccuracy of ± 0.1 °C (3σ) from -55 °C to 125 °C after single-point trimming. This work demonstrates that substantial gains in energy efficiency can be achieved by using CT readout.

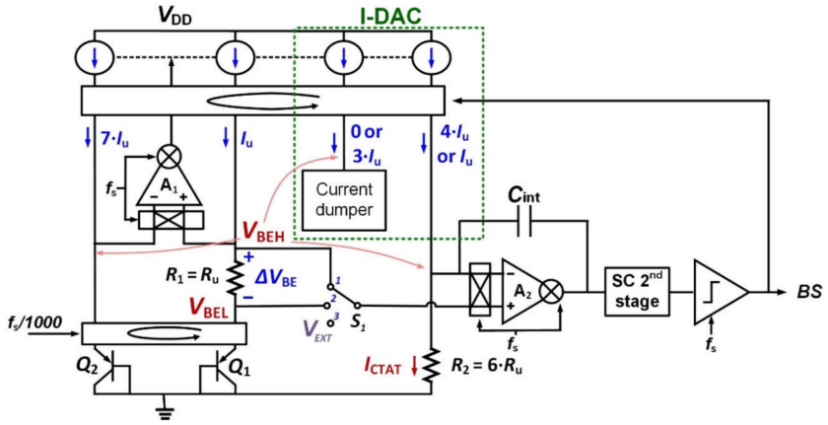

Figure 1.3: PNP based Temperature Sensor with CT Readout [1]

In parallel to the resolution-driven approach of [1], Tang et al. [8] showed that energy efficiency can also be significantly improved by reducing power consumption while maintaining high accuracy, as shown in

Figure 1.4. Their design introduces a capacitively biased BJT front-end, in which sampling capacitors are first precharged to V_{DD} and then discharged through diode-connected BJTs to generate PTAT and CTAT voltages. Because this capacitive biasing approach requires only a small voltage headroom (approximately 150 mV) to establish the BJT's operating point, it enables robust sub-1 V operation even when V_{BE} approaches 0.8 V at cold temperatures. Combined with a low-power inverter-based $\Delta\Sigma$ readout architecture—where auto-zeroed inverter stages provide sufficient gain for precision digitization while operating at nanoampere-level bias currents—this allows the sensor to operate from a 0.95 V supply while consuming only 810 nW at room temperature. Fabricated in a 0.18-µm CMOS process, the sensor achieves an inaccuracy of ± 0.15 °C (3σ) from -55 °C to 125 °C after single-point trimming and a state-of-the-art resolution figure of merit (FoM) of $0.34\,\mathrm{pJ}\cdot^{\circ}\mathrm{C}^2$. This work demonstrates that aggressively lowering supply voltage and removing static power offer an effective and complementary path toward improving the energy efficiency of BJT-based temperature sensors.

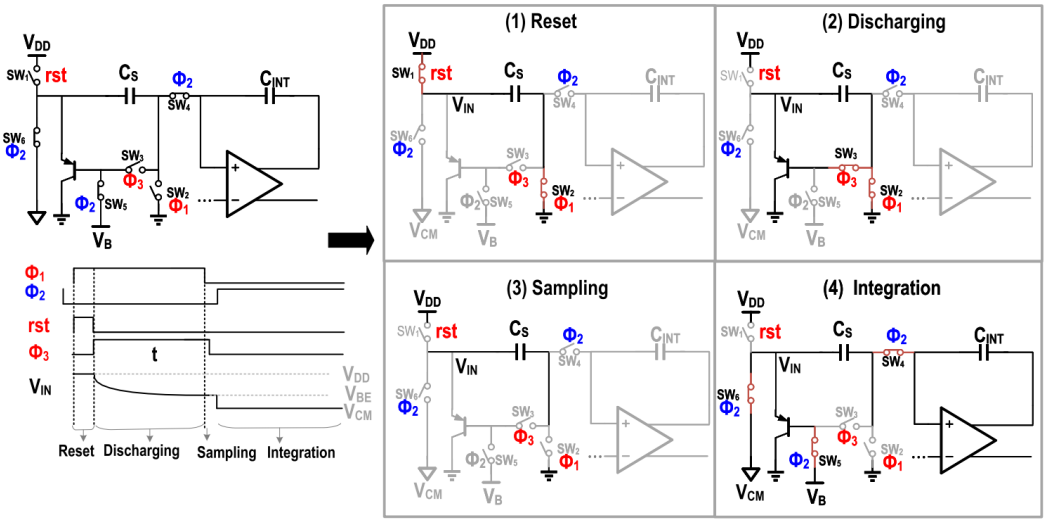

Figure 1.4: The PNP based front-end of Zhong 2023 [8]

Table 1.1: Performance summary of prior-art BJT-based temperature sensors

	JSSC'17 [7]	JSSC'23 [8]	JSSC'25 [1]
Sensor type	PNP	PNP	PNP
Architecture	DTΔΣM	DTΔΣM	CTΔΣM
Technology	0.16 µm	0.18 µm	0.18 µm
Supply current [µA]	4.6	0.81	9.5
Supply voltage [V]	1.5–2	0.95–1.4	1.7–2.2
Temperature range [°C]	-55–125	-55–125	-55–125
3σ Inaccuracy [°C] (1-pt trim)	±0.06	±0.15	±0.1
Resolution FoM $[pJ \cdot K^2]$	7.8	0.34	0.85

A summary of the performance characteristics of the discussed BJT-based temperature sensors is provided in Table 1.1, serving as a benchmark for evaluating the results presented in this work.

This work aims to further improve the energy efficiency of PNP-based temperature sensors with CT

readout while preserving their intrinsic accuracy and robustness against process and stress variations. To this end, the proposed design focuses on reducing the supply current of design [1]—and thus the overall power consumption—to achieve an additional enhancement in energy efficiency.

1.4. Organization of the thesis

The remainder of this thesis is organized as follows. Chapter 2 provides a detailed comparison of several existing temperature sensor architectures and introduces the proposed design. The noise, power, and accuracy performance of the proposed topology are analyzed and compared with state-of-the-art works. Chapter 3 presents the circuit-level implementation of the proposed sensor, including the design considerations and final configurations of the BJT front-end. This chapter also includes an analysis of simulated noise and power, along with a discussion of signal timing. Chapter 4 presents the simulation results obtained using the Cadence Spectre environment, including sensor resolution, power consumption, supply sensitivity, and temperature inaccuracy. Finally, Chapter 5 concludes the thesis by summarizing the main findings and outlining potential directions for future research.

2

Architecture Considerations

To further enhance the energy efficiency of state-of-the-art temperature sensors, architectural innovations are required to address the inherent limitations of existing designs. In this section, a state-of-art PNP-based work [1] is reviewed and analyzed to provide a basis for comparison. Building upon several insights from other works, a more energy-efficient architecture is proposed, followed by a first-order analysis to estimate the achievable Figure-of-Merit (FoM) of the proposed design.

2.1. A CT current-mode PNP-based design

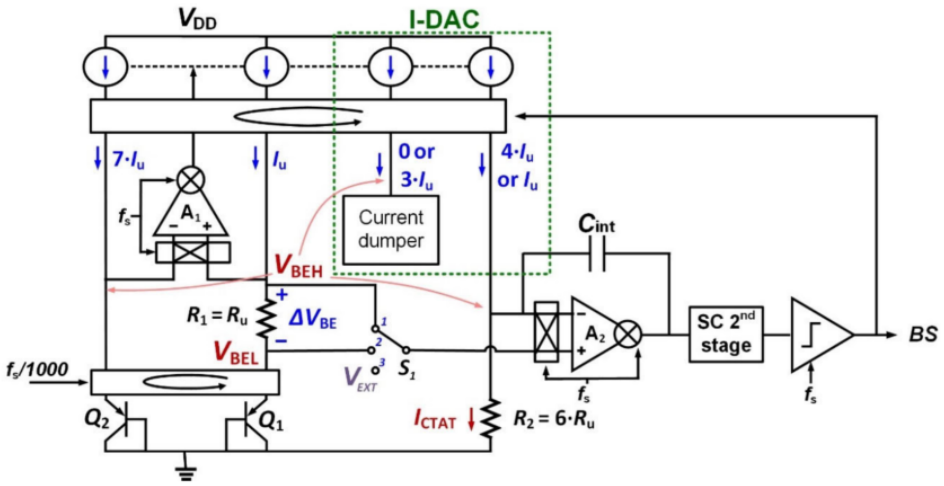

Figure 2.1: PNP based Temperature Sensor with CT Readout [1]

In [1], as shown in Figure 2.1, the sensing element consists of two PNP transistors. Biasing them with current ratio 7:1, two temperature-dependent voltages are generated —V_{BE} (a voltage complementary to absolute temperature) and ΔV_{BE} (a voltage proportional to absolute temperature)

$$V_{be} = n\frac{kT}{q}\ln\left(\frac{I_c}{I_s}\right) = n\frac{kT}{q}\ln\left(\frac{I_{PTAT}}{I_s}\cdot\frac{\beta}{\beta+1}\right) \tag{2.1}$$

$$\Delta V_{be} = V_{be2} - V_{be1} = n\frac{kT}{q}\ln\left(\frac{7I_{PTAT}}{I_{PTAT}}\frac{\beta_2(\beta_1+1)}{\beta_1(\beta_2+1)}\right) = n\frac{kT}{q}\ln(7\frac{\beta_2(\beta_1+1)}{\beta_1(\beta_2+1)}) \tag{2.2}$$

where β_1 and β_2 are the current gains of Q_1 and Q_2. Biasing them in "flat" region, the mismatch between β_1 and β_2 can be tolerated [1].

With V_{BE} and ΔV_{BE}, the temperature-dependent currents I_{PTAT} and I_{CTAT} can be generated through resistors R_1 and R_2. The equations are shown below:

$$I_{PTAT} = \frac{\Delta V_{BE}}{R_1} \tag{2.3}$$

$$I_{CTAT} = \frac{V_{BE}}{R_2} \tag{2.4}$$

The biasing circuit comprises an amplifier (A_1), a resistor (R_1), and PMOS current sources. In this biasing circuit, the PMOS current sources generate two biasing currents with a 7:1 ratio. The amplifier (A_1) biases the PMOS current sources, ensuring that all current sources have the same output voltage. As a result, the voltage across the bias resistor (R_1) becomes a well-defined ΔV_{BE}, which in turn generates the PTAT current according to Equation 2.3.

The ADC is implemented as a continuous-time delta–sigma modulator (CTDSM), featuring a second-order loop filter. The loop filter comprises a first-stage continuous-time integrator and a second-stage switched-capacitor (SC) integrator. The first-stage integrator is also reused to generate I_{CTAT} (2.4). This design effectively mitigates kT/C noise while minimizing power consumption. The current DAC consists of a resistor R_2, a dumper, and multiple current sources. The DAC output alternates between $I_{\text{PTAT}} - I_{\text{CTAT}}$ and $4I_{\text{PTAT}} - I_{\text{CTAT}}$, controlled by the modulator's output bitstream. Figure 2.2 shows the dual-level DAC topology and the plot of I_{PTAT}, $4I_{\text{PTAT}}$, and I_{CTAT} versus temperature. Each time the DAC switches its output current, the terminal voltages of the internal current sources also change, resulting in switching transient errors. To address this, the inclusion of a dumper ensures that the terminal voltages remain constant during switching, thereby mitigating the effects of these transients. To address intermodulation effects between dynamic element matching (DEM) and the output bitstream modulation, a bitstream-controlled DEM (BSC-DEM) technique is employed [9]. This approach ensures that each DEM state occurs with equal frequency, regardless of the bitstream sequence.

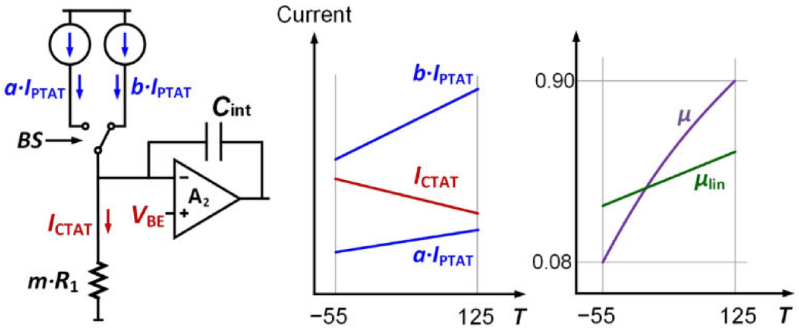

Figure 2.2: Simplified circuit diagram with a dual-level IDAC, and the resulting currents versus temperature.[1]

To achieve high accuracy, the design of [1] employs multiple dynamic error-correction techniques. Chop-

ping is applied to the biasing amplifiers A_1 to suppress offset and $1/f$ noise, while DEM suppresses mismatch in the PMOS current sources and the PNP devices. A bitstream-controlled DEM (BSC-DEM) scheme is used to avoid intermodulation with the modulator bitstream, ensuring that each DEM state is exercised with nearly equal frequency [\cite {1356649}]. Together, these techniques effectively suppress offset and mismatch, enabling the sub-0.1°C inaccuracy reported in [1].

The primary contributors to power consumption in this design are the low-noise amplifier A_1, the current-mode DAC, and the BJTs. The dominant sources of noise, on the other hand, are the amplifier A_1, the bias resistor, the PMOS current sources, and the BJTs. The input-referred noise of A_1 limits the energy-resolution efficiency of this design because it is directly in series with ΔV_{BE}. As a result, A_1 is biased with $6I_{\mathrm{PTAT}}$, accounting for about 25% of the front-end power consumption and roughly 30% of its total noise.

2.2. Proposed architecture

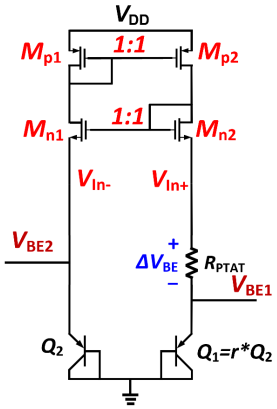

Figure 2.3: Self Biased current voltage mirror (CVM)

In [1], amplifier A_1 add extra noise and power, limiting the overall energy efficiency. To eliminate this amplifier, a current–voltage mirror (CVM)-based biasing circuit can be adopted, as shown in Figure 2.3. This circuit consists of a PMOS current mirror and an NMOS voltage mirror. The PMOS current mirror defines the current ratio between the two branches, while the NMOS voltage mirror ensures equivalent source voltages for the two NMOS transistors. However, in this topology, the drain–source voltages (V_{DS}) of the two PMOS transistors differ, resulting in a current ratio error. Consequently, a voltage mismatch appears at the sources of the NMOS transistors, which results in an error in ΔV_{BE}.

To address this issue, a self-biased symmetrically matched CVM was first proposed in [10], where a feedback common-gate differential pair compensates for the mismatch, as shown in Figure 2.4. This CVM was later adopted in a dynamic-threshold MOST (DTMOST) based temperature sensor design in [11], achieving an inaccuracy of ± 0.4 °C (3σ) from -40 °C to 125 °C with a power consumption of 600 nW. In that design, the PMOS current sources were self-biased in weak inversion to save voltage headroom.

However, when applying the self-biased symmetrically matched CVM to the PNP-based CT readout design in [1] to replace the power-hungry amplifier, a new challenge arises. The design in [1] employs a current-mode readout scheme, in which the PMOS current sources are biased in strong inversion to minimize their noise contribution. If this CVM is applied to [1] while keeping the PMOS current sources

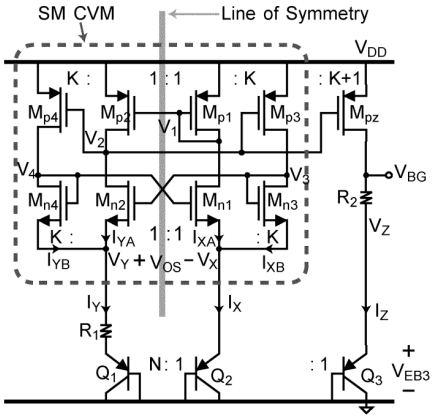

Figure 2.4: Self Biased Symmetrically Matched CVM [10]

in strong inversion to maintain a similar noise level, the required voltage headroom becomes

$$V_{\text{headroom}} = V_{\text{GS,p}} + V_{\text{Dsat,n}} = V_{\text{th,p}} + V_{\text{ov,p}} + V_{\text{Dsat,n}} = V_{\text{th,p}} + V_{\text{Dsat,p}} + V_{\text{Dsat,n}},$$

where $V_{\text{GS,p}}$ is the gate–source voltage of the PMOS current mirror, $V_{\text{ov,p}}$ is its overdrive voltage, and $V_{\text{Dsat,p}}$ and $V_{\text{Dsat,n}}$ are the saturation voltages of the PMOS current mirror and the NMOS voltage mirror, respectively.

Compared with the original implementation that relies on a power-hungry amplifier—where the current mirror requires only $V_{\text{Dsat,p}}$ of headroom when cascodes are neglected—the use of a strong-inversion PMOS current mirror in the CVM therefore increases the front-end voltage headroom by an additional $V_{\text{Dsat,n}} + V_{\text{th,p}}$.

Although biasing the NMOS voltage mirror in weak inversion can reduce $V_{\text{Dsat,n}}$ to approximately 0.1 V, the contribution of $V_{\text{th,p}}$ remains significant, resulting in an additional 530 mV of voltage headroom at cold temperatures ($-55\,^{\circ}\text{C}$). This increased headroom limits the ability of the design to operate at low supply voltages, thereby offsetting the advantage gained by eliminating the power-hungry amplifier. Consequently, a more effective biasing approach is needed—one that maintains strong-inversion operation of the PMOS current mirror while minimizing headroom requirements.

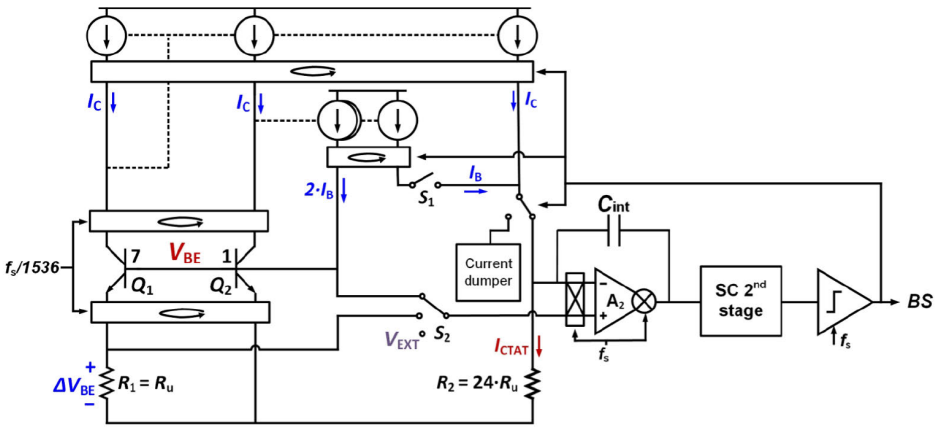

Figure 2.5: Front-end Implementation of NPN based Temperature Sensor [12]

Interestingly, the biasing technique used in an NPN-based CT readout design [12] achieves precisely this balance. As illustrated in Figure 2.5, two complementary biasing loops are employed: a PMOS biasing loop driven by a low-power amplifier A_1, and an NPN biasing loop realized by a high-threshold-voltage NMOS common-source stage followed by a current-mirror output stage. The resulting V_{BE} and I_{PTAT} are then applied to a second order CTDSM.

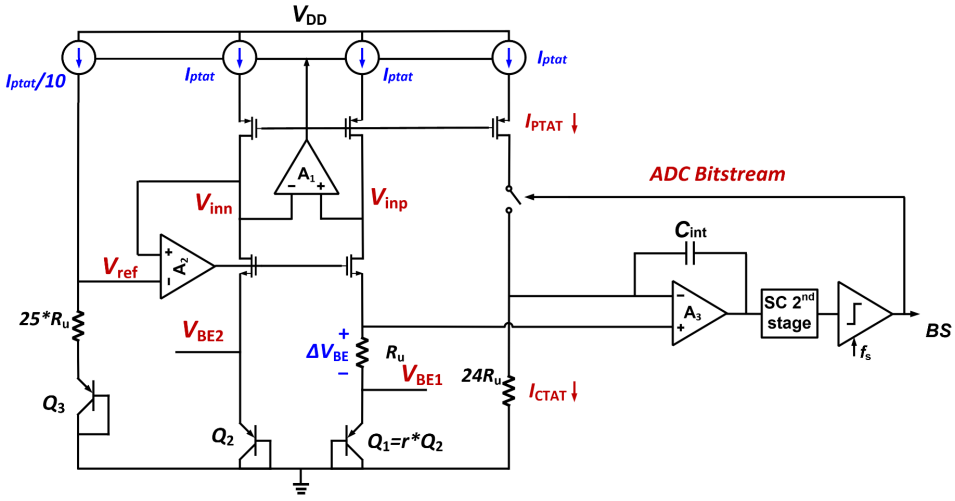

Figure 2.6: Proposed architecture with CVM biasing and CT readout.

A similar dual-loop biasing strategy can be applied to the PMOS current mirror and NMOS voltage mirror of the CVM, as illustrated in Figure 2.6. In this configuration, A_1 establishes a feedback loop that biases the PMOS current mirror, while A_2 forms a second loop that biases the NMOS voltage mirror. This second loop is closed through a reference branch consisting of a resistor and a PNP transistor, which are biased by a PTAT current to produce a CTAT reference voltage. By biasing the PMOS and NMOS devices in this manner, the required voltage headroom—neglecting the cascodes—is reduced from $V_{\mathrm{Dsat,n}} + V_{\mathrm{Dsat,p}} + V_{\mathrm{th,p}}$ to $V_{\mathrm{Dsat,n}} + V_{\mathrm{Dsat,p}}$, corresponding to a 530 mV reduction in the supply-voltage requirement.

In the proposed front-end, the PMOS devices in the current mirror operate in strong inversion, whereas the NMOS devices in the voltage mirror operate in weak inversion, thereby minimizing their noise contribution. Neglecting the cascodes of the PMOS current mirror, the required voltage headroom is $V_{\mathrm{Dsat,n}} + V_{\mathrm{Dsat,p}}$, leading to only a 0.1 V higher supply voltage compared to the design in [1]. Furthermore, the noise introduced by the two additional biasing amplifiers is effectively attenuated by the output impedance of the NMOS voltage mirror, allowing these amplifiers to be designed with relaxed noise requirements and thus lower power consumption.

Unlike the previous implementation [1], which use a current ratio to generate a PTAT voltage, the proposed architecture uses an emitter-area ratio. This choice simplifies the biasing network and further reduces power consumption.

For analog-to-digital conversion, the proposed system reuses the second-order continuous-time delta–sigma modulator from the NPN-based CT readout design in [12].

2.3. Noise Analysis

In this section, the main noise contributors of the proposed design are analyzed, followed by a comparison with the implementation in [1].

2.3.1. Noise of the proposed design

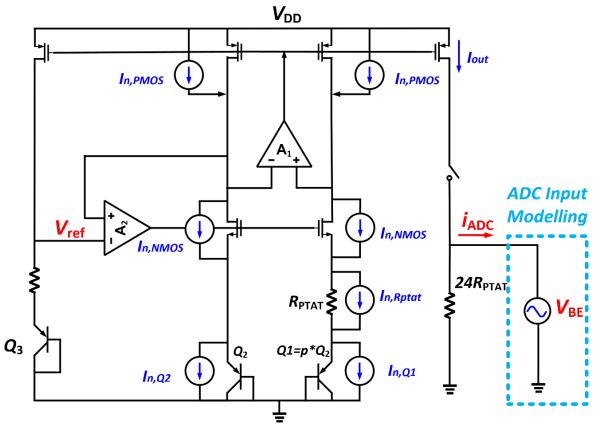

Figure 2.7: All noise Sources in the Proposed Architecture.

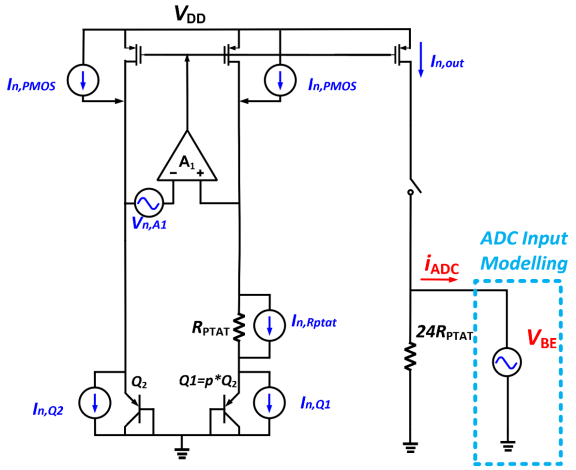

Figure 2.8: All noise Sources in the conventional front-end [1].

The main noise contributors in the proposed architecture are the PMOS current sources, the NMOS voltage mirror, the PTAT resistor, and the PNPs, as shown in Figure 2.7. In the conventional front end of [1], the corresponding contributors are the PMOS current sources, the biasing amplifier A_1, the PTAT resistor, and the PNPs, as shown in Figure 2.8. Their respective contributions to the PTAT current delivered to the IDAC are summarized and compared in Table 2.1. Since the CTAT path contributes negligible noise compared to the PTAT path [2], only the PTAT-current noise is considered. All noise values are obtained from Cadence simulations.

Table 2.1: Noise power comparison between the design [1] and the proposed work

Noise Source	Original front-end [1] (pA^2/Hz)	Share (%)	Proposed front-end (pA^2/Hz)	Share (%)
Current mirrors	0.0779 ($g_m/I_D = 4.57$)	22.89	0.0933 ($g_m/I_D = 2.70$)	23.15
Opamp A_1	0.0975 ($g_m/I_D = 28.47$)	28.65	0	0
Voltage mirrors	0	0	0.113 ($g_m/I_D = 29.41$)	28.03
Resistors	0.1269 ($I_D = 390\,\text{nA}$)	37.29	0.127 ($I_D = 390\,\text{nA}$)	31.51
BJTs	0.038 ($I_D = 390\,\text{nA}$)	11.17	0.0698 ($I_D = 390\,\text{nA}$)	17.32
Total	0.3403	100	0.4031	100

Several differences can be observed. First, in [1] the amplifier A_1 is a major noise contributor, with a noise power of about $0.0975\ \text{pA}^2/\text{Hz}$. In the proposed design this block is removed and replaced by an NMOS voltage mirror, whose noise contribution is $0.113\text{pA}^2/\text{Hz}$. Although slightly higher ($\approx 1.16\times$), its magnitude is essentially comparable to that of A_1 in the original design.

Secondly, the PMOS current mirrors contribute about $1.2\times$ more absolute noise in the proposed design than in [1], even though a lower g_m/I_D is used. This stems from the presence of the NMOS voltage mirrors, which modify the way PMOS-mirror noise currents are transferred to the PTAT branch, thereby increasing their contribution.

Third, the PTAT resistor remains the dominant noise source in both designs, and its absolute noise

power is essentially unchanged.

Finally, the BJT noise contribution in the proposed design is roughly twice that of [1]. This results from the way the 7:1 PTAT ratio is implemented. In [1] the ratio is set by scaling the bias currents, so one PNP is biased at $7I_{\mathrm{PTAT}}$ and contributes proportionally less thermal noise. In the proposed design the same ratio is realized by emitter-area scaling while keeping the bias currents equal, so both PNPs are biased at at I_{PTAT}, contributing comparable noise.

Overall, the total PTAT-current noise of the proposed design is about 20% higher than that of [1].

Table 2.2: Noise power comparison between the the area–ratio variant of [1] and the proposed work

Noise Source	Area–ratio variant of [1] (pA^2/Hz)	Share (%)	Proposed front-end (pA^2/Hz)	Share (%)
Current mirrors	0.083 ($g_m/I_D = 4.57$)	22.23	0.0933 ($g_m/I_D = 2.70$)	23.15
Opamp	0.0975 ($g_m/I_D = 28.47$)	26.11	0	0
Voltage mirrors	0	0	0.113 ($g_m/I_D = 29.41$)	28.03
Resistors	0.1269 ($I_D = 390\,\mathrm{nA}$)	33.96	0.127 ($I_D = 390\,\mathrm{nA}$)	31.51
BJTs	0.066 ($I_D = 390\,\mathrm{nA}$)	17.69	0.0698 ($I_D = 390\,\mathrm{nA}$)	17.32
Total	0.3734	100	0.4031	100

To further isolate the impact of replacing the biasing amplifier with the CVM-based biasing scheme, an area–ratio variant of [1] was simulated, in which the two PNP devices use a 7:1 emitter-area ratio while being biased with the same current. The resulting noise breakdown is summarized in Table 2.2.

Several observations follow. First, when the original front end is modified to use an area ratio, the BJT noise increases from 0.038 to 0.066 $\mathrm{pA}^2/\mathrm{Hz}$, closely matching the value obtained in the proposed design ($0.070\mathrm{pA}^2/\mathrm{Hz}$). This confirms that the increase in BJT noise is an intrinsic consequence of using an area ratio rather than an artifact of the CVM-based biasing.

Second, the PMOS current-mirror noise in the area–ratio variant of [1] increases only slightly (from 0.078 to 0.083 $\mathrm{pA}^2/\mathrm{Hz}$) and remains lower than in the proposed front end ($0.093\mathrm{pA}^2/\mathrm{Hz}$). The remaining difference is therefore attributable to the introduction of the NMOS voltage mirrors, whose noise-transfer characteristics cause a larger portion of the PMOS-mirror noise to appear in I_{PTAT}.

Third, the noise contributions of the PTAT resistor and the biasing amplifier A_1 are unchanged when the original design [1] is modified to use an area ratio, as both elements operate identically in the two variants.

Overall, replacing the current-ratio biasing in [1] by an area ratio accounts for a significant portion of the noise increase (from 0.340 to $0.373\mathrm{pA}^2/\mathrm{Hz}$). The additional increase in the proposed CVM-based front end (to 0.403 $\mathrm{pA}^2/\mathrm{Hz}$) arises mainly from the noise of the NMOS voltage mirrors and their impact on PMOS-mirror noise transfer. Despite this, the CVM-based biasing remains attractive due to its substantially lower power consumption.

2.4. Power considerations

The power performance of the proposed design and the design in [1] is summarized in Table 2.3. Replacing the current-ratio-based front-end with an area-ratio-based implementation reduces the supply current of the BJT branches from $8I_{\mathrm{PTAT}}$ to $2I_{\mathrm{PTAT}}$. Furthermore, substituting the power-hungry amplifier with an NMOS voltage mirror and two low-power biasing amplifiers (A_1 and A_2) decreases the amplifier current from $6I_{\mathrm{PTAT}}$ to $0.3I_{\mathrm{PTAT}}$. The replacement of the $4 \times I_{\mathrm{PTAT}}$ IDAC with a $1 \times I_{\mathrm{PTAT}}$ IDAC further lowers the overall supply current. In addition, the reduced output current of the IDAC

allows the first integrator in the CTDSM to operate with a much smaller bias current—$1.5I_{\text{PTAT}}$ instead of $4I_{\text{PTAT}}$—resulting in additional power savings across the entire system.

Table 2.3: Power consumption comparison between the design [1] and the proposed work

Supply current	Design [1] ($V_{DD} = 1.7\,\text{V}$)	Proposed Design ($V_{DD} = 1.5\,\text{V}$)
BJTs	$8I_{\text{PTAT}}$	$2I_{\text{PTAT}}$
Op amp	$6I_{\text{PTAT}}$	$0.35I_{\text{PTAT}}$
DAC branch	$4I_{\text{PTAT}}$	$1I_{\text{PTAT}}$
DSM opamp	$4I_{\text{PTAT}}$	$1.5I_{\text{PTAT}}$
Rest of the DSM	$2.35I_{\text{PTAT}}$	$1.6I_{\text{PTAT}}$

The estimated power consumption of the proposed design is $6.45\,I_{\text{PTAT}} \times 1.5\text{ V} \approx 3.75\ \mu\text{W}$.

Compared with the $16.15\ \mu\text{W}$ consumed by the design in [1], this represents a reduction by approximately a factor of $4.3\times$.

2.5. Mismatch problems

In the proposed architecture, the CTDSM measures temperature by balancing the PTAT and CTAT currents, which can be expressed as [13]:

$$I_{\text{PTAT}} = \frac{\Delta V_{BE}}{R_1} = \frac{V_T}{R_1}\ln(p \cdot r) + V_{OS}, \tag{2.5}$$

$$I_{\text{CTAT}} = \frac{V_{BE}}{R_2} = \frac{V_T}{R_2}\ln\left(\frac{I_{\text{PTAT}}}{I_S} \cdot \frac{\beta}{\beta+1}\right), \tag{2.6}$$

where p is the current ratio between the ($R_{\text{PTAT}} + \text{PNP}$) and PNP branches, r is the emitter area ratio between transistors Q1 and Q2, V_{OS} is the offset introduced by the biasing circuit, I_S is the saturation current of the PNP, and β is the current gain of the PNP transistor.

The average bitstream value μ at the output of the CTDSM can be derived from the following equations:

$$\mu\,(I_{\text{PTAT},BS=1} - I_{\text{CTAT}}) + (1-\mu)\,(I_{\text{PTAT},BS=0} - I_{\text{CTAT}}) = 0, \tag{2.7}$$

$$\mu = 1 - \frac{I_{\text{CTAT}}}{I_{\text{PTAT}}} = 1 - \frac{\ln\left(\frac{I_{\text{PTAT}}}{I_S} \cdot \frac{\beta}{\beta+1}\right)}{m\ln(p \cdot r)}, \quad \text{where } m = \frac{R_2}{R_1}. \tag{2.8}$$

Since μ is a nonlinear function of temperature, it must be linearized and converted into temperature using fitted parameters A, B, and α:

$$\mu_{\text{lin}} = \frac{\alpha \cdot \Delta V_{BE}}{V_{\text{ref}}} = \frac{\alpha \cdot \Delta V_{BE}}{\alpha \cdot \Delta V_{BE} + V_{BE}} = \frac{\alpha}{\alpha + m(1-\mu)}, \tag{2.9}$$

$$T\ (^\circ\text{C}) = A \cdot \mu_{\text{lin}} - B. \tag{2.10}$$

From the equations above, it can be observed that process variations in p, r, I_S, m, and β directly affect the temperature accuracy of the sensor. The V_{OS} error can be mitigated by a well-defined biasing circuit. According to the schematic shown in Figure 2.6, the spread in p mainly arises from mismatches in the current mirrors, while the spread in r is primarily caused by mismatches between the PNP transistors. The variation in I_S originates from process corner deviations of the PNP devices, whereas the spread in m results from mismatches between resistors R_1 and R_2. In addition, the input offset of amplifier A_1 and the mismatch of the NMOS differential pair also influence the accuracy of ΔV_{BE} and, consequently, the temperature measurement. Therefore, dynamic compensation and trimming techniques are required to mitigate these variations and ensure reliable calibration.

2.6. Dynamic techniques for better matching

To address the aforementioned error sources, several dynamic error-correction techniques are employed in the proposed design.

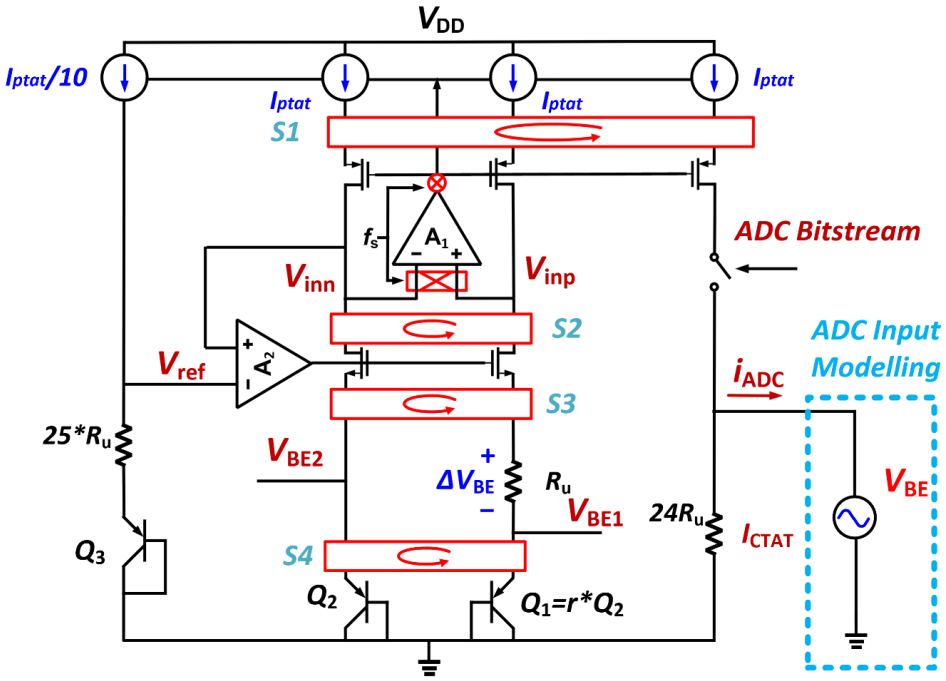

Figure 2.9: Dynamic error-correction techniques in proposed front-end

Mismatch in the PMOS current mirrors is suppressed by applying DEM, as shown in Figure 2.6. In this design, the three PMOS unit devices are dynamically rotated to averages out their mismatch. To shift the flicker noise of the PMOS devices out of band, the DEM operates at the sampling frequency (f_S = 80 kHz). After the downstream sinc^2 low-pass filtering, the residual DEM-shaped noise is effectively removed.

The offset of amplifier A_1 is mitigated by chopping at a frequency equal to the sampling frequency f_S. Since the worst-case flicker-noise corner of A_1 is approximately 680 Hz, a chopping frequency equal to the DEM frequency of the PMOS current mirror ensures that the entire flicker-noise spectrum is modulated well beyond the baseband.

The mismatches of the NMOS voltage mirror and PNP transistors are mitigated by the DEM techniques. Similar to the PMOS current mirrors and amplifier A_1, the NMOS unit device is dynamically selected

according to the bitstream at f_S, which effectively shifts its flicker noise to higher frequencies while avoiding intermodulation with the bitstream. The PNPs, on the other hand, are modulated at a relatively low DEM frequency of $\frac{f_S}{1536}$, because their flicker-noise corner is below 10 Hz and thus has a negligible effect on resolution. Consequently, a lower DEM frequency can be used to minimize quantization noise folding and switching transients without compromising the overall noise performance.

2.7. Summary

This chapter described the design methodology and analyzed the noise and power performance of the proposed architecture. The following chapter focuses on the implementation details of each circuit block.

3

Circuit Implementation

In this chapter, the circuit-level implementation of the proposed sensor, including the design considerations and final configurations of each building block, is presented. The system is divided into two main sections: the BJT front-end and the delta–sigma modulator (DSM). This chapter also includes an analysis of simulated noise and power, along with a discussion of signal timing.

3.1. BJT front-end

As illustrated in Figure 3.1, the front-end consists of seven primary components: BJTs, resistors, current mirrors, voltage mirrors, PMOS biasing loop, and NMOS biasing loop. The bias current I_{PTAT} is copied and applied to a CTDSM, as in [12].

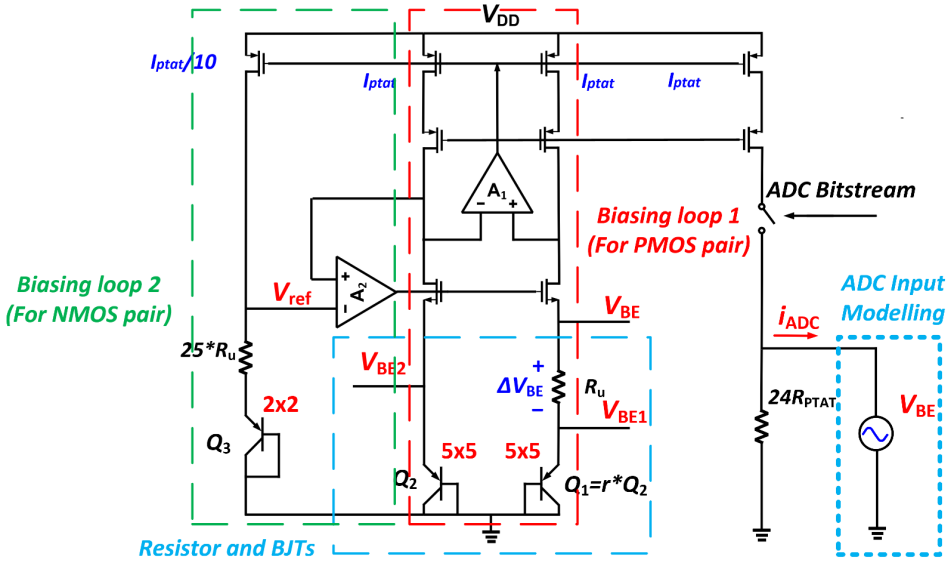

Figure 3.1: The PNP-based front-end of proposed design.

3.1.1. BJTs and resistors

In this work, two PNP transistors are used to generate the CTAT voltage V_{BE} and the PTAT voltage ΔV_{BE}. To maintain compatibility with the CTDSM readout in [1], the PTAT current I_{PTAT} is fixed at 390 nA at room temperature, which is achieved by using a 132 kΩ PTAT resistor together with a 7:1 current-density ratio between the two PNP devices.

Unlike the design in [1], where the 7:1 ratio is implemented by scaling the bias currents, the proposed design realizes the same ratio through emitter-area scaling while keeping the bias currents equal. This approach reduces the current density of the low-V_{BE} device by 7×. With this choice, both devices still operate within the relatively flat region of the β–current characteristic, as confirmed by the measured β distribution of the 5 μm × 5 μm PNP array shown in Figure 3.2. Within the corresponding bias-current range ($40.5nA$ to $508nA$) of the two devices over temperature, the extracted β mismatch remains below 0.03, and the resulting contribution to the ΔV_{BE} error after a single-point trim is less than 50mK. The use of area scaling avoids the need for extra current branches, which reduces overall power consumption by approximately 25%.

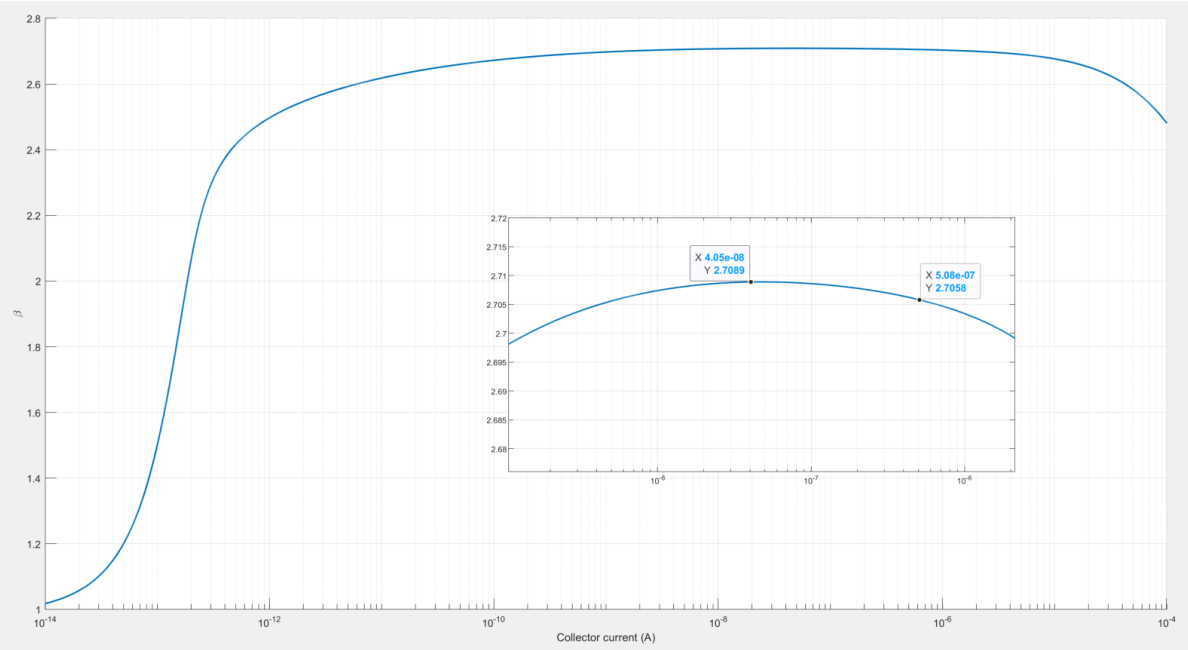

Figure 3.2: Current gain β of a 5 μm × 5 μm PNP as a function of collector current.

3.1.2. Current Mirrors

The current mirrors establish an accurate current ratio between the two PNP branches and provide the PTAT current to the CTDSM. In the proposed design, the mirror is implemented as a PMOS current mirror with a single cascode stage to enhance the output impedance, as illustrated in Figure 3.1. Its main design considerations are output impedance, noise, voltage headroom, and high-temperature leakage.

(1) Voltage Headroom:

The required voltage headroom is given by $V_{\text{Dsat,cm}} + V_{\text{Dsat,cas}}$, both of which decrease as the PMOS aspect ratio W/L increases. In the proposed design, the mirror transistors use $W/L = 0.9\ \mu\text{m}/30\ \mu\text{m}$, resulting in $V_{GS} = 1V$ at $-55°\text{C}$ and $V_{GS} = 1.3V$ at $125°\text{C}$. Under these bias conditions, the mirror-transistor saturation voltage is approximately 450 mV at $-55°\text{C}$ and 730 mV at $125°\text{C}$. The cascode

device using $W/L = 8\ \mu\text{m}/6\ \mu\text{m}$ adds a further 65 mV and 121 mV at the same temperatures, respectively. The resulting total voltage headroom ensures reliable operation under a 1.5 V supply.

(2) Output impedance: Because the NMOS voltage mirrors appear only in the PNP branches, the PMOS current mirror in the IDAC branch operates with a larger V_{DS}, which would introduce a systematic current error due to channel-length modulation. To suppress this effect, long-channel PMOS devices ($L = 30\ \mu\text{m}$) together with an $8\mu\text{m}/6\mu\text{m}$ cascode stage are employed, achieving an output resistance of approximately 5.5 GΩ. This limits the worst-case current-copying mismatch between the PNP and IDAC branches to about 110 pA at 125°C, corresponding to a temperature error of roughly 30 mK.

(3) Noise: The dominant noise sources are flicker noise and thermal noise. Flicker noise decreases with gate area,

$$\overline{i_{n,1/f}^2} = \frac{K_f}{C_{\text{ox}}^2 WLf}, \tag{3.1}$$

while thermal noise increases with transconductance,

$$\overline{i_{n,\text{thermal}}^2} = 4kT\gamma g_m. \tag{3.2}$$

To suppress flicker noise, a gate area of $0.9\ \mu\text{m} \times 30\ \mu\text{m}$ is used, pushing the flicker-noise corner below 724 Hz. After BSC-DEM at 80 kHz and subsequent decimation filtering, its residual contribution becomes negligible. While a smaller W/L ratio can further reduce thermal noise, it increases the required voltage headroom, leading to a higher supply voltage and power consumption.

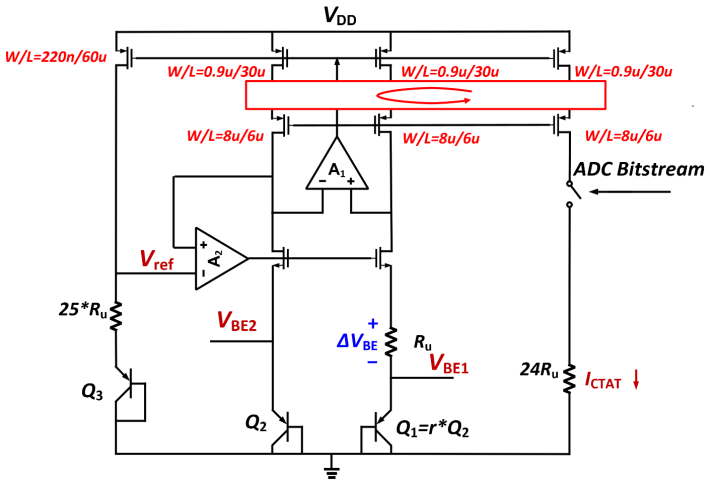

Figure 3.3: Implementation of PMOS current mirror in the front-end.

(4) Leakage: High-temperature substrate leakage must remain sufficiently small to avoid distortion of the mirrored current. With the bulk of the mirror transistor tied to its source, the leakage current exhibits a strong dependence on V_{DS}; hence, the mirror is biased with a drain–source voltage $V_{DS} = 550mV$ at -55°C and $V_{DS} = 750mV$ at 125°C, suppressing the worst-case leakage stays below 2.4pA at 125°C while preserving proper saturation. This worst-case leakage corresponds to less than 1mK of temperature error.

DEM switches are placed between the mirror transistors and their cascodes to avoid large switching transients resulting from the V_{DS} mismatch between the IDAC current mirror ($V_{DD} - V_{BE}$) and the PNP-branch current mirror ($V_{DD} - V_{BE} - V_{DS,\text{NMOS}}$). The switches are implemented using minimum-size

NMOSMVT2V devices to minimize charge injection. The final implementation is shown in Figure 3.3.

3.1.3. Voltage Mirrors

The voltage mirror, implemented using an NMOS pair, biases the PNP loop and forces the PTAT voltage ΔV_{BE} across the resistor. Its design considerations are similar to those of the PMOS current mirrors, which include output impedance, noise, and voltage headroom.

Two device options are available for the NMOS voltage mirror: standard-threshold NMOS (NMOS2V) and medium-threshold NMOS (NMOSMVT2V). Their selection involves a trade-off between output impedance and gate-source capacitance (C_{GS}). NMOS2V devices provide higher output impedance but exhibit larger C_{GS} than NMOSMVT2V. Since both options require amplifier A_1 to use a cascode input stage to achieve sufficient gain, the lower C_{GS} of NMOSMVT2V offers a superior overall frequency response and is therefore preferred.

(1) Output Impedance: The finite gain of the bias amplifier A_1 introduces a voltage mismatch between the NMOS drain nodes, which in turn, causes a source voltage difference that adds a systematic error to ΔV_{BE}. A higher NMOS output impedance attenuates this error and thus relaxes the gain requirement of A_1. However, increasing the channel length to boost output impedance also increases C_{GS}, degrading the loop bandwidth. Therefore, a careful trade-off is required. In the proposed design, the channel length of the NMOS voltage mirrors is chosen as 1 μm, yielding $r_{on} \approx 7.81$ MΩ. With the 55 dB DC gain of A_1, the resulting finite-gain error is suppressed to below 70 mK after trimming.

(2) Flicker and Thermal Noise: The thermal noise of the voltage mirrors decreases with increasing g_m and therefore with larger W/L at a fixed bias current (see Section 2.3). Their flicker noise is shifted towards f_S by the BSC-DEM operation and subsequently suppressed by digital decimation. In this design, the NMOS gate area is chosen as $WL = 30\ \mu\text{m} \times 1\ \mu\text{m}$, which is comparable to the area of the PMOS current sources. This results in a similar flicker-noise corner of approximately 790 Hz. Since this corner frequency is well below the sampling frequency $f_S = 80kHz$, the residual flicker noise after BSC-DEM and digital decimation becomes negligible.

The selected aspect ratio of $W/L = 30\mu\text{m}/1\mu\text{m}$ provides a high $g_m/I_D = 29.41$ and thereby minimizes thermal noise for the given bias current. Further increasing W/L yields negligible noise improvement while substantially increasing C_{GS}, which would degrade the loop gain–bandwidth of the PMOS biasing loop.

(4) Voltage headroom: The headroom is set by $V_{\text{Dsat,n}}$, which decreases as the NMOS W/L increases. With the chosen aspect ratio of $W/L = 30\mu\text{m}/1\mu\text{m}$, the saturation voltage of the NMOS devices is approximately 0.1 V.

The NMOS voltage mirror exhibits an offset of about 1 mV, which would directly corrupt ΔV_{BE} and lead to a temperature error around 3°C. To suppress this, DEM is applied to the NMOS pair, requiring switches at both their drain and source terminals. Using switches on only one terminal would reroute the PTAT-resistor branch to the wrong input of A_1 during swapping, breaking the loop's feedback polarity. The source-side switches are merged with the PNP-DEM switches, as discussed in Section 3.1.6. All switches are implemented with minimum-size NMOSMVT2V devices to minimize charge injection.

3.1.4. PMOS Biasing Loop

The PMOS biasing loop sets the operating point of the PMOS current mirrors while minimizing voltage headroom. As shown in Fig. 3.1, the loop consists of the PMOS current mirrors, NMOS voltage mirrors, PNPs, PTAT resistor, and the PMOS bias amplifier A_1. The implementation of the other blocks has already been discussed, this section focuses on the design of A_1.

Amplifier A_1 must satisfy five main constraints: sufficient DC gain, adequate GBW, low bias current, sufficient input/output swing, and stable phase margin across PVT. The following subsections discuss these requirements and the resulting design choices.

The topology of A_1 is shown in Figure 3.4. A PMOS input pair is used to enable an output swing as low as 200 mV, which allows the W/L of the PMOS current mirror to be minimized for lower noise. Unconventionally, A_1 only employs PMOS cascodes. This choice is driven by device operating regions: the PMOS input pair is biased in weak inversion to maximize loop GBW, requiring large W/L and limited channel length, which reduces intrinsic output resistance and motivates the added cascode. The NMOS load transistors operate in strong inversion with long channels, naturally providing high output impedance without additional cascode devices.

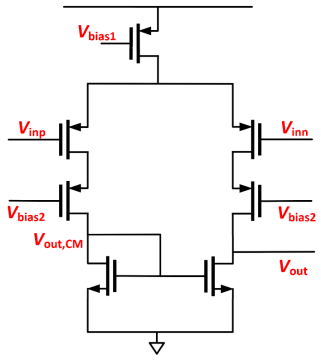

Figure 3.4: Schematic of Biasing Amplifier A_1.

(1) Sufficient DC gain: A high DC gain is required to accurately establish the bias conditions of the PNP front-end and suppress systematic error in ΔV_{BE}. Given the NMOS voltage mirror resistance $r_{\text{on}} = 7.81\ \text{M}\Omega$, the DC gain must ensure that the resulting ΔV_{BE} error remains below 0.1mV. The required gain is approximately

$$A_{\text{DC}} > \frac{V_{\text{out}} - V_{\text{out,CM}}}{V_{\text{error,max}}},$$

corresponding to more than 55dB.

This is achieved using weak-inversion PMOS inputs with $g_m = 1.35\ \mu\text{S}$ and a cascoded output resistance of $r_{op} = 30\ G\Omega$. The NMOS load uses long-channel strong-inversion devices with $r_{on} = 500\ M\Omega$, maximizing gain.

(2) High Gain–Bandwidth Product (GBW): The GBW of A_1 determines the loop gain–bandwidth product (LGBW) of the PMOS biasing loop, which governs the loop's ability to track DEM- and chopping-induced switching transients. From [12], a loop gain-bandwidth product of 120kHz is required. In this loop, the dominant pole is set by the C_{GS} of the PMOS current mirror. Achieving a higher GBW for A_1 therefore requires increasing the transconductance g_m of its input stage, which in turn necessitates both a higher g_m/I_D and sufficient bias current.

Accordingly, the input stage of A_1 is implemented with $W/L = 5\ \mu\text{m}/1\ \mu\text{m}$, achieving $g_m/I_D = 25.9$, and is biased with $I_{\text{PTAT}}/8$. This configuration provides a worst-case GBW of approximately 55 kHz, resulting in a loop gain–bandwidth of 640 kHz, which with an 80 kHz DEM rate ensures that the resulting transient errors remain below 50 mK.

To ensure stability across PVT variations, the PMOS biasing loop is designed with a phase margin above 45°. A 500 fF Miller capacitor and a 1 kΩ zero-nulling resistor are placed between the input and output of A_1 to establish a dominant pole. The zero-nulling resistor positions the left-half-plane zero introduced by the Miller capacitor so that it partially cancels the secondary pole of the loop, as shown in Figure 3.5. This compensation improves phase margin with minimal impact on loop bandwidth, enabling robust stability and fast settling without sacrificing energy efficiency.

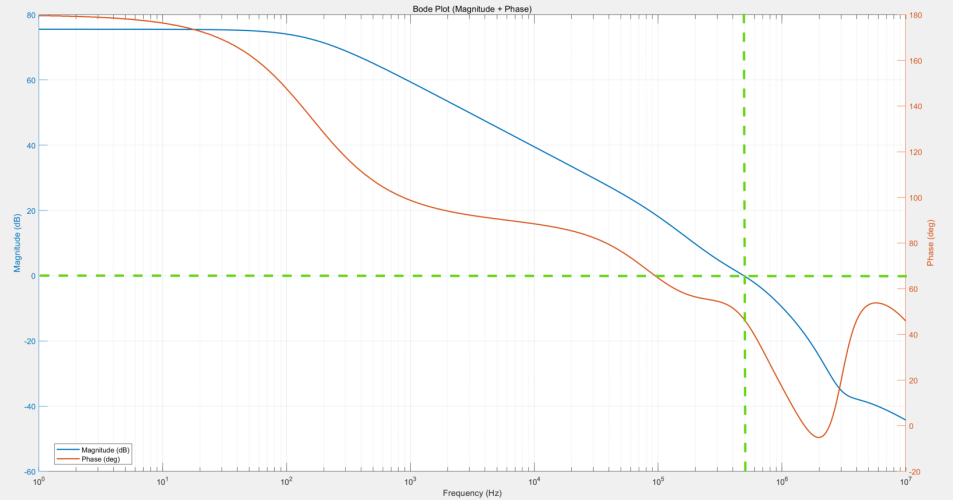

Figure 3.5: Bode plot of the PMOS biasing loop.

(3) Adequate input/output swing: To ensure linear operation across temperature and process corners, the input common-mode range must span $V_{BE} + V_{\text{Dsat,NMOS}}$ from $-55°\text{C}$ to $125°\text{C}$ (608.8mV–928.4mV at 1.5V supply). The output swing must cover the PMOS mirror's gate voltage range (169.7mV–523.6mV). Figure 3.6 shows simulation results confirming sufficient margin across PVT variations.

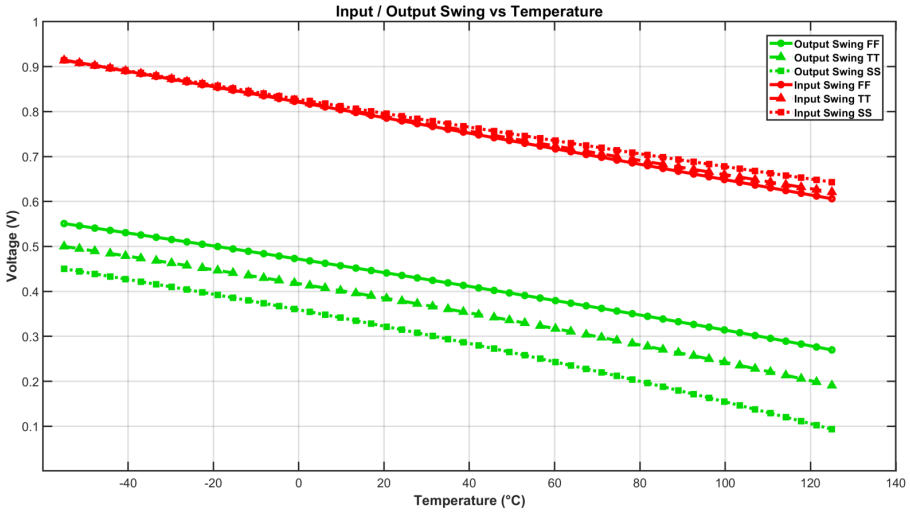

Figure 3.6: Input and output swing of the PMOS bias amplifier A_1.

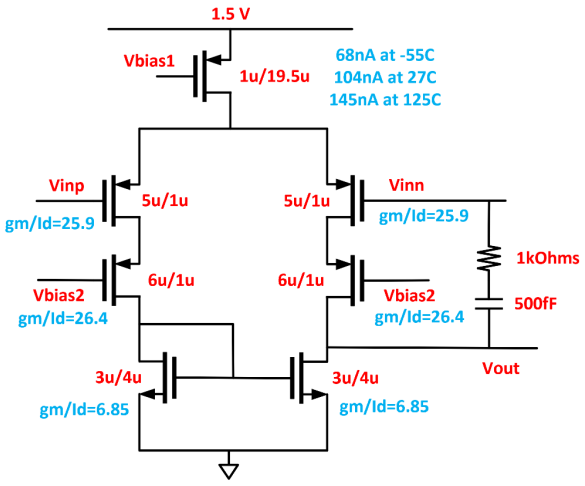

Figure 3.7: Implementation of Biasing Amplifier A_1.

The final implementation of amplifier A_1 is shown in Figure 3.7, with transistor dimensions, g_m/I_D operating points, and bias currents annotated.

3.1.5. NMOS biasing loop

The NMOS biasing loop is designed to establish the gate and drain bias voltages of the NMOS transistors in the voltage mirrors while maintaining the minimum possible voltage headroom. As shown in Figure 3.1, this loop consists of the PMOS current mirror, the NMOS voltage mirror, the reference-voltage–generation branch, the PNP transistors, and the biasing amplifier A_2.

Reference-Voltage–Generation Branch

To implement the reference-voltage–generation branch, the primary design objective is to generate a reference voltage (V_{ref}) that guarantees reliable operation of the front-end across the entire temperature range while maintaining the minimum possible voltage headroom. The upper and lower bounds of the allowable V_{ref} are determined by the biasing requirements of the transistors in the front-end, as shown in Equations (3.3) and (3.4). These boundaries ensure that all devices remain properly biased in their active regions under all process, voltage, and temperature (PVT) conditions.

$$V_{\text{upper,limits}} = V_{DD} - V_{Dsat,CM} - V_{Dsat,CM,cas}. \tag{3.3}$$

$$V_{\text{lower,limits}} = V_{BE} + V_{Dsat,VM}. \tag{3.4}$$

The parameters in (3.3) and (3.4) are defined as follows: $V_{Dsat,CM}$ is the drain–source saturation voltage of the PMOS transistors in the current mirror, $V_{Dsat,CM,cas}$ is that of the cascode PMOS devices, $V_{Dsat,VM}$ is the drain–source saturation voltage of the NMOS transistors in the voltage mirror, and V_{BE} is the base–emitter voltage of the PNP transistor.

As illustrated in Figure 3.8, both the upper and lower limits of V_{ref} exhibit CTAT behavior, decreasing with increasing temperature. Since the upper boundary scales proportionally with the supply voltage

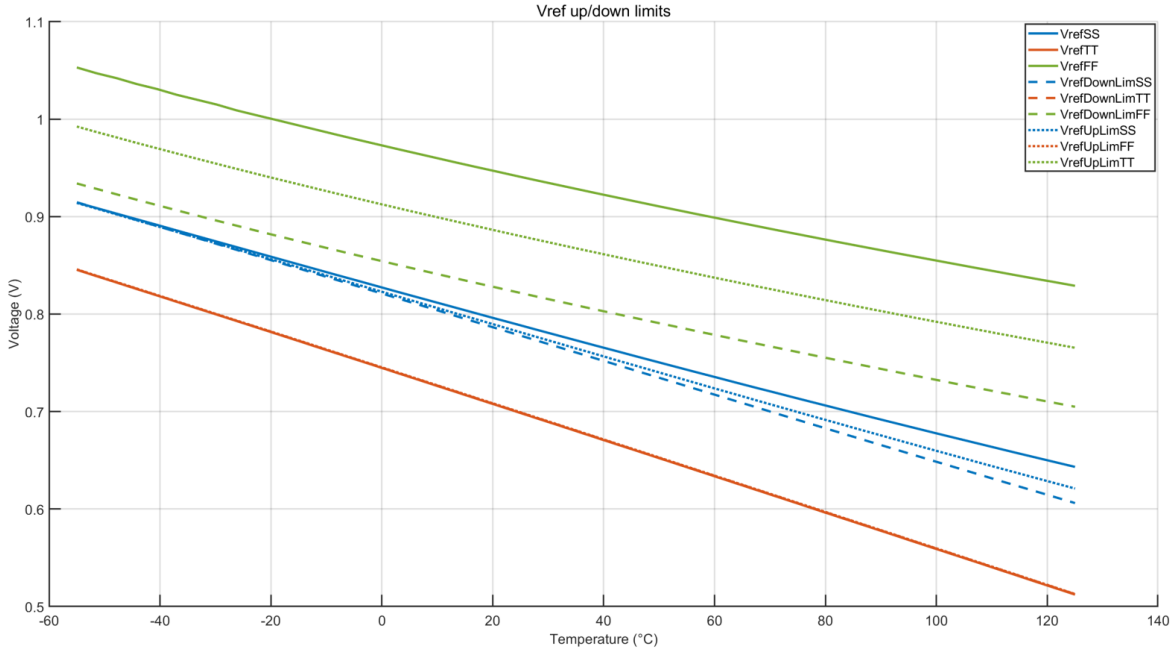

Figure 3.8: Vref, the upper boundary, and the lower boundary at FF, TT, SS corners.

V_{DD}, the design objective is to minimize V_{DD} by positioning V_{ref} as close as possible to the lower boundary while still providing sufficient margin to ensure adequate output impedance in the NMOS voltage mirrors. This allows the front-end to operate with the smallest feasible supply voltage while still ensuring correct transistor biasing.

Consequently, an ideal V_{ref} should satisfy two key conditions that enable the lowest achievable V_{DD}:

1. Temperature dependence: V_{ref} should track the CTAT slope of the lower boundary so that the required headroom remains small across temperature, allowing operation at a lower V_{DD}.
2. Process-corner variation: The corner spread of V_{ref} should be minimized to avoid a worst-case corner dictating a larger V_{DD}, enabling a lower supply voltage and higher energy efficiency.

According to Equation 3.4, the reference voltage V_{ref} is generated by allowing a PTAT current to flow through a series combination of a resistor and a PNP transistor. The PNP, implemented with a $2\ \mu\text{m} \times 2\ \mu\text{m}$ emitter and biased at $I_{PTAT}/10$, produces a V_{BE} that closely tracks the $5\ \mu\text{m} \times 5\ \mu\text{m}$ PNPs used in the front-end, while its small emitter area allows similar V_{BE} at lower current. The series resistor of $25R_{PTAT}$ converts the PTAT current into a PTAT voltage whose temperature dependence matches that of $V_{Dsat,VM}$. The sum of the resistor voltage and the PNP V_{BE} therefore forms a V_{ref} that follows the lower boundary across temperature and remains close to it while preserving sufficient headroom for reliable NMOS-mirror saturation. In addition, using a PNP—biased with a PTAT current—provides a V_{BE} with much smaller corner spread than the V_{GS} of a MOSFET, improving corner stability and saving roughly 200 mV of headroom compared with a MOS-based implementation.

Implementation of amplifier A_2

Amplifier A_2 functions as an error amplifier that continuously compares the reference voltage V_{ref} with the drain voltage (V_{inn}) of the NMOS pair. Its output drives the gates of the NMOS transistors, adjusting their gate voltage until the drain voltage precisely matches V_{ref}.

For the design of amplifier A_2, the key parameters considered are DC gain, gain–bandwidth product (GBW), power consumption, and input/output voltage swing.

(1) Sufficient DC gain: The DC gain of A_2 determines how accurately the drain voltages of the NMOS voltage mirror can be biased to the reference voltage V_{ref}. However, because the drain voltage of the NMOS pair only slightly affects their operating point parameters (g_m, V_{TH}, and r_{out}) due to the high output impedance of the devices, the required biasing accuracy—and thus the gain requirement of A_2—can be relatively relaxed. In this design, a DC gain of approximately 40 dB is sufficient, which can be easily achieved using a single-stage five-transistor operational transconductance amplifier (5T-OTA) topology.

(2) High gain–bandwidth product (GBW): A sufficiently large GBW is also required to ensure fast loop settling. In the proposed architecture, the PMOS and NMOS biasing loops are coupled; therefore, the NMOS biasing loop must be designed with a much higher loop gain bandwidth than the PMOS biasing loop to prevent it from limiting the overall transient response. Consequently, the worst-case GBW of A_2 is chosen 18.6kHz, resulting a worse-case loop gain bandwidth 2192.8kHz, which is around 3.5× higher than that of PMOS biasing loop.

(3) Minimized bias current: The power consumption of A_2 is primarily determined by the required GBW. With the target GBW 18.6kHz, a bias current of $I_{\text{PTAT}}/10$ is used, which is enough to achieve the target loop gain bandwidth.

(4) Adequate input/output swing: The input and output voltage swings of A_2 are determined by the drain and gate voltage variations of the NMOS voltage mirror over the entire temperature range. The input voltage, corresponding to the drain voltage of the NMOS pair, varies from 608.8 mV to 928.4 mV. The output voltage, which drives the gate of the NMOS pair, varies from 684.1 mV to 1.29 V. To accommodate these voltage ranges under a 1.5 V supply while maintaining sufficient voltage headroom, a 5T-OTA topology with an NMOS input stage is adopted.

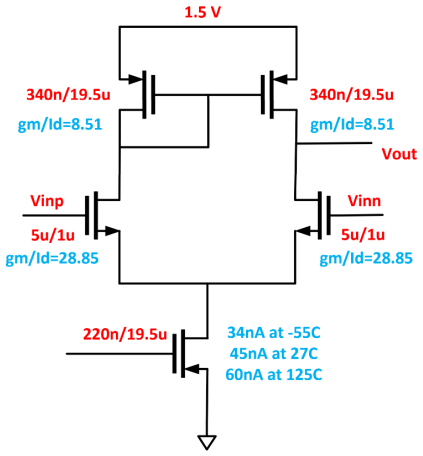

Figure 3.9: Schematics of the biasing amplifier A_2 for voltage mirror.

Figure 3.9 shows the schematic of the implemented amplifier A_2, with the device dimensions, g_m/I_D efficiencies, and bias currents of all transistors indicated.

3.1.6. BJT and NMOS Swap Circuitry

In the proposed design, two sets of DEM switches exist in the PNP loop: one for NMOS DEM and one for PNP DEM. Their R_{on} mismatch introduces error in the generated ΔV_{BE}. Prior work [12] only required one set of switches and used clock boosting to reduce R_{on}. With two sets, the accumulated R_{on} mismatch would be excessive. To resolve this, the two sets of switches are merged through a modified DEM scheme, eliminating the extra resistance imbalance between the NMOS and PNP branches and thereby suppressing ΔV_{BE} distortion while preserving full DEM functionality.

The challenge is illustrated in Figure 3.10. The X-controlled switch sets located after NMOS1 and NMOS2 interact differently with the A–H controlled switch set, preventing a direct merging of the two networks.

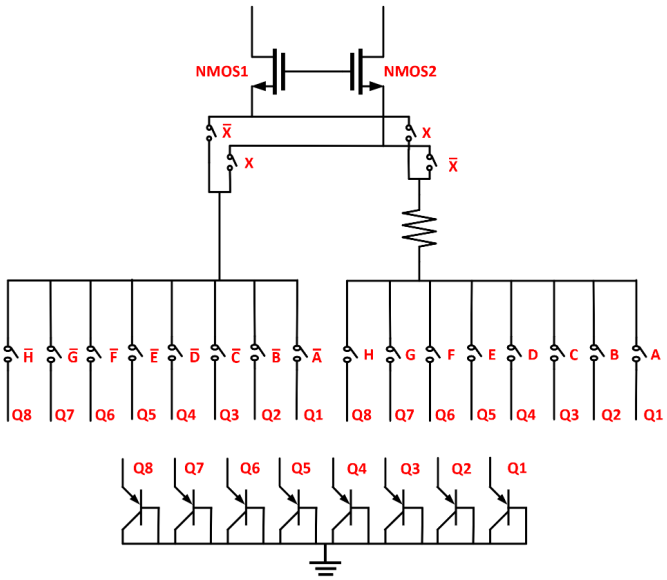

Figure 3.10: The two NMOS branches with two separated switch groups

To enable a correct one-to-one mapping between X-controlled switch sets and A - H controlled switch set, the subsystem consisting of the PTAT resistor, the shorted interconnect, and the A–H controlled switches must be duplicated. Once duplicated, the two switching paths become fully independent, allowing each set of X-controlled switches to be merged locally with its corresponding A–H controlled switches. The resulting modified DEM structure is shown in Figure 3.11.

With this merged topology, the ΔV_{BE} error induced by both R_{on} mismatch and R_{off} leakage is reduced by approximately half. The DEM switches are implemented using minimum-size NMOS devices ($W/L = 220\,\text{nm}/180\,\text{nm}$) to minimize charge injection. Under clock boosting—implemented by driving the switches with a $2V_{\text{DD}}$ gate voltage— r_{on} is reduced to about 5 kΩ (with $r_{\text{off}} = 75$ GΩ at 125°C). As a result, the temperature error is suppressed below 80 mK.

In this modified DEM scheme, the single R_{PTAT} used is duplicated. Mismatch between the two R_{PTAT} resistors therefore introduces a spread in the generated I_{PTAT}. However, this mismatch does not directly translate into temperature error. What ultimately determines accuracy is the ratio $R_{\text{CTAT}}/R_{\text{PTAT}}$, since these two resistors set the relative scaling of V_{BE} and ΔV_{BE} in the PTAT/CTAT current domain. As shown in [1], the effect of resistor mismatch in this ratio can be accurately measured and compensated

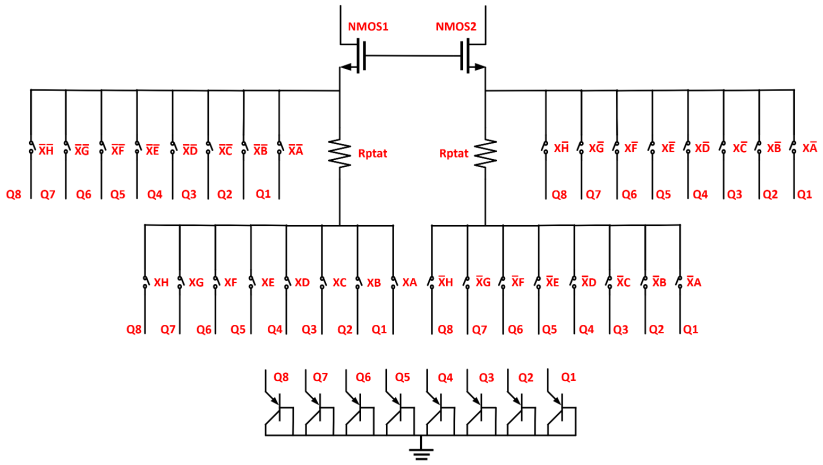

Figure 3.11: Final DEM switch implementation combining the two switch groups.

in the digital domain, reducing the resulting temperature error to below 0.1°C. By applying the same calibration procedure, the mismatch between the duplicated R_{PTAT} and the R_{CTAT} can likewise be corrected, so the duplication of R_{PTAT} does not compromise overall accuracy.

3.2. Delta-Sigma Modulator

3.2.1. DSM Topology

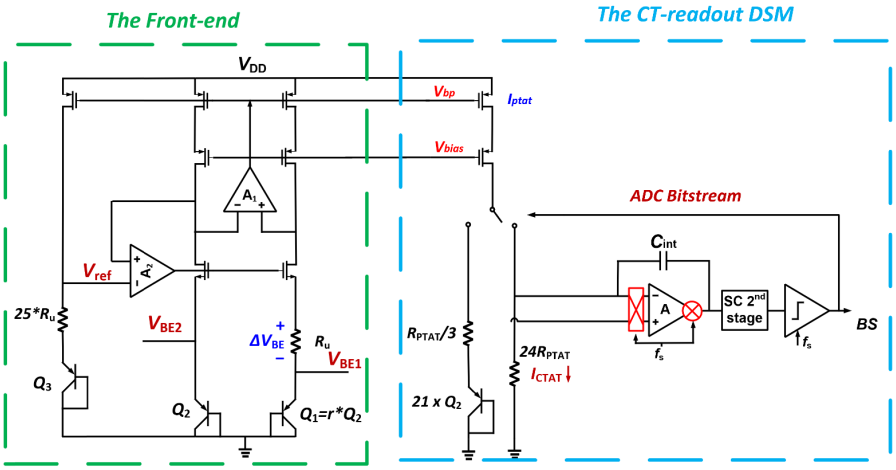

Figure 3.12: Schematics of the CT-readout DSM reused in [12].

In this work, the CTDSM architecture reported in [12] is reused for fair comparison, as illustrated in Figure 3.12. The adopted modulator employs a second-order feed-forward topology with an oversampling ratio (OSR) of 3072. Under these conditions, the quantization noise is suppressed negligible with an acceptable conversion time of 40 ms for a sampling frequency of 80 kHz. The feed-forward configuration is chosen because it reduces the signal swing at the output of the first integrator, thereby minimizing distortion and enhancing modulator stability [14].

3.3. Power and noise analysis

Table 3.1 summarizes the simulated thermal noise contributions (referred to ΔV_{BE}) and the current consumption of the proposed design at room temperature (27 °C). As expected, the DSM contributes significantly less noise and power consumption compared to the sensor front-end, demonstrating that the overall performance is predominantly limited by the analog front-end circuitry.

Table 3.1: Table comparing the noise performance and current consumption of the circuit components.

Subcircuit	Component	Noise ($\mathrm{nV}/\sqrt{\mathrm{Hz}}$)	Noise power contribution (%)	Consumed current (μA)	Current usage (%)
Front-end	BJTs	33.34	16	(BJTs: 1.17)	(BJTs: 46.8)
	PTAT resistor	45.67	30		
	CTAT resistor	16.76	4		
	Current mirrors	36.48	20		
	Voltage mirrors	44.35	29.6		
	Bias opamps	–	–	0.29	11.6
DSM	1^{st} integrator	5.02	0.4	0.78	31.2
	2^{nd} integrator	–	–	0.26	10.4
Full circuit		83.4	100	2.5	100

The thermal noise floor of the total circuit, referred to ΔV_{BE}, is 83.4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, which corresponds to a temperature noise of 0.264 $\mathrm{mK}/\sqrt{\mathrm{Hz}}$ based on the temperature sensitivity equation of ΔV_{BE} reported in [13]. The simulated supply current and voltage are 2.5 μA and 1.5 V, respectively, resulting in a total power consumption of 3.75 μW.

As discussed in the previous chapter, the proposed architecture replaces the power-hungry biasing amplifier of [1] with an NMOS voltage mirror and a set of low-power biasing amplifiers. Although this increases the total front-end noise power by about 20%, it enables a substantial reduction in energy consumption—from 16.15 μW in [1] to 3.75 μW in this work.

As a result, the resolution of the proposed design is limited by the higher front-end noise—stemming from (1) the use of a 7:1 emitter-area ratio, which increases the BJT thermal noise, and (2) the replacement of the low-noise biasing amplifier by an NMOS voltage mirror, whose noise contribution is slightly larger than that of A_1—yielding a simulated resolution of 1.97 mK versus the 1.1 mK achieved in [1]. Using this resolution, the estimate of the figure of merit (FoM) becomes

$$\mathrm{FoM}_{\mathrm{proposed}} = (1.97\ \mathrm{mK})^2 \times 2.5\ \mu\mathrm{A} \times 1.5\ \mathrm{V} \times 38.4\ \mathrm{ms} \approx 558\ \mathrm{fJ} \cdot \mathrm{K}^2.$$

Compared to the 850 $\mathrm{fJ} \cdot \mathrm{K}^2$ FoM reported in [1], this represents an improvement of roughly 1.5×.

3.4. Summary

This chapter covered the realization of the major circuit blocks in the sensor, focusing on the BJT front-end and the DSM architecture. The corresponding analyses of power usage and noise sources were also included. In the next chapter, the simulated performance of the designed CMOS temperature sensor will be explored in detail.

4

Simulation results

4.1. Resolution

Figure 4.1 shows the simulated temperature resolution as a function of conversion time, evaluated for integer multiples of the sinc^2 window length. The curve is obtained from a bitstream of 2400000 bits and converted to temperature resolution using a room-temperature sensitivity of 280 K. As shown, the proposed design reaches a resolution of 1.97 mK at a total conversion time of 38.4 ms. This conversion time corresponds to exactly two full periods of the PNP dynamic-element-matching (DEM) cycle used in the front end, ensuring that DEM-induced mismatch and ripple are fully averaged out in each measurement.

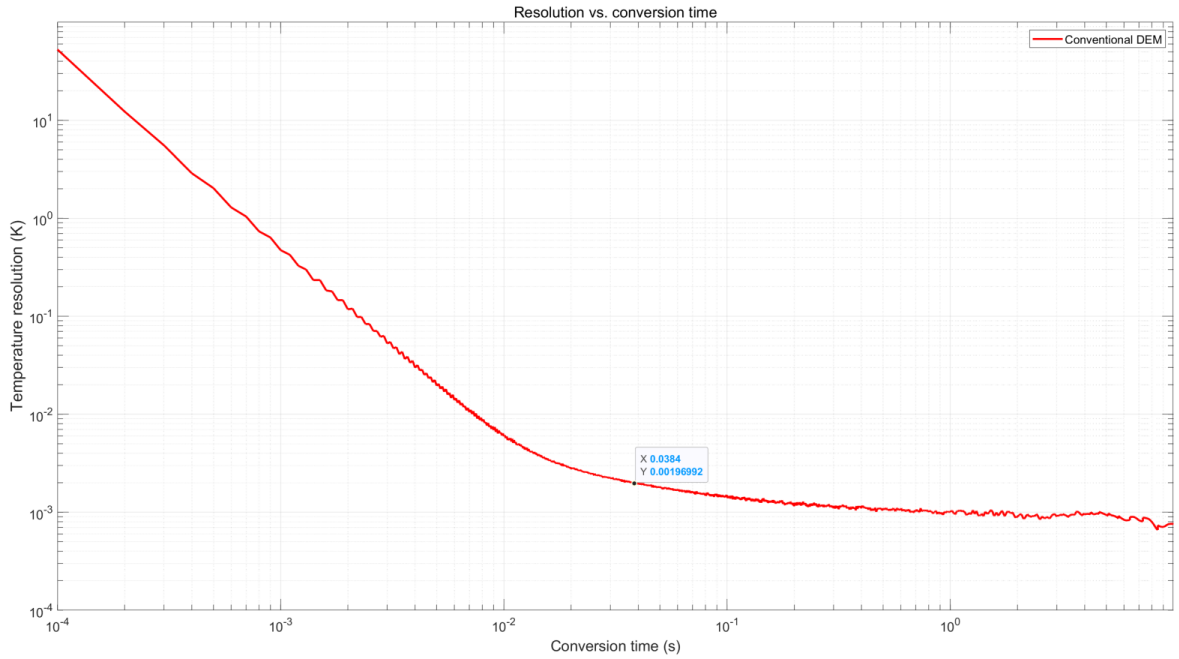

Figure 4.1: Plot: Resolution over conversion time at 300K

For comparison, the design reported in [1] attains a 1.1 mK resolution at a similar conversion time of 40 ms. Although the proposed design exhibits approximately 1.78× worse resolution, its power consumption is only one-fifth that of [1], resulting in a significantly improved energy efficiency.

The reduced resolution of the proposed design can be directly attributed to its higher front-end noise. Two factors explain this increase. First, the use of a 7:1 emitter-area ratio raises the thermal noise of the PNP pair, as both devices now are biased with same current and contribute comparable amounts of noise. Second, the NMOS voltage mirror used in the proposed CVM biasing scheme generates more noise than the biasing amplifier A_1 in [1]. Together, these effects lead to a higher PTAT-current noise level, and thus a lower achievable resolution compared to [1].

The resulting figure of merit (FoM) of the proposed design is calculated as

$$\text{FoM}_{\text{proposed}} = P_{\text{total}} \times \text{Resolution}^2 \times \text{Conversion Time} = 0.558 \text{ pJ·K}^2,$$

representing approximately 1.5× improvement over the 0.850 pJ·K^2 achieved by the design in [1].

4.2. Power Supply Sensitivity

The variation in temperature accuracy as the supply voltage is swept from 1.5 V to 2.2 V is shown in Figure 4.2. For each supply voltage, a full transient Monte-Carlo simulation was performed over the entire temperature range (−55°C to 125°C), and the maximum temperature error after one-point trim obtained across all samples and temperatures is reported. As shown, the accuracy degrades significantly when the supply voltage deviates from its nominal value. In particular, the temperature inaccuracy exceeds 0.1°C when the supply voltage drops below 1.5 V or rises above 1.8 V.

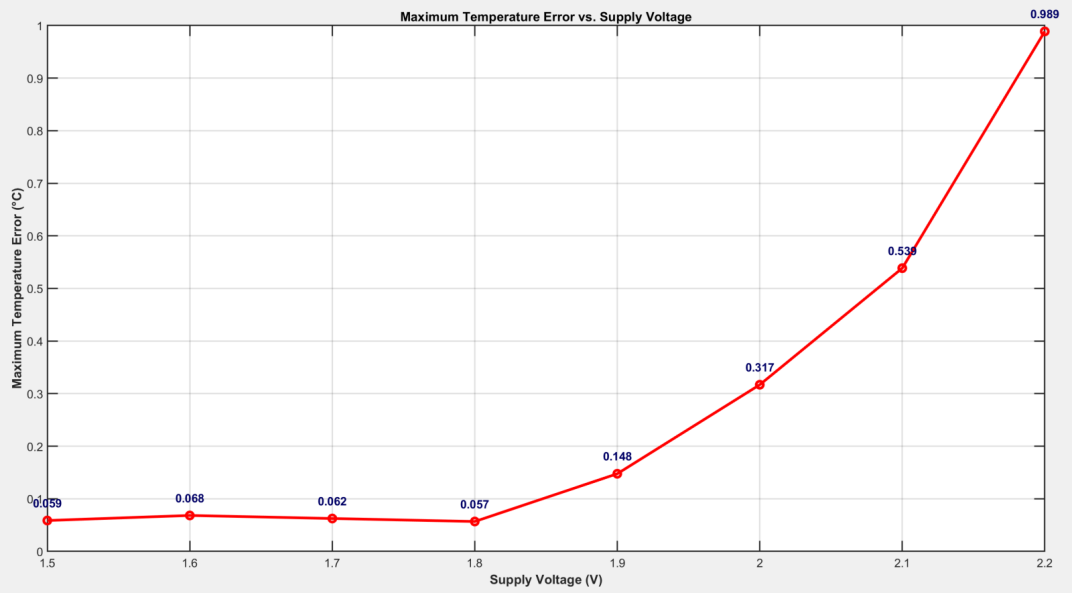

Figure 4.2: Plot: The maximum temperature error over supply 1.4V to 2.2V

When the supply voltage exceeds 1.8 V, the gate voltage of the PMOS current mirror also increases, requiring the PMOS biasing amplifier A_1 to generate a higher output voltage, as shown in Figure 3.3. However, as discussed in Section 3.1.4, amplifier A_1 employs a PMOS input stage, which inherently limits its upper output swing. When the required output voltage approaches this limit, the input stage

of A_1 moves out of its saturation region and into the linear region, reducing the effective gain of the amplifier. The resulting finite-gain error again manifests in ΔV_{BE}, leading to a deterioration in overall temperature accuracy.

4.3. Accuracy

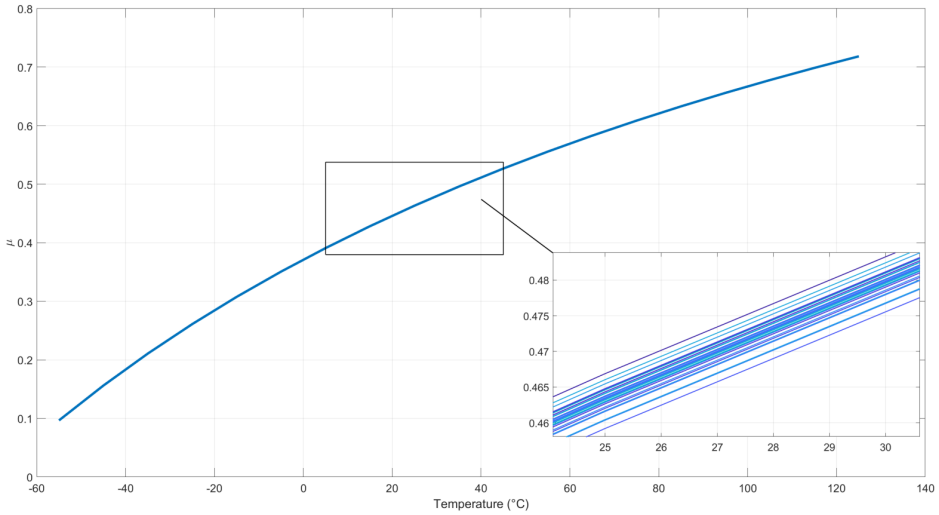

Figure 4.3: Raw output (μ) of the sensors over 3 temperatures (-55°C, 27°C, 125°C)

Figure 4.3 shows the averaged bitstream value (μ) obtained from transient Monte Carlo simulations with 30 samples. Both process-corner variations (representing batch-to-batch spread) and device mismatch (representing die-to-die spread) are included in the analysis. For simplicity, the temperature is swept from -55°C to 125°C with a step of 10°C. The μ values are then converted into temperature using Equations 2.8–2.10, with fitting parameters $\alpha = 11.9892$, $A = 635.2000$, and $B = -281.2099$.

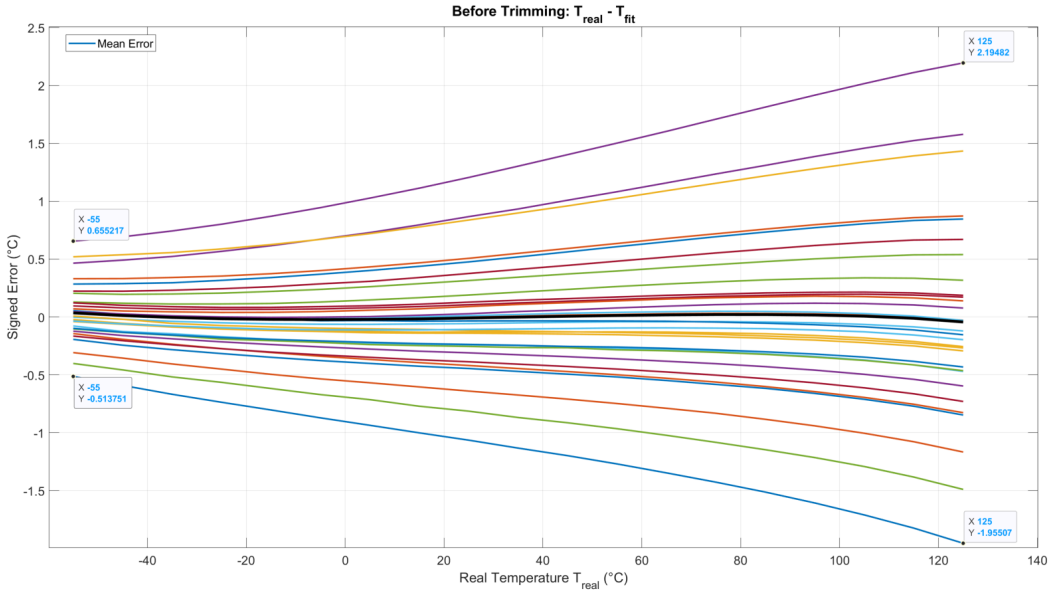

Figure 4.4: Accuracy of the temperature sensor before trim

Figure 4.4 presents the temperature error before trimming. As can be observed, the temperature spread exhibits a proportional-to-absolute-temperature (PTAT) behavior, which is set by variations

in the transistor saturation current I_S. At 125°C, the 3σ inaccuracy is approximately ±2.2°C. This variation can be effectively compensated through PTAT trimming, which can be implemented either by adjusting circuit parameters at the physical level [7] or by applying digital post-processing to the sensor output [15].

As reported in [7], when the analog-to-digital converter (ADC) output is defined as $X = V_{BE}/\Delta V_{BE}$, the PTAT spread caused by variations in I_S manifests as an offset shift in the bitstream average μ. Therefore, applying an offset trim can effectively cancel the spread in V_{BE}.

The same principle applies to the proposed BJT-based temperature sensor, whose output represents a scaled version of X, as shown in equation 4.1:

$$\mu = 1 - \frac{I_{\text{CTAT}}}{I_{\text{PTAT}}} = 1 - \frac{X}{m}, \quad \text{where } m = \frac{R_2}{R_1},\ X = \frac{V_{BE}}{\Delta V_{BE}}. \tag{4.1}$$

Therefore, a C-parameter trimming scheme is employed to maximally calibrate the PTAT error. This relationship is expressed in equation 4.2, where C serves as the trimming parameter that ensures all sensors output exactly 27°C at room temperature.

$$\mu_{\text{lin}} = \frac{\alpha}{\alpha + m(1 - (\mu + C))}, \tag{4.2}$$

As shown in Figure 4.5, the calibration effectively compresses the temperature spread, resulting in a 3σ inaccuracy of approximately ±0.1°C over the −55°C to 125°C range.

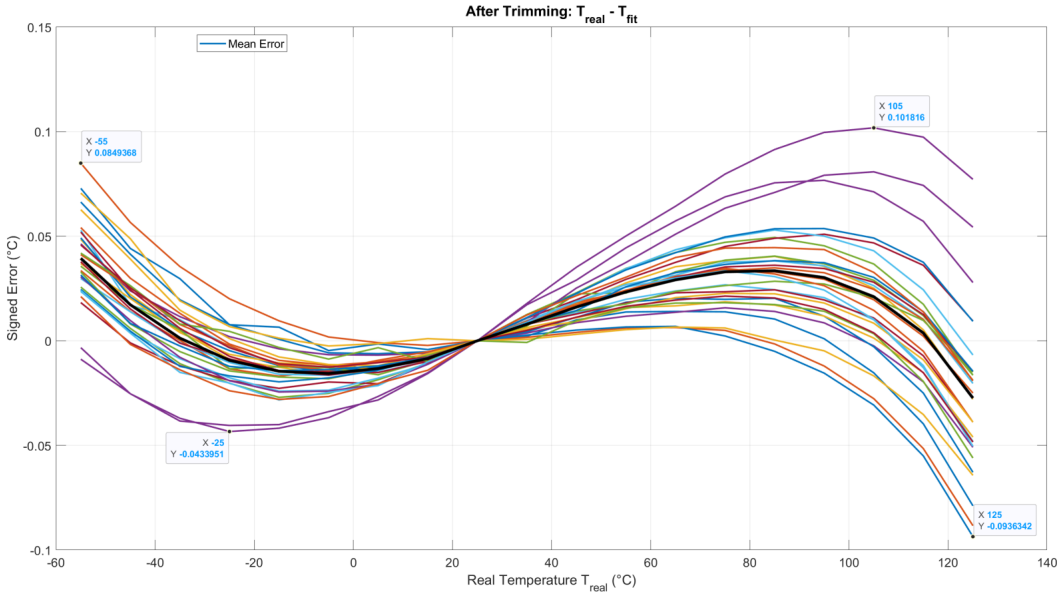

Figure 4.5: Accuracy of the temperature sensor after trim

4.4. Summary

Table 4.1 presents a summary of the performance of the proposed BJT-based temperature sensor, along with a comparison to other state-of-the-art low-power BJT implementations. As shown, the proposed design achieves a state-of-art figure of merit (FoM) of $0.43pJ \cdot K^2$, while maintaining a comparable

accuracy of 0.1°C (3σ) over the military temperature range from -55°C to 125°C.

Table 4.1: Performance summary and comparison to the state-of-the-art

Parameter	JSSC'17 [7]	JSSC'25 [16]	JSSC'25 [1]	JSSC'24 [12]	ISSCC'25 [17]	This work
Sensor type	PNP	PNP	PNP	NPN	NPN	PNP
Architecture	DTΔΣM	DTΔΣM	CTΔΣM	CTΔΣM	CTΔΣM	CTΔΣM
Technology [µm]	0.16	0.022	0.18	0.18	0.18	0.18
Chip area [mm^2]	0.16	0.01	0.12	0.07	0.05	–
Supply current [µA]	4.6	3.625	9.5	2.5	1.8	2.5
Supply voltage [V]	1.5–2.0	0.8-1.1	1.7–2.2	1.4–2.2	1.4–2.2	1.5–1.8
Temperature range [°C]	-55–125	-40–125	-55–125	-55–125	-55–125	-55–125
3σ Inaccuracy [°C]	±0.06	±0.4	±0.1	±0.1	±0.1	±0.1
Resolution [mK]	15	4.7	1.1	1.22	0.79	1.97
Conversion time [ms]	5	6.4	40	38.4	51	38.4
Resolution FoM [$pJ{\cdot}°C^2$]	7.8	0.41	0.85	0.2	0.08	0.56

5

Conclusion and Future work

5.1. Conclusion

In this work, an energy-efficient PNP-based BJT temperature sensor employing a loop-biased, symmetrically matched current–voltage mirror (CVM) has been designed, analyzed, and verified through simulation. The proposed architecture enhances the energy efficiency of PNP-based temperature sensors while maintaining high accuracy across the full military temperature range. The key contribution of this work is the introduction of the loop-biased symmetrically matched CVM, which replaces the power-hungry biasing amplifier (A_1) used in the state-of-the-art design [1]. This modification enables the front end to achieve comparable noise performance with less than one-quarter of the power consumption. Combined with extensive use of dynamic error-suppression techniques, the proposed sensor offers significantly improved energy efficiency over amplifier-biased PNP designs [1], while still maintaining competitive accuracy and temperature range. Overall, this work demonstrates that a CVM-biased front-end can significantly improve the energy–resolution trade-off of PNP-based temperature sensors, providing a solid basis for future ultra-low-power precision sensing systems.

5.2. Future Work

5.2.1. Better Energy Efficiency

Noise power spectral density reduction

Although the proposed CVM-based front end eliminates the power-hungry biasing amplifier of [1], the NMOS voltage mirror remains a significant noise contributor, accounting for nearly 30% of the total PTAT-current noise and ultimately limiting the achievable resolution.

A straightforward improvement is to replace the medium-threshold NMOSMVT2V devices used in the voltage mirror with standard-V_T NMOS transistors of identical dimensions. Device simulations indicate that this substitution reduces the intrinsic thermal noise of the mirror by roughly a factor of two while keeping g_m and r_o essentially unchanged, as summarized in Table 5.1.

For standard NMOS devices, the intrinsic current thermal noise decreases with increasing channel length

Table 5.1: Comparison between NMOSMVT2V and NMOS2V (same size 30u/1u)

Device	g_m	I_{bias}	g_{mb}	$g_{ds} = 1/r_o$	Noise $[A^2]^1$	Noise to I_{PTAT} $[A^2]^2$
NMOSMVT2V (30u/1u)	11.37u	386.747n	2.213u	128n	19×10^{-26}	11.4×10^{-26}
NMOS2V (30u/1u)	10.88u	386.725n	2.52u	111.38n	8.8×10^{-26}	5.54×10^{-26}

[1] Intrinsic drain current thermal noise of a single NMOS.

[2] Combined noise contribution of two NMOS voltage mirrors to I_{PTAT}.

while maintaining the same W/L and bias current, as shown in Table 5.2. This is because short-channel effects—such as velocity saturation—elevate the effective channel noise, whereas longer devices exhibit lower thermal noise [18].

Table 5.2: Comparison among NMOS2V devices of various sizes

Device	g_m	I_{bias}	g_{mb}	$g_{ds} = 1/r_o$	Noise $[A^2]^1$	Noise to I_{PTAT} $[A^2]^2$
NMOS2V (5.4u/180n)	10.416u	386.717n	2.3u	724n	15×10^{-26}	9.6×10^{-26}
NMOS2V (30u/1u)	10.88u	386.725n	2.52u	111.38n	8.8×10^{-26}	5.54×10^{-26}
NMOS2V (60u/2u)	10.63u	386.718n	2.45u	75.81n	7.5×10^{-26}	5.0×10^{-26}
NMOS2V (90u/3u)	10.48u	386.772n	2.41u	63n	7.0×10^{-26}	4.8×10^{-26}

[1] Intrinsic drain current thermal noise of a single NMOS.
[2] Combined noise contribution of two NMOS voltage mirrors to I_{PTAT}.

The main limitation on further increasing the device length arises from the associated parasitic capacitances, particularly C_{gd}, which sets the second pole of the PMOS-biasing loop and limits the achievable loop-gain bandwidth when Miller compensation is applied. In addition, the intrinsic noise reduction obtained from enlarging the device dimensions exhibits diminishing returns, making aggressive device-length scaling ineffective.

Based on these considerations, the medium-threshold NMOSMVT2V devices were replaced by standard-NMOS2V devices with $W/L = 30\ \mu\text{m}/1\ \mu\text{m}$. This modification reduces the overall PTAT-current noise power spectral density from 0.4031 pA^2/Hz to 0.3419 pA^2/Hz, corresponding to an improvement of approximately 15%, as summarized in Table 5.3.

Table 5.3: Overall noise power comparison between the NMOS2V voltage mirrors and NMOSMVT2V voltage mirrors

Noise Source	NMOS2V $30\mu\text{m}/1\mu\text{m}$ (pA^2/Hz)	NMOSMVT2V $30\mu\text{m}/1\mu\text{m}$ (pA^2/Hz)
Current mirrors	0.0945	0.0933
Voltage mirrors	0.055	0.113
Resistors	0.1269	0.127
BJTs	0.0655	0.0698
Total	0.3419	0.4031

Noise bandwidth reduction

Even with the noise reduction described above, the achievable resolution of the proposed architecture is limited by the way the CTDSM integrates the PTAT current. In a CTDSM, the input-referred thermal-noise bandwidth is inversely proportional to the integration time. In the current design, however, I_{PTAT}

is only integrated during the "0" phases of the ADC bitstream. This restricts its effective integration time for a given conversion period, resulting in a higher noise bandwidth and a lower $SNR_{I_{\mathrm{PTAT}}}$.

Since ΔV_{BE} is an order of magnitude smaller than V_{BE}, the SNR of I_{PTAT} is much lower than that of I_{CTAT}. As a result, the overall SNR at the DSM output is dominated by the SNR of I_{PTAT}.

To achieve better energy efficiency, a recent work [17] introduced an I_{CTAT} DAC in which the bitstream-controlled switching network is moved from the PTAT branch to the CTAT branch, as illustrated in Figure 5.1. This approach maximizes the integration time of I_{PTAT} and thereby minimizes its noise bandwidth. Incorporating a similar I_{CTAT} DAC into the proposed architecture—replacing the existing $1 \times I_{\mathrm{PTAT}}$ DAC—would allow a significantly longer integration window for the PTAT current. This would reduce its noise bandwidth, increase the SNR of I_{PTAT}, and thus improve the overall resolution of the sensor.

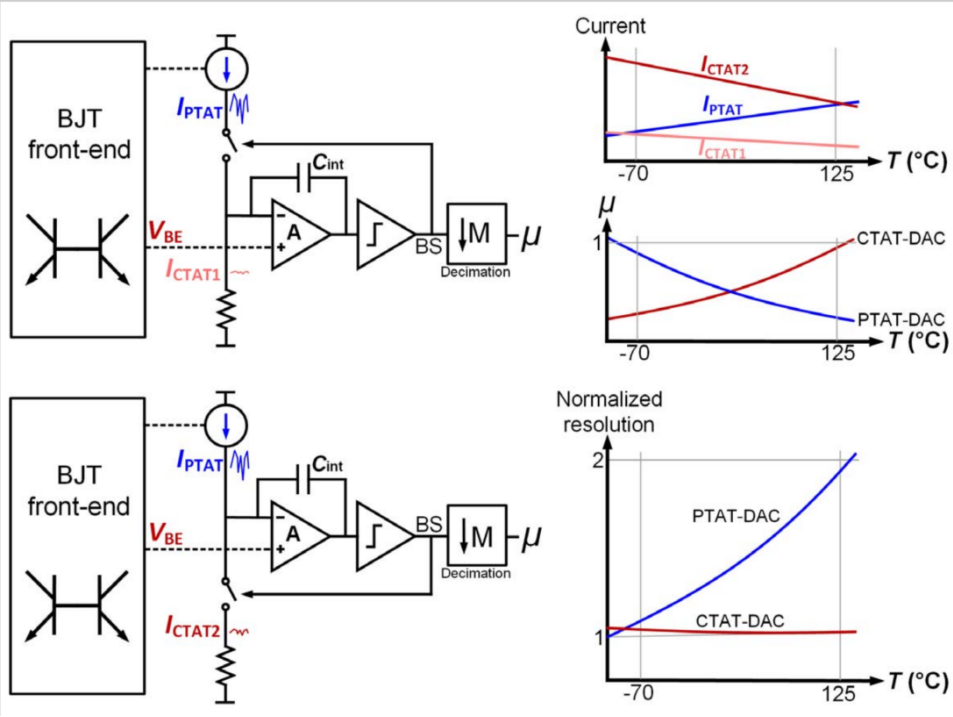

Figure 5.1: Topology of the I_{CTAT} DAC proposed in design [17]

6

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