Design of a High Voltage Arbitrary Wave Shape Generator for Dielectric Testing

Ganeshpure, D.A.

DOI
10.4233/uuid:0a34b7ef-d18b-4f86-be16-62128a52dd7c

Publication date
2024

Document Version
Final published version

Citation (APA)
Ganeshpure, D. A. (2024). *Design of a High Voltage Arbitrary Wave Shape Generator for Dielectric Testing*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:0a34b7ef-d18b-4f86-be16-62128a52dd7c

Design of a High Voltage Arbitrary Wave Shape Generator for Dielectric Testing

Design of a High Voltage Arbitrary Wave Shape Generator for Dielectric Testing

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates to be defended publicly on
Wednesday, 10 January 2024 at 15:00 o'clock

by

Dhanashree Ashok Ganeshpure

Master of Science in Electrical Engineering,
Delft University of Technology, The Netherlands.
Born in Akola, India

This Dissertation has been approved by the promotors.

Composition of the Doctoral Committee:

Rector Magnificus	Chairperson
Prof. ir. P.T.M. Vaessen	Delft University of Technology, promotor
Prof. dr. ir. P. Bauer	Delft University of Technology, promotor
Dr. M. Ghaffarian Niasar	Delft University of Technology, copromotor

Independent members:

Prof. dr. ir. M. Popov	Delft University of Technology
Prof. dr. ir. G. Rietveld	University of Twente
Prof. dr. G. Burt	University of Strathclyde, UK
Dr. C.A. Plet	DNV, Canada
Prof. dr. ir. A.H.M. Smets	Delft University of Technology, reserve member

This research work is sponsored by KEMA Laboratories, Arnhem, The Netherlands.

Printed by:

ISBN 000-00-0000-000-0

An electronic version of this dissertation is available at
http://repository.tudelft.nl/.

|| श्री ||

माझ्यावर निरपेक्ष प्रेम करण्यारा आणि मला
सदैव पाठिंबा देणाऱ्या, माझ्या प्रिय
आई आणि बाबांना हा प्रबंध समर्पित!!

CONTENTS

List of Abbreviations

APS	Auxiliary Power Supply
APOD	Alternate Phase Opposition Disposition
AWG	Arbitrary Wave shape Generator
CHB	Cascaded H Bridge
DAC	Damped Alternating Current
DSP	Digital Signal Processor
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EU	European Union
ESP	Electrical Sustainable Power
FPGA	Field Programmable Gate Array
FRT	Fault Ride Through
HV	High Voltage
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
KVL	Kirchhoff's Voltage Law
LCC	Line Commutated Converters
LI	Lightning Impulse
LPIT	Low Power Instrument Transformer
LSC	Level Shift Control
LV	Low Voltage
MMC	Modular Multilevel Converter
MV	Medium Voltage
NLC	Nearest Level Control
NPT	Non Punch Through

NPC	Neutral Point Clamp
PD	Partial Discharge
PE	Power Electronics
POD	Phase Opposition Disposition
PCB	Print Circuit Board
PCIe	Peripheral Component Interconnect Express
PSC	Phase Shift Control
PT (Chp 2)	Potential Transformer
PT (Chp 5)	Punch Through
PWM	Pulse Width Modulation
RES	Renewable Energy Sources
SHE	Selective Harmonic Elimination
SI	Switching Impulse
SiC MOSFET	Silicon Carbide Metal Oxide Semiconductor Field-Effect Transistor
SM	Submodule
SPC	Standard Processing Cores
SST	Solid State Transformer
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
TO	Test Object
TOV	Transient Over Voltages
VLF	Very Low Frequency

LIST OF SYMBOLS

η	Voltage efficiency of the Marx generator
η_{APS}	Power efficiency of the APS
α_1	Time constant which decides the tail time of the LI waveform
α_2	Time constant which decides the front time of the LI waveform
a	Slope of the the average modulation index ($n_{u,l}$) during the soft start-up
C_1	Equivalent input capacitance for Marx generator
C_2	Equivalent output capacitance for Marx generator
C_b	Coupling capacitor
C_{cable}	Capacitance of MV Cable
$C_{CB(a)}$	Capacitance of MV circuit breaker: between contacts
$C_{CB(b)}$	Capacitance of MV circuit breaker: between contact and Tank
C_{CT}	Capacitance of MV current transformer
C_{DC}	DC-link capacitance
C_{eqv}	Equivalent capacitance in the circulating current circuit
C_{HG}	Capacitance of MV distribution transformer: between HV winding and ground
C_{HL}	Capacitance of MV distribution transformer: between HV and LV winding
C_{load}	Load capacitance
C_{LG}	Capacitance of MV distribution transformer: between LV winding and ground
C_{PT}	Capacitance of MV potential transformer
C_s	Submodule capacitance
C_{se}	Additional input capacitance
C_{TO}	Capacitance of test object (general)
C_{turn}	Capacitance of MV distribution transformer: between turns
d	Decimal part of the average modulation index ($n_{u,l}$)
F_s	Switching frequency of the semiconductor devices
$f_{1\%error}$	Large-signal bandwidth
f_{3dB}	Small-signal bandwidth

$f_{suppres}$	Suppressing frequency formed by the filter
$G_b(s)$	Band pass filter transfer function
$G_k(s)$	Controller transfer function
$G_p(s)$	Plant transfer function
i_c	Circulating current
I_c	Average circulating current
i_{ch}	Charging current
I_{ch}	Average Charging current
i_i	Impulse current
$i_{u,l}$	Upper and Lower arm current
i_s	Output current
I_s	Average output current
i_{SM}	Current consumption of the APS
K_p	Proportional controller gain
$K^i_{pu,l}$	Proportional controller gain for the arm controller for the i^{th} submodule from the upper and lower arm
K_i	Integral controller gain
L_a	Arm inductance
n	Integer part of the average modulation index ($n_{u,l}$)
N	Number of submodules per arm
$n_{u,l}$	Average insertion indices for upper and lower arm
$n^i_{u,l}$	Insertion index of i^{th} submodule from upper and lower arm
m_a	Modulation index
P_{APS}	Power consumption of the APS
R_a	Arm resistor
R_f	Front resistor
R_G	Gate resistor
R_h	Tail resistor
R_{leakge}	Leakage resistor parallel to the test object
R_p	Protection resistor
R_{per}	Parallel resistor
THD_{nonsin}	THD definition for non-sinusoidal waveforms
T_c	Charging time required for the soft start-up algorithm to work

$v_{SM,initial}$	Initial SM capacitor voltage across the basic building block
v_u	Total voltage across the lower arm submodules
V^*_{ref}	Reference voltage waveform
$v^{avg}_{u,l}$	Average total voltage across the upper and lower arm submodules
$v^i_{u,l}$	Voltage of i^{th} submodule from upper and lower arm submodules
w	Angular frequency of the reference waveform
w_c	Resonant frequency
T_{s1}	Time taken for all SMs to have APS + Delay before the soft start-up algorithm starts
T_{s2}	Time for stage 2 in the soft start-up algorithms for 3 SMs
T_s	Simulation step of the real-time simulator
T_{sw}	Period of the chosen switching frequency
v_a	Output voltage applied across the test object
V_a	Average output voltage applied across the test object
v_c	Circulating voltage
V_{CE}	Collector to emitter voltage in IGBT
V_{DC}	Total input DC-link voltage
V_{DS}	Drain to source voltage in MOSFET
V_{GE}/V_{GS}	Gate to emitter/source voltage in IGBT / MOSFET
$V_{h,ref}$	Voltage magnitude of h^{th} harmonic from reference waveform
$V_{h,out}$	Voltage magnitude of h^{th} harmonic from output waveform
$V_{1,out}$	Voltage magnitude of fundamental harmonic from out waveform
$v_i(t)$	Voltage expression of LI waveform
V_m	Peak magnitude of the LI waveform
v_l	Total voltage across the lower arm submodules
v_s	Internal switching voltage of the MMC
v_{SM}	SM capacitor voltage across the basic building block
$v^i_{SM,u,l}$	SM capacitor voltage across the i^{th} basic building block from upper and lower arm
$V_{SM,avg}$	Average SM capacitor voltage across the basic building block
$V_{SM,avg,t}$	Average SM capacitor voltage across the basic building block at time t

LIST OF FIGURES

LIST OF TABLES

SUMMARY

Due to the massive integration of wind and solar energy using power electronic converters, High Voltage (HV) equipment in the electrical power system, such as switchgear, cables, and transformers, are experiencing new and/or different electrical stresses. This includes higher dV/dt stress and complex wave shapes due to the solid-state switching, which can degrade the reliability of the grid by weakening the dielectric material of the grid assets.

Additionally, existing HV test sources, i.e., transformers (cascaded and resonant), Marx generators, and rectifier circuits, face many limitations. Firstly, they do not have the flexibility to generate complex wave shapes. Secondly, the HV test sources have limited current capability from a few hundred milliamperes to a few amperes. Lastly, building a customized test setup is time-consuming when multiple HV test sources have to be combined to generate complex waveforms.

To address the above-mentioned challenges, an Arbitrary Wave shape Generator (AWG) for dielectric testing of HV grid assets is needed. A Modular Multilevel Converter (MMC) topology is selected as a promising solution, considering its modular structure, low harmonic content, and scalability to higher voltage levels. Dielectric testing of Medium Voltage (MV) class equipment is chosen as the first target for the MMC-based HV AWG, and a modular prototype is considered the final goal of the PhD.

HV TEST REQUIREMENTS

HV test requirements and their procedures are compiled for the conventional tests of MV class equipment. Moreover, requirements for non-standards wave shapes are summarized considering the unconventional tests arising with the hybrid grid. This compilation delivers specifications for the MMC-based HV AWG in terms of the required voltage rating, current rating, and the bandwidth. It is important to highlight that HV grid assets behave electrically as a capacitance during the dielectric tests. Within this PhD thesis, two main HV test requirements are addressed. The first requirement for the HV AWG is the output voltage range of 10 kV to 100 kV, load capacitance range of 50 pF to 10 nF and large-signal bandwidth up to 2.5 kHz. The second requirement is about the generation of steep pulses with a rise time of a few microseconds for a voltage magnitude of 250 kV across the capacitive load of 10 nF.

DESIGN TRADE-OFFS OF MMC-BASED HV AWG

Although the MMC technology is well-maturated for HVDC transmission applications, the HV test requirements pose different challenges, and this thesis identifies different design trade-offs for the HV AWG application to generate accurate voltage waveforms. These design trade-offs are about the main MMC parameters, such as the number of Submodules (SMs) per arm, arm inductance, arm resistance, modulation technique, SM

capacitance, and control system, and their design criteria are developed. The performance of the proposed design guidelines is demonstrated with a simulation model and a scaled-down prototype with a 300 V DC-link voltage, where bipolar, unipolar, and mixed polarity waveforms are generated with a THD less than 3 %. Apart from the arm resistor-based passive damping, active damping methodology is investigated for HV AWG application to reduce the losses in the arm resistor. Additionally, the feasibility of the proposed design guidelines is validated with the simulation model for the full-scale prototype of the MMC-based HV AWG.

CONTROL HARDWARE OF HV AWG

Though the modular structure of the MMC offers scalability with respect to its hardware SM, the controller hardware can be a challenge to generate high-frequency waveforms with arbitrary wave shapes. For this thesis, a commercially available Real Time Simulator (RTS) named Typhoon-HIL is selected, considering its flexibility to program arbitrary waveforms in the Field Programmable Gate Array (FPGA) without coding in any special hardware description language. Its performance is demonstrated in the scaled-down prototype where sinusoidal waveforms up to 5 kHz reference frequency are generated with THD less than 5 %.

STEEP PULSE GENERATION

The second HV test requirement about the steep pulse generation is investigated with the MMC topology, and it has found that the inherent nature of series-connected SMs of MMC makes it very difficult to obtain such a short rise time across the large capacitive load of 10 nF. Hence, an integrated hybrid circuit of MMC and Marx generator circuit is proposed for the complex waveform with rise time faster than 100 μs. The finite output impedance of the MMC interacts with the Marx generator circuit parameter and affects the front time and tail time. This thesis provides proper guidelines about choosing circuit parameters to obtain accurate rise and tail time, and these are validated experimentally with a scaled-down prototype.

DEMONSTRATION OF THE MV SM DESIGN

The important deliverable of this PhD thesis is the hardware design of a scalable MV SM (up to 3 kV) as a building block, to realize the 100 kV full-scale prototype of the HV AWG from commercially available components. The scalable design of MMC SM requires its Auxiliary Power Supply (APS) to be obtained from the SM capacitance. This additional component creates severe challenges to the MV SM design implementation in terms of its required SM capacitance value, start-up, steady-state, and shut-down procedures based on the derived current model of the APS. Based on the detailed quantitative analysis of the parameters mentioned above, the modular prototype of the MMC-based HV AWG is realized using a single MV SM per arm for various wave shapes, with the required wide output range of 0.12 kV to 1.2 kV, and frequency range of 1 Hz to 600 Hz with THD within 5 %. The proposed design of the scalable MV SM satisfies the second HV test requirement. Additionally, it can be used for performing dielectric tests such as partial discharge measurements or aging tests of the HV insulation material.

SAMENVATTING

Als gevolg van de massale integratie van wind- en zonne-energie met behulp van vermogens elektronische omvormers krijgt hoogspanningsapparatuur in het elektriciteitsnet, zoals schakelapparatuur, kabels en transformatoren, nieuwe en/of andere elektrische belasting. Dit omvat hogere dV/dt en complexe golfvormen als gevolg van het schakelen van halfgeleiders, wat de betrouwbaarheid van het net negatief kan beïnvloeden door verzwakking van het isolatiemateriaal van de netcomponenten.

Bovendien hebben bestaande hoogspanningstestbronnen, zoals transformatoren (cascade en resonant), impulsgeneratoren en gelijkrichterschakelingen, veel beperkingen. Ten eerste hebben ze niet de flexibiliteit om complexe golfvormen te genereren. Ten tweede hebben deze testbronnen een beperkte stroomcapaciteit in het bereik van een paar honderd milliampère tot een paar ampère. Tot slot is het bouwen van een testopstelling tijdrovend wanneer meerdere bronnen gecombineerd moeten worden om complexe golfvormen te genereren.

Een oplossing voor bovengenoemde uitdagingen is het gebruik van een Arbitrary Waveshape Generator (AWG) voor het dielektrisch testen van hoogspanningscomponenten. De Modular Multilevel Converter (MMC) topologie is geselecteerd als veelbelovende oplossing op basis van de modulaire structuur, lage harmonische vervorming en schaalbaarheid naar hogere spanningsniveaus. Het dielektrisch testen van middenspanningsklasse apparatuur is gekozen als eerste doel voor de op een MMC-gebaseerde HV AWG, waarbij het modulaire prototype beschouwd wordt als het einddoel van dit proefschrift.

HOOGSPANNINGSTESTEISEN

Voordat dieper wordt ingegaan op het ontwerp van de op een MMC-gebaseerde hoogspanningsgenerator Worden de testeisen en procedures voor conventionele middenspanningsapparatuur verzameld. Bovendien worden de vereisten voor niet-standaard golfvormen samengevat, rekening houdend met de onconventionele tests die bij het hybride net van de toekomst voorkomen. Dit overzicht levert specificaties op voor de op een MMC-gebaseerde HV AWG in termen van de vereiste spanning, stroom en bandbreedte. Het is belangrijk om te benadrukken dat de testen componenten zich elektrisch gedragen als een capaciteit tijdens dielektrische testen. In dit proefschrift worden twee belangrijke eisen Behandeld voor de AWG. De eerste eis omvat spanningen in het bereik van 10 kV tot 100 kV, belastingscapaciteiten tussen 50 pF tot 10 nF en een bandbreedte tot 2,5 kHz. De tweede eis gaat over het genereren van steile pulsen met een stijgtijd van enkele microseconden voor spanningen tot 250 kV over een capacitieve belasting van 10 nF.

ONTWERP KEUZES VAN OP EEN MMC-GEBASEERDE AWG

Hoewel de MMC-technologie geschikt is voor HVDC transmissietoepassingen, geven de hoogspannignstesteisen andere uitdagingen. In dit proefschrift worden verschillende ontwerp keuzes geanalyseerd voor de HV AWG-toepassing om nauwkeurige spanningsgolfvormen te genereren. Deze ontwerp keuzes omvatten de belangrijkste MMC parameters, zoals het aantal SMs per arm, de arminductie, de armweerstand, modulatie techniek, SM capaciteit en het regelsysteem. De prestaties van het voorgestelde ontwerp worden aangetoond met behulp van een simulatiemodel en een laagspanningsprototype met 300 V DC-bus, waarmee bipolaire, unipolaire en complexe golfvormen kunnen worden gegenereerd met THD van minder dan 3 %. Naast de passieve demping gebaseerd op de armweerstand, wordt de actieve dempingsmethodologie onderzocht voor AWG-hoogspanningstoepassingen om de verliezen in de armweerstand te verminderen. De haalbaarheid van het voorgestelde ontwerp wordt gevalideerd met een simulatiemodel voor een MMC AWG op ware grootte.

BESTURINGSHARDWARE VAN DE AWG

Hoewel de modulaire structuur van de MMC schaalbaarheid met betrekking tot de hardware biedt, kan de besturingshardware een uitdaging zijn om hoogfrequente golfvormen met willekeurige golfvormen te genereren. Voor dit proefschrift is een commercieel verkrijgbare Real Time Simulator (RTS) genaamd Typhoon-HIL geselecteerd vanwege de flexibiliteit van Typhoon-HIL om willekeurige golfvormen in de veldprogrammeerbare poortarray te programmeren zonder codering in Hardwarebeschrijvingstaal. De prestaties ervan zijn aangetoond door middel van een laagspanningsprototype waarmee sinusoidale golfvormen tot 5 kHz met een THD van minder dan 5 % zijn gegenereerd.

OPWEKKEN VAN STEILE PULSEN

De tweede eis over het genereren van steile pulsen is onderzocht voor MMC-topologie, en het bleek dat de inherente eigenschappen van in serie geschakelde SMs het erg moeilijk maakt om pulsen met een korte stijgtijd te krijgen over een capacitieve belasting van 10 nF. Een geïntegreerde hybride schakeling van een MMC en Marx generator wordt voorgesteld voor complexe golfvormen met stijgtijden kleiner dan 100 μs. De interactie van de eindige uitgangsimpedantie van de MMC met de parameters van het Marx generatorcircuit beïnvloedt de fronttijd en de rugtijd. Dit proefschrift geeft richtlijnen voor het kiezen van de juiste circuitparameters om een nauwkeurige front- en rugtijd te krijgen en wordt experimenteel gevalideerd met een prototype.

DEMOSTRATIE VAN HET ONTWERP VAN DE MIDDENSPANNINGS SM

Het belangrijke resultaat van dit proefschrift is het hardware ontwerp van een schaalbare Middenspannings SM (tot 3 kV) die geschikt is om het een 100 kV prototype AWG op ware grootte te realiseren met behulp van commercieel verkrijgbare componenten. Het schaalbare ontwerp van De MMC SM vereist dat de hulpvoeding (APS) uit de condensator van de SM wordt verkregen. Deze hulpvoeding creëert enkele grote uitdagingen voor de realisatie van het SM-ontwerp in termen van de vereiste grootte van de condensator, opstart-, stationaire en uitschakelprocedures op basis van het stroommodel van de APS. Gebaseerd op de gedetailleerde kwantitatieve analyse van bovengenoemde parameters,

wordt het modulaire prototype van de op een MMC-gebaseerde AWG gerealiseerd met een enkele middenspannings SM per arm die geschikt is voor verschillende golfvormen, en het vereiste brede uitgangsbereik van 0,12 kV tot 1,2 kV, een frequentiebereik van 1 Hz tot 600 Hz en met maximaal 5 % THD. Het voorgestelde ontwerp van de schaalbare middenspannings SM voldoet aan de hoogspanningstesteisen en kan bovendien worden gebruikt bij het uitvoeren van dielektrische testen zoals partiele ontladingsmetingen of verouderingstesten van isolatiemateriaal.

1

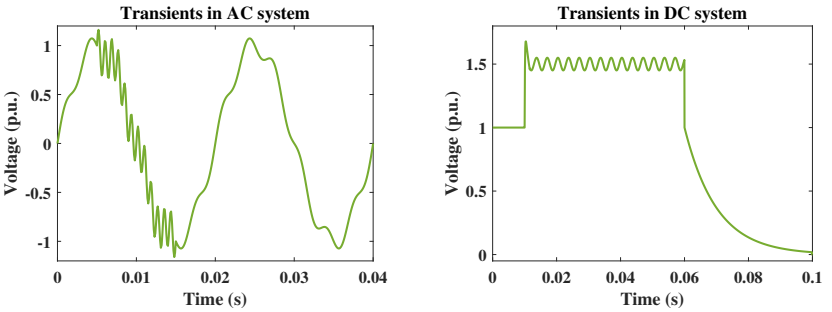
INTRODUCTION

1.1. MOTIVATION

Extensive use of fossil fuels for electricity, heat, and transportation has significantly increased greenhouse gas emissions, impacting the Earth's ecosystem. To restore climate change and leave a safe space for future generations, the Paris Agreement was signed in 2015 by 196 parties to limit the temperature rise to 1.5 °C by the end of this century [1]. This has started extensive efforts to decarbonize the three sectors mentioned above with more sustainable solutions such as renewable energy sources for electricity and electrifying the other sectors. Hence, the electrical power network, the biggest man-made structure, is experiencing massive changes in its components and working operations. Earlier, the electricity used to flow in one direction from the generation centers to the demand centers. Currently, the electricity flow is multi-directional, and users can participate in supplying electricity with roof-top solar panels, electric vehicle batteries, or bio-fuel sources [2]. The growth in the semiconductor industry has revolutionized the electrical power network, where many variable energy sources generating DC or variable frequency AC can be integrated into the AC network with Power Electronic (PE) converters.

Due to numerous distributed generation systems and massive integration of Renewable Energy Sources (RES) by PE converters, High Voltage (HV) equipment in the electrical power system, such as switchgear, cables, and transformers, are experiencing new and/or different electrical stresses [3][4]. Fig. 1.1 illustrates a few examples of the new and/or different electrical stresses occurring in the hybrid electrical AC and DC power network. For this reason, HV equipment must endure higher dV/dt stress due to faster solid-state switching, which can degrade the grid's reliability by weakening the dielectric insulation of the HV grid assets. Conventional HV dielectric test sources, i.e., transformers (cascaded and resonant), impulse generators, and DC generators, face many limitations. Firstly, they do not have the flexibility to generate complex wave shapes. Secondly, HV test sources often have limited current capability in the range of mA to A. Lastly, building a customized test setup is time-consuming when multiple HV test

sources have to be combined to generate complex waveforms. This emphasizes that a universal HV test source is necessary to cope with all the above challenges and limitations with the existing HV test sources and to facilitate the testing with the new future stresses, which are often customer specific. Eventually, this will speed up the necessary step-change needed for the energy transition. Since these new electrical stresses are mainly generated by the switching mechanisms of the semiconductor devices, the same ingredient is chosen to develop a programmable HV test source for future and advanced dielectric tests of various grid assets.



Figuur 1.1: New electrical stresses occurring in the electrical power network.

Though PE converters have been developed for a long time, adapting them as an HV test source for dielectric testing with arbitrary wave shape has many challenges. As the name suggests, the HV testing application requires an HV PE converter, ideally with a modular and scalable design to adapt to different voltage levels. The high voltage brings many challenges in realizing such a PE-based HV AWG from commercially available components. Next, it is important to highlight that the equivalent load during a dielectric test is capacitive [5]. Hence, there will not be any intended active power transfer in the PE-based HV Arbitrary Wave shape Generator (AWG). This significantly differs from the kW to GW (HVDC converters) range of active power transfer occurring in the typical PE converter. Lastly, the power efficiency of the converter is of utmost importance in energy transmission, whereas voltage accuracy is paramount in HV testing. With the differences mentioned above, specifications will be voltage and current capability, slew rate (rate of rise), and bandwidth.

1.2. SCOPE, OBJECTIVE AND RESEARCH QUESTIONS

Based on the motivations and research challenges mentioned above, the PhD objective can be defined as follows:

"Design of a High Voltage Arbitrary Wave shape Generator for Dielectric Testing"

As a first attempt of the PE-based HV AWG, tests of Medium Voltage (MV) class equipment are targeted within this PhD. The voltage rating of the MV equipment ranges between 1 kV and 36 kV [6]. They are tested at much higher voltage, mainly with power fre-

quency waveform and lightning impulse waveform at much higher voltage magnitude than its rated voltage [7]. Hence, a modular prototype of the HV AWG will be designed and realized in the ESP lab of TU Delft instead of moving directly to the full-scale prototype, and it is defined as the final goal of the PhD. Based on the research objective, the following research questions are formulated, which are investigated in detail in this thesis.

Q1. What is HV testing/dielectric testing? How is it performed? (Chapter 2, Appendix A & Appendix B)

This research question provides the foundation for designing the PE-based HV AWG by compiling all test requirements and specifications. The conventional tests for MV equipment are summarized as per IEC standards in Chapter 2 and Appendix A in consulting with various test engineers from KEMA labs. Similar to Fig. 1.1, various unconventional test waveforms establish a concrete motivation for such a PE-based HV AWG, which is enhanced by showcasing limitations with existing HV test sources. Additionally, a PD measurement circuit is designed to study the effect of the switching waveform generated by the PE converter on the applied dielectric stress, which provides a good indication of choosing system parameters for the PE-based HV AWG.

Q2. What is a promising solution direction for HV AWG? How to design the selected solution as a HV AWG? (Chapter 3 & Chapter 4)

Various possible solutions, such as Modular Multilevel Converter (MMC), Cascaded H Bridge (CHB), and HV amplifier, are compared to choose a promising solution direction for the HV AWG. Then, the design trade-offs of the selected topology are investigated thoroughly with simplified equivalent circuits of the PE converter. The design trade-offs are about the choice of implemented modulation technique, control methodology, and passive elements. Then, the proposed design trade-offs are verified with the MATLAB-Simulink simulations and a scaled-down experimental prototype. In the end, system parameters for the full-scale prototype of the HV AWG are designed, and its performance is demonstrated with MATLAB-Simulink simulations. Ultimately, this chapter delivers a fundamental understanding and comprehensive design guidelines for realizing the HV AWG using the selected PE converter topology.

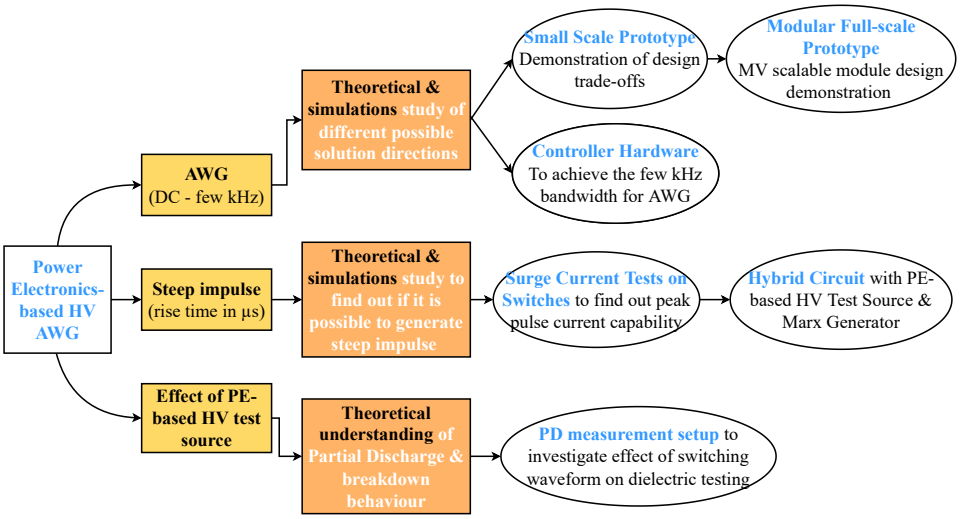
Q3. How to design hardware and control of HV AWG? (Chapter 4 & Chapter 6)

This question dives deeper into two main challenges of the HV AWG, i.e., the hardware and control design. Chapter 6 presents the innovative hardware design of an MV Submodule (SM) from the commercially available components that satisfy all HV testing requirements. It is essential to highlight that the MV SM is scalable and can be stacked together to realize the full-scale prototype. A proper operation of the MV SM is achieved by formulating and designing precise start-up, steady-state, and shut-down procedures, and its performance is demonstrated in Chapter 6. Moreover, a protection system is designed in case a fault occurs in the part of the HV AWG or outside of the HV AWG when

the test object breaks down. The second challenge about the control hardware that can implement high-frequency gate pulse generation is discussed in Chapter 4, where an optimal control hardware is chosen considering the accuracy of waveform generation at high frequency with the ability to program different wave shapes and to withstand harsh Electromagnetic Compatibility (EMC) environments during the HV tests.

Q4. How to generate steep pulses with rise time as few microseconds using HV AWG? (Chapter 5)

Steep pulses with a rise time of as few μs, such as lightning impulse, can be challenging for the PE-based HV AWG, and its feasibility is studied with the selected topology from Chapter 3. Upon investigating the chosen topology, many challenges are observed concerning the switch current capability, communication error, and stray elements. For the PE-based HV AWG to be a universal test source, it has been integrated with the Marx generator to generate steep pulses and complex waveforms. This unique combination of two sources is studied analytically, and its performance is demonstrated with the simulations model and experimental setup.



Figuur 1.2: PhD scope.

Fig. 1.2 summarizes the scope of the PhD with the above-mentioned research questions. Overall, the PhD research is divided into three aspects. The first aspect concerns generating arbitrary wave shapes up to a few kHz range. This research chooses a promising PE solution direction, and its design trade-offs are investigated analytically with simulation models and the experimental setup. With the help of these design trade-offs, an innovative and scalable MV module is realized using off-the-shelf components. Considering the harsh EMC environment in the HV test labs, the appropriate control hardware is chosen for the selected PE solution. The second research aspect is about performing

the feasibility study for steep pulse generation from the PE-based HV test source, and a novel hybrid solution is proposed to generate various complex waveforms that include steep pulses. The third research direction is to understand the effect of the switching waveform generated by the PE-based HV test source on the applied dielectric stress with Partial Discharge (PD) measurement setup.

1.3. CONTRIBUTIONS

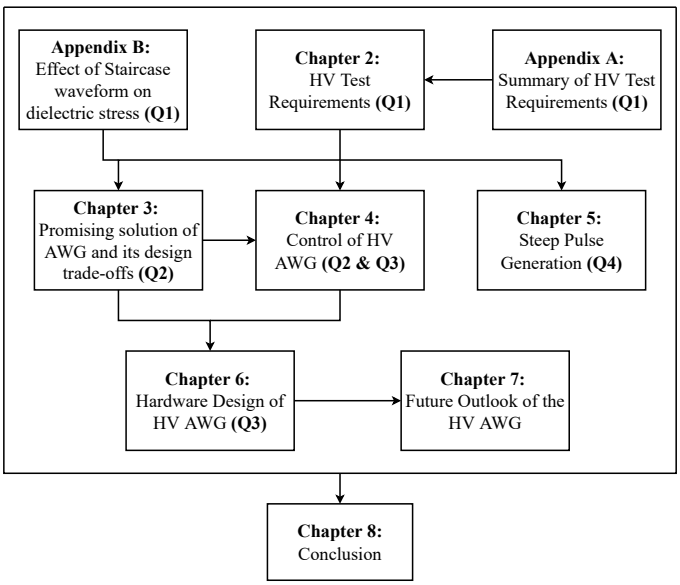
The main contributions from this PhD research are as follows:

- Extensive summary of the conventional and unconventional HV test requirements with acknowledging the limitations of the existing HV test sources **(Chapter 2 & Appendix A)**
- A newly developed PD measurement setup to understand the effect of the switching waveform generated by the PE-based HV AWG on the applied dielectric stress **(Appendix B)**
- Comprehensive design guidelines for adapting a PE converter as an HV AWG with an analytical model, simulation model, and a scaled-down prototype **(Chapter 3)**
- Investigations of various control methodologies for the PE-based HV AWG **(Chapter 3 & Chapter 4)**
- Selection of control hardware to generate accurate gate pulses at high switching frequency **(Chapter 4)**
- Innovative design of the MV scalable SM and its demonstration with a modular prototype **(Chapter 6)**
- Feasibility study of steep pulse generation from the PE-based HV test source and a proposed novel solution is investigated to achieve it **Chapter 5)**
- A future outlook of the PE-based HV AWG with a complete design guide for KEMA Labs to further develop the HV test source **(Chapter 7)**

1

1.4. OUTLINE OF THESIS

Based on the research questions and contributions, the outline of the PhD thesis can be drawn, as shown in Fig. 1.3. The first line from the thesis outline contains Chapter 2, Appendix A, and Appendix B, and this content creates a strong foundation of HV testing application for designing the PE-based HV AWG. The second line is about the detailed study of the PE converter, which contains the mathematical modelling, simulation studies, and experimental results with the scaled-down prototype. Based on the design trade-offs obtained previously, a scalable modular prototype of the HV AWG is designed, and its performance is demonstrated in Chapter 6. From all the lessons learned while realizing the modular prototype, a complete design guide is prepared for KEMA Labs to actualize a full-scale prototype in their testing facility in Chapter 7.



Figuur 1.3: Thesis Outline.

2

HV TEST REQUIREMENTS

Before diving into the details of designing a new power electronics-based HV test source, this chapter gives an overview of the HV test requirement, including both conventional and unconventional tests. The conventional tests summarize IEC standards for the four most common MV grid assets: switchgear, power transformer, cable, and instrument transformer. Additionally, the simplified HV test circuit of the equipment mentioned above is shown to clarify the test object and HV connections. Later, the unconventional test waveforms are summarized for various tests ranging from material tests to HVDC cables tests. Furthermore, the characteristics of existing HV test sources are discussed, where their limitations are highlighted to introduce the power electronics-based HV test source. Since the HV testing application is much different from the usual power transmission application of power electronic converters, these differences are highlighted to help develop the design criteria. Finally, the design requirements for the power electronics-based HV test source are summarized.

2.1. INTRODUCTION

Before integrating the power grid equipment into the grid, sample items are tested to determine the electric, mechanical, and thermal properties for reliable operation. HV tests are used to determine the dielectric properties such as the dielectric strength, partial discharges, and dielectric losses of MV and HV insulation materials [8]. During these dielectric tests, the equipment insulation behaves electrically as a capacitance [5]. Power grid equipment and their testing have a long history of more than one century [9]. These test procedures are standardized for a particular voltage class by different standards organizations such as IEC and IEEE. They are called conventional HV tests for now on in this thesis. In the following subsections, the conventional HV tests of MV equipment are summarized, where the rating of the equipment ranges between 1 kV and 36 kV [6]. Note that MV class grid equipment is prone to many critical operating conditions and thus must withstand voltages above its rated values that reach HV levels (36 kV to 150 kV [6]). Similarly, HV equipment needs to be tested at extra-high voltage levels, which means

much more than 150 kV). As a first attempt of the PE-based HV AWG, tests of Medium Voltage (MV) class equipment are targeted within this PhD.

2.2. CONVENTIONAL TESTS

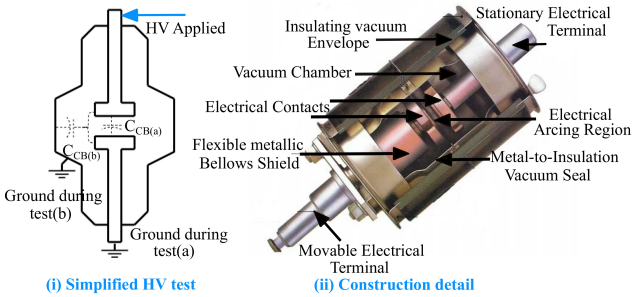
Among many types of MV equipment, the four most common in commercial testing are chosen, i.e., switchgear, transformers, cables, and instrument transformers. In the EU, these types of equipment are tested according to the IEC standards [10][11][12][13], mainly with sinusoidal and lightning impulse test waveforms [14]. Here, the sinusoidal can be a power frequency waveform, or the frequency can vary between 10 Hz and 500 Hz for onsite testing [15]. To reduce the size of the onsite test equipment, a Very Low Frequency (VLF) test is conducted for MV cables, where the frequency is reduced between 0.01 Hz to 1 Hz [15]. The Lightning Impulse (LI) is a steep impulse with 1.2 μs rise time and 50 μs tail time. The power frequency tests and LI tests of MV class equipment are conducted at a higher voltage than the rated voltage of the equipment due to the different switching transients [7]. For example, 3 kV equipment will be tested with 10 kV, and a 36 kV rated equipment is tested at 70 kV to 80 kV [12]. Similarly, the LI test is performed at a voltage that is 6 to 7 times higher than the rated voltage of the equipment, depending on the voltage class of the equipment. For example, a 36 kV transformer will be tested with 170 kV to 220 kV lightning impulse [12]. In some cases, the manufacturer or owner of the Device Under Test (DUT) can customize a test that demands a higher voltage than the standardized value to test the limits of their equipment. Apart from these standard dielectric tests, some of the equipment needs additional tests, and they are summarized in the following subsection with their particular test circuits. Moreover, the conventional tests for different equipment are summarized in Appendix A with more details, such as how long it takes to prepare and perform tests.

2.2.1. CIRCUIT BREAKER

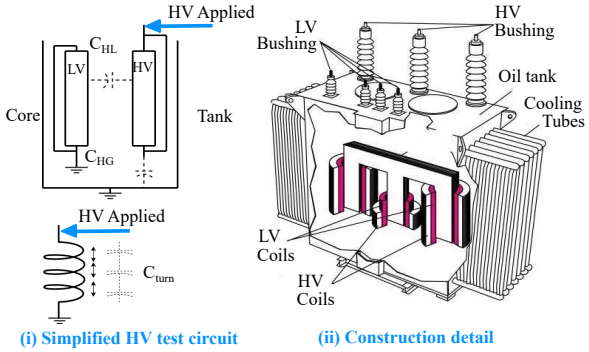
The most commonly used MV switchgear is a vacuum circuit breaker, and Fig. 2.1 shows the structure of the vacuum circuit breaker with its dielectric test circuit. The power frequency and lightning impulse tests are performed to test two types of HV insulation shown in Fig. 2.1(i). In the first test, HV insulation between two contacts of the circuit breaker is tested, and it is represented by a capacitance of $C_{CB(a)}$. The second type of HV insulation is between the contact when shorted, and the metal enclosure of the circuit breaker. The insulation under test is represented as $C_{CB(b)}$. The value of capacitance $C_{CB(a)}$ and $C_{CB(b)}$ is taken to be the same as 50 pF [16]. Generally, many dielectric tests need to be performed on different combinations of vacuum circuit breaker configurations, and these configurations are summarized in IEC 62271-1 [10]. Additionally, Fig. 2.1(ii) shows the internal mechanical structure of an MV vacuum circuit breaker.

2.2.2. DISTRIBUTION TRANSFORMER

MV class transformers are generally distribution transformers, converting MV to LV to distribute to consumers. Among many tests for the distribution transformer, the applied voltage test is a power frequency test of one-minute duration to check the insulation strength between the winding under test. In contrast, the other winding and tank are



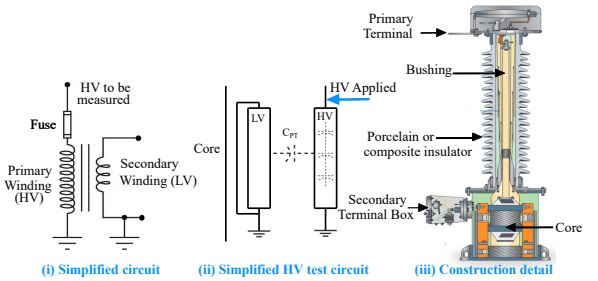
Figuur 2.1: MV vacuum circuit breaker [17].



Figuur 2.2: MV Distribution Transformer [20].

grounded. During the applied voltage test, approximately two times higher than the maximum system voltage is applied. Insulation strength between two turns is investigated using a voltage at LV winding at a higher frequency and for a shorter duration to avoid core saturation. Details of this calculation are given in Appendix A. Since this is a low-voltage test, it is excluded from the test list. During the LI test, a high-speed voltage transient appears along the winding, which behaves as a transmission line, and an uneven voltage distribution occurs in the winding [18]. Hence, performing the LI and chopped LI tests is very critical. More details about the chopped LI waveform are given in Appendix A. Two IEC standards are followed to perform these tests on the distribution transformers, and these are IEC 60076-1, IEC 60076-3, and IEC 60076-11 [11][12][19].

During the applied voltage test, it is possible to measure capacitances (C_{HL} and C_{HG}), as shown in Fig. 2.2. Based on the real MV transformer test in KEMA Labs, the value of low voltage winding capacitance to ground (C_{LG}) is taken to be 19 nF to 26 nF and the value of high voltage winding capacitance to ground (C_{HG}) is taken to be 12 nF to 16 nF. The relationship between total inter-turn capacitance ($C_{turn}/(n_{discs}-1)$) can be calculated from $\alpha = \sqrt{C_{HG}(n_{discs}-1)/C_{turn}}$, where n_{discs} represents the number of discs in the winding [21]. Since the value of α is always more than 1, the total inter-turn capacitance ($C_{turn}/(n_{discs}-1)$) is much smaller than the winding to ground capacitances [22]. For the impulse test, the parallel combination of inter-turn and winding-to-ground capacitance

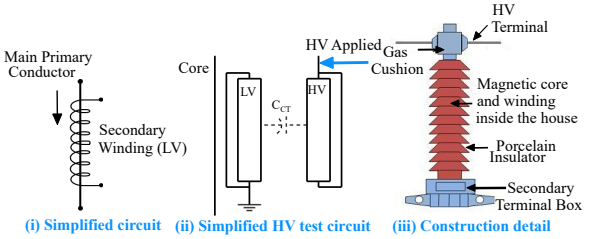


Figuur 2.3: Potential Transformer (PT) [27].

will be dominated by the winding-to-ground capacitance. Hence, a rough value of 10 nF is the maximum capacitance value to consider when generating LI waveforms.

2.2.3. INSTRUMENT TRANSFORMERS

Instrument transformers are step-down transformers with fixed low-voltage winding suitable for measurement. There is a significant difference between a distribution transformer and an instrument transformer regarding its construction and operation [23]. Hence, the dielectric tests performed on the distribution transformer and PT are different in their test circuit, as shown in Fig. 2.3 and 2.2. Though the test connections are the same for the distribution transformer and CT, there is only a single turn in the primary winding of a CT with a toroidal core [24] instead of a standard E core in the distribution transformer [25]. Also, there is a particular test named multiple chopped impulse test for CT where 600 consecutive pulses must be applied [26]. The equivalent test capacitance for the voltage transformer and current transformer can be considered as 1 nF and 0.25 nF, respectively [21].

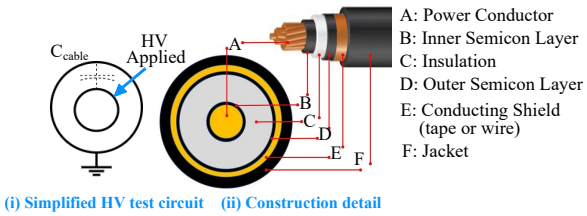


Figuur 2.4: Current Transformer (CT) [24].

2.2.4. AC CABLE

The list of tests for AC cables is similar to that of the transformers. But, there is an important difference in that the cable temperature needs to be maintained per the manufacturer's design guidelines. Hence, even the dielectric tests are conducted while a rated current flows through the conductor to maintain the temperature. Also, there is no need to perform a chopped lightning impulse test on cables as done for transformers. Cables

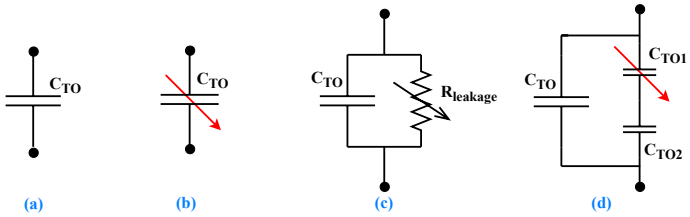
behave as capacitance, and the manufacturer gives the capacitance value per kilometer or meter, or even when not given, it is possible to measure it easily. The voltage is applied across the power conductor and conducting shield to test insulation strength. Fig. 2.5 shows the cable's construction details with its simplified HV test circuit diagram. The capacitance of 10 m cable is roughly 2 nF [28].



Figuur 2.5: MV AC Cable [29].

2.2.5. TEST OBJECT BEHAVIOUR

As explained before, HV equipment predominantly behaves as an equivalent capacitance. However, some of the test conditions change it, and they are summarized in this subsection. When there is a breakdown in the test object, the breakdown path decides the impedance of the test object, and it is represented as a variable impedance in Fig. 2.6(b). An external environment, such as a wet test, is created artificially for outdoor HV equipment. This will increase the leakage current that the test source needs to supply, and it can be modeled as a variable resistor parallel to the capacitor, as shown in Fig. 2.6(c). Additionally, one more phenomenon called non-disruptive discharge occurs in the test object, where small cavities within the insulation break down. Fig. 2.6(d) shows the test objects which can be used for such a phenomenon. For simplicity, only Fig. 2.6(a) is considered a load to the HV AWG, and all typical capacitances of mentioned HV grid assets are summarized in Table 2.1.



Figuur 2.6: Test Object Behaviour (a) Normal (b) During Breakdown (c) For Outdoor Equipment (d) For Partial Discharges within the HV insulation.

2.3. UNCONVENTIONAL TESTS

Unconventional HV tests include material tests where non-sinusoidal waveforms such as rectified sinusoidal or triangular or pulse are used to correlate the dielectric property

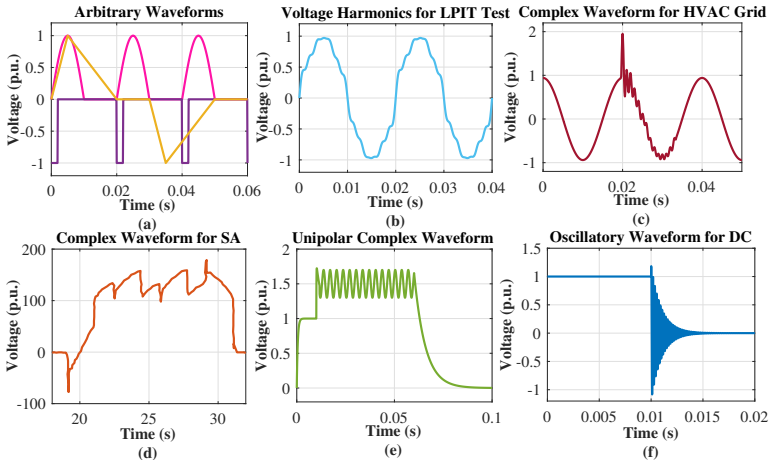
Tabel 2.1: Typical Range of the Equivalent Capacitance of Dielectric Insulation Materials

Vacuum Circuit Breaker [16]	Power Transformer [16]	AC Cable [28] (for L=10 m)	Instrument Transformer [21]
$C_{CB(a)}$=50 pF $C_{CB(b)}$=50 pF	C_{HG}=12-16 nF C_{LG}=19-26 nF	C_{cable}=1-10 nF	C_{PT}=1 nF C_{CT}=0.25 nF

to the condition of the MV or HV insulation, e.g., location of the defect, type of defect, lifetime, etc.,[30][31]. These waveforms are shown in Fig. 2.7(a). These arbitrary waveforms are generated using a function generator and HV amplifier circuit [32]. However, the HV amplifier limits the material thickness under test and can not be used for testing MV equipment with few tens of nF. Additionally, unconventional tests include a harmonic test of Low Power Instrument Transformer (LPIT). Here, the higher order harmonics up to 40^{th} or even 50^{th} are needed to be generated to test the accuracy of the Potential Transformer [26], and it is shown in Fig. 2.7(b). This testing is increasingly important, considering higher harmonics are injected into the HV grid and must be measured accurately. The waveform in Fig. 2.7(c) is a transient waveform experienced by the 380 kV rated cable when a circuit breaker is operated in one of the sections of the Dutch transmission network [33]. Besides the most common grid assets mentioned above, surge arresters are heavily used in HVAC and HVDC systems for protection. Fig. 2.7(d) shows voltage stress experienced by a valve arrester in an LCC converter station generated due to a 12-pulse converter bridge [34]. For reliable operation of the HVDC converter station, generating this voltage stress to test the valve arrester before deploying it in the field is essential. However, creating such a test waveform with existing HV test sources is difficult.

Furthermore, these tests include future and advanced waveforms required to test MV/HV equipment with real electric stress generated due to the inverter-dominated power grid. One such complex waveform is the unipolar DC waveform explicitly caused in the symmetric monopole HVDC transmission system [4], as shown in Fig. 2.7(e). The mentioned complex waveform consists of switching impulse and superposition of a 6^{th} harmonic component of the fundamental grid frequency of 50 Hz and a DC component value. The specific waveform is generated when the cable experiences a pole-to-ground fault. In this case, the voltage on another cable line can become two times higher than the rated values. This is usually restricted to 1.5 times the rated value by installing surge arresters. When the surge arrester reacts toward the fault, the control of the HVDC MMC protects the solid-state switches, e.g., IGBTs, by going into a blocked state, and the converter acts as a diode rectifier [35]. The AC side circuit breaker identifies this fault and disconnects the converter from the grid after tens of ms. This waveform needs three different HV test sources to generate DC, switching impulse, and 6^{th} harmonic sinusoidal. Hence, it is complicated to design such a circuit. Apart from this waveform, the HVDC cable has to be tested with Temporary Over Voltage (TOV) [36]. One example of such a TOV is shown in Fig. 2.7(f), and a resonant circuit is proposed in [37] to generate the waveform for performing dielectric testing. However, the circuit faces issues in repeatability when creating the waveform with the same parameters. Apart from the HVDC cable, the DC circuit breaker needs to be tested with different TOVs, as described in [38]. In summary,

more and more future dielectric tests, similar to Fig. 2.7, will be customized based on the grid owner's transient calculations for the specific installation.



Figuur 2.7: Different impulse waveforms (a) Arbitrary waveforms for PD detection (b) Sinusoidal with voltage harmonics for LPIT test (c) Complex waveforms for HVAC Grid(d) Complex waveform for Surge Arrester (SA) (e) Unipolar complex waveform (f) DC oscillatory test waveform.

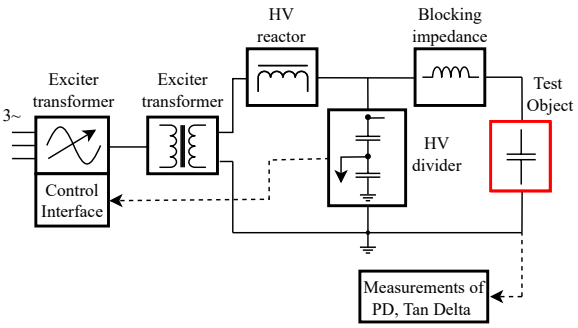
2.4. EXISTING HV TEST SOURCES

Conventional HV test sources include transformers (cascaded and resonant), impulse generators, and rectifier circuits, which can generate 50 Hz/60 Hz sinusoidal, lightning, and switching impulses, and DC respectively. It is possible to vary the sinusoidal frequency using a resonant circuit, especially in onsite testing. These testing equipment are well developed and optimized over time concerning efficiency, accuracy, size, and cost. However, these test sources are not flexible to generate waveforms other than sinusoidal, impulses, or DC. Apart from these conventional test sources, there are a few solutions to improve the flexibility of generated test waveforms. They are summarized in the following subsections.
Additionally, reducing the test preparation time for commercial testing facilities like KEMA laboratories is crucial. As described above in Section 2.2, a list of tests is to be conducted on HV equipment. Generally, these test sources are stationary, and test objects are moved from one test source to another to perform testing. Preparation time for a power frequency test of one minute can be half a working day. Preparing a LI test can take half to a full working day to obtain the required wave shape across a transformer. More information about the testing time for particular MV equipment is summarized in Appendix A.

2.4.1. RESONANT CIRCUIT

The resonant circuit is commonly used in HV tests to enhance the capability of the input test source. Such a resonant test circuit is handy during onsite testing since it is compact

enough to fit in a truck. One typical example of the resonant circuit is shown in Fig. 2.8(a) onsite cable testing. Due to the long cable length, the capacitance of the cable under test will be much larger than 10 nF. Hence, the resonant circuit is formed between an inductor tank and the cable under the test. Thus, the output voltage and current of the AC transformer can be enhanced [8]. With this circuit, it is also possible to generate variable frequency ranging from 20 Hz to 300 Hz [39]. Fig. 2.8 shows a resonant test circuit manufactured by HIGHVOLT [40] designed to generate hundreds of kilovolts. It is important to note that such a resonant circuit is limited to generating the sinusoidal wave shape.



(a)

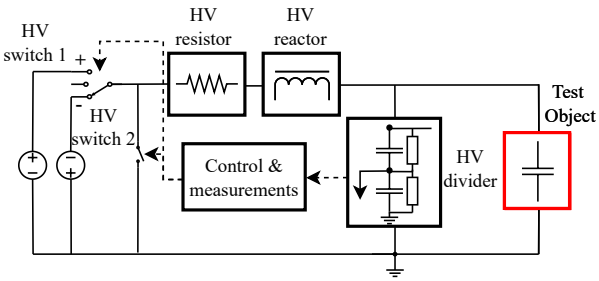
(b)

Figuur 2.8: (a) Resonant circuit (b) Commercial test device manufactured by HIGH VOLT for onsite testing [40].

Similar to the resonant circuit shown above, the VLF test circuit shown in Fig. 2.9 is standard to perform onsite testing of the MV cable, where the frequency is reduced 0.01 Hz to 1 Hz [41]. Megger developed this specific test circuit, and it has the advantage of storing and recovering 90 percent of the energy within the charged cable via the choke. Additionally, the same circuit can be used to generate a Damped Alternating Current (DAC) using the HV switch 2.

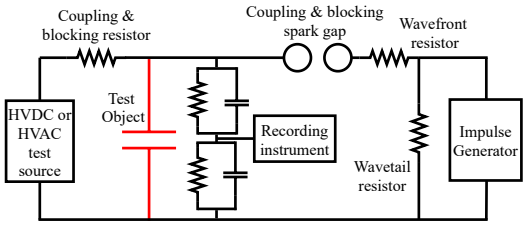
2.4.2. SUPERIMPOSED WAVEFORM CIRCUIT

As the voltage rating of the equipment increases, stresses on HV equipment become severe and need to be tested with superimposed waveforms [42]. It includes superimposing switching and lightning impulses on a sinusoidal or DC waveform. It involves



Figuur 2.9: VLF test circuit

carefully designing a combination of two HV test sources with a decoupling circuit, as shown in Fig. 2.10(a). Building such a setup and obtaining accurate results is a tedious process. Also, this circuit design needs to be repeated for different test objects. However, it is challenging to generate the unipolar test waveform shown in Fig. 2.7(c) from this superimposed waveform circuit since it will need one more source in parallel, and it is not realized yet in the literature. Fig. 2.10(b) shows the test circuit in the Mannheim lab facility of KEMA labs, and it can generate voltage up to 800 kV.



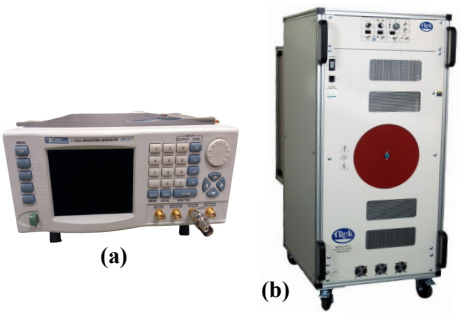
(a)

(b)

Figuur 2.10: (a) Test circuit for superimposed waveform generation [42] (b) Test setup from Mannheim KEMA Lab [16].

2.4.3. FUNCTION GENERATOR AND HV AMPLIFIER SETUP

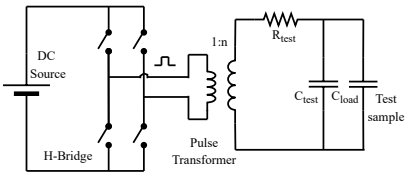
Many HV researchers are working with non-conventional test waveforms such as triangular, square, trapezoidal, and sinusoidal with variable frequency for measuring partial discharge and space charge phenomenon as shown in Fig. 2.7(a) [30]. These non-conventional test waveforms are generated using a function generator and HV amplifier setup, as shown in Fig. 2.11. The function generator can be programmed to produce any waveform mentioned above. The HV amplifier amplifies the LV signal to the desired high voltage, and such an amplifier box is available up to 60 kV. However, the commercially available HV amplifiers have limited bandwidth, slew rate, and current capability since there are many challenges concerning designing HV amplifiers at higher voltage, with more slew rate and larger bandwidth. The first major issue with the HV amplifier to increase the current rating is the complexity of dissipating more heat in the transistor due to the linear region of operation. The second major issue is that the HV DC Source supply can provide a limited drain current, eventually reducing the amplifier's bandwidth.



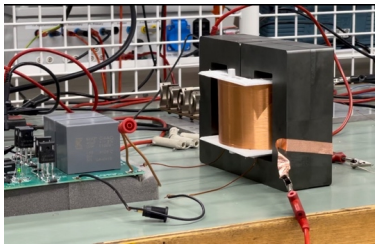
Figuur 2.11: (a) Function Generator (b) Trek HV Amplifier [32].

2.4.4. H-BRIDGE AND PULSE TRANSFORMER

The power electronic converters generate switching waveforms, and these switching waveforms are applied to the connected electrical machine or transformer insulation in applications in control drives [43] or in Solid State Transformer (SST) [44]. Hence, it is vital to study the insulation properties and aging mechanisms of the connected MV/HV insulation when subjected to such a switching waveform with high dv/dt. The switching waveform at MV is generated using an H-bridge circuit and a pulse transformer circuit to step it to a desired voltage, as shown in Fig. Fig. 2.12(a). One experimental setup developed in the ESP Lab of TU Delft is demonstrated in Fig. 2.12(b)[45], which can go up to 14 kV after the pulse transformer. Inherently, the test circuit is effective in material testing to generate a switching frequency of a few hundreds of kHz and rise time of hundreds of ns at MV range. It will be hard to scale up the voltage with the H-bridge and Pulse transformer design to MV equipment testing since the blocking voltage rating of available switches is limited.



(a)



(b)

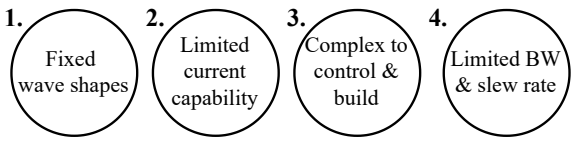
Figuur 2.12: H-Bridge and Pulse Transformer (a) Schematic (b) Experimental Setup [45].

2.4.5. LIMITATIONS OF THE EXISTING HV TEST SOURCES

From the discussion mentioned above about the existing HV test sources or newly developed test circuits, they face several limitations in four major dimensions, as summarized in a Fig. 2.13. Not all test sources suffer from all restrictions. However, as discussed in Section 2.3, it is increasingly important to solve all these challenges and provide a universal test circuit to test the HV grid assets with the actual voltage stresses to ensure the reliable operation of future electric power grids. With the massive improvement in commercial semiconductor devices, the same basic unit is used for developing a next-generation HV test source. The penetration of semiconductor devices is already visible with the last two test circuits. Apart from generating various wave shapes with much higher current capability, the power electronics-based test source can give better controllability during the breakdown of the test object for faster fault detection and for switching off the supply before the test object is completely destroyed. This helps greatly the failure investigation and root-cause analysis. Though the first prototype of the power electronics-based test source will be less efficient, accurate, and compact than conventional test sources, it will evolve as the technology matures. The above-described comparison is summarized in Table 2.2.

Tabel 2.2: Comparison of Conventional HV Test Sources versus Power Electronics-based Test Source

Conventional HV test sources	**Power Electronics-based test sources**
No flexibility to generate different waveforms	Programmable test source to generate arbitrary waveforms
Moving test object consumes time	Idea of using single test source for multiple tests
Less controllability over breakdown	More controllability over breakdown
Already efficient, accurate, and compact Hence, it is cost effective	It will require time to evolve mature, Hence costly
Several years of experience to operate Have proved reliable	Digital interface to operate Limited years experience with such equipment



Figuur 2.13: Limitations with the existing HV test source.

2.5. DIFFERENCE BETWEEN HV AWG AND ENERGY TRANSMISSION APPLICATION

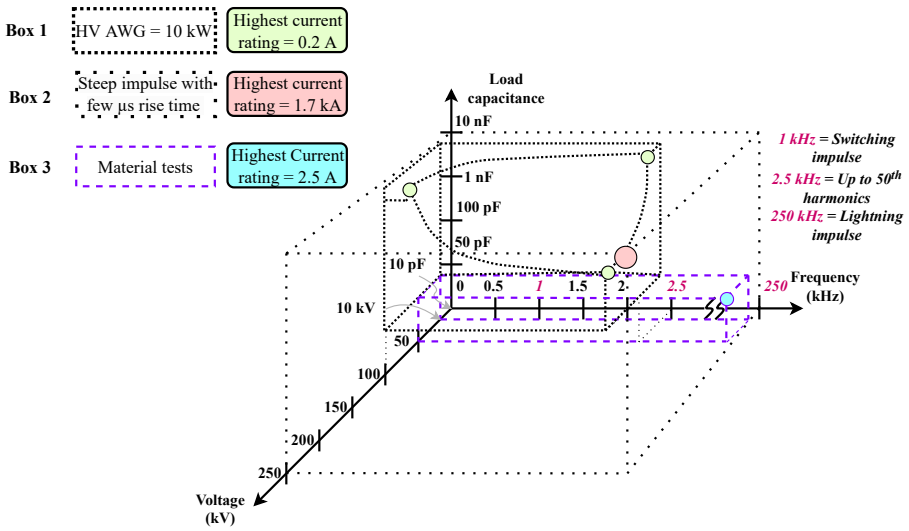
The HV AWG application poses some unique requirements to a power electronic converter compared to its usual power transmission application. The differences are summarized in the following section with bullet points.

- *The magnitude of power transfer*: For the AWG, the mentioned capacitive load will require a relatively low output current requirement of up to a few A. This small current constitutes the reactive power transfer to the equivalent capacitive load to build up voltage stresses. Hence, the active power requirement is low and represents only the losses within the converter and test object, which significantly differs from the HVDC transmission application, where active power flows are in the MW range [46].
- *Test object behaviour*: During an HV test, the breakdown of the test object or flashover is a likely phenomenon. Hence, the test source should supply sufficient energy for the breakdown and protect itself rapidly (in several μs or few ms). In power applications like renewable energy generation, it could be necessary that the power electronics supply energy for a fault in a coordinated matter that can last a relatively long time (several ms) without disconnection, e.g., Low Voltage Ride Through [47].
- *Frequency of use*: Generally, a power electronic converter integrated into the grid is used for continuous operation. A test source is used only for a fixed amount of time during working hours. The typical test duration for dielectric tests varies from 1 minute to 4 hours, except for long-term testing and pre-qualification tests.
- *Performance parameter*: The power efficiency of the converter is of utmost importance in energy transmission, but voltage accuracy is essential in HV testing. Since there is no intentional, active power transfer, specifications will be voltage and current capability, slew rate, and small- and large-signal bandwidth.

2.6. CONCLUSIONS OF HV TEST REQUIREMENTS WITH FUTURE OUTLOOK

Fig. 2.14 summarizes the HV test requirements, which show variable voltage and frequency operation along with a typical value of the load capacitance. Generally, the power electronic converter is designed for fixed output voltage and frequency. In this figure, three boxes are visible, showing different HV test requirements. The outer box with

a lighter dotted line is for the lightning impulse with 1.2 µs rise time across 10 nF load capacitance with the peak of 250 kV. As discussed in Section 2.2, the required LI voltage for 36 kV class equipment is in the range of 180 kV to 220 kV and the choice of 250 kV is made to keep a sufficient margin for future demands. Similarly, the second box with dark dots contains a maximum voltage of 100 kV considering the margin from 80 kV requirement. On the contrary to the LI tests, much less current, as little as 0.2 A, is sufficient for other test requirements, as shown in the dark-dotted box. The dark-dotted box has one corner missing to keep the DC source's power rating within 10 kW. The inner dark-dotted box and outer lighter-dotted box are referred to as Box 1 and Box 2, respectively, and these requirements are addressed separately in Chapters 3 and 5, respectively. The third box with purple color dotted line is for material tests that require comparatively less voltage (10 kV to 50 kV) and have low load capacitance (10 pF to 50 pF) and this is addressed in Chapter 4 of this thesis. The feasibility of the power electronics-based HV AWG is investigated for generating all these different wave shapes.



Figuur 2.14: Summary of HV test requirements for the power electronics-based HV AWG.

As the need for non-conventional and complex wave shape dielectric testing for the "tailor-made fit-for-purpose solutions" increases, an HV test source addressing all HV test requirements shown in Fig. 2.14 is of utmost importance for the electricity industry to prepare to transition to a more sustainable grid with massive RES integration. This is especially critical because the required level of investment is enormous, while the construction rate in the power system is lagging behind.

3

PROMISING HV AWG SOLUTION AND ITS DESIGN TRADE-OFFS

This chapter selects Modular Multilevel Converter (MMC) as most promising topology for the High Voltage (HV) Arbitrary Wave shape Generator (AWG) considering various advantageous offered by the topology. Hence, the main focus of this chapter is to investigate various design trade-offs of the MMC-based HV AWG for dielectric testing of various grid assets highlighted in Box 1 in Chapter 2. The HV AWG applications pose unique operating conditions to the MMC, which influences the selection of the various system parameters. This influence of the MMC system parameters is studied in detail analytically, with MATLAB-Simulink simulations and a down-scaled MMC prototype. Moreover, the challenges of realizing the full-scale MMC setup are discussed. The discussed design guidelines are applied to simulate the full-scale prototype with 67 submodules per arm.

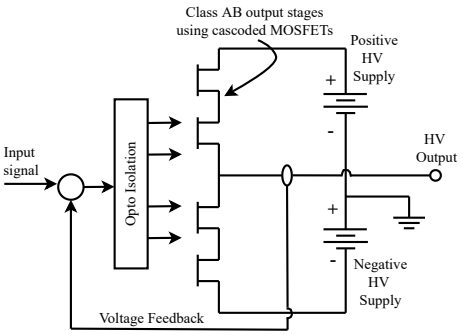
3.1. COMPARISON OF PROMISING SOLUTIONS

Based on the discussion in chapter 2, it follows that the semiconductor-based solutions may hold promise for overcoming some of the challenges with conventional test methods, and warrants a deeper feasibility analysis. Semiconductor devices can work either in the ohmic region (MOSFET) or saturation region (IGBT) with varied impedance

This chapter is based on:

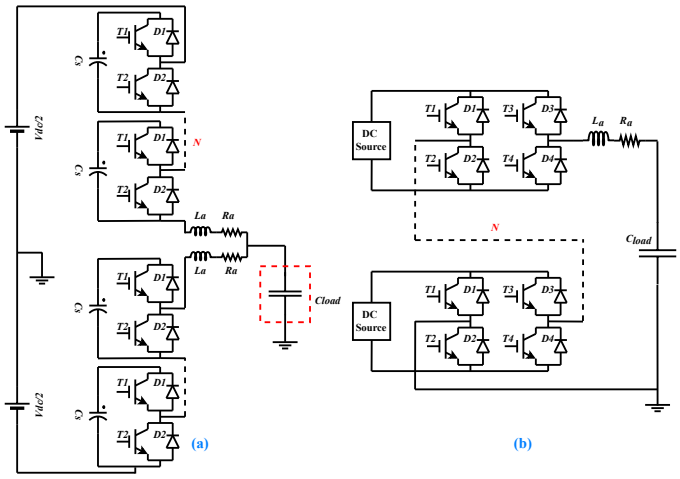
- D. A. Ganeshpure, T. B. Soeiro, M. G. Niasar, P. Vaessen and P. Bauer, "Design Trade-Offs of Modular Multilevel Converter-Based Arbitrary Wave Shape Generator for Conventional and Unconventional High Voltage Testing,ïn IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 584-605, 2021, doi: 10.1109/OJIES.2021.3125747
- D. A. Ganeshpure, T. B. Soeiro, M. G. Niasar, P. Vaessen and P. Bauer, "Modular Multilevel Converter-based Arbitrary Wave shape Generator used for High Voltage Testing,"2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC), 2021, pp. 124-131, doi: 10.1109/PEMC48073.2021.9432544.

or in the switching region where it conducts with a small resistance and blocks the voltage with negligible no current flowing. This leads to two different solution directions for Arbitrary Wave shape Generation (AWG). Based on the ohmic/saturation region of operation of semiconductor devices, HV amplifiers are designed, and they are used with a function generator as an AWG. The schematic of such an HV amplifier design is shown in Fig. 3.1, which contains the class AB amplifier configuration with cascaded MOSFETs [48]. In the ohmic/saturation region of operation, semiconductor devices exhibit relatively high losses [49], restricting the current flowing due to the heat generated in the HV amplifier. With an equivalent capacitive load, the bandwidth of the voltage waveform obtained from such an amplifier is limited [32] since the current flowing through the capacitive load is directly proportional to the frequency of the voltage waveform applied to it. Hence, this PhD thesis for the HV AWG investigates another solution direction of the multilevel switching converters.



Figuur 3.1: Schematic of HV amplifier circuit [48].

The most matured multilevel converter topologies for HV application are Modular Multilevel Converter (MMC) and Cascaded H Bridge (CHB) topologies, and their schematics are shown in Fig. 3.2. In the literature, there are few attempts to use multilevel converter topologies for arbitrary wave shape generations in applications like dielectric barrier discharge plasma actuator [50][51], HVDC valve testing [52], and HV testing [53]. Among MMC and CHB, mostly, CHB topology or its variants with different DC source implementations are chosen to implement an AWG over MMC. Technically, MMC and CHB have similar working principles since MMC has evolved from the CHB [54], and their qualitative comparison is presented in Table 3.1. A CHB converter has one converter arm, where each H-bridge submodule has a dedicated DC source. An MMC can be seen as two series-connected CHBs, without the distributed DC sources, and interconnected by a single DC voltage source [55]. For the AWG application, the MMC can be implemented using half-bridge submodules, unlike the intrinsic H-bridge circuit of the CHB.
Based on the comparison presented in the above Table 3.1, the primary difference lies with the DC source requirement in both solutions. For generating positive and negative waveforms, the MMC needs two isolated DC voltage sources or a single source with at least two split capacitors, each rated for the maximum generated voltage. In comparison, the many distributed DC sources in the CHB are rated for submodule voltage level



Figuur 3.2: Schematic of (a) MMC topology (b) CHB topology.

Tabel 3.1: Comparison of MMC and CHB Topology for the Same Output Voltage of $V_{DC}/2$ magnitude and for N submodules per arm.

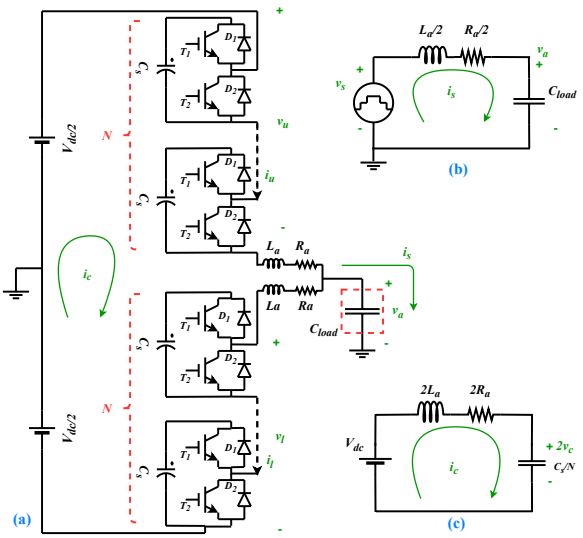
	MMC with Half Bridge	**CHB with Full Bridge**
No of Arms	Two arms and mid-point of the two arms is output	Single arm with series output
Switches	Quantity=4N	Quantity=4N
	$I_{switch}=I_{output}/2$	$I_{switch}=I_{output}$
	$V_{blk}=V_{DC}/N$	$V_{blk}=V_{DC}/2N$
	$P_{switch}=I_{output}V_{DC}/2N$	$P_{switch}=I_{output}V_{DC}/2N$
	1 switch is inserted	2 switches are inserted
Submodule capacitance	Quantity=2N	Quantity=N
	Actively, submodule capacitor voltage need to be balanced	Individual DC sources can balance voltage
Arm inductance	Quantity=2	Quantity=1
	2 times less energy content	2 times more energy content
Input DC Source implementation	1. Single input DC source with split capacitors 2. Two identical DC sources	N DC sources are required with isolation required for full output voltage
AWG Capability	Same voltage waveform capability with complex converter control	Same voltage waveform capability with complex DC Source design

and have a floating potential requiring insulation for the maximum generated voltage. This isolation for the maximum generated voltage will be necessary because each DC source is typically fed by a DC-DC isolated converter connected to the same low voltage battery [50] or medium voltage grid [56]. Therefore, the design scalability of the CHB becomes more challenging [50]. This design feature is crucial for customized tests

at different voltage levels for the application at hand. Hence, the MMC is chosen as an advantageous solution for an HV AWG.

3.2. SCHEMATIC OF MMC AS HV AWG

Fig. 3.3(a) shows the schematic of the MMC-based HV test source, which has been adapted from the original MMC topology for power transmission application[57][58]. It has a single phase of an MMC, a split DC source, the AC filter comprising the upper and lower arm inductance (L_a), and a capacitive load (C_{load}) representing the equivalent electrical model of the HV equipment. In the schematic, there is a series resistance (R_a) along with the arm inductance. This resistance helps to damp the oscillations generated due to the resonance between the arm inductance and the load capacitance. As discussed earlier in Section 2.6, the converter's power efficiency is not an important performance parameter. Hence, this passive damping methodology is chosen to control the MMC-based AWG in this chapter to study the design trade-offs. However, the losses in the arm resistors are closely monitored during the design process to ensure its practicability. Please note that this methodology of using resistive-based damping is a common practice in conducting HV tests [14].



Figuur 3.3: (a) MMC Schematic for HV AWG application (b) Output current circuit (c) Circulating current circuit.

By applying Kirchhoff's Voltage Law (KVL) in the upper and lower arm, dynamic equations of the MMC can be obtained, as shown in (3.1) and (3.2). Note that (3.3) can be obtained by subtracting (3.2) from (3.1), whereas (3.4) is derived by adding (3.1) and (3.2). Equations (3.3) and (3.4) are coupled equations with four variables v_u, v_l, i_u, and i_l, where $v_{u,l}$ is the sum of all submodule capacitor voltages in the upper and lower arm respectively, $i_{u,l}$ is the current flowing through the upper and lower arm respectively. By using

the linear transformation shown in (3.5) and (3.6), (3.3) and (3.4) can be simplified [55]. In (3.5) and (3.6), i_s represents the output current, v_s can be understood as the inner electromotive force (emf) generated due to the switching of the submodule capacitors, i_c represents the circulating current, which is driven by the circulating voltage (v_c). After substituting (3.5) and (3.6) into (3.3) and (3.4), partially decoupled differential equations can be obtained, as shown in (3.7) and (3.8):

$$\frac{V_{DC}}{2} - v_u - R_a i_u - L_a \frac{di_u}{dt} - v_a = 0 \tag{3.1}$$

$$\frac{V_{DC}}{2} - v_l - R_a i_l - L_a \frac{di_l}{dt} + v_a = 0 \tag{3.2}$$

$$v_l - v_u + R_a(i_l - i_u) + L_a\left(\frac{di_l}{dt} - \frac{di_u}{dt}\right) - 2v_a = 0 \tag{3.3}$$

$$V_{DC} - v_l - v_u - R_a(i_l + i_u) - L_a\left(\frac{di_l}{dt} + \frac{di_u}{dt}\right) = 0 \tag{3.4}$$

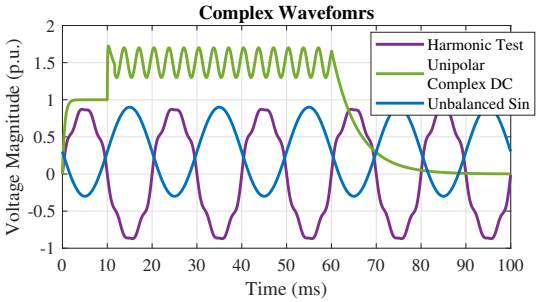
$$i_s = i_u - i_l \qquad v_s = \frac{(v_l - v_u)}{2} \tag{3.5}$$

$$i_c = \frac{(i_u + i_l)}{2} \qquad v_c = v_u + v_l \tag{3.6}$$

$$v_s - \frac{R_a}{2} i_s - \frac{L_a}{2} \frac{di_s}{dt} - v_a = 0 \tag{3.7}$$

$$\frac{V_{DC}}{2} - v_c - R_a i_c - L_a \frac{di_c}{dt} = 0 \tag{3.8}$$

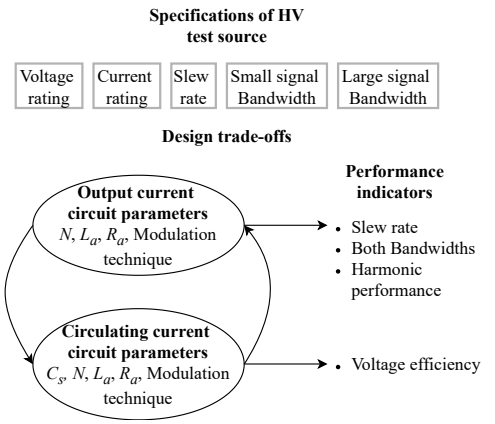
Equation (3.7) is a differential equation in terms of output current and inner emf. It can be represented with the RLC circuit, as shown in Fig. 3.3(b). Similarly, (3.8) is a differential equation in terms of circulating current and circulating voltage. If (3.8) is multiplied by two and the circulating voltage is represented by the voltage across the inserted submodule capacitance ($C_{eqv} = C_s/N$), it is possible to represent (3.8) with the RLC circuit, as shown in Fig. 3.3(c). In the output current of the circuit, the passive network (L_a, R_a, C_{load}) acts as a filter to v_s and attenuates the harmonics across the load capacitance. The observation above is important with respect to defining design constraints on the arm inductance and series resistance. The output current flowing through the arm inductance and resistances is responsible for building the desired voltage stress across the load capacitance. The upper and lower arm current charge or discharge the inserted submodule capacitors over their average value. The change in the submodule capacitor voltage will change the inner emf (v_s) and, in turn, the output voltage. This is how the output current circuit and the circulating current circuit are coupled with the submodule capacitor voltage feedback, and this partial coupling is shown with purple boxes in Fig 3.3. Nevertheless, it is important to simplify the complex MMC structure into these simple circuits to understand the design trade-offs and to provide an optimal design of the test source, which is covered in the next section. Among the many complex waveforms illustrated in Fig. 2.7 with Chapter 2, three waveforms are selected to demonstrate the various design trade-offs. The selected waveforms are shown in Fig. 3.4 which covers unipolar, bipolar and unbalanced waveforms.



Figuur 3.4: Complex waveforms demonstrated in this Chapter.

3.3. DESIGN TRADE-OFFS IN THE CHOSEN SOLUTION

Based on two simplified circuits, design trade-offs of the MMC-based AWG are summarized in Fig. 3.5, along with the specifications and the performance indicators. As discussed in the previous section, the output current circuit dictates the harmonic performance of the output voltage waveforms. Hence, the small- and large-signal bandwidth and slew rate will be determined by the component of the output current circuit, i.e., the number of submodules (N), L_a, R_a, and the modulation techniques. Moreover, the submodule capacitor voltages are balanced by the circulating current circuit, which is essential for the voltage magnitude accuracy. This section will analyze different design trade-offs present with the choice of modulation technique, L_a, R_a, N, switches, submodule capacitance, control system, control hardware, and overall control architecture.



Figuur 3.5: Specifications and design trade-offs of MMC-based AWG.

3.3.1. MODULATION TECHNIQUES

There are a wide variety of modulation techniques available for the MMC in literature. They can be broadly classified based on the switching frequency generated in v_s as high-

frequency or low-frequency modulation techniques. High-frequency modulation techniques generate Pulse Width Modulation (PWM) waveform, with the switching frequency typically in kHz range. In contrast, low-frequency modulation techniques generate a staircase signal with a switching frequency comparable to the fundamental frequency.
High-frequency modulation techniques can be further divided into carrier-based and space vector modulation techniques. As the name suggests, carrier-based modulation compares carrier waveforms with the reference waveform to control the switches. For each submodule, carrier waveforms can be either phase-shifted in time or level-shifted in amplitude. The phase-shifted carrier makes Phase Shift Carrier (PSC) modulation [59], and it naturally utilizes all submodules evenly. The Level Shifted Carrier (LSC) modulation can be divided into three different types such as phase disposition, Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) [60]. LSC modulation has one remarkable disadvantage that it uses the submodule unevenly. To reduce the computational efforts for the controller, [61] discusses the implementation of phase disposition LSC PWM using single carrier waveform. The effect of variable modulation index can be solved by adapting dynamic carrier overlapping modulation techniques as implemented in [62]. In space vector modulation (SVM), gate pulses for switches are calculated by representing the desired output voltage vector in a multiple layered hexagon structure, as discussed in [58][63]. The computation efforts in SVM modulation are simplified in [64] to make it suitable for MMC. There are multiple publications available discussing novel updates to the above-mentioned techniques [65][66].
Among the various high-frequency modulation techniques, PSC is chosen to evaluate for application of AWG due to its characteristics of even use of submodules. This special characteristic can naturally balance the submodule capacitor voltage facilitating on improving the active control for the HV AWG application [67]. For other techniques, an external controller or sorting algorithms are required to balance the submodule capacitor voltages [68][69].
Low-frequency modulation techniques includes the Selective Harmonic Elimination (SHE) and Nearest Level Control (NLC). In SHE, the gate pulses are pre-programmed to obtain the desired harmonic performance without comparing the carrier waveforms to the reference waveform [70]. NLC calculates the gate pulse by rounding off the reference waveform to the desired number of submodules [71]. This gives an easy and simple solution for gate pulse calculations in the HV MMC applications where large number of submodules are implemented. Hence, this is chosen in this chapter among the low-frequency modulation techniques to verify the features of this technique for the HV AWG application. It is important to note that NLC, similarly to LSC, requires either a controller or sorting algorithm to balance the capacitor voltage.

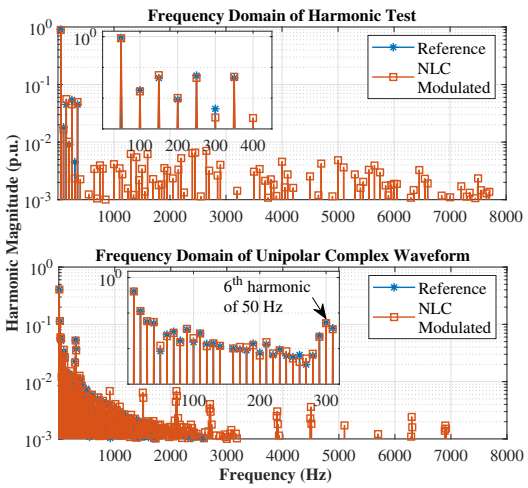
NEAREST LEVEL CONTROL (NLC)

NLC calculates the number of submodules to be inserted using either equation (3.9) or (3.10) and assign gate pulses accordingly. Equation (3.9) results in (N+1) number of output voltage levels [71], whereas equation (3.10) generates (2N+1) number of output voltage levels [72].

$$n_{u,l} = round_{0.5}\left(\frac{N(V_{DC} \mp 2V_{ref})}{2V_{DC}}\right) \tag{3.9}$$

$$n_{u,l} = round_{0.25}\left(\frac{N(V_{DC} \mp 2V_{ref})}{2V_{DC}}\right) \tag{3.10}$$

Fig. 3.6 show the frequency domain analysis of the complex waveforms depicted in Fig. 3.4. Since the unbalanced sinusoidal waveform does not have a complex frequency spectrum, its frequency domain analysis is not elaborated here. They are generated with N = 12, and (2N + 1) NLC modulation technique. In Fig. 3.6, it can be observed that the frequency domain waveform of reference and that of NLC modulated does not match for both harmonic test and unipolar waveforms. The mismatch is more prominently visible in the zoomed picture of the harmonic test waveform. Please note that the y axis scale used in Fig. 3.6 is logarithmic, and the small visible difference in this scale will already give an error in the range of 10 %. For the harmonic test, the error for up to the third harmonics needs to be limited to 1 %. Additionally, the harmonic test waveform contains harmonics up to the 7^{th} order, and the variable frequency operation nature of NLC inserts relatively high magnitude of harmonics close to the reference value, e.g., the 8^{th} harmonic, which makes the filtering requirement significantly high. For the unipolar complex waveform, the NLC modulated waveform has higher switching harmonics present in the large baseband harmonics of the reference waveform. This makes it extremely difficult to remove the switching harmonics introduced by the NLC operation. Harmonics introduced by NLC will reduce in magnitude as the number of submodules is increased. Unfortunately, they are not considerably shifted too far on the right side of the highest order of the reference harmonic, and hence they still can interfere with the baseband harmonics. The switching harmonics present due to NLC is difficult to remove for waveforms with a complex frequency spectrum, and one example is shown in [73]. The Total Harmonic Distortion (THD) of these NLC modulated waveforms are within 5 %, but it affects the type of electric stress applied to the insulation under stress, as discussed in detail in Appendix B.

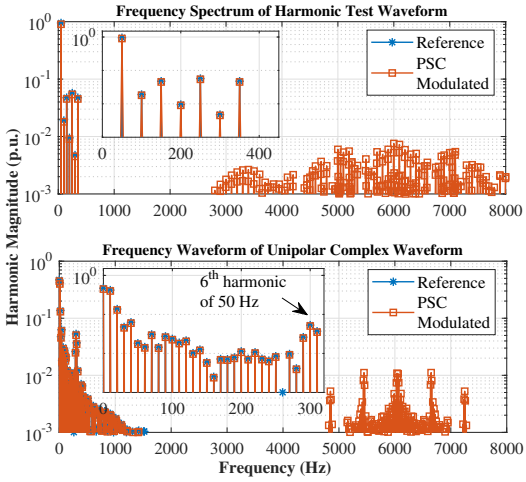


Figuur 3.6: Frequency spectrum of NLC modulated waveforms which were shown in Fig. 3.4.

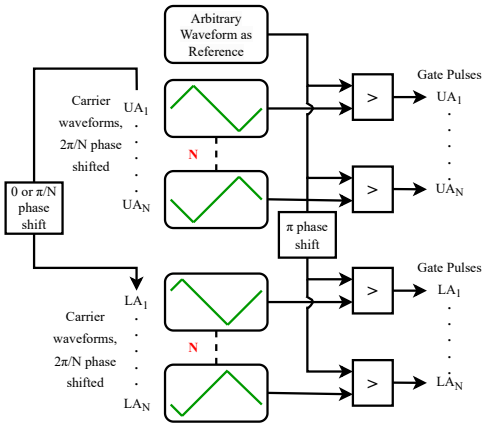
PHASE SHIFT CARRIER (PSC)

In PSC, a traditional sine-triangle double edge modulation technique is used where each submodule is assigned with a different carrier signal. They are phase-shifted between them by $2\pi/N$. These phase-shifted carrier signals move the carrier harmonics to the N^{th} carrier frequency. The upper arm and lower arm can use the same carrier signals, or they can be phase-shifted by π/N. With π/N phase difference in the case of N is even, and 0 phase difference in the case of N is odd, generates $(2N+1)$ number of levels in the output voltage of the converter [59]. This further improves the harmonic spectrum of the output voltage, moving the first carrier frequency to $2N^{th}$ of the fundamental carrier frequency. This specific phase difference between the upper and the lower arms ensures that the upper and lower arm submodules switch at different time instant, generating a higher number of levels and cancelling out more harmonics.

Fig. 3.7 shows the frequency domain analysis of the complex waveforms depicted in Fig. 3.4. Since the unbalanced sinusoidal waveform does not have a complex frequency spectrum, its frequency domain analysis is not elaborated here. They are generated with N = 12, PWM carrier frequency of 252 Hz, and $(2N+1)$ PSC modulation technique. In Fig. 3.7, it can be observed that the frequency domain waveform of the reference and that of the PSC modulated match significantly for both harmonic test and unipolar complex waveform. This means that the switching harmonics produced due to PSC do not interfere with the baseband harmonics of the complex waveforms. The separation of switching harmonics from baseband harmonics is crucial for AWG application to generate accurate output wave shapes. Hence, this modulation technique is more beneficial than NLC, and it is chosen for the HV AWG studied through out this PhD thesis. The implementation of the PSC modulation technique is illustrated with a block diagram, as shown in Fig. 3.8.



Figuur 3.7: Frequency spectrum of PSC modulated waveforms which were shown in Fig. 3.4.



Figuur 3.8: Block diagram of the PSC modulation techniques.

3.3.2. ARM INDUCTANCE AND SERIES RESISTANCE

Since the equivalent passive network load acts as a series RCL filter, it is possible to choose the correct values of L_a and R_a to attenuate the unwanted high-frequency harmonics from the output voltage waveform. This is important for the HV AWG application because the waveform determines the electric stress applied to the DUT, and these voltage harmonics may cause unwanted additional dielectric stress in the test subject [3][74]. More sophisticated AC filter topologies commonly used in renewable energy generation such as the third-order LCL filter [75][76] add too many fully-rated components, particularly the full-rated voltage filtering capacitors, leading to increased the system's complexity and cost. Hence, the transfer function of the selected equivalent second-order RLC low-pass AC filter as necessary for the system design is shown in (3.11). The condition to remove the unwanted voltage harmonics is shown in (3.13), and the suppressing frequency ($f_{suppres}$) depends on the implemented modulation technique. For example, in Fig. 3.7, the undesirable voltage harmonics starts in the frequency of about 3 kHz to 4 kHz, and this frequency can be used as $f_{suppres}$. Additionally, L_a and R_a influence the small-signal bandwidth (f_{3dB}), large-signal bandwidth ($f_{1\%err}$), and slew rate for the given load capacitance C_{load}. In an open loop operation of the MMC-based AWG, both small- and large-signal bandwidths can be quantified, as shown in (3.12) and (3.15) from (3.11). Additionally, (3.14) defines damping requirement [77] for the second-order systems, which is important for the stable operation of the MMC with capacitive load. The damping requirement is derived based on the critical damping condition on the second-order control system. From the four established requirements in (3.12)-(3.15), large-signal bandwidth (3.12) and suppressing frequency (3.13) can be used to choose L_a and R_a. If the chosen resistance satisfies (3.14), then the choice of L_a and R_a can be used. If these equations are analyzed, it can be understood that the magnitude of the arm inductance and load capacitance should be lower to obtain larger signal bandwidths and a higher slew rate. The value of the series resistor changes as the value of arm inductance and load capacitance change as per (3.14). With lower values of arm inductance and load capacitance, the suppressing frequency is increased. High suppressing

frequency requires higher equivalent switching frequency and higher accuracy on the controller. These trade-offs on the filter design and definition of the above-mentioned terminologies are summarized in Fig. 3.9, where the series damping resistance for all 4 combinations of L_a and C_{load} is chosen as per (3.14).

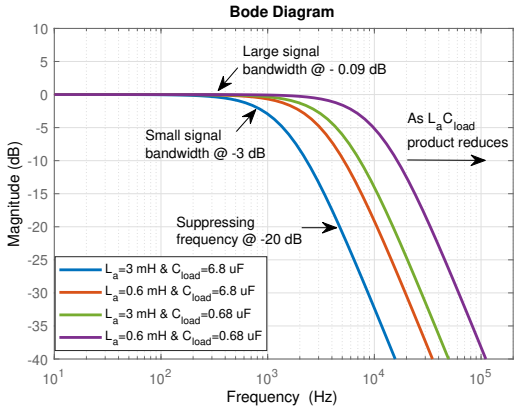
$$\frac{V_a(s)}{V_s(s)} = \frac{1}{s^2 \frac{L_a}{2} C_{load} + s \frac{R_a}{2} C_{load} + 1} \tag{3.11}$$

$$abs\left(\frac{V_a(s)}{V_s(s)}\right)_{@f=f_{1\%err}} = 0.99 \tag{3.12}$$

$$abs\left(\frac{V_a(s)}{V_s(s)}\right)_{@f=f_{suppres}} = 0.1 \tag{3.13}$$

$$R_a \geq \sqrt{(\frac{8L_a}{C_{load}})} \tag{3.14}$$

$$abs\left(\frac{V_a(s)}{V_s(s)}\right)_{@f=f_{3dB}} = 0.708 \tag{3.15}$$



Figuur 3.9: Effect of L_a and C_{load} variation on the filter profile.

3.3.3. NUMBER OF SUBMODULES AND SWITCHES

The influence of the number of submodules on the modulation technique and filtering requirement is discussed in the previous two sections. However, the number of submodules is designed based on the DC link voltage and blocking capability of the commercially available switches. Table 3.2 shows the required blocking voltage capability for the given number of submodules for the 200 kV DC link. The DC link voltage is chosen so that 100 kV output voltage is produced. For the MMC with the half-bridge submodule implementation and the mid-point connection, as shown in Fig. 3.3, the DC link voltage must be twice the output voltage rating. In the Table 3.2, it is visible that the blocking voltage capability needs to be higher. This requirement resembles that of the HVDC energy

transmission application [78]. However, the power modules designed for the HVDC application are rated for a very high current (kA range). Since the maximum current rating requirement for this new application is 0.2 A, discrete switches are preferred. Apart from the high blocking capability, the switches should have high switching frequency capability to get higher large-signal bandwidth. For 2.5 kHz large-signal bandwidth, the switching frequency should be much higher than 2.5 kHz. Available discrete MV IGBTs (2.5 kV, 3.3 kV, 4 kV, 4.5 kV) can operate efficiently less than 5 kHz switching frequency [79]. With the given constraints of voltage rating, switching frequency, and current requirement, the choice of Silicon Carbide (SiC) MOSFETs is advantageous. These devices are readily commercially available in TO-package for up to 3.3 kV rating, e.g., G2R120MT33J from GeneSiC Semiconductor. Though MV SiC MOSFETs (10 kV, 15 kV) are pre-released by CREE-WOLFSPEED [80], they are not yet ready commercially.

Tabel 3.2: Number of Submodule and Voltage Rating per Submodule

Number of submodules	Voltage rating per submodule (kV)
12	16.7
33	6
50	4
67	3
100	2
200	1

3.3.4. SUBMODULE CAPACITANCE AND ITS VOLTAGE BALANCING

Next to the switches, the choice of submodule capacitance is crucial in determining voltage efficiency, size, and cost of the MMC-based AWG. Since the converter is not designed for active power transfer, the traditional condition of the total energy stored in all submodule capacitance per MVA rating of the converter [81] might not be valid. Another important usage of submodule capacitance is to keep its voltage ripple within a limit such as 10 % of the average submodule capacitor voltage [82][83]. Many researchers have worked on deriving the submodule capacitor voltage for MMC with HVDC power transmission application [55][84][67]. However, the same ripple expression can not be directly used for HV AWG application since hardly any active power is being transferred to the the equivalent capacitive load. Hence, the voltage ripple expressions are derived in the following section for the equivalent capacitive load and non-sinusoidal wave shape. The partially coupled and complex dynamic model of MMC is simplified by averaging principle [55]. With this principle, it is possible to simplify the product of two continuous varying variables ($n^i_{u,l}$ and $v^i_{u,l}$) using (3.16) into (3.17). In these equations, $n^i_{u,l}$ is the modulation index of i^{th} submodule from the upper and lower arm. The averaging principle is used to calculate continuous modulation indices for the upper and lower arm, which is defined as $n_{u,l}$. Additionally, $v^i_{u,l}$ is the individual submodule capacitor voltage of i^{th} submodule from the upper and lower arm. $v^{avg}_{u,l}$ is the average total submodule capacitor voltage in the upper and lower arm. The same principle can be used to derive the capacitor voltage dynamic equations, as shown in (3.18). Equation (3.19) is derived for the upper and lower arm capacitor voltage ripple by substituting the upper and lower arm

current expressions from (3.5) and (3.6) in (3.18). Generally, in the HVDC transmission application, the average circulating current magnitude I_c is determined by the input and output power balance equation. If it is applied for HV testing application with capacitive load $V_{DC}I_c = V_aI_s\cos(\phi)$, the average circulating current is found to be zero since $\cos(\phi)$ is zero. Please note that the losses occurring in the arm resistors are neglected in this mathematical derivation considering its small magnitude.

$$n_{u,l} = \frac{1}{N}\sum_{h=1}^{N} n_{u,l}^{i} \qquad v_{u,l}^{i} = \frac{v_{u,l}^{avg}}{N} \tag{3.16}$$

$$v_{u,l} = \sum_{h=1}^{N} n_{u,l}^{i} v_{u,l}^{i} = n_{u,l} v_{u,l}^{avg} \tag{3.17}$$

$$C_s \frac{dv_{u,l}^{i}}{dt} = n_{u,l}^{i} i_{u,l}^{i} \qquad \frac{C_s}{N}\frac{dv_{u,l}}{dt} = n_{u,l} i_{u,l} \tag{3.18}$$

$$\frac{C_s}{N}\frac{dv_{u,l}}{dt} = n_{u,l}\left(\pm\frac{i_s}{2} + i_c\right) \tag{3.19}$$

Zero average circulating current can be interpreted as this current is present only to charge or discharge the inserted submodule capacitor voltage without having a large DC component, unlike the traditional application of MMC. As per the circulating current circuit in Fig. 3.3(c), this circulating current balances the voltage between the DC link and inserted submodules. Hence, it is possible to neglect the circulating current from the ripple expression in (3.19). Assuming the output voltage is an arbitrary voltage waveform, it is represented as Fourier series, as shown in (3.21) and (3.22), where the modulation index is represented as m_a. Additionally, the output current and insertion indices are derived from (3.21) and (3.22) in (3.23) and (3.24), respectively. When equation (3.23) and (3.24) are substituted in (3.20), the time derivative of capacitor voltage is derived and simplified in (3.25). For a sinusoidal waveform, it is possible to derive the analytical equation of the total capacitor voltage, as shown in (3.26). For non-sinusoidal waveforms, MATLAB or Maple software can solve the integration numerically.

$$\frac{C_s}{N}\frac{dv_{u,l}}{dt} = n_{u,l}(\pm\frac{i_s}{2}) \tag{3.20}$$

$$f(t) = \frac{a_0}{2} + \sum_{h=1}^{\infty}(a_h cos(hwt) + b_h sin(hwt)) \tag{3.21}$$

$$v_a = m_a\frac{V_{DC}}{2}f(t) \tag{3.22}$$

$$i_s = m_a\frac{V_{DC}}{2}wC_{load} \times \sum_{h=1}^{\infty}(-a_h hsin(hwt) + b_h hcos(hwt)) \tag{3.23}$$

$$n_{u,l} = \pm\frac{m_a f(t)}{2} + \frac{1}{2} \tag{3.24}$$

$$\frac{C_s}{N}\frac{\mathrm{d}v_{u,l}}{\mathrm{d}t} = [\pm\frac{m_a V_{DC} w C_{load}}{4} \times \sum_{h=1}^{\infty} h(b_h cos(hwt) - a_h sin(hwt))] \times [\frac{m_a(\frac{a_0}{2} + \sum_{h=1}^{\infty}(a_h cos(hwt) + b_h sin(hwt))) \pm 1}{2}] \tag{3.25}$$

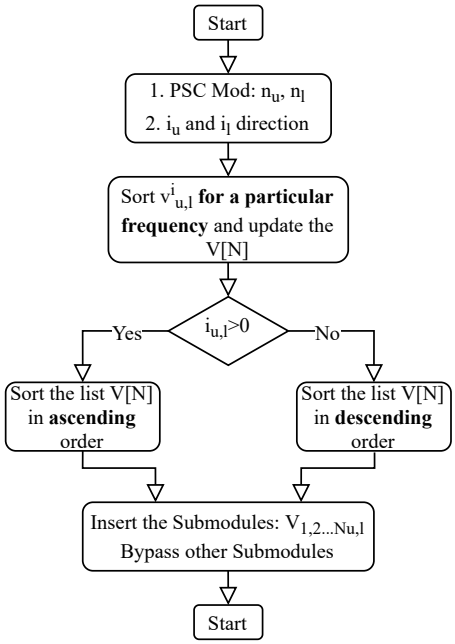
$$v_u(t) - V_{DC} = \frac{m_a^2 V_{DC} C_{load} N}{32 C_s}(1 - cos(2wt)) + \frac{m_{req} V_{DC} C_{load} N}{8 C_s} sin(wt) \tag{3.26}$$

$$v_u^i(t) - v_u^{avg} = \frac{m_a^2 V_{DC} C_{load}}{32 C_s}(1 - cos(2wt)) + \frac{m_{req} V_{DC} C_{load}}{8 C_s} sin(wt) \tag{3.27}$$

From voltage ripple expression per submodule in (3.27), it is clear that the ripple magnitude is independent of the frequency since the charge time product remains the same for different frequencies. However, it is mainly dependant on the ratio of the load capacitance and submodule capacitance and the DC link voltage. The derived expression of the ripple is verified in Sections 3.4 and 3.5 with the scaled-down prototype and the full-scale simulation results. It is important to note that the capacitor voltage ripple is kept within 1 % of the average capacitor voltage for more accurate output voltage waveforms. This strict ripple restriction does not require a large value of submodule capacitance since the HV AWG needs a low current magnitude. Hence, the full-scale prototype will have submodule capacitance in μF range, which is proved to be feasible later in Section 3.5. With negligible circulating current, the submodule capacitor voltages are naturally balanced within MMC without the strict requirement of an arm energy controller [69] or sorting algorithm [68][85]. Because, the PSC modulation technique naturally distributes submodule insertion and bypassing evenly [67]. Additionally, if the switching frequency is chosen to be a non-integer multiple of the fundamental frequency [59] with proper selection of the submodule capacitance, it is possible to have improved balanced capacitor voltages. However, the open-loop control of submodule capacitor voltage can lead to slightly different average capacitor voltage values due to small variations in each submodule hardware such as different delay in gate driver, tolerances in the submodule capacitance value, etc. Hence, a combination of both techniques is recommended here to improve the reliability of the HV AWG test source. In this chapter, a simple sorting is implemented, where upper and lower arm capacitor voltages are sorted for desired frequency, and the gate pulses are assigned based on the direction of arm current and sorted capacitor voltages. The flowchart of the implemented sorting algorithm is illustrated in Fig. 3.10.

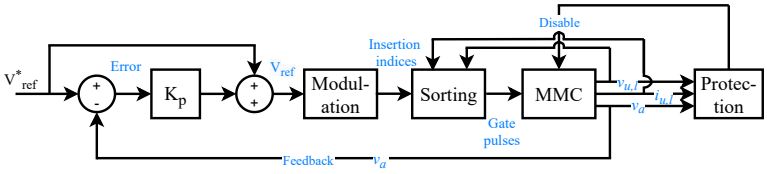
3.3.5. CONTROL SYSTEM

Since the HV AWG application does not need to control the power transfer, the control system block for MMC is adapted for accurate voltage waveform generation, as shown in Fig. 3.11. The feedback control of the voltage across the load ensures an acceptable steady-state error, and the measurement of the output current can provide fast protection in case of faults, e.g., flashover. Fig. 3.11 presents a simplified control system implemented and tested in the scaled-down prototype of the MMC-based AWG that will be discussed in Section 3.4. The accuracy of the output voltage waveforms is improved



Figuur 3.10: Flowchart of the implemented sorting algorithm.

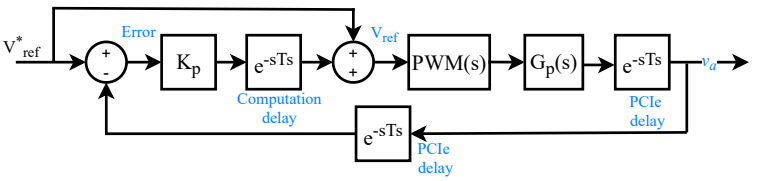
with the reference voltage feedforward loop. This particular controller is chosen for its simplicity and stable operation, and as it will be shown in the next session, it gives good results. Additionally, the submodule capacitor voltages are balanced using a simple selective sorting mechanism as discussed in Section 3.3.4.



Figuur 3.11: Control system of the MMC-based AWG.

Apart from the parameters discussed in Section 3.3.2, the available bandwidth for the generated voltage waveform gets affected by the closed-loop control. Its effect can be studied using the closed-loop block diagram of the MMC-based AWG in the continuous time domain, as shown in Fig. 3.12. This block diagram consists of the computation and communication delays named Peripheral Component Interconnect Express (PCIe). These delays are represented as exponential functions, and they depend upon the sampling period (T_s) implemented in the controller. Equation (3.11) represents the plant's transfer function ($G_p(s)$). The generation of PWM in the continuous time domain can be represented as shown in (3.28) [86]. The modulation index (m_a) and the sampling

period determine the magnitude of this transfer function. Additionally, the pulse width modulator samples the data with Zero-Order Hold (ZOH) function. Hence, it is fully represented in (3.28). The closed-loop transfer function of MMC is derived as shown in (3.29). This transfer function gives the small- and large-signal bandwidth, including the controller. It is visible that the sampling period plays an important role in determining the final bandwidth of the test source and its effect on the scaled-down prototype, and the full-scale prototype is studied in Section 3.4 and 3.5, respectively.



Figuur 3.12: Block diagram of the control system of the MMC-based AWG.

$$G_{PWM}(s) = \frac{m_a G_{zoh}(s)}{T_s} = \frac{m_a(1-e^{-sT_s})}{sT_s} \tag{3.28}$$

$$\begin{aligned} \frac{V_a(s)}{V_s(s)} &= \frac{G_{sys}(s)}{1+G_{sys}(s)} \\ G_{sys}(s) &= (1+G_{cd}(s))\frac{G_{pFB}(s)}{1+G_{pFB}(s)} \\ G_{cd}(s) &= K_p e^{-sT_s} \\ G_{pFB}(s) &= G_{PWM}(s)G_p(s)e^{-2sT_s} \end{aligned} \tag{3.29}$$

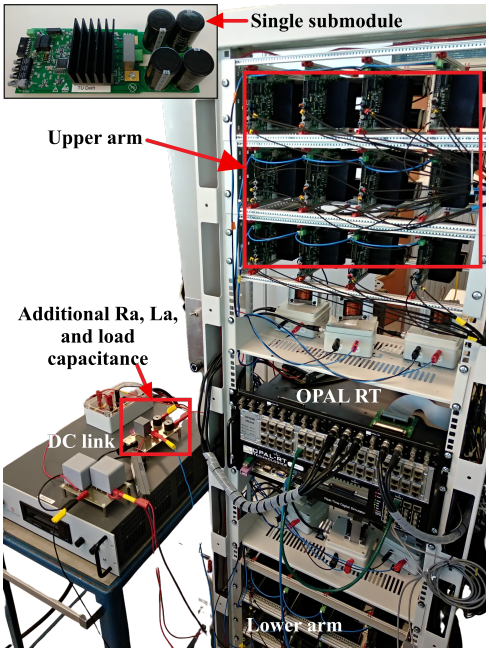
3.4. ANALYTICAL, SIMULATION AND HARDWARE RESULTS

The above-discussed design trade-offs of the MMC-based AWG are verified with the MATLAB-Simulink simulation and the existing scaled-down MMC prototype. This scaled-down MMC has 12 submodules where a half-bridge topology is implemented using the IGBTs PS219B4-S/-AS/-CS. It is tested with 300 V DC link voltage which can generate peak output voltage of 150 V. The load capacitance is chosen to be 6.8 µF to keep the same current rating as that of the full-scale prototype where the output voltage is 100 kV, and the load capacitance is 10 nF. This hardware setup is controlled using the OPAL-RT simulator (OP5600). Each submodule receives an enable and gate pulse signal and sends back the measurements of the submodule capacitor voltage via a digital voltage oscillator and fiber optics. The measurements of the output voltage across the load capacitance, the DC link voltage, and the arm currents are fed back to the OP5600. With the existing scaled-down prototype of MMC, the design trade-offs of the MMC-based AWG are demonstrated with 150 V output voltage rating, 6.8 µF load capacitance, and 200 Hz large-signal bandwidth. For these specifications, the value of L_a and R_a can be calculated to be 3 mH and 60 Ω, respectively, from equations (3.12) and (3.13). The above-

Tabel 3.3: System Parameters of Scaled-down MMC Setup

No.	Description	Symbol	Values
1.	DC-link voltage	V_{DC}	300 V
2.	Maximum output voltage	V_a	150 V
3.	Modulation index	m_a	0.9
4.	Number of submodules	N	12
5.	Switching frequency	F_s	1002 Hz
6.	Large-signal bandwidth (Open loop)	$f_{1\%err}$	200 Hz
7.	Submodule capacitance	C_s	4 mF
8.	Arm inductance	L_a	3 mH
9.	Arm resistance	R_a	60 Ω
10	Load capacitance	C_{load}	6.8 µF

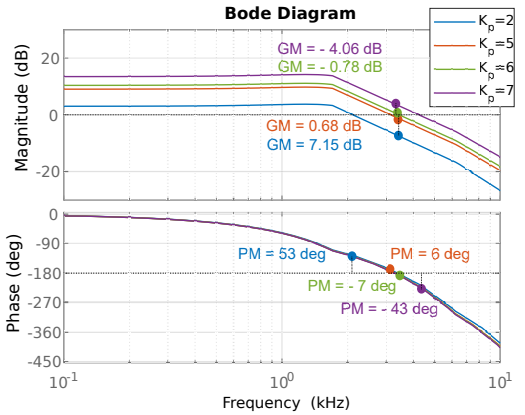
mentioned system description is summarized in Table 3.3. Fig. 3.13 presents the experimental hardware of the scaled-down MMC prototype.



Figuur 3.13: Experimental hardware setup.

The controller and various delays do impact the small- and large-signal bandwidth depending upon the sampling period, as discussed in (3.29). For the scaled-down prototype operated by OPAL-RT, the minimum obtained sampling period is 20 µs. Additionally, the parameter variations on the controller stability are studied using gain and phase margins, as shown in Fig. 3.14. From this figure, it is clear that the maximum proportional gain possible is five, after which the control system is unstable with ne-

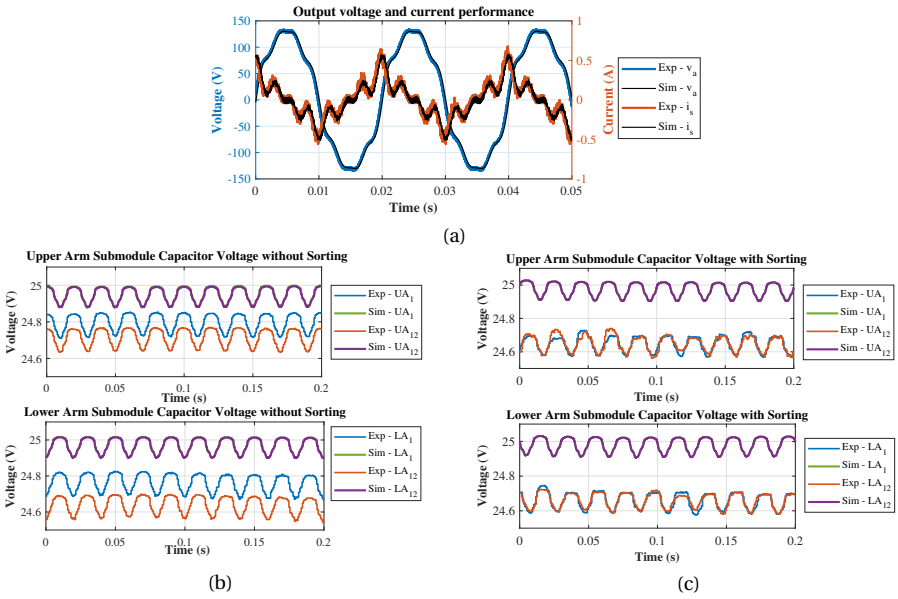
gative gain and phase margin [87]. Hence, the small- and large-signal bandwidths are calculated for the same gain and 4.04 kHz, and 4.49 kHz are the obtained values for both bandwidths. These bandwidths are higher than the large-signal bandwidth calculated for the open-loop. Hence, the closed-loop is not affecting the bandwidth for generating accurate waveforms up to 200 Hz.



Figuur 3.14: Variations of the proportional gain on controller/system stability.

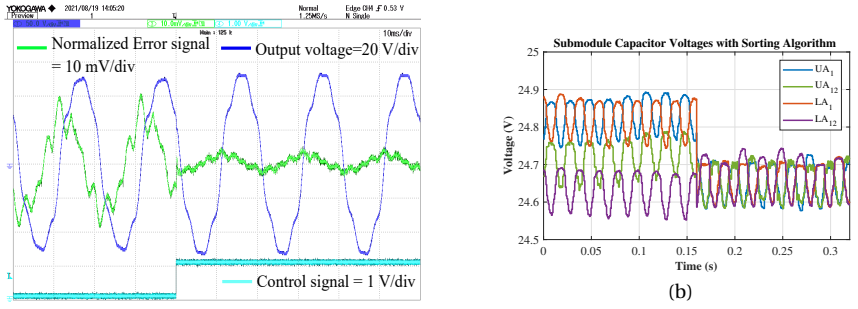
The performance of the scaled-down MMC-based AWG is demonstrated with three waveforms, i.e., harmonic test waveform, unipolar DC waveform, and unbalanced sinusoidal waveform, as discussed in Section 3.2. Other periodic and complex waveforms are shown in the appendix A. First, the simulation results are compared with the scaled-down prototype for the harmonic waveform in Fig. 3.15 for output voltage, output current, and submodule capacitor voltages. For clarity in the waveforms, only 4 submodule capacitor voltages are plotted i.e., Upper Arm 1 (UA_1), Upper Arm 12 (UA_{12}), Lower Arm 1 (LA_1), Lower Arm 12 (LA_{12}). It is clear from Fig. 3.15 that the MATLAB-Simulink simulations with ideal switches match well the experimental results. Small variations in the average submodule capacitor voltages in both arms can be attributed to the small tolerances present in the different submodules in terms of PWM delays in gate driver, submodule capacitance values, etc. Please note that the difference in average value of UA_1 and UA_{12} is only 0.33 %. These non-idealities present in different submodules can be eliminated by implementing a sorting algorithm as discussed in Section 3.3.4, and its performance is shown in Fig. 3.15(c). From this figure, it can be concluded that the sorting algorithm removes the non-idealities present in each submodule and brings the average values of all submodules together.

Furthermore, Fig. 3.16(b) shows the sorting algorithm working and how it brings the submodule capacitor voltage together dynamically. For simplicity, the submodule capacitor voltages are sorted continuously equivalent to a simulation step of 20 µs. Additionally, Fig. 3.16(a) illustrates the performance of the proposed proportional controller. In this figure, the closed-loop control is enabled at 40 ms. The error signal is normalized to 1 with a factor of 150 V. When the control is enabled, the error is reduced significantly,

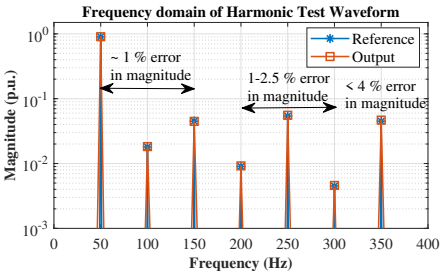


Figuur 3.15: Comparison of simulation results with experimental results for Harmonic test waveform in time domain (a) Output voltage and current, Submodule capacitor voltage (b) without sorting (c) with sorting.

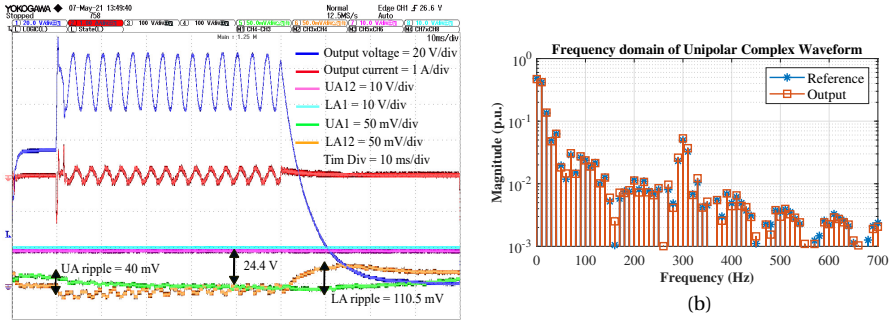
correcting the output voltage waveform. Moreover, the performance of this waveform is verified with the reference waveform in the frequency domain in Fig. 3.17. With correct values of filter and closed-loop control, it is possible to keep the error in the inserted harmonic magnitude around 1 % for up to third harmonics and within 4 % for higher harmonics. As per the design condition applied by (3.12), the error in the first three inserted harmonics remains around 1 %. Though the condition of 1 % error was applied till 4th harmonic, the slightly higher error of 1.73 % is obtained in the 4th harmonic due to its small magnitude (0.5 % of fundamental magnitude).



Figuur 3.16: Performance of (a) Proportional controller (b) Sorting algorithm implementation for Harmonic test waveform.



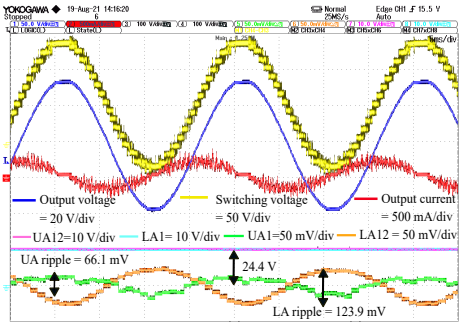
Figuur 3.17: Harmonic test waveform in frequency domain.



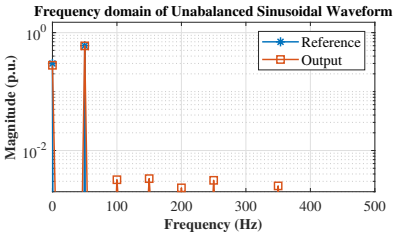
Figuur 3.18: Unipolar complex waveform in (a) Time domain (b) Frequency domain.

Second, Fig. 3.18(a) presents an oscilloscope screenshot of the unipolar complex waveform generated from the scaled-down prototype. The output current and voltage are measured from external voltage and current probes. The pre-selected submodule capacitor voltages (UA_1, UA_{12}, LA_1, LA_{12}) are acquired in real time from the OPAL-RT measurements. Hence, these waveforms are scaled down to stay within the limits of the analog output ports of the OPAL-RT. The submodule capacitor voltages are normalized to 10 with a factor of 2.5. The bottom waveforms are submodule capacitor voltages from 1^{st} submodule from the upper arm and the 12^{th} submodule from the lower arm. From this screenshot, it is visible that the ripple of the upper and lower arm submodules are different. It is because of the unipolar waveform. When an unipolar waveform is generated from the MMC, one of the arms (in this case: UA) is not get fully utilized, and only a maximum of half of its number of submodules are inserted. However, this does not affect the capacitor voltage balancing. Additionally, this waveform is not repetitive, and voltage balancing is not at the most priority. After the first test is finished with this waveform, the MMC will need to restart with all capacitor voltages charged to the average values for the next test. Additionally, the full-scale simulation results show the capacitor voltage ripple in detail. This complex waveform consists of a switching impulse that has a rise time of 250 µs which constitutes the peak magnitude of the waveform. The error in this peak magnitude is kept to be 0.1 %, which is well within limits given in the IEC standard [14]. Moreover, the performance of this waveform is verified with the reference

waveform in the frequency domain in Fig. 3.18(b).
Similar to the unipolar complex waveform, Fig. 3.19 shows the performance of unbalanced sinusoidal waveform in the time domain. For even mixed polarity waveform, the upper and lower arm voltage ripple has different values, as shown in Fig. 3.19(a). However, this does not affect the capacitor voltage balancing. The quality of the generated waveform is illustrated in the frequency domain in Fig. 3.19(b), and they match well for the DC component and 50 Hz component. With this waveform, mathematical ripple expression derived in Section 3.3.4 is compared analytically, with simulations, and with experiments. First, the ripple expression is plotted together with simulation and experimental results in Fig. 3.20.



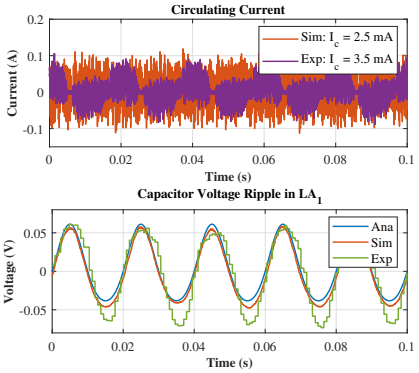
(a)



(b)

Figuur 3.19: Unbalanced sinusoidal waveform in (a) Time domain (b) Frequency domain.

Additionally, the circulating current obtained from simulation and experimental results is plotted together with the ripple expression. The simulation results match well with the analytical results for capacitor voltage ripple. Even the experimental results match well in the positive cycle of ripple. However, the experimental ripple is slightly higher on negative peaks compared to analytical and simulation results. It could be because of the low magnitude (110 mV) measured from a digital voltage oscillator designed to measure relatively high voltage (200 V). Furthermore, the average circulating current with a simulation model and experimental setup is relatively low, verifying the assumption of zero average circulating current. Please note that the circulating current is switching positive or negative depending upon the balance between the DC link and the total voltage of the inserted submodule capacitors. If the total voltage of the inserted submodule capacitors is higher than the DC link, the circulating current will be negative and vice versa. The average capacitor voltage ripple is compared for the harmonic test waveform and unbalanced sinusoidal waveform in Table 3.4. Since the unipolar complex waveform has a complex Fourier spectrum, it becomes computationally challenging to derive the analytical expression even numerically. For the two waveforms, the analytically calculated voltage ripple matches the simulation results. However, a slightly higher value is obtained experimentally due to measurement inaccuracies. With the load capacitance of 6.8 μF and submodule capacitance of 4 mF, the ripple is kept within 1 % of the average capacitor voltage, which satisfies the earlier condition decided in Section 3.3.4.
To analyse the quality of the obtained waveforms furthermore, the definition of THD is



Figuur 3.20: Comparison of capacitor voltage ripple analytically, using simulations, and experimentally.

Tabel 3.4: Verification of SM Capacitor Ripple Calculations for Various Waveforms

	Analytically calculated (mV)	Simulation results (mV)	Downscaled prototype (mV)
1. Harmonic test waveform	110.2	111.3	131.8
2. Unbalanced sin waveform	UA = 53.5 LA = 99.4	UA = 43.3 LA = 111.5	UA = 40 LA = 110.5
3. Sinusoidal	114.7	115.6	127.7
4. Triangular	114.3	116.4	127.9
5. Trapezoidal	114.7	119.6	141.4

adapted for non-sinusoidal voltage waveforms, as shown in (3.30), to quantify the harmonic performance of the MMC-based AWG. The obtained THD for the harmonic test waveform, unipolar complex waveform, and unbalanced sinusoidal waveform is 0.34 %, 3.30 %, and 3.66 % respectively. These THD values are well below 5 % which is within the industrial standard of the allowed distortion in the grid [88]. Apart from the quality of the obtained voltage wave shape and balancing of the submodule capacitor voltages, the losses in the added series resistance are less than 1 W for the shown wave shapes, which justify the usage of the passive damping technique. The overall performance of the AWG is summarised in Table 3.5.

$$THD_{nonsin} = \frac{\sqrt{\sum_{h=0}^{\infty}(V_{h,ref} - V_{h,out})^2}}{V_{1,out}} \tag{3.30}$$

Apart from the selected waveforms shown in Fig. 3.4, more periodic and complex waveforms are obtained from the scaled-down prototype and they are illustrated in Fig. 3.21 and Fig. 3.22. The performance of these waveforms are shown in time and frequency domain. Additionally, all the other performance parameters are summarized in Table 3.5. The derived capacitor voltage expression is compared with the simulation and experimental results in Table 3.4. As observed earlier, the experimentally obtained voltage

Tabel 3.5: Performance of Scaled-down MMC Setup for Waveforms Which Were Shown in Fig. 3.4

	Magnitude error (%)	THD (%)	Losses (W)
1. Harmonic test waveform (K_p=5)	1 % till 3rd harmonic up to 4 % in higher harmonic	0.34	0.89
2. Unipolar complex waveform (K_p=1)	0.1 % error in the peak of switching impulse	3.30	0.3
3. Unbalanced Sine waveform (K_p=3)	2.9 % error in the positive peak	3.66	0.3
4. Sinusoidal (K_p=3)	0.67	0.47	0.76
5. Triangular (K_p=2)	0.67	0.59	0.53
6. Trapezoidal (K_p=2)	2.22	0.38	1.07
7. Asymm. Triangular (K_p=2)	2.22	1.07	1.45
8. Complex waveform 1 (K_p=2)	1.36	0.72	0.19
9. Complex waveform 2 (K_p=2)	3.79	1.10	0.17

ripple is slightly higher, especially for trapezoidal based waveform due to measurement inaccuracies at low voltage. The negligible circulating current answers why the submodule capacitor voltages get balanced even when higher harmonics are generated

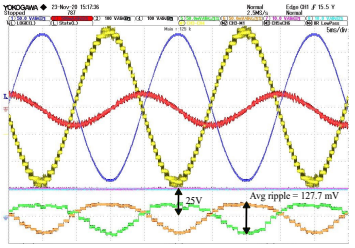
3.5. RESULTS OF FULL-SCALE PROTOTYPE

The performance of the full-scale HV MMC-based AWG is verified with MATLAB-Simulink simulations with 67 submodules per arm and the system parameters are summarized in Table 3.6. The system can generate 100 kV with 10 nF load capacitance. The values of L_a and R_a are designed as per the guideline discussed in Section 3.3.2. Additionally, the closed-loop system discussed in Section 3.3.5 is designed for the full-scale prototype with a proportional gain of 5 and a simple sorting algorithm with a sorting frequency of 5 kHz. From the transfer function derived in (3.29), small- and large-signal controller bandwidth is calculated as 31.2 kHz and 35.3 kHz respectively with 200 ns sampling period. These controller bandwidths show that they do not interfere with the designed open-loop bandwidth of the voltage waveform.

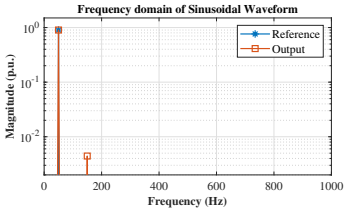
Tabel 3.6: System Parameters of Full-scale HV MMC Setup

No.	**Description**	**Symbol**	**Values**
1.	DC-link voltage	V_{DC}	200 kV
2.	Output voltage	V_a	100 kV
3.	Modulation index	m_a	0.9
4.	Number of submodules	N	67
5.	Large-signal bandwidth (Open loop)	$f_{1\%err}$	500 Hz
6.	Submodule capacitance	C_s	10 µF
7.	Arm inductance	L_a	3.2 mH
8.	Arm resistance	R_a	9.1 kΩ
9.	Load capacitance	C_{load}	10 nF

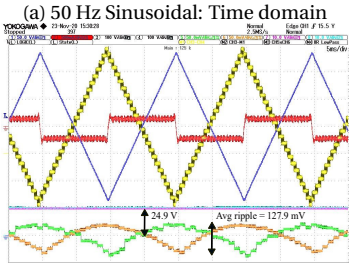
Similar to the down-scaled prototype, the performance of the full-scale AWG is showca-



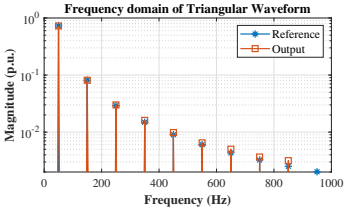
(a) 50 Hz Sinusoidal: Time domain



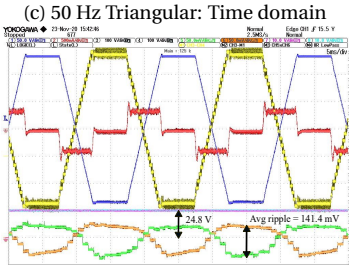
(b) 50 Hz Sinusoidal: Frequency domain



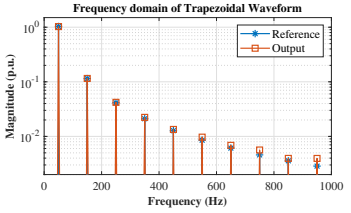
(c) 50 Hz Triangular: Time domain



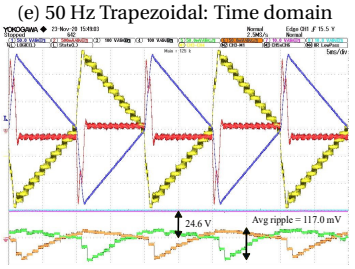
(d) 50 Hz Triangular: Frequency domain



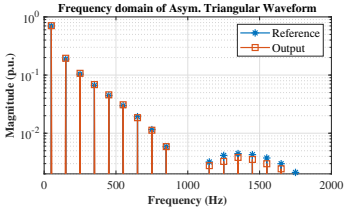
(e) 50 Hz Trapezoidal: Time domain



(f)50 Hz Trapezoidal: Frequency domain

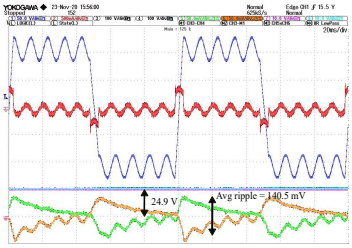


(g) 50 Hz Asymm. Triangular: Time domain

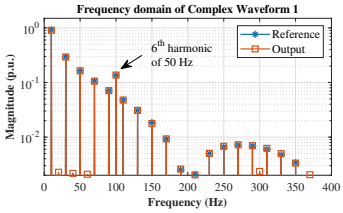


(h) 50 Hz Asymm. Triangular: Frequency domain

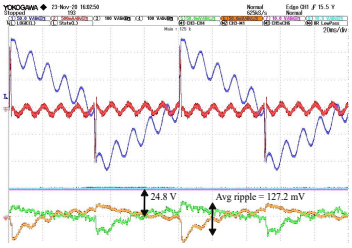
Figuur 3.21: Periodic waveforms generated from the small prototype of the MMC-based AWG [Blue: v_a=50 V/div, red: i_s=0.5 A/div, Yellow: v_s=50 V/div, Pink & sky blue: UA_{12} & LA_1=10 V/div, Orange & Green: UA_1 & LA_{12}=50 mV/div, Time Div=5 ms/div]



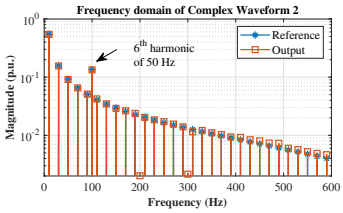
(a) 10 Hz Complex waveform 1: Time domain



(b) 10 Hz Complex waveform 1: Frequency domain



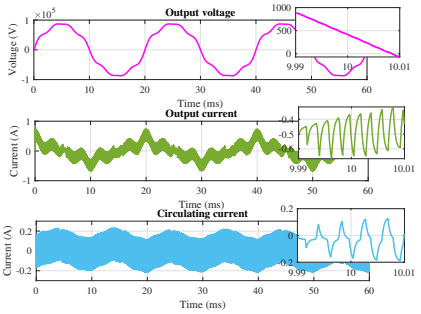
(c) 10 Hz Complex waveform 2: Time domain



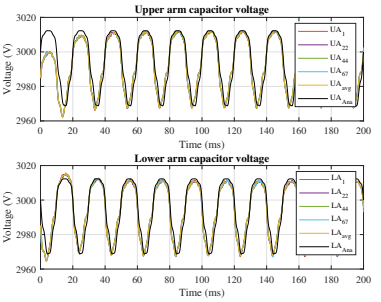
(d) 10 Hz Complex waveform 2: Frequency domain

Figuur 3.22: Complex waveforms generated from the small prototype of the MMC-based AWG [Blue: v_a=50 V/div, red: i_s=0.5 A/div, Yellow: v_s=50 V/div, Pink & sky blue: UA_{12} & LA_1=10 V/div, Orange & Green: UA_1 & LA_{12}=50 mV/div, Time Div=20 ms/div]

sed with three wave shapes in Fig. 3.23, Fig. 3.24, and Fig. 3.25. These figures show the performance of HV AWG in terms of output voltage, output current, and circulating current with their zoomed pictures. Here, the dynamics of switching circulating current is visible with the zoomed pictures for all three waveforms. This proves the assumption of negligible circulating current with the simulations of the full-scale prototype. Especially for the unipolar complex waveform in Fig. 3.24(a), the zoomed picture of a switching impulse is shown. With the proper design of the MMC system parameters, the switching impulse shows an expected rise time of 250 µs. Hence, the obtained THD of the waveform is less than 1 %. Similarly, the harmonic test waveform can generate much more accurate harmonics. All these results are summarized in Table 3.7, along with losses that occurred in the arm resistors. These losses are reasonable for the 10 kW full-scale system, where these losses constitute only 2 % of the total power delivered from the input side. Furthermore, these figures show the selected (1^{st}, 27^{th}, 44^{th}, 67^{th}) submodule capacitor voltages from upper and lower arms along with their average values. For harmonic test and unbalanced sinusoidal waveform, the analytically derived submodule capacitor voltage is plotted along with the simulation results. The derived analytical expression matches well with the simulation results of the full-scale prototype. Please note that the chosen submodule capacitance of 10 µF is sufficient for the load capacitance of 10 nF, keeping the ripple 1.5 % of the average capacitor voltage. For unipolar complex waveform, only one cycle is needed, and it is seen clearly that the upper and lower arm have a different ripple.

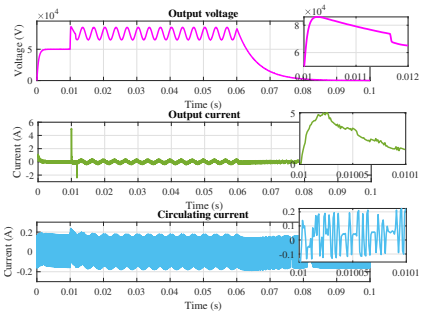


(a) Output performance

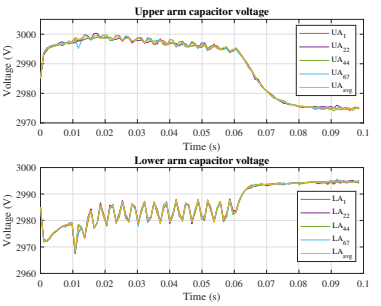


(b) Submodule capacitor voltage

Figuur 3.23: Performance of harmonic test waveform.

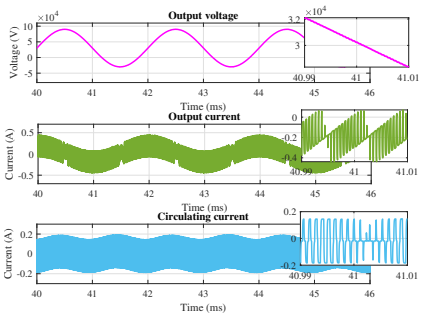


(a) Output performance

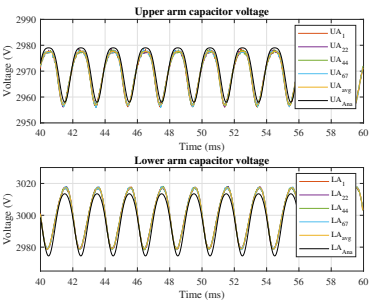


(b) Submodule capacitor voltage

Figuur 3.24: Performance of unipolar complex waveform.



(a) Output performance



(b) Submodule capacitor voltage

Figuur 3.25: Performance of 50 Hz unbalanced sinusoidal.

Tabel 3.7: Performance of Full-scale HV MMC Setup for Waveforms Which were Shown in Fig. 3.4

	Magnitude error (%)	THD (%)	Losses (W)
1. Harmonic test waveform (K_p=5)	Less than 1 % for all harmonics	0.01	223.52
2. Unipolar complex waveform (K_p=5)	Approx. 0 % error in the peak of switching impulse	0.2	163.53
3. Unbalanced Sine waveform (K_p=5)	Approx. 0 % error in the positive peak	0.15	238.65

3.6. CONCLUSIONS FOR PROMISING HV AWG SOLUTIONS AND DESIGN TRADE-OFFS

Considering the many advantages offered by the MMC converter topology, this chapter selects it for HV AWG application to generate complex arbitrary waveforms with good accuracy. Based on the design requirements presented in Chapter 2, the design trade-offs of the MMC-based HV AWG are analyzed for Box 1 requirement highlighted in Fig. 2.14. The analytical modelling of MMC is performed by simplifying the complex structure of the MMC into two partially coupled circuits, i.e., output current and circulating current circuit. The output current circuit determines the harmonic performance of the AWG. Its parameters, i.e., modulation technique, L_a, R_a, N, semiconductor devices, submodule capacitance, and control system are studied in detail to obtain the accurate voltage waveforms as per HV testing standards. The circulating current circuit balances the inserted submodule capacitor voltages and the submodule capacitance plays an important role here.

It is found that the PSC modulation technique provides additional advantages over NLC by shifting the carrier harmonics to N^{th} of the switching frequency without changing any baseband harmonics present due to non-sinusoidal wave shape. The arm inductance and series resistance filter the undesirable voltage harmonics and determine the available small- and large-signal bandwidth and slew rate. To obtain higher bandwidths and slew rate, lower values of arm inductance should be used. However, it demands a higher switching frequency to attenuate the carrier harmonics, and a higher switching frequency needs higher accuracy from the controller hardware. Hence, SiC MOSFETs seems to be the most suitable solution with the possibility of higher switching frequency. Apart from this, the analytical expression of submodule capacitor voltage ripple is derived from selecting the value of submodule capacitance using the averaging principle. This derivation is based on the fact that the HV AWG application does not need a large circulating current. This is the reason why submodule capacitor voltages are well balanced even when complex wave shapes are generated.

The discussed design trade-offs are demonstrated using MATLAB-Simulink simulations and a down-scaled prototype of a MMC with 12 submodules. Firstly, an important observation is that the obtained simulations with MATLAB-Simulink match well with the

experimental results. Secondly, the down-scaled prototype can already provide voltage waveforms with reasonable accuracy for the design value of voltage, current, bandwidth, and the control system. These waveforms include bipolar, unipolar, and mixed polar waveforms to show the performance of MMC-based AWG. The THD of most waveforms is less than or around 1 % except for unipolar complex waveform and unbalanced sinusoidal waveform where it is around 3 %. Thirdly, the theoretical assumption of negligible circulating current and the derived submodule capacitor voltage expression are proved with MATLAB-Simulink simulations and experimentally with the down-scaled prototype. Additionally, the sorting algorithm is implemented to improve the submodule capacitor voltage balancing by removing non-idealities in different submodules. On the same topic, the ripple in the submodule capacitor voltages suggests that the submodule capacitance requirement for HV AWG application is much smaller than that for the traditional energy transmission application of MMC. In the end, the performance of the full-scale HV AWG is verified in MATLAB-Simulink with 67 submodules, especially for the circulating current dynamics, submodule capacitance choice, and harmonic performance of the output voltage. In summary, this chapter provides a complete analysis of design guidelines for realizing an MMC-based HV AWG for performing dielectric testing on grid assets.

4

CONTROL ASPECTS OF HV AWG

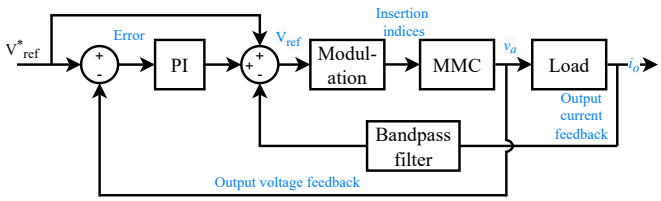
Chapter four of the thesis dives deeper into the control aspects of the HV AWG. First, the active damping control methodology is explored for the MMC-based HV AWG in order to eliminate losses in the arm resistor. Hence, detailed mathematical modeling is performed to design the PI controller and tune the active bandpass filter for implementing the active damping for the HV AWG application. The performance of the developed active damping control methodology and the PI controller have been demonstrated with a 50 Hz *sinusoidal waveform and arbitrary waveforms such as triangular, trapezoidal, and complex waveforms with MATLAB-Simulink simulations. The second part of the Chapter deals with the selection of the controller hardware for the HV AWG application based on the two main requirements of accurate gate pulse generation at the high-frequency waveform and the required robustness against the harsh EMC environment during the HV tests. The performance of the selected controller is demonstrated with a scaled-down prototype of MMC-based AWG, where sinusoidal and other arbitrary waveforms are generated up to* 5 kHz *with a THD less than 5 %.*

This chapter is based on following research articles:

- X. Zhou, D. A. Ganeshpure, T. B. Soeiro, M. G. Niasar, Y. Wu, and P. Vaessen, "Implementation of Active Damping Control Methodology on Modular Multilevel Converter(MMC)-Based Arbitrary Wave Shape Generator Used for High Voltage Testing", in 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023
- D. A. Ganeshpure, T. B. Soeiro, M. G. Niasar, and P. Vaessen, "The Control Stage of a Modular Multilevel Converter-based Arbitrary Wave shape Generator for Dielectric Testing of High Voltage Grid Assets", in 2023 11th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Jeju, Korea (South), 2023

4.1. ACTIVE DAMPING CONTROL METHODOLOGY

Although passive damping with the arm resistor simplifies the control architecture and provides satisfactory results in the Chapter 3, the losses in the arm resistor can become significant as the DC link voltage increases. Furthermore, the resistance of the arm limits the maximum magnitude of the circulating current flowing through the circuit, limiting the voltage balancing capability of the submodule capacitor of the MMC. Therefore, active damping control methodology can be advantageous for the MMC-based AWG and it is investigated further in this section. The active damping techniques have been extensively researched and developed based on the conventional three-phase, two-level, and three-level (NPC and T-type) topologies [89]-[90]. It can generally be categorized into filter-based [89]-[91] and loop-feedback-based methods [92]-[90]. The filter-based active damping is realized by cascading the designed filter, for instance, the notch filter in the current control loop. Loop-feedback-based active damping measures the capacitor voltage or current and feedback to the controller output. The filter-based active damping methodology is chosen to attenuate resonance without adding a large lossy arm resistor. The active damping control methodology has been implemented in MMC control to suppress unwanted high-frequency, as discussed in [93]-[94]. However, all the existing literature studies it for sinusoidal reference. Hence, it is important to examine the capabilities of the active damping methodology when non-sinusoidal waveforms need to be generated. Fig. 4.1 shows the proposed closed-loop control configuration for the MMC-based AWG. The voltage feedback ensures the minimal steady-state error. The band pass filter measures the output current waveform to identify the resonance frequency in the MMC circuit and it is critical to tune the filter appropriately to the resonant frequency. Considering the two control loops present in the proposed control configuration, it is important to study the stability of the proposed control system, as it will be shown in the upcoming sections.

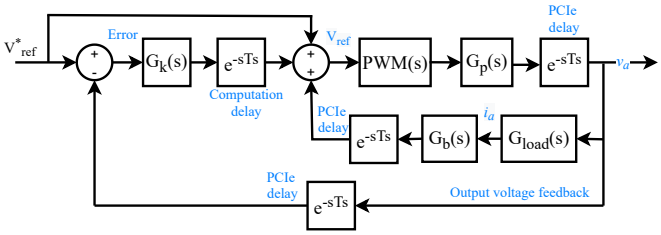


Figuur 4.1: Closed loop system of the MMC-based AWG.

4.1.1. CONTROL SYSTEM IN TIME DOMAIN

The detailed block diagram of the control system in the continuous-time domain is shown in Fig. 4.2. To study the stability of the closed-loop control, the transfer functions of each block are needed, such as the controller ($G_k(s)$), the plant ($G_p(s)$), the band pass filter ($G_b(s)$), and the load ($G_{load}(s)$) and they are derived in the following sections. Additionally, there are several system delays to consider in studying the stability of the control system. First, the computational delay represents the amount of time between the sampling instant and the duty cycle updating instant [95]. Second, the PCIe (Periphe-

ral Component Interconnect Express) delay in the forward and feedback paths is present due to the architecture of the real-time simulator, where T_s is the simulation step of the real-time simulator.



Figuur 4.2: Block diagram of the control system of the MMC-based AWG as a continuous equivalent.

4

PI CONTROLLER ($G_k(s)$)

The Proportional-Integral (PI) controller is one of the most widely used controllers in all converter topologies due to its simplicity and effective performance. It is chosen as a next step from the proportional controller from the last Chapter 2. An ideal representation of the PI controller is defined in (4.1). Here, K_p corresponds to the proportional gain, and K_i represents the integral gain. Additionally, the controller computation delay must be included since it impacts the stability of the closed-loop system. The combined transfer is shown in (4.2).

$$G_k(s) = K_p(1 + K_i\frac{1}{s}) \tag{4.1}$$

$$G_k^{'}(s) = K_p e^{-sT_s}(1 + K_i\frac{1}{s}) \tag{4.2}$$

PLANT ($G_p(s)$)

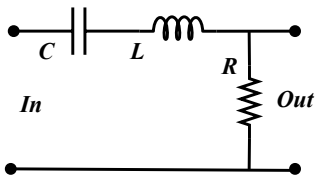
The output current circuit shown in Fig. 3.3(b) dictates the dynamics of the MMC. Hence, the plant transfer function is derived from it in the following equations, where $V_a(s)$ and $V_s(s)$ are variables representing the output voltage and the switching voltage in the Laplace domain. The transfer function representing the PWM process is shown in (4.6) [96].

$$V_s(s) = s\frac{L_a}{2}I(s) + \frac{R_a}{2}I_s(s) + \frac{1}{s}\frac{I_s(s)}{C_{load}} \tag{4.3}$$

$$V_a(s) = \frac{1}{s}\frac{I_s(s)}{C_{load}} \tag{4.4}$$

$$G_p(s) = \frac{V_a(s)}{V_s(s)} = \frac{2}{s^2 L_a C_{load} + sR_a C_{load} + 2} \tag{4.5}$$

An equivalent transfer function could be represented by a sampler with a gain of 1/Ts, followed by a zero order hold (ZOH) that compares the sampled input data with the carrier wave input data. m_a represents the ratio of the modulation amplitude to the carrier



Figuur 4.3: Series band pass filter.

amplitude. Furthermore, (4.7) shows the combined transfer function for the plant in the forward path.

$$G_{PWM}(s) = \frac{m_{PWM}G_{zoh}(s)}{T_s} = \frac{m_{PWM}(1-e^{-sT_s})}{sT_s} \tag{4.6}$$

$$G_p^{'}(s) = G_p(s)G_{PWM}(s)e^{-sTs} \tag{4.7}$$

BAND PASS FILTER ($Gb(s)$)

As mentioned in the introduction, a filter-based active damping controller is proposed to suppress the resonance present in the MMC-based AWG. To do so, it is important to identify the resonant frequency in the output characteristics of the MMC-based HV AWG, and the band pass filter is selected by choosing particular band frequencies around the resonance (ωc) [94]. The filter operates between frequencies $\omega 1$ and $\omega 2$, and its transfer function is derived based on a typical RLC band pass filter. The physical implementation of such a series band pass filter is shown in Fig. 4.3 [97], and its transfer function is derived from (4.8). Depending on the resonant frequency, the band pass filter can be altered by changing the values of $\omega 1$ and $\omega 2$.

$$\begin{aligned} G_b(s) &= \frac{R}{\frac{1}{sC}+sL+R} \\ &= \frac{s(\omega_2-\omega_1)}{s^2+s(\omega_2-\omega_1)+\omega_1\omega_2} \end{aligned} \tag{4.8}$$

$$\omega_{1,2} = \mp\frac{1}{2RC} + \sqrt{\frac{1}{2R^2C^2}+\frac{1}{LC}} \tag{4.9}$$

In this control system, the resonance is measured from the output current. Therefore, the output current is obtained from the output voltage considering the capacitive load. On the basis of this relationship, the transfer of the band-pass filter is altered, including the PCIe delay, as shown in (4.11).

$$G_{load}(s) = \frac{I_a(s)}{V_a(s)} = sC \tag{4.10}$$

$$G_b^{'}(s) = \frac{G_b(s)}{sC}G_{load}(s)e^{-sTs} \tag{4.11}$$

4.1.2. DISCRETIZATION OF THE CLOSED LOOP

As the real-time simulator works with a fixed time step, studying the stability of the control implemented in the continuous domain may not provide an exact answer to the question. It is necessary to discretize the transfer functions from (4.2), (4.7), and (4.11). The discretization of the PI controller in (4.2) is shown in (4.12) by placing $1/s = z/(z-1)$ for the integral gain and $e^{-sTs} = 1/z$.

$$G_k^{'}(z) = Z\{G_k^{'}(s)\} = \frac{k_p}{z}(1 + k_i \frac{z}{z-1}) \tag{4.12}$$

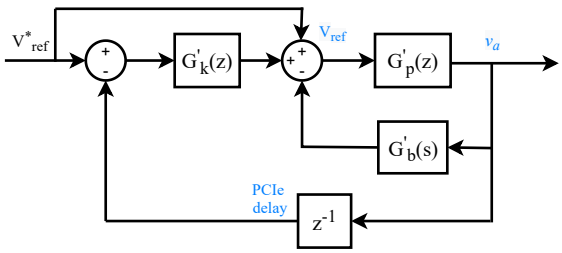
For plant discretization, the modulation index in the PWM transfer function is assumed to be 1 to simplify the process ($m_a = 1$). It should be noted that $G_{pwm}(s)$ need to be multiplied by T_s to compensate the $1/T_s$ in (4.6). Combining the plant transfer function and converting it into the z domain results in a discrete plant transfer function, as shown in (4.13). Similarly, the band-pass filter is converted from the Laplace domain to the Z domain. Therefore, the whole discretization system can be simplified and represented as shown in the block diagram in Fig. 4.4.

$$\begin{aligned}
G_p^{'}(z) &= Z\{G_p^{'}(s)\} \\
&= Z\{G_{pwm}(s)\, T_s G_p(s) e^{-sTs}\} \\
&= Z\{\frac{1-e^{-sT_s}}{sT_s}\, T_s G_p(s) e^{-sTs}\} \\
&= \frac{z(-(1+B)e^{-YT_s} - (1+C)e^{-XT_s} - B - C)}{(z-e^{-XT_s})(z-e^{-YT_s})} + \frac{(e^{-XT_s-YT_s} + Be^{-YT_s} + Ce^{-XT_s})}{(z-e^{-XT_s})(z-e^{-YT_s})} \\
B &= \frac{Y}{X-Y} \qquad C = \frac{X}{Y-X} \\
X &= \frac{R_a C_{load} + \sqrt{R_a^2 C_{load}^2 - 8L_a C_{load}}}{2L_a C_{load}} \qquad Y = \frac{R_a C_{load} - \sqrt{R_a^2 C_{load}^2 - 8L_a C_{load}}}{2L_a C_{load}}
\end{aligned} \tag{4.13}$$

$$\begin{aligned}
G_b{}'(z) &= Z\{G_b^{'}(s)\} \\
&= \frac{N^2(e^{2M-N} - e^{-N})}{M(ze^{2M-N}) - z^2e^M - e^{M-2N} + ze^{-N})} + \frac{N(e^{2M-N} - 2ze^M + e^{-N})}{(ze^{2M-N}) - z^2e^M - e^{M-2N} + ze^{-N})} \\
M &= \frac{\sqrt{\omega_1^2 - 6\omega_1\omega_2 + \omega_2^2}}{2} \quad N = \frac{\omega_2 - \omega_1}{2}
\end{aligned} \tag{4.14}$$

4.1.3. STABILITY ANALYSIS OF THE PROPOSED CONTROL SYSTEM

To ensure the safe operation of the hardware, it is essential to analyze the stability of the system. The stability criteria is studied with the gain margin and phase margin of



Figuur 4.4: Simplified discretization system.

an open-loop transfer function, and it is derived in (4.15). In addition, the closed-loop transfer function of the system is derived in (4.16).

$$G'_{pFB}(z) = \frac{G'_p(z)}{G'_p(z)G'_b(z)+1}$$
$$G_{ol}(z) = (1+G'_k(z))G'_{pFB}(z) \tag{4.15}$$

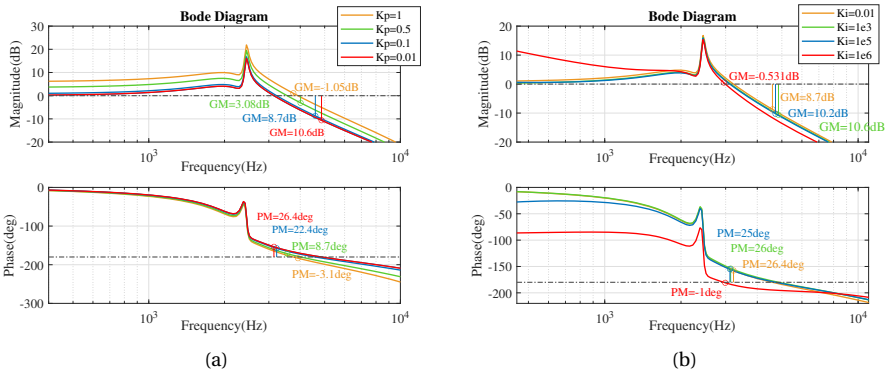
$$G_{cl}(z) = (1+G'_k(z))\frac{G'_{pFB}(z)}{G'_{pFB}(z)G'_k(z)z^{-1}+1} \tag{4.16}$$

Similar to Chapter 3 in Section 3.4, the load capacitance is chosen to be 6.8 µF. However, the arm inductor is further reduced to 1.32 mH from 3 mH to increase the resonant frequency. Thus, the expected resonant frequency is:

$$\omega_c = \frac{1}{\sqrt{\frac{L_a}{2}C_{load}}} = 14927\,\mathrm{rad\,s^{-1}} = 2375\,\mathrm{Hz} \tag{4.17}$$

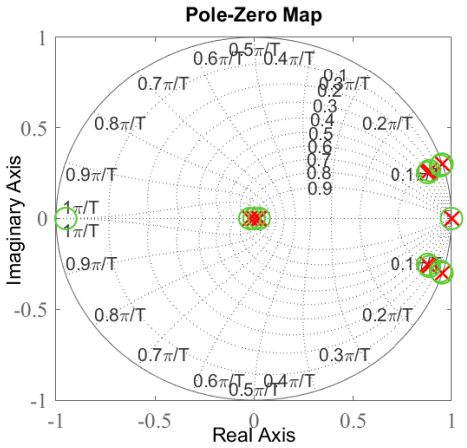
Hence, the band pass filter is designed based on (4.11), where $\omega 1 = 14327\,\mathrm{rad\,s^{-1}}$ and $\omega 2 = 15527\,\mathrm{rad\,s^{-1}}$ are chosen to ensure that the bandwidth is wide enough. For a PI controller, the transient response of the regulation system is mostly determined by the proportional term, while the integral term impacts the steady-state response. Therefore, the two can be analyzed separately. Bode plots based on open-loop system transfer functions are shown in Fig. 4.5.

Fig. 4.5 illustrates some common observations. On the one hand, when Kp increases, the magnitude of the PI controller increases. On the other hand, a lower Kp keeps the system stable, but might provide a poor transient response to the system. The influence of Ki values on the stability is significantly less compared to Kp. Hence, the bode plot of much higher values of Ki are plotted in Fig. 4.5(b). Additionally, sample time affects delays in the discrete-time domain. After analyzing the influence of Kp and Ki, the PI controller is built with Kp = 0.001 and Ki = 0.01, since it offers a safe gain margin of 10.9 dB and a phase margin of 27.8 deg. The pzmap of the closed-loop system is drawn in Fig. 4.6. According to the Jury stability criterion [98], the closed-loop system is stable.



(a) (b)

Figuur 4.5: Discrete domain (a) Variable Kp while Ki=0 (b) Variable Ki while Kp=0.01.



Figuur 4.6: Poles-zeros map with active damping.

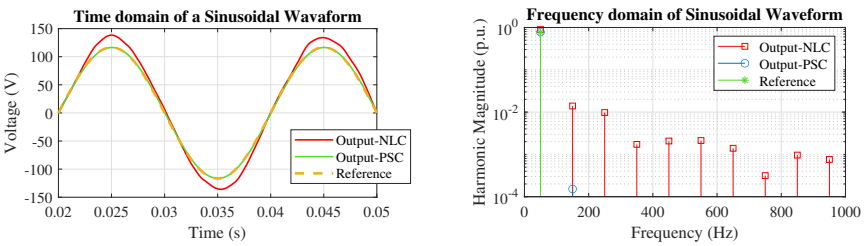
4.1.4. SIMULATION RESULTS OF THE PROPOSED CONTROL SYSTEM

The analysis of the proposed active damping control methodology is demonstrated using MATLAB-Simulink simulations of an MMC-based AWG with 12 submodules per arm. Similar to in Chapter 3, the DC-link voltage of 300 V is chosen, and the value of load capacitance is selected to be 6.8 μF to keep the current rating the same as the full-scale prototype. The arm resistance of 10 Ω is simulated considering stray resistance and considering a minimum value required for the active damping. Later, the arm inductance is chosen to be 1.32 mH, where the resonant frequency is calculated to be 2376.9 Hz. Hence, the switching frequency is chosen higher than the resonant frequency, and the selected value of switching frequency is 3770 Hz, which is a non-integer multiple of 50 Hz fundamental frequency of various waveforms [59]. Additionally, the bandpass filer required is designed considering the resonant frequency in the middle, and the system parameters for the simulation model are summarized in Table 4.1.4.

As discussed earlier, the performance of two chosen modulation methods, PSC and NLC, is first compared in Fig. 4.7. This figure shows that the PSC offers more accurate tracking of the reference voltage in the time domain and generates fewer base band harmonics in the frequency domain. It is observed that there is a significant difference in the quality of the waveforms obtained. Although PSC modulation can accurately track the reference voltage, NLC modulation results in distortion, leading to a gap between the output voltage and the reference. This inaccuracy with NLC is due to the switching frequency being lower than that of PSC. This makes it difficult for the controller to correct the error. Therefore, the PSC modulation is chosen to generate the rest of the arbitrary voltage waveforms.

Tabel 4.1: System Parameters of the MMC Setup

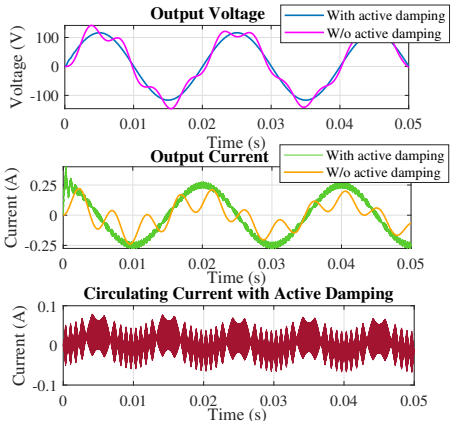
No.	Description	Symbol	Values
1.	DC-link voltage	V_{DC}	300 V
2.	Modulation index	m_a	0.8
3.	Number of submodules	N	12
4.	Switching frequency	F_s	3770 Hz
5.	Arm resistance	R_a	10 Ω
6.	Arm inductance	L_a	1.32 mH
7.	Load capacitance	C_{load}	6.8 µF
8.	Resonance frequency	ω	14927 rad/s
9.	Low cut-off frequency	$\omega 1$	14327 rad/s
10.	High cut-off frequency	$\omega 2$	15527 rad/s



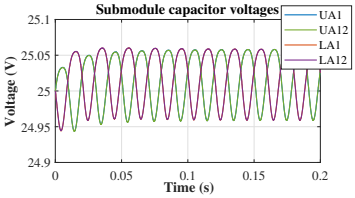
Figuur 4.7: Comparison between NLC and PSC with active damping control (a): Time domain (b) Frequency domain.

Fig. 4.8 and Fig. 4.9 illustrate the output results with active damping in both the time and frequency domains. As can be seen from Fig. 4.8(a), the output voltage is sinusoidal when active damping is applied, whereas, without active damping, the output voltage has distortion, demonstrating that the proposed active damping method is effective. One of the most important performance parameters of an MMC is the submodule capacitor voltages, shown in Fig. 4.8(b), which are well balanced. Additionally, the frequency domain analysis is conducted on the output voltage waveforms and reference waveforms, which shows that the generated output voltage waveforms match well with the reference waveform in Fig. 4.8(c). Moreover, Fig. 4.9 illustrates the performance

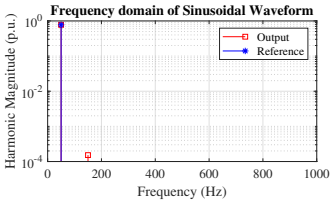
of the active damping control methodology when applied to more arbitrary waveforms, even when the complex waveform is generated with a combination of 10 Hz trapezoidal waveform and 100 Hz sinusoidal waveform. Furthermore, the quality of the obtained waveforms is analyzed with the Total Harmonic Distortion (THD), and its definition is adapted for the non-sinusoidal voltage waveforms, as shown in (3.30) [99]. The obtained THD of the waveforms is less than 1 % summarized in Table 4.2.



(a) Output Characteristics in time domain.



(b) Submodule capacitor voltages.



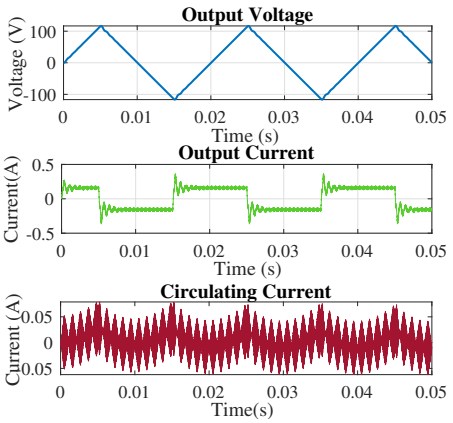
(c) Output Characteristics in frequency domain.

Figuur 4.8: Performance of active damping control methodology for 50 Hz sinusoidal waveform.

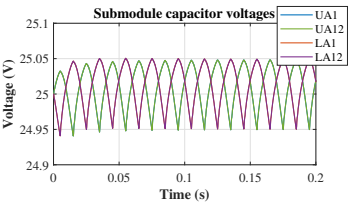
Tabel 4.2: THD of MMC-Based AWG with PSC for Periodic Waveforms

No.	Waveforms	THD(%)	Losses (W)
1.	Sinusoidal	0.02	0.09
2.	triangular	0.194	0.22
3.	Asymmetric triangular	0.645	0.07
4.	Complex	0.500	0.06

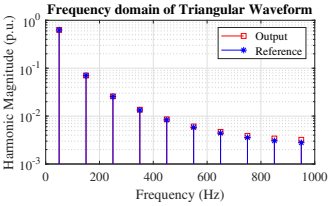
Apart from the THD and the SM capacitor voltages, it is important to check the losses in the relatively tiny arm resistor of 10 Ωand compare it to the passive damping. These results show that the proposed active damping methodology for MMC-based AWG works well to suppress the oscillations in the converter and generate accurate voltage waveforms. Moreover, the losses have been reduced significantly by the factor of 6, similar to the reduction in the arm resistor. Please note that the losses occurring in the scaled-down prototype are not significant. However, they will increase significantly for the full-scale prototype. This is achieved with the double control loop proposed in the above sections, which can add significant challenges for the control hardware implementation, restricting the obtained bandwidth of the waveform HV AWG. Hence, this method is not implemented in the further Chapters of the thesis.



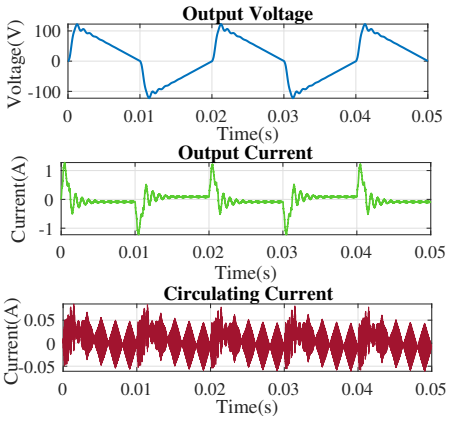
(a) Output Characteristics in time domain.



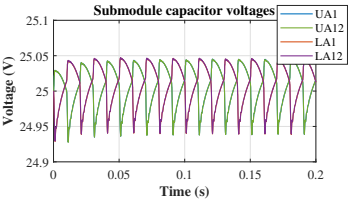
(b) Submodule capacitor voltages.



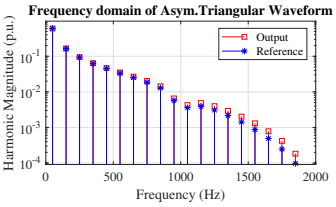
(c) Output Characteristics in frequency domain.



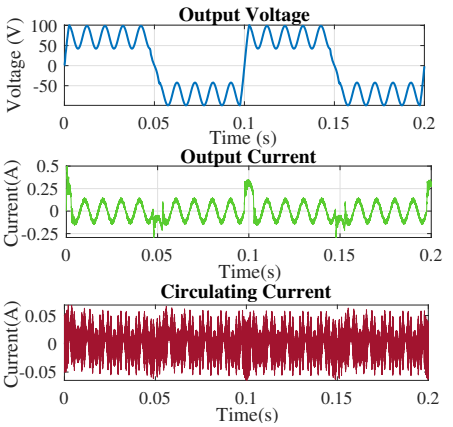
(e) 50 Hz Asym. triangular in time domain.



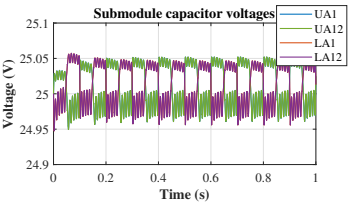
(f) Submodule capacitor voltages.



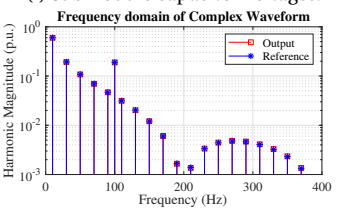
(g) Output Characteristics in frequency domain.



(h) Complex waveform with 10 Hz sine component in time domain.



(i) Submodule capacitor voltages.



(j) Output Characteristics in frequency domain.

Figuur 4.9: Performance of active damping control methodology with different arbitrary waveforms.

4.2. CONTROL HARDWARE

Though the modular structure of the MMC offers scalability with respect to its hardware submodule, the controller hardware can create challenges for the scalability of the MMC with a large number of submodules. For the HVDC transmission application, the number of submodules per arm is in the range of 300 to 400, which makes a total of 1800 to 2400 submodules for 3-phase operation [100][101][102]. Such a structure requires a smaller sampling period, higher computing power, and bigger communication burden for the centralized controller implementation [103]. The MMC-based AWG with a submodule voltage rating above 3 kV will have 67 submodules or less, as shown in Table 3.2. It is important to note that the MMC-based AWG is a single phase implementation. Hence, the total number of submodules are 134 or less, which is roughly 5 % of the total submodules required for a HVDC application. Hence, it is possible to have the centralized controller implemented in the FPGA in a single master control strategy [104]. The second reason for choosing the centralized controller is robustness. If the test object experiences a flashover and partial discharges, it can affect the distributed controller present on each submodule [105]. Considering the centralized controller and PSC modulation technique, the MMC-based AWG will need several FPGAs to implement the control. Programming different complex wave shapes in FPGA using VHDL or Verilog can be tedious for the test engineer. Therefore, to simplify the system operation, Real-Time Simulators (RTSs) are chosen to implement the controller of the HV AWG, where the programming for different waveforms can be done using a MATLAB-Simulink interface or similar software.

4.2.1. REAL TIME SIMULATOR AS A CONTROLLER

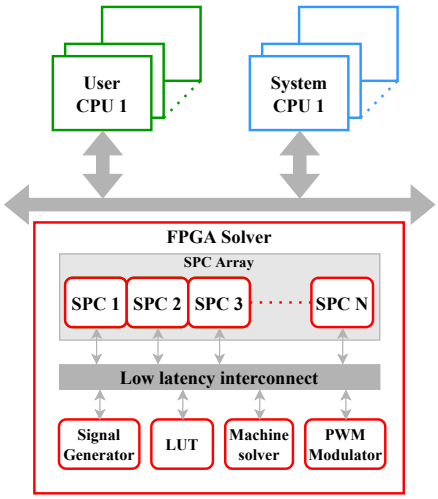
RTSs are becoming popular in power electronics since they can implement switches and other topologies accurately in the FPGA. Additionally, RTSs are used as a controller to test the power electronics hardware. They can be a suitable solution for MMC since they have many IO ports for controlling many submodules and the availability of an FPGA. Commercially, RTSs are developed by Typhoon HIL, OPAL-RT, dSpace, RT Box and RTDS Simulators. Generally, all these RTSs have a CPU core to process the software interface and multiple CPU and FPGA cores to implement the desired model of a controller, a converter system, or an entire power system. Additionally, FPGA cards are installed at all IO ports to achieve fast communication with external hardware or another RTS. OPAL-RT and dSpace use the MATLAB-Simulink interface, and RTDS uses the RSCAD interface to program the model. However, Typhoon HIL has developed a Python-based software interface to program the CPU and FPGA cores. All the available RTSs have advantages for the particular application.

The modulation technique presented in Fig. 3.8 will be implemented in the RTS, and the generated gate pulses will be communicated to the actual hardware via the fibre optic cables. Additionally, the RTS receives the data from the MMC hardware, such as submodule capacitor voltages, arm currents, and hardware health information through a fault signal, for implementing closed-loop control and protecting the MMC hardware. The critical element of the controller implementation is the accuracy of the reference waveform, carrier waveforms, and the generated gate pulses, especially when the refe-

rence waveform has a high frequency, such as 5 kHz. The controller needs to operate at a very small simulation step to generate such a high fundamental frequency. Since the Typhoon HIL devices can go to the simulation step of 200 ns [106], this chapter explores it as a controller for the MMC-based AWG. It includes the theoretical understanding of the RTS architecture, the implementation of the discussed modulation technique, and the effect of the simulation step.

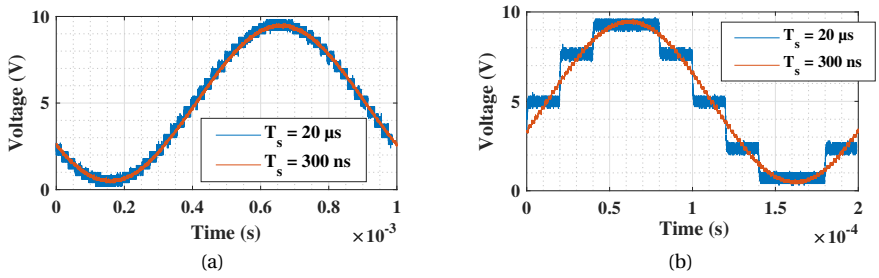
4.2.2. TYPHOON-HIL AS A CONTROLLER

The Typhoon HIL architecture is shown in Fig. 4.10, which consists of User CPUs, System CPUs, and FPGA with multiple Standard Processing Cores (SPCs) to process different aspects of the electrical circuits. The System CPUs deal with the low dynamics phenomena such as Voltage RMS calculation or handle the system communication protocol. The User CPUs are under direct user control, and the minimum possible simulation step is 200 ns [106]. Depending upon the complexity of the model, the simulation step needs to be altered so that the implemented model does not have an overrun error. Overrun means the simulation step is insufficient for the RTS to perform all the computations involved within that step [107]. Hence, overruns must be avoided at all costs for the proper operation of the implemented model.



Figuur 4.10: Typhoon HIL architecture.

The internal PWM modulator block in the FPGA solver can generate accurate gate pulses. This block can configure the carrier waveforms generation in the FPGA for the required switching frequency, the phase shifts, and the dead time. After the generation of these carrier waveforms in the FPGA, they are compared with the reference waveform from the User CPU to generate the gate pulses in the FPGA. The Typhoon HIL devices can generate accurate carrier waveforms with frequencies as high as 500 kHz [108]. It is important to verify if the User CPU can generate accurate reference waveform up to 5 kHz frequency. Hence, the reference waveforms from the HIL-404 device are plotted on an oscilloscope



Figuur 4.11: Performance of RTS for generating high-frequency reference waveform (a) 1 kHz (b) 5 kHz.

using an analog output port for two different simulation steps. These waveforms are plotted for two frequencies in Fig. 4.11. From these figures, it is clear that the 20 µs simulation step is not enough to generate a high-frequency reference waveform, and a lower simulation step is required, which is offered by the HIL-404 device.

Moreover, these SPCs in the FPGA solver have dedicated resources for converter modeling, non-ideal switch implementation, etc., as shown in Fig. 4.10. Different configurations of these SPCs give an optimized performance for a particular application. For example, configuration 3 of the HIL-404 device allows 32 non-ideal switches, which can be implemented in the FPGA, and this number is double when compared to the other SPCs configurations [109].

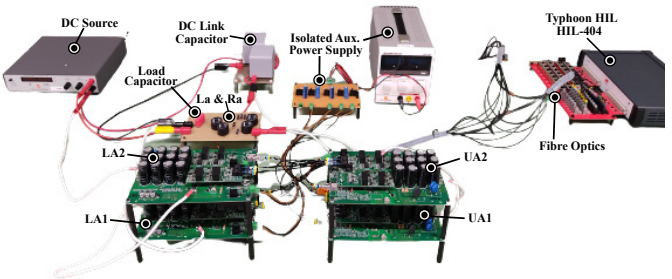
4.2.3. EXPERIMENTAL SETUP AND RESULTS

The performance of the HIL-404 device as a controller for the MMC-based AWG is demonstrated with a scaled-down prototype. As discussed in Chapter 2 in Fig. 2.14, the MMC-based HV AWG is aimed to be designed for the output voltage of 100 kV with a capacitive load up to 10 nF [99]. However, to test the controller performance, the output voltage is scaled down to 150 V, and it is tested with a higher capacitive load of 100 nF. The arm inductance and arm resistance is designed to obtain the large signal bandwidth of 27.4 kHz and the small signal bandwidth of 49.3 kHz considering the goal of generating 5 kHz waveform. The scaled-down prototype is shown in Fig. 4.12 with two submodules, and these system parameters of the scaled-down MMC hardware setup are summarized in Table 4.3.

The performance of the scaled-down prototype is demonstrated with sinusoidal waveforms with different frequencies, such as 1 kHz, 3 kHz, and 5 kHz in Fig. 4.13. These figures show the output characteristics, such as the voltage and current of the MMC-based AWG. Additionally, it is important to verify that the submodule capacitor voltages are well-balanced. Hence, they are displayed for a long duration of 1 s. The submodule capacitor voltages are balanced to a particular average value for all three waveforms and are not deviating away. However, the average value of submodule capacitor voltages is different for higher switching frequency waveforms. Please note that the implemented control system for the MMC-based AWG is an open loop. Generally, the open loop control is sufficient for the MMC-based AWG at lower frequency waveforms, as shown in Fig. 4.13(a), with a proper choice of switching frequency. Chapter 3 in Section 3.3.4 explains

Tabel 4.3: System Parameters of Down-Scaled MMC Setup

No.	Description	Label	Value
1.	DC link Voltage	V_{dc}	300 V
2.	Output Voltage	V_a	150 V
3.	Number of Submodules	N	2
3.	Modulation Index	m_a	0.9
4.	Submodule Capacitance	C_s	75 µF
5.	Load Capacitor	C_{load}	100 nF
6.	Arm Inductor	L_a	247 µH
7.	Arm Resistor	R_a	90 Ω
8.	Large Signal Bandwidth	$f_{1\%err}$	27.4 kHz
9.	Small Signal Bandwidth	f_{3dB}	49.3 kHz

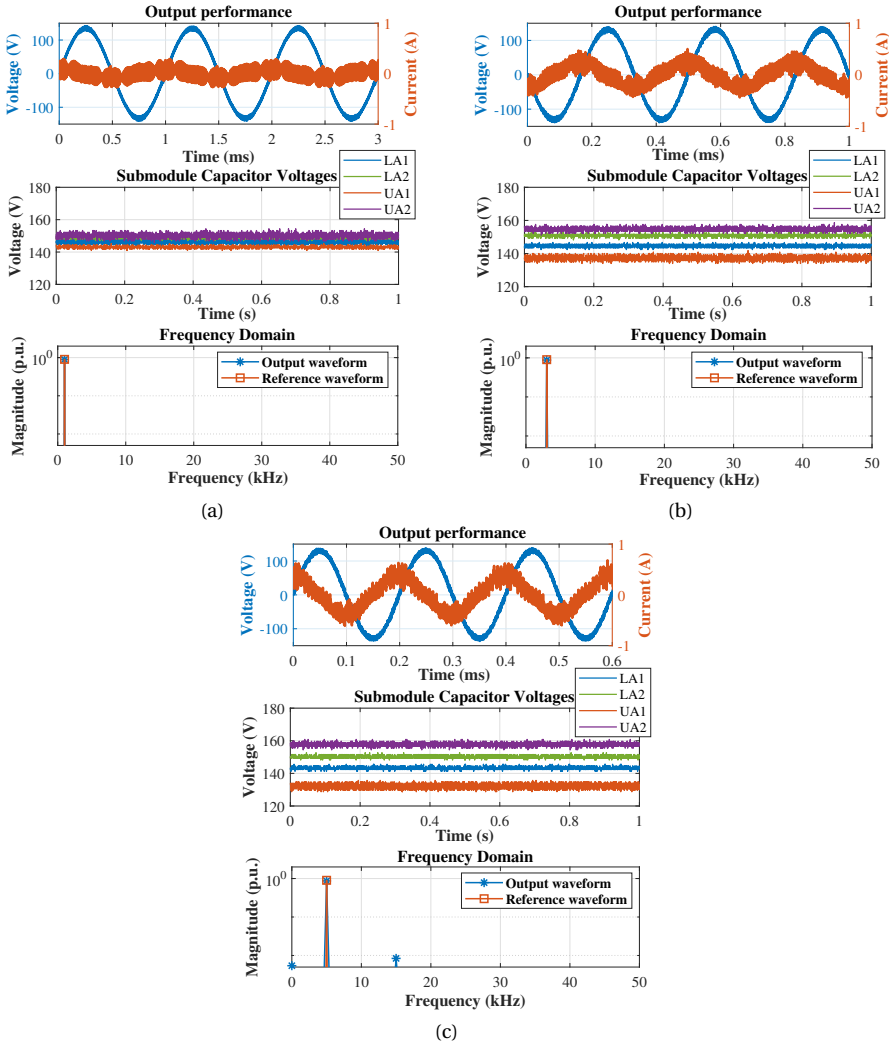


Figuur 4.12: Scaled-down hardware prototype of the MMC-based AWG with Typhoon HIL as a controller.

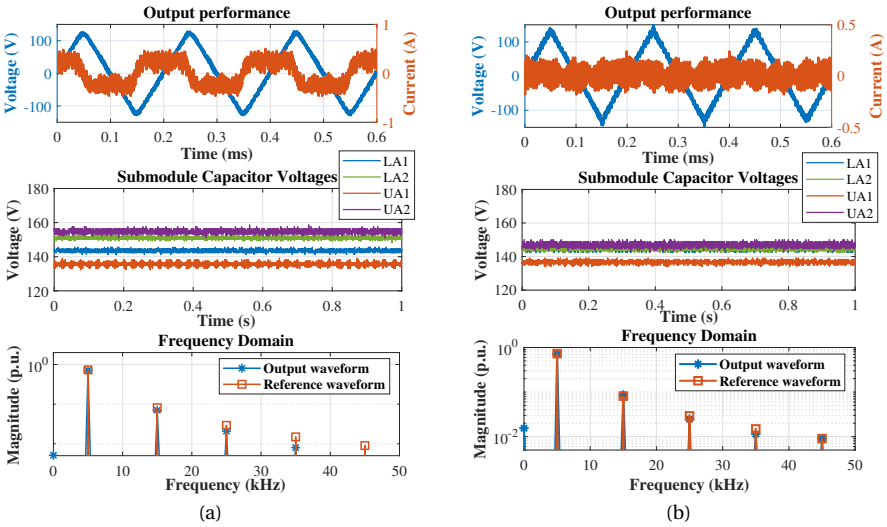
that the the switching frequency should be a non-integer multiple of fundamental frequency. However, when the fundamental frequency is higher than 1 kHz, an additional criteria needs to be considered which is that the sideband frequency $2NF_s$ should be an integer multiple of the fundamental frequency to balance the submodule capacitor voltages [59]. Moreover, the quality of the obtained waveforms is shown in the Frequency domain, and the THD values are summarized in Table 4.4, along with the selected value of switching frequencies. It is essential to highlight that the THD of all three sinusoidal waveforms is roughly around 1 %.
Additionally, the performance of the MMC-based AWG is shown with other arbitrary

Tabel 4.4: Performance of the MMC-based AWG for High Frequency Generation

Waveform	Switching Frequency	THD
Sin with 1 kHz	100.750 kHz	0.4 %
Sin with 3 kHz	144.750 kHz	0.9 %
Sin with 5 kHz	144.750 kHz	1.2 %
Tri with 5 kHz (Filter 1)	144.750 kHz	4.11 %
Tri with 5 kHz (Filter 2)	178.750 kHz	3.62 %
Square with 50 kHz	100.750 kHz	2.01 %



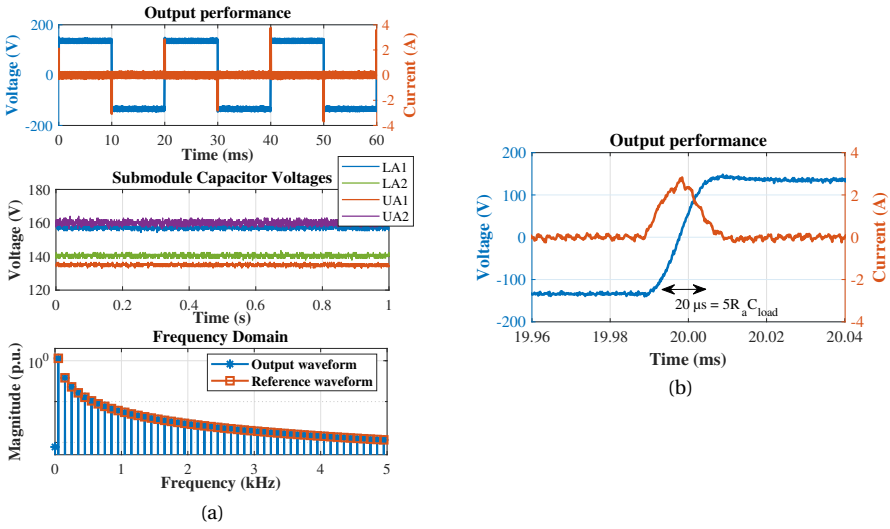
Figuur 4.13: Performance of RTS for generating high-frequency reference waveform (a) 1 kHz (b) 3 kHz (c) 5 kHz.



Figuur 4.14: Triangular waveform with 5 kHz Frequency (a) Filter 1 and switching frequency of 144.750 kHz (b) Filter 2 and switching frequency of 178.750 kHz

wave shapes, such as triangular and square waveforms. First, the triangular waveform is generated at a high frequency of 5 kHz, as shown in Fig. 4.14(a). Apart from the output characteristics and submodule capacitor voltages, frequency domain analysis is performed to verify the quality of the waveforms. It is visible that the output waveform is not following the reference waveform well after 5^{th} harmonics (25 kHz) since the designed filter has a large signal bandwidth around the same frequency. Hence, another filter is designed by reducing the load capacitance to more realistic values to 6 nF and increasing the arm resistance to 256 Ω, while the value of arm inductance is kept the same. This filter has large signal bandwidth of 200 kHz and small signal bandwidth of 631 kHz. The effect of the new filter is shown in Fig. 4.14(b). Here, the frequency domain harmonics are improved. However, the output voltage waveform has more switching harmonics since the suppressing frequency is farther away with the new filter. This problem can be solved by having higher number of submodules and by having a closed-loop control. Additionally, the submodule capacitor voltages are well balanced since the large-signal bandwidth is far from the fundamental harmonics. The quality of these arbitrary wave shapes is calculated by adapting the definition of THD as follows in (3.30). The values of THD for two high-frequency waveforms are 4.1 % and 3.6 % with Filter 1 and Filter 2. Due to a larger bandwidth, Filter 2 improves the THD better.

Apart from the triangular waveform, a square waveform is generated from the MMC-based AWG since this is a typical voltage stress experienced by the HV equipment in the inverter-dominated electrical network. The main focus of the test is to check the slope. Hence, a nominal frequency of 50 Hz is chosen with Filter 1 and switching frequency of 100.750 kHz. Its performance is shown in Fig. 4.15. The submodule capacitor voltages are balanced with a slightly different average value. It could be because of the DC part present in the square waveform. Additionally, the frequency domain waveform resem-



Figuur 4.15: (a) Square Waveform with 50 Hz frequency. (b) Zoomed version of Square Waveform with 50 Hz frequency.

bles the output waveform and the reference waveform, and the obtained THD value is 2.01 %. Moreover, the zoomed version of the slope of the square waveform is shown in Fig. 4.15(b). Based on the output current circuit shown in Fig. 3.3, the slope can be theoretically calculated as five times the $R_a C_{load}$ time constant. The slope of 20 µs is obtained, which can be further improved with a more realistic load capacitances and a smaller value of arm inductor.

In summary, the MMC-based AWG can generate arbitrary wave shapes up to 5 kHz with THD less than 5 %, matching the industrial standard for voltage quality [88]. Apart from the controller accuracy, other factors such as the filter design (R_a, L_a, C_{load}), choice of switching frequency, and the number of submodules play a crucial role in obtaining a good quality of voltage waveform. A closed-loop control can improve the accuracy of the generated waveforms.

4.3. CONCLUSIONS FOR CONTROL ASPECTS OF THE HV AWG

Among many possible control methodologies available for the MMC topology, active damping control methodology is investigated in the first half of the chapter to eliminate the losses occurring in the arm resistor. Even though active damping methodologies have been implemented for converter topologies, it is verified that the bandpass filter-based active damping methodology can be implemented when non-sinusoidal complex waveforms are generated from the MMC. Since there are two closed loops present in the proposed system, studying the stability criteria is necessary, and it is done using the bode plot and the pole-zero plot. With the designed gains for the PI controller, the performance of the implemented closed-loop control system is verified with MATLAB-Simulink simulations with scaled-down parameters of the HV AWG, and it is important

to highlight that the THD of the obtained waveform is within 1 %. Moreover, it is observed that the losses have been significantly reduced by implementing the active damping methodology. However, considering the involved computation cost and accuracy of measurement, passive damping methodology is implemented in further work of HV AWG.

Since the RTS can have many FPGAs in parallel and offer a simpler way to configure the FPGA without knowing the VHDL language, one of the commercially available RTS is selected considering the minimum possible simulation step offered in the second half of the chapter. Since the HV AWG application have reference waveform at high-frequency in the kHz range, it is crucial to have the simulation step in hundreds of nanoseconds. The selected commercial device is Typhoon-HIL 404, and it can withstand the harsh EMC environment in the HV testing facility. The performance of the Typhoon HIL is demonstrated with the scaled-down prototype, where large-signal bandwidth of 5 kHz is achieved with THD within 5 %. Here, the importance of filter design and choice of frequency is showcased, and how it is critical when the frequency of the reference waveform increases in the kHz range. These experimental results prove that the MMC-based AWG can go up to 5 kHz to generate accurate waveforms, fulfilling the Box 1 requirement of the HV AWG.

5

STEEP PULSE GENERATION

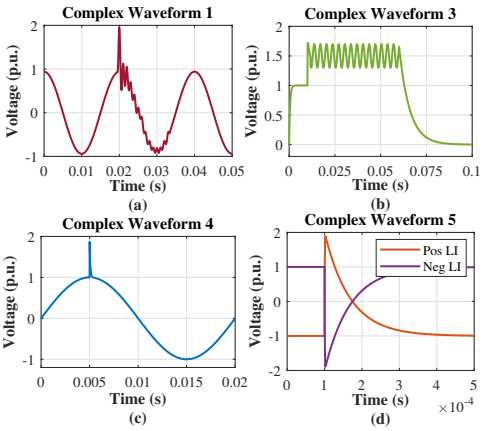
As described in Chapter 2, the HV test requirement includes steep pulse generation like the Lightning Impulse (LI) waveform, and it is defined by Box 2 in Fig. 2.14. This chapter aims to understand the challenges present with the MMC topology to generate fast-rising waveforms, where one of the significant challenges is the current capability of the switches. To obtain a steep pulse across the capacitive test object, fast rising current waveform must flow in the MMC. Hence, the pulse current capability of various discrete switch technologies is compared experimentally to check if it can reach the requirement posed in Chapter 2. Since it turns out to be a very complex design using a MMC to generate steep pulses, Marx generator circuits are chosen to create waveforms that have a rise time faster than $100\,\mu s$. *Additionally, for complex waveforms, an integrated hybrid circuit of MMC and Marx generator is designed. This chapter studies the coupled circuit in detail to find out that the MMC circuit influences the impulse generation and it interferes with the impulse formation if the time constants formed by the MMC output circuit are close to one of the time constants of the impulse waveform. However, with the MMC parameters carefully designed, it is possible to generate complex waveforms from the integrated hybrid circuit, and its performance is demonstrated with the scaled-down prototype and HV Simulations.*

This chapter is based on following research articles:

- D. A. Ganeshpure, A. P. Soundararajan, T. B. Soeiro, M. G. Niasar, P. Vaessen and P. Bauer, "Comparison of Pulse Current Capability of Different Switches for Modular Multilevel Converter-based Arbitrary Wave shape Generator used for Dielectric Testing of High Voltage Grid Assets,"2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. 1-11
- D. A. Ganeshpure, T. B. Soeiro, M. G. Niasar, N. Kulkarni, Pavol Bauer, and P. Vaessen, "Design of Integrated Hybrid Configuration of Modular Multilevel Converter and Marx Generator to Generate Complex Waveforms for Dielectric Testing of MV and HV Grid Assets", Revision is submitted, IEEE Open Journal of the Industrial Electronics Society - July 2023

5.1. INTRODUCTION

This chapter performs a feasibility study if it is possible to generate steep pulses such as LI waveforms from the MMC-based HV AWG. Chapter 2 has introduced many complex arbitrary wave shapes, and Fig. 5.1 shows specific waveforms, which include SI and LI waveforms. As described earlier, Fig. 5.1(c) and Fig. 5.1(d) can be generated using the superimposed circuit described in Fig. 2.10. However, Fig. 5.1(a) and Fig. 5.1(b) can not be generated by conventional HV test sources or test circuits. Hence, this chapter dives deeper into the feasibility study of the steep pulse generation and finds an integrated hybrid circuit to expand the capability of the MMC-based HV AWG.



Figuur 5.1: Typical complex voltage waveforms required for the dielectric tests of grid assets [110][111][99][112].

5.2. CHALLENGES GENERATING STEEP PULSES FROM MMC

There are several challenges for generating LI from an MMC, and they can be summarized as follows:

- A pulse current with large magnitude and fast rise
- Compensation of jitter in several series-connected switches
- Large stray inductance in the circuit

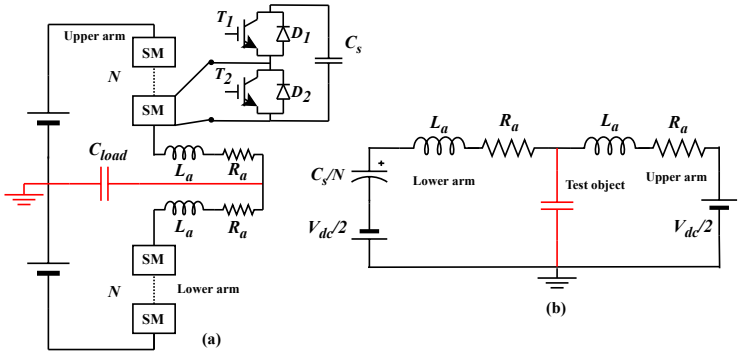
As discussed in Chapter 2, the typical value of dielectric capacitance found in MV and HV grid equipment ranges from 50 pF to 10 nF [16]. Considering the worst-case scenario that the LI waveform with 250 kV is applied across a capacitive load of 10 nF, it creates a pulse with large magnitude. From the schematic of MMC-based HV AWG in Fig. 5.2(a), it is possible to derive the equivalent circuit to calculate the exact current required to generate LI in Fig. 5.2(b). Based on this equivalent circuit, the submodule current required to generate LI waveform for the worst case scenario is shown in Fig. 5.3. The rise of 0.2 μs is calculated as the difference of time instants when the current magnitude is 10 % and

Tabel 5.1: Application Requirement on Pulse Current

Pulse Current (A)	Rise time (μs)	Slew rate (A/μs)
1685	0.2	8425

90 % of the peak current. Table 5.1 summarizes the pulse current required for generating LI. Suppose the high current-rated IGBT modules are chosen to be incorporated into the MMC considering the generation of short impulses. In that case, the MMC-based HV test source will be bulky and costly. Moreover, other low-frequency waveform tests do not need a high current. Therefore, this chapter investigates the pulse current capability of commercially available TO-packaged discrete switches instead of modules, which could be suited for the LI tests of grid assets.

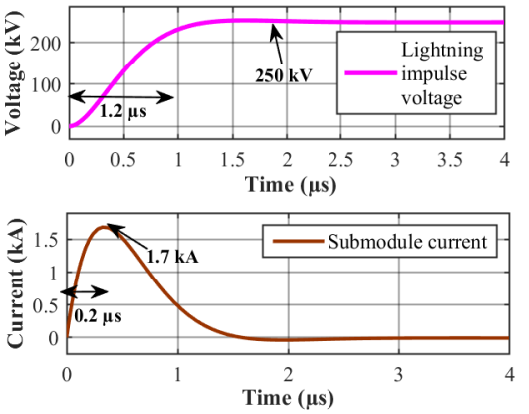
Apart from the pulse current capability, the MMC structure has several SMs in series, which creates two more problems, as summarized above. To generate the steep pulse in the range of few of μs across the capacitive load, all switches have to be fired together, and it needs a dedicated control and communication architecture, as discussed in [113]. Direct fiber optic to trigger all multi-stages of MMC is proposed to limit the jitter with distributed control on each stage. The next problem is the stray inductance present in the series-connected large SMs, and it can limit the rise time generated across the capacitive load. In this chapter, the pulse current capability of the TO-packaged switches is studied experimentally to check if they are suitable for the steep pulse generation from MMC.



Figuur 5.2: (a) Schematic of the MMC-based HV AWG (b) Equivalent circuit of MMC for LI operation.

5.3. PULSE CURRENT CAPABILITY

All switch manufacturers mention pulse current capability with other electrical properties in their datasheets. However, the single pulse current amplitude mentioned in these data sheets is rather limited to 2 to 3 times the rated continuous current at 25 °C junction temperature. Additionally, the short circuit test results on different semiconductor devices indicate that these devices can withstand much higher pulse current for short



Figuur 5.3: LI voltage waveform and the required current provided by the MMC.

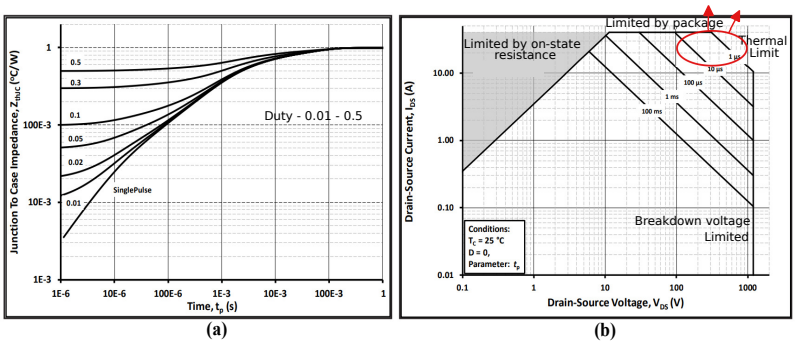
5

duration [114] [115] [116] [117]. However, these studies have analysed only the pulse current capability of a single switch technology, and benchmarking among other technologies is missing. In [117], pulse current capability of Silicon Carbide (SiC) MOSFET is compared with Field Stop (FS) IGBT. This section presents a comparison of 8 switches with different switch technologies and manufacturers to obtain the highest peak current with a fast rise time. The categories of different comparison is as follows:

- Comparison among Non-Punch Through (NPT) IGBT technology, Si Cool MOSFET technology, and SiC MOSFET technology
- Comparison between 2nd and 3rd generation SiC MOSFET technology
- Comparison between FS IGBT technology and 3rd SiC MOSFET technology
- Investigation of the NPT IGBTs with a different blocking voltage rating

5.3.1. THEORETICAL BACKGROUND AND ADOPTED METHODOLOGY

The current capability of a particular switch is limited by various factors such as its on-state resistance, thermal stability limit, and package limit [118]. Fig. 5.4(b) shows these factors for a CREE-Wolfspeed device named C2M0160120D. Fig. 5.4(a) shows the thermal impedance of the same switch for a single pulse with variable duty (0.01 to 0.5). As it is visible, the thermal impedance drops significantly as the pulse length is shortened, and thus this property enables the switch to safely conduct pulse currents of magnitudes much greater than its own rated current. As highlighted in Fig. 5.4(b), this chapter aims to find a safe operating point outside the typical SOA given in the switch datasheets for a single pulse application without damaging the device. The idea is to perform the pulse current tests in an MMC submodule prototype especially designed for the AWG application where TO-packaged switches can be implemented. Therein, various switch technologies are tested, and later their performances are benchmarked to find the most suitable switch technologies for the MMC-based HV AWG.



Figuur 5.4: C2M0160120D (a) Transient Thermal Impedances (Junction - Case) (b) Safe Operating Area.

Since the requirements of the HV AWG application demands high pulse currents similar to the short circuit tests, switches are tested by discharging the charge stored in the capacitor into the Device Under Test (DUT) via an auxiliary loop that has minimal stray inductance and resistance to obtain the highest peak pulse current with the fastest rise time. Various external electrical factors determine the magnitude and rise time of the peak pulse current. The factors that affect magnitude of peak pulse current are Gate to Source/Emitter voltage (V_{GS}/V_{GE}) and Drain/Collector to Source/Emitter voltage (V_{DS}/V_{CE}). V_{GS}/V_{GE} determines the thickness of the conduction channel and hence higher values of V_{GS}/V_{GE} results in a thicker conduction channel. Hence more electrons can pass through the channel. V_{DS}/V_{CE} determines the potential difference applied across the bulk of the switch. Higher values of V_{DS}/V_{CE} results in higher potential difference applied across the bulk during the linear region of conduction and hence higher drain current. The gate resistance (R_G) determines the rise time directly as the time constant of the conduction channel is directly proportional to R_G [115]. Lower value of gate resistance results in a faster turn-on of the DUT. Thus, the lowest value of R_G is preferred. At high values of V_{DS}/V_{CE}, all DUTs undergo saturation because of pinch-off, limiting the peak pulse current magnitude to its final value [119]. Additionally, such a high magnitude of current heats up the DUT, resulting in increased bulk resistance of the DUT, reducing the peak magnitude of the current even further [120]. Therefore, first, the effect of the above-mentioned electrical parameters is studied experimentally using single switch technology. Later, the electrical behavior of different switch technologies with the same aforementioned electrical parameters are compared to one another to find out the most suitable technology that could satisfy the high current demand of the HV AWG application.

To study the pulse current capability, multiple switches are chosen, and their details are summarized in Fig. 5.5. First, Cree-Wolfspeed C2M0160120D device is selected to test the experimental setup for constant V_{GS} while applying variable V_{DS} and vice-versa. Additionally, the same tests are repeated on three different devices to understand their behavior statistically. The three boxes in Fig. 5.5 represent different groups for comparing the pulse current behaviors of various switch technologies. IGBTs are classified into NPT, Punch Through (PT), and Trench Gate Field Stop (FS) based on the

presence of an n+ buffer layer. Among these, NPT IGBT (SGW25N120) and FS IGBT (IHW40N120R5) from Infineon are selected to investigate their pulse current capabilities. Additionally, more NPT IGBTs from IXYS with higher blocking voltage capability, such as 1.7 kV (IXGH24N170) and 3.0 kV (IXBH20N300), are added to the list. MOSFETs are inherently famous for their faster switching characteristics over current carrying capacity. Therefore, Cool Si MOSFET (IPW90R120C3) from Infineon is selected to obtain a faster rise time. Since SiC MOSFET combines higher current carrying capability and fast switching characteristics, multiple devices from CREE-Wolfspeed with different current capabilities are selected to compare with other technologies.

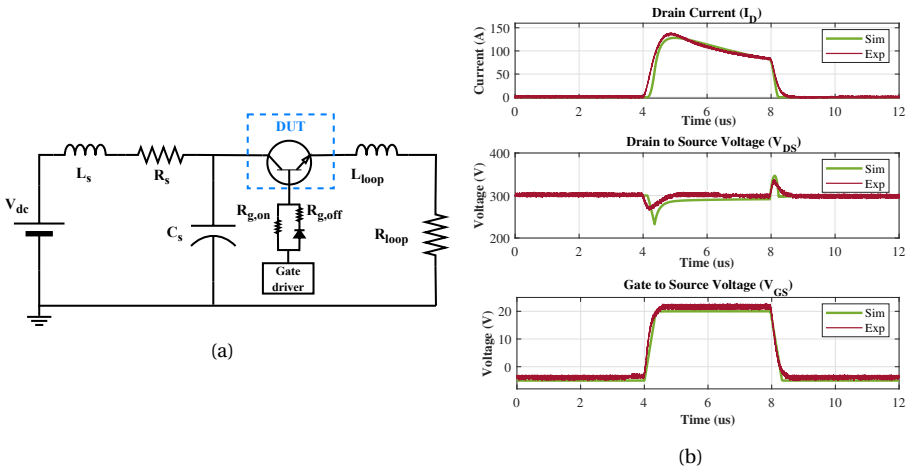
No.	Device name	Manufacturer	V_{BR} (V)	I_D/I_C 25 °C (A)	I_{pulse} (A)	Op range for V_{GS} (V)
1.	C2M0160120D SiC MOSFET	CREE-Wolfspeed	1200	18	40	-5 /+20
2.	C3M0075120D SiC MOSFET	CREE-Wolfspeed	1200	32	80	-5 /+15
3.	C2M0080120D SiC MOSFET	CREE-Wolfspeed	1200	36	80	-5 /+20
4.	IPW90R120C3 Cool Si MOSFET	Infineon	900	36	96	± 20
5.	SGW25N120 NPT IGBT	Infineon	1200	46	84	± 20
6.	IXGH24N170 NPT IGBT	IXYS	1700	50	150	± 20
7.	IXBH20N300 (NPT IGBT)	IXYS	3000	50	150	± 20
8.	IHW40N120R5 FS IGBT	Infineon	1200	80	200	± 20
9.	C3M0016120D SiC MOSFET	CREE-Wolfspeed	1200	81	200	-5 /+15

Figuur 5.5: Details of the tested switches.

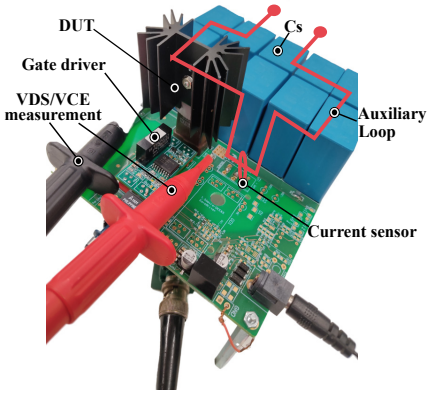
5.3.2. EXPERIMENTAL SETUP AND RESULTS

Fig. 5.6(a) shows the schematic of the test circuit to characterize the selected switches with an installed capacitance of 198 µF. In the actual test setup, the circuit is realized using a half-bridge submodule of an MMC where the high side switch is shorted using a wire for current measurement, and the low side switch acts as a DUT. Indeed, even if the submodule PCB design is optimized, some stray inductance and stray resistance are added to the auxiliary loop. Their respective values are measured from the setup when the DUT is not inserted in the DUT holder. Hence, the stray inductances and resistances are measured with an impedance analyzer (Agilent 4294 A) in two steps. Firstly, these values are measured from the positive DC voltage to the Drain of the DUT. Secondly, these values are measured from the Source of the DUT to the negative DC voltage. By adding these values, the loop inductance and resistance can be calculated as 120 nH and 160 mΩ. This means that the different switching technologies from different manufacturers can add different inductance and resistance to the auxiliary loop. The packaging of these discrete switches can add significant inductance to the loop, as illustrated in [121][122]. That is why it is crucial to investigate the pulse current capability of different switches experimentally. Furthermore, the test circuit is studied in the LTspice with a SiC MOSFET from Cree-Wolfspeed (C2M0160120D) with its actual spice model, and

the simulation results are compared with the experimental setup in Fig. 5.6(b). If the stray inductance and resistance are reduced from 120 nH and 160 mΩ to 30 nH and 40 mΩ in the spice model, the peak pulse current and the rise time of current waveform do not change. That means the DUT is saturating and limiting the pulse current over the stray inductance and resistance. The drain/collector current flowing through the DUT is measured using a Panasonic current sensor model 411. The V_{DS}/V_{CE} and V_{GS}/V_{GE} are measured using a differential probe from Keysight N2791A.



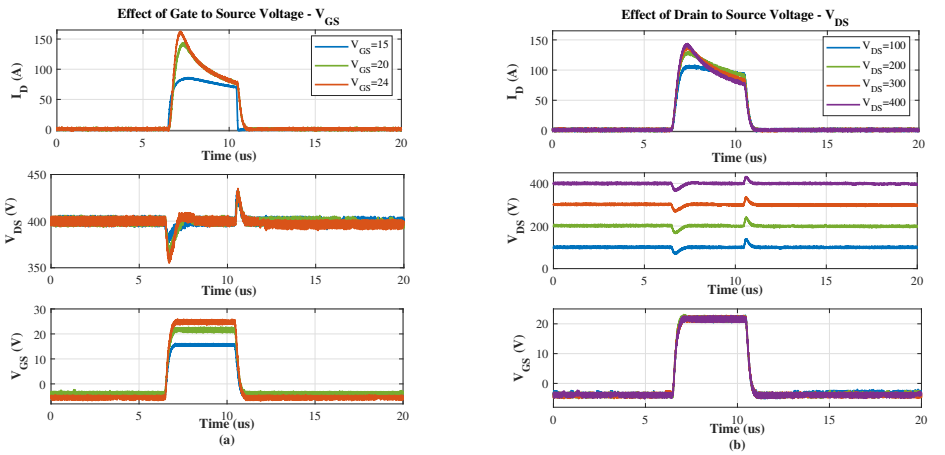
Figuur 5.6: (a) Schematic of the test setup (b) Comparison of LT-spice simulation and experimental results of C2M0160120D .



Figuur 5.7: Experimental setup for pulse current test of various switch technologies.

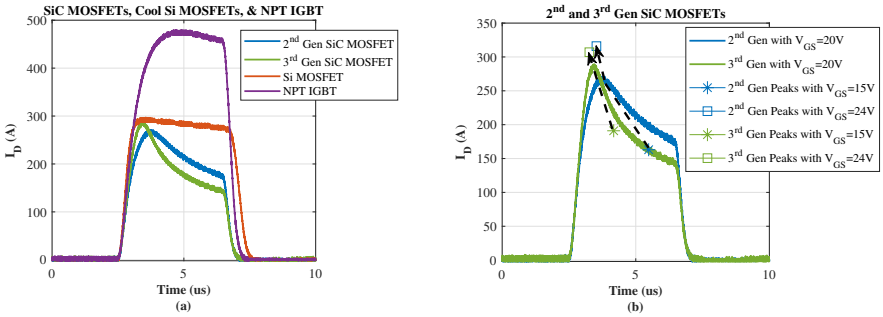
The experimental setup is shown in Fig. 5.7. As discussed in the previous section, several circuit parameters affect the pulse current characteristic of the DUT, such as V_{GS}/V_{GE}, V_{DS}/V_{CE}, and the turn-on gate resistance ($R_{g,on}$). To obtain the fastest rise time from

the DUT, the external turn-on gate resistance is set to 0 Ω for testing limits of all DUTs. Please note that the discrete switches have an internal gate resistance that limits the current rise time. However, the turn-off transient of the switch is limited by a much higher turn-off gate resistance ($R_{g,off}$), and the selected value is 10 Ω for all DUTs. The effect of V_{GS}/V_{GE} and V_{DS}/V_{CE} are studied with a SiC MOSFET (C2M0160120D), as shown in Fig. 5.8. With higher values of V_{GS}/V_{GE} and V_{DS}/V_{CE}, higher peak pulse currents are obtained with a faster rise time. However, the peak pulse current is more sensitive to V_{GS}/V_{GE} since it directly affects the thickness of the conduction channel that carries the current. Moreover, for the same V_{GS}/V_{GE}, the peak current capability is saturated for higher values of V_{DS}/V_{CE}, as it is visible in Fig. 5.8(b). These findings complement the theoretical understanding of these external electrical factors affecting the pulse current magnitude. Additionally, these tests are performed on multiple devices, their peak pulse currents are almost the same, and a maximum difference of 1.2 % is found. Hence, for other DUTs, statistical analyses are not performed.



Figuur 5.8: C2M0160120D (a) Effect of the turn-on-gate-to-source voltage for constant V_{DS} = 400 V (b) Effect of applied drain-to-source voltage V_{GS} = 20 V.

The first box from the list of tested switches consists of the NPT IGBT, Si Cool MOSFET, and SiC MOSFETs from 2nd and 3rd Generation with roughly the same rated current capability. The pulse current obtained from these four different technologies are compared at Fig. 5.9(a) for V_{GS} = 20 V. Since V_{GE}/V_{GS} and V_{CE}/V_{DS} waveforms follow a similar profile as shown in Fig. 5.8, they are excluded in Fig. 5.9 and further figures. It is visible that the NPT IGBT conducts a much higher magnitude of pulse current than all three technologies. However, Table 5.2 presented the rise time and obtained a slew rate, where NPT IGBT has the slowest rise time. Whereas the tested Si Cool MOSFET delivers the fastest rise time of 0.450 µs considering its superior switching performance. However, Si Cool MOSFET has an almost flat current profile compared to SiC MOSFET and Si IGBT, where higher V_{GS} values does not increase the peak current but only reduce the rise time. In the case of SiC MOSFETs, the current profile is significantly different at the peak and at the end of 4 µs. The 3rd generation SiC MOSFET performs better than the 2nd generation for



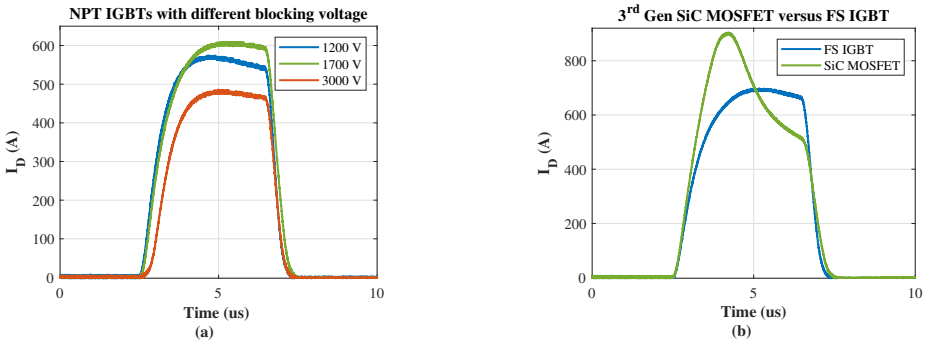
Figuur 5.9: V_{GS} = 20 V and V_{DS} = 300 V: Comparison of (a) SiC MOSFETs, Si MOSFET, and NPT IGBT (b) 2nd and 3rd generation SiC MOSFETs.

V_{GS} = 20 V both in terms of the peak current and the rise time. However, this behaviour has changed at V_{GS} = 24 V in terms of the peak current obtained, as shown in Fig. 5.9(b). This change can be attributed to the difference in the operating range of V_{GS} of 2nd and 3rd Generation SiC MOSFETs.

Tabel 5.2: Comparison Among 2nd and 3rd Generation SiC MOSFETs, Si MOSFET, and NPT IGBT

	C3M0075120D Gen SiC MOSFET I_c=32 A, I_p=80 A			C2M0080120D Gen SiC MOSFET I_c=36 A, I_p=80 A		
V_{GS} (V)	15	20	24	15	20	24
Pulse current obtained (A)	191	286	307	163	271	314
Times the rated current	6	8.9	9.6	4.5	7.53	8.7
Rise time (µs)	1.01	0.57	0.46	1.43	0.73	0.55
Slew rate (A/µs)	189	502	667	114	371	634
	IPW90R120C3 Cool Si MOSFET I_c=36 A, I_p=96 A			SGW25N120 NPT IGBT I_c=46 A, I_p=84 A		
V_{GS} (V)	15	20	24	15	20	24
Pulse current obtained (A)	297	296	295	281	476	570
Times the rated current	8.2	8.2	8.2	6.1	10.3	12.4
Rise time (µs)	0.53	0.42	0.44	1.06	1.04	1.04
Slew rate (A/µs)	560	705	670	265	458	548

Fig. 5.10(a) compares the pulse current capability of NPT IGBTs with different breakdown voltage ratings. The peak current obtained from 1.7 kV rated switch is the highest. However, the rise time to reach the peak current increases as the blocking voltage rating of the devices increases since their switching performances are poorer with a higher blocking voltage rating. Fig. 5.10(b) compares the performance of the 3rd Generation SiC MOSFET and FS IGBT at V_{GS} = 24 V. SiC MOSFET performs much better with respect to both the peak current capability and the rise time, and it is summarized in Table 5.3,



Figuur 5.10: V_{GS} = 24 V and V_{DS} = 300 V: (a) Effect of blocking voltage for NPT IGBTs (b) Comparison of SiC MOSFETs and FS IGBT.

which was also observed in [117].

5

Tabel 5.3: Comparison between 3rd Generation SiC MOSFET and FS IGBT

	C3M0016120D 3rd Gen SiC MOSFET I_c=81 A, I_p=200 A			IHW40N120R5 FS IGBT I_c=80 A, I_p=200 A		
VGS (V)	15	20	24	15	20	24
Pulse current obtained (A)	579	809	905	287	554	697
Times the rated current	7.2	10	11.2	4.5	6.9	8.7
Rise time (µs)	2.47	1.24	1.06	1.27	1.32	1.36
Slew rate (A/µs)	234	652	854	226	420	521

5.3.3. DISCUSSION OF EXPERIMENTAL RESULTS

The quantitative comparison from the last section shows that the 3rd generation SiC MOSFET with 30 A current rating has a comparable rise time as the Si Cool MOSFET (0.040 µs faster). Additionally, the amplification factor of the peak current with respect to the rated current for the same SiC MOSFET is 9.6, which is 9.3 % higher than the Cool MOSFET but 30 % lower than the NPT IGBT. However, the slew rate obtained from SiC MOSFET is higher than the NPT IGBT by 17.8 %. In Table 5.2, Cool Si MOS delivered the highest slew rate of 705 A/µs, which is 5.6 % higher than the SiC MOSFET. When the 30 A rated SiC MOSFET is compared with the 81 A rated SiC MOSFET, the latter delivers a much higher peak current, however, with a slower rise time. Additionally, the 81 A rated SiC MOSFET has achieved the highest slew rate among all tested switches, which is 17.5 % higher than the Si Cool MOSFET.

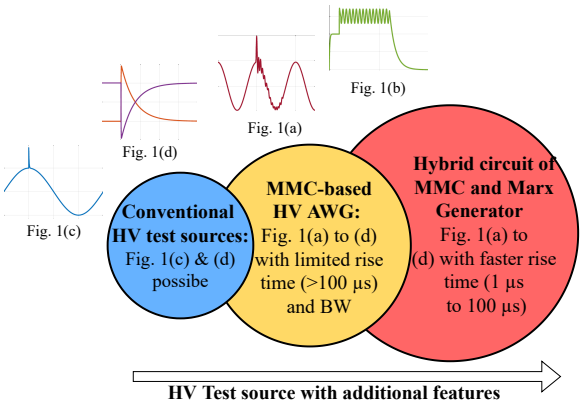
Apart from the quantitative comparison, it is important to understand qualitatively why different switch technologies behave differently in Fig. 5.9 and Fig. 5.10. The Si MOSFET has the flattest current profile, whereas the drain current of SiC MOSFETs rises to a peak and reduces to a lower value at the end of 4 µs. Compared to these two technologies, Si IGBTs exhibit similar behavior of flat current profile with the Si MOSFET, with a much

slower rise time. In all three device technologies, the DUT is saturated, and the conduction channel is pinched off considering the high value of the applied V_{DS}/V_{CE} [119]. The pinched-off state of the conduction channel adds significantly higher resistance for the drain/collector current to flow, and hence the peak value of the drain/collector current is limited. Additionally, when such a high current flows in the device, the temperature inside the substrate increases, and hence the overall bulk resistance increases. This relationship is linear in Si MOSFET and Si IGBT [123]. Hence, they have a flat pulse current profile in Fig. 5.9 and Fig. 5.10. However, SiC MOSFETs exhibit unique behaviour. When the temperature of the SiC device rises, the conduction channel exhibits a negative temperature coefficient. That is, the conduction channel resistance drops significantly, and charge carrier mobility increases in the conduction channel leading to the conduction of higher current magnitudes at the beginning of the current profile. But later, the resistance of the drift region dominates the overall resistance of the device as it starts to increase as the temperature increases leading to low values of drain current at the end of the current profile [115][123]. Due to these two effects, the current in SiC MOSFETs rises to a higher value and starts reducing to a lower value.

Apart from these dynamic factors, the obtained pulse current from various switches generally depends on the thickness of the device since the on-state resistance or bulk resistance directly depends on it. Among the different types of IGBTs, FS IGBT has the smallest thickness compared to NPT and PT IGBTs [124]. Therefore, it gives a comparable performance to a SiC MOSFET. With superior SiC material properties, the thickness of SiC MOSFET is significantly lowered [125]. Combining this property with the positive coefficient of channel mobility with temperature, SiC MOSFETs have superior performance. Among the Si MOSFET and IGBT which have flat profiles, the IGBT allows a higher peak pulse current considering its lower on-state resistance [119]. Nevertheless, this highest slew rate obtained from the 81 A SiC MOSFET is ten times smaller than the requirement of the application. Additionally, the obtained peak current and rise time are two times lower and five times slower than the requirement. Hence, it can be concluded that the SiC MOSFET with a lower current rating and lower voltage rating will have superior switching performance, which may give the fast rise time of 0.2 µs. However, multiple lower current rated SiC MOSFETs need to be connected in parallel to meet the requirement of the peak current, similar to discussed in [126]. This makes the switch implementation complex to generate such a severe dv/dt stress across the capacitive load.

5.4. MOTIVATION FOR THE HYBRID CIRCUIT

Even though the parallel operation of several low current rated SiC MOSFETs may satisfy the necessary peak pulse current capability, it is not ideal for the MMC-based HV AWG to increase the complexity even further. Hence, another solution direction of hybrid circuit is explored in the following sections to satisfy the steep pulse requirement. The hybrid circuit of an MMC and Marx generator combines the capability of these two sources, making the complex waveforms with steep impulses possible. Fig. 5.11 summarizes the additional capabilities offered by this hybrid HV test circuit compared to the conventional HV test source circuit.



Figuur 5.11: Summary of additional capabilities offered by the MMC-based HV AWG.

5

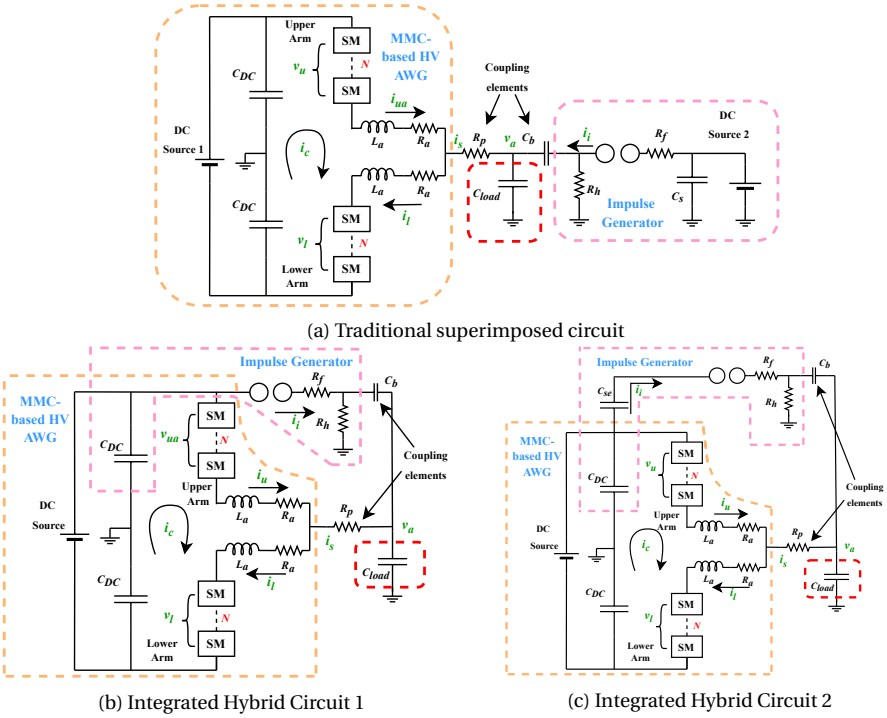
The traditional superimposed circuit in Fig. 2.10 can add an impulse waveform on a sinusoidal or DC waveform. However, the MMC-based HV AWG can generate other high-frequency harmonics in the transient voltage stresses experienced by different HV equipment with the limited rise time possible up to 100 µs. This limit is set considering the arm current flowing through the switches during steep rising impulses. However, when the rise time is increased from 1.2 µs to 100 µs, the current peak shown in Fig. 5.3 is reduced 100 times. With the current peak reduced to roughly around 17 A, discrete switches with 5 A to 9 A can be chosen since they can withstand 2-3 times higher current than rated values.

This chapter focuses on the hybrid circuit design and generation of the complex wave shapes from Fig. 5.1(a) and (b) with LI and the two conventional test waveforms shown in Fig. 5.1(c) and (d). Moreover, the capability of the MMC-based AWG is showcased with 100 kV output voltage in the MATLAB-Simulink simulation, and the test object is kept the same as MV equipment (10 nF).

5.5. SCHEMATIC OF THE PROPOSED HYBRID CIRCUIT

Fig. 2.10 from Chapter 2 shows the IEC-recommended circuit for generating the waveforms which include DC or sinusoidal with steep impulses. Similarly, the MMC and Marx generator circuit can be connected in parallel across the load capacitor, as shown in Fig. 5.12(a). It includes the complete schematic of the MMC-based HV AWG and a single stage of the impulse generator. Additionally, some coupling elements are necessary to protect two different circuits from each other, and their design is discussed in later sections. From the schematic of this hybrid circuit, it is clear that both test sources need capacitor-based DC input sources. Considering the high cost and large sizes of the HV DC sources and the capacitors, two possible integrated hybrid circuits are proposed in Fig. 5.12(b) and 5.12(c) which combines the DC input side of these sources. Additionally, the integrated circuit can reduce the preparation time for the superimposed test because it removes the need to move different equipment and test objects from one lab section

to another, which can be crucial in commercial testing.



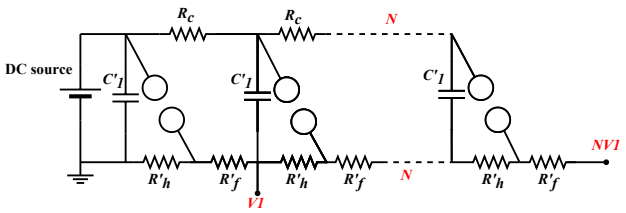
(a) Traditional superimposed circuit

(b) Integrated Hybrid Circuit 1

(c) Integrated Hybrid Circuit 2

Figuur 5.12: MMC-based HV AWG to generate LI waveform.

The two proposed integrated hybrid circuits are pretty similar, except Fig. 5.12(c) has an additional capacitor (C_{se}). From the basic understanding of the Marx generator circuit, the input capacitor gets entirely discharged into the test object [127]. It means that the DC link capacitance (C_{DC}) from Fig. 5.12(b) will be discharged after one impulse, which is not suitable for the proper operation of the MMC-based HV AWG. Hence, Fig. 5.12(c) has an additional capacitor C_{se} which does not allow the C_{DC} capacitor discharge during the impulses by charging up the C_{se} capacitor negatively. This means that the voltage combined from C_{DC} and C_{se} will be zero, keeping the working principle of the Marx generator circuit intact. Additionally it is essential to highlight that the design of the hybrid circuit in Fig. 5.12(a) and Fig. 5.12(c) is the same except for the additional design requirement for the DC side in case of the later circuit. Please note that all sub-figures in Fig. 5.12 contain single stage of Marx generator. To obtain higher voltage than the DC source, multi-stage Marx generator circuit need to be used and its schematic is shown in Fig. 5.13. However, the feasibility of the integrated hybrid circuit is conducted with the single stage Marx generator and their design guidelines are discusses in the following section.



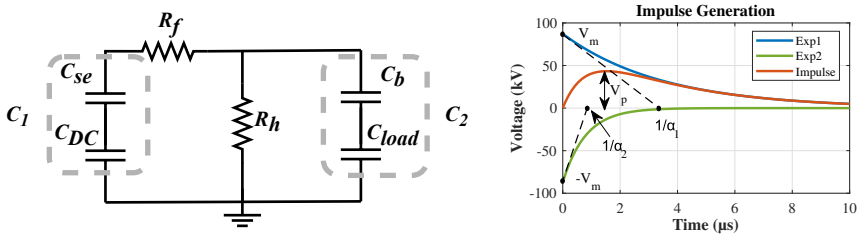
Figuur 5.13: Cascaded Marx generator circuit.

5.5.1. DESIGN GUIDELINES

Though the design guidelines of the MMC-based HV AWG and Marx generator are known, the two test circuits are coupled with each other using two coupling elements. The first one is the parallel resistor (R_p) connected just before the load capacitor, and it protects the HV AWG during the impulse formation from high currents. The second element is the coupling capacitor (C_b) which protects the impulse generator from the HV AWG test source by blocking low-frequency waveforms. It is possible to use a capacitor or a spark gap as a protective element. However, a capacitor offers more reliable operation compared to the spark gap [128]. Please note that the design recommendations of the above-mentioned two additional parameters are common for both the traditional and integrated hybrid circuits. Moreover, the source capacitor (C_{se}) is added in the integrated hybrid circuit, which helps to maintain the voltage across the split DC link capacitor (C_{DC}) during the impulse formation. The design of the source capacitor can be derived from the Marx generator design guidelines. However, it affects the DC side input of the MMC-based HV AWG. Hence, it is essential to study its effect on the regular operation of the MMC-based HV AWG. With these additional elements and the involved coupling of two circuits, the design of such an integrated hybrid circuit needs to be carefully done analytically, with a simulation model and experimental setup. For simplicity, the analytical study of the integrated hybrid circuit is divided into three parts, i.e., Marx generator side, MMC side, and the coupled circuits, and each part is elaborated in the following subsections.

FROM MARX GENERATOR SIDE

Fig. 5.14(a) shows the schematic of the equivalent Marx generator circuit adapted from the integrated hybrid circuit. Here, the DC side input capacitor (C_1) is a series combination of two capacitors C_{se} and C_{DC} and the load capacitor (C_2) is also a series combination of two capacitors C_b and C_{load}. In this circuit, the impulse waveform is formed by subtracting one exponential function from another, as shown in Fig. 5.14(b). Mathematically, the impulse waveform is represented in (5.1), where the relationship of the circuit parameters (R_f, R_h, C_1 and C_2) to the time constants (α_1 and α_2) is shown from (5.2) to (5.5) [7]. The first exponential function ($e^{-\alpha_1 t}$) dictates the tail time of the impulse, and the second exponential function ($e^{-\alpha_2 t}$) decides the front time of the impulse. The rise time and the tail time of the impulse can be altered using the front resistor (R_f) and the tail resistor (R_h), respectively. Here, V_m is the magnitude of both of the exponential functions, and the V_p is the peak amplitude of the obtained impulse waveform.



(a) (a)

Figuur 5.14: (a) Equivalent Marx generator circuit (b) Impulse formation.

Tabel 5.4: Relationship of Time Constants of Impulse Waveforms to α_1 and α_2

Impulse Waveform	$1/\alpha_1$ (μs)	$1/\alpha_2$ (μs)
Lightning Impulse (1.2 μs/50 μs)	68.2	0.405
Switching Impulse (250 μs/2500 μs)	3155	62.5

5

$$v_i(t) = V_m(e^{-\alpha_1 t} - e^{-\alpha_2 t}) \tag{5.1}$$

$$\alpha_1, \alpha_2 = \frac{a}{2} \mp \sqrt{(\frac{a}{2})^2 - b} \tag{5.2}$$

$$a = \frac{1}{R_f C_1} + \frac{1}{R_f C_2} + \frac{1}{R_h C_1} \tag{5.3}$$

$$b = \frac{1}{R_f R_h C_1 C_2} \tag{5.4}$$

$$k = R_f C_2 \tag{5.5}$$

$$V_m = \frac{V_0}{k(\alpha_2 - \alpha_1)} \tag{5.6}$$

Though it is evident that the time constants (α_1 and α_2) in the exponential functions dictate the rise time and tail time of the impulse waveforms, the relationship is irrational, and it must be computed numerically as done in [7]. Table 5.4 shows the relationship for the most common impulse waveforms in the HV testing. Based on these values, the front resistor and tail resistor can be calculated from (5.7) and (5.8) for the given value of capacitances (C_1 and C_2). The square-root term must exceed zero to obtain real front and tail resistor values. Hence, this puts a maximum condition on the ratio of C_1 and C_2 capacitors for real values of front and tail resistors, and it is shown in (5.9).

$$R_f = \frac{1}{2C_1}[(\frac{1}{\alpha_1} + \frac{1}{\alpha_2}) - \sqrt{(\frac{1}{\alpha_1} + \frac{1}{\alpha_2})^2 - \frac{4(C_1 + C_2)}{\alpha_1 \alpha_2 C_2}}] \tag{5.7}$$

$$R_h = \frac{1}{2(C_1 + C_2)}[(\frac{1}{\alpha_1} + \frac{1}{\alpha_2}) + \sqrt{(\frac{1}{\alpha_1} + \frac{1}{\alpha_2})^2 - \frac{4(C_1 + C_2)}{\alpha_1 \alpha_2 C_2}}] \tag{5.8}$$

$$\frac{C_1}{C_2} \leq \frac{(\alpha_1 - \alpha_2)^2}{4\alpha_1\alpha_2} \tag{5.9}$$

The following important criterion for creating design guidelines for the Marx generator is the voltage efficiency (η) of the impulse waveform. Fig. 5.14(b) makes it clear that the peak of the impulse waveform (V_p) will always be less than the charged voltage (V_m) of the input capacitor. However, it is possible to obtain higher voltage by having Marx generator with multiple stages, as shown in Fig. 5.13. Here, for the single stage Marx generator, the voltage efficiency (η) is defined as the ratio of V_p to V_m and the magnitude of V_p can be obtained by finding the maxima of expression (5.1), and this leads to the efficiency expressions, as shown in (5.10)[7]. If $C_1 > C_2$ and $\alpha_2 >> \alpha_1$, the efficiency expression can be simplified, and it is shown in (5.11). This means that the ratio of C_1 and C_2 should be as large as possible to obtain high voltage efficiency. However, it should be less than the value calculated in (5.9) to obtain real values of front and tail resistors for the given impulse waveform.

$$\eta = \frac{(\alpha_2/\alpha_1)^{-}[\alpha_2/(\alpha_1 - \alpha_2)] - (\alpha_2/\alpha_1)^{-}[\alpha_2/(\alpha_2 - \alpha_1)]}{k(\alpha_2 - \alpha_1)} \tag{5.10}$$

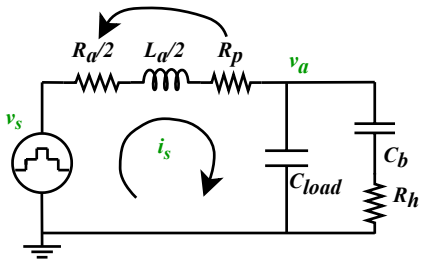
$$\eta \approx \frac{1}{1 + (C_2/C_1)} \tag{5.11}$$

FROM MMC SIDE

Fig. 5.15 shows the equivalent circuit of the MMC when integrated with the Marx generator. It has three additional elements which are the parallel resistor (R_p), the coupling capacitor C_b and the tail resistor R_h. All three are affecting the normal operation of the MMC-based AWG. Hence, their selection must consider the following three conditions:

- The transient current is limited within the permitted range of the switches and other passive elements during the superposition of impulse waveform
- The continuous arm current values need to be less than 5 A considering the rating of the designed switches
- The output voltage should not be dropped more than 1 % due to the increased load to the MMC.
- The normal operation of MMC needs to be restored, like balancing SM capacitor voltages and quality of output voltage waveform.

As explained earlier, the parallel resistor (R_p) is added before the load capacitor to protect the MMC from high transient currents generated when the impulse is superimposed on the arbitrary waveform. However, the equivalent circuit from Fig. 5.15 shows that the parallel resistor is in series with the arm resistor (R_a), and it can protect the MMC from transients generated during the impulse formation. This will reduce the requirement for an additional HV resistor. Hence, the arm resistor, apart from damping the resonance in the MMC-based AWG between the load capacitor and arm inductor, is designed to limit the arm current transient occurred due to the sudden change in the output voltage



Figuur 5.15: MMC Side.

(v_a) during the superposition of LI. As per the transfer function of the output current circuit of the MMC from Fig. 5.15, the minimum value of R_a to avoid undesired oscillations is defined in (5.12) [99]. It considers only the load capacitance instead of the series connection of two capacitances since the coupling capacitor is connected to the Marx generator, and a higher value of R_a is needed to avoid oscillations during the impulse formation. Secondly, the resistance limits the peak current, and its magnitude can be estimated using the following expression (5.13). Additionally, the large arm inductor value reduces the di/dt on the switches, as shown in (5.14).

$$R_a \geq \sqrt{(\frac{8L_a}{C_{load}})} \tag{5.12}$$

$$I_{u,l} = \frac{V_p}{R_a} \tag{5.13}$$

$$L_a = V_p / (\frac{\mathrm{d}i_{u,l}}{\mathrm{d}t}) \tag{5.14}$$

The effect of the added load (C_b & R_h) to the MMC can be studied by finding its transfer function, and it is shown in (5.15) to (5.17). This transfer function clearly shows that the load has changed the typical second-order low-pass filter with two poles to a system with three poles and one zero. From the bode plot of this transfer function, the magnitude at the reference frequency of the MMC should be checked so that the voltage drop across the load of the MMC can be determined. Moreover, this added load affects the continuous arm current flowing through the MMC. The value of the coupling capacitor should be much higher than the load capacitor to obtain a higher voltage drop across C_{load} compared to C_b. However, it can overload the MMC, affecting the output voltage peak and drawing excessive current from the MMC. Assuming the value of C_b is much larger than C_{load}, the value of the coupling capacitor dictates the current flowing from the arm current ($I_{u,l} = V_a w C_b/2$). This current consumption should be kept within 5 A, considering the design specification of the test source. Generally, the chosen value of R_h is significantly less compared to the impedance of the capacitor.

$$\frac{V_a[s]}{V_s[s]} = \frac{2(C_b R_h s + 1)}{C_b C_{load} L_a R_h s^3 + p s^2 + q s + 2} \tag{5.15}$$

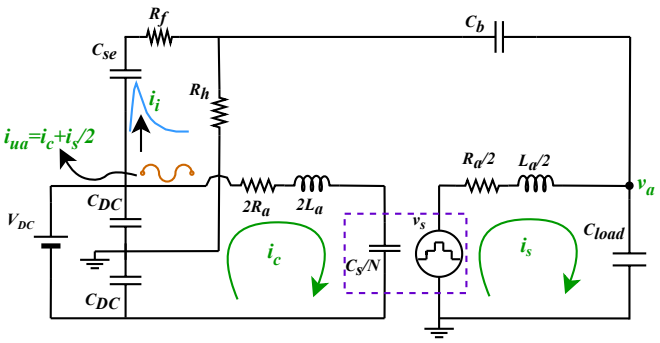
$$p = ((C_{load} R_a R_h + L_a) C_b + C_{load} L_a) \tag{5.16}$$

$$q = ((R_a + 2R_h) C_b + C_{load} R_a) \tag{5.17}$$

The equivalent load of the MMC-based HV AWG is capacitive. Hence, there is no significant active power transfer in the MMC, with the average circulating current being zero [99]. Additionally, the output current requirement is not high (less than 5 A). Hence, the SM capacitor voltage balancing can be maintained with Phase Shift Carrier (PSC) modulation technique since it inherently uses the SMs evenly [67]. A similar principle is applied in this case since the value of the tail resistor is low.

COUPLED CIRCUIT

Fig. 5.16 shows the equivalent circuit of MMC together with the Marx generator circuit and the coupling capacitor. In the following subsections, the coupled circuit is analysed from the DC side, and the Marx generator circuit design is revisited with considering the influence of the MMC branch ($L_a/2$ and $R_a/2$).



Figuur 5.16: Coupling with integrated hybrid circuit.

INPUT DC SIDE

The input DC side is the same for the two test sources for the integrated hybrid circuit. Hence, it is essential to look into the design of the DC link capacitors (C_{DC}) and the source capacitor (C_{se}) while considering the coupling of two test circuits, as shown in Fig. 5.16. The DC link capacitance value should be as large as possible since it maintains the DC link voltage and generate proper bipolar waveforms without any offset in the MMC output voltage. However, as the DC link voltage increases, finding capacitors commercially available for more than a few hundred nanofarads is more problematic. This capacitor provides the continuous arm currents ($i_u = i_c + i_s/2$) for the MMC, and it acts as a DC source to charge the Marx generator capacitor (C_{se}) with the impulse current (i_i). The value of this DC link capacitor can be decided based on the allowed voltage

rippled due to the continuous MMC arm current (dv_1) and due to the short and very steep impulse (dv_2). The value of C_{se} should be chosen based on the ratio required for the better efficiency of the Marx generator, as shown in (5.9).

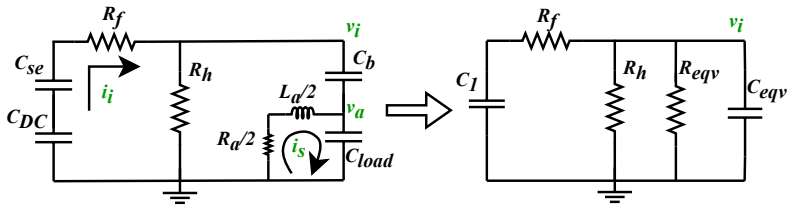
$$C_{DC} = \frac{1}{4 f d v_1} \frac{I_s}{2} \tag{5.18}$$

$$I_s = m_a V_{DC} \pi f C_b \tag{5.19}$$

$$C_{DC} = \frac{1}{d v_2} \int_0^{500\,\mu s} i_i \, dt \tag{5.20}$$

MARX GENERATOR WITH MMC

Fig. 5.16 shows the complete coupled circuit where the MMC branch ($L_a/2$ and $R_a/2$) is connected parallel to the load capacitor (C_{load}). This inductive load changes the behavior of impulses generated with the hybrid circuit of the MMC and the Marx generator. Generally, the superimposed circuit discussed in [110] and [111] does not have this effect since the transformer or HV DC source has a large impedance, reducing its effect on the Marx generator. However, the arm inductor present in the MMC is finite, and it can not be increased infinitely since it decides the output voltage characteristics of the MMC. Though the equations from (5.1) to (5.11) give an excellent understanding of the Marx generator, it is important to analyse the updated circuit with the influence of the MMC branch, as shown in Fig. 5.17. The influence of the added MMC branch can be studied by calculating the equivalent parallel resistor (R_{eq}) and equivalent load capacitor (C_{eq}) for a particular frequency considering the impulse rise time or tail time from (5.21) and (5.22). The equivalent circuit can allow using the same equations to determine the front and tail resistors, as shown in (5.12) and (5.13) with updated Marx generator parameters.



Figuur 5.17: Updated Marx generator circuit with MMC.

$$\begin{aligned} R_{eq} = (&C_b^2 L_a^2 w^4 + 2 C_b C_{load} L_a^2 w^4 + C_{load}^2 L_a^2 w^4 + C_b^2 R_a^2 w^2 + \\ &2 C_b C_{load} R_a^2 w^2 + C_{load}^2 R_a^2 w^2 - 4 C_b L_a w^2 - 4 C_{load} L_a w^2 + 4) / 2 C_b^2 R_a w^2 \end{aligned} \tag{5.21}$$

$$\begin{aligned} C_{eq} = (&C_b (C_b C_{load} L_a^2 w^4 + C_{load}^2 L_a^2 w^4 + C_b C_{load} R_a^2 w^2 + C_{load}^2 R_a^2 w^2 - 2 C_b L_a w^2 \\ &- 4 C_{load} L_a w^2 + 4)) / (C_b^2 L_a^2 w^4 + 2 C_b C_{load} L_a^2 w^4 + C_{load}^2 L_a^2 w^4 + C_b^2 R_a^2 w^2 \\ &+ 2 C_b C_{load} R_a^2 w^2 + C_{load}^2 R_a^2 w^2 - 4 C_b L_a w^2 - 4 C_{load} L_a w^2 + 4) \end{aligned} \tag{5.22}$$

The equivalent circuit mentioned above gives the correct impulse waveform across the equivalent load (R_{eq} & C_{eq}) and not across the actual load. Hence, the voltage across the actual load (v_a) needs to be derived from the voltage across the equivalent load (v_i). The voltage across the actual load is derived first in the Laplace domain and then in the time domain from (5.23) to (5.27). Here, it is important to highlight that the time domain equation in (5.26) has another exponential term with α_3 time constant, and its value is dictated by the MMC parameters (R_a and L_a) and load parameters (C_{load} and C_b). Hence, the relation between time constants and impulse parameters shown in Table 5.4 is not valid anymore. Depending upon the MMC parameters and load parameters, the required α_1 and α_2 will differ, ultimately changing the choice of R_f and R_h.

$$\begin{aligned} V_a[s] &= \frac{(\frac{R_a+sL_a}{2})||(\frac{1}{sC_{load}})}{(\frac{R_a+sL_a}{2})||(\frac{1}{sC_{load}}) + \frac{1}{sC_b}} V_i[s] \\ &= \frac{s^2c+sd}{s^2+sa_2+b_2} V_i[s] \\ &= \frac{s^2c+sd}{s^2+sa_2+b_2}(\frac{Vm}{s+\alpha_1} - \frac{Vm}{s+\alpha_2}) \end{aligned} \tag{5.23}$$

$$a_2 = \frac{R_a}{L_a}; b_2 = \frac{2}{L_a(C_b+C_{load})} \tag{5.24}$$

$$c = \frac{C_b}{(C_b+C_{load})}; d = \frac{R_aC_b}{L_a(C_b+C_{load})} \tag{5.25}$$

$$\begin{aligned} v_a(t) &= \mathcal{L}^{-1}[\frac{s^2c+sd}{s^2+sa_2+b_2}(\frac{Vm}{s+\alpha_1} - \frac{Vm}{s+\alpha_2})] \\ &= V_{m1}e^{-\alpha_1 t} - V_{m2}e^{-\alpha_2 t} - V_{m3}e^{-\alpha_3 t} \end{aligned} \tag{5.26}$$

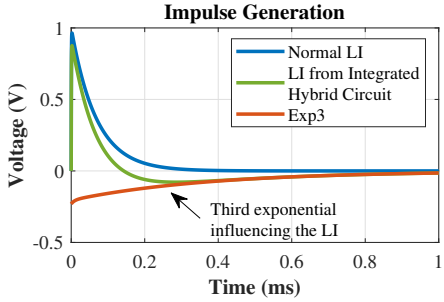
$$\alpha_3 = \frac{a_2}{2} - \sqrt{(\frac{a_2}{2})^2 - b_2} \tag{5.27}$$

$$V_{m1} = \frac{-(\alpha_1 c - d)\alpha_1}{a_2\alpha_1 - \alpha_1^2 - b_2}; V_{m2} = \frac{(\alpha_2 c - d)\alpha_2}{a_2\alpha_2 - \alpha_2^2 - b_2} \tag{5.28}$$

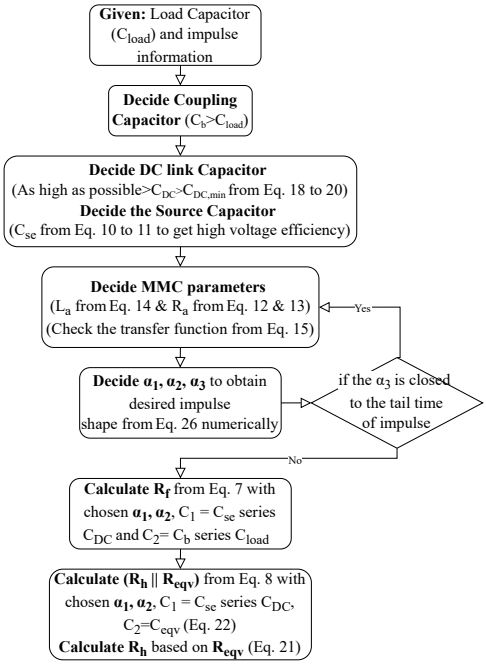
$$V_{m3} \approx \frac{(\alpha_1-\alpha_2)(a_2\alpha_1\alpha_2 c - \alpha_1\alpha_2 d - \alpha_1 b_2 c - \alpha_2 b_2 c + b_2 d)}{(a_2\alpha_2 - \alpha_2^2 - b_2)(a_2\alpha_1 - \alpha_1^2 - b_2)} \tag{5.29}$$

Fig. 5.18 shows the influence of the third exponential function on LI generation with circuit parameters as $R_a = 700$, $L_a = 6\,\text{mH}$, $C_b = 1\,\mu\text{F}$ and $C_{load} = 100\,\text{nF}$. Though the magnitude of the exponential term with α_3 time constant is not high, it impacts the tail time of the LI by reducing its value, and it adds a slight negative overshoot to the LI. Since the time constant of the third exponential function is much higher than the rise time of the impulse, it does not affect it. Hence, it is crucial to choose the MMC and load parameters

so that rise time is not affected. Additionally, this third exponential limits how much tail time one can obtain with the given MMC and load parameters. For example, the time constant of the third exponential with the above-mentioned circuit parameters is 376 µs, and it is already not possible to obtain a tail time of more than 130 µs. The increase in the R_h has little influence on the tail time after this limit. It is important to choose the arm resistor that damps the resonance properly as per (5.12) for the above-derived equations to be valid. Fig. 5.19 summarizes a step-wise procedure for choosing the system parameters of the integrated hybrid circuit.



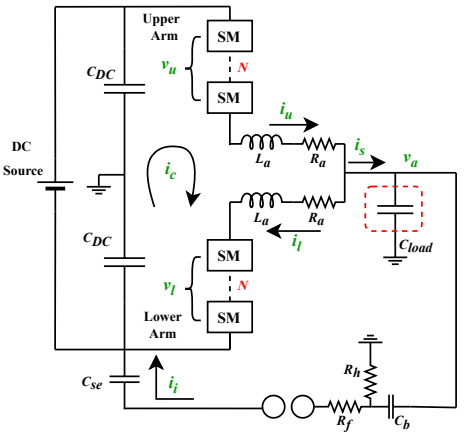
Figuur 5.18: LI when generated from Integrated Hybrid Circuit.



Figuur 5.19: Parameter design procedure for the integrated hybrid circuit.

NEGATIVE IMPULSE

Generally, the negative impulse is generated by charging the input side capacitor to a negative voltage [127]. The negative impulse is generated using the bottom DC link capacitor with the integrated hybrid circuit since it is negatively charged. The schematic of an integrated hybrid with negative impulse capability is shown in Fig. 5.20. Physically, the power connection of the source capacitor has to be changed from the +DC side to the -DC side capacitor. Additionally, the current direction is reversed since the negative impulse will generate current to flow from the load to the source. The other working principle of the integrated hybrid circuit remains the same as the positive impulse circuit with the current reversal.



Figuur 5.20: Integrated hybrid circuit for negative impulse generation.

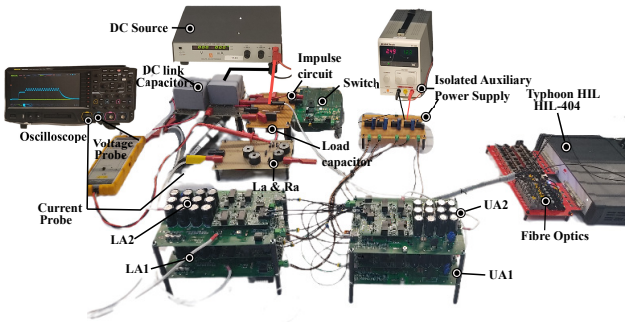
5.5.2. SIMULATION AND EXPERIMENTAL RESULTS

The concept of the integrated hybrid circuit and the above-discussed analysis are validated with MATLAB-Simulink simulations and experimental results, where the prototype is built for a scaled-down voltage level. The output voltage of 100 kV is scaled down to 150 V where the DC link voltage is 300 V with 2 submodules per arm. The 10 nF load capacitor is a worst-case scenario for the LI waveform generation. However, for the scaled-down prototype, a higher value of the load capacitor of 100 nF is chosen to demonstrate the design of the integrated hybrid circuit since few submodules are present. For the given load capacitor, a coupling capacitor of 1 µF is used to get 90 % of the impulse voltage across the load. The DC link capacitors for the Marx generator circuit are fixed to be significantly high value of 220 µF. For the source capacitor, 1.1 µF is chosen to obtain the voltage efficiency as high as 92 % as per (5.11). Since there is a voltage drop across the coupling capacitor, the obtained efficiency will be around 82 %. For the MMC, the arm inductance of 6 mH is selected, which imposes the arm resistor to be more than 698 Ω. With the availability of a resistor in the ESP lab of TU Delft, an arm resistor of 750 Ω is added in the MMC to damp oscillations and to limit the transient in the arm current. By following the procedure summarized in Fig. 5.19, the front resistor and tail

Tabel 5.5: System Parameters of the Scaled-down Prototype

No.	Description	Label	Value
1.	DC link Voltage	V_{DC}	300 V
2.	Output Voltage	V_a	150 V
3.	Number of Submodules	N	2
4.	Modulation Index	m_a	0.9
5.	Submodule Capacitance	C_s	75 µF
6.	Arm Resistor	R_a	750 Ω
7.	Arm Inductor	L_a	6 mH
8.	Load Capacitor	C_{load}	100 nF
9.	Coupling Capacitor	C_b	1 µF
10.	DC link Capacitor	C_{DC}	220 µF
11.	Source Capacitor	C_{se}	1.1 µF
12.	Front Resistor	R_f	5.45 Ω
13.	Tail Resistor	R_h	76.7 Ω

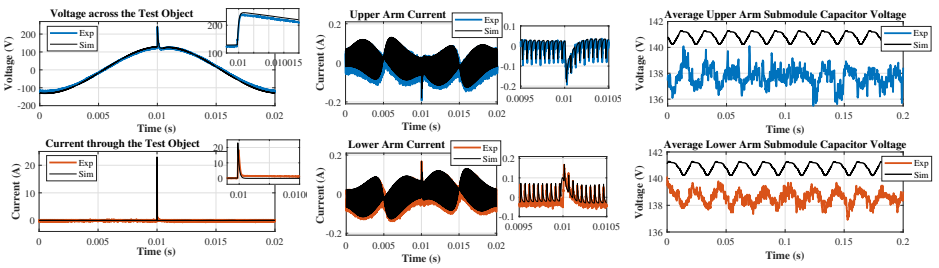
resistor are calculated to be 5.1 Ω and 79.7 Ω, respectively. However, based on the availability of resistors, the closest values of 5.45 Ω and 76.7 Ωare prepared for the hardware. These system parameters are summarized in Table 5.5. Additionally, Fig. 5.21 shows the scaled-down prototype used for demonstrating the experimental results. It is essential to highlight that the Marx generator circuit is made compact with the least possible wiring to avoid stray inductance, limiting the overshoot in the LI [8]. Also, a discrete TO-247 SiC MOSFET (H090) is implemented instead of a spark gap to demonstrate the idea of the integrated hybrid circuit.



Figuur 5.21: Scaled-down experimental setup.

Fig. 5.22 showcases the LI superimposed on a 50 Hz sinusoidal waveform where the MATLAB-Simulink simulation results match well with the experimental results. Here, Fig. 5.22(a) displays the output voltage and current. The LI is superimposed on the sinusoidal waveform at 0.01 s, where the current through the test object is raised as high as 17 A in the experimental work to 22 A in the simulation results. The amount of current is reduced in the experiment considering the higher resistance and non-ideal nature of switching. The rise time and tail time of the obtained LI are 1.0 µs and 48 µs, respecti-

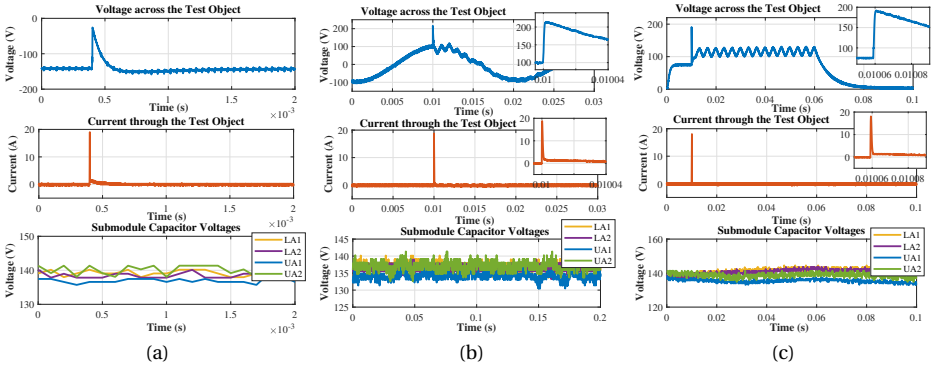
vely. The rise time and tail time are calculated based on the IEC standard (IEC60060-1) [14], and the obtained values are within the tolerances mentioned in the standard. Since the implemented tail resistor is slightly less than the designed values, the obtained tail time has a small error. Additionally, the magnitude of LI is 115 V, which gives the voltage efficiency of 77 %. This value is less than the designed value of 82 %, considering the estimation of the efficiency is done with an approximate formula. Fig. 5.22(b) shows the arm currents and the transient current occurring at the superposition of impulse is well within the limit of the switches, and the peak of the transient current is the same as that of the estimate in (5.13). Lastly, Fig. 5.22(c) shows the average submodule capacitor voltages, and the ripple waveform matches well from the simulation to the experimental results with an offset in their average voltages. It can be attributed to the higher arm resistor in the experiments. In this figure, the LI is superimposed on the positive peak of the sinusoidal. However, the time instant where the impulse is superimposed can be varied by changing the offset of the gate pulse sent to the switch.



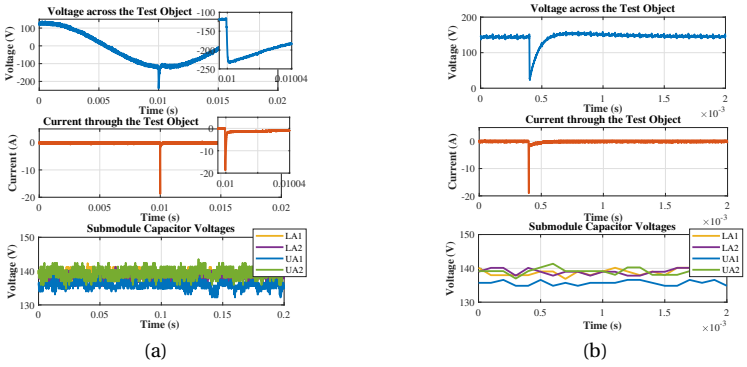
(a) Output characteristics (b) Arm Currents (c) Submodule Capacitor voltages

Figuur 5.22: Positive LI superimposed on 50 Hz sinusoidal waveform.

Fig. 5.23 shows the positive LI superimposed on three other arbitrary wave shapes, where the output voltage, output current, and the submodule capacitor voltages are shown. First, Fig. 5.23(a) displays the superposition of positive LI on the negative DC waveform for the duration of 2 ms. The second waveform in Fig. 5.23(b) is the transient waveform containing 50 Hz sinusoidal and higher harmonics. At last, Fig. 5.23(c) shows the unipolar complex waveform with LI at the 0.02 s time instant. For the unipolar waveform like in Fig. 5.23(a) and Fig. 5.23(c), the submodule capacitor voltages are shown only for the time interval of the output voltage waveform. These waveforms are not continuously generated like sinusoidal, but they are generated as a single shot. Because the submodule capacitor voltages start to get unbalanced with its continuous generation, especially due to just 2 submodules per arm. Generation of unipolar waveform needs further work to invent proper control methodology using Full Bridge topology and is out of scope of this PhD thesis. Fig. 5.24 displays the results when negative LI is superimposed on sinusoidal and DC waveform. As discussed in the last section, the working principle of the negative impulse generation is the same where the current direction is reversed.



Figuur 5.23: Positive LI superimposed on (a) Negative DC (b) 50 Hz Sinusoidal and higher harmonics (c) Unipolar complex waveform.



Figuur 5.24: Negative LI superimposed on (a) 50 Hz sinusoidal (b) Negative DC waveform.

5.5.3. HV SIMULATION RESULTS

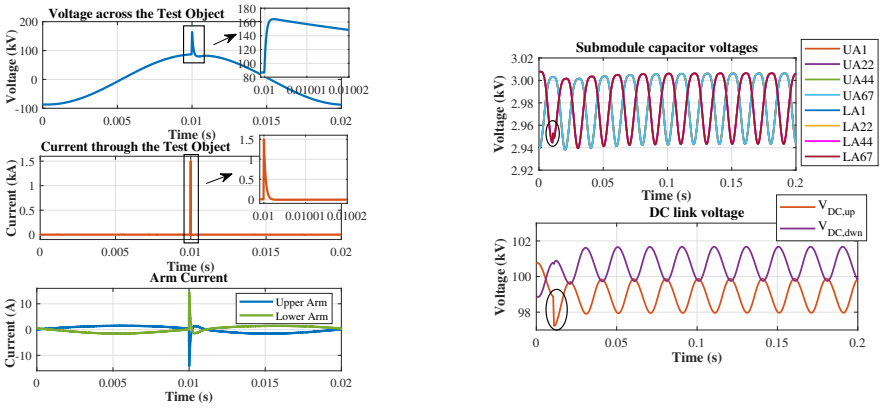
This section demonstrates the performance of the integrated hybrid circuit with 200 kV DC link voltage and 10 nF of load capacitor. This study is important to verify if it is possible to choose system parameters at high voltage and achieve the superposition of LI without affecting the MMC. Similar to the scaled-down prototype, the coupling capacitor is first chosen to be 100 nF considering the 90 % voltage drop across the load capacitor. The DC link capacitor at HV can not be very high, and it is chosen based on the Equations from 5.18 to 5.20 to keep the voltage ripple within a limit. Hence, the DC link capacitor is chosen to be 5 µF so that the continuous voltage ripple is kept to be around 2 %, and the LI drops the voltage by the same amount. The additional source capacitor is chosen to be 500 nF to obtain the voltage efficiency high in the range of 95 %. For HV MMC, the arm inductance and the arm resistor are chosen to be 9 mH and 5 kΩ. For the LI generation, the front and tail resistors are calculated by following the flowchart summarized in Fig. 5.19, and they are 51 Ω and 1318 Ω. The above-mentioned system parameters for the HV simulation is summarized in Table 5.6.

The MATLAB-Simulink simulation results with the above-mentioned parameters are shown

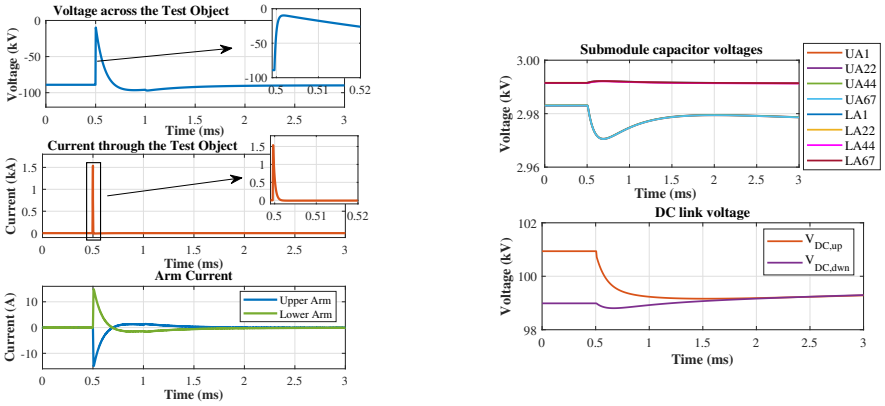
Tabel 5.6: System Parameters of the HV Simulation Model

No.	Description	Label	Value
1.	DC link Voltage	V_{DC}	200 kV
2.	Output Voltage	V_a	100 kV
3.	Number of Submodules	N	67
4.	Modulation Index	m_a	0.9
5.	Submodule Capacitance	C_s	75 µF
6.	Arm Resistor	R_a	5 kΩ
7.	Arm Inductor	L_a	9 mH
6.	Load Capacitor	C_{load}	10 nF
8.	Coupling Capacitor	C_b	100 nF
9.	DC link Capacitor	C_{DC}	5 µF
10.	Source Capacitor	C_{se}	100 nF
11.	Front Resistor	R_f	51 Ω
12.	Tail Resistor	R_h	1318 Ω

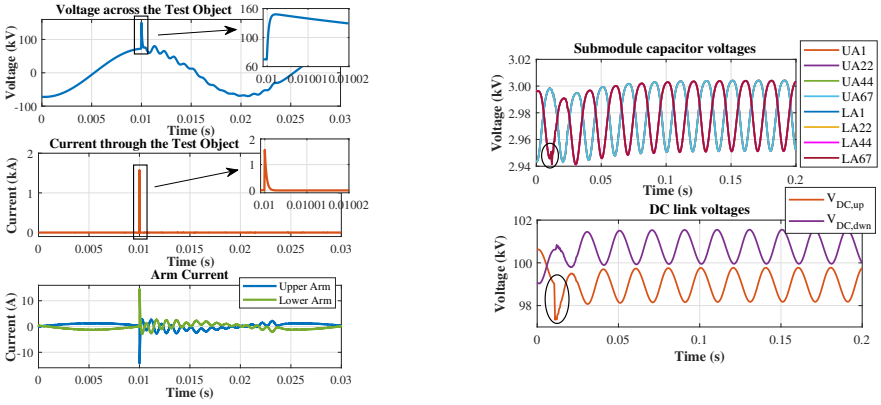
in Fig. 5.25 to Fig. 5.30 with positive and negative impulse generation. These figures include information about the output voltage, output current, arm currents, submodule capacitor voltages from the selected submodules (UA1, UA22, UA44, UA67, LA1, LA22, LA44, and LA67), and the voltage across the DC link capacitor voltage. It is important to highlight that the choice of arm resistor is sufficient, and it limits the transient arm current to 13 A. Most semiconductor devices can handle a pulse current of 2-3 times higher than its rated values as discussed in first section of this chapter. Since the arm currents are limited during the superposition, their effect on the submodule capacitor voltages is limited for all wave shapes. However, the coupling capacitor and the tail resistor add load to the MMC and draw significant arm current, resulting in a kW level of losses. This can be reduced by reducing the load or coupling capacitor to reduce steady-state current. Additionally, the submodule capacitor voltages are better balanced with DC and unipolar waveform with 67 submodules than 2 submodules. The generated LI has rise and fall time of 1.2 µs and 50 µs since ideal switches and resistors are used. The obtained voltage efficiency is 77.2 %, which is the typical efficiency value with the Marx generator circuit.



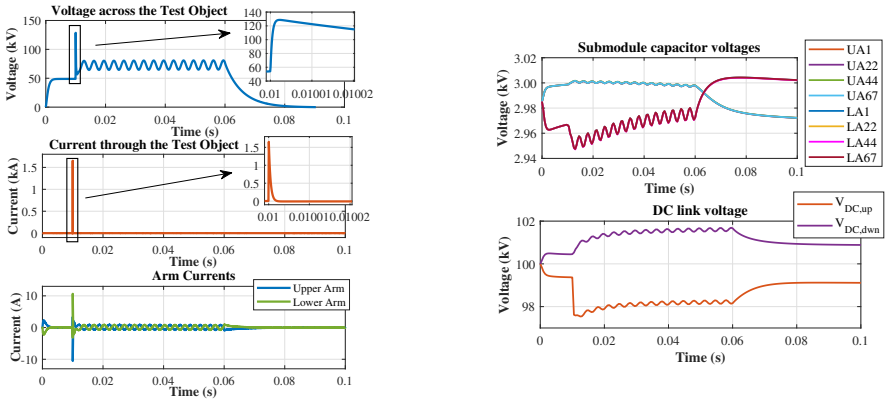
Figuur 5.25: Positive LI superimposed on positive peak of 50 Hz sinusoidal waveform.



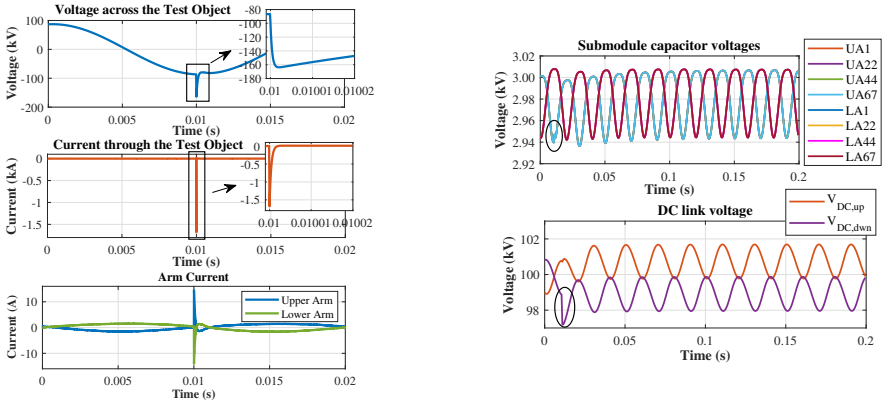
Figuur 5.26: Positive LI superimposed on negative DC waveform.



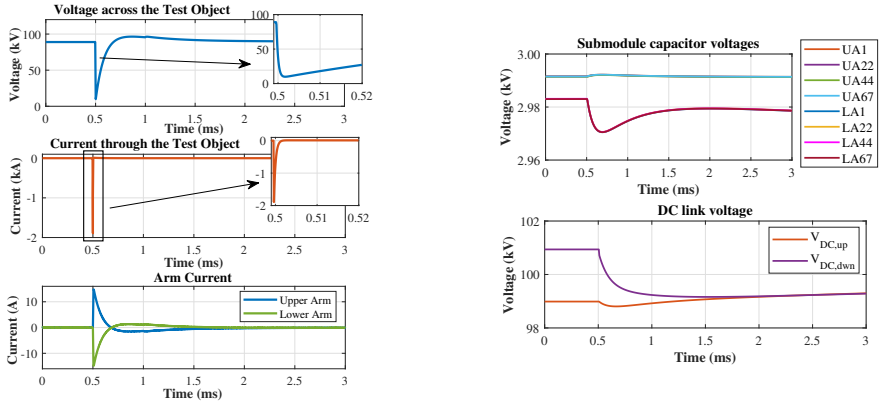
Figuur 5.27: Positive LI superimposed on 50 Hz sinusoidal and higher harmonics waveform.



Figuur 5.28: Positive LI superimposed on unipolar complex waveform.



Figuur 5.29: Negative LI superimposed on negative peak of 50 Hz sinusoidal waveform.



Figuur 5.30: Negative LI superimposed on positive DC waveform.

5.6. CONCLUSIONS FOR STEEP PULSE GENERATION

This chapter begins with summarizing challenges for generating steep impulses from the MMC-based HV AWG. Among all the challenges described in Section 5.2, the pulse current capability is crucial in the determining size and cost of the MMC design. Hence, it is investigated experimentally to find the most suitable SM device technology which can satisfy requirement for generating steep impulses like LI that demands a high peak current for a relatively short time. The first comparison is made among Non-Punch Through (NPT) Si IGBT, Field Stop (FS) Si IGBT, Si MOSFET, and SiC MOSFETs with roughly the same current rating of 40 A. It is found that the Si MOSFET gives the fastest rise time of 0.42 µs and the NPT IGBT gives the highest current amplification factor of almost 12 times greater than its own rated current. However, 3rd Generation SiC MOSFET combines Si MOSFET and NPT IGBT capabilities to generate a fast rise time and high peak pulse current. Additionally, the FS IGBT is compared with the SiC MOSFET. The SiC MOSFET performs better in peak current capability and the obtained rise time. All in all, the research results and the stringent HV AWG requirements for LI show that the application requires a relatively complex switch implementation with far superior current capability than during normal operation. Therefore, a parallel connection of several TO-packaged devices is necessary to generate LI from MMC-based HV AWG. Parallel connection will increase the complexity of the MMC-based HV AWG even further. Hence, a more practical approach is chosen where the MMC-based HV AWG will generate steep impulse waveform up to 100 µs, which includes SI waveform. However, for waveforms which are steeper than 100 µs, this chapter introduces a new hybrid configuration combining MMC and the Marx generator.

Of the three proposed configurations, the chosen integrated hybrid circuit is studied analytically with respect to the Marx generator circuit, from the MMC side, and when they are coupled together. Interestingly, the finite values of the MMC arm inductor and arm resistor affect the Marx generator circuit and influence impulse formation by adding a third exponential function. This influence of the MMC circuit is significant when the time constant of rise time or tail time is comparable to that of the MMC circuit. This chapter provides an exhaustive summary of how to choose the front resistor and tail resistor and its limitation of impulse formation. All discussed design guidelines are verified with a scaled-down hardware prototype and HV simulation results with full-scale voltage. It demonstrates that the designed system works well, giving a time-controllable LI waveform superimposed on different arbitrary wave shapes without the MMC being affected by the impulse formation. For the full-scale prototype, a multi-stage Marx generator will be needed to fulfill the voltage magnitude of LI and it will be critical to coordinate the control of MMC and Marx generator.

6

HARDWARE DESIGN OF HV AWG

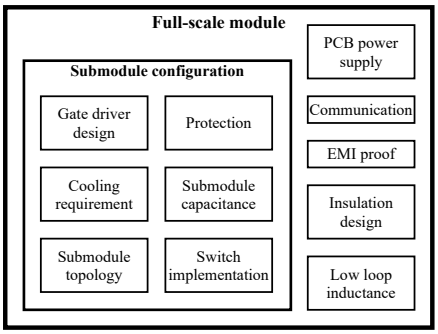
This chapter demonstrates a hardware implementation of a Medium Voltage (MV) Submodule (SM) to be used in a Modular Multilevel Converter (MMC)-based High Voltage (HV) Arbitrary Wave shape Generator (AWG). The MV SM is scalable with its own onboard Auxiliary Power Supply (APS), and it is constructed by connecting 3 Full-Bridge SMs in series from the commercially available component. The designed MV SM can be operated for a wide voltage range of 0.8 kV *to* 2.7 kV *to incorporate different test objects ranging from HV insulation material to MV equipment and generate wide output range of* 0.12 kV *to* 1.2 kV. *Considering the hardware non-idealities in the APS, gate driver, and switches, the series operation of three SMs is ensured using an arm energy controller. Based on the current-based model of APS, SM capacitance design criteria are updated for variable frequency output waveform, and the minimum DC-link voltage is calculated for the proper start-up of this scalable MMC module. Apart from the variable voltage per SM, the HV AWG application poses different conditions, such as a low value of SM capacitance value and the HV DC sources with a current rating of a few tens of milliamperes. Hence, this chapter proposes exclusive design guidelines for the proper start-up, steady-state and shut-down operation of the MMC-based AWG. Additionally, this chapter dives deeper analytically into the soft start-up algorithm to understand its working principle and to design the average charging current within the limit for any number of submodules of the arm. In the end, their performance is showcased with a single MV SM per arm, operating at a different voltage (*0.8 kV *to* 2.7 kV*) and frequency levels (*1 Hz *to* 600 Hz*) and generating different wave shapes, such as triangular, sinusoidal with different harmonics and pulse waveforms. Additionally, the Fault Ride Through (FRT) capability is verified for the MMC-based HV AWG.*

This chapter is based on following research article:

- D. A. Ganeshpure, T. B. Soeiro, M. Gagic, M. G. Niasar, P. Bauer and P. Vaessen, "Demonstration of Scalable Series-Connected Submodule of Modular-Multilevel-Converter- Based Arbitrary Wave Shape Generator Used for High-Voltage Testing From Off-the-Shelf Component,ïn IEEE Open Journal of the Industrial Electronics Society, vol. 4, pp. 371-386, 2023

6.1. INTRODUCTION TO HARDWARE DESIGN

This section summarizes challenges concerning realizing the full-scale prototype that can deliver a peak voltage of 100 kV with a Fig. 6.1. As discussed in Chapter 3, switches are the centrepiece in determining the voltage rating of the submodule. With the suggested solution of selecting SiC MOSFETs, the protection design becomes more challenging [129]. Apart from that, the auxiliary power supply design is critical for the scalability of the SM design. Generally, this auxiliary power is obtained from the submodule capacitance [130]. However, the large range of output voltage ratings of the MMC requires a variable DC link voltage. It is more advantageous to change the DC link voltage instead of reducing the number of levels, affecting the harmonic performance. As per the HV test requirements in Chapter 2, the output voltage needs to vary between 10 kV to 100 kV, which needs the DC link voltage to vary from 20 kV to 200 kV for a constant modulation index in MMC implemented with Half-Bridge (HB) SM topology. This is especially an issue for the onboard APS. Because the APS needs to convert a wide range of voltage to 12 V, 15 V, or 24 V.



Figuur 6.1: Challenging elements in the full-scale submodule.

Additionally, the PCB design for the submodule has other challenges of insulation design, cooling system design, and low loop and stray inductance [131]. Apart from the challenges within the submodule, a MMC-based HV AWG needs two full-rated DC voltage sources as the input or one full-rated DC source with two capacitors to make a midpoint connection for bipolar waveforms. As explained earlier, the dielectric tests do not require high currents. Hence, the current rating of available HV DC sources is low, in the approximate range of tens of milliamperes. This condition gives additional challenges in the start-up procedure of the MMC-based HV AWG.

6.2. MV SM DESIGN DETAILS

Two essential constraints which dictate the MV submodule design are available switches and the APS, and their choices are discussed below to create the MV SM structure.

Tabel 6.1: Switches Considered

Switches	Blocking Voltage	Continuous Current Id @ 25 °C
G2R120MT33J	3300	35 A
G3R450MT17J	1700	9 A
G3R350MT12J	1200	11 A

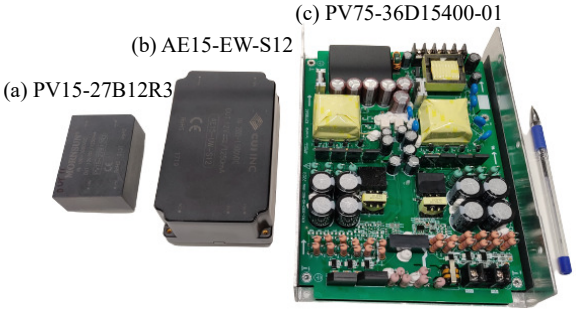
6.2.1. SWITCHES

A very high switching frequency is critical to generate accurate voltage waveforms from MMC-based HV AWG. Hence, Silicon Carbide (SiC) MOSFET is an ideal choice over Si-based MOSFETs, or IGBTs [99]. Though CREE-Wolfspeed has developed a pre-developed version of 6.5 kV, 10 kV, and 15 kV SiC MOSFETs [80], they are not commercially available as of the writing of this thesis. Some interesting commercially available SiC MOSFETs are summarized in Table 6.1, which are more cost-effective solutions compared to MV SiC MOSFETs even when they become available in the future. The highest voltage blocking capability of these commercially available SiC MOSFETs is 3.3 kV. The TO-263-7 package is chosen considering the advantages of the Surface Mount Technology, such as high-density packaging and lower parasitics. SiC MOSFETs with 1.2 kV and 1.7 kV are available for a wide current range, and the devices in Table 6.1 are chosen based on the current required for this application.

6.2.2. AUXILIARY POWER SUPPLY

For the HV application, drawing the auxiliary power for the PCB from the onboard SM capacitance is expedient. Otherwise, the APS of the topmost SM will need isolation from the total DC link voltage. This limits the output voltage as discussed in [50][53] and makes the converter design non-scalable. Hence, the implementation of APS becomes critical, especially when the power supply needs to convert a wide range of SM voltage to a relatively small voltage of 12 V. For this requirement of APS, many converter topologies are studied in the literature, such as flyback [132], Input Series Output Parallel (ISOP) [133], or other variants [134][135]. As discussed in many of these publications, implementing such an APS is challenging due to isolation requirements, series operation of switches, etc. Since the APS of the SM impacts critical factors such as reliability, safety, and cost-effectiveness, it has been decided to go with the commercially available solutions for the MMC-based HV AWG.

Two isolated DC-to-DC converters are found that satisfy the application criteria commercially. The first converter named PV15-27B12R3 from Mornsun Power has input voltage range of 0.1 kV to 1 kV and it step-downs it to 12 V. The other converter named AE15-EW-S12 from CUI Inc has a wider input range from 0.2 kV to 1.5 kV. Additionally, Mornsun is developing a converter with an even wider input range converter from 0.25 kV to 3.3 kV. It is called PV75-36D15400-01, and a sample of this product is available for research. The photos of all three auxiliary power supplies are shown in Fig. 6.2, and their description is compared in Table 6.2.



Figuur 6.2: Commercially available auxiliary power supplies.

Tabel 6.2: Details of Commercially Available Auxiliary Power Supplies

	Manufacturer	Power	Efficiency (Typ.)
0.1 kV to 1 kV PV15-27B12R3	Mornsun Power	15 W	81 %
0.2 kV to 1.5 kV AE15-UW-S12	CUI Inc	15 W	71 %
0.25 kV to 3.3 kV PV75-36D15400-01	Mornsun Power	32 W	70 %

6.2.3. STRUCTURE OF MV SUBMODULE

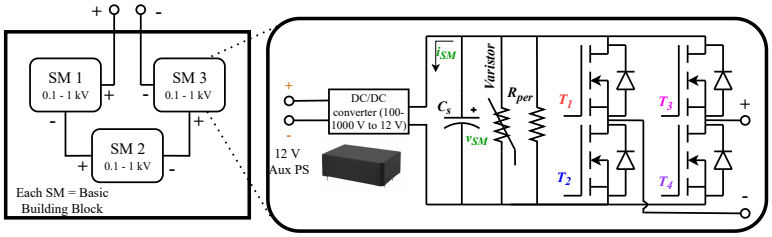
Based on the current availability of the switches and the APS, the highest voltage per SM can be 1.5 kV with 3.3 kV SiC MOSFETs switches and AE15-UW-S12 APS. However, this low voltage per SM creates a challenge for the controller and communication since it means one needs a minimum of 134 SMs per arm without considering redundancy. As discussed in [99], the minimum of 67 SMs with 3 kV can be an optimum solution. The 3 kV switch can be realized either using series combination of three 1.7 kV or series combination of two 3.3 kV. Since the current rating requirement of the HV testing application is quite less than 35 A, stray capacitances in the 3.3 kV switches, will not give optimum switching performance at the current level such as 1 A. Since the high-switching frequency is crucial to the application, low current-rated 1.7 kV are chosen, which is also much cheaper solution compared to 3.3 kV switches. Though it is possible to connect 1.7 kV switches in series to create a 3 kV switch, the APS is not available commercially, which converts 3 kV to low voltage. Even if the PV75-36D15400-01 APS gets available commercially, the APS is much larger and will consume more space than the SM capacitance on the MMC module. Hence, it is not an optimal solution for the application. Hence, a 3 kV MV SM is realized using three 1 kV SMs connected in series as shown in Fig. 6.3.

Fig. 6.3(b) is a zoomed picture of a single SM that can operate between 0.1 kV to 1 kV rating, and it is called the basic fundamental block in the further part of the thesis. The basic fundamental block is realized using a 1.7 kV rated SiC MOSFET and PV15-27B12R3 APS. The structure of the single SM in Fig. 6.3(b) consists of a Full-Bridge (FB) SM topology, SM capacitance (C_s), parallel resistor (R_{per}), PV15-27B12R3 APS, and varistor. Note

Tabel 6.3: Comparison of Different Submodule Topology with Constant Voltage per Submodule (1 kV) and Output Voltage (100 kV)

Parameters	MMC with HB	MMC with FB	MMC with Hybrid	CHB with FB
1. Switch states	0, Vc	0, Vc, -Vc	0, Vc, -Vc	0, Vc, -Vc
2. DC link voltage	200 kV	100 kV	100 kV	-
3. No of SM (N)	N=Vdc/Vc =200	N=3Vdc/2Vc =150	N_HB=100 N_FB=50, N=150	N=Vout/Vc =100
4. Total switches	4N = 800	8N=1200	16N/3=800	4N=400
5. Arm Current	io/2	io/2	io/2	io

that the isolation capability of this APS is 4 kV, which ensures that the proposed MV SM design can be stacked on each other to build a 100 kV MMC-based HV AWG. The FB topology is chosen for the HV AWG application since it gives more flexibility to control the SM capacitance voltages and offers the advantage of obtaining the peak output voltage the same as the DC link voltage compared to HB topology [136]. It means that the DC link voltage requirement is reduced by half, which is a great advantage, especially for this HV application. The FB MMC requires twice the number of submodules compared to the HB MMC. However, it is possible to use both HB and FB in the same arm to keep the number of submodules same as HB, while the DC-link voltage is reduced by half. The FB topology share is shown in Table 6.3.



(a) 3 kV MV SM (b) 0.1- 1 kV SM Structure

Figuur 6.3: MV SM structure.

The last column of Table 6.3 compares CHB to MMC with different SM topologies. For the same output voltage and blocking voltage per SM, CHB with FB requires half of the SMs per arm, with the current requirement to be doubled. However, considering the challenges with scaling the design to higher voltage levels, FB SM topology is selected with MMC. However, in this thesis, the FB is operated as HB to demonstrate this MV SM design. Hence, when all SMs in series connection are counted as N in each arm, the number of levels obtained in the output voltage will be $2(N/3)+1$ since $N/3$ SMs are operated as one MV SM.

6.3. HARDWARE AND CONTROL CHALLENGES

There were four significant challenges faced in realizing this scalable MV SM design. The first challenge is creating equal voltage sharing among the series operation of 3 SMs due to the hardware's non-idealities. The second is about the start-up issues faced due to the installed APS and the low current rating HV DC source. The third is about the SM capacitance design considering the effect of the installed APS. The last discussed part is about the protection design for the HV AWG in case of any fault within or outside the converter.

6.3.1. HARDWARE NON-IDEALITIES

There are three SMs connected in series, and they must share the voltage equally, which can be disturbed by either of the following four factors. They are discussed in detail with possible solutions to ensure equal voltage sharing.

GATE PULSES

Though gate pulses of all SMs are controlled synchronously, 3 SMs connected in series can have different time delays. The delay can be attributed to the controller, the communication hardware, and/or to the gate driver design. A real-time simulator from OPAL-RT OP5600 is used as a controller and sends synchronized gate pulse signals. Additionally, the fibre optic connection keeps the delay to a few nanoseconds. All four switches are controlled independently using an ACPL-344JT gate driver IC with a typical value of the propagation delay as 100 ns.

SWITCHES

Switches in different SMs can have different parasitic capacitances that take different times to turn on and off even though they receive the gate pulses simultaneously.

AUXILIARY POWER SUPPLY (APS)

This isolated DC-to-DC converter is connected parallel to the SM capacitance. It can greatly influence the voltage sharing of the series connection. The current consumption by the APS (i_{SM}) can be calculated from the following Equation (6.1):

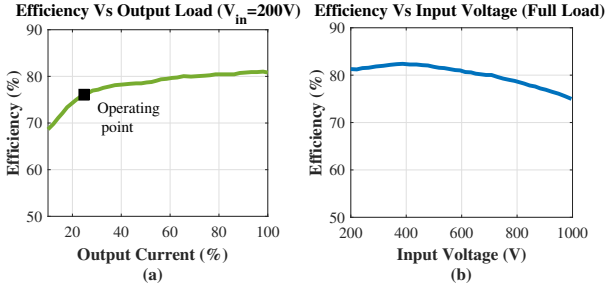
$$P_{APS} = v_{SM} i_{SM} \eta_{APS} \tag{6.1}$$

Here, P_{APS} is the power consumption of APS for that SM PCB board, and v_{SM} is the voltage across the SM capacitance. Additionally, η_{APS} is the efficiency of the APS. The multiple APSs connected to three SMs in series can have different η_{APS} and different P_{APS}. Hence, even if they start with the same initial voltage $v_{SM,initial}$, eventually, they will start deviating from the $v_{SM,initial}$ since the i_{SM} will be different which will deplete the SM voltage differently. Since i_{SM} increases as v_{SM} reduces, there is a positive feedback loop. It means that the SM which has lower SM voltage consumes higher i_{SM}, leading to a faster reduction in the v_{SM}. Hence, without any control, the unequal voltage sharing will worsen faster.

Fig. 6.4 shows the efficiency of the converter as per the P_{APS} and v_{SM}. The load of the onboard APS is the PCB consumption around 3.6 W. This amount is 24 % of the 15 W,

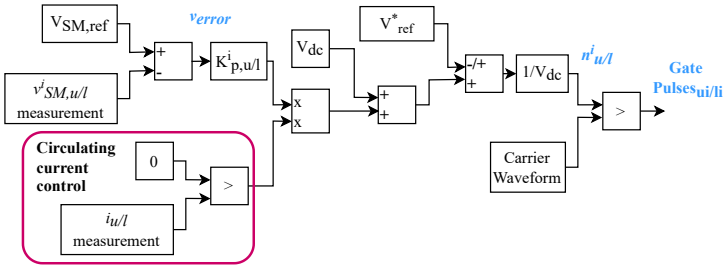
which is the full power capability of the APS. Fig. 6.4(a) highlights the operating point as per the percentage of full load, and it is clear that the efficiency is less than 80 %. As per the voltage graph in Fig. 6.4(b), the highest efficiency is achieved at the 50 % of the highest possible voltage. Lower efficiencies at higher voltages are not a problem since the current consumption will be drastically reduced, making it easier to balance the series operation.

Among the three discussed non-idealities in the hardware, the difference in the APS consumption (i_{SM}) affects the equal voltage sharing the most since the APS consumption can be different dynamically and during steady state since the v_{SM} vary as per the output voltage to be produced. It is possible to use a parallel resistor (R_{per}) to assist in equal voltage sharing among series-connected SMs. However, the value of this R_{per} needs to be tuned as per the APS consumption. i_{SM}. Since this consumption varies by so many factors, as mentioned above, it is tedious to tune R_{per} for different cases. Additionally, it is more beneficial to utilize the control rather than the power connection for safety and reliability. Hence, the individual SM-based arm energy controller is proposed to ensure equal voltage sharing among series-connected SMs.



Figuur 6.4: APS - PV15-27B12R3 (a) Efficiency vs Output Load (b) Efficiency vs Input Voltage.

A simple proportional controller is designed for equal voltage sharing during the steady state operation, and its implementation for a single SM is shown in Fig. 6.5. All SM capacitor voltages are measured and compared with the reference value. The output of the proportional controller is added or subtracted from the DC voltage. The decision of addition or subtraction is made based on the arm's current direction. Since the average circulating current in the steady-state operation of the MMC-based HV AWG is zero, the effect of the circulating current is taken into the arm energy controller by changing the sign. The sign of the arm current decides whether the controller output is added or subtracted from the DC link voltage. This variation in the DC link voltage changes the reference waveform, which changes, in turn, the gate pulses. This adjustment counteracts the APS current consumption and other hardware non-idealities, resulting in equal voltage sharing among the SMs. As discussed in [99], Phase Shift Carrier (PSC) modulation technique is used to generate gate pulses from the reference waveform with a switching frequency as a non-integer multiple of the fundamental frequency.

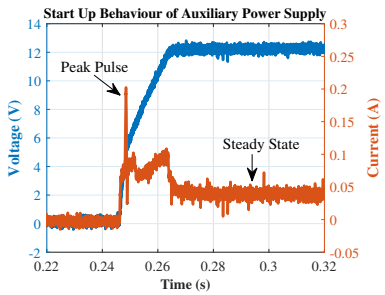


Figuur 6.5: Arm energy controller per SM.

6.3.2. START-UP PROCEDURE

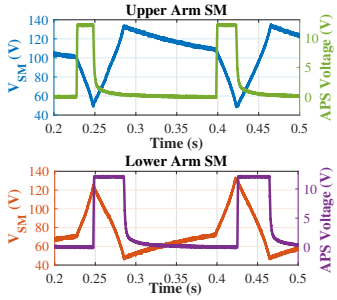
The MMC-based HV AWG needs a black-start capability since SMs do not have auxiliary power until the voltage per SM reaches roughly 100 V. Using the anti-parallel diodes of the MOSFETs, it is possible to charge the SM capacitor voltages to 100 V. However, the series operation of APS has the following major issues:

1. The voltage at which different APS turns on is quite wide and varies between 60 V to 85 V [137].
2. The inrush current drawn by the APS can be as high as 200 mA when the input voltage is 100 V and SM capacitance (C_s) is 75 µF, as shown in Fig. 6.6.
3. Different APS have a different delay to start-up even when the SM capacitor voltage is the same in all SMs.

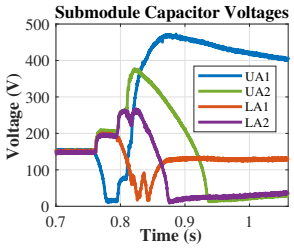


Figuur 6.6: Start up behaviour of auxiliary power supply with V_{SM}=100 V and C_s=75 µF.

These issues combined create problems in the start-up as shown in Fig. 6.7 for one SM in each arm and two SMs connected in series in each arm with SM capacitance of 75 µF and $v_{SM,initial}$ of roughly 100 V. Fig. 6.7(a) shows the SM capacitor voltage and the output of the APS for the Upper Arm (UA) and Lower Arm (LA). The APS from UA turns on at 0.23 s. However, it experiences a considerable voltage drop due to the in-rush current of the APS. Hence, when LA gets its auxiliary power, the APS from UA turns off. A similar problem occurs for two SMs in each arm, as shown in Fig. 6.7(b) with the four SM capacitor voltages. It is important to point out that the second SM from UA (UA2) gets its auxiliary



(a) 1 SMs each Arm



(b) 2 SMs each Arm

Figuur 6.7: Issue with the auxiliary power supply at C_s=75 µF.

power last, which is 50 ms after the first SM gets its auxiliary power supply. This time difference in receiving the auxiliary power for different SMs can be different depending on many system parameters such as SM capacitance value, the current capability of the DC source, etc. The solution to this problem is multi-fold. First of all, it needs to have a proper start-up procedure. Secondly, the choice of SM capacitance and initial SM capacitor voltage ($v_{SM,initial}$) needs to be done properly considering all the above-mentioned non-idealities in the APS. The following section addresses all these challenges to ensure a proper start-up and steady-state operation of the MMC-based HV AWG.

6

START-UP GUIDELINE

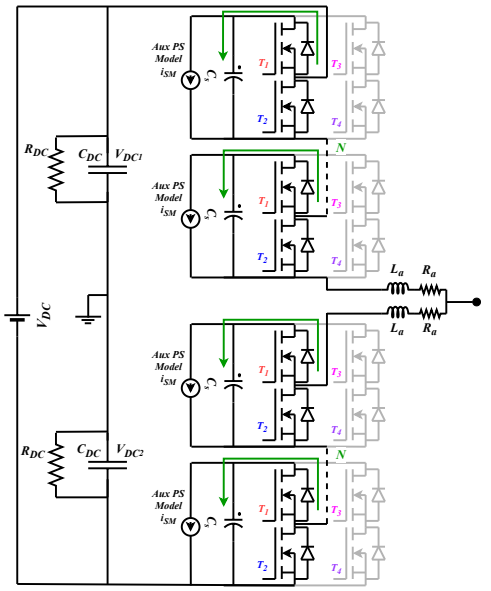
To avoid the issues shown in Fig. 6.7, the following guidelines are important to follow:

- To directly apply the DC link voltage with current controlled mode to charge the SMs to a minimum voltage of 100 V fast and simultaneously.
- As discussed earlier, most HV DC sources can supply only up to a few tens of mA. Hence, it is important to implement a soft start-up to charge the SM capacitor voltages from $V_{DC}/2N$ to V_{DC}/N without requiring large inrush current.
- The SM which gets the APS first is kept inserted, so the SM capacitor voltage is maintained even after the transient and steady current drawn by the APS.

To be on the safe side, gate pulses as per particular reference waveform are inserted after 5 ms to 20 ms after all SMs receive auxiliary power. This methodology of insertion of SMs ensures that the circulating current maintains the SM capacitor voltage while the APS is draining the current (i_{SM}). The path for charging the SMs is shown with a schematic in Fig. 6.8. Also, it limits the SM capacitor voltages whose APSs are not turned on, unlike in Fig. 6.7(b).

SOFT START-UP IMPLEMENTATION

The SM capacitor voltages are charged to $V_{DC}/2N$ with current limiting mode on the HV DC source where the anti-parallel diodes are conducting the charging current. It is assumed that the APSs of all SMs are turned on before implementing the soft start-up algorithm, and this stage is considered Stage 0. At the instant of soft start-up algorithms

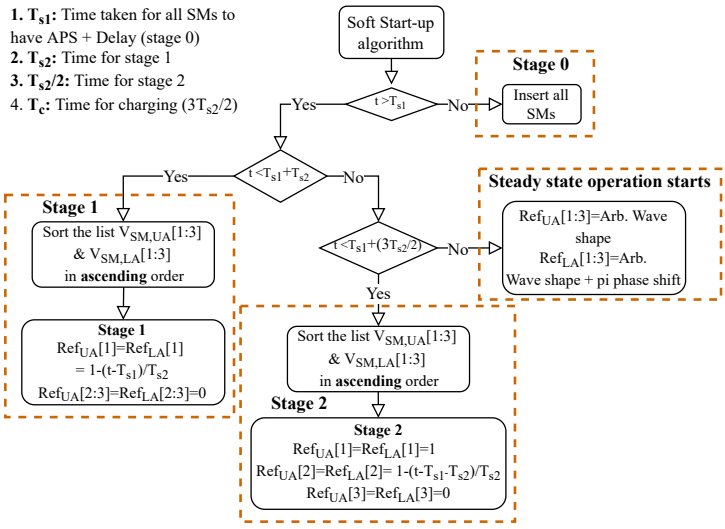


Figuur 6.8: Schematic of MMC during the start-up.

6

begins (T_{s1}), all N SMs are inserted. The soft start-up algorithm charges the SM capacitor voltages to V_{DC}/N by changing the inserted SMs per arm from N to N/2, as described in [138]. This soft start-up algorithm differs from using a PI controller to keep the charging current constant in [139][140]. However, the former start-up algorithm is chosen, considering it does not produce any output voltage or current during the soft start-up. It is ideal to apply the desired dielectric voltage stress directly. The charging algorithm can be achieved in two stages for N = 3. In the first stage, two SMs from each arm are always inserted, and single SM from each arm are switching with varying duty ratios from 1 to 0 in T_{s2} duration. During this first stage, the total inserted SMs from both arms changes from six to four. In the second stage, one SM from each arm are always inserted, one SM from each arm are always bypassed and one SM from each arm are switching with varying duty ratios from 1 to 0.5 in $T_{s2}/2$ duration. During both stages, SMs are sorted to decide which one to be inserted based on the SM capacitor voltages. Hence, any variations present in the SM capacitor voltages at T_{s1} time instant are disappeared, and equal voltages are obtained among series-connected SMs when the reference waveform is being generated, which helps the arm energy controller. Fig. 6.9 shows the exact soft-start algorithm for N = 3.

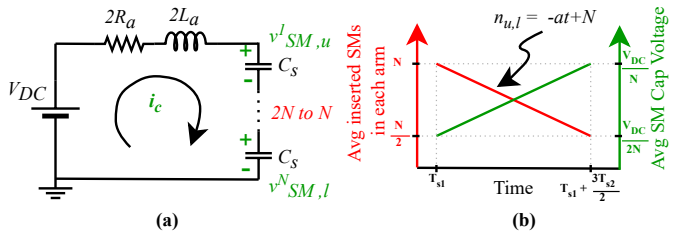
The basic working principle of this soft start-up algorithm is shown in Fig. 6.10 when N can be any number more than three. From the circulating current circuit shown in Fig. 6.10(a) [99], it is clear that the soft start-up algorithm is influenced by the passive element values such as the arm inductance, the arm resistance, and the SM capacitance. Additionally, Fig. 6.10(b) shows the overall dynamics of the SM insertion in both arms and how the SM capacitor voltages are charged from $V_{DC}/2N$ to V_{DC}/N. The dynamic of the SM insertion is linear with a negative slope of 'a', and it can be represented in (6.2),



Figuur 6.9: Soft start-up algorithm for N = 3.

assuming $T_{s1} = 0$. Another equation can represent the same equation, where the integer part of $n_{u,l}$ is 'n' and its decimal part is 'd'. The desired rise in the SM capacitor voltages for three submodules is obtained in two stages, as explained above. In the first stage, n equals 2, and d varies from 1 to 0. In the second stage, n is reduced to 1, and d varies from 1 to 0.5, where $n_{u,l}$ is reached to 1.5. More stages would be needed to reduce the inserted submodules from N to N/2 for a higher number of submodules.

$$n_{u,l} = -at + N = n + d \tag{6.2}$$



Figuur 6.10: Working principle of soft start-up algorithm (a) Circulating current circuit (b) Insertion index.

Fig. 6.11 shows the detailed switching behavior of all SMs from both arms with variable duty and how the charging current is generated. Here, the switching frequency is T_{sw}, and the duty ratio 'd' is the same as the decimal part mentioned above. As soon as the inserted SM is reduced from 2N to $2N-2$, a positive voltage is built across the arm inductance and arm resistance, resulting in a positive charging current i_{ch}. When the $n_{u,l}$ reaches to N/2, then the algorithm stops. The dynamics behind this soft start-up al-

gorithm can be understood analytically with equations shown below from (6.3) to (6.7). First, it is important to find the relation between the average instantaneous voltage of SM capacitor voltage and DC-link voltage, and it is shown in (6.3). For any integer value of $n_{u,l}$ (n), it is possible to write two equations for charging current and for discharging current, as shown in (6.4) and (6.5) respectively. Since the dynamics of charging current are linear, it is possible to derive the peak charging current using (6.6), and it is simplified in (6.7).

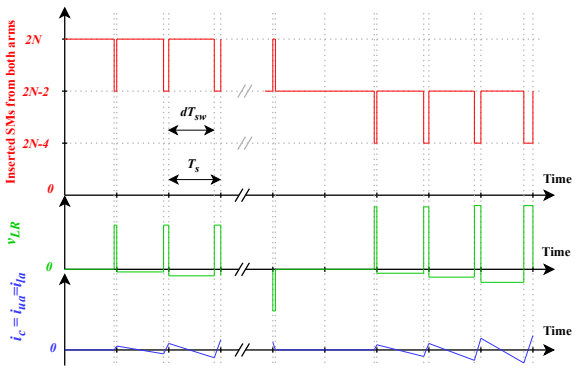
$$V_{SM,avg,t} = \frac{V_{DC}}{2n_{u,l}} = \frac{V_{DC}}{2n+2d} \tag{6.3}$$

$$2R_a i_{ch} + 2L_a \frac{\mathrm{d}i_{ch}}{\mathrm{d}t} = V_{DC} - (2n+2)V_{SM,avg} \tag{6.4}$$

$$2R_a i_{ch} + 2L_a \frac{\mathrm{d}i_{ch}}{\mathrm{d}t} = V_{DC} - 2nV_{SM,avg} \tag{6.5}$$

$$2R_a I_{pp} + 2L_a \frac{I_{pp}}{(1-d)T_s} = V_{DC} - 2n\frac{V_{DC}}{2n+2d} \tag{6.6}$$

$$I_{pp} = \frac{d(1-d)T_s V_{DC}}{4(n+d)(L_a + R_a(1-d)T_s)} \tag{6.7}$$



Figuur 6.11: Waveforms during the soft start-up.

The maximum peak current for this charging can be derived when the integer part (n) is the lowest, and the minimum value of n can be calculated for any number of submodules as shown in (6.9). Additionally, it is possible to derive the maximum value of I_{pp} with respect to the decimal part (d), and its value is derived as shown in (6.10). Hence, the maximum value of I_{pp} can be calculated from (6.8). Note that this instantaneous peak current is supplied by the DC-link capacitors (C_{dc}), and the average charging current is provided by the DC source. Calculating the average current drawn by the DC source is possible, assuming the energy conservation principle. Additionally, when the capacitors are charged through a resistor, it is well known that the energy supplied by the DC source is split equally between the resistor and capacitor. With this assumption, it is possible to

calculate the average charging current (I_{ch}) using the equation shown in (6.11). Here, T_c is the time to charge the SM capacitors. It is related to the slope of the insertion index as $T_c = a/N$. Depending upon the current capability of the HV DC source, the time for charging should be calculated from (6.12).

$$I_{ppm} = \frac{d_m(1-d_m)T_s V_{DC}}{4(n_m+d_m)(L_a+R_a(1-d_m)T_s)} \tag{6.8}$$

$$n_m = floor(\frac{N-1}{2}) \tag{6.9}$$

$$d_m = \frac{-(R_a T_s * n_m + L_a n_m + \sqrt{(L_a R_a T_s n_m^2 + L_a^2 n_m^2 + L_a R_a T_s n_m + L_a^2 n_m))}}{(-R_a T_s n_m + L_a)} \tag{6.10}$$

$$V_{DC} I_{ch} T_c = 2\frac{1}{2}(2N)C_s[(\frac{V_{DC}}{N})^2 - (\frac{V_{DC}}{2N})^2] \tag{6.11}$$

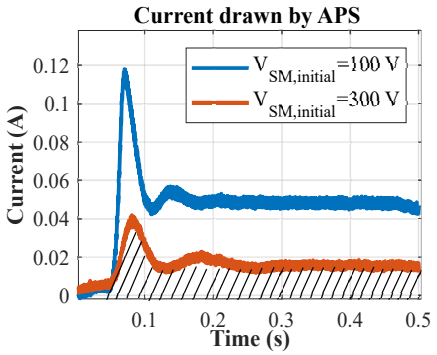
$$T_c = \frac{2NC_s}{V_{DC} I_{ch}}[(\frac{V_{DC}}{N})^2 - (\frac{V_{DC}}{2N})^2] \tag{6.12}$$

6.3.3. SM CAPACITANCE CHOICE

SM capacitance value is one of the most critical parameters in determining voltage efficiency, size, and cost of the MMC-based HV AWG. All advantages offered by MMC come with the challenge of balancing SM capacitance voltages. Generally, the SM capacitance value is designed according to the total energy stored in all SM capacitance per MVA rating of the converter or to keep the capacitor voltage ripple within a limit. In [99], the capacitor voltage ripple is derived for HV AWG application, and it has been proven that 10 μF is enough to generate accurate voltages. However, that design guideline did not include the series operation of SMs or the effect of the onboard APS. Additionally, the start-up issues shown in Section 6.3.1 can be solved with the right design of the SM capacitance value and the initial voltage of the SM. These issues are not seen in typical HV MMC hardware since the SM capacitance lies in mF range. As described in [141], the SM capacitance takes 50 % of the total volume of the SM. Hence, for this HV AWG application, it is not wise to increase the SM capacitance to mF range since it can drastically increase the size and cost of the MMC-based HV AWG. Additionally, a larger SM capacitance value requires a longer time to charge the SM to $v_{SM,initial}$, which is especially problematic since most HV DC sources can not provide current more than a few tens of mA.

The APS current consumption affects both the start-up and steady-state operation of the MMC-based HV AWG if the SM capacitance value is not large enough. During the start-up, APS draws an inrush current of 200 mA, which creates the first voltage drop ($\Delta v_{SM,1}$) in the SM capacitor voltage. Secondly, the SM capacitor voltage needs to be maintained until all SMs get the APS working, creating a second voltage drop of $\Delta v_{SM,2}$. Combining both voltage drops, the SM capacitor voltage should not drop less than 75 V, where the APS turns off [137]. In Fig. 6.7(a), the SM capacitor voltage drop from 100 V to 50 V in the first 20 ms and the APS turns off. This clearly shows that the $\Delta v_{SM,1}$ itself is 50 V. This

should be reduced to 12.5 V so that $\Delta v_{SM,2}$ can be 12.5 V and the SM capacitor voltage will not drop below 75 V. Since the $\Delta v_{SM,1}$ needs to be reduced from 50 V to 12.5 V, the SM capacitance value needs to be increased roughly four times from 75 µF to 310 µF as per (6.13). With the higher value of SM capacitance, the APS has a different dynamic performance, as shown in Fig. 6.12. It draws less peak current with a relatively smoother current wave shape compared to the 75 µF capacitance. Also, it is important to note that the in-rush peak current reduces as the $V_{SM,initial}$ is increased.



Figuur 6.12: SM capacitance design.

In the experiments, it has been observed that the mismatch in start-up delay of different APSs can be as high as 300 ms to 450 ms when 6 SMs are present with 310 µF capacitance and a HV DC source with limited current capability. Instead of increasing the SM capacitance further, the $V_{SM,initial}$ voltage is varied from 100 V to 300 V to find an optimum point where the total SM capacitor voltage drop is not below 75 V. Using (6.13) and (6.14), the minimum value of $V_{SM,initial}$ is calculated to be 130 V for 310 µF with 450 ms delay between first and last APS to turn-on. The integration in (6.14) is obtained from the area under the curve from Fig. 6.12.

$$i_{SM} = C_s \frac{\mathrm{d}v_{SM}}{\mathrm{d}t} \tag{6.13}$$

$$\Delta v_{SM} = \frac{1}{C_s} \int_0^{t=0.45} i_{SM}\, dt \tag{6.14}$$

Apart from the start-up, the APS consumption disturbs the charge time product during the steady state, creating a larger SM capacitor voltage ripple for lower frequency waveform. Hence, it is important to have enough SM capacitance for lower frequency waveform to keep the voltage ripple around 10 % of the average SM voltage value [82][84]. The ripple is largest when the SM capacitor voltage is lowest since the APS consumption is highest. For $V_{SM,initial}$ = 130V, the steady state SM capacitor voltage is 260 V. Hence, the I_{SM} is calculated to be 17.8 mA from (6.1), considering 78 % efficiency. Considering 10 % of 260 V, the allowed capacitor voltage ripple is 26 V. It is possible to calculate the minimum possible frequency from (6.15). The Δt in (6.15) is half of the period. The minimum possible frequency is 1.1 Hz. The MMC-based AWG can go low frequency since

there is almost negligible active power transfer to the load, and the transferred reactive power is also low, drawing only a few amperes of arm current and zero average circulating current.

$$\Delta t = \frac{\Delta V_{SM} C_s}{I_{SM}} = \frac{26 \times 310 \times 10^{-6}}{0.0178} = 0.42\,\text{s} \tag{6.15}$$

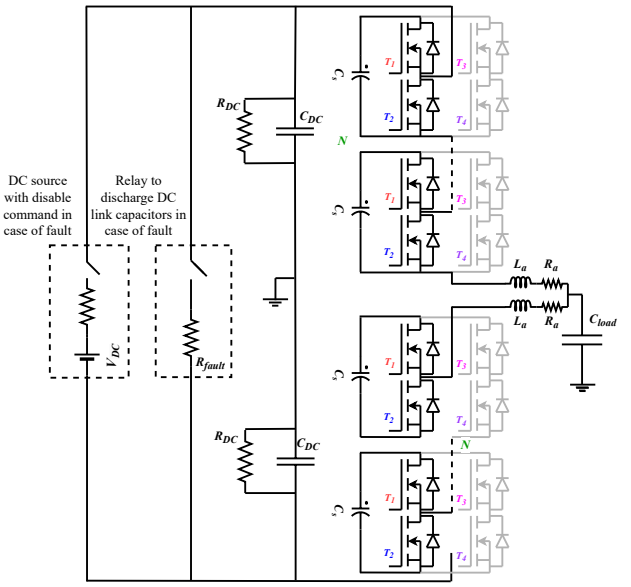
6.3.4. PROTECTION DESIGN

Apart from proper start-up, steady state, and shutdown operation of the HV AWG, it is essential to protect the converter from undesired fault scenarios. Among many possible failures in the converter, the breakdown of the inductor can create extremely severe di/dt and peak amplitude of the current in the particular arm since there is no limiting inductor. Hence, it is crucial to protect the switches and other components on the SMs from these extreme currents and voltages. The installed gate driver (ACPL-344JT) can detect the high current magnitudes and di/dt flowing through switches. Apart from that, each SM PCB has over-voltage protection. One SM among each arm has the current sensor and can detect over-current scenarios. The fault signal from the gate driver, over-voltage fault signal, and over-current fault signal are sent to an AND gate on each SM to generate a fault signal which is sent to the central controller. In case of any fault on any SM, all SMs will be disabled together to avoid any damage. The controller is implemented in the real-time simulator (OPAL-RT), and it can disable the switches as fast as 20 μs. Hence, the Fault-Ride Through (FRT) capability is not present in the implemented protection system design since the switches are blocked right after the fault occurs. Additionally, it is essential to discharge the DC link in case of a fault condition and turned-off the DC source. Hence, an HV relay is installed to discharge the DC link capacitance through the fault resistor and disable the HV power supply. This relay can be operated manually. Fig. 6.13 shows the updated schematic of MMC-based HV AWG with the implemented protection. Additionally, the overall timeline of operation of the MMC-based with a single MV SM is shown in Fig. 6.14.

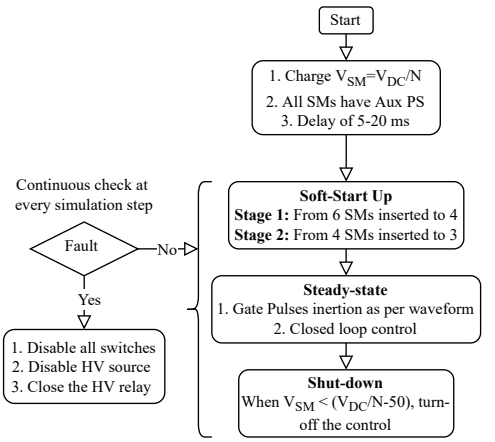
6.4. HARDWARE SETUP AND RESULTS

The design of this series-connected MV SM is verified with the experimental setup as shown in Fig. 6.15 with one MV SM in each arm. This MV SM is scalable in the sense that they can be stacked on top of each other to build the HV AWG with an output voltage rating of 100 kV. For testing a single MV SM to its maximum rating of 3 kV, the load capacitance is down-scaled from 10 nF to 680 nF to keep the same current rating. The design of the arm inductance (L_a) and arm resistance (R_a) is determined as per the design guidelines discussed above and their values are 27 mH and 150 Ω, respectively. The value of arm inductance is higher since there is only one SMs per arm in the current experimental setup, which needs higher inductance to filter the voltage harmonics. Additionally, the value of arm resistance is reduced lower than the over-damped system discussed in (3.14) to limit the losses in the lab-scale setup to 40 W.

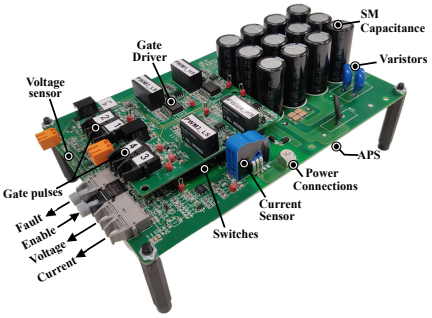
This hardware setup is controlled using the OPAL-RT simulator (OP5600). Each SM receives an enable and four gate pulse signals and transmits back the SM capacitor vol-



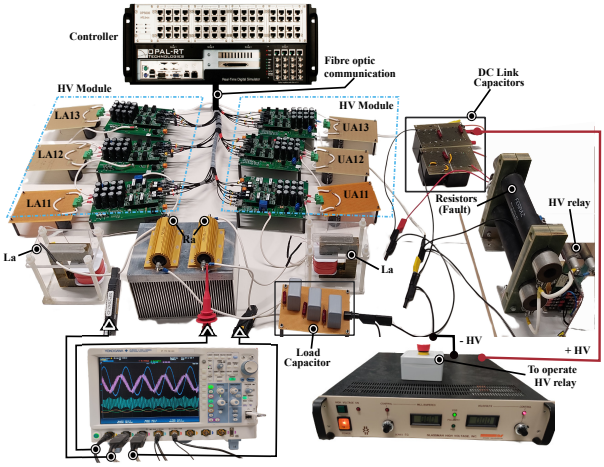
Figuur 6.13: Protection circuit of MMC-based AWG with single MV SM.



Figuur 6.14: Overview of MMC-based AWG with single MV SM operation.



(a) Basic building block



(b) MMC-based AWG with Single MV SM

Figuur 6.15: Experimental setup

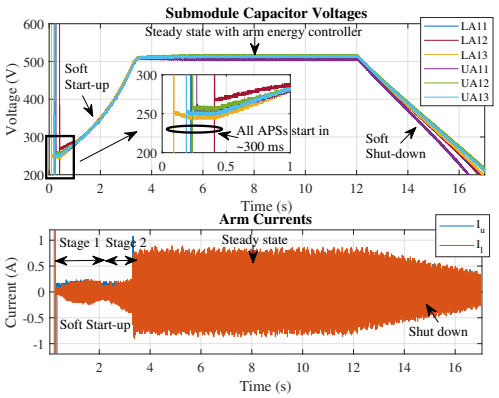
tage, fault signal, and arm current measurements via a digital voltage oscillator and fiber optics. The output voltage and arm currents are measured using the HV differential probe (CT4072) and current probes (N2782B). The above-discussed system parameters are summarized in Table 6.4. In this table, the switching frequency (F_s) is chosen as 7011 Hz or 9011 Hz for balancing the SM capacitor voltage naturally. Additionally, Fig. 6.15(a) shows the basic fundamental block of the MV SM, which is SM PCB, and Fig. 6.15(b) displays the experimental setup of HV AWG.

First, the dynamic performance of the MMC-based AWG with a single MV SM has showcased in Fig. 6.16 with 1.55 kV DC link voltage. Hence, the steady state SM capacitor voltages are properly balanced between 500 V to 520 V, which concludes that the implemented arm energy controller is working correctly. Additionally, the soft start-up algorithm discussed in Section 6.3.2 is working properly that the SM capacitor voltages are slowly rising from (V_{DC}/2N) to (V_{DC}/N) without drawing large charging current. The model developed in Section 6.3.2 is verified with the experimental results shown in Fig. 6.16. A sufficient large charging time (T_c) of 3 s is chosen so that the average current drawn from the HV DC source is limited to 80 mA which is almost the same as the experimentally ob-

Tabel 6.4: System Parameters of the MMC-based AWG with single MV SM

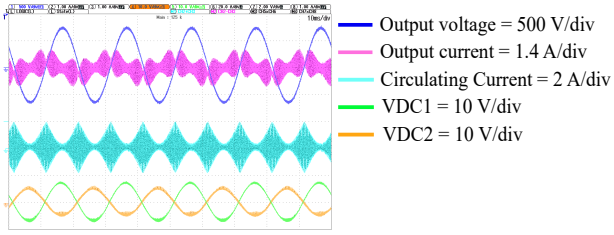
No	Description	Symbol	Values
1.	DC-link voltage	V_{DC}	0.8 kV-2.7 kV
2.	Output voltage	V_a	0.2 kV-1.2 kV
3.	Modulation index	m_a	0.3-0.9
4.	Number of SMs	N	3
5.	Switching frequency	F_s	7011 Hz/9011 Hz
6.	SM capacitance	C_s	310 μF
7.	Arm inductance	L_a	27 mH
8.	Arm resistance	R_a	150 Ω
9.	Load capacitance	C_{load}	680 nF

tained value of 78 mA. Moreover, the detailed model of maximum peak-to-peak charging current is found to be 420 mA, while the model predicted it to be 480 mA. Additionally, the zoomed picture of the start-up shows that the delay between the first APS and the last APS turning on is 300 ms. Fig. 6.17 shows the output voltage, output current, and circulating current during steady state operation at 1.555 kV with 0.9 modulation index, which generates 700 V peak sinusoidal. The higher values of steady-state arm currents are supplied by the DC link capacitors with a small voltage ripple as shown in Fig. 6.17 with green V_{DC1} and orange waveform V_{DC2}.

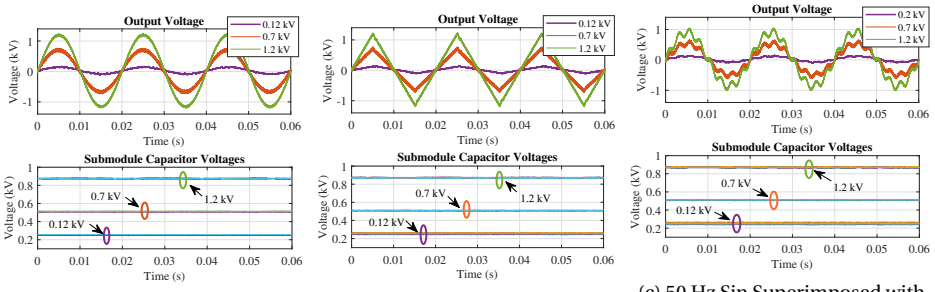


Figuur 6.16: Soft start-up and soft shut-down of the MMC-based AWG with single MV SM.

Secondly, the performance of the MMC-based AWG with a single MV SM per arm is showcased for the wide output voltage range. Though the MV SM was aimed to operate from 0.3 kV to 3 kV, the issues with lower voltage are discussed in Section 6.3 in detail, and those issues can be solved with a larger minimum voltage of 0.8 kV (3×0.267 kV). Earlier, when the minimum voltage per SM could go to as small as 0.3 kV, the MMC-based AWG with a single MV SM could have an output voltage from 0.135 kV to 1.35 kV considering a 0.9 modulation index. Since the minimum operable voltage of the MMC is elevated to 0.8 kV, the lower voltages are obtained with a 0.3 modulation index. Hence, the minimum obtained output voltage is 0.12 kV, and the performance of the MMC-

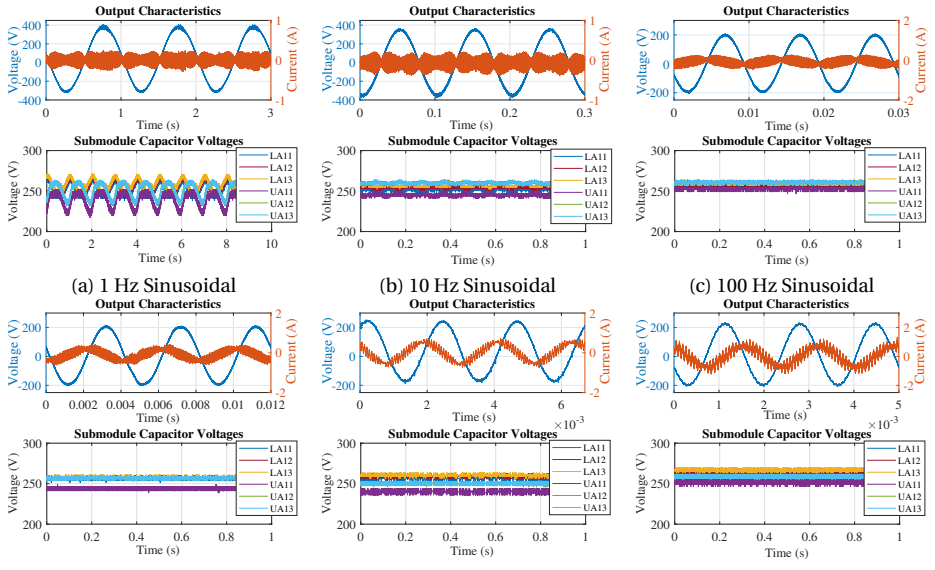


Figuur 6.17: Steady state performance the MMC-based AWG with single MV SM.



(a) 50 Hz Sinusoidal (b) 50 Hz Triangular (c) 50 Hz Sin Superimposed with 400 Hz Sin

Figuur 6.18: Experimental results with wide output voltage range.

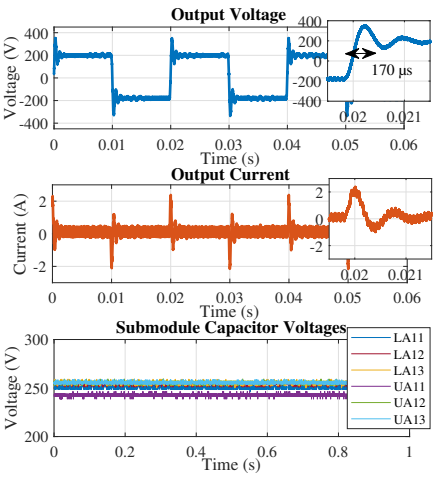


(a) 1 Hz Sinusoidal (b) 10 Hz Sinusoidal (c) 100 Hz Sinusoidal

(d) 250 Hz Sinusoidal (e) 450 Hz Sinusoidal (f) 600 Hz Sinusoidal

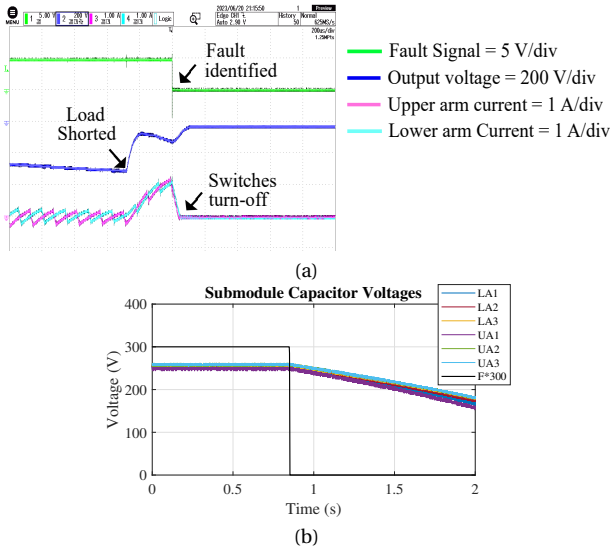
Figuur 6.19: Experimental results with wide output frequency range.

based AWG at this output voltage for different wave shapes is shown in Fig. 6.18(a) to (c). Additionally, a mid-range of 0.7 kV is chosen with 1.55 kV DC link voltage and 0.9 modulation index. The highest voltage is chosen to be 1.2 kV, operating at 88 % of the full-rated MV SM for safety reasons. Each figure displays the output voltage and the SM capacitor voltages at different operating conditions. It can be observed that the series operation of the 3 SMs is working properly for different wave shapes at different operating voltages as required. Additionally, though the obtained waveforms are only with a single MV SM without any output voltage control, their quality is acceptable with THD around 5 %. The THD for the non-sinusoidal waveform is obtained from 3.30.



Figuur 6.20: Square pulse waveform.

Apart from the wide voltage range, Fig. 6.19(a) and (f) shows the operation of MMC-based AWG when the reference waveform is varying from 1 Hz to 600 Hz. As discussed in Section 6.3, the large ripple of roughly 30 V is visible in Fig. 6.19(a). The large capacitor voltage ripple of 30 V exists only because of the APS consumption, as per the calculations from (6.15). The capacitor voltage ripple is reducing from 10 Hz to 600 Hz waveform since the APS consumption is negligible due to the minimum period with high frequency. Note that the SM capacitor voltages are shown for 1 s irrespective of the frequency of the waveform, and all SM capacitors are balanced well. With only a single SM per arm, the current harmonics are not filtered in any of the waveforms shown, and the switching harmonics are distinctively visible in 600 Hz since the ratio of switching frequency to reference waveform is lowered. Additionally, the THD of all waveforms shown in Fig. 6.19 are within 5 %. The fastest rise obtained from the MMC-based HV AWG is found to be 170 µs when 800 V DC voltage is applied with a modulation index of 0.9. Its performance is shown in Fig. 6.20, and the obtained slew rate is 2.35 V/µs. The rise time generated from the MMC-based HV AWG is limited since the arm inductor is present, and switches have limited current capability [142]. After verifying the start-up, steady-state and shut-down operation of the MMC-based HV AWG, the FRT capability of the test source is verified in Fig. 6.21. Here, the load capacitor is shorted using an HV relay



Figuur 6.21: Fault Ride Through (FRT) performance (a) Output characteristics (b) SM Capacitor Voltages.

with a small resistance of 40 Ω. When such an event occurs, the arm current increases, and the over-current protection operates when the current crosses the set point of 1 A. As discussed in Section 6.3.4, the fault protection operates within 40 µs and protects the MMC hardware.

6.5. CONCLUSIONS FOR HARDWARE DESIGN OF THE HV AWG

To test HV equipment with increasingly complex transients obtained from various power system studies, this chapter demonstrates the performance of the scalable series connected MV SM design for the MMC-based HV AWG. The proposed MV SM generates a wide output voltage range of 0.12 kV to 1.2 kV to satisfy the requirement posed by the HV AWG application. Additionally, the proposed design of SM capacitance works for different arbitrary wave shapes with a wide output frequency range from 1 Hz to 600 Hz. With the extensive quantitative analysis of the system parameters affecting the start-up behaviour, a new and comprehensive start-up procedure is formulated for the proper operation of the MMC-based HV AWG. During the steady state operation, the series connection of 3 SMs works as expected with the designed control system for a wide SM voltage range and different wave shapes with different frequencies. Overall, this MV SM fulfills HV test requirements, and the design behaves as expected and can generate bipolar voltage waveforms for dielectric testing of various insulating materials and HV equipment. With the MV SM realized using the off-the-shelf component, the proposed design is recommended to develop the MMC-based HV AWG for testing for MV class equipment.

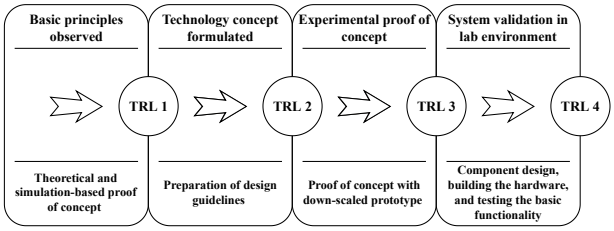
7

FUTURE OUTLOOK OF THE HV AWG

This chapter presents the current status of the MMC-based HV AWG and discusses what further steps to be followed. Based on the lesson learnt during the PhD thesis, a detailed design flow and required verification tests are prepared to proceed further to realize the full-scale prototype of the MMC-based HV AWG.

7.1. INTRODUCTION

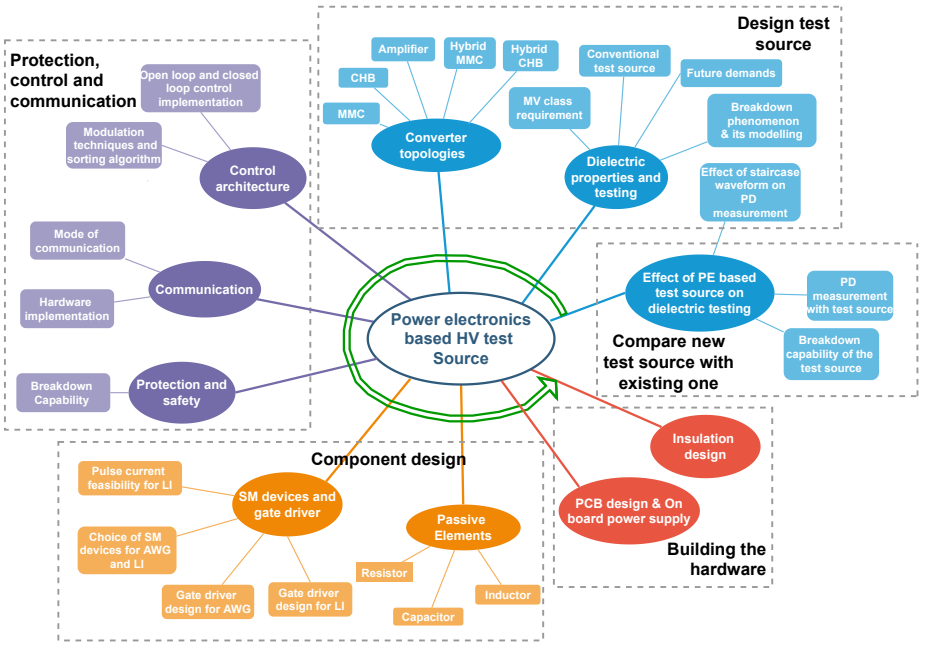
With this PhD thesis, the research in the MMC-based HV AWG reaches the Technology Readiness Level (TRL) of 4, where the MMC prototype is validated in the lab environment in Chapter 6. Earlier, TRL 1 was achieved with the preliminary analytical and simulation studies of the MMC-based HV AWG [73]. The next step of TRL 2 and 3 was achieved where exhaustive design trade-offs were discussed analytically, with MATLAB-Simulink simulations and scaled-down MMC prototype in Chapter 3 [99]. Fig. 7.1 shows the overall status of the development of the MMC-based HV AWG using TRL levels, as discussed in [143].



Figuur 7.1: Current status of the MMC-based HV AWG.

Moreover, Fig. 7.2 compiles all the technical challenges to realize a PE-based HV AWG. As per the figure, the challenges are divided into five parts, which are investigated in de-

tail in this thesis to realize the full-scale prototype of the MMC-based HV AWG. Within the PhD time frame, PD measurement or dielectric breakdown tests could not be performed with the newly designed test source. Based on the lessons learned during this PhD thesis, this chapter provides essential guidelines for realizing the full-scale prototype of the MMC-based HV AWG. Firstly, guidelines are given specific to the hardware and control development with a design flow for further development of the test source. Secondly, various verification tests are summarized for building the full-scale prototype. Lastly, some guidance is given to identify what is the root cause of the most common issues faced in the complex MMC topology.

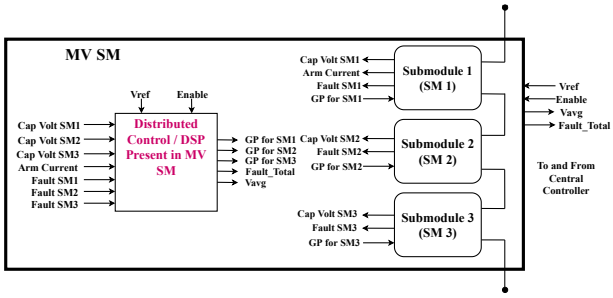


Figuur 7.2: Involved challenges in the PE-based HV AWG

7.2. DESIGN FLOW FOR MMC HARDWARE AND CONTROL

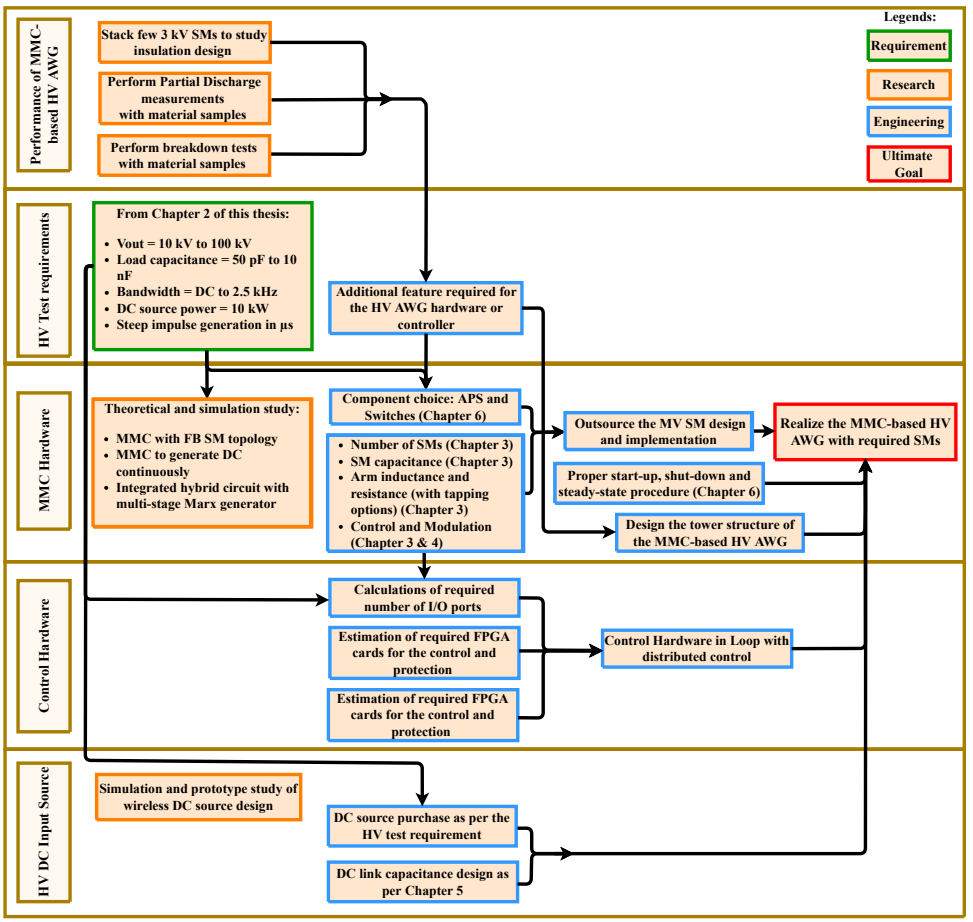
The experimental results from Chapter 6 prove the feasibility of the series operation of 3 SMs to create an MV SM, and this MV SM is scalable to stack more of these to create the 100 kV rated MMC-based HV AWG. Since the MV SM is realized using commercially available component, producing the MMC-based HV AWG is possible and cost-effective. One of the significant challenges faced was the APS and its mismatch during the start-up. A hardware solution to control the start of all APSs together will be helpful. Secondly, the demonstration of the MV SM is done with a central controller where all data of the SM capacitor voltage, fault, enable, and gate pulse data is exchanged with the central controller. Moving to a distributed controller for the full-scale prototype will be necessary, as shown in Fig. 7.3. The arm energy controller shown in Fig. 6.5 should be implemen-

ted in the local DSP to reduce the total required fiber optic communication units. In the current system, each SM has 7 to 8 fiber optics; the total fiber optic elements for the MV SM will be 23 to 24 fiber optic elements. The distributed control system will reduce the number of fiber optic elements to 4 per HV module.



Figuur 7.3: Overall control architecture for MV SM

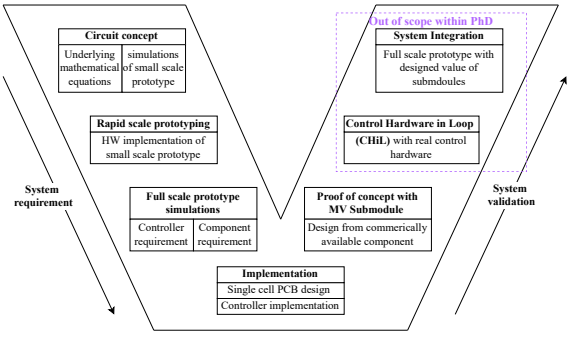
Currently, the input of the MMC-based HV AWG is implemented using a Glassman High Voltage source (EQ series with 10 kV voltage rating and 120 mA current rating) and two split capacitors of 50 μF. A similar structure is proposed for the full-scale prototype of the HV AWG, where the split capacitors are reduced to lower values, as low as a few microfarads. However, HV DC source with a variable voltage range from 20 kV to 200 kV is needed. For such an implementation, there is a traditional cascaded rectifier design [127] or transformer with diode rectifier-based design [144]. To realize the MMC-based HV AWG, the following design flow is suggested in Fig. 7.4, including both research and engineering activities.



Figuur 7.4: Design flow for further development of the MMC-based HV AWG.

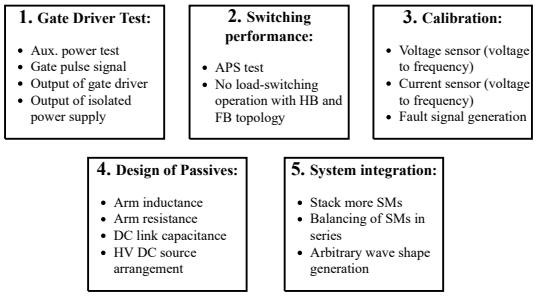
7.3. TESTS FOR FINAL VERIFICATION

Based on the design flow, a V model diagram is prepared in Fig. 7.5 for the overall development and realization of the MMC-based HV AWG. One of the critical subsequent tests in the system verification will be control hardware in the loop to test the capability to generate high-frequency waveforms when a high number of SMs are needed to be controlled. Later, the proposed hardware design of MV SM from Chapter 6 should be optimized from the prototype design to the HV testing requirements, as discussed above, to perform the system integration.



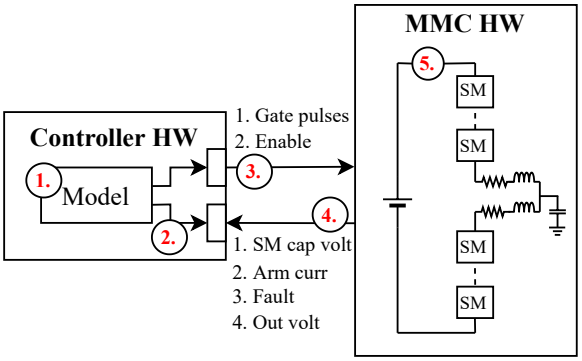
Figuur 7.5: V model of the PE-based HV AWG.

The system integration starts by preparing many single SMs, and Fig. 7.6 shows the stepwise tests required to prepare a single SM. As per Fig. 7.6, the gate driver board must be tested to get the proper gate signal for the MOSFET. Secondly, the switching performance and the onboard APS verification must be verified. Next, a critical step of calibrating the voltage and current sensor must be performed. The current sensor is absent in all SMs except two SMs from each arm to measure arm current. Additionally, the fault signal generation must be tested for overvoltage and overcurrent conditions. The system integration will be performed with the tested many individual SMs and passives involved with the HV DC source.



Figuur 7.6: Tests to be performed at SM level.

One of the significant challenges in system integration with such a complex converter topology is to perform the root-cause analysis when the converter is not working. Hence,



Figuur 7.7: Most common issues that can happen in system integration of the MMC-based HV AWG.

it is advisable to know what to expect with the critical system parameters of the MMC, such as **output voltage, SM capacitor voltages, modulation indices, and arm currents** using the theoretical understanding and simulation model. Fig. 7.7 shows the miniature circuit diagram of the MMC-based HV AWG, including its connection to the controller hardware, with the most common issues faced, which are discussed below:

1. Controller model: The first issue can happen in designing and building the controller model, and this issue can be studied using the simulation model. Here, it is crucial to know the ideal behavior of most of the components in the simulation and understand its effects on the system's performance. For example, each APS has different current consumption and efficiency, making it hard to tune the controller parameters directly from the simulation model.

2. IO port configuration: Connecting the correct model output to the correct IO port is essential. This can be ensured by following proper labeling, and any changes in the IO use should be updated. For example, during the soft start-up implementation, the UA and LA gate pulses were altered in the IO configuration, creating the wrong output voltage.

3. Output connections: MMC topology has many outputs for centralized and distributed control. Hence, it is important to follow an SM-based approach. It means that the fiber optic connection should not be changed once the particular SM is tested for its basic functionalities and calibrated for the voltage and current sensor data.

4. Input connections: The input connection to the controller with its correct calibration is crucial for the closed-loop control.

5. Open circuit in power loop: While preparing the experimental setup, one of the connections in the power loop may be missed. This can be identified by observing no current drawn from the DC source, and the SM capacitor voltages are not charged.

7.4. CONCLUSIONS FOR FUTURE OUTLOOK OF THE HV AWG

This chapter has provided an overview of the present state of the MMC-based HV AWG technology while also delving into the forthcoming stages of development. Drawing insights from the lessons learned throughout the course of the PhD thesis, a detailed design methodology has been outlined, accompanied by essential validation procedures. By diligently following this strategic road map, tangible and impactful outcomes in the realization of an HV AWG can be assured.

8

CONCLUSIONS AND FUTURE RECOMMENDATIONS

8.1. CONCLUSIONS

This PhD thesis investigates the MMC-based solution to fulfill the upcoming customized dielectric test requirements for various HV grid assets and provide additional capabilities during conventional tests, such as faster isolation of the device under a test set-up in case of breakdown or reducing the test preparation time. The most preeminent conclusions from this PhD thesis are as follows:

1. The MMC solution is chosen over CHB and HV amplifiers since it offers the required scalability to higher voltages and current ratings despite its complex control. Its capabilities are showcased analytically with a simulation model and a scaled-down prototype with a DC-link voltage of 300 V.

2. Generating steep pulses in the μs range from series-connected SMs in MMC topology becomes increasingly difficult. Hence, a unique integrated hybrid solution is proposed, which combines the MMC and Marx generator to generate complex waveforms with steep impulses. A similar analytical study approach, with a simulation model and a scaled-down prototype, is used to prove its feasibility.

3. A suitable controller hardware is selected for the HV AWG application considering the requirement of the high-frequency reference waveform generation and the capability to program various complex wave shapes easily

4. Apart from these studies, this PhD thesis provides a scalable MV SM design for the MMC-based HV AWG from commercially available components. The performance of the proposed design is demonstrated with a DC-link voltage of 2.7 kV with proper start-up, steady-state and shut-down behaviour.

5. Based on lessons learned during the PhD thesis, clear guidance is formulated for further developments of the MMC-based HV AWG.

Apart from these highlighted conclusions, the following section dives deeper into concluding the PhD research as per research questions discussed in the Introduction Chapter.

Q1. What is HV testing/dielectric testing? How is it performed?

Dielectric tests of HV grid assets such as cables, transformers (distribution and instrument), and switchgear have a long history, and they are standardized in terms of IEC or IEEE standards for particular voltage classes. As this PhD aims to target dielectric tests of MV class equipment, required tests are compiled for the grid assets mentioned in Chapter 2 and Appendix A. The most common tests are power frequency and LI with 1.2 µs rise time with much higher voltage magnitude than the rating of the equipment, taking into account the transient voltages in the electrical grid. All equipment mentioned above has a particular structure and needs dedicated dielectric tests to test all configurations. Hence, the test circuit is studied in detail for all equipment mentioned above, and some of the instrument transformers need particular types of tests.
However, the massive integration of renewable energy sources using PE converters is creating new and/or different electric stresses for these HV grid assets. Chapter 2 summarizes them for studying dielectric properties at the material, HVAC, and HVDC levels. These waveforms are not standard and need a programmable HV test source with bandwidth in the range of kHz. Additionally, Chapter 2 identifies limitations with the existing HV test sources and test circuits to generate the new electric stresses, which underpins the motivation for the PE-based HV AWG. Since the HV testing application is significantly different from the PE converter's usual power transmission application, key differences are highlighted to identify design trade-offs for the PE-based HV AWG.
This research question delivers HV test requirements with a 3D diagram of output voltage, load capacitance, and frequency as given in Fig. 2.14. The test requirements are divided into three boxes depending on the current required and different converter operations. Box 1 is limited by the power rating of the DC source to be 10 kW. Box 2 is mainly about generating steep pulses such as LI, and its feasibility is performed for the outermost point in the 3D diagram in Fig. 2.14. Box 3 covers generating high-frequency waveforms across HV insulation material to perform PD measurements or ageing tests.

Q2. What is a promising solution direction for HV AWG? How to design the selected solution as a HV AWG?

Among the HV amplifier and multilevel PE converter topologies, the MMC converter topology is considered the most promising solution for HV AWG applications, considering the various benefits offered to achieve precise arbitrary waveform generation. Different design trade-offs of MMC-based HV AWG are studied in detail in Chapter 3, considering multiple challenges posed by the HV testing requirements. The harmonic performance of the AWG is predominantly influenced by the choice of modulation technique, arm inductance (L_a), arm resistance (R_a), number of SMs (N), semiconductor devices, submodule capacitance, and control systems. The relationship between the above-mentioned

parameters is well elaborated in Chapter 3 to obtain accurate voltage waveforms. Additionally, the circulating current is almost negligible in the HV AWG application, which makes it possible to balance the SM capacitor voltages even when higher harmonics are generated from the MMC-based AWG. Based on the negligible circulating current observation, SM capacitor voltage ripple expression is derived, which proves that the SM capacitance in the μF range is sufficient to generate an accurate waveform. This analytical understanding has been developed for the first time and proves to be the foundation of further work on the MMC-based HV AWG.
The design trade-offs discussed in this study are validated with MATLAB-Simulink simulations and a scaled-down prototype of a 12-submodule MMC. A significant observation is that the simulations conducted in MATLAB-Simulink closely match the experimental outcomes from the scaled-down prototype. Moreover, the scaled-down prototype already demonstrates a reasonable level of accuracy in generating voltage waveforms, and these generated waveforms encompass bipolar, unipolar, and mixed polarity waveforms, effectively showcasing the MMC-based AWG's performance. The Total Harmonic Distortion (THD) for most waveforms is either around or below 1 %, except for the unipolar complex waveform and unbalanced sinusoidal waveform, where it reaches around 3 %. Furthermore, the theoretical assumption of negligible circulating current and the derived expression for submodule capacitor voltage are substantiated through MATLAB-Simulink simulations and experimental observations using the scaled-down prototype. The validated design guidelines prepared are applied for the full-scale prototype of the MMC-based HV AWG, and its performance is examined in MATLAB-Simulink with 67 submodules in each arm. Like the scaled-down studies, the assessment encompasses aspects such as circulating current dynamics, submodule capacitance selection, and harmonic output voltage characteristics. In essence, this chapter offers comprehensive design guidelines for realizing an MMC-based HV AWG tailored to the requirements for the dielectric testing of grid assets.
Even though the arm resistance-based passive damping methodology presents satisfactory results in damping the resonance between arm inductance and load capacitance, it creates losses in the arm resistor as the DC link voltage increases. Hence, a filter-based active damping methodology is implemented using a bandpass filter, which measures the resonance, and PI-based control removes the resonance. The performance of the designed control loops is shown with the MATLAB-Simulink MMC model with 12 submodules per arm, where various waveforms such as triangular, trapezoidal, and a combination of trapezoidal and sinusoidal waveforms are generated from the MMC-based AWG with THD less than 1 %. Even though the active damping methodology reduces losses in the arm resistor, the involved control loops can limit the possible large-signal bandwidth with the MMC-based HV AWG. Hence, passive damping control methodology is preferred over active damping.

Q3. How to design hardware and control of HV AWG?

Chapter 6 of this thesis proposes an innovative structure of a scalable MV SM design of the HV AWG. It consists of 3 Full-Bridge (FB) SMs, each rated for 1 kV, connected in series, and it is a scalable design with its own onboard APS with a wide input range to satisfy the HV test requirement in Box 1. The onboard APS consumption puts additional criteria

on the SM capacitance design, eventually affecting the minimum possible frequency obtainable from the output waveform. Additionally, the onboard APS creates challenges for a proper start-up procedure and steady-state operation, considering the non-idealities present in individual SMs. Hence, a special start-up algorithm is formulated and studied analytically for N SMs per arm. Also, an arm energy controller ensures equal voltage sharing for the series-connected SMs in the steady-state operation. The performance of the proposed design is demonstrated with a single SM per arm where the DC link voltage is varied from 0.8 kV to 2.7 kV. In order to get the required ten times wide output range (0.12 kV to 1.2 kV), the modulation index is reduced from 0.9 to 0.3 without affecting the THD of the obtained waveforms to get a lower output voltage. Now, different bipolar wave shapes, such as triangular and sinusoidal, with different harmonics, can be generated with the above-mentioned wide output voltage range. Additionally, various sinusoidal waveforms with frequencies ranging from 1 Hz to 600 Hz are demonstrated with the modular prototype of MMC. Moreover, the Fault Ride Through (FRT) capability is verified with the modular prototype of the MMC-based HV AWG, providing fast isolation from any breakdown of the device under test.

Though the modular structure of the MMC offers scalability concerning its hardware submodule, the controller hardware can create challenges for the scalability of the MMC with many submodules. With a large number of submodules, the MMC-based HV AWG will need several FPGAs to implement the control. Since programming different complex wave shapes in FPGA using VHDL or Verilog can be tedious for the test engineer, a commercially available Real Time Simulator (RTS) with multiple FPGAs included can be a solution. Among various commercially available options, Typhoon HIL satisfies the criteria of the small simulation step and can generate accurate high-frequency reference waveforms, carrier waveforms, and gate pulses. Its performance is demonstrated in Chapter 4 with a scaled-down prototype of the MMC-based AWG with two submodules per arm, and arbitrary high-frequency waveforms up to 5 kHz (large-signal bandwidth) are generated accurately with THD less than 5 %. This satisfies the bandwidth requirement of Box 1 from Chapter 2.

Q4. How to generate steep pulses with rise time as few μs using MMC-based HV AWG?

The series connections of many SMs create severe challenges for the MMC to generate steep pulses such as the LI waveform. As discussed in Chapter 5 of this thesis, it is clear that the low current-rated discrete switches can not fulfill the required pulse current specifications to generate the LI waveform due to the presence of stray inductance in the loop. Even when high current-rated switches are used, the stray inductance in the path and jittering effect in the MMC topology makes it impractical to obtain rise times in the range of μs when a capacitive load of 10 nF is connected. To solve this challenge and meet the Box 2 requirements from Chapter 2, a novel concept of an integrated hybrid test circuit of MMC and the Marx generator is proposed and investigated further analytically with a simulation model and the scaled-down prototype. It has been identified that the finite output impedance of the MMC interferes with the Marx generator circuit, affecting the rise or tail time of the waveform. The interference is minimal when the time constant of the MMC circuit is much higher than both time constants involved in the generated impulse, and this impact of the MMC circuit parameter on the Marx genera-

tor circuit design can be derived from the proposed analytical model. With the design flow prepared in Chapter 5, proper rise time and tail time are obtained in the simulation model, and the scaled-down prototype confirms the validity of the design flow.

8.2. FUTURE RECOMMENDATIONS

Based on the the discussion in Chapter 7, following recommendations for further development of the MMC-based HV AWG are formulated:

- Effect of MMC-based HV AWG on Dielectric Testing: This PhD thesis has delivered a modular prototype of the MMC-based HV AWG, which can go up to 3 kV. It will be valuable to perform a PD measurement and dielectric strength tests with oil paper or epoxy material insulation as a load. This will be an important verification considering the inherent switching behaviour of the MMC as an HV test source, which may interfere with the dielectric testing and affect the measurements.
- MMC with FB Topology: Most studies within this PhD are performed with Half-Bridge (HB) topology. However, as highlighted in Chapter 6, using the FB topology to reduce the DC-link voltage requirement by half is possible. Additionally, the flexibility offered by the FB MMC can support to generate unipolar and DC waveforms continuously when the onboard APS is connected parallel to the SM capacitance.
- Integrated Hybrid Circuit with MMC and multi-stage Marx Generator: Chapter 5 has proposed the integrated hybrid circuit of MMC with a single-stage Marx generator for the initial proof of concept study to superimpose LI waveform with higher voltage magnitude than the DC link voltage. However, the magnitude of the LI impulse or any fast-rising impulse can be much higher than the DC link capability of the MMC. Hence, it is crucial to study the multi-stage Marx generator to configure it with the MMC.
- Demonstration of Box 3 requirements: The test requirements summarized in Chapter 2 are named Box 1, 2, and 3. This PhD thesis has answered Box 1 requirements in detail and Box 2 requirements up to the scaled-down prototype level. However, Box 3 requirements are not explicitly demonstrated in the prototype, especially the low capacitance and high bandwidth. It is essential to mention that the SiC MOSFETs can be operated with 250 kHz switching frequency. With the correct design of the filter, it is possible to generate high-frequency pulse-modulated waveforms for low capacitive load at a relatively low voltage range of 10 kV to 50 kV.

A

SUMMARY OF HV TEST REQUIREMENT

This Appendix is prepared in-consultation with the HV test engineers from the KEMA Labs which summarized dielectric test requirement as per IEC standards. In the first tabular format, general dielectric test requirements are summarized with the details about the various test waveforms such as sinusoidal, DC, and various impulse waveforms. Fig. A.1 show various impulse waveforms and how the rise time and tail times are defined as per IEC standards [14]. Additionally, it consists testing procedure and voltage measuring system for the particular test waveform [127]. The next tabular format reviews all dielectric test requirements for the selected MV equipment for their type tests [10][11][12][26][13]. Additionally, the IEC standards for the HVDC cable testing is summarized since it requires additional challenging superimposed test waveforms [111].

This Appendix is based on a report written in collaboration with various test engineers from KEMA Labs

General dielectric testing procedures (IEC 60060-1 and IEC 60060-2)

DC signal				
Types of DC signal	**Voltage wave shape**	**Current requirement**	**Testing procedure**	**Voltage generation and measurement**
• Switching behaviour • Square waveform • Trapezoidal waveform • Constant DC part	• Ripple factor should be less than 3% (half the difference between the max and min) • Test duration less than 60s, ±1% in peak voltage • Test duration more than 60s, ±3% in peak voltage • For wet and pollution tests, voltage drop <10% is acceptable	• Capacitive current (largest component) • Dielectric absorption current • Continuous leakage current • PD current • Assuming voltage slew rate as 200 kV/μs and max load capacitance as 10 nF, charging current peak required is 2 kA	• Voltage should be increased with 2% of U per second when the applied voltage is above 75% of U	• **Voltage generation:** Cascaded rectifier • **Voltage measurement:** arithmetic mean value, ripple factor and any transient • **Converting device:** Resistive (High) divider or universal divider
Sinusoidal signal				
Frequency range	**Voltage wave shape requirement**	**Current requirement**	**Testing procedure**	**Voltage generation and measurement**
• **Lab tests:** 45 to 65 Hz • **Onsite tests:** 10 to 500 Hz (optional) • **VLF:** 0.01 to 1 Hz (optional)	• Difference in +ve and -ve peak <2% • Ratio of peak to RMS = $\sqrt{2} \pm 5\%$ • THD used in PD pattern recognition • For short tests < 60s, ±1% of the specified level • For long tests > 60s, ±3% of the specified level	• **Dry tests** below 100 kV: > 100 mA • **Wet tests** below 100 kV: > 1 A • **Artificial pollution**: 1 to 5 A	• **Application of test voltage:** Raised slowly (2% of U per sec for voltage above 75%), maintained at rated voltage for 60 s, and rapidly decreased (not interrupted) • **Withstand test** • **Disruptive discharge test**	• **Voltage generation:** Trafo, cascaded trafo, resonance circuit • **Converting device:** capacitive divider or universal divider

	• Rated frequency variation should be less than 1% • For wet and pollution tests, ≤20% • No significant effect on disruptive discharge voltage with Non-disruptive discharge voltage		• **Assured disruptive discharge test**	
Lightning impulse (LI)				
Types of LI	**Voltage wave shape requirement**	**Current requirement**	**Testing procedure**	**Voltage generation and measurement**
• Standard: Full wave (Figure A-1(a)) • Tail chopped (Figure A-1(b)) • Front chopped (Figure A-1(c)) – only there for insulators • Linearly rising front chopped (Figure A-1(d))	• Rise time = 1.2 μs±30%, Fall time = 50 μs±20% • Voltage peak = Vp±3% • Time to chop ~ 2 μs to 5 μs. Time to chop should be faster than front time.	• C_{max}= 10 nF • dv = 200 kV • dt = 1.2 us • Maximum current required to charge this capacitor is 2 kA	• **Proc A:** 3 impulses and no failure • **Proc B:** 15 impulses and less than 2 failures • **Proc C:** 3 impulses and additional 9 more if more 2 are failed • First positive polarity and later negative polarity. 2 min between each polarity	• **Voltage generation:** Marx generator with variable resistors • **Converting device:** Resistive (low) divider or capacitive damped divider
Switching impulse (SI)				
Types of SI	**Voltage wave shape requirement**	**Current requirement**	**Testing procedure**	**Voltage generation and measurement**
• Standard SI (Figure A-1(e))	• Rise time = 250 μs ± 20% • Fall time = 2500 μs ± 60% • Peak value of voltage = Vp ± 3%	• C_{max}= 10 nF • dv = 200 kV • dt = 250 us • Maximum current required to charge this capacitor is 8 A	• Similar to LI	• **Voltage generation:** Marx generator with variable resistors • **Converting device:** Capacitive divider or

				capacitive damped divider
Composite signal (2 terminal devices)				
Types	**Voltage wave shape requirement**	**Current requirement**	**Testing procedure**	**Voltage generation and measurement**
• Combination of power frequency and impulses • Combination of DC and impulses	• Voltage value (voltage variation < ±5 %) • Time delay (±0.05Tp, where Tp is time to peak of an impulse)	• For single test source to generate two wave shapes, it will be addition of currents required by two wave shapes	• Specific to test object	• Superimposition of two test sources

36 kV class switchgear and control gear (IEC 62271-1)

No	Type of test	Details	Time taken to prepare and perform test	Test object modelling
1.	Power frequency withstand test	70 kV (common value) and 80 kV (across isolating distance) for 1 min Routine and type test	For 3 phase switchgear (panel) 0.5 day – for 1 min test it takes 4 hours to prepare	• Load capacitance for both types of test is considered to be in the range of 50 pF. • $R_{leakage}$ in parallel to load capacitance is considered in the range $0.2V_{output}$ and V_{output}.
2.	Lightning impulse test	145 / 170 kV (common value) and 165 / 195 kV (across isolating distance) with Procedure B Type test	3 days – different cases to be tested Total impulses = 600	

36 kV class power transformer (IEC 60076-1 and IEC 60076-3)

No	Type of test	Details	Time taken to prepare and perform test	Test object modelling
1.	Applied voltage test	70 kV for 1 min Routine test	Power rating < 4 MVA ~ 0.5 hour	• Applied voltage test: Load capacitance (LV) = 19-26 nF Load capacitance (HV) = 12-16 nF • Induced voltage test: Load capacitance is less than applied voltage test since generally α ($\alpha = \sqrt{\frac{Cg}{Cl}}$ >1)
2.	Induced voltage withstand test (IVW)	$2U_r/\sqrt{3}$, higher frequency with less duration to avoid core saturation. $Duration = 120 \times \frac{rated\ frequency}{test\ frequency}\ not\ less\ than\ 15\ s$	~ 0.5 hour	
3.	Induced voltage test with PD measurement (IVPD)	Test circuit is similar as IVW test	0.5 day	
4.	Lightning impulse test	• 170 / 200 kV with Procedure B • Usually negative polarity • The values of waveshape specified may not always be obtainable. In the impulse testing of large power transformers and reactors, of low winding inductance	0.5 day	

		and/or high surge capacitance, wider tolerances may have to be accepted. Type test		• Impulse test: Parallel combination of C_g and C_s per turn will also be less than C_g value. • $R_{leakage}$ in parallel to load capacitance is considered in the range $0.2V_{output}$ and V_{output}.
5.	Chopped wave lightning impulse test for the line terminals (LIC)	187 kV/220 kV Special test	1 day	

36 kV class instrument transformer (IEC 61869-1)

No	Type of test	Details	Time taken to prepare and perform test	Test object modelling
1.	Power frequency withstand test	Primary terminal – 70 kV for 1 min Secondary terminal – 3 kV for 1 min Routine test	~ 0.5 hour	Load capacitance for PT = 1 nF for 36 kV Load capacitance for CT = 0.25 nF for 36 kV Rleakage in parallel to load capacitance is considered in the range 0.2Voutput and Voutput.
2.	PD measurement	U_m (36 kV) / 0.693U_m (25 kV) / 1.732 U_m (62 kV) (based on earthing) maintained for 30 s Routine test	0.5 day	
3.	Lightning impulse test	• Primary terminals 145 kV/170 kV • Procedure B, 15 impulses of each polarity Type test	0.5 day	
4.	Measurement of tan delta	Rated frequency and voltage $U_m/\sqrt{3}$ Special test	0.4 day	
5.	Chopped impulse test	• Primary terminal, only negative polarity (2 chopped impulses between 1 FL and 14 FL) • Instant of chopping = 2 to 5 µs • Opposite polarity overshoot should be less than 30 % Special test	0.4 day	
6.	Multiple chopped impulse test	• The test voltage shall be applied **between the primary terminals (connected together) and earth for CT's**,	2 days	

		and **between the primary high voltage terminals and the primary earth terminals** for earthed voltage transformers • The prescribed peak value of the test voltage shall be **70 % of the rated lightning impulse withstand voltage**. The impulse front of the test voltage should be **1,2/50 µs wave.** • **The virtual duration of voltage collapse**, measured according to IEC 60060-1, **shall not exceed 0,5 µs** and the circuit shall be so arranged that the over swing to opposite polarity of the impulse shall be approximately 30 % of the prescribed peak voltage. • **600 consecutive impulses** shall be applied, approximately at a rate of 1 impulse/min. Special test		

36 kV class AC cable (IEC 60502)

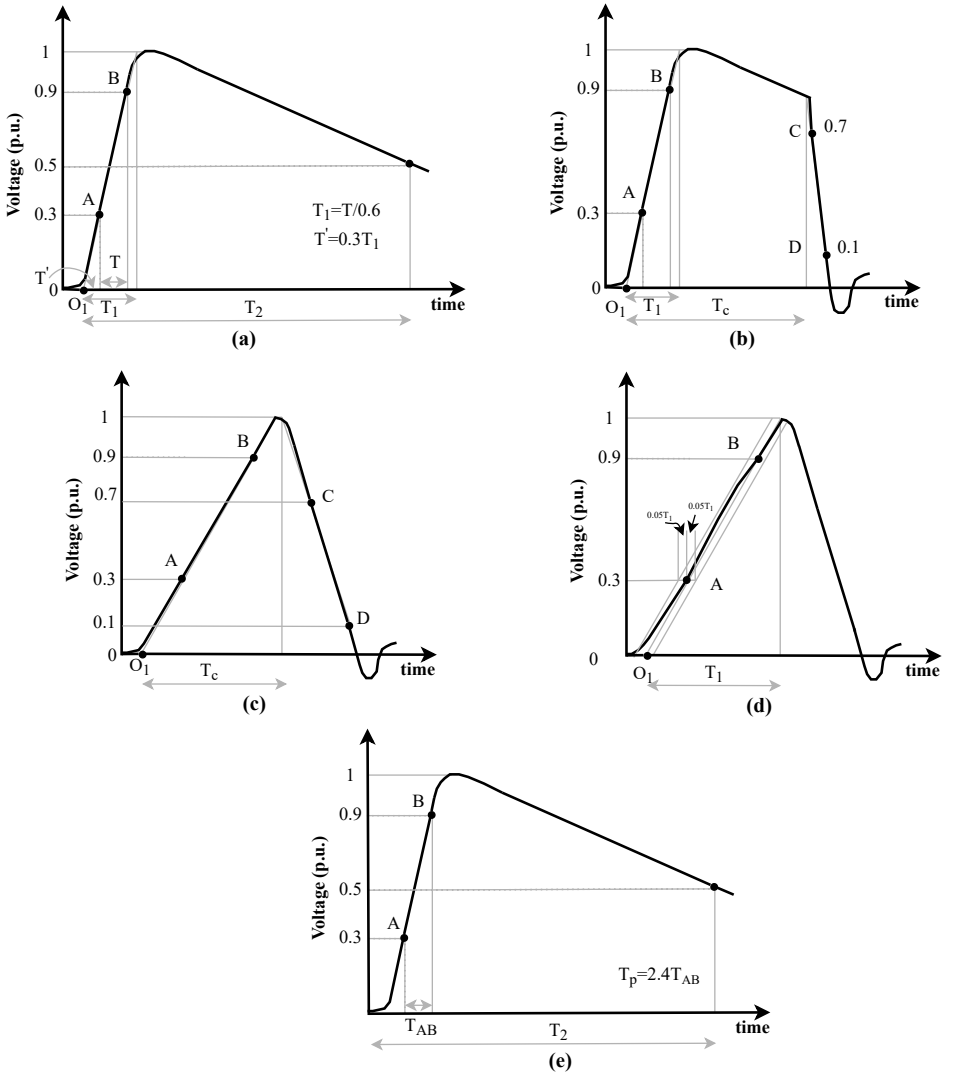
No	Type of test	Details	Time taken to prepare and perform test	Test object modelling
1.	Power frequency withstand test	63 kV for 5 min (1 hour) Routine test 70 kV for 4 hours (5 hours) Sample test 70 kV for 4 hours with maintained conductor temperature (1 day) Type test	Routine test – 1 hour Sample test – 5 hours Type test – 1 day	Sample test: Length = 5 m Type test: Length = 10-15 m Range of capacitance = 0.2-0.7 nF/m
2.	PD measurement	Raised to 36 kV gradually and maintained for 10 s and reduced to 31.14 kV. Routine test	(depends upon background noise – 0.5-1 day)	$R_{leakage}$ in parallel to load capacitance is considered in the range $0.2V_{output}$ and V_{output}.

3.	Lightning impulse test	• 170 kV • This test shall be performed on the sample at a conductor temperature 5 K to 10 K above the max conductor temp • 10 Positive and 10 Negative. Sequence given in IEC 60230 • 15 min power frequency voltage test should be performed Type test	1 day	Length = 10-15 m
4.	Measurement of tan delta	• This test shall be performed on the sample at a conductor temperature 5 K to 10 K above the max conductor temp • The tan δ shall be measured with an alternating voltage of at least 2 kV at the temperature specified above. Type test	1 day	Length = 10-15 m

HVDC cable (IEC 62895)

No	Type of test	Details	Time taken to prepare and perform test	Test object modelling
1.	DC withstand test	$U_T = 1.85U_o$ for 1 hour An AC test combined with PD measurement is recommended – where suitable. Test parameters shall be agreed between manufacturer and customer Routine test	0.5 day	Cable length = at least 30 m 0.25 nF/m.
2.	Polarity reversal test	Polarity reversals within two minutes at voltage of $1.45U_o$ (Type test) or $1.25\ U_o$ (Prequalification test – PQ test) – only present for LCC technology	0.5 day Prep time 2-3 hours	
3.	Lightning impulse with DC	• $U_{p1} = 1.15\ U_0$ • $T_{cond} > T_{cond,max}$ by 0 to 5 K higher for minimum 10 hours before test and maintained during the test • The cable shall withstand without failure 10 positive and 10 negative voltage impulses of the appropriate value. Rest period between two polarity of 24 hours with constant DC applied	• Preparation time few days to weeks. It depends upon test object height and required structure to	

4.	Switching impulse with DC	• $U_{p2,s}$ = 1.15U_0 and $U_{p2,o}$ = 1.15U_0 • T_{cond}>$T_{cond,max}$ by 0 to 5 K higher for minimum 10 hours before test and maintained during the test • The cable shall withstand without failure 10 positive and 10 negative voltage impulses of the appropriate value. Rest period between two polarity of 24 hours with constant DC applied	mount everything. • Operation and maintenance of water resistor consume time • Calibration of graphs consumes time • For SI, front and tail resistor needs to be changed and calibration of the graph needed	



Figuur A.1: Different Impulse Waveforms (a) LI (b) Tail chopped LI (c) Front chopped LI (d) Linearly rising front chopped (e) SI [14]

B

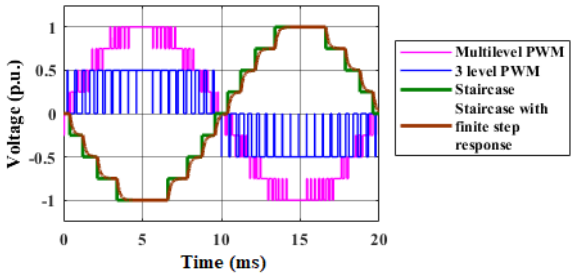
EFFECT OF STAIRCASE WAVEFORM ON APPLIED DIELECTRIC STRESSS

This appendix presents a comparison in Partial Discharge (PD) behaviour when an air corona setup is subjected to different waveforms, namely an idealized 50 Hz sinusoidal and staircase-based sinusoidal waveforms near inception voltage and at a higher voltage. In this study, it has been observed that the PD repetition rate and the Phase-Resolved PD (PRPD) pattern with the staircase waveform better resemble that of a pure sinusoidal waveform if the number of voltage levels of the staircase waveform is sufficiently increased. When observed more closely at the PRPD pattern near inception voltage, PDs tend to occur near the slope of the staircase waveform, even when the step voltage is small.

The evaluation of insulation stresses in grid assets can be conducted by examining Partial Discharges (PD), dielectric losses, breakdown strength, and electric field distribution. Since there is extensive knowledge about PD behaviour in 50 Hz sinusoidal waveform, this is selected as a bench-marking case to study the effect of the staircase waveform. Hence, this paper compares PD behaviour under pure sinusoidal and staircase waveform made of different voltage levels. It is important to point out that the maximum number of levels generated from an MMC is a design constraint which strongly affects the cost and complexity of the system. Thus, to identify the minimum number of levels and suitable step response of the generated voltage waveform that produces acceptable performance closer to the desired (ideal) reference is of paramount importance for the optimal design of the test source.
[145][146] studied the effect of a 2 level Pulse Width Modulated (PWM) waveform on the HV insulation system of electrical machines. It was found that the features of the

This chapter is based on:

- D. A. Ganeshpure, L. C. C. Heredia, M. G. Niasar, P. Vaessen, T. B. Soeiro and P. Bauer, "Analysis of Partial Discharge Behaviour under Staircase-based Sinusoidal Voltage Waveforms,"2020 IEEE 3rd International Conference on Dielectrics (ICD), 2020, pp. 894-897, doi: 10.1109/ICD46958.2020.9342005.



Figuur B.1: Different wave shapes as the output of the PE converters

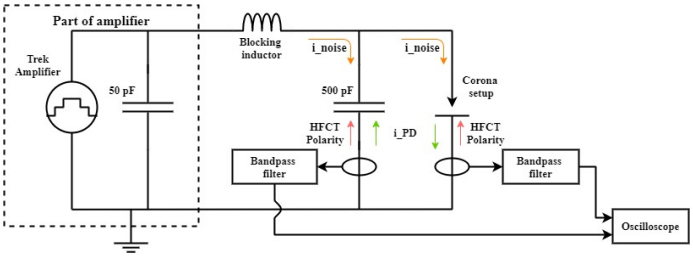
PWM waveform, i.e. switching frequency, duty ratio, and voltage magnitude have a deep impact on the PD magnitude, repetition rate, phase and time-resolved pattern. Ref. [147][148] suggested that the higher the number of levels in the PWM waveform, the lesser is the PD magnitude and inception voltage. Also, it is concluded in [147] that the multilevel PWM applies a new type of stress, which is a combination of AC, DC, and chopped waveforms.

For a better understanding of different wave shapes mentioned above, the typical voltages generated by power electronic systems operating with 3-, and 9-levels are shown in Fig. B.1. Note that the graphs in pink and blue are generated by voltage source converters operated with PWM modulation logics, while the voltage generated in green and brown are created by a multilevel converter operated with NLC. 3-levels PWM waveforms are quite critical with respect to both magnitude and frequency of dV/dt application when compared to the staircase waveform. Multilevel PWM waveforms are mainly critical with respect to frequency of dV/dt application when compared to the staircase waveform with the same number of levels. This paper offers a comparison in PD behaviour when an air corona setup is subjected to a pure 50 Hz sinusoidal and staircase waveform with a different number of voltage levels and different step responses for each voltage level.

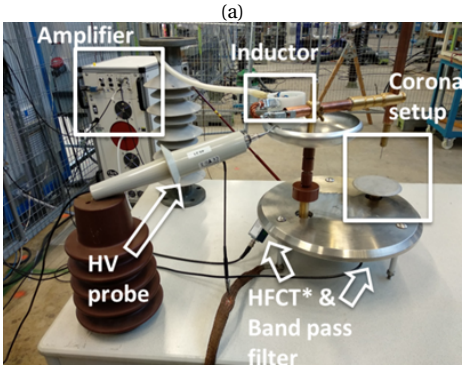
B.1. EXPERIMENTAL SETUP

Since the MMC-based HV test source is not yet ready in our laboratory, an arbitrary waveform generator and a Trek 30/20A HV amplifier setup are used to generate the desired staircase waveform with different number of levels. The test object is a traditional air corona with a needle length of 3.2 cm with a diameter of 0.3 mm. PD measurements are performed using two identical High-Frequency Current Transformers (HFCTs), along with a high-end oscilloscope, Tektronix DPO 7354C. Each HFCT has a gain of 9.1 mV/mA and bandwidth of 40 kHz to 130 MHz. A coupling capacitor is used to provide a low impedance and high-frequency path for the PD signal. In addition, a blocking inductor is installed to limit the noise from the amplifier. The schematic and the actual PD measurement setup are shown in Fig. B.2. After the HFCTs, band-pass filters (1.37 MHz – 90 MHz) are installed to filter the capacitive current present when the staircase waveform is applied.

The polarities of the two installed HFCTs are in the same direction so that it is possi-



(a)



(b)

Figuur B.2: (a) Schematic (b) Actual PD Measurement Setup

ble to check if the measured signals are PDs or electrical disturbances by comparing the polarity of signals obtained from both HFCTs. Before the actual PD measurement, the setup is checked to be PD free by measuring PDs without the corona needle. After preparing the setup, PDs are captured using a single HFCT, which is below the test object to showcase the results. The methodology used is as listed in the following:

- Apply different wave shapes such as sinusoidal and staircase waveforms with 3-, 5-, 7-, 13-, and 41-levels to observe the trend. Also, the step response in staircase waveforms has finite delay as defined by the slew rate of the HV amplifier and the impedance of the circuit. This delay is made longer by adding a resistor and the performance of sinusoidal and staircase waveforms with 41-, and 68-levels are compared with and without the resistor.

- Due to the presence of an overshoot in the staircase waveforms, the inception voltage changes slightly for different staircase waveforms as a function of the overshoot. To avoid this effect, the performance of different waveforms is compared at a voltage slightly higher than the inception voltage i.e. 5.6 kV and a voltage of 8 kV, some 40 % higher than the 5.6 kV.

- Fixed number of PD events (1000) are captured for each measurement, and the repetition rate is calculated based on the timestamp of the last PD. Each wave shape is not tested repetitively. Hence, the showcased results don't analyze the pseudo-stochastic behaviour of PD.

Tabel B.1: Trend in the PD Repetition Rate with Sinusoidal and Staircase Waveform with a Different Number of Voltage Levels

No of Levels	Vp=5.6 kV	Vp=8 kV	
	Avg. repetition rate (PD k.pulses/s)	Avg. repetition rate (PD k.pulses/s)	Voltage at which first PD observed (kV)
3 levels	0.4	6.2	-5.5
5 levels	0.3	4.1	-5.4
7 levels	0.2	3.8	-5.3
13 levels	0.2	3.1	-5.2
41 levels	0.1	2.9	-5.0
Pure Sine	0.1	2.7	-5.0

B.2. RESULTS

This section presents the obtained experimental results in four subsections, each showing the effect of the staircase waveform with a different number of voltage levels and with the different step response, on repetition rate, and Phase-Resolved PD (PRPD) pattern.

B.2.1. EFFECT OF THE STAIRCASE WAVEFORM WITH A DIFFERENT NUMBER OF VOLTAGE LEVELS ON THE PD REPETITION RATE

The average repetition rate for sinusoidal and staircase waveforms with different voltage levels are summarized in Table B.1 at the peak voltage of 5.6 kV and 8 kV. The voltage at which the first PD occurs at the higher voltage is also represented along with the repetition rate in Table B.1.

B.2.2. EFFECT OF THE STAIRCASE WAVEFORM WITH A DIFFERENT NUMBER OF VOLTAGE LEVELS ON THE PRPD PATTERN

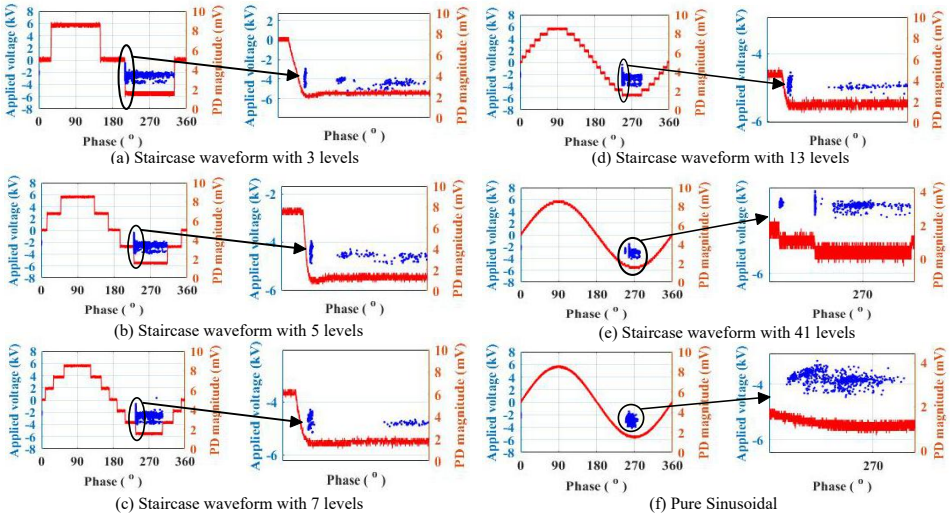
The PRPD patterns of sinusoidal and staircase waveforms with a different number of voltage levels are shown in Fig. B.3 at peak voltage of 5.6 kV. The PRPD pattern at higher voltage of 8 kV is shown for the pure sinusoidal and staircase waveform with 41 levels in Fig. B.3 since this gives a response closer to the pure sinusoidal.

When further zoomed into Fig. B.3(e), three different stages of PD patterns are observed as shown in Fig. B.3. In stage I, PDs occurs just after the slope. In stage II, PDs occur on the slope. Stage III shows random behaviour of PDs as seen in DC. In this case, the magnitude of voltage step is 280 V.

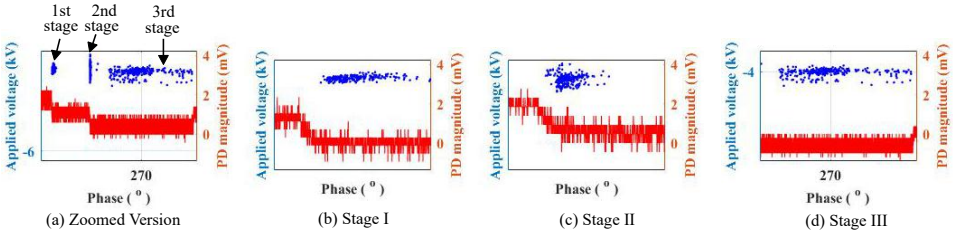
Fig. B.5 shows the PRPD pattern for 41 level staircase waveform and sinusoidal waveform with a zoomed picture. In this case, the magnitude of voltage step is 400 V.

B.2.3. EFFECT OF THE STAIRCASE WAVEFORM WITH A DIFFERENT STEP RESPONSE ON THE PD REPETITION RATE

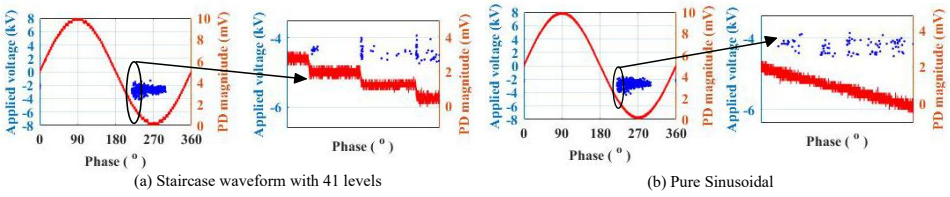
The step response of the staircase waveform is changed by adding a resistor of 100 k˙ in series with the blocking inductor. By adding such a resistor, the step response is changed from 10 μs to 50 μs. The obtained results are compared for 41 levels, 68 levels, and pure



Figuur B.3: Comparison of sinusoidal and staircase waveform with a different number of voltage levels on the PRPD pattern at Vp = 5.6 kV



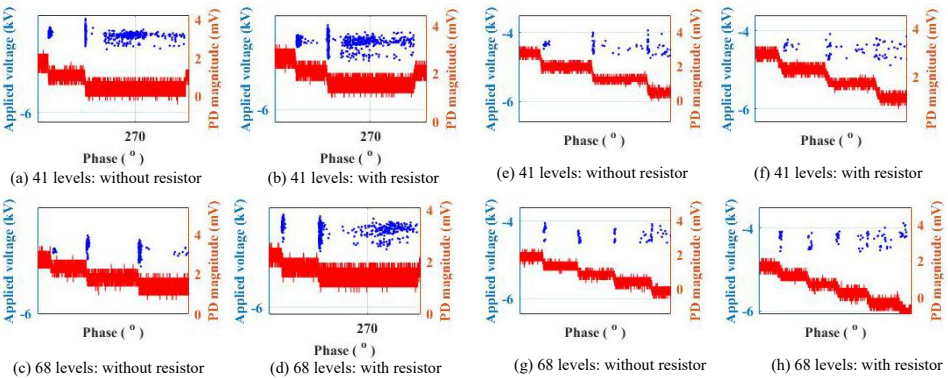
Figuur B.4: PRPD pattern for staircase waveform with 41 level at Vp = 5.6 kV



Figuur B.5: Comparison of sinusoidal and staircase waveform with 41 levels on the PRPD pattern at Vp = 8 kV

Tabel B.2: Trend in the PD Repetition Rate with Sinusoidal and Staircase Waveform with a Different Step Response

No of levels	Avg. repetition rate @ Vp=5.6 kV (PD k.pulses/s)		Avg. repetition rate @ Vp=8 kV (PD k.pulses/s)	
	Without Res	With Res	Without Res	With Res
41 levels	0.1	0.1	2.6	2.6
68 levels	0.1	0.1	2.5	2.6
Pure Sine	0.1	0.1	2.6	2.6



(a) 41 levels: without resistor (b) 41 levels: with resistor (e) 41 levels: without resistor (f) 41 levels: with resistor

(c) 68 levels: without resistor (d) 68 levels: with resistor (g) 68 levels: without resistor (h) 68 levels: with resistor

Figuur B.6: PRPD pattern (a) to (d): Vp = 5.6 kV & (e) to (h): Vp = 8 kV

sinusoidal in Table B.1.

B.2.4. EFFECT OF THE STAIRCASE WAVEFORM WITH A DIFFERENT STEP RESPONSE ON THE PRPD PATTERN

The effect of different step response of the staircase waveform is shown in Fig. B.6 with zoomed pictures since the full cycle PRPD pattern is not changing drastically.

B.3. DISCUSSION OF RESULTS

The observations made from the obtained results are summarized below:

- The average PD repetition rate of the staircase waveform at Vp = 5.6 kV and Vp = 8 kV resembles one of the pure sinusoidal as the number of levels is increased, as shown in Table B.1.
- At Vp = 8 kV with the staircase waveforms, the voltage at which the first PD observed changes due to involved voltage steps. As the magnitude of the voltage step is reduced in the staircase waveform, the voltage at which the first PD observed becomes the same as pure sinusoidal.
- PRPD pattern of staircase waveform changes near inception voltage when compared to the sinusoidal case. There are bulk of PDs occurring near the slope even

though the magnitude of the voltage step is relatively small (≈ 230 – 400 V).

- When zoomed into the performance of 41 levels near inception voltage in Fig. B.4, three stages are observed as described below:
  - Stage I – PDs occur just after the slope, as shown in Fig. B.4(b).
  - Stage II – PDs occur on the slope in Fig. B.4(c)
  - Stage III – PDs occur randomly, as shown in Fig. B.4(d). There is a gap between PD occurring on the slope and the subsequent constant (DC) part.

  This behaviour suggests that the electric stress applied is a combination of AC, DC, and transient.
- The average PD repetition rate of staircase waveforms with different step responses is almost the same, as shown in Table B.2.
- For the staircase waveform with a slower step response, the concentrated bulk of PDs move to the subsequent constant (DC) part in the case of a staircase waveform with 41 levels near inception and higher voltage. However, this is not distinctly visible for the staircase waveform with 68 levels with the PRPD pattern shown in Fig. B.6.

B.4. CONCLUSIONS

For the corona discharges in air, the PD performance of the staircase waveform resembles the pure sinusoidal as the number of voltage levels is increased. However, a significant difference has been observed with the PRPD pattern near inception voltage with the staircase waveform. A staircase waveform with a slower step response did not conclusively shift the bulk of PDs away from the voltage steps near inception voltage. Primary analysis suggests that the applied electric stress with the staircase waveform is a combination of AC, DC, and transient. Nevertheless, further investigations and measurements are needed to find out why the PRPD pattern changes near the inception and how the step response affects it. In summary, the change in PRPD pattern near inception voltage with staircase waveforms indicates different electrical stress compared to pure sinusoidal, and therefore the MMC based HV test source rated for 100 kV should generate with at least 68 levels with a rather slow step response.

BIBLIOGRAPHY

[1] Paris Agreement by United Nations, Available Online: https://unfccc.int/process-and-meetings/the-paris-agreement [Accesed on 02 August 2023].

[2] O. Saad en C. Abdeljebbar, "Historical Literature Review of Optimal Placement of Electrical Devices in Power Systems: Critical Analysis of Renewable Distributed Generation Efforts", *IEEE Systems Journal*, jrg. 15, nr. 3, p. 3820–3831, 2021.

[3] T. Bengtsson, F. Dijkhuizen, L. Ming e.a., "Repetitive fast voltage stresses-causes and effects", *IEEE Electrical Insulation Magazine*, jrg. 25, nr. 4, p. 26–39, 2009.

[4] S. Mukherjee, Y.-J. Häfner, S. Nyberg en M. Saltzer, "Cable overvoltage for MMC based VSC HVDC system: Interaction with converters", *CIGRE India Journal*, jrg. 7, nr. 2, p. 18–23, 2018.

[5] F. H. Kreuger, "Industrial High Voltage Volume I: 1. Electric Fields, 2. Dielectrics, 3. Constructions", 1991.

[6] "NEN-EN 50160, Voltage characteristics of electricity supplied by public electricity networks", 2010.

[7] J. Kuffel en E. Kuffel, *High voltage engineering fundamentals*. Elsevier, 2000.

[8] W. Hauschild, E. Lemke e.a., "High-voltage test and measuring techniques", 2014.

[9] T. J. Blalock, "High-Voltage Testing: man-made lightning at the 1939 World's Fair [History]", *IEEE Power and Energy Magazine*, jrg. 8, nr. 2, p. 62–81, 2010.

[10] "IEC 62271-1, High-voltage switchgear and controlgear – Part 1: Common specifications for AC switchgear and controlgear", 2017.

[11] "IEC 60076-1, Power transformers – Part 1: General", 2011.

[12] "IEC 60076-3, Power transformers – Part 3: Insulation levels, dielectric tests and external clearances in air", 2013.

[13] "IEC 60502-2, Power cables with extruded insulation and their accessories for rated voltages from 1 kV (Um = 1,2 kV) up to 30 kV (Um = 36 kV) – Part 2: Cables for rated voltages from 6 kV (Um = 7,2 kV) up to 30 kV (Um = 36 kV)", 2014.

[14] "IEC 60060-1, High-voltage test techniques - Part 1: General definitions and test requirements", 2011.

[15] "IEC 60060-3, High-voltage test techniques - Part 3: General definitions and test requirements", 2011.

[16] "Internal Test Reports, KEMA Laboratories, Arnhem, Netherlands, Confidential",

[17] 4 Methods of Medium – Voltage Circuit Breaker Design, Available Online: https://testguy.net/content/245-4-Methods-of-Medium-Voltage-Breaker-Design [Accesed on 24 April 2021].

[18] A.-I. Singuran, "The Investigation of Newly Designed Transformer Windings with Reduced Thickness of Oil-Impregnated Paper Insulation", 2012.

[19] "IEC 60076-11, Dry-type Transformers", 2018.

[20] Design Construction of Power Transformer, Available Online: http://eee-resetsg.blogspot.com/2016/02/construction-of-power-transformer.html [Accesed on 31 May 2021].

[21] A. Greenwood, "Electrical transients in power systems", 1991.

[22] M. Ghaffarian Niasar en W. Zhao, "Impulse voltage distribution on disk winding: calculation of disk series capacitance using analytical method", in *2020 IEEE International Conference on High Voltage Engineering and Application (ICHVE)*, 2020, p. 1–4.

[23] Difference Between Current Transformer (CT) & Potential Transformer (PT), Available Online: https://circuitglobe.com/difference-between-current-transformer-ct-and-potential-transformer-pt.html [Accesed on 31 May 2021].

[24] Current , how it works?, Available Online: https://www.electrical4u.com/current-transformer-ct-class-ratio-error-phase-angle-error-in-current-transformer/ [Accesed on 25 May 2021].

[25] Different types of Transformers - Shell and Core type Transformer, Available Online: https://www.electricalengineeringinfo.com/2015/01/types-of-transformers-shell-type-transformer-core-type-transformer.html [Accesed on 31 May 2021].

[26] "IEC 61869-6, Instrument transformers - Part 6: Additional general requirements for low-power transformers (IEC 61869-6:2016, IDT)", 2016.

[27] "Potential Transformers", [Accesed on 25 May 2021].

[28] TWENPOWER MEDIUM-VOLTAGE XLPE CABLES, TKF Cable, Available Online: https://www.tkf.nl/files/content/twenpower-engels-2015.09.09.115800.pdf [Accesed on 17 April 2022].

[29] A. Shekhar, X. Feng, A. Gattozzi e.a., "Impact of DC voltage enhancement on partial discharges in medium voltage cables—An empirical study with defects at semicon-dielectric interface", *Energies*, jrg. 10, nr. 12, p. 1968, 2017.

[30] X. Wang, "Partial discharge analysis at arbitrary voltage waveform stimulus", proefschrift, KTH Royal Institute of Technology, 2012.

[31] A. Cavallini, G. Montanari en L. Mariut, "The influence of test voltage waveforms on partial discharge activity in XLPE", in *2012 IEEE International Symposium on Electrical Insulation*, IEEE, 2012, p. 554–557.

[32] Advanced Energy - High Voltage Power Amplifier Products, Available Online: https://www.advancedenergy.com/products/high-voltage-products/high-voltage-amplifiers/ [Accesed on 13 December 2020].

[33] F. Barakou, "Investigation of the impact of EHV underground power cables on the resonant and transient grid behavior", 2018.

[34] Development & Testing Surge Arresters for DC Applications,INMR, Available online: http://www.inmr.com/development-testing-surge-arresters-applications/ [Accesed on 24 April 2021].

[35] PD4.3 – Report on Performance, Interoperability and Failure Modes of Selected Protection Methods, Available Online: https://www.promotion-offshore.net/results/deliverables/ [Accesed on 18 November 2023].

[36] M. Saltzer, M. Goertz, S. Wenig e.a., "Overvoltages experienced by DC cables within an HVDC transmission system in a rigid bipolar configuration", in *Proceedings of the 10th International Conference on Insulated Power Cables (Jicable'19), Versailles, France*, 2019, p. 23–27.

[37] S. Alapti, K. Johansson, M. Sjoberg en M. Klang, "Transient Over Voltage Testing of Cable Systems in MMC-HVDC Links: A Concept Study Including Verification", B1–10 514, 2022.

[38] J. Cao, P. Tuennerhoff, C. Gao e.a., "Design, test and application of HVDC circuit breakers", 2022.

[39] G. P. Lourduraj, "Feasibility study of oil immersed power electronic based high voltage test source for onsite testing purpose", 2019.

[40] HVAC testing of underground cable up to 132 kV, Available Online: https://demo.chrisansgroup.com/energy/final/photo-gallery.html [Accesed on 02 August 2023].

[41] Underground cables: Preventing failure with partial discharge testing, Available Online:https://us.megger.com/et-online/september-2015/underground-cables-preventing-failure-with-partia [Accesed on 29 November 2023].

[42] "IEC 62895, High voltage direct current (HVDC) power transmission – Cables with extruded insulation and their accessories for rated voltages up to 320 kV for land applications", 2017.

[43] J. Oliver en G. Stone, "Implications for the application of adjustable speed drive electronics to motor stator winding insulation", *IEEE Electrical Insulation Magazine*, jrg. 11, nr. 4, p. 32–36, 1995.

[44] J. W. Kolar en G. Ortiz, "Solid-state-transformers: Key components of future traction and smart grid systems", in *Proceedings of the International Power Electronics Conference-ECCE Asia (IPEC 2014)*, IEEE, 2014, p. 18–21.

[45] P. Mathew, M. G. Niasar en P. Vaessen, "Design of High-frequency Fast-rise Pulse Modulators for Lifetime Testing of Dielectrics", *IEEE Transactions on Dielectrics and Electrical Insulation*, p. 1–1, 2023.

[46] E. KONTOS, "Protection of Multiterminal HVDC Grids based on Modular Multilevel Converters", proefschrift, Delft University of Technology, 2018.

[47] P. N. Joshi en S. Dadaso Patil, "Improving low voltage ride through capabilities of grid connected residential solar PV system using reactive power injection strategies", in *2017 International Conference on Technological Advancements in Power and Energy (TAP Energy)*, 2017, p. 1–3.

[48] High Voltage Amplifiers and Piezo Drivers, Available Online: https://www.acalbfi.com/nl/technologies/power-supplies/high-voltage-power-supplies/high-voltage-amplifiers-and-piezo-drivers [Accesed on 25 November 2023].

[49] L. Lorenz, "Semiconductor Power Devices: Physics, Characteristics, Reliability", *IEEE Power Electronics Magazine*, jrg. 6, nr. 1, p. 86–87, 2019.

[50] F. A. Dragonas, G. Neretti, P. Sanjeevikumar en G. Grandi, "High-Voltage High-Frequency Arbitrary Waveform Multilevel Generator for DBD Plasma Actuators", *IEEE Transactions on Industry Applications*, jrg. 51, nr. 4, p. 3334–3342, 2015.

[51] S. A. Saleh, B. Allen, E. Ozkop en B. G. Colpitts, "Multistage and Multilevel Power Electronic Converter-Based Power Supply for Plasma DBD Devices", *IEEE Transactions on Industrial Electronics*, jrg. 65, nr. 7, p. 5466–5475, 2018.

[52] C. Davidson, J. Vodden en J. Snazell, "A new test circuit for operational testing of HVDC valves", 2019.

[53] P. Lei, Y. Mingtian, L. Geqi, Z. Qiaogen en H. Kun, "A high voltage multi level arbitrary waveform generator for insulation testing", *IEEE Transactions on Dielectrics and Electrical Insulation*, jrg. 26, nr. 2, p. 405–411, 2019.

[54] F. Briz, M. Lopez, A. Rodriguez en M. Arias, "Modular Power Electronic Transformers: Modular Multilevel Converter Versus Cascaded H-Bridge Solutions", *IEEE Industrial Electronics Magazine*, jrg. 10, nr. 4, p. 6–19, 2016.

[55] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga en R. Teodorescu, *Design, control, and application of modular multilevel converters for HVDC transmission systems*. John Wiley & Sons, 2016.

[56] J. E. Huber en J. W. Kolar, "Volume/weight/cost comparison of a 1MVA 10 kV/400 V solid-state against a conventional low-frequency distribution transformer", in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, p. 4545–4552.

[57] A. Alesina en M. Venturini, "Solid-state power conversion: A Fourier analysis approach to generalized transformer synthesis", *IEEE Transactions on Circuits and Systems Ii: Analog and Digital Signal Processing*, 1981.

[58] A. Lesnicar en R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range", in *2003 IEEE Bologna Power Tech Conference Proceedings,*, deel 3, 2003, 6 pp. Vol.3-.

[59] K. Ilves, L. Harnefors, S. Norrga en H.-P. Nee, "Analysis and Operation of Modular Multilevel Converters With Phase-Shifted Carrier PWM", *IEEE Transactions on Power Electronics*, jrg. 30, nr. 1, p. 268–283, 2015.

[60] A. Hassanpoor, S. Norrga, H.-P. Nee en L. Ängquist, "Evaluation of different carrier-based PWM methods for modular multilevel converters for HVDC application", in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, p. 388–393.

[61] D. Ronanki en S. S. Williamson, "Single Carrier-Based Pulse Width Modulator for Modular Multilevel Converters", in *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2018, p. 1–6.

[62] F. Zhou, Q. Xu, A. Luo e.a., "Carrier dynamic overlapping switching frequency optimal pulse width modulation method for modular multilevel converters", *Journal of Modern Power Systems and Clean Energy*, jrg. 6, nr. 6, p. 1306–1318, 2018.

[63] A. Dekka, B. Wu, N. R. Zargari en R. L. Fuentes, "A Space-Vector PWM-Based Voltage-Balancing Approach With Reduced Current Sensors for Modular Multilevel Converter", *IEEE Transactions on Industrial Electronics*, jrg. 63, nr. 5, p. 2734–2745, 2016.

[64] D. Ronanki en S. S. Williamson, "A Simplified Space Vector Pulse Width Modulation Implementation in Modular Multilevel Converters for Electric Ship Propulsion Systems", *IEEE Transactions on Transportation Electrification*, jrg. 5, nr. 1, p. 335–342, 2019.

[65] A. Dekka, B. Wu en N. R. Zargari, "A Novel Modulation Scheme and Voltage Balancing Algorithm for Modular Multilevel Converter", *IEEE Transactions on Industry Applications*, jrg. 52, nr. 1, p. 432–443, 2016.

[66] Z. Li, P. Wang, H. Zhu, Z. Chu en Y. Li, "An Improved Pulse Width Modulation Method for Chopper-Cell-Based Modular Multilevel Converters", *IEEE Transactions on Power Electronics*, jrg. 27, nr. 8, p. 3472–3481, 2012.

[67] W. van der Merwe, P. Hokayem en L. Stepanova, "Analysis of the N-Cell Single Phase MMC Natural Balancing Mechanism", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, jrg. 2, nr. 4, p. 1149–1158, 2014.

[68] K. Ilves, L. Harnefors, S. Norrga en H.-P. Nee, "Predictive Sorting Algorithm for Modular Multilevel Converters Minimizing the Spread in the Submodule Capacitor Voltages", *IEEE Transactions on Power Electronics*, jrg. 30, nr. 1, p. 440–449, 2015.

[69] S. Fan, K. Zhang, J. Xiong en Y. Xue, "An Improved Control System for Modular Multilevel Converters with New Modulation Strategy and Voltage Balancing Control", *IEEE Transactions on Power Electronics*, jrg. 30, nr. 1, p. 358–371, 2015.

[70] Z. Du, L. M. Tolbert, J. N. Chiasson en B. Ozpineci, "Reduced Switching Frequency Active Harmonic Elimination for Multilevel Converters", *IEEE Transactions on Industrial Electronics*, jrg. 55, nr. 4, p. 1761–1770, 2008.

[71] Q. Tu en Z. Xu, "Impact of Sampling Frequency on Harmonic Distortion for Modular Multilevel Converter", *IEEE Transactions on Power Delivery*, jrg. 26, nr. 1, p. 298–306, 2011.

[72] P. Hu en D. Jiang, "A Level-Increased Nearest Level Modulation Method for Modular Multilevel Converters", *IEEE Transactions on Power Electronics*, jrg. 30, nr. 4, p. 1836–1842, 2015.

[73] D. Ganeshpure, "Modular Multilevel Converter (MMC) based High Voltage Test Source: Demonstration of a proof of concept with a mathematical model and simulation study for arbitrary wave shapes generation", 2018.

[74] D. A. Ganeshpure, L. C. C. Heredia, M. G. Niasar, P. Vaessen, T. B. Soeiro en P. Bauer, "Analysis of Partial Discharge Behaviour under Staircase-based Sinusoidal Voltage Waveforms", in *2020 IEEE 3rd International Conference on Dielectrics (ICD)*, IEEE, 2020, p. 894–897.

[75] K.-B. Park, R. M. Burkart, B. Agostini en T. B. Soeiro, "Application of 1.7-kV 700-A SiC LinPak to Optimize LCL Grid-Tied Converters", in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, 2019, p. 1–7.

[76] T. B. Soeiro, K.-B. Park en F. Canales, "High voltage photovoltaic system implementing Si/SiC-based active neutral-point-clamped converter", in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, p. 1220–1225.

[77] Second order systems, Available Online: https://www.et.byu.edu/ tom/classes/436/ClassNotes/Class20(Second-Order).pdf [Accesed on 31 May 2021].

[78] A. Shekhar, T. B. Soeiro, Z. Qin, L. Ramírez-Elizondo en P. Bauer, "Suitable Submodule Switch Rating for Medium Voltage Modular Multilevel Converter Design", in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, p. 3980–3987.

[79] Power Semiconductor 2020 - 2021 Product Catalog, Available Online: https://www.ixys.com/Documents/Selectorguide.pdf [Accesed on 27 May 2021].

[80] V. Pala, E. Brunt en J. Casady, Simplifying power conversion with medium voltage SiC MOSFETs, Available Online: https://www.wolfspeed.com/downloads/dl/file/id/860/product/0/simplifying_power_conversion_with_medium_voltage_sic_mosfets.pdf [Accesed on 10 May 2021].

[81] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors en T. Jonsson, "VSC-HVDC Transmission with Cascaded Two-level Converters", in *Cigré session*, 2010, B4–B110.

[82] M. Zygmanowski, B. Grzesik en R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter", in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, p. 1–10.

[83] A. Shekhar, L. B. Larumbe, T. B. Soeiro, Y. Wu en P. Bauer, "Number of Levels, Arm Inductance and Modulation Trade-offs for High Power Medium Voltage Grid-Connected Modular Multilevel Converters", in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, 2019, p. 1–8.

[84] C. Oates, "Modular Multilevel Converter Design for VSC HVDC Applications", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, jrg. 3, nr. 2, p. 505–515, 2015.

[85] A. Hassanpoor, L. Ängquist, S. Norrga, K. Ilves en H.-P. Nee, "Tolerance Band Modulation Methods for Modular Multilevel Converters", *IEEE Transactions on Power Electronics*, jrg. 30, nr. 1, p. 311–326, 2015.

[86] Y. Wu, T. B. Soeiro, A. Shekhar, J. Xu en P. Bauer, "Virtual Resistor Active Damping with Selective Harmonics Control of LCL-Filtered VSCs", in *2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)*, 2021, p. 207–214.

[87] B. C. Kuo en D. C. Hanselman, *Matlab tools for control system analysis and design*. Prentice-Hall, Inc., 1994.

[88] "IEC 61000-2-4: Electromagnetic compatibility (EMC) - Part 4: Compatibility levels in industrial plants for low-frequency conducted disturbances", 2017.

[89] J. Dannehl, M. Liserre en F. W. Fuchs, "Filter-Based Active Damping of Voltage Source Converters With *LCL* Filter", *IEEE Transactions on Industrial Electronics*, jrg. 58, nr. 8, p. 3623–3633, 2011.

[90] X. Wang, F. Blaabjerg en P. C. Loh, "Virtual RC Damping of LCL-Filtered Voltage Source Converters With Extended Selective Harmonic Compensation", *IEEE Transactions on Power Electronics*, jrg. 30, nr. 9, p. 4726–4737, 2015.

[91] S. Leitner, M. Yazdanian, S. Ziaeinejad, A. Mehrizi-Sani en A. Muetze, "Internal Model-Based Active Resonance Damping Current Control of a Grid-Connected Voltage-Sourced Converter With an LCL Filter", *IEEE Transactions on Power Systems*, jrg. 33, nr. 6, p. 6025–6036, 2018.

[92] D. Pan, X. Ruan, C. Bao, W. Li en X. Wang, "Capacitor-Current-Feedback Active Damping With Reduced Computation Delay for Improving Robustness of LCL-Type Grid-Connected Inverter", *IEEE Transactions on Power Electronics*, jrg. 29, nr. 7, p. 3414–3427, 2014.

[93] Y. Wu, A. Shekhar, T. B. Soeiro en P. Bauer, "Voltage Source Converter Control under Distorted Grid Voltage for Hybrid AC-DC Distribution Links", in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, deel 1, 2019, p. 5694–5699.

[94] Y. Li, H. Pang, M. Kong, J. Lu, K. Ji en G. Tang, "Compensation control and parameters design for high frequency resonance suppression of MMC-HVDC system", *CSEE Journal of Power and Energy Systems*, jrg. 7, nr. 6, p. 1161–1175, 2021.

[95] J. Ma, X. Wang, F. Blaabjerg, L. Harnefors en W. Song, "Accuracy Analysis of the Zero-Order Hold Model for Digital Pulse Width Modulation", *IEEE Transactions on Power Electronics*, jrg. 33, nr. 12, p. 10 826–10 834, 2018.

[96] Y. Wu, T. B. Soeiro, A. Shekhar, J. Xu en P. Bauer, "Virtual Resistor Active Damping with Selective Harmonics Control of LCL-Filtered VSCs", in *2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)*, 2021, p. 207–214.

[97] M. Tran, A. Kuwana, H. Kobayashi e.a., "Design of Active Inductor and Stability Test for Passive RLC Low Pass Filter", in *10th Int. Conf. on CCSEA*, deel 10, 2020, p. 203–224.

[98] E. Jury, "A simplified stability criterion for linear discrete systems", *Proceedings of the IRE*, jrg. 50, nr. 6, p. 1493–1500, 1962.

[99] D. A. Ganeshpure, T. B. Soeiro, M. G. Niasar, P. Vaessen en P. Bauer, "Design Trade-Offs of Modular Multilevel Converter-Based Arbitrary Wave Shape Generator for Conventional and Unconventional High Voltage Testing", *IEEE Open Journal of the Industrial Electronics Society*, jrg. 2, p. 584–605, 2021.

[100] P. L. Francos, S. S. Verdugo, H. F. Álvarez, S. Guyomarch en J. Loncle, "INELFE — Europe's first integrated onshore HVDC interconnection", in *2012 IEEE Power and Energy Society General Meeting*, 2012, p. 1–8.

[101] T. Heath, P. R. Green, M. Barnes en D. Kong, "Design, construction and testing of a modular multilevel converter with a distributed control architecture", in *15th IET International Conference on AC and DC Power Transmission (ACDC 2019)*, 2019, p. 1–6.

[102] S. P. Teeuwsen, "Modeling the Trans Bay Cable Project as Voltage-Sourced Converter with Modular Multilevel Converter design", in *2011 IEEE Power and Energy Society General Meeting*, 2011, p. 1–8.

[103] B. Xia, Y. Li, Z. Li e.a., "Decentralized Control Method for Modular Multilevel Converters", *IEEE Transactions on Power Electronics*, jrg. 34, nr. 6, p. 5117–5130, 2019.

[104] W. Li, L.-A. Grégoire en J. Bélanger, "A Modular Multilevel Converter Pulse Generation and Capacitor Voltage Balance Method Optimized for FPGA Implementation", *IEEE Transactions on Industrial Electronics*, jrg. 62, nr. 5, p. 2859–2867, 2015.

[105] M. Hochberg, M. Sack, D. Herzog, A. Weisenburger en G. Mueller, "Design Validation of a Single Semiconductor-Based Marx-Generator Stage for Fast Step-Wise Arbitrary Output Waveforms", *IEEE Transactions on Plasma Science*, jrg. 46, nr. 10, p. 3284–3290, 2018.

[106] Typhoon HILL Specifications, Available Online: https://www.typhoon-hil.com/ [Accesed on 7 March 2023].

[107] S. Subramaniam, "Implementation of Control for MMC-Based Arbitrary Wave Shape Generator in the OPAL-RT Simulator", 2021.

[108] PWM Modulator, Available Online: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/pwm_modulator.html?hl=pwm%2Cmodulatore [Accesed on 7 March 2023].

[109] Typhoon HILL SPCs Details, Available Online: https://ticket.typhoon-hil.com/kb/faq.php?id=184 [Accesed on 7 March 2023].

[110] J. Wu, "Effects of Transients on High Voltage Cable Insulation", 2020.

[111] "IEC 62895, High Voltage Direct Current (HVDC) power transmission", 2017.

[112] S. Alapti, K. Johansson, M. Sjoberg, M. Klang, A. Abbasi en M. Saltzer, "Transient Over Voltage Testing of Cable Systems in MMC-HVDC Links: A Concept Study Including Verification", *CIGRE Session*, 2022.

[113] M. Hochberg, M. Sack, D. Herzog e.a., "A fast modular semiconductor-based Marx generator for driving dynamic loads", *IEEE Transactions on Plasma Science*, jrg. 47, nr. 1, p. 627–634, 2018.

[114] T. B. Soeiro, E. Mengotti, E. Bianda en G. Ortiz, "Performance Evaluation of the Body-Diode of SiC Mosfets under Repetitive Surge Current Operation", in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, deel 1, 2019, p. 5154–5159.

[115] C. Ionita, M. Nawaz, K. Ilves en F. Iannuzzo, "Short-circuit ruggedness assessment of a 1.2 kV/180 A SiC MOSFET power module", in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, p. 1982–1987.

[116] T. Basler, J. Lutz, R. Jakob en T. Brückner, "Surge current capability of IGBTs", in *International Multi-Conference on Systems, Signals & Devices*, 2012, p. 1–6.

[117] S. Yin, Y. Gu, S. Deng, X. Xin en G. Dai, "Comparative Investigation of Surge Current Capabilities of Si IGBT and SiC MOSFET for Pulsed Power Application", *IEEE Transactions on Plasma Science*, jrg. 46, nr. 8, p. 2979–2984, 2018.

[118] J. Schoiswohl, "Linear mode operation and safe operating diagram of power-MOSFETs", *Infineon Technologies AG: Munich, Germany*, 2017.

[119] N. Mohan, T. M. Undeland en W. P. Robbins, *Power electronics: converters, applications, and design*. John wiley & sons, 2003.

[120] B. J. Baliga, *Fundamentals of power semiconductor devices*. Springer Science & Business Media, 2010.

[121] L. Zhang, S. Guo, X. Li, Y. Lei, W. Yu en A. Q. Huang, "Integrated SiC MOSFET module with ultra low parasitic inductance for noise free ultra high speed switching", in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, p. 224–229.

[122] F. Denk, K. Haehre, S. Eizaguirre Cabrera e.a., "RDS (on) vs. inductance: comparison of SiC MOSFETs in 7pin D2Pak and 4pin TO-247 and their benefits for high-power MHz inverters", *IET Power Electronics*, jrg. 12, nr. 6, p. 1349–1356, 2019.

[123] Z. Chen, D. Boroyevich en J. Li, "Behavioral comparison of Si and SiC power MOSFETs for high-frequency applications", in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, p. 2453–2460.

[124] Process Enhancements Increase IGBT Efficiency for Motor Drive Applications, Available Online: https://www.digikey.be/nl/articles/process-enhancements-increase-igbt-efficiency-for-motor-drive-applications [Accesed on 07 August 2023].

[125] Comparison of SiC MOSFET and Si IGBT, Available Online: https://toshiba.semicon-storage.com/info/application_note_en_20200817_AKX00087.pdf?did=69799 [Accesed on 07 August 2023].

[126] W. Jiang, X. Wang, J. Yuan e.a., "Compact pulsed power and its industrial applications", in *2009 IEEE Pulsed Power Conference*, 2009, p. 1–10.

[127] F. H. Kreuger, "Industrial High Voltage Volume II: 4. Co-ordinating, 5. Measuring, 6. Testing", 1992.

[128] A. Voß, M. Gamlin en A. Haefely Test, "Superimposed Impulse Voltage Testing on extruded DC-Cables according IEC 62895", 2017.

[129] A. Marzoughi, R. Burgos en D. Boroyevich, "Active Gate-Driver With dv/dt Controller for Dynamic Voltage Balancing in Series-Connected SiC MOSFETs", *IEEE Transactions on Industrial Electronics*, jrg. 66, nr. 4, p. 2488–2498, 2019.

[130] T. Modeer, S. Norrga en H.-P. Nee, "High-Voltage Tapped-Inductor Buck Converter Utilizing an Autonomous High-Side Switch", *IEEE Transactions on Industrial Electronics*, jrg. 62, nr. 5, p. 2868–2878, 2015.

[131] D. Rothmund, "10 kV SiC-Based Medium-Voltage Solid-State Transformer Concepts for 400 V DC Distribution Systems", proefschrift, ETH Zurich, 2018.

[132] G. Rizzoli, L. Zarri, J. Wang, Z. Shen, R. Burgos en D. Boroyevich, "Design of a two-switch flyback power supply using 1.7 kV SiC devices for ultra-wide input-voltage range applications", in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, p. 1–5.

[133] O. S. Senturk, T. Maerki, P. Steimer en S. McLaughlin, "High voltage cell power supply for modular multilevel converters", in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, p. 4416–4420.

[134] D. Cottet, F. Agostini, T. Gradinger e.a., "Integration technologies for a medium voltage modular multi-level converter with hot swap capability", in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, p. 4502–4509.

[135] T. Modeer, S. Norrga en H.-P. Nee, "High-Voltage Tapped-Inductor Buck Converter Utilizing an Autonomous High-Side Switch", *IEEE Transactions on Industrial Electronics*, jrg. 62, nr. 5, p. 2868–2878, 2015.

[136] L. He, K. Zhang, J. Xiong, S. Fan en Y. Xue, "Low-Frequency Ripple Suppression for Medium-Voltage Drives Using Modular Multilevel Converter With Full-Bridge Submodules", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, jrg. 4, nr. 2, p. 657–667, 2016.

[137] DC to DC converter, PV15-27B12R3, Available Online: https://www.mornsun-power.com/html/pdf/PV15-27B12R3.html [Accesed on 30 December 2022].

[138] K. Shi, F. Shen, D. Lv, P. Lin, M. Chen en D. Xu, "A novel start-up scheme for modular multilevel converter", in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, p. 4180–4187.

[139] B. Li, D. Xu, Y. Zhang e.a., "Closed-Loop Precharge Control of Modular Multilevel Converters During Start-Up Processes", *IEEE Transactions on Power Electronics*, jrg. 30, nr. 2, p. 524–531, 2015.

[140] B. Li, Y. Zhang, D. Xu en R. Yang, "Start-up control with constant precharge current for the modular multilevel converter", in *2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, 2014, p. 673–676.

[141] A. Grid, "HVDC-VSC: transmission technology of the future", *Alstom Grid*, jrg. 1, p. 13–17, 2011.

[142] D. A. Ganeshpure, T. B. Soeiro, M. G. Niasar, P. Vaessen en P. Bauer, "Modular Multilevel Converter-based Arbitrary Wave shape Generator used for High Voltage Testing", in *2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)*, 2021, p. 124–131.

[143] Stability Pathfinder Webinar, Available Online: https://www.nationalgrideso.com/document/150301/download [Accesed on 29 November 2023].

[144] R. Pietsch, U. Stephan, M. Felk en T. Steiner, "Development tests, type tests, factory acceptance tests and on-site tests using modular and mobile DC test systems", *CIGRE-IEC 2019 Conference on EHV and UHV (AC & DC)*, 2019.

[145] P. Wang, A. Cavallini en G. C. Montanari, "Characteristics of PD under square wave voltages and their influence on motor insulation endurance", *IEEE Transactions on Dielectrics and Electrical Insulation*, jrg. 22, nr. 6, p. 3079–3086, 2015.

[146] B. Florkowska, J. Roehrich, P. Zydroi en M. Florkowski, "Measurement and analysis of surface partial discharges at semi-square voltage waveforms", *IEEE Transactions on Dielectrics and Electrical Insulation*, jrg. 18, nr. 4, p. 990–996, 2011.

[147] M. Florkowski, P. Błaszczyk en P. Klimczak, "Partial discharges in twisted-pair magnet wires subject to multilevel PWM pulses", *IEEE Transactions on Dielectrics and Electrical Insulation*, jrg. 24, nr. 4, p. 2203–2210, 2017.

[148] P. Seri, G. C. Montanari en R. Hebner, "Partial discharge phase and amplitude distribution and life of insulation systems fed with multilevel inverters", in *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, IEEE, 2019, p. 1–6.

LIST OF PUBLICATIONS

JOURNAL PUBLICATIONS:

- **D. A. Ganeshpure**, T. B. Soeiro, M. G. Niasar, P. Vaessen and P. Bauer, "Design Trade-Offs of Modular Multilevel Converter-Based Arbitrary Wave Shape Generator for Conventional and Unconventional High Voltage Testing,ïn IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 584-605, 2021.

  Best Energy Paper Award (Second prize) By TU Delft Power Web Institute 2023

- **D. A. Ganeshpure**, T. B. Soeiro, M. Gagic, M. G. Niasar, P. Bauer and P. Vaessen, "Demonstration of Scalable Series-Connected Submodule of Modular-Multilevel-Converter- Based Arbitrary Wave Shape Generator Used for High-Voltage Testing From Off-the-Shelf Component,ïn IEEE Open Journal of the Industrial Electronics Society, vol. 4, pp. 371-386, 2023.

- **D. A. Ganeshpure**, T. B. Soeiro, M. Gagic, M. G. Niasar, P. Bauer and P. Vaessen, “Design of Hybrid Configurations of Modular Multilevel Converter and Marx Generator to Generate Complex Waveforms for Dielectric Testing of Grid Assets”, (Revision is submitted in IEEE Open Journal of the Industrial Electronics Society)

- Y. Zang, M. G. Niasar, **D. A. Ganeshpure**, et al, "Partial Discharge Behavior of Typical Defects in Power Equipment Under Multilevel Staircase Voltage,ïn IEEE Transactions on Dielectrics and Electrical Insulation, vol. 29, no. 4, pp. 1563-1573, Aug. 2022

CONFERENCE PUBLICATIONS:

- **D. A. Ganeshpure**, L. C. C. Heredia, M. G. Niasar, P. Vaessen, T. B. Soeiro and P. Bauer, "Analysis of Partial Discharge Behaviour under Staircase-based Sinusoidal Voltage Waveforms,"2020 IEEE 3rd International Conference on Dielectrics (ICD), Valencia, Spain, 2020, pp. 894-897

- **D. A. Ganeshpure**, T. B. Soeiro, M. G. Niasar, P. Vaessen and P. Bauer, "Modular Multilevel Converter-based Arbitrary Wave shape Generator used for High Voltage Testing,"2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC), Gliwice, Poland, 2021, pp. 124-131

- **D. A. Ganeshpure**, A. P. Soundararajan, T. B. Soeiro, M. G. Niasar, P. Vaessen and P. Bauer, "Comparison of Pulse Current Capability of Different Switches for Modular Multilevel Converter-based Arbitrary Wave shape Generator used for Dielectric Testing of High Voltage Grid Assets,"2022 24th European Conference on Power

Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. 1-11

- **D. A. Ganeshpure**, T. Batista Soeiro, M. G. Niasar and P. Vaessen, "The Control Stage of a Modular Multilevel Converter-based Arbitrary Wave shape Generator for Dielectric Testing of High Voltage Grid Assets,"2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia), Jeju Island, Korea, Republic of, 2023, pp. 2226-2233

- X. Zhou, **D. A. Ganeshpure**, T. B. Soeiro, M. G. Niasar, Y. Wu, and P. Vaessen, "Implementation of Active Damping Control Methodology on Modular Multilevel Converter (MMC)-Based Arbitrary Wave Shape Generator Used for High Voltage Testing", in 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023

- G. Yu, M. G. Niasar, **D. Ganeshpure**, T. B. Soeiro and P. Bauer, "A Transformer Isolated Driving Method for SiC MOSFETs with a Constant Negative Off Voltage,"2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC), Gliwice, Poland, 2021, pp. 39-45

ACKNOWLEDGEMENTS

As I navigated the typically solitary journey of a PhD, I feel incredibly fortunate to have been surrounded by a supportive network of individuals who have generously contributed to my journey in various ways. Here, I want to express my gratitude to all those who played a pivotal role in my academic pursuit.

I would like to extend my sincere gratitude to my Promoter, *Peter Vaessen*, for having faith in my ability to undertake a challenging PhD topic. Throughout this journey, you have been an unwavering source of support, offering freedom and numerous opportunities to develop my personal and technical skills. Your contagious enthusiasm and insightful feedback on my papers and presentations have been invaluable. Thank you for being an inspiring guide and mentor. In addition, I would like to express my gratitude to my other Promoter, *Pavol Bauer*, for skillfully steering my research project in the right direction and providing invaluable support to sustain my work in the Power Electronics lab. I am thankful for your guidance and support, which have been instrumental in my growth as a researcher.

Thiago, I consider myself incredibly fortunate to have been under your supervision. Your mentorship has played a pivotal role in shaping my technical skills and boosting my confidence in power electronics. I extend my heartfelt gratitude for the extensive discussions on steering my research project, the collaborative efforts in debugging the lab setup, and the detailed feedback you've generously provided on my papers. Your passion for power electronics is truly inspiring, and I am sincerely thankful for your guidance. *Mohamad*, I am extremely grateful for your constant support during the thesis work with your critical thinking while planning research work or debugging the lab setup. Your remarkable enthusiasm for helping and guiding your students is commendable, and I feel fortunate to have benefited from your assistance in finalizing my thesis work in Delft.

Since my PhD project has collaborated with KEMA labs (previously known as DNV GL), I deeply appreciate the guidance I have received, especially during the initial phase of my research. *Cees*, you have been pivotal in my decision to pursue this PhD. Your extensive knowledge of HV testing and HV power electronics immensely helped in many stages of the PhD. *Benjamin*, your discipline and strong technical background in HV testing have helped me plan the work properly and motivated me to perform PD measurement setup. *Aditya, Mircea and Sjoerd*, your insights into HV testing have significantly enhanced my practical understanding of commercial HV testing, laying the foundation for this thesis. *Nadew and Hong*, thank you for introducing me to the KEMA lab facility and sharing your valuable insights into HV testing.

During my PhD, a significant portion of my time was dedicated to working on various test setups. I am immensely grateful for the invaluable support from the ESP Lab staff; they were instrumental in finishing the experimental work from this thesis in time. *Bart*,

I appreciate your practical insights into power electronics hardware development, especially in the challenging 3 kV MV SM setup. *Joris*, your expertise in OPAL-RT and control hardware greatly expedited the troubleshooting process (especially when my company supervisor visited me in 2020). *Harry*, I am thankful for your generous attitude and assistance, particularly in navigating the complexities associated with the scaled-down prototype of MMC. *Mladen*, your indispensable help in building PCBs, your presence in the lab and your continuous supervision were instrumental in finalizing the 3 kV MV SM demonstrator within the time frame. Thank you, *Remko*, for being an invaluable mentor and facilitating a rich learning experience in the lab. *Luis*, collaborating with you on PD measurement setup for the ICD conference paper was insightful and rewarding. *Radek*, I am grateful to you for recruiting me for the Smit transformer testing project, which led me to pursue a PhD in the high voltage technology group. *Paul*, your quirky way of teaching students is unique, and I would like to thank you for sharing your vast practical knowledge about HV testing. *Wim*, thank you for always being so caring and helpful in developing setups. *Gert*, thank you for your help in developing the typhoon-hil setup and the HV inductor building and testing. Thank you, *Imke*, for your support in the HV lab and for sharing your practical knowledge about commercial HV testing.

Beyond my official supervisors, I am fortunate to have received assistance from various faculty members within the DCE&S and HVT groups. *Aditya*, your guidance on MMC and the generous lending of your hardware setup played a crucial role in swiftly completing the scaled-down prototype experiments. Armando, thank you for your support in understanding HV testing requirements and developing the PD measurement setup. *Jianning*, your expertise in OPAL-RT significantly contributed to the control hardware work from this thesis. *Babak*, I am grateful for your valuable insights on my PhD topic, which have been beneficial since my master's thesis. *Chris*, thank you for your insights on HV testing and insulation coordination.

Sharmila and *Marieke*, thank you for arranging so many practical aspects of PhD so we can focus on delivering the research work. Special thanks to *Sharmila* for being a patient listener and offering your support during the personal struggles in the final year of PhD.

I got excellent guidance from many senior PhD students during my initial PhD days. A special appreciation goes to *Minos* for presenting the topic of MMC so captivatingly that I chose it as my master's thesis and PhD focus. While our paths did not cross in a collaborative setting, the impact of your introduction to MMC resonates throughout my work. I extend my sincere gratitude to *Niels, Udai, Faizal, Soumya,* and *Pavel* for their invaluable guidance about power electronics hardware setups and many other small hick-ups. *Jiayang*, thank you for sharing your knowledge about superimposed testing and lending your PD measurement setup after you finished it; it helped me gain experimental results much faster. *Fabio*, thank you for sharing your knowledge on PD testing in simple words and supporting PhDs tremendously. *Alessandro* and *Guillermo*, thank you for your cheerful welcome to the high voltage group and for helping with practical aspects of the lab. All your shared knowledge and advice were instrumental in navigating the complexities of doctoral research.

PhD is not just about developing technical expertise, but it is also a journey to discover yourself. I want to express my heartfelt gratitude to *Claartje* for accompanying me on the journey of discovering my true nature and wholeheartedly embracing it. Your support has been pivotal in helping me enjoy the PhD process, preventing any moments of breakdown on my part.

I have had an excellent opportunity to collaborate with various MSc students who contributed significantly to this thesis topic and helped me learn many things technically and proved hugely beneficial for my personal development. Thank you *Getssy, Guangyao, Stella, Sandhyaa, Swaminathan, Ajeeth, Nitish, Xiaochuan*, and *Jiantong* for your hard work and fun chat during stressful times. Even though I was not officially involved in the thesis project of *Suraj, Philip* and *Ashutosh*, I had fun working with you and learned many things from you. Besides MSc students, collaboration with a guest PhD student, *Yiming* was very fruitful. You picked up the PD measurement setup quickly, generating a very good Journal paper.

As per the phrase "Misery loves company", I am very fortunate to share this PhD journey with many PhDs who have been extremely kind to help me stay sane and did not get bothered by my questions neither in the office nor the lab. *Farshid*, we started the PhD journey on the same day. Even though our PhD topic was completely different, I enjoyed our coffee room discussions, which can go to a deeper philosophical level. *Francesca, Marco, Wenli*, and *Wiljan*, you started your PhDs just a few months ahead of me, and I can not thank you enough for sharing all the tips and tricks before various milestones in the PhD journey. *Ibra*, even if you joined a few months later than me, you finished it early and shared many tips for form B approval. *Marco, Francesca, Wenli, Yang, Lyu, Calvin, Sachin*, and Guangyao, we have spent many hours in the power electronics lab together, sharing many equipment and components too. I am so grateful to share that time, and I have learned so many things from you. *Tianming*, your knowledge of magnetics for high-frequency applications is amazing. Thank you for being so helpful with building and testing the HV inductor. Next, I want to mention *Gautam*, you supported me towards the end of my PhD when I was in my lowest moment to finish the experimental results for a journal paper. Thank you very much.
Sachin and *Guangyao*, it is amazing to have you both in the neighbouring room to borrow any equipment or share any worries about the experimental setup. *Hitesh*, it was nice to have you in the lab when I was almost towards finishing the experiments as a company in the power electronics lab. *Djurre*, it was nice to share the office the other half-time. I started in your office and then moved. Your love for Indian food is amazing; I hope you are still cooking. *Christian* and *Weichuan*, thank you for creating a fun office environment in the new office, and it was nice to have sweets shared among us. *Joel*, thank you for rescuing me from Sohrab in the lunch discussion. I still struggle to keep up with Zumba; I hope to get better after the defence. *Miad*, it was fun to hand over the MMC setup to you. I wish you all the best with it. *Rohan* and *Siddhesh*, you were Marathi language buddies. *Siddhesh*, even when you joined a bit later, we had many coffee discussions and were there for each other; language helps a lot. Discussing *Gangwei, Robin, Junjie*, and *Faezeh* with you all in the power electronics lab was nice. *Lucia* and *Yunhe*, we hardly had any common work stream in Delft. It is amazing to work in Shell

together. *Reza* and *Zhengzhao*, we did not work so much together in Delft. However, it is exciting to work together in your SST design now in the FlexH2 project. *Alejandro*, it was amazing to have you in our department for a while, I wish you the best for your PhD. *Sohrab*, I kept your name as last here to show that I almost forgot you. I am happy you are continuing the AWG work, and I wish you the best of luck. Compared to many PhDs, we are unlucky who could not travel a lot. Still, I have had a nice trip to Aalborg with *Nakisa*, to Germany (EPE Europe) with *Sachin* and *Guangyao* and to South Korea (ECCE Asia) with *Yang, Lyu, Guangyao, Robin Jianning, Gautham*, and *Zian*.

Lucia, I am so grateful to you for explaining the job role in Shell and referring me internally. Also, *Francesca*, thank you very much for your push to apply for the position even when I was not sure. Having a job offer 7 to 8 months in advance was quite helpful to have a deadline to finish the PhD. Let's have a lot more fun together after the defence.

I started working in Shell's grid connection technology department even when I had not even started with my thesis draft. My team lead,*Paul* and *Jackie* and all my team members, *Yin, Songda, Lucia, Robert, Vinay, Digvijay, Dan*, and *Renata*, are incredibly supportive in terms of managing/sharing my workload and being very kind in listening to my PhD struggles. I could not have finished the thesis so fast without a friendly work environment there.

Henk, I am highly inspired by your electrical machines classes and your overall attitude towards research. I always remember your advice that you can get answers to your questions by asking the right questions. The Indian education system does not foster curiosity. However, I was fortunate to have three teachers (*Gurus*) in India who introduced "curiosity"to me early. Hence, I could pick it up here in Delft relatively fast. First, I am incredibly grateful to my father for sowing that seed of curiosity from my childhood. *Mangeshkar Sir*, you cultivated that seed during a two-year coaching program at IITPK Institute in Pune, and I can not thank you enough for that. BITSian days were a whole new ground for me, surrounded by talent from all over India and exposing me to many similar-minded students with whom I can grow together. During my limited work experience in India, *Badave Sir*, you identified my interest in fundamental studies and offered projects with similar themes with constant technical and emotional support to manage my first commercial job.

Nitish, you are my family in the Netherlands with whom I do not need to pretend anything. We can have an honest discussion about any topic in the World and learn from each other. You have played a crucial role in my decision to pursue a PhD, and your support has helped me survive it and enjoy many moments together with *Berta*. *Kalpit*, it is so nice that we started the tradition of "Rakshabandhan"here, and I love the special bond we created in the Netherlands and hoping to spend more time with you and *Abhilasha* together. *Adwait*, I never imagined we would become close friends again after Tata Motors. I am so glad you found the PhD position in Delft, and you have been such a significant emotional support to survive different PhD stresses. We have had many fun gaming nights with Kishan. *Kishan*, you are another constant in our Delft Katta group, whose stud attitude is almost envious. I appreciate your support throughout the PhD and am excited to enjoy more in Shell's Hague campus. *Anshuman, Nidarshan*, and *Ravi*,

it is always amazing to host you in the house and enjoy different Indian festivals. *Sanjay* and *Satish*, we have had a fantastic time together even after our masters, and it was a wonderful trip to Italy. *Sachin* and *Supriya*, I can not thank you enough for bringing India to the Netherlands by starting up the grocery shop and keeping the quality and variety of items top-notch. *Kaivalya dada*, your NL experience helped my parents to get comfortable with my choice of TU Delft. *Devashri tai*, thank you for welcoming me to your house when I was loneliest in this country. All of you make it joyful to stay 6000 km away from my family for an extended period.

Pallavi, you are my saviour in almost all emergencies. I can share anything with you, and you can lend me a listening ear with excellent solicited advice. You will hit me to say thank you here, so I will say we are there for each other. *Riya*, you are another person with whom I can talk about anything and get huge support. *Shikha*, even when you are in the USA, we are a message away from each other for any needs, and I love your passion for fitness. *Ishwari*, I love the special bond and understanding we have for each other. *Biki, Gaurav, Gurumurti, Komal, Shridevi, Ruchi, Sayali, Shruti, Shalaka, Nutan*, you are staying on various continents, and I am grateful to have you as a robust support system.

Anuja, I could not have done the wedding shopping without your support. Thank you for caring for so many things in India; it greatly reduced my stress so that I could focus on my PhD work. I look forward to spending quality time in Germany or the Netherlands. *Aditya dada* and *Nikita vahini*, thank you for taking care of Baba during the surgery. Thank you for making it special when we visit Mumbai. *Sheela moushi, Alka moushi, Gawande Kakaji, Asha moushi*, thank you for always insisting to become financially independent since childhood. You ladies are my biggest cheerleaders.

Mazi Aai, you have given me a bit of your patience, tenacious and sensitive nature, which is a great package to become a good researcher. *Maze baba*, I always say you are a visionary for your generation. I can not thank you enough for creating a rational and logical environment while I am growing up. I am incredibly grateful to you both for being the best parents to a girl child in India, providing me with all possible opportunities and investing a large portion of money in getting me into Delft. This thesis is payback to that.

Shriram, you have been my *Dhruv tara* in terms of support, being with me throughout the process of my PhD. You have been among very few people who can accept me the way I am, even when I have problems doing so. Thank you for making my career, health and mental well-being a priority. I am so happy with the house and life we built together in the Netherlands. You missed many travel and fun activities due to my PhD and COVID. Let's have a lot more fun after I earn my PhD.

BIOGRAPHY

Dhanashree Ashok Ganeshpure was born in Akola, India in 1993. She received a bachelor's degree in electrical and electronics engineering from BITS Pilani University, Goa, India, in 2015 and a master's degree (cum laude) in electrical power engineering from Delft University of Technology, Delft, The Netherlands, in 2018. In her engineering career from 2011 to 2018, she did many internships and research projects at various industries and research institutes. From March 2019, she pursued a PhD degree with the HV Technology Group and DC Energy Conversion & Storage (DCE&S) group at the Delft University of Technology on the topic of Design of a High Voltage Arbitrary Wave Shape Generator for Dielectric Testing. Currently, she works in Shell as an electrical engineer to facilitate the integration of various renewable energy sources into the grid using novel power electronics solutions.