Single Grain Si TFTs for RF and 3D ICs

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Single-grain Si TFTs have been fabricated using accurate 2D location control of large Si grain with the μ -Czochralski process. TFTs fabricated inside the crystalline islands of 6 μm show a mobility ($600\text{cm}^2/\text{Vs}$) as high as that of the SOI counterpart, despite of the low-temperature ($<350^\circ\text{C}$) process. By applying a tensile stress into the grain, the mobility surpasses even the SOI counterparts. We have succeeded in controlling crystallographic orientation of the location-controlled Si grains as well, by combination of metal induced lateral crystallization and the micro-Czochralski process. Owing to the orientation control, uniformity in device properties approaches to the level of the SOI counterpart. Using the high performance single-grain (SG) Si TFTs, we have fabricated RF amplifier. The cut-off frequency of the RF device is 5.5 GHz with a channel length of 1.5 μm . We have even succeeded to stack two SG-TFT layers with which CMOS inverters were fabricated. This will open several new applications in TFTs of RF wireless communication, 3D-ICs with device level integration, and flexible electronics.

Introduction

Thin-film transistors (TFTs) using amorphous silicon (a-Si) and low-temperature poly-Si (LTPS) have been successfully applied to active matrix liquid crystal displays (AMLCDs). The basic structure, a thin semiconductor layer on an insulating substrate, dates from the very first invention of the field effect transistor (1). Because it was difficult to obtain a single-crystalline Si layer on a insulator, MOSFETs have chosen the bulk crystalline Si substrate for the channel material. As oppose to the ULSI, the TFTs had been facing difficulty in obtaining the single-crystalline channel material for a long time. This has restricted TFT's performance and the applications as shown in Fig. 1 .

The situation, however, has been changed by recent advancement of laser crystallization process. Advanced laser crystallization process (2-5) has made it possible to control location of a large Si grains two dimensionally and to position the TFT channel inside the grain, thereby realizing "single-grain Si TFTs". It should be noted that lateral grain growth process only, e.g., SLS (6), CLC (7), SELAX (8), cannot full fill the conditions. The single-grain (SG) Si TFTs obtained by the μ -Czochralski process (2,5) exhibits indeed a field effect mobility as high as the SOI counterpart. With a maximum process temperature of 350°C , transistors that were fabricated inside the location-controlled grains exhibit mobility of $600\text{ cm}^2/\text{Vs}$ (9) and $280\text{ cm}^2/\text{Vs}$ for electrons and holes, respectively. As shown in Fig. 1, the high performance SG-TFTs are going to open new markets for the TFTs, such as RF wireless display, 3D-ICs with monolithic integration and flexible electronics. The 3D-ICs in particular will break-through problems of ULSI

with the conventional 2D-ICs, i.e., the long transit delay in the interconnects and the limited integration of different functions. The 3D-ICs with SG-TFTs will be the ultimate cooperation between TFT and ULSI, which originated from the single invention.

In this paper we first review the μ -Czochralski process, which realizes the 2D location-control of large Si grains. We show that defects inside the location controlled Si islands are only coincident site lattice (CSL) boundaries, which are not electrically active. TFTs fabricated inside the crystalline islands of 6 μm show a mobility ($600\text{cm}^2/\text{Vs}$), despite of the low-temperature ($<350^\circ\text{C}$) process. By applying a tensile stress into the grain, the mobility surpasses even that of the SOI counterparts. We show also a way to control crystallographic orientation of the location-controlled Si grains and to minimize variation of the properties. We will also demonstrate RF low-noise amplifier and CMOS inverters with stacked two SG-TFT.

Figure 1. Various system applications as a function of TFT mobility.

Single-grain Si TFTs

The μ -Czochralski (grain-filter) process

Excimer laser crystallization (ELC) is a well-established method for producing poly-Si films on non-heat resistant substrates (10). As shown in Fig. 1, applications of the poly-Si TFTs are limited to display driver due to the low field-effect mobility of around $100\text{ cm}^2/\text{Vs}$. The low mobility is due to potential barriers formed at random grain boundaries (GBs) which trap carriers. Lateral grain growth (6-8) can reduce the effect of GBs, however, the mobility is still limited due to inevitable incorporation of the random GBs. If the location of the silicon islands is controlled, the position of the channel region of FETs can also be aligned inside the island. The 2D location control of Si grains can eliminate inclusion of the random GBs and enables formation of single-grain (SG) TFTs.

A few have been reported the 2D location control of Si grains and formation of TFTs inside those (2-5). Among them the μ -Czochralski (grain-filter) process (2,5) has advantages in terms of the wide energy density window for obtaining the 2D location control, and alignment accuracy over the other methods.

Figure 2. Schematic for the μ -Czochralski (grain-filter) process and single-grain Si TFTs

As depicted in Fig. 2, the μ -Czochralski process has a locally increased thickness of the a-Si film in a cavity (grain-filter) in a substrate. Upon excimer-laser irradiation, the grain filter melts non-completely, whereas the surrounding melts completely. During vertical growth of the pre-existing seeds in the grain filter, occlusion of grains occurs reducing the number of growing grains. By increasing the aspect ratio, only single grain can be filtered out from many pre-existing fine grains. Experimental details for forming the grain-filter structure has been described elsewhere (2,9). The hole diameter is approximately 100 nm. A 250 nm thick a-Si film is then deposited by LPCVD. A single 56ns long XeCl (308nm) excimer-laser light irradiates the Si surface.

Figure 3. SEM image and EBSD mapping of a grid of location-controlled grains showing the CSL GBs $\Sigma 3$ (gray) and $\Sigma 9$ (black) and the random GBs (white).

A SEM image of location-controlled grains is shown in Fig. 3. Si grains of 6 μm per side are thereby obtained in predetermined positions via the μ -Czochralski process. Although random grain boundaries are absent inside the grains, some of the grains have planar defects which are generated from either the center of the film or from the rim of the grain filter. Electron backscattering diffraction (EBSD) analysis of such grains showed that the planar defects generating from the holes are mainly $\Sigma 3$ coincidence site lattice (CSL) boundaries, followed by $\Sigma 9$ and $\Sigma 27$. TEM (11) revealed that the boundary plane for the $\Sigma 3$ CSL boundary is predominantly $\{111\}$.

Local electrical characterization of the grain boundaries

We have directly measured local electrical properties of the CSL boundaries in the location-controlled Si islands (12). Figure 4 depicts a scanning capacitance microscopy (SCM) image and C-V measurement at a random GB, $\Sigma 9$ and $\Sigma 3$ CSL boundaries. It should be noted that the grain filter diameter is widened to 500 nm to intentionally incorporate the random GBs. Three crosses represented in the SCM image indicate points used for the C-V measurements. One can find the clear difference on C-V characteristics between the curves for the three boundaries. Capacitance drop as well as slope is largest for the curve of $\Sigma 3$, and smaller for $\Sigma 9$, followed by one for random GBs. The smaller drop and slope of the C-V curve indicate higher density of state within forbidden gap and/or tails of conduction band. This result suggests that the $\Sigma 9$ boundary has trap states and electrical activity; however, it is much less than that of random boundary. Similar results have been obtained with SSRM (13). Those are consistent with our ab-initio atomic modeling result; $\{111\}\Sigma 3$ CSL boundary has no states in the forbidden gap and at band tails due to absence of irregular coordination at the boundary.

Figure 4. SCM mapping image of the location control of grains (left) and C-V curves (right) at various CSL boundaries indicated in the image.

TFT fabrication and characterization

TFTs are fabricated inside the location-controlled grains obtained by the μ -Czochralski process. For investigation of the CSL boundary effect, we have varied position of channel inside the grain, as depicted in the inset of Fig 5 (b). We have shifted the TFT channel position in the island with respect to the grain filter. In X position, the radially grown CSL boundary is parallel to the carrier flow direction. Possible CSL boundary of Y is perpendicular to the carrier flow direction.

Detailed TFT process was explained elsewhere (2,9). Here we describe it shortly. After the location-control of the grain, the Si film is patterned into islands. The transistors are designed so that a single grain covers the entire channel area of a TFT. A 120 nm thick ECR-PECVD SiO_2 layer was deposited as a gate insulator at room temperature and annealed in water vapor at 333°C. The source and drain are implanted with P ion ($1 \times 10^{16} \text{ cm}^{-2}$), which is then activated by the excimer-laser annealing. The maximum process temperature is 350°C. As a reference, TFTs on silicon on insulator (SOI) with $\{100\}$ orientation were fabricated with the same process conditions.

The SG TFTs at the X position give an average field-effect mobility μ_{FEe} of $597 \pm 101 \text{ cm}^2/\text{Vs}$, which is well comparable with that of the SOI ($727 \pm 18 \text{ cm}^2/\text{Vs}$). The high

mobility of the SG-TFTs is attributed to the fact that the carriers do not experience the CSL boundaries because it is parallel to the direction of current flow. The mobility is slightly lower and the standard deviation is higher than those of the SOI-TFTs. Those are because surface orientation of the location-controlled grains is random from which some orientations reduce the mobility due to higher effective mass. When the channel position is at Y, the average μ_{FE} decreases to 528 cm^2/Vs , which is caused by the CSL boundaries perpendicular to the carrier flow. This leads to the conclusion that reduction of the mobility by the presence of the CSL boundaries is only 10% in average.

Figure 5. Transfer characteristics (a) and field-effect mobility of n-channel single-grain Si TFTs fabricated at various positions in the location controlled grain.

High mobility by tensile strain

Figure 6 shows the electron field-effect mobility as a function of energy density of excimer-laser. It can be seen that the mean mobility about 600 cm^2/Vs is obtained for a wide range of energy densities. The single-grain is obtained in the wide energy density range where only melt depth changes in the depth of the grain filter. The wide energy density window is a very important advantage of the μ -Czochralski process.

At the highest energy density, we obtained a mean field-effect mobility of as high as 883 cm^2/Vs for the X position. The peak value at the X position even reaches to 1200 cm^2/Vs . A mean field-effect mobility value of 814 cm^2/Vs and 773 cm^2/Vs is obtained for C and Y position, respectively. For p-channel SG-TFTs, we achieved a mean field-effect mobility value of 320 cm^2/Vs , with a peak value of 500 cm^2/Vs . Those extremely high mobilities can be explained by the tensile stress in the location-controlled grains (14) with a combination of high quality Si/SiO₂ interface. At the highest energy, the grain filter finally completely melts (11) during the excimer-laser irradiation. Since there is no seed left in the grain filter, the molten-Si should wait for the spontaneous nucleation to solidify. The molten-Si solidifies with much higher solidification velocity due to the severe undercooling, compared to the non-complete melt condition, building up the

tensile stress in the grain. With micro-Raman technique, we have measured a tensile stress of 1.2 GPa in the grain.

Figure 6. Mobility of the SG-TFT as a function of laser energy density for various positions in the grain

Location and Orientation Control of Si Grains

Both location- and orientation-control of Si grains has been achieved by combining metal induced lateral crystallization (MILC) and the μ -Czochralski process (15). The former controls crystallographic orientation of grains to (110) which is used as a seed crystal whereas the latter controls the 2D location of the grains. After the grain-filter formation, Ni was deposited by sputtering and patterned into an island which has a distance of 20 μm away from the grain filter. After pre-annealing and removing the Ni, the sample was further annealed at 600°C for 4h in N_2 ambient for the MILC. Figure 7(a) shows the SEM image after the MILC. The MILC poly-Si, which has needle-like grains, covered the whole matrix of grain-filter. The total length of lateral crystallization was 67 μm . From EBSD, it was found that the MILC has surface crystallographic orientation of (110). Then the thin layer of the MILC poly-Si, which is contaminated by the Ni, was etched away. In the grain filter the MILC poly-Si was still left. After that, a new 250nm thick a-Si layer was deposited by sputtering and the sample was crystallized with one shot of excimer-laser at a substrate temperature of 450°C.

Figure 7. (a) SEM image of Si right after the MILC process and (b) EBSD mapping of the location-controlled grains after laser crystallization of the sample (a).

After the laser crystallization, we found that the location-controlled grains with $6\mu\text{m}$ was obtained and the needle shape defects disappeared. Fig.7 (b) shows EBSD mapping of eight location-controlled grains after the laser crystallization. We see that all the eight grains have (110) orientation with a few CSL boundaries at the edge which indicate the (110) MILC poly-Si has grown into the grain-filter and has seeded the laser crystallization inheriting the orientation. It was found that Ni concentration 10^{17} cm^{-3} was decreased below the SIMS detection limit ($5 \times 10^{15}\text{ cm}^{-3}$) owing to the removing process of the MILC poly-Si layer.

Using the orientation controlled grains, the SG TFTs were fabricated with the similar process described above, except for the change of gate SiO_2 into 100 nm ICP-PECVD SiO_2 . The channel width and length was both $2\mu\text{m}$. Table I shows statistical variation of the TFT characteristics values. With the grain orientation control, we have obtained an average mobility of $507\text{ cm}^2/\text{Vs}$ with a standard deviation of $32\text{ cm}^2/\text{Vs}$ (6%), which is a great improvement compared to without the orientation control (25%) (9) and approaches to that of the SOI counterpart (2%). The average mobility is decreased due to the (110) orientation, whereas the uniformity is improved owing to orientation control. It should be noted that we have recently succeeded to control the orientation into (100) as well (16).

Table I. SG-TFTs by μ -Czochralski with/w.o the MILC process

	μ -Czochralski only	MILC + μ - Czochralski	SOI
Average mobility (cm^2/Vs)	579	507	727
Deviation (cm^2/Vs)	139 (25%)	32 (6%)	18(2%)
S (V/dec)	0.45	0.24	0.18
V_{th} (V)	1.55	0.4	1.1
Leakage current (A)	$5.70\text{E-}12$	$2.45\text{E-}12$	$1.7\text{E-}12$

RF and 3D integrated circuits

RF Circuits

Using the high performance SG-TFTs we have designed and fabricated RF low-noise amplifier with on-chip spiral inductors to demonstrate its potential for realizing high performance analog/RF applications on large-area substrates (17). Here a modified BSIM-SOI transistor model (18) is used for the simulation of the SG-TFTs. The BSIM-SOI with a proper modification of the mobility is carried out. The model has been verified for n- and p-channel DC and low frequency AC conditions as well by comparison with measurement results.

Firstly n- and p-channel SG-TFTs and passive devices have been integrated and measured over the frequency range of 50 MHz to 20 GHz. Multiple finger devices achieve a sufficient transconductance g_m and gain at RF with a low extrinsic gate resistance of Al. Fig. 8(a) shows the chip photograph of a SG-TFT with 20 fingers and 5 rows used for RF characterization and, Fig. 8(b), a cascode dual-gate SG-TFT amplifier. Fig. 9(a) reveals that the measured current gain-bandwidth f_T is 5.45 GHz at a drain-source V_{DS} and gate-source V_{GS} bias of 3 V ($I_D=25\text{mA}$ and $g_m=16\text{mS}$). The corresponding unity-power-gain frequency f_{max} is 11.45 GHz. With the unity gain bandwidths in the 5 to 6 GHz range, amplifiers can be designed in the sub-1 GHz frequency range with expected gains in the 10s of dBs.

Figure 8. Chip photographs of SG-TFT with total width of 500 μm and $L = 1.5 \mu\text{m}$ used for RF characterization (a) and cascode amplifier with dual-gate SGTFTs(b).

Figure 9. Measured RF performance of the SG-TFT: h_{21} and G_{MAX} as function of frequency (a) and measured and simulated S-parameters (b) of the cascode RF amplifier.

A cascode dual-gate SG-TFT amplifier has been designed with 433 MHz ISM band. The cascode amplifier circuit uses as load a 35 nH on-chip inductor designed for a resonance of 430 MHz. As shown in Fig. 9(b), the 433 MHz ISM amplifier achieves useful RF gain of more than 10 dB, good isolation (better than 25 dB), and IIP3 of 10 dBm. Such an amplifier could also be used in the IF stage of a transmitter or receiver operating at a higher RF front-end frequency.

3D-ICs

We have fabricated CMOS inverters with two layer SG-TFTs (19). The process flow starts with formation of bottom SG-TFT layer using the μ -Czochralski process. For the gate oxide, we deposited a 30 nm-thick ICP enhanced CVD oxide at 250°C. The bottom layer is then passivated by ILD of 2 μ m thick PECVD-TEOS oxide grown at 350°C. The ILD was planarized using the CMP with the final roughness of 5 nm (20). Processing the second layer starts also with the μ -Czochralski process and follows the same process flow as the bottom layer. After planarization of a passivation SiO_2 by etch-back process, vias were opened to connect the bottom layer to pads and also to top layer contacts. Finally interconnects are formed by a 675 nm-thick Al sputtered at 350°C. The maximum process temperature is 350°C after the a-Si LPCVD step.

Figure 10. TEM image of inverter with two-layer SG-TFTs.

Figure 10 shows a cross-sectional TEM image of the fabricated CMOS inverters with two SG-TFT layers having the nMOS on top of the pMOS. The cross section is made along the gate width direction. The width of the pMOS is 4.2 μ m, twice of the nMOS. The gate length of both transistors is 1.5 μ m. The single-grain channels, the poly-Si gates at the both bottom and top layers, and the common connection can clearly be seen.

Figure 11. Transfer characteristics of the bottom (a) and top (b) SG TFTs

Figure 11 shows transfer characteristics of the bottom (a) and top (b) SG TFTs for the both n- and p-channels. A good matching of the transfer characteristics between the top and bottom transistors is observed. The top layer field-effect mobilities are 565 and 159 cm^2/Vs and bottom layer mobilities are 393 and 141 cm^2/Vs , for the nMOS and pMOS devices, respectively. Table II summarizes the average characteristic values for different devices on each layer. The devices on the top layer have slightly better performance than those on the bottom layer. This is due to process variations such as better gate patterning

Figure 12. Output characteristics of CMOS inverters with pMOS at the (c) top and (d) by dry etching for the top. Main reason for the higher leakage of the bottom layer TFTs, is accidental over-etching of Si island during gate patterning process.

The output characteristics of the CMOS inverters are also shown in Figure 12. Two different CMOS configurations have been made: nMOS on pMOS (a) and pMOS on nMOS (b). For both types, switching voltage of the inverters lies around 2 V. The input signal swings from 0 to 5 V, and so does the output. The first type shows slightly better inverter characteristics, which may be due to the process variation.

Table II. TFT properties of the two layer SG-TFTs.

Type of device	Mobility [cm^2/Vs]	S [mV/dec]	V _{th} [V]	I _{d(max)} [A]	I _{leak} [A]
nMOS Top	565	245	-0.8	2.19E-05	5.39E-12
pMOS Top	159	95	-2.4	1.61E-05	2.80E-13
nMOS Bottom	393	280	-0.6	1.81E-05	1.49E-10
pMOS Bottom	141	151	-2	1.43E-05	9.2E-13

Conclusions

We demonstrated that the single-grain Si TFT through the μ -Czochralski process can be used for wireless RF and also 3D ICs. Large Si grains of 6 μm per side are thereby obtained in predetermined positions via the μ -Czochralski process. We show that defects inside the location controlled Si islands are only CSL boundaries of which the most is electrically inactive. The SG Si TFTs fabricated inside the crystalline islands of 6 μm show a high mobility ($600\text{cm}^2/\text{Vs}$) in a wide energy density window, despite of the low-temperature ($<350^\circ\text{C}$) process. By applying a tensile strain into the grain, the mobility surpasses even that of the SOI counterparts. We have succeeded in controlling

crystallographic orientation of the location-controlled Si grains, by combination of metal induced lateral crystallization and the μ -Czochralski process. Owing to the (110) surface orientation control, uniformity of device properties approaches to the level of the SOI counterpart. We also demonstrated the RF low-noise amplifier and the 3D-ICs by CMOS inverters with stacked two SG-TFT. The cut-off frequency of the RF device is 5.5 GHz with a channel length of 1.5 μ m. This will open several new applications in TFTs of RF wireless communication, 3D-ICs with device level integration.

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