MICROMACHINING TECHNIQUES USING LAYERS GROWN IN AN EPITAXIAL REACTOR
MICROMACHINING TECHNIQUES USING LAYERS GROWN IN AN EPITAXIAL REACTOR

PROEFSCHRIFT

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1.1 Small is beautiful

In the last decades an enormous improvement in price to performance ratio and functionality has taken place in the field of electronics. Palm top organizers exhibit more computing power than the bulky room filling computers of the end of the 1950’s, which used electron tubes. The invention of the transistor made it possible to down-scale electronic circuits. Printed circuit boards (PCB) with discrete transistors, resistors, capacitors, and coils offered lower power consumption, smaller size and better performance than their tube containing predecessors. The next step was the development of the integrated circuit, on which several transistors and passive components are miniaturized in a way which is similar, but many times smaller, than in PCB electronics. Again power consumption, price, and performance were considerably increased.

At the same time the complexity of both the devices and their production process has increased considerably. Large investments are needed to develop complex electronic circuits such as microprocessors, together with their fabrication processes. The reason why it is possible to sell these products at low prices, is that they are batch fabricated. Once the
fabrication process is developed and the lay-out of the chip is completed, the development costs of a device can be divided by a very large number of chips. Circuits which perform completely different functions are made by just changing the lay-out of the photomasks which are used in the fabrication process.

The development process of electronic circuits has made it possible to manipulate electrical data in a very sophisticated way. Unfortunately, human beings are not capable to directly interact with these data, without the help of devices which translate data into a form which can be perceived by human senses. These translators are called sensors and actuators. A data processing unit consists of a sensor, which converts information into an electrical signal, electronics, which manipulates the information, and an output actuator, which interacts with the environment, or displays information.

One of the many systems which contain a sensor, read-out electronics, and an output actuator is an air bag system. In this case, the sensor is an acceleration sensor, which detects the deceleration of a car. The output of the electronics determines whether the air-bag is to be inflated or not, based on the deceleration information. In the above example, the main cost of the system is determined by the price of the sensor and air bag, and not by the electronics. Therefore, in order to reduce the price of the total unit, it is important to reduce the price of the sensing element. This could be done by making the sensor in the same batch fabrication process as the electronics.

1.2 Micromachining

The technique which enables the batch fabrication of mechanical sensors and actuators, in a process which is similar to electronics fabrication, is called micromachining. Miniature membranes, springs, masses, and other mechanical components, are fabricated using a combination of lithography and etching. The excellent mechanical properties of silicon, together with the availability of process equipment which was originally developed for electronics fabrication, make silicon an ideal material for the fabrication of miniature mechanical structures. Currently, silicon micromachining is widely used to fabricate low-cost sensors and actuators for high-volume markets. The increased functionality and performance of silicon sensors
also opens new possibilities to develop custom made, high performance devices, which can be sold at much higher prices, and lower volumes.

The first high volume application of silicon sensors were pressure sensors. Nowadays the majority of the world’s pressure sensing devices is fabricated around a micromachined silicon membrane. Silicon acceleration sensors, with applications in the automotive field such as air bag sensors, are sold in large quantities and at low prices. The addition of a self-test feature to these sensors has greatly improved the reliability of the air bag systems. Currently, considerable effort is being put into the development of miniature gyroscopes which are needed in the next generation of vehicle dynamic control. The stability of the “baby Benz”, for example, improved dramatically when a vehicle dynamic control system was implemented.

Micromachined actuators can be found in ink-jet printer heads. In this application a precise volume of a ink is transported to a piece of paper. A second example of a micromachined actuator is a micro-pump, which is part of an implantable device that is used to deliver precise volumes of drugs to a patient. A third example of a micromachined actuator is the DMD chip, which was developed by Texas Instruments. In this chip thousands of micro-mirrors modulate a light beam to form a color projection display.

1.3 Objective and organization of this thesis

The objective of the work presented in this thesis is to develop new micromachining techniques which combine the advantages of both bulk and surface micromachining, and to build sensors and actuators which demonstrate the capabilities of these new processes.

Chapter 2 will introduce the most important existing micromachining techniques. It will describe the basic process steps, and strong and weak points of the current micromachining techniques.

In chapter 3 the development of epi micromachining techniques will be presented. Epi micromachined structures are constructed of material which is grown in an epitaxial reactor. These layers can be either monocrystalline or polycrystalline (epipoly). Epi micromachining techniques combine the
advantages of surface- and bulk micromachining, while limiting their disadvantages.

The first epi micromachined demonstrator is an acceleration sensor which will be presented in chapter 4. In this chapter the basic theory, design considerations, and fabrication of these devices will be presented, together with a simple read-out circuit, which was needed to characterize the DC and AC performance of these devices.

Epi-micromachined thermal actuators and pressure sensors are presented in chapter 5. A simple theory about thermal actuators is developed, and used to analyze the performance of fabricated actuators. In order to further demonstrate the capabilities of the epipoly material, it will be shown that it is possible to fabricate piezoresistive pressure sensors in this layer.

Finally, in chapter 6, conclusions are drawn.
2.1 Introduction

The aim of this chapter is to briefly introduce the reader to the most well known micromachining methods which are based on silicon, or use a silicon substrate. This will put the work of the next chapters into perspective.

There are numerous methods to fabricate micro-mechanical structures in silicon and other materials. This chapter will give a brief overview of the most commonly used techniques, together with their advantages, and disadvantages. In section 2.2 the ‘traditional’ bulk silicon micromachining technique will be described, and section 2.3 introduces surface micromachining. In the next two sections, section 2.4, and section 2.5, two newer techniques will be described which open possibilities to form a whole new range of structures, namely bulk micromachining by dry etching and porous silicon micromachining. The last technique which will be described in this chapter is LIGA, which uses electroplating of thick metal layers to construct micromechanical structures and micromoulds. This section ends with a conclusion in section 2.7.
2.2 Wet anisotropic bulk micromachining

The oldest micromachining technique is bulk micromachining. In this technique, the silicon substrate is etched away to form micromechanical structures, such as membranes, which are an essential part of i.e. pressure sensors, surface acoustic wave devices, and thermal flowsensors. One of the first bulk micromachined devices is a pressure sensors which was fabricated by Honeywell in 1962 [2.1]. Other bulk micromachined structures which are mass produced are silicon accelerometers, where the silicon is used to form a seismic mass which is suspended by beams, which act as springs [2.2].

The fabrication of a piezoresistive silicon pressure sensor will be described to explain the most frequently used bulk micromachining technique. It is illustrated in figure 2-1.

![Piezoresistor formation](image)

![Interconnect](image)

![Membrane etching](image)

Fig. 2-1  Fabrication scheme of a piezoresistive pressure sensor.

The fabrication starts with a (100) silicon double-sided polished wafer. In its simplest form, four p-type piezoresistors are fabricated by implantation or diffusion of a p-type dopant such as boron in the n-type bulk or epitaxial layer. Then the piezoresistors are connected in a Wheatstone bridge configuration, using thin metal lines on oxide. These steps are standard IC fabrication steps. After the electrical part of the fabrication process is completed the micromachining process starts. On the back side of the wafer a square shaped hole is etched in a nitride or silicon oxide layer, which acts as an etch mask for the subsequent wet etching of the silicon wafer. Silicon etching is usually carried out using potassium hydroxide
(KOH) solutions. The silicon etch rate in KOH is dependent on the crystal orientation and <100> planes are etched much faster than <111> planes [2,3,2,4]. This results in etched cavities with 54.7° side walls with respect to the silicon surface.

*Etch stop techniques*

A crucial part in the fabrication of a bulk micromachined pressure sensor is the etching of the membrane. The sensitivity of the resulting pressure sensor depends strongly on the thickness of the membrane, and there are various methods to control this thickness.

The most straightforward and cheapest method for membrane thickness control is the timed etch stop. The wafers are etched in the etchant for a predetermined time. The thickness of the resulting membrane is determined by the starting thickness of the wafer and by the etch rate of the etchant. This technique is usually done in two steps. In the first step most of the bulk is etched away, and the resulting thickness is measured. From this measurement the current etch rate is calculated, together with the required etch time to obtain the target thickness. Advantages of this technique are the simple set-up, and the absence of the need for special etch-stop layers in the substrate. The disadvantage of this technique is the limited accuracy and non-uniformity of the resulting membrane thickness, and the need to measure the thickness of the membranes to determine the extra etch time, needed to obtain the target thickness.

Another method is electrochemically controlled etching (ECE) [2,5]. In this technique an n-type epitaxial layer is grown on top of a p-type substrate. During silicon etching this epitaxial layer is electrically connected to the positive clamp of a voltage source. The negative clamp is connected to a platinum counter electrode in the etchant. The etching of the silicon substrate stops when the depletion layer between the epitaxial layer and the bulk substrate is reached. With this technique the resulting membrane thickness can be controlled with a very high accuracy. Disadvantages of this method are the need of an epitaxial layer, an external power source, and special etch fixtures which increase production costs. Recently, a new technique was reported which utilizes an on-chip galvanic cell to generate the power which is needed to obtain an etch stop [2,6]. This promising technique does not need special etch fixtures, and is very interesting for the fabrication of silicon bulk micromachined devices.
Micromachining techniques

The last etch stop techniques which will be described here are based on chemical etch selectivity. The first of these techniques is the high boron etch stop method, which depends on a high decrease in the silicon etch rate when it is heavily doped with boron [2.7]. The University of Michigan has been very successful in the use of this technique to produce microprobes for nerve monitoring [2.8]. A disadvantage of this technique is the limited usefulness of the highly doped silicon. A low-doped stress-free piezoresistive sensor, for instance, cannot be produced using this technique, because of the high boron concentration which is needed for the etch stop. A second method is the use of a buried oxide layer under the epitaxial layer [2.9]. The etching stops at the interface between the silicon and the buried oxide layer. For this technique SIMOX (Separation through IMplantation of OXygen) wafers are commercially available. In these wafers oxygen is implanted at elevated temperatures. After high temperature annealing this implanted oxygen forms a silicon dioxide layer which is buried under a layer of monocrystalline silicon. With increasing use and production of these wafers the high price of these wafers is expected to reduce in the near future. An alternative to SIMOX wafers is the use of epitaxial lateral overgrown silicon which is grown over buried oxide islands [2.10]. This technique, however, is not straightforward and commercially unattractive. A new possibility is the use of an silicon-oxide-epipoly structure. This technique is discussed in chapter 5.

Wet silicon etchants and their characteristics

In the previous section KOH was used to etch the silicon for membrane formation. KOH is the most used etchant in bulk micromachining, but there are also alternatives which will be described here.

Etchants with similar etch characteristics as KOH [2.3,2.4], are EDP (ethylenediamine-pyrocatechol-water) [2.11], hydrazine [2.12, 2.13], and TMAH (tetra-methyl-ammonium-hydroxide) [2.14]. Each of these etchants etches silicon in an anisotropic way. The characteristics of these etchants are summarized in table 2-1 [2.15].

Of all the etchants listed in the table TMAH is the least hazardous. However, KOH is inorganic and easy for disposal. This, together with its high etch rate and good selectivity towards silicon nitride makes KOH the preferred silicon etchant in the pressure sensor industry.
2.2 Wet anisotropic bulk micromachining

<table>
<thead>
<tr>
<th>Etchant</th>
<th>Masking layer</th>
<th>anisotropy (100)/ (111)</th>
<th>SiO$_2$ etch rate (Å/hr)</th>
<th>SiN etch rate (Å/hr)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>KOH</td>
<td>SiO$_2$, SiN, Cr, Au</td>
<td>400:1</td>
<td>1700-3600</td>
<td>&lt;1</td>
<td>Not clean-room compatible</td>
</tr>
<tr>
<td>Hydrazine</td>
<td>SiO$_2$,SiN, most metals</td>
<td>16:1</td>
<td>100</td>
<td>&lt;10</td>
<td>highly toxic, explosive</td>
</tr>
<tr>
<td>EDP</td>
<td>SiO$_2$, SiN, Cr, Au</td>
<td>35:1</td>
<td>120</td>
<td>60</td>
<td>highly toxic</td>
</tr>
<tr>
<td>TMAH</td>
<td>SiO$_2$, SiN, Cr, Au</td>
<td>300:1</td>
<td>&lt;100</td>
<td>&lt;20</td>
<td>cleanroom compatible</td>
</tr>
</tbody>
</table>

Bulk micromachining is an excellent fabrication method for a range of applications. Some advantages of bulk micromachining over other micromachining methods are:

+ **In bulk micromachining the mechanical structures consist of monocrysaline silicon, which is an excellent mechanical material.**

+ **The well known piezoresistive effect of monocrysaline silicon allows the fabrication of sensors with piezoresistive read-out using a Wheatstone bridge. This results in very simple read-out circuitry, although the temperature dependency of the piezoresistive effect has to be taken into account.**

+ **Bulk micromachining is the most mature technique of all micromachining techniques, since it is the oldest technique used in mass production.**

There are several drawbacks in bulk micromachining using the anisotropic wet etchants mentioned above. The most important are the limited freedom of design and the relatively large size of the produced structures.
Micromachining techniques

- Due to the anisotropic etch characteristics of KOH structures with convex corners will be underetched rapidly. This underetching can be avoided by using special corner compensation structures but these consume considerable area. This imposes severe limits on the type of shapes that can be fabricated.

- The relatively large size of bulk micromachined structures is caused by the non vertical sidewalls which result from the anisotropic characteristics of the etchants. As a result the minimum side length of a square area needed to perforate a wafer is about 1.4 times larger than the wafer thickness. The thickness of wafers tends to increase with the ever increasing wafer diameters. As a result bulk micromachined devices become larger and etch times will increase when bulk micromachined devices are made on a larger substrate.

- In bulk micromachining the wafers must be processed from both the front and backside. For the alignment of front and backside masks special lithography equipment is needed.

- Bulk micromachined structures often have very high steps and even holes through the wafers. The holes make it difficult to handle the wafers in machines which use vacuum grippers for automatic wafer handling and the high steps often lead to photoresist step coverage problems during lithography.

2.3 Surface micromachining

The surface micromachining technique yields structures which are fabricated in material which is deposited on top of the wafer surface. An advantage of this method is the high freedom in design and the possibility to scale up to higher wafer diameters without the need to increase chip size, since the size of the structures is independent on the wafer thickness. The first surface micromachined device was reported in 1965 [2.16]. This paper reported on a CMOS transistor with free standing resonating metal gate. The first surface micromachined structures based on polysilicon construction material date from the 1980's [2.17, 2.18].

The fabrication of surface micromachined structures starts with a silicon wafer which may have electronic circuits already built-in. On this wafer a
sacrificial layer is deposited. Typically PSG (Phosphorous-Silicate-Glass) is used for this purpose since it has a very high etch rate and low deposition temperature [2.19]. Then this layer is patterned in such a way that holes are etched where the micromechanical structure needs to be anchored to the substrate. Subsequently, the construction layer is deposited and patterned. Doped polysilicon is usually used for this purpose since it is a conductor with good mechanical properties. In the last step, the sacrificial layer is etched away, leaving free-standing polysilicon structures [2.20]. For sophisticated structures up to five polysilicon layers have been stacked and patterned to form structures like micromotors [2.21]. The basic fabrication process is illustrated in figure 2-2.

**Sacrificial layers**

The purpose of a sacrificial layer is to form the air gap between the constructional layer and the substrate, and to define the anchor points to the substrate. A wide range of materials has been applied as sacrificial layer, such as aluminum [2.22], polysilicon [2.23], polymers [2.24], SOI oxide [2.25], thermal oxide [2.26], and deposited oxide [2.19]. In most surface micromachining processes PSG is used as a sacrificial layer. The ideal sacrificial layer has the following properties:

- Low deposition temperature. This is especially important when surface micromachining is performed as a post process on a wafer with built-in electronics. A high thermal
Micromachining techniques

budget would alter the characteristics of the electronics due to extra diffusion of the dopants.

- **High deposition rate.** A high deposition rate makes it economically viable to produce thick layers. The thicker the sacrificial layer, the lower the probability of sticking of the microstructures after the final sacrificial etch.

- **High etch rate.** A high etch rate makes it possible to fabricate large freestanding structures, without the need to perforate these structures with access holes for the sacrificial etchant.

**Construction layers**

Most of the requirements for construction layers are similar to those of the sacrificial layer. Materials reported as construction layers are polysilicon [2.27], silicon nitride [2.28], silicon carbide [2.29], aluminum [2.30], and oxide [2.31]. Polysilicon is mostly used as construction layer. A construction layer should have:

- **Low deposition temperature.** This is only important for surface micromachining processes which are carried out using a wafer in which contains electronics.

- **High growth rate.** A high growth rate makes it possible to grow thicker layers in a limited time. A thicker layer is less delicate in handling and gives the opportunity to produce devices which have larger electrical output signals.

- **High chemical resistance to the sacrificial etchant.** The structure should not deteriorate from the sacrificial etching process.

- **Low resistance.** For most applications the construction layer should be electrically conductive in order to be able to make electrical connections to the devices.

- **Low tensile stress and a low stress gradient.** Low tensile stress prevents problems associated with compressive stress, such as bi-stable operation (‘oil canning’), and sticking to the substrate. A low stress gradient is needed to avoid vertical curvature of fabricated structures.

Surface micromachining offers several advantages to the designer of microstructures. Here is a list of some of the advantages:
2.3 Surface micromachining

+ The shape of microstructures is not longer restricted to the limited number of shapes which can be made using bulk micromachining.
+ It is possible to use more than just one construction layer. This opens the possibility to fabricate complex multilevel structures, such as micromotors.
+ Since all process steps are done at the front-side of the wafer, no special double sided alignment is needed.
+ The area of the structures can be much smaller than the area of bulk micromachined structures, since no area is needed to etch trough a complete wafer.

Drawbacks of surface micromachining are caused by the limited thickness of the construction layer and by the properties of the construction layer itself:

- Typically the thickness of the sacrificial layer and construction layers are in the 0.5-2μm range. These thicknesses are a result of a trade-off between growth time, and desired thickness. This limits the mechanical ruggedness and maximum value of lateral capacitances which can be made with these processes.
- The low level signals resulting from surface micromachined structures make on-chip integration of read-out electronics often mandatory. This complicates the fabrication process, since all micromachining process steps must be compatible with the electronics process.
- The grain structure of polysilicon makes it a less ideal material than monocrystalline silicon.
- The properties of polycrystalline films are highly dependent on the processing parameters like deposition temperature, doping and annealing [2.32].
- The piezoresistive effect of polysilicon is much lower than the piezoresistive effect of monocrystalline silicon [2.33].
2.4 Bulk micromachining using dry etching

Nowadays, the once clear difference between surface and bulk micromachining has faded, due to the development of new dry etching techniques. In these techniques micromachined structures are fabricated in the top part of the silicon substrate. The fabricated structures are made of monocrystalline silicon and have the excellent mechanical quality of bulk micromachined parts, combined with the small feature size of surface micromachined structures. There are three different approaches which will be described here, namely the SCREAM / BSM processes, SOI processes and finally a process which uses a new generation of fast deep dry etching equipment.

2.4.1 SCREAM / BSM

Both SCREAM (Single Crystal Reactive Etching and Metallization) and BSM (Black Silicon Method) are completely dry processes. They both use a combination of isotropic and anisotropic etching steps. The SCREAM process, which was developed at Cornell University [2.34], starts with the deposition of an oxide masking layer. Then trenches are etched in the silicon using an anisotropic etch. After the desired depth is reached, the trenches are covered with a thin oxide layer, which is removed from the bottom by an anisotropic plasma etch. Now the trench is etched somewhat deeper using the original anisotropic silicon etch recipe, followed by undercutting of the structures using an isotropic plasma etch. Finally, the structure (with the oxide still present) is metallized in order to make electrical contacts to the various free standing parts. Short circuit between the separate parts of the structure does not occur due to the poor step coverage of sputtered aluminium. The process is described in figure 2-3.

![Trench etching and isotropic etching](image)

**Fig. 2-3  The SCREAM process [2.34].**

BSM, developed by the MESA institute [2.35], utilizes silicon on oxide wafers, and a metal masking layer. The important difference with
2.4 Bulk micromachining using dry etching

SCREAM is that the sidewall passivation is achieved in the plasma etcher. First, the upper silicon layer is etched anisotropically until the buried oxide is reached. A CHF\(_3\) plasma etch is used to etch the underlying oxide and deposit a fluorocarbon (FC) on the sidewall, which protects the sidewall during further etching, and also has a low surface tension to reduce sticking. Finally, an isotropic RIE etch removes the silicon from under the upper silicon resulting in the structure shown in figure 2-4.

![Diagram showing trench etching, sidewall passivation and buried oxide etching, and isotropic underetching.]

Fig. 2-4  *The BSM process [2.35].*

2.4.2 SOI wafers

The second method is very similar to traditional surface micromachining and uses silicon on insulator (SOI) wafers. Three methods to prepare SOI material are presented here. In the first method SIMOX wafers (Separation by IMplantation of OXygen) are used [2.9]. These are wafers in which oxygen is implanted in the bulk silicon at elevated temperature, followed by a high temperature anneal. This results in a silicon oxide layer which is buried under a thin layer of monocrystalline silicon. The thickness of the monocrystalline layer can be increased by epitaxial growth. An alternative to the SIMOX method is the use of BESOI wafers (Bonding and Etch back of Silicon On Insulator) [2.36]. In this technique a silicon wafer is bonded on an oxidized silicon wafer. One of the wafers is polished and etched back until the silicon on top of the oxide layer has the desired thickness. A third alternative, which combines the SIMOX and BESOI processes is the smart-cut process [2.37]. In this technique one wafer is oxidized and
implanted with hydrogen. This wafer is then fusion-bonded to a second wafer. During the high-temperature anneal of the bonding process the implanted wafer splits at the depth where the hydrogen atoms were implanted. After polishing this process yields an SOI wafer and a wafer which can be re-used for oxidation and hydrogen implantation.

A mask is applied on the SOI wafer, and the monocrystalline top layer is patterned by anisotropic dry etching. The structures are released by etching in an oxide etchant. Anchors are defined by large areas which will not be completely undercut in the time needed to free the moving structures. The various parts of the wafers are galvanically insulated from each other by the oxide which is left under the anchoring points. The process is described in figure 2-5.

![Starting SOI wafer](image)

![Anisotropic silicon etch](image)

![Sacrificial oxide etch](image)

Fig. 2-5  *The SOI process.*

### 2.4.3 Deep dry etching

The third method came with the development of fast anisotropic dry etching equipment. These processes rely on equipment which is capable to etch very deep trenches, with a very high aspect ratio, and good mask selectivity. The structures are typically 50-100μm thick, while the lateral dimensions are similar to those of surface micromachined structures. This makes it possible to fabricate large lateral capacitances on a small chip area.

The fabrication process described here circumvents problems associated with wet sacrificial etching and uses two wafers. In the first step trenches are etched in a carrier wafer to define the anchors of the mechanical structures. Then this wafer is oxidized and fusion bonded to a second
2.4 Bulk micromachining using dry etching

wafer. This wafer is polished back to the desired thickness of the mechanical structures. Then a deep-etch mask is aligned to the carrier wafer and the structures are etched until the structural wafer is completely etched through, leading to free standing structures, without the need for wet sacrificial etching [2.38, 2.39]. The process is described in figure 2-6.

![Diagram of MEMS fabrication using deep silicon etching, combined with wafer bonding](image)

The lateral capacitances of the resulting structures can be very high due to the high thickness and thus large area of the structures. Sticking during fabrication is not an issue since no sacrificial wet etch step is needed. Vertical sticking during operation is not a problem since the structures are very stiff in the vertical direction.

2.4.4 Comparison of dry etching techniques

The SCREAM / BSM, SOI, and deep silicon etching techniques each have their own advantages and disadvantages. In this sub section they will be compared using table 2-2:
Micromachining techniques

Table 2-2  Comparison of dry etching micromachining techniques.

<table>
<thead>
<tr>
<th>Property</th>
<th>SCREAM / BSM</th>
<th>SOI</th>
<th>Deep Si etching</th>
</tr>
</thead>
<tbody>
<tr>
<td>wet release etch?</td>
<td>no</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td>capacitances</td>
<td>medium-high</td>
<td>medium</td>
<td>very high</td>
</tr>
<tr>
<td>crystalline Si</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>electrically insulated</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>wafer bonding needed?</td>
<td>no</td>
<td>no/yes</td>
<td>yes</td>
</tr>
<tr>
<td>width of free structure</td>
<td>yes</td>
<td>not really</td>
<td>no</td>
</tr>
<tr>
<td>limited by underetch rate?</td>
<td>small</td>
<td>small</td>
<td>small</td>
</tr>
</tbody>
</table>

2.5 Porous silicon micromachining

In porous silicon micromachining, structures are fabricated using porous silicon as a sacrificial layer [2.40]. The mechanical layers can consist of silicon, silicon nitride, or any other layer which is not attacked by the porous silicon formation process. The advantage of porous silicon as sacrificial layer over deposited layers is that the sacrificial layer can be made much thicker than other sacrificial layers, and that no extra deposition step is needed if the substrate is used as sacrificial material. Due to its high surface area, porous silicon can easily be removed in diluted alkaline solutions like KOH or even photoresist developer.

Porous silicon is formed by anodic etching of silicon in HF or other fluoride containing solutions [2.41]. Under anodic bias silicon-silicon bonds are attacked by fluoride ions, resulting in the formation of a sponge-like structure. Porous silicon micromachining has the following advantages:

- The sacrificial layer can be very thick: This reduces parasitic capacitances between the mechanical structures and the substrate, and reduces the probability of vertical sticking of the devices.
Mechanical structures can be made of monocrystalline silicon without the need for wafer bonding or SIMOX wafers.

The shape of the etched structures is determined by the shape of doped regions and offers high flexibility.

Disadvantages of porous silicon are:

- For porous silicon formation electrical contact and an external power supply are needed. This complicates the fabrication process.
- Different parts of the structure are not electrically insulated since they are all connected via the substrate.
- The lateral underetch rate is comparable to the vertical underetch rate. This limits the width of the structures to be underetched.
- Thickness control of the porous silicon layer is not always easy. For many applications, however, this is not a problem.

A range of microstructures have been fabricated where porous silicon was used to increase the air gap in surface micromachining [2.42], and also for bulk micromachining [2.43, 2.44].

2.6 LIGA

LIGA (German Lithographic, Galvanik and Abformung) is a combination of X-ray lithography, electro-deposition, and moulding. Originally, the process was intended to produce moulds which can be used for mass production of micromachined injection moulded devices [2.45]. The basic fabrication steps are shown in figure 2-7 (this picture was found on the internet). The process starts with a conductive substrate on which a thick (up to 1 mm) photoresist layer is spun, typically PMMA. This photoresist layer is irradiated using X-rays and developed to define a mask with vertical sidewalls. Subsequently, a metal layer is grown using electroplating. Nickel is most commonly used for this purpose. Finally, the resist is stripped and the structure is ready to be used as a mould to mass produce microstructures, using an injection moulding technique.
Micromachining techniques

Later, the sacrificial LIGA process was derived from the original LIGA process. This process has similarities with surface micromachining: Firstly a sacrificial metal layer such as titanium is deposited on the wafer. Then thick photoresist is applied, exposed, and developed, followed by electroplating of a metal which is resistant against the sacrificial etchant, like nickel. Then the photoresist is removed and the sacrificial layer is etched, yielding released nickel structures. In this case the LIGA structure is the final goal and not a mould to build many copies of the same product.

Fig. 2-7  The LIGA process.

The LIGA technique can be used to produce high aspect ratio metal structures. Since all the processing steps are performed at low temperature the process is ideal as a post process module after electronics formation. LIGA can be a quite expensive technology due to the high cost of x-ray exposure of the PMMA resist. This is caused by the need for special masks which do not transmit X-rays and the X-ray exposing tool is very expensive. This is not a big problem when the LIGA structure is used as a mould to produce injection-moulded devices, but for sacrificial LIGA injection moulding is not possible. Recently a new process using EPON SU-8 resist has been developed [2.46]. This resist can be used in combination with UV-light exposure in a conventional contact aligner and makes the process much cheaper. A disadvantage of the SU-8 process is the lower attainable aspect ratio of the structures.
LIGA has the following advantages:

- The fabrication process is compatible with electronics processing as long as it is carried out after the electronics processing is complete.
- The high cost of X-ray lithography can be divided by a very large number of injection moulded parts.
- With EPON SU-8 resist thick structures can be made with acceptable aspect ratio and low cost.

Disadvantages of LIGA are

- The mechanical quality of the nickel structures is lower than their silicon counterparts.
- For electroplating each wafer needs to be connected to an external power source. This is labor intensive.

2.7 Conclusion

In this chapter a brief overview of several micromachining techniques has been given, together with their advantages and disadvantages. It is impossible to tell which of the techniques is the best one, since each technique has its own positive and negative aspects. For each application a technique has to be chosen which is the most suitable in the given situation, depending on freedom of design, cost of fabrication, and preferred read-out method.

2.8 References


2.8 References


Micromachining techniques

rations and great structural heights by synchrotron radiation and lithography, galvanoforming and plastic moulding (LIGA process)

3.1 Introduction

In this chapter the development of fabrication processes which use the epitaxial layer, or a layer grown in an epitaxial reactor, as a construction material is described. With the epitaxial reactor, it is possible to grow relatively thick monocristalline or polycristalline silicon layers in a limited time. The excellent uniformity of doping and thickness, together with their low mechanical stress values, make these layers an ideal material for the fabrication of micromechanical structures. Epi micromachined structures have the same shape as surface micromachined structures, and the only real difference between epi- and surface micromachining is the type of layer which is used as constructional layer. This layer is much thicker, and can be made of monocrystalline silicon. The removal of sacrificial material, and the subsequent drying process, can lead to the same problems as in conventional surface micromachining. This chapter starts with a description of the silicon epitaxy in which the epitaxial reactor and the chemistry are described. Subsequently, methods for sacrificial etching and drying of epi micromachined structures are described. Then the development of three epi-micromachining methods will be described. The first one is based on epitaxial lateral overgrowth.
The second one uses of porous silicon as a sacrificial layer. The third method uses epipoly as construction material. This method is less complicated than the previous ones, but yields polycrystalline structures.

3.2 Silicon epitaxy

Silicon epitaxy is a thermal chemical vapor deposition (CVD) process, in which a solid silicon layer is grown from a gas which contains silicon atoms. The goal of this section is to give the reader some basic knowledge about CVD processes and to introduce the reactor and chemistry which was used in the experiments described in this thesis. For a more in depth description of epitaxy the reader is referred to the literature [3.1, 3.2].

3.2.1 CVD reaction steps and growth rate

In CVD processes a thin layer of solid material is grown from a gaseous source. In CVD the following process steps, which are illustrated in figure 3-1, can be distinguished [3.1]:

a) Arrival of the reactants:

1. Bulk transport of reactants.
2. Reactant diffusion to the surface.
3. Adsorption, or chemisorption of the species at the surface.

b) Surface reaction:

4. Heterogeneous surface reaction catalyzed by the surface.
5. Surface diffusion.
7. Desorption of gaseous reaction products.

c) Reaction product removal:

8. Gaseous diffusion of reaction product away from the surface.
The growth rate of a CVD layer is determined by the slowest of all process steps. At low temperatures the reaction steps which occur at the wafer surface determine the growth rate, and the reaction is called surface reaction limited. When the temperature is raised, the reactions at the surface take place very quickly, and the growth rate is determined by the rate at which reactants can arrive at the surface, or the rate at which products can leave the surface. In this case the reaction is called mass transport limited [3.3].

3.2.2 Chemistry

The reaction system used in the experiments described in this thesis is a hydrogen-dichlorosilane-hydrogenchloride (H$_2$-DCS-HCl) system. DCS (SiH$_2$Cl$_2$) is a gas which consists of silicon atoms which are surrounded by two hydrogen and two chlorine atoms. The hydrogen is used as a carrier gas, and the HCl is used to clean the reaction chamber between depositions and can be added during deposition to enhance the selectivity of silicon growth, as will be described in section 3.4.

Alternatively to DCS, SiH$_4$, SiHCl$_3$ or SiCl$_4$ can be used as silicon source gases. The more chlorine in the source gas, the lower the growth rate, and the higher the quality of the grown layer. DCS is a good compromise between growth rate and layer quality.

During silicon growth the following overall reaction occurs [3.4]:

\[
\text{SiH}_2\text{Cl}_2 \leftrightarrow \text{Si} + 2\text{HCl}
\]  (3-1)

Since equation 3-1 is an equilibrium reaction addition of HCl to the source gas will shift the reaction to the left hand side, resulting in a lower silicon
growth rate. Silicon atoms which are incorporated in the crystal lattice are less reactive than silicon atoms which are not (yet) incorporated in the surface. Therefore the HCl selectively removes silicon atoms which are not (yet) bonded on the right spot in the crystal lattice, which enhances the layer quality.

3.2.3 The epitaxial reactor

The epitaxial reactor used in the experiments described in this thesis is an ASM Epsilon One reactor. This is a single wafer type reactor in which the wafers are heated by halogen lamps. In this reactor it is possible to assign a different recipe to each wafer, which is extremely convenient to study the influence of growth parameters on layer properties. The reaction chamber consists of a quartz rectangular tube in which a silicon carbide wafer susceptor is rotating. Reactants are supplied from one side of the chamber and flow horizontally over the wafer surface. At the other side of the chamber reaction waste is pumped away. With this reactor it is possible to grow at temperatures between 500 and 1200°C, at pressures between 20 Torr and atmospheric pressure. Figures 3-2 and 3-3 shows schematic drawings of the reactor. These figures shows the load-locks (1), wafer transfer (2) and process chamber (3).

![Diagram of epitaxial reactor](image)

**Fig. 3-2** Schematic drawing of the epitaxial reactor.
3.3 Sacrificial etching and sticking reduction

The last step in all surface and epi micromachining processes is the sacrificial etch step. In this step the sacrificial layer, which acts as a support and spacer for the structures, is removed, leaving them free standing. This step is rather critical, since attack of interconnect layers and sticking of the microstructures to the substrate can be severe problems in surface micromachining. In this section methods to prevent the attack of aluminum and sticking are discussed.

In the processes described here it is assumed that the sacrificial layer consists of silicon dioxide. This is not the case in the porous silicon epi micromachining process, but as the sacrificial etchants for all processes are based on hydrofluoric acid the method which are described here are valid for all micromachining processes described in this chapter. Sacrificial oxide is etched in two steps via [3.6]:

\[
\text{SiO}_2 + 2\text{H}_2\text{O} \rightarrow \text{Si(OH)}_4 \quad (3-2)
\]

\[
\text{Si(OH)}_4 + 4\text{HF} \rightarrow \text{SiF}_4 + 4\text{H}_2\text{O} \quad (3-3)
\]
Unfortunately the hydrofluoric acid also contains hydronium ions which can rapidly attack the aluminum interconnect via:

$$2 \text{Al} + 6 \text{H}_2\text{O}^+ \rightarrow 2\text{Al}^{3+} + 3\text{H}_2 + 6\text{H}_2\text{O}$$ \hspace{1cm} (3-4)

This last reaction can lead to severe problems such as shown in Fig. 3-4 [3.5].

![Image of micro-motor and aluminum](image_url)

**Fig. 3-4** *Aluminum attack during sacrificial etching made this micro-motor useless [3.5].*

Another common problem of sacrificial etching is sticking of the microstructures to the substrate. This is caused by capillary forces which pull the delicate structures down to the substrate during evaporation of the rinsing fluid. Once the structures touch the substrate van der Waals forces, solid bridging, liquid bridging, electrostatic forces or hydrogen bridging cause them to permanently stick to the substrate [3.7, 3.8, 3.9]. This process is visualized in Fig. 3-5.

This section will describe several ways to avoid both the sticking and interconnect attack problem. For a detailed study on stiction mechanisms the reader is referred to Legtenberg et al. [3.7]. Interconnect attack can be avoided by HF vapor etching, the use of photoresist, and the use of alternative etchants. These methods are described in sections 3.3.1 to
3.3.3. Sticking can be avoided by special rinsing and drying methods as will be described in section 3.3.4.

Fig. 3-5 Capillary forces during drying lead to sticking of the microstructures to the substrate [3.7].

3.3.1 HF vapor etching

As the name suggests, in HF vapor etching the sacrificial layer is etched using HF vapor. The wafer is exposed to the HF vapor which etches the oxide. To avoid condensation of water at the surface (see reaction (3-3)), the wafer is kept at elevated temperature. However, the temperature of the wafer should not be too high since water is needed to initiate the two step etching process via reaction (3-2). A wafer temperature between 40°C and 50°C is a good compromise between etch rate and sticking: at a higher wafer temperature the etch rate drops to zero and at a lower temperature sticking occurs. Since there is hardly any water available no hydronium will form and the aluminum will not be attacked. A second advantage of this process is the absence of capillary forces, so sticking is not an issue here. This method is described by Offenberg et al. [3.6].
3.3.2 Aluminum protection using photoresist

The most straight-forward method to protect the aluminum from the sacrificial etchant is the use of photoresist. This method works well when the resist has to adhere to just silicon and aluminum, but limits the maximum etch time. This limit is more severe when the resist has to stick to nitride since resist does not adhere very well to this material [3.5]. The choice of etchants is limited, since most etchants attack resist.

3.3.3 Etching using alternative etchants

Another method to reduce the attack of interconnect during sacrificial etching is the use of alternative etch mixtures, such as a mixture of Buffered HF and glycerine, [3.10] or “pad” etchants, (a mixture of acetic acid, ammonium-fluoride and water) [3.11]. These methods offer reasonable selectivity towards aluminum, at the cost of a low oxide etch rate.

A new approach is to etch in very high HF concentrations [3.12]. Since HF is a weak acid the concentration of hydronium is relatively low, while the concentration of HF is high. This means that reactions (3-2) and (3-3), which are responsible for the oxide etching process, occur much more quickly than reaction (3-4), which causes aluminum attack. This technique approaches the method of HF vapor etching without the need of special equipment. After sacrificial etching the devices need to be kept wet before they are dried in a special way to prevent sticking. Traditionally the sacrificial etchant is removed by a dilution rinse. In order to keep the devices wet when they are taken out of the wet etch, the fluid in the etch bath needs to have a low surface tension. IPA and acetone are commonly used for this purpose. Experiments were performed to investigate the applicability of this etching process in combination with epipoly and aluminum interconnect.

The experiments were carried out using the highest commercially available HF concentration (73% manufacturer: Fluka). In order to lower the etch rate, and to lower the surface tension of the etchant, the HF was diluted with various parts of IPA. A lower etch rate is convenient when a timed etch is used, since a small error in timing is less critical. The etch rate of thermal oxide and aluminum were measured and the etch selectivity was calculated. The same experiments were performed for mixtures of 40% HF and IPA. The results are shown in figure 3-6.
3.3 Sacrificial etching and sticking reduction

Fig. 3-6  Etch rates for thermal oxide (a) and Aluminum (b) and etch selectivity (c) in mixtures of IPA and HF.
Epi Micromachining

The highest selectivity is achieved for pure 73% HF. However, addition of IPA to the HF is preferred since this makes it possible to take the etched sample out of the etchant without the need of dilution rinsing. For 40% HF concentrations (in water) the aluminum etch rate is higher due to the increased hydronium concentration. The oxide etch rate is mostly dependent on the HF concentration in the etchant: 40% HF has almost the same oxide etch rate as 73% HF diluted with 1 part IPA. The initial increase in oxide etch rate for 73% HF with low IPA additions as shown in Fig.3-6 (a) can be explained by the increased wetting capability of this mixture, compared to undiluted 73%HF.

A comparison between alternative etch mixtures is given in Table 3-1. Of all etchants undiluted 73% HF offers the highest etch rate, and highest selectivity. Dilution of the 73% HF with one part IPA lowers the etch rate and selectivity, but offers possibility to take samples directly out of the etchant without the need for dilution rinsing. This simplifies the etching procedure and saves chemicals. HF quickly attacks resist, so this etchant can not be used in combination with resist metal protection or temporary resist spacers which support the structures during drying (see section 3.3.4).

Table 3-1  *Comparison of oxide etchants with selectivity towards aluminum*

<table>
<thead>
<tr>
<th>Etchant</th>
<th>Oxide rate (nm/min)</th>
<th>Al rate (nm/min)</th>
<th>Selectivity</th>
<th>Resist survival</th>
</tr>
</thead>
<tbody>
<tr>
<td>73% HF</td>
<td>1500 (thermal)</td>
<td>2.2</td>
<td>680</td>
<td>no</td>
</tr>
<tr>
<td>73% HF:IPA 1:1</td>
<td>833 (thermal)</td>
<td>12</td>
<td>69</td>
<td>no</td>
</tr>
<tr>
<td>BHF/glycol [3.10]</td>
<td>95 (thermal)</td>
<td>.55</td>
<td>170</td>
<td>yes</td>
</tr>
<tr>
<td>Pad etch [3.11]</td>
<td>200 (PSG)</td>
<td>5</td>
<td>40</td>
<td>yes</td>
</tr>
</tbody>
</table>
3.3 Sacrificial etching and sticking reduction

3.3.4 Sticking prevention

When a liquid etchant is used for sacrificial etching, the samples need to be dried in a special way to prevent sticking of the structures to the substrate. Sticking is caused by the capillary forces of the drying liquid which pull the structures towards the substrate during the drying process. Once the structures and substrate touch one another they will irreversibly stick to each other. There are several methods to prevent sticking. For a thorough review on sticking and sticking prevention methods the reader is referred to Tas [3.13]. The most commonly used methods to prevent sticking will be presented here:

- *Use of low-surface tension final rinsing fluid*
- *Use of Self Assembling Monolayers (SAMs)*
- *Super-critical drying*
- *Freeze drying*
- *Use of temporary support structures.*

**Use of low-surface tension final rinsing fluid**

In this method the final rinsing of the samples is done in a fluid which has a low surface tension. These fluids inhibit much lower capillary forces than water and when the structures are not too flexible (i.e. short or thick) they will not be pulled towards the substrate. A temperature slightly above room temperature also lowers the capillary forces. Iso-propyl-alcohol (IPA) at a drying temperature of about 45°C can be used for this purpose [3.14].

**Use of Self Assembling Monolayers (SAMs)**

This method is based on the reduction, or prevention of capillary forces between the released structures and the substrate [3.15]. A special organic layer of octadecyltrichlorosilane (OTS) is formed at the surface of the released structures. OTS coated surfaces show a much higher contact angle (Fig.3-7 (a)) of water drops than hydrophilic surfaces (Fig.3-7 (b)). A contact angle above 90° results in a convex curvature of the water film between the structure and the substrate, resulting in the absence attractive forces between the surfaces. This is illustrated in Fig.3-7.
Super-critical drying

In super-critical drying capillary forces are completely avoided. This method was first reported by Mulhern et al. [3.16]. In super-critical drying liquid is transferred into gas via the supercritical phase. When a substance in the liquid phase at a pressure greater than the critical pressure is heated, it undergoes a transition from a liquid to a supercritical fluid at the critical temperature. This transition does not form an interface; the liquid simply changes throughout the system into the gaseous state [3.16]. This phenomenon is utilized to avoid the surface tension effects which would occur during conventional drying. The process is shown as trajectory (a) in the phase diagram of figure 3-8 [3.17].
3.3 Sacrificial etching and sticking reduction

Carbon dioxide is usually used as the supercritical fluid because of its low critical temperature and pressure (31.1°C and 72.8 atm.). Since water and carbon dioxide do not mix an intermediate mixing agent is used, for instance acetone, or methanol. The rinsing water is replaced by the mixing agent, and the sample is brought into a pressure chamber. In this pressure chamber the mixing agent is replaced by liquid carbon dioxide. Then the temperature of the pressure chamber is raised beyond the super critical point of the carbon dioxide, and the gaseous carbon dioxide is vented. After all the carbon dioxide is vented, the pressure chamber is brought back to room temperature, and the now dry sample is taken out of the chamber.

Freeze drying

In contrast to super-critical drying, which uses a transition from the fluid to the gaseous phase via the supercritical region, freeze drying makes the transition from the liquid to the gas phase via the solid phase. This method is commonly used in the biological field for sample preparation. In freeze drying the rinsing fluid is frozen and sublimated. The process is illustrated as trajectory (b) in figure 3-8. Since the transition from solid to gas phase does not involve any liquid there are no capillary forces. Sublimation can be enhanced by lowering the pressure around the sample and special equipment for freeze drying can be bought from companies which serve the biological field. The freeze drying technique was first applied to surface micromachining by Guckel et al. [3.18]. He performed evaporation cooling of a water-methanol mixture in a vacuum chamber at 0.15 mbar. A much more elegant method, which does not need a vacuum chamber, was introduced by Legtenberg et al. [3.19]. In this method the samples are rinsed in iso-propanol (IPA) or in water, followed by a dilution rinse in IPA, which serves as an intermediate mixing agent. Then the IPA is replaced by cyclohexane in a dilution rinsing step. Finally the sample is put on a cold plate at a temperature between 0°C and -7°C under a nitrogen flow. At this temperature the cyclohexane freezes quickly as the melting point is +7°C and immediately sublimates. The nitrogen flow serves two purposes: Firstly it prevents condensation of water vapor from the surrounding air on the sample, and secondly it increases the sublimation rate, since the partial pressure of the cyclohexane above the sample stays low. When all the cyclohexane is evaporated the cold plate is heated up to room temperature and the sample is ready to use. A schematic view of the freeze-drying set-up is shown in Fig.3-9.
Fig. 3-9  Freeze drying set-up

Use of temporary support structures.

An interesting approach to avoid sticking is to temporarily support or stiffen the structures during sacrificial etching and drying. One method is to do the sacrificial etch via access holes and drying of the structures before the structural layer is patterned by dry etching [3.20]. In a second approach the structures are supported with photoresist, which is patterned before sacrificial etching, and ashed in an oxygen plasma at the end of the process [3.21, 3.22]. This method can easily be combined with aluminum protection using photoresist. A SEM photograph of a surface micromachined structure with photoresist support is shown in Fig. 3-10.

Fig. 3-10  SEM photograph of a surface micromachined structure which is supported by photoresist strips.
Another approach is to do the sacrificial etch in a normal way and do the final rinse in an acetone/resist mixture. After soft-baking the structures are completely enclosed in resist, which can subsequently be ashed in an oxygen plasma [3.23].

3.4 Merged epitaxial lateral overgrowth

3.4.1 Introduction

Merged epitaxial overgrowth (MELO) is a technique to construct micromachined structures in monocrystalline silicon, using oxide as a sacrificial layer. Monocrystalline silicon has superior properties compared to polysilicon. In this technique the environmental conditions in the epitaxial reactor are altered in such a way that epitaxial growth occurs only on silicon areas, while growth is prevented in areas where the silicon is masked by a dielectric layer, such as silicon oxide or silicon nitride. Selective silicon deposition is achieved by lowering the temperature in the epitaxial reactor and by addition of hydrogen chloride (HCl) to the hydrogen (H₂) dichlorosilane (SiH₂Cl₂ = DCS) gas system. Silicon is deposited by decomposition of the DCS while the HCl etches the silicon. In this way silicon is deposited on silicon, while polysilicon nuclei on the dielectric layer are etched away due to their larger surface area, at the cost of a lower deposition rate. This technique is called selective epitaxial growth (SEG). Once the thickness of the selectively grown epitaxial layer is equal to the thickness of the dielectric layer the growth continues both vertically and laterally, thereby growing over the dielectric layer. This step is called epitaxial lateral overgrowth (ELO). When the dielectric layer consists of strips the growth fronts of the ELO layer will merge in the center of the strip, leading to oxide islands which are covered by epitaxial silicon (MELO). Then the microstructures are etched in the part of the epitaxial layer which is above the oxide island, and the oxide is etched away in the sacrificial etch step. The process is illustrated in Fig.3-11

In this section the suitability of the MELO process for micromachining applications is investigated.
Fig. 3-11  MELO growth process.
3.4.2 MELO process.

The MELO process was carried out at a temperature of 950 °C and a pressure of 60 Torr using a SiH₂Cl₂-HCl-H₂ gas system. A p-type wafer with thermal oxide was used as a dielectric layer. This layer was patterned by a combination of plasma and wet etching. After 90% of the layer had been plasma-etched, the rest of the layer was removed by wet etching. This ensures a silicon interface which is free of RIE damage. Alternatively the whole layer can be dry etched, followed by a thin oxidation and wet removal of this oxide. Before epitaxial growth an in-situ prebake was carried out 1000°C. This prebake in hydrogen is needed to remove any native oxide from the substrate to ensure good quality of the grown layer. During the prebake silicon reacts with silicon dioxide and evaporates as silicon monoxide [3.24]. A temperature of 1000°C for 2 minutes was chosen for the MELO process, since for higher prebake temperatures void formation at the substrate / oxide layer was observed. Fig.3-12 shows a SEM photograph of a cross section of an epi/oxide interface after selective epitaxial growth when the prebake was carried out at 1150°C. During the 2 minutes prebake a 2μm void was formed due to the same reaction which removes the native oxide.

![Image](image_url)

Fig. 3-12 Undercut at the Si/oxide interface when the prebake is carried out at 1150°C for 2 minutes.

The selectivity of the MELO process depends on the HCl to DCS ratio, the type of layer to be overgrown and on the geometry of the structures [3.25, 3.26]. In our processes a HCl to DCS ratio of 3 was sufficient to achieve selectivity. For a detailed report on growth morphology and selectivity the reader is referred to [3.3 ] and [3.27].
3.4.3 MELO structures

Structures were fabricated in a 4 µm thick MELO layer which was grown over 4 µm wide and 1µm thick thermal oxide islands which were oriented in the <100> direction. Orientation of the oxide islands in the <110> directions leads to a non planar surface as reported in [3.3]. The MELO layer was patterned and the sacrificial oxide was etched. This lead to the beam shown in Fig. 3-13

![Image](image.png)

Fig. 3-13  *Free standing single-crystalline silicon beam fabricated using the MELO technique.*

The fabrication of larger structures such as accelerometers was also attempted. This was not successful because the fabrication of the masses required numerous seed holes in the mass area, which are needed as a starting point for the MELO growth. The many perforations in the mass do not have a well defined direction with respect to the crystal lattice, and this leads to a very rough honeycomb-like surface. A longer growth time, and thus a thicker layer, will have a positive influence on the planarity, but will lead to higher deposition times, and may not be compatible with the electronics fabrication process. A SEM photograph of a honeycomb-mass with a beam, which connects it to a monocrystalline edge, is shown in figure 3-14.
3.5 Porous silicon epi micromachining

This section describes the development of an epi-micromachining process based on the use of porous silicon. After an introduction to porous silicon, the theory behind porous silicon formation will be described, followed by experiments which were performed to develop a usable process for micromachining. The section ends with some examples of accelerometer structures which were fabricated using the porous silicon method. A large part of this section is taken from a previously published article [3.28].

3.5.1 Introduction

In porous silicon technology, the sacrificial layer is formed in the silicon substrate, and can be processed from the front side. Porous silicon membranes have been formed using the full thickness of the wafer [3.29], and channels of 100μm deep in the silicon substrate have been formed using a porous sacrificial layer [3.30]. Furthermore, sacrificial porous silicon is a material that makes it possible to manufacture structures of high mechanical and electrical quality [3.31]. The formation of the sacrificial layer can be patterned both by selective substrate doping, as
porous silicon formation is highly selective with respect to different dopant types and concentrations [3.32,3.33], and by masking of the substrate [3.30]. Porous silicon provides a planar surface, and is formed much faster than thermally grown or chemically deposited sacrificial layers. It can be used directly as a sacrificial layer [3.31] and can also be oxidized to form thick sacrificial oxide layers [3.33], thick oxide layers for thermal isolation [3.34], and for SOI applications [3.35]. The large surface area of porous silicon yields a high etch rate in any dilute hydroxide solution at room temperature. The use of porous silicon as a sacrificial layer also greatly reduces processing time and complexity, as well as device area, over bulk micromachining. Sacrificial porous silicon can also be used to increase the air gap between microstructures and the substrate in traditional surface micromachining processes [3.36].

The formation of porous silicon is an isotropic process, so devices may lie in any direction relative to the crystal orientation and structures have very well-defined geometries since etch stops obtained by differential doping offer excellent selectivity [3.32,3.33]. Finally, this technology is fully compatible with standard electronics processes, provided that a non-alkali solution, such as photoresist remover, is used to remove the porous silicon [3.30]. Up to now the porous silicon process is not commercially used because the porous silicon formation procedure is less straightforward than other micromachining techniques.

In this section the development of a porous silicon micromachining process, using a 4μm thick epitaxial layer as the mechanical layer, and a porous layer of a few microns, will be described.

3.5.2 Porous Silicon Formation

Porous silicon is formed by the anodic electrochemical etching of monocristalline silicon in hydro-fluoric (HF) acid or any other fluoride containing solution (Fig.3-15) [3.37].

Porous silicon can also be formed using chemical etching [3.38], but this has a much lower formation rate. Porous silicon is formed by $F^-$ attack of the Si-Si bonds via [3.38]:

$$\text{Si} \rightarrow \text{Si}^{4+} + 4e^- \quad (3-5)$$

$$\text{Si}^{4+} + 6F^- \rightarrow \text{SiF}_6^{2-} \quad (3-6)$$
3.5 Porous silicon epi micromachining

Fig. 3-15 *Anodic etching for formation of porous silicon in HF solution.*

From equation (3-5) it is clear that holes are needed in the first step of porous silicon formation. Holes are supplied by application of an anodic bias, which moves the positive charge carriers (holes) to the Si surface where they weaken the Si-Si bonds, allowing them to be attacked by F⁻ ions. When suitable etch parameters (HF concentration and current density) are used, pores are formed in the substrate [3.38]. The term 'anodic etching' or 'anodization' is used to describe pore formation because the semiconductor acts as the anode in the electrochemical reaction in which silicon atoms are removed from the crystal. Ethanol is often added to the HF solution to reduce its surface tension. This allows the H₂ gas, which is formed during the formation process, to escape more quickly. Prevention of H₂ sticking to the surface improves the homogeneity of the resulting porous layer [3.39].

There are several theories for the exact nature of the pore formation in the literature [3.40,3.41,3.42,3.43]. All agree on the need for holes in this process, but there is less agreement on the reaction at tip of the pore. Depending on the etching conditions both n and p type material can be selectively etched, although the resulting pore structure is quite different as shown in Fig.3-16 [3.44]. In p type material both the pore diameters and the interpore spacings are extremely small with a homogeneous and highly interconnected pore network as shown in Fig.3-16(b). In n-type material the pore diameter is larger and the pores are more like pipes.
Fig. 3-16  Structure of porous silicon in a) n-type material and b) p-type material [3.44]

The formation mechanism of porous silicon is a charge exchange between the semiconductor surface and the electrolytic HF solution. The Si-HF interface acts as a Schottky contact and the charge exchange mechanism is dependent upon the dopant type of the silicon. In p-type material, holes are readily available at the Si-HF interface. In the case of n-type silicon, holes may be generated by light. For n- material tunnelling of electrons away from the interface facilitates the etching [3.45]. In the absence of light, significant pore formation in n-type substrates occurs only at doping levels above approximately $10^{18}$ cm$^{-3}$, when the space charge region is narrow enough to allow tunnelling. The relative rates of pore formation in n-type and p-type silicon of different dopant concentrations and a constant voltage are shown in Fig.3-17 [3.32].

Fig. 3-17  Rates of pore formation in p-type and n-type silicon as a function of dopant concentration with no light generation (taken from Eijkel et. al. [3.32])
Porous silicon formation follows the lines of current flow and therefore the masking can have a significant influence on the shape of the porous layer. Pore formation begins in the unmasked silicon regions, and the rate and time of the etch must be precisely controlled to obtain the necessary depth and lateral dimensions of porous material. Fig.3-18 shows four masking configurations [3.46]. In the first, Fig.3-18(a), an insulating mask is used in conjunction with n-type material. The result is a thin layer of underetching directly under the mask due to an excess of holes in that region. For a p-type substrate, shown in Fig.3-18(b), where holes are plentiful, deeper porous formation is found at the edge of the mask. This is due to a higher current density in this region. Any film that will not be etched by the HF during anodization, including silicon nitride, amorphous silicon carbide (a semi-insulating material), photoresist and the noble metals, can be used as a masking layer [3.46]. Photoresist can be used alone to mask pore formation only if the HF solution is relatively weak and the anodization time required is less than approximately ten minutes [3.46]. Stronger solutions or longer etching times result in the photoresist being attacked by the HF. Regardless of the masking layer and anodization time, however, photoresist may be left on during anodic etching to provide an extra layer of masking protection against pore formation. For short anodization times, n-doped polycrystalline silicon over a thin layer of SiO₂ can also be used as the masking layer and constructional material, as it is made resistant to pore formation by the combination of a protective photoresist layer, insulation from the substrate, and the reverse biased HF-polysilicon junction [3.30,3.46]. Alternatively, silicon nitride may be used as both a masking and a mechanical layer. When a conducting mask is used, as shown in Fig.3-18(c), there is no current concentration at the edge of the mask and therefore a simple underetching is found. A similar structure is found when an n-type diffusion mask is used as shown in Fig.3-18(d). This technique has the advantage that the resulting structures are constructed of monocristalline silicon. Here, however, it is the low doped areas that are made porous and subsequently dissolved, and the free standing structures are limited in thickness to the depth of the implant [3.46]. An alternative to an n-implanted region is the growth of an n-type epitaxial layer in which the structures are formed. This has the advantage of a better defined thickness and a more uniform doping concentration in the structures, which helps to minimize mechanical stress gradients in the constructional layer.
Fig. 3-18  *Four porous silicon formation patterns using a mask*: (a) n-type material with an insulating mask, (b) p-type material using an insulating material, (c) using a conducting mask and d) patterned n-type doping in a p-type substrate (taken from [3.46])

There are several parameters which define the etch rate, or rate of porous silicon formation. The most important are dopant type and concentration, HF concentration, and applied current density [3.38]. Since pore growth is believed to be controlled by the diffusion of holes from the silicon crystal to the Si-HF interface for p-type material [3.40], and the tunnelling of
electrons from the Si-HF interface to the crystal for heavily doped p- and n-type material [3.41], factors that affect the rate of these transfers therefore control the etch rate. The etch rate increases with current density, since a higher current density provides an increase in the number of charge carriers, and thereby the rate of charge exchange across the interface. The porous layer thickness increases with dopant concentration for both n-type and p-type silicon. A higher dopant concentration leads to larger pore diameters and deeper pores, so the layer which is removed in the KOH is thicker. The rate differential as a function of dopant concentration is much greater for n-type than for p-type substrates due to the low probability of tunnelling at low doping levels. An increase in HF concentration has been found to result in a drop in porosity [3.47], probably due to the H\(^+\) ions effectively passivating the surface [3.48]. Higher HF concentration has also been found to result in an increase in pore formation rate [3.49].

More recently alternative etchants for porous formation have been investigated. One of these etchants, based on ammonium fluoride and acetic acid has the distinct advantage of having an extremely low etch-rate for aluminum [3.37].

### 3.5.3 Experiments

To characterize the porous silicon formation process experiments were carried out using uniformly doped p, p+, n, and n+ samples which were anodized at two current densities and two HF concentrations. Silicon nitride was used as masking material. A mask containing holes at increasing separation distances was used to measure the lateral porous silicon formation rate, using a microscope. An example of an etched sample is shown in Fig.3-19.

Lateral pore formation rates as a function of current density and two different HF concentrations (20% and 40%), for p and p+ doped silicon is shown in Fig.3-20. As expected, an increase in HF concentration, current and doping concentration leads to an increase in the porous silicon formation rate. The effect of HF concentration is less pronounced for the low doped material, which was also found by Steiner et. al [3.30].
Fig. 3-19  *Example of a sample after porous silicon formation.*

Fig. 3-20  *Etch rate as a function of applied current for p and p+ type material.*
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![Graph showing etch rate vs. HF concentration for different doping levels.]

**Fig. 3-21** Lateral porous silicon formation rate of p and n-type silicon as a function of HF concentration.

When the lateral porous silicon formation rates for n-type and p-type silicon are compared like in Fig. 3-21, it seems like the n-type material etches much faster. This is caused by the etching mechanism in n-type material which is masked by an insulating material (Fig. 3-18(a)). The porous layer is formed directly under the surface of the masking layer, and is very thin. The vertical etch rates of n-type material is lower than the vertical etch rate of p-type material which etches almost isotropically.

Data on pore formation rate as a function of current density, HF concentration and doping, may be used to make predictions regarding the selectivity of different etch recipes, or combinations of particular current densities and HF concentrations, for different types of silicon. The greatest differences in pore formation rates between differently doped types of silicon, when measured on separate uniformly doped substrates, occur when both a high current density and a high HF concentration are used in anodic etching. The etching of each type of material is dependent upon several factors. By adjusting the etching parameters selective porous formation can be achieved [3.49]. Such a technique has been applied to selective porous formation of p+ silicon [3.50]. In this case buried p+ layers, under an n-type epitaxial layer, were made porous to enable the formation of a buried oxide. In this case care should be taken to minimize...
the thermal processing, to prevent out-diffusion and auto-doping of the epitaxial layer.

To investigate the selectivity of porous silicon formation a sample was made using a p-type substrate in which both p⁺-type and n-type areas were implanted. The material was anodically etched in 5% HF using a current density of 0.1A/cm². Then the porous silicon was etched in diluted KOH. This lead to the result shown in Fig. 3-22.

![Fig. 3-22 SEM photograph showing the selective nature of porous formation](image)

The p-type substrate has been etched under the n-type region as expected. An additional etch has occurred at the surface of the n-type diffusion. In this layer the doping concentration was sufficiently high for porous formation to occur. So p⁺-type etches faster than p-type silicon, the n⁺⁺-type silicon at the surface of the diffused n-type rings is also etched, and n type silicon is not at all attacked.

The relative pore formation rates in the different dopant types of silicon found in these samples were very different from those found on uniformly doped samples. This was because different amounts of current flowed through different regions due to the non-uniformity of the doping pattern. When n-type and p-type silicon are side by side, a diode voltage exists across the junction, causing the current to stay on one side of the junction and that material to become porous much more quickly than the material...
on the other side of the junction. As a result, even though lateral pore formation rates in n+ silicon were found to be higher than those in p- and p+ silicon on uniformly doped samples, n+ rings act as an etch stop to pore formation in p- and p+ material. When pore formation in lightly p-doped areas reaches p+ silicon, on the other hand, the rate of formation increases dramatically, as there is no diode voltage across the junction and current flow increases in the low resistivity p+ material. The 40% HF / 80mA/cm² recipe has been found to provide the best pore formation selectivity at dopant junctions.

3.5.4 Use as a Sacrificial Layer

Sacrificial Techniques

Once silicon has been made porous, it can be removed in diluted hydroxide solutions (KOH, NaOH, NH₄OH, etc.) and, because of its high surface area, dissolves very quickly even at room temperature [3.33,3.51]. KOH concentrations as low as 1%, at room temperature have been used to remove porous silicon layers [3.52]. Care must be taken to keep the etch rate slow enough so that the reaction does not become violent, causing delicate microstructures to be destroyed by bubbles. Porous silicon can also be removed by photoresist remover, if this is more compatible with a specific process [3.30]. The large gaps resulting from the porous silicon sacrificial etch process, together with the resulting rough surface make the drying process less critical in comparison to other sacrificial etching techniques.

Anodic etching provides an additional sacrificial technique known as electropolishing. For a solution of any given HF concentration, there is a critical current density above which electropolishing, rather than porous silicon formation, takes place under conditions of anodization. Electropolishing uniformly removes portions of the crystal rather than etching channels into a substrate that remains otherwise intact. Silicon is made porous when the reaction between the holes and the fluoride atoms is limited by the number of available holes and it is uniformly etched when the reaction is limited by the number of available fluoride ions. The critical electropolishing current density increases with HF concentration, so electropolishing is favoured by high current densities and low HF concentrations [3.53].
3.5.5 Fabrication of accelerometer structures

Lateral and vertical micro-accelerometer structures have been fabricated using an n-epitaxial layer on a p-type substrate. Fabrication begins with the growth of a lightly doped n-epitaxial layer over a p-type substrate (Fig. 3-23a). Next, a layer of LPCVD nitride and a layer of PECVD oxide are deposited, and the oxide is patterned using a dry etch to serve as a mask for plasma etching the nitride and epi layers. Openings are etched through the epi down to the substrate in patterns defining the shape of the accelerometer (Fig. 3-23b). The devices are then anodically etched, making the silicon underneath the beams porous as shown in Fig. 3-23c. Finally, the porous silicon is removed in KOH, releasing the beams from the substrate (Fig. 3-23d).

![Diagram of fabrication process]

Fig. 3-23 Processing sequence for fabrication of accelerometers

A SEM photograph of a lateral accelerometer structure is shown in Fig. 3-24, and a close up of a vertical accelerometer structure is shown in Fig. 3-25.
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Fig. 3-24  *SEM photograph of a lateral accelerometer structure.*

Fig. 3-25  *SEM photograph showing part of a vertical accelerometer structure.*

To allow current flow during anodization through doped buried layers, openings must be etched through the epi to expose the buried layers to HF solution [3.31]. Anodization must take place for a long enough time so that free standing structures are completely undercut by the lateral progression of pore formation, and the full desired thickness of the sacrificial layer is
reached by the vertical progression of the etching. A SEM photograph of a structure which is not yet completely undercut is shown in Fig. 3-26.

![SEM photograph of a partly underetched structure.](image)

Fig. 3-26  *SEM photograph of a partly underetched structure.*

### 3.6 Epipoly micromachining

#### 3.6.1 Introduction

In the epipoly technique the epitaxial reactor is used to grow a polycrystalline layer in which micromechanical structures are constructed. The use of an epitaxial reactor to grow polysilicon layers for MEMS fabrication was first reported by Offenberg et al. [3.54] In the epitaxial reactor the growth rate of the polysilicon is more than 200 times higher than in a conventional LPCVD reactor because the growth temperature is much higher. This makes it possible to grow thick polysilicon layers in a relatively short time. The epipoly process offers the possibility to combine the growth of a polysilicon layer, for micromechanical structure fabrication, with the growth of a conventional epitaxial layer, for electronics fabrication, in one combined deposition step. This reduces the process complexity and thermal budget when compared to conventional smart surface micromachining. However, fabrication of sensor and read-out electronics on the same chip is no longer mandatory here, as will be explained later. The fabrication process for epipoly microstructures is more conventional than the porous silicon and MELO processes and has
3.6 Epipoly micromachining

the disadvantage of using poly-cristalline silicon as construction material. However, the much thicker and very low-stress polysilicon layers grown in the epitaxial reactor offer several advantages when compared to conventional surface micromachining, especially when lateral accelerometers are to be fabricated.

The high thickness of the layer leads to higher lateral capacitances, as the area of the electrodes scales with the thickness of the construction layer. This makes a two chip approach for accelerometers feasible: the mechanical structure is fabricated on one chip, and the read-out circuitry is fabricated on a second chip which is mounted in the same housing. This has a positive influence on fabrication complexity and thus on yield. Furthermore, the thick epipoly layer is much stiffer in the vertical direction than thinner conventionally grown polysilicon layers, leading to a reduction in vertical sticking probability.

When compared to the porous silicon and MELO processes, this technique offers the advantage of fully galvanically insulated areas, so leakage currents of reverse biased (unpassivated) diodes do not occur here. Furthermore there is no limit on the area of the structures which can be underetched, provided the rest of the chip can withstand long etch times.

3.6.2 Experiments

The experiments described in this section are aimed on the optimization of the epipoly layer properties with respect to mechanical stress and electrical resistance. Epipoly layers were grown at different process conditions and taken through the standard Delft DIMES01 bipolar process [3.55], or were subjected to the same thermal budget. In this way the user of the layer has the possibility to integrate bipolar electronics on the same chip.

Base process.

Several experiments were performed to investigate growth morphology, growth rate and mechanical stress in the epipoly layer. Unless mentioned otherwise the fabrication process of the samples was as follows:

On a p-type wafer a 700nm thick thermal oxide was grown, followed by deposition of a conventionally grown 200nm thick low-stress polysilicon layer [3.56]. This conventional LPCVD polysilicon layer is needed as a seed layer for epipoly growth. Without this layer, the epipoly surface would be much rougher. Moreover no epipoly growth would occur on
oxide areas which are located close to bare silicon areas. This is caused by the selective nature of the epi growth in the presence of a silicon/oxide interface. Then an epipoly layer was grown in the epitaxial reactor using a HCl/DCS gas system under the following conditions (unless mentioned otherwise):

- **Temperature:** 1050 °C
- **Pressure:** 60 Torr
- **H₂ flow:** 50 slm
- **DCS:** 360 sccm
- **HCl:** 0 slm
- **Prebake:** 1000°C, 2 minutes in hydrogen
- **Deposition time:** 4 minutes.

Since the mechanical properties of the epipoly layer is the dominating factor for MEMS applications these properties were optimized first and the electrical properties were only measured for the layers which passed the mechanical test.

The following parameters were addressed:

- **poly seed layer structure**
- **oxidation**
- **nitride protection during oxidation steps**
- **epipoly growth temperature and doping**
- **sacrificial oxide area and thickness**
- **gas composition during epipoly growth**
- **prebake temperature**

**Poly seed structure**

Experimental

On three oxidized wafers a low-stress LPCVD polysilicon seed was deposited (deposited as semi amorphous structure and in-situ annealed at 600°C [3.56]) and on three oxidized wafers a standard LPCVD polysilicon seed (deposited directly as polysilicon) was grown. One wafer from each group was annealed at 1100°C as this is the highest temperature step during the bipolar process. On all the wafers an epipoly layer was grown at
standard conditions. Then one quarter of each wafer was doped using the deep p-type insulation diffusion step using a solid boron source, and one quarter was doped using the POCl₃ collector contact diffusion of the bipolar process. The remaining half received only the $1 \times 10^{16}$ cm$^{-3}$ in situ arsenic doping of the epi growth. Then the epipoly was patterned and RIE etched followed by sacrificial etch and freeze drying. Two control wafers received either low-stress or standard LPCVD poly and epipoly, but were not taken through the bipolar process.

In order to measure the strain, pointer structures as shown in Fig. 3-27 were used. These structures can be used to measure both compressive and tensile strain [3.57,3.58]. In the case of tensile stress, the two horizontal beams of figure 3-27(a) will become shorter. This causes a clockwise rotation of the vertical beam. In the Berkeley type pointer the length of wide vertical beam changes. This causes the horizontal beam to bend and leads to a rotation of the small vertical beam.

![Diagram](image)

(a)  (b)  

**Fig. 3-27 Strain measurement structures.** (a) Delft type, (b) Berkeley type.

Results

All the wafers that were taken through the bipolar process showed very high compressive strain levels irrespective of poly seed layer or doping type and level. The wafers which did not see any of the bipolar steps, on the other hand, had a much lower stress level. The conclusion of this experiment is that the high compressive strain level in the epipoly layer
after bipolar processing is caused by either the high temperature treatment, or by the oxidation. The poly seed structure does not seem to have an influence on the stress of the resulting epipoly later. Low-stress polysilicon was taken as standard seed layer for further experiments.

Oxidation

Experimental

For this experiment two oxidized wafers received a low-stress LPCVD poly seed layer, followed by epipoly growth. Then one was annealed for 10 minutes at 1100°C in oxygen and the other one was annealed for the same time and temperature in argon. Then the wafers were RIE etched, followed by sacrificial etching and stress measurement.

Results

The wafer which was annealed in argon did not have any noticeable difference in stress level compared to the as-deposited layer from the previous experiment. Both stress levels were below the accuracy of the stress measurement method. The oxidized wafer, on the other hand, showed a high compressive strain level, even after this very short oxidation step. Oxygen penetration during oxidizing steps was the likely cause of the compressive strain in the epipoly after bipolar processing. This could mean that a standard diffusion process cannot be used to dope the epipoly layer, and that the epipoly layers must be shielded from oxygen during oxidation.

Nitride protection

The previous experiment revealed that penetration of oxygen in the epipoly layer was the likely cause of compressive strain in the layer. In the next experiment oxygen penetration in the epipoly layer is prevented by the use of a nitride shielding layer, similar to the technique used in LOCOS processes. This experiment will give more insight in the influence of oxygen on the strain level of the epipoly layer.

Experimental

Epipoly was grown using the same recipe as in the previous experiment. Then one half of the wafer was covered with nitride followed by a 4 hours and 40 minutes oxidation step at 1100°C. This is approximately the normal total thermal budget of the bipolar fabrication process. Then the
nitride was stripped and the epipoly was patterned, followed by sacrificial etching and strain measurement.

Results

The half of the wafer which was not shielded from oxygen during the oxidation step showed a high compressive strain level. The protected half, however, did not show any measurable mechanical strain. The compressive strain can easily be observed by an array of double clamped beams, such as shown in Fig.3-28. The strain was calculated from the strain measurement device given in Fig.3-29 using the formulas of [3.57]. From this structure the compressive strain in the oxidized layer was calculated to be 800με. The strain in the protected layer was below the accuracy of the measurements. This experiment strongly indicates that oxygen penetration is the dominant factor which causes compressive stress in epipoly. Furthermore, it shows that development of compressive strain can be prevented by the use of a nitride shielding layer. After presentation of this procedure [3.59] a more detailed study about the influence of oxygen anneals on epipoly stress was done by Fürtsch et al [3.60]. His results were similar.

Fig. 3-28  An array of double clamped epipoly beams with lengths of 100,200,..1000 μm and a width of 2, 4 and 6 μm. (a) epipoly layer passivated with nitride during oxidation, (b) epipoly not passivated during oxidation.
Fig. 3-29 Strain measurement structures. The device which covered with nitride during the oxidation process shows no measurable strain (left), while the unprotected device indicates compressive strain (right).

**Growth temperature**

Experimental

In this experiment three oxidized wafers with a low-stress LPCVD poly seed layer were used to analyze the influence of the epipoly growth temperature on the mechanical and electrical properties of the epipoly layers. Epipoly was grown at 950, 1050 and 1150°C at 60 Torr pressure. For each deposition temperature the growth time was adjusted to grow a 4μm thick monocrystalline epilayer, since this is the epi layer thickness of the bipolar process. Then one quarter of the wafer was implanted with boron at 100keV and a dose of $5 \times 10^{15}$ cm$^{-2}$. Two other quarters were implanted with phosphorus and arsenic respectively at the same energy and dose, while the remaining quarter received only the in-situ arsenic dope of the epipoly growth process. Then a 200nm thick low-stress LPCVD nitride layer was grown to shield the epipoly wafer from oxygen penetration during further bipolar processing steps, as oxygen penetration would lead to high compressive strain levels. After this, the wafers were put in a furnace at 1100°C for 4 hours and 40 minutes in oxygen in order to simulate the full bipolar process without performing all the different steps. Then the nitride layer was stripped in boiling phosphoric acid and trenches were etched through the epipoly layer, followed by sacrificial etch.
Results

On all the wafers the mechanical stress levels were very low. Due to the limited size of the strain measurement structures it was not possible to obtain a reliable quantitative strain estimation, but all the strain measurement structures indicated no strain, or very low tensile levels. In order to get more insight in the mechanical difference of the grown layers beams were pulled-in electrostatically. Fig.3-30 shows the measurement set-up.

![Diagram of pull-in voltage measurement](image)

**Fig. 3-30 Pull-in voltage measurement. A voltage is applied between anchor and counter electrode.**

A voltage is applied between the free-etched beam and a counter electrode. The resulting electrostatic force pulls the mean towards the counter electrode. The voltage is slowly increased while observing the beam through a microscope. When the pull-in voltage is reached the beam collapses to the counter electrode. After collapsing, the beams irreversibly stick to the counter electrode. They did, however, return to their straight position if the activation voltage was left below the pull-in voltage. The width of the used beams was 3μm, the gap between beam and counter electrode was 3μm and the thickness was 4μm. The results of these measurements are plotted in Fig.3-31.
Fig. 3-31 Relation between pull-in voltage and beam length for several growth temperatures and doping types.

The pull-in voltage is determined by a combination of Young's modulus and intrinsic strain of the layer. From the measurements can be concluded that the various layers have very similar mechanical characteristics. If the mechanical strain in the layer is neglected the relation between pull-in voltage $V_{pi}$ and Young's modulus $E$ for a double sided clamped beam is:

$$V_{pi} = \frac{1.220 \pi^2 E I_y d^3}{l^2 b \varepsilon}$$

(3-7)

where $l$ is the length of the beam, $d$ is the air gap between beam and counter electrode, $I_y$ is the moment of inertia of the beam, $\varepsilon$ is the permittivity and $b$ the width of the beam (in this case the thickness of the epipoly layer). The dimensions are also given in figure 3-30. The moment of inertia of a beam with width $b$ and thickness $d$ is given by:

$$I_y = \frac{bh^3}{12}$$

(3-8)
Substituting (3-8) in (3-7) and rewriting results in a formula to calculate the Young's modulus:

$$E = \frac{V_P^2 L^4}{12 h^3 d^3}$$  \hspace{1cm} (3-9)

When the Young's modulus is calculated from the measurements of figure 3-31 an average value of 170 GPa is found. This is in good agreement with values found in literature which are in between 150 and 175 GPa [3.58, 3.62, 3.63, 3.64].

The resistance of a 500μm long 4μm wide free standing double clamped beam was measured to investigate the influence of growth temperature on the resistivity of the different epipoly layers. The results are plotted in Fig. 3-32.

Fig. 3-32 Relation between epipoly growth temperature and sheet resistance.

A higher epipoly growth temperature results in a lower sheet resistance of the layer. Since the sheet resistance of the layer is acceptable for MEMS fabrication at all growth temperatures used, 1050°C was chosen as the standard deposition temperature, since this is the standard epi growth temperature of the bipolar process. The designer also has the freedom to choose any of the dopants used in this experiment.
Sacrificial oxide

Experimental

In this experiment the influence of the sacrificial oxide thickness and type on the epipoly planarity was investigated. Two wafers were thermally oxidized to grow 700nm and 100nm sacrificial oxides. One control wafer was not oxidized. Then a standard LPCVD low-stress polysilicon seed layer was grown. The poly seed layer and underlying oxide were removed from the wafer in a chess-board pattern. The size of the squares was 1x1cm². Then epi/epipoly was grown at standard conditions for all wafers and the surface of the wafers was scanned using an alphastep surface profiler. Phospho-silicate glass (PSG) and low temperature oxide (LTO) were investigated as a fast etching alternative for the sacrificial thermal oxide. LPCVD tetra-ethyl-ortho-silicate oxide (TEOS) was evaluated since this layer is stable at high temperatures and can be grown on top of dielectric layers.

Results

The surface scans of the three wafers are shown in Fig. 3-33.

The wafer with the thickest sacrificial layer is shown in Fig. 3-33(a). From this scan it is clear that the surface of the wafer is not planar. It was not even possible to do proper leveling of the measurement as there were no reference points which could be used to level the measurement. There is a step at the epi/epipoly interface, and the epi and epipoly layers are concave and convex respectively. This non-planarity is believed to be caused by a temperature gradient over the epi and epipoly areas during growth. In the epi-reactor the wafers are heated by halogen lamps. The epipoly areas become warmer than the epi areas because of the thermal insulation properties of the underlying oxide. Since the average temperature of the wafer is set to 1050°C the centre of the epipoly squares are above this temperature and the temperature in the centre of the epi areas is below 1050°C. The plots of the wafer with thinner sacrificial oxide (Fig. 3-33(b)) and no oxide at all (Fig. 3-33(c)) support this hypothesis. The resulting surface is much more planar. The step at the interface still exists, as this step is not caused by a temperature gradient, but by a preference of the DCS to decompose at the monocrystalline silicon rather than at the poly seed. The difference in step height at the interface between poly and epipoly in the three samples is caused by the difference in underlying oxide thickness. In order to get a surface as planar as possible the
3.6 Epipoly micromachining

Fig. 3.33  Surface scans of the epi/epipoly interface for (a) a wafer with 700nm sacrificial oxide, (b) a wafer with 100nm sacrificial oxide and (c) a wafer without sacrificial oxide. Note the difference in Y-axis scale for wafer a.

temperature gradient over the wafer during epi/epipoly growth should be minimized. This is accomplished by minimizing the areas with buried oxide and choosing the oxide thickness not larger than necessary.

The use of PSG and LTO is not possible in the epipoly process, since these layers are not stable at the high growth temperatures of the epipoly. The LTO delaminated from the wafer surface during cooling down causing particles in the epi reactor. With a PSG sacrificial layer, polysilicon bubbles were formed during epi growth, caused by the out-gassing from
the PSG layer. These bubbles were also observed by Farooqui, who used this phenomenon to fabricate hemispherical shells in polysilicon \[3.65\]. An example of such a bubble is shown in Fig. 3-34.

![Poly bubble](image)

**Fig. 3-34** Polysilicon bubble caused by out-gassing of the underlying PSG layer.

LPCVD TEOS showed the same characteristics as thermally grown silicon dioxide. This layer can be used when it is impossible to use a conventional thermal silicon dioxide layer, for instance in multilevel epipoly micromachining processes.

**Gas composition**

Experimental

In this experiment five oxidized wafers with a low-stress LPCVD poly seed layer were used to analyze the influence of the gas composition during epi growth on the relative growth rate between monocrystalline silicon and epipoly. As in the previous experiment, the poly seed layer and underlying oxide were removed from the wafer in a chess-board pattern. Epipoly was grown at a temperature of 1050°C, a pressure of 60 Torr a dichlorosilane (DCS) flow of 100 slm and a HCl flow of 0, 100, 200, 300 and 400 slm respectively. The deposition time was adjusted to grow a 4µm thick monocrystalline epilayer for all wafers. After epi growth the surface of the wafer was scanned using an alphastep surface profiler.
Results

Fig. 3-35 shows a SEM photograph of an area with combined epi and epipoly. The step height at the epi/epipoly interface is a function of the HCl/DCS ratio. The dependence of the gas composition on step height is given in Fig. 3-35. The more HCl the higher the step height and the higher the relative growth rate difference. This was expected since HCl is added to DCS to prevent polysilicon nucleation and growth in selective epitaxial growth recipes, where monocrystalline silicon is grown on bare silicon and poly nucleation is prevented on oxide areas.

![SEM photograph of epi and epipoly growth](image)

**Fig. 3-35** SEM photograph of a combination of epi and poly growth on the same chip (left) and step height at the epi/epi-poly interface versus HCl to DCS ratio (right).

3.6.3 Epipoly growth morphology

The growth morphology of the epipoly is largely independent on the process parameters in the epitaxial reactor and on the poly seed layer, although the layer is rougher when the seed layer is completely omitted. The epipoly layer has a columnar structure as can be clearly seen on the TEM picture in Fig. 3-36. After a very thin interface layer between the poly seed layer and the epipoly layer only a few polysilicon grains win and grow into columns with a diameter between 1 and 2 μm. The orientation of the grains was measured using X-ray diffraction and is mostly <100> and <335>.

When epipoly and (100) monocrystalline silicon are grown simultaneously the growth rate of the epipoly is always lower than the growth rate of the epi. An experiment was carried out to investigate the difference in growth rate between epipoly and monocrystalline silicon. Three 100mm wafers
Fig. 3-36 TEM photograph of an epipoly layer. The columnar structure is clearly visible.

were prepared for this experiment. The first wafer had a bare monocrystalline silicon surface and the second one was completely covered with a polysilicon seed layer. On the third wafer, 27 squares of monocrystalline silicon, with an area of 1cm², were patterned in a chess board configuration and the rest was poly. On these wafers silicon was deposited in the epitaxial reactor at 1050°C for 8 minutes, using a DCS flow of 360sllm and a pressure of 60 Torr. The weight of the wafers was measured before and after deposition. From this measurement the thickness of the layer was calculated. The growth rate of the epipoly layer was found to be 92% of the growth rate of the monocrystalline silicon. The increase in mass of the chess board pattern wafer can be estimated by multiplying the relative area of the monocrystalline and polycrystalline silicon by their growth rates. This estimation is exactly equal to the measured value. The results of this experiment is shown in table 3-2.
Table 3-2  Results of the experiment to measure the growth rates of monocristalline silicon and epipoly.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Mass increase (mg.)</th>
<th>Layer thickness (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mono</td>
<td>157</td>
<td>8.59</td>
</tr>
<tr>
<td>Poly</td>
<td>145</td>
<td>7.92</td>
</tr>
<tr>
<td>Chess board</td>
<td>149</td>
<td>8.15 (average)</td>
</tr>
</tbody>
</table>

The global growth rate difference can be explained as follows: At 1050°C the growth rate of the silicon is limited by diffusion of reaction species to the surface of the wafer. Silicon is deposited by decomposition of silane containing species at the surface of the wafer. At the same time, silicon is etched by HCl. The rough epipoly surface has a larger area than the smooth monocristalline surface and thus the etching process will be faster for the epipoly layer, leading to a lower deposition rate.

A local growth rate difference between epi and epipoly can be explained using surface energy considerations. For the silicon atoms it is energetically favorable to be a part of the monocristalline silicon lattice. This leads to a local growth increase of monocristalline silicon at the epi/epipoly interface at the cost of the local epipoly growth rate.

The growth rate difference is illustrated in Fig.3-37 and can be used to maximize surface planarity by tuning the total thickness of the sacrificial oxide layer and the poly seed layer. A completely planar surface, however, is not attainable since the growth rate difference in the vicinity of an epi/epipoly interface will be much larger than the average growth rate difference between epi end epipoly over the whole wafer.

![Fig. 3-37 Progression of simultaneous epi and epipoly growth. For clarity the growth rate difference is exaggerated.](image-url)
The SEM photographs of Fig. 3-38 show the growth morphology at the epi-epipoly interface.

![SEM photographs showing the growth morphology at the interface between epipoly and epi: top view (a); cross section (b).](image)

3.6.4 Epipoly structures

Demonstrator structures were fabricated in a simplified epipoly process. In this process it is possible to fabricate simple free standing structures, but it is not possible to make multilevel electrical connections. The simplified process starts with a p-type wafer on which 1 μm thermal sacrificial oxide is grown. Then a 200nm thick poly seed layer was grown in a conventional LPCVD reactor, followed by a 4 μm thick epipoly layer which was grown at the same conditions as the base process in paragraph 3.6.2. This layer is implanted with boron and annealed in argon. Then 1 μm of PECVD oxide was deposited which was used as a masking layer for the subsequent plasma etching of trenches through the epipoly layer. In a last step the oxide underneath the moving parts of the structures was etched away. The anchors of the structures were formed by areas which are too large to be completely undercut during the sacrificial etch process. The process is described in Fig. 3-39.

A SEM photograph of a structure fabricated in the process of Fig. 3-39 is shown in Fig. 3-40.
3.6 Epipoly micromachining

Fig. 3-39  *Simplified epipoly process.*

Fig. 3-40  *Beam fabricated in the simplified epipoly process. This particular beam is 1mm long.*
3.6.5 Practical issues when working with epipoly

There are some properties of epipoly which need special attention during design and fabrication of the structures. These originate from the topography of the surface of this layer. As can be seen from the SEM photographs the epipoly surface is very rough. During lithography reflecting light will be scattered once it is reflected from the rough surface. Hence, a photoresist which absorbs scattered light such as HiPR6517HC is recommended when small structures (smaller than 2μm) are to be fabricated. Another option would be to mechanically polish the surface of the wafer after epipoly growth, but this complicates the fabrication process.

When the alignment markers of the wafer are covered with epipoly it is impossible for the wafer stepper to align the wafer. This problem can be avoided by clearing the alignment mark regions from the poly seed layer and oxide before epipoly growth, or by stripping the epipoly on top of these markers after epipoly growth.

When epipoly and epi are grown next to each other there will always be a step at the epi/epipoly interface. The designer should locate mechanical and electronical structures far enough from the interface to ensure a reasonably planar surface. Furthermore, when epi and epipoly are combined in the same process, the epipoly areas should not be larger than strictly needed. This ensures a uniform temperature of the wafer during epi/epipoly growth, which has a positive effect on surface planarity.

3.7 Epipoly accelerometer fabrication process

In this paragraph a fabrication method for epipoly accelerometers will be described, using the work of the previous paragraphs. The standard epipoly process will be expanded with an extra polysilicon interconnect layer below the mechanical epipoly layer. This enables electrical connection of the structures and the crossing of interconnect lines. In this description the bipolar fabrication process is not included, but all the processing steps are compatible with the bipolar fabrication process. The fabrication starts with a p-type (100) wafer. On this wafer alignment markers are grown using a two-step oxidation process. This oxide is not stripped, since a thick oxide layer between the micromechanical structures and the substrate helps to reduce parasitic capacitances. After oxidation a
layer of silicon nitride is grown to shield the marker oxide from the sacrificial etchant during the sacrificial etch (Fig.3-41(a)). Then the first LPCVD polysilicon layer is grown and patterned (PS0) (Fig.3-41(b)). This layer is used to provide electrical shielding under the moving structures and to interconnect the epipoly structures. After PS0 patterning the sacrificial layer is deposited (Fig.3-41(c)). LPCVD TEOS oxide is used for this purpose as it is the most stable non-thermal oxide available. After deposition the TEOS layer is annealed at 1100°C since this is the highest temperature which occurs during later processing. Now anchors are etched in the sacrificial layer, and an LPCVD poly seed layer is grown (Fig.3-41(d)). Immediately after poly seed growth the wafers are taken in the epitaxial reactor and a thick epipoly layer is deposited (Fig.3-41(e)). This layer is implanted and covered with a thin nitride layer, followed by an anneal for 4 hours and 40 minutes to simulate the thermal budget of the DIMES01 bipolar process. This treatment makes it possible to integrate bipolar read-out electronics in a later stage. After this anneal the nitride is stripped, and aluminum is sputtered and patterned (Fig.3-41(f)). Now the epipoly layer is patterned using reactive ion etching (RIE etching) and a plasma oxide mask (Fig.3-41(g)). Depending on the sacrificial etch process a resist mesh structure is made on the wafer in order to support the structures during sacrificial etching. Then the wafer is cut into chips and the sacrificial layer is etched using either the 73%HF/IPA process combined with freeze drying or they are etched in pad etch using temporary resist support structures which are ashed in an oxygen plasma (Fig.3-41(h)). A more detailed description of this process is given in the appendix.

**Fig. 3-41** *Epipoly process for accelerometer fabrication.*
Fig. 3-41 Epipoly process for accelerometer fabrication.
3.8 Combination of epipoly and porous silicon

In the previous paragraph a process has been described to fabricate epipoly acceleration sensors. This process can be combined with a porous silicon sacrificial layer in addition to the oxide sacrificial layer. The porous silicon technique offers the possibility to fabricate very large gaps under the moving structures. These large gaps lower the possibility of vertical sticking of the microstructures and help to minimize parasitic capacitances to the substrate. Furthermore, they offer the possibility to improve the quality factors of resonating structures, since a larger gap between the structures and the substrate lowers the air damping force [3.66].

In this technique the silicon nitride in the areas under the moving structures is removed before the epipoly layer is grown. On the back-side of the wafers aluminum is sputtered which is needed to make electrical connection for the porous silicon formation process (Fig. 3-42(a)). After structuring of the epipoly layer the sacrificial oxide is etched in a fluoride containing etchant (Fig. 3-42(b)). Concentrated HF can be used for this purpose to minimize etching times. Then the wafer is brought in a diluted HF solution in which it is electropolished at low current densities (Fig. 3-42(c)).

Fig. 3-42 Epipoly fabrication process in combination with porous silicon.
Electropolishing, rather than porous silicon formation is favoured in this process, because the violent reaction, associated with porous silicon removal in KOH, can easily destroy the delicate structures.

Figure 3-43 shows 8 μm thick epipoly structures which are suspended over a 10μm deep electropolished area. In this case a mixture of 40%HF, ethanol and water was used in a 1:25:25 ratio. The current density was 60mA/cm² and the anodization time was 60 min. The ethanol was added to enhance the uniformity of the electropolishing process. A detailed description of the process which yields this structure is given in the appendix.

![Image](image.png)

Fig. 3-43 Example of an 8 μm thick free standing epipoly structure which is suspended over a 10μm electropolished gap.

## 3.9 Conclusions

In this chapter three epi micromachining processes have been presented.

In the MELO process it is possible to fabricate monocristalline beams with a well defined substrate gap. The size and orientation of the free standing structures is limited by the capabilities of the ELO process. The complicated MELO process is suitable for the fabrication of separate beams, but the fabrication of large underetched areas is not possible.
The porous silicon micromachining technique presented here yields monocrystalline structures with large substrate separations. The rough surface and large substrate gaps facilitate the drying process after sacrificial etching. The structures are not galvanically insulated from the substrate and the underetch distance is limited.

Of all the techniques presented here the epipoly method is preferred, since it offers the possibility to fabricate large underetched structures, which are completely insulated from the substrate. Another advantage is the possibility to use a thin underlying polysilicon layer to interconnect different parts of the structures. A disadvantage, when compared to the MELO and porous silicon processes, is the polycrystalline structure of the layer, which offers inferior material quality and higher leakage currents when pn-junctions are fabricated.

A combination of the epipoly and porous silicon process yields structures with very large gaps between the free standing structures and the substrate. This approach can be useful to minimize parasitic capacitances to the substrate and to lower air damping forces. Furthermore the probability of vertical sticking is reduced.

Sacrificial etching problems such as sticking and aluminum interconnect attack can be solved by the use of concentrated hydro-fluoric acid (73% HF) for sacrificial layer etching in combination with freeze drying. An alternative to this method is the use of photoresist to protect the aluminum and to temporarily stiffen the structures. This resist is removed in an oxygen plasma.

3.10 References


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3.10 References

M.S. thesis, Electronic Instrumentation Laboratory, Faculty of Electrical Engineering, Delft University of Technology, The Netherlands, A95-09, June 1995.


3.10 References


4.1 Introduction

In this chapter the theory, design, and measurements of epipoly accelerometers will be described. The largest application area of silicon acceleration sensors is the automotive market, for which several accelerometers have been introduced. Accelerometers are used as crash sensors in air-bag applications, as sensing element in active suspension applications, and in other applications concerning vehicle dynamics. The success of silicon accelerometers in the automotive field is a result of the combination of excellent reliability and good performance at a price which is much lower than any other acceleration sensing element. An epipoly acceleration sensor has been developed in order to demonstrate the potential of epipoly structures in acceleration sensing.

In this chapter the reader is first introduced in the general principle of acceleration sensing, together with some basic mathematics on acceleration sensors. Then two examples of commercially available silicon acceleration sensors will be given. Subsequently the design of two epipoly accelerometers will be described, followed by measurement results. At the end of this chapter some conclusions will be drawn.
4.2 Introduction to silicon acceleration sensors

An acceleration sensor consists of a seismic mass which is suspended by a spring. An acceleration on the mass results in a force which is counterbalanced by a reaction force of the spring. In order to obtain an output signal, the position of the mass or the deformation of the spring is measured. A damping force is needed to suppress unwanted mechanical resonance at the resonance frequency of the mass-spring system. Usually a thin air film between the moving mass and stationary parts of the accelerometer structure is provides this force. The mass-spring structure can be fabricated using bulk- [4.1], surface- [4.2], and epi-micromachining processes, as well as in SCREAM [4.3], LIGA [4.4] and other micromachining methods.

4.2.1 Analytical model of an accelerometer

A mechanical model of an acceleration sensor is given in figure 4-1. The sensor consists of a mass, which is suspended by a spring and damped by a damper. This model will be used to introduce a basic analytical model about the mechanical behaviour of acceleration sensors.

![Mass-spring system](image)

Fig. 4-1 Mass-spring system.
4.2 Introduction to silicon acceleration sensors

Let us consider the system described in figure 4-1. According to Newton's second law of motion an acceleration of the system will result in a force on the mass via,

\[ F_{\text{mass}} = ma \]  \hspace{1cm} (4-1)

where \( F_{\text{mass}} \) is the force on the mass, \( a \) is the applied acceleration and \( m \) is the mass of the mass. This force will cause the spring to be elongated or shortened until the force is counterbalanced by a reaction force of the expanding spring via Hooke's law,

\[ F_{\text{spring}} = -k\Delta z \]  \hspace{1cm} (4-2)

where \( F_{\text{spring}} \) is the reaction force of the spring, \( k \) the spring constant and \( \Delta z \) the elongation of the spring. Together, the mass and the spring determine mechanical sensitivity \( S_{\text{mech}} \) of the sensor,

\[ S_{\text{mech}} = \frac{\Delta z}{a} = \frac{m}{k} \]  \hspace{1cm} (4-3)

and the mechanical resonance frequency \( \omega_0 \)

\[ \omega_0 = \sqrt{\frac{k}{m}} \]  \hspace{1cm} (4-4)

Note that the product of the square of the resonance frequency and sensitivity of the sensor is constant. As a result a sensor with a high mechanical sensitivity will always have a low resonance frequency.

The behaviour of the acceleration sensor around the resonance frequency is determined by the damping forces acting on the system. The damping force \( F_{\text{damper}} \) is coupled to the velocity \( v \) at which the mass is moving via the damping constant \( b \):

\[ F_{\text{damper}} = bv \]  \hspace{1cm} (4-5)
Epipoly accelerometers

The total second order behaviour of the mechanical sensitivity of a mass spring system can be described using the following equation:

$$ S = \frac{\Delta z}{a} = \frac{m}{k} \left( \frac{j\omega}{\omega_0} \right)^2 \frac{1}{\beta \omega_0 + 1} $$

(4-6)

where the damping coefficient $\beta$ is defined as:

$$ \beta = \frac{b}{\sqrt{k}m} $$

(4-7)

The critical value for the damping coefficient is $\sqrt{2}$. A lower value leads to a peak at the resonance frequency and a larger value makes the bandwidth lower than necessary as shown in figure 4-2.

![Graph showing the influence of the damping coefficient on the behaviour of the sensor around the resonance frequency.](image)

Fig. 4-2 Influence of the damping coefficient on the behaviour of the sensor around the resonance frequency.

When an acceleration sensor is developed, the designer needs to find an optimum compromise between sensitivity and bandwidth by choosing optimum values of the mass, spring constant, and damping forces. These values cannot be chosen freely, since the desired electrical properties and the possibilities of the fabrication process limit the designers freedom.
4.3 Example of commercially available sensors

In this section two completely different commercially available acceleration sensors will be discussed. The first sensor is an acceleration sensor of which millions have been sold by ICSensors Inc. This traditional piezoresistive bulk micromachined device does not have any on chip electronics, operates in open-loop mode, and is mainly used as crash test sensor in airbag applications. The second sensor, made by Analog Devices, is a surface micromachined part which is combined with CMOS read-out electronics. It is operated in a motional feed-back mode. These sensors are also used in air-bag applications, as well as in lower g-range applications such as vehicle dynamics. The two sensors represent the two most extreme approaches that can be found in micromachining.

4.3.1 The ICS 3021 acceleration sensor

This ICSensors acceleration sensor is produced in a bulk micromachining process [4.1]. The mass and beams are formed by etching parts of the bulk material. The sensitive direction of the sensor is perpendicular to the wafer plane. The mass and springs are completely made of monocrystalline silicon. In the beams piezoresistors are placed which are connected in a wheatstone bridge formation. When an acceleration is applied a displacement of the mass will deform the beams, causing the stress in the beams to change at the location of the piezoresistors. The stress in the piezoresistors will change their value and cause an imbalance in the Wheatstone bridge. The output of the Wheatstone bridge is in first order linearly dependent on the applied acceleration. The sensor has an output voltage which is large enough to allow off-chip electronics for further signal handling, such as amplification and temperature compensation. Mechanical protection and air damping of the sensor is achieved by the use of top and bottom caps which are fabricated in wafers which are bonded to the sensor wafer. An extra feature of the sensor is the addition of a self test electrode in the top cap of the sensor. With this electrode it is possible to electrostatically attract the mass and check the functionality of the sensor system. A schematic drawing of the sensor is given in figure 4-3.
4.3.2 The ADXL50

The Analog Devices ADXL50 is produced in a surface micromachining fabrication process, which is combined with a CMOS production process [4.2]. Both the sensor and the read-out electronics are combined on the same chip. This is mandatory, since the output signal of the sensor would be too small to be detectable by off-chip electronics. The sensor is sensitive in a direction parallel to the wafer surface. The mass, springs, and electrical connections are all made of polysilicon. The mass forms the center electrode of a differential capacitor, which is used for position measurement of the mass. An electrostatical feed-back system forces the mass back into the center position, and the feed-back signal is a measure for the applied acceleration. The same electrostatic force is used for the self test of the sensor. The capacitance is measured between beams which are connected to the mass, and beams which are connected to the substrate. Figure 4-4 shows the measurement principle of the sensor.

A photograph of the sensor is given in figure 4-5. In this picture the mass, interdigitized fingers for capacitance detection and springs are visible.
4.3 Example of commercially available sensors

Fig. 4-4 Measurement method used in the ADXL50

Fig. 4-5 Chip photograph of the ADXL50. (reprinted with permission of K. Chau)
4.4 Design of epipoly acceleration sensors

4.4.1 General lay-out of the sensors

Epipoly accelerometers have the same shape as surface micromachined accelerometers: A mass which moves parallel to the wafer plane is suspended by in-plane beams. The position of the mass is detected capacitively. In contrast to surface micromachined acceleration sensors, the read-out electronics are not integrated on the same chip. In this paragraph the design of two of the realized sensors will be described. The first accelerometer is the smallest of the two. It is fabricated in the process described in paragraph 3.7 of this thesis and will be referred to as sensor #1. The second acceleration sensor is made using the fabrication process which combines epipoly and porous silicon micromachining of section 3.8, and will be referred to as sensor #2. Both sensors have folded beams which suspend the mass. The mass is the center electrode of a differential capacitor, which is formed by beams which move together with the mass, and two pairs of counter electrodes which are fixed to the substrate. The upper and lower counter electrodes are electrically interconnected. When the mass moves upwards the total capacitance of the upper electrode increases, while the lower capacitance decreases. The imbalance of the two capacitors is a measure for the acceleration. A schematic drawing of the sensor layout is given in figure 4-6.

Fig. 4-6 Drawing of the realized epipoly acceleration sensors. Overall view (a) and close-up showing the dimensions used in the analytical description of the sensors (b).
4.4 Design of epipoly acceleration sensors

4.4.2 Sensitivity calculation

In order to estimate the electrical sensitivity of the sensors, the mass, spring constant, and nominal capacitance need to be calculated. The formulas which have been used to do this estimation will be presented first.

The mass, \( m \), of the sensor is calculated by multiplication of the area of the sensor, \( A_{\text{mass}} \), by the thickness \( h \) of the epipoly layer and the mass density \( \rho \) of the mass:

\[
m = A_{\text{mass}} h \rho
\]  
(4-8)

The capacitance of one finger, \( C_{\text{finger}} \), is estimated using the parallel plate estimation of a capacitor. The relation between capacitance and dimensions of the finger is:

\[
C_{\text{finger}} = \frac{\varepsilon l_{\text{finger}} h}{d}
\]  
(4-9)

In which \( \varepsilon \) is the electrical permittivity of the dielectric layer (air in this case, so \( \varepsilon = \varepsilon_0 \)), \( l_{\text{finger}} \) is the length of one finger, \( h \) is the thickness of the epipoly layer, and \( d \) is the thickness of the air gap between the fingers (see figure 4-6). The nominal capacitance \( C_0 \) is calculated by multiplying the capacitance of one finger, \( C_{\text{finger}} \), by the total number \( n \) of fingers.

\[
C_0 = n C_{\text{finger}}
\]  
(4-10)

The spring constant of the suspension can be derived from the spring constant of one single beam [4.5].

\[
k_{\text{beam}} = \frac{E h w^3}{l_{\text{spring}}^3}
\]  
(4-11)

where \( E \) is the Young's modulus of the beam material, \( h \) is the thickness of the beam, \( w \) is the width of the beam end \( l_{\text{spring}} \) is the length of the beam (see figure 4-6). Once one realizes that the mechanical equivalent of the folded flexure suspension of the mass is the same as 4 parallel springs,
which consist of a series of two springs, (see figure 4-7) it is not difficult to calculate the spring constant of the suspension system:

![Spring Diagram]

**Fig. 4-7** The suspension is formed of four parallel springs which consist of two springs in series.

\[
k = \frac{2Eh w^3}{l_{spring}^3}
\]  
(4-12)

From the above equation, the mechanical sensitivity, and the resonance frequency of the sensor can be calculated:

\[
S_{mech} = \frac{l_{spring}^3 \rho A_{mass}}{2Ew^3}
\]  
(4-13)

\[
\omega_0 = \sqrt{\frac{1}{kS_{mech}}}
\]  
(4-14)

Note that the thickness of the epipoly does not influence the mechanical sensitivity or the resonance frequency of the sensor.

Now it is time to consider the change in capacitance due to an applied acceleration. When an acceleration \(a\) is applied, the capacitor gap increases, or decreases by a value \(\Delta d\).

\[
\Delta d = S_{mech}a
\]  
(4-15)
This leads to a new value of the top capacitance, $C_{top}$, and the change in top capacitance, $\Delta C_{top}$, becomes:

$$\Delta C_{top} = C_{top} - C_0 = \frac{\varepsilon_0 nlh}{d - \Delta d} - \frac{\varepsilon_0 nlh}{d} = \frac{\varepsilon_0 nlh}{d} \left( \frac{\Delta d}{d - \Delta d} \right) \quad (4-16)$$

In practice, $\Delta d$ is small compared to $d$. In this case equation (4-16) can be simplified to:

$$\Delta C_{top} = C_0 \frac{\Delta d}{d} \quad (4-17)$$

In the same way, one can derive the change in capacitance for the bottom capacitance, which becomes:

$$\Delta C_{bottom} = -C_0 \frac{\Delta d}{d} \quad (4-18)$$

The output voltage of the read-out circuit which will be presented in section 4.4.3 depends on the carrier voltage, $V_{carrier}$, amplification, $H$, and imbalance in sensor top- and bottom capacitances via:

$$V_{out} = H V_{carrier} (C_{top} - C_{bottom}) = H V_{carrier} C_0 \frac{2 \Delta d}{d} \quad (4-19)$$

Now, we can substitute all variables of equation (4-19) with variables which depend only on the sensor dimensioning, and draw conclusions about the dependence of the electrical sensitivity, $S_e$, of the sensor on design parameters.

$$S_e = \frac{V_{out}}{a} = H V_{carrier} n\varepsilon_0 hl_{finger}^3 l_{spring}^3 \rho A_{mass} \frac{2}{d^2} \frac{1}{Ew^3} \quad (4-20)$$

Note that the electrical sensitivity depends strongly on the dimensioning of the spring, (to the third power) on the width of the capacitor gap, (square) and linearly on the layer thickness, number of fingers, length of capacitor fingers, area of the mass, carrier voltage, and amplification of the read-out circuit.
4.4.3 Read-out circuit

This subsection will describe the circuit which was employed to obtain an electrical output signal. There are several methods to convert the imbalance of a differential capacitor into an output voltage. The well known circuits that can be found in literature include the impedance bridge [4.6], the relaxation oscillator [4.7], CMOS switched capacitor circuits [4.8], and charge amplifiers [4.9].

Circuit description

The circuit of [4.9] was chosen to be used for the read-out of the realized sensors, because of its high sensitivity, simplicity, and availability. The aim of this circuit was to be able to characterize the mechanical properties of the sensors, and not to produce the best possible system. The system consists of a signal generator, the sensor capacitors, two charge amplifiers, a demodulator, and an instrumentation amplifier. The amplitude of the high-frequency carrier signal is modulated by the sensor capacitors. This signal is amplified by the charge amplifiers. Then the amplitude of the two signals is retrieved using a AM demodulator circuit. The difference in amplitude is fed into an instrumentation amplifier which produces the output signal. An overview of the system together with signal shapes is given in figure 4-8 [4.9].

![Circuit Diagram](image_url)

Fig. 4-8 Functional overview of the sensor system [4.9].

The electrical circuit which performs the function described in figure 4-8 is given in figure 4-9.
4.4 Design of epipoly acceleration sensors

![Electrical circuit diagram](image)

<table>
<thead>
<tr>
<th>sensor</th>
<th>charge amp.</th>
<th>AM demod.</th>
<th>instrumentation amplifier</th>
</tr>
</thead>
</table>

Fig. 4-9 Electrical circuit to convert the sensor capacitance imbalance into an electrical output signal.

**Circuit dimensioning**

When the carrier frequency is chosen well above the -3dB point of \( R_f \) and \( C_f \) and the parasitic effects are neglected the output signal of the charge amplifier \( V_{o1} \) will be:

\[
V_{o1} = V_{carrier} \frac{C_0 + \Delta C}{C_f} \tag{4.21}
\]

The value of the nominal capacitance of the sensors will be around 1pF. Therefore \( C_f \) is chosen to be 1pF. The carrier signal frequency is chosen to be 100kHz. \( R_f \) is needed to supply the input offset current of the opamp. \( R_f \) and \( C_f \) determine the lower boundary of the bandwidth of the charge amplifier. When \( R_f \) is made 10m\( \Omega \), the charge amplifier will function correctly from a frequency above 16kHz. The upper limit of the bandwidth of the charge amplifier is determined by the gain-bandwidth product of the opamp.

When the mechanical structure of the acceleration sensor is very sensitive to electrostatic forces the amplitude of the carrier signal cannot be made too large, since a too large signal would cause the mass to collapse against one of the counter electrodes. A low amplitude of the carrier voltage can result in a charge amplifier output signal amplitude which is below the
Epipoly accelerometers

forward diode voltage of a silicon diode. Therefore, germanium diodes have been chosen, which have a forward voltage of 0.2V. This makes it impossible to integrate this circuit on a silicon chip. This is not a problem, since in a real system synchronous detection would be a more elegant method to demodulate the signal, and synchronous detectors can easily be integrated.

The diodes, together with $R_d$ and $C_d$ act as a peak detector. This detector is used to measure the amplitude of the AM modulated signal. The values of $R_d$ and $C_d$ are a compromise between maximum attainable bandwidth of the demodulator circuit, and maximum allowable ripple. In our circuit values of 8.2k$\Omega$ and 22nF have been used, which gave satisfactory results.

The gain of the instrumentation amplifier is determined by resistors $R_1..R_7$. When $V_{o1}$ and $V_{o2}$ are well above the forward diode voltage the transfer function of this circuit is:

$$V_{out} = \frac{R_2 R_6}{R_1 R_4 + R_1 R_5} (V_{o1} - V_{o2})$$  \hspace{1cm} (4-22)

The total gain of the instrumentation amplifier, $H_{inamp}$, was set to 200 by choosing the following values: $R_1=1k\Omega$, $R_2,R_3=100k\Omega$, $R_4,R_5,R_6,R_7=10k\Omega$.

With these component values the output voltage of the sensor system with respect to the change in capacitance $\Delta C$ becomes:

$$V_{out} = V_{carrier} H_{inamp} \frac{2 \Delta C}{C_f} = V_{carrier} \frac{400 \Delta C}{10^{-12}}$$  \hspace{1cm} (4-23)

For a detailed analysis of the noise behaviour, resolution and other performance indicators of the circuit the reader is referred to [4.9].

4.4.4 Lay-out design guidelines

Before the lay-out of the acceleration sensors can be performed, a set of design guidelines is presented and justified. They are set in such a way that the fabrication process is robust. If the sum of the misalignment of two masks plus lateral overetching of the layers is smaller than 1$\mu$m the process will still produce working devices. In practice this condition can
4.4 Design of epipoly acceleration sensors

be met easily, since the alignment of the masks is done using a waferstepper, and the etching of the layers is done using anisotropic dry etching equipment. The design rules for the epipoly acceleration sensor process are given in figure 4-10. A vertical cross section is used here, since it is believed to give more insight in the layer stack.

![Diagram of epipoly acceleration sensor](image)

Fig. 4-10 Design rules for accelerometer fabrication process (vertical cross-section).

**Anchor dimensions (SAC)**

The minimum size of the holes in the sacrificial layer (SAC) which anchor the free standing structures to the substrate is $3 \times 3 \mu m^2$ (figure 4-10 a). When the length of the anchor is larger than $4 \mu m$, a width of $2 \mu m$ is acceptable. The minimum distance of an anchor point to the edge of any other layer is $1 \mu m$ (figure 4-10 b)

**Polysilicon interconnect layer (PS0)**

The PS0 layer is used to interconnect the various free standing parts of the structures. The minimum line width for interconnect is chosen to be $6 \mu m$ (figure 4-10 c), and the minimum spacing between two PS0 lines is $1 \mu m$ (figure 4-10 d). Furthermore, a PS0 layer is located under the freestanding structures. This layer is kept at the same potential as the free standing structures, in order to eliminate electrostatic forces between the freestanding structures and the substrate, which would result in vertical collapsing of the devices.
Epipoly accelerometers

Minimum trench width (PS1)

The minimum trench width in the epipoly layer (PS1) is chosen to be 2μm (figure 4-10 e), although working devices using trench widths of only 1μm have been fabricated. The practical reason for this design rule is that it is very difficult to avoid lateral sticking of devices with small trench widths. An exception is made for overtravel-stops, which have a slightly smaller trench width than the rest of the device.

Minimum beam width (PS1)

The minimum beam width of the epipoly layer (PS1) is chosen to be 2μm (figure 4-10 f), although from a robustness point of view a larger beam width is preferable. In general all beams are dimensioned at 4μm, except for the springs of the sensors, which can be 2μm or 3μm.

Overlap of construction layer over sacrificial layer (PS1 on SAC)

The epipoly construction layer (PS1) is dry etched using an oxide masking layer. This etch step should always stop on the underlying sacrificial oxide (SAC) layer, since the selectivity of the etching process towards polysilicon and silicon nitride would be too low to guarantee survival of these underlying layers. Therefore the minimum overlap of PS1 over SAC is chosen to be 1μm (distance b in figure 4-10).

Overlap of construction layer over poly 0 layer (PS0 on PS1)

The PS0-PS1 overlap is chosen to be 1μm (figure 4-10 g). PS0 and PS1 might be on top of each other for two reasons: a) The PS0 layer is used to interconnect parts which are made in PS1. b) The PS0 layer, which acts as a shield under the moving part, is partly extended under the stationary part of the structure, in order to avoid vertical steps on areas where trenches need to be defined in the PS1 layer.

Maximum underetch distance

The maximum underetch distance is set to 5μm from each side. This design rule results in a mass which has many perforations, which act as access holes for the sacrificial etchant. Larger underetch distances would lead to unacceptably long etch times.

The design guidelines are summarized in table 4-1.
4.4 Design of epipoly acceleration sensors

Table 4-1  Summary of design guidelines

<table>
<thead>
<tr>
<th>parameter</th>
<th>description</th>
<th>size (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>PS1 anchor</td>
<td>3</td>
</tr>
<tr>
<td>b</td>
<td>SAC over any PS</td>
<td>1</td>
</tr>
<tr>
<td>c</td>
<td>min. PS0 width</td>
<td>6</td>
</tr>
<tr>
<td>d</td>
<td>min PS0 spacing</td>
<td>1</td>
</tr>
<tr>
<td>e</td>
<td>min. PS1 trench width</td>
<td>2</td>
</tr>
<tr>
<td>f</td>
<td>min. PS1 beam width</td>
<td>2</td>
</tr>
<tr>
<td>g</td>
<td>overlap PS0-PS1</td>
<td>1</td>
</tr>
</tbody>
</table>

4.4.5 Sensor dimensioning and predicted performance

Many epipoly acceleration sensors have been designed and fabricated. The dimensioning and predicted performance of two of them, together with some specific lay-out details, will be presented in this paragraph. Note that the damping coefficient of the sensors is not calculated. The DC sensitivity and nominal capacitance were more important in these designs and these determine the resulting damping force. Moreover, the mathematical models for squeeze film damping which were found in literature did use approximations which are not valid for these epipoly acceleration sensors. This resulted in very large differences in the calculated damping coefficients for various mathematical damping models. As the aim of these accelerometers is to demonstrate the potential of the epipoly process the detailed mathematical analysis on squeeze film damping is not given.

Design of sensor 1

Sensor 1 is the smallest of the two sensors. This sensor is kept small in order to minimize the probability on lateral and vertical sticking. The sensor is fabricated in the fabrication process described in section 3.7. The thickness of the epipoly layer is 8μm. The length of and the width of the spring are 300μm and 3μm respectively. The mass consists of 13 vertical strips, which have a width of 4μm, and a length of 500μm. 27 horizontal beams, with a length of 625μm and a width of 4μm, cross the vertical strips of the mass. A part of 250μm at two sides of these beams (except for the outer two) is used to form the read-out capacitors, making the total number of capacitor fingers 24 per side. The capacitor gap is 2μm, and the
thickness of the epipoly layer is 8μm. The lay-out of the sensor is given in figure 4-11. Note that the number of both horizontal and vertical beams in the figure differs from the number of beams in the released design.

Fig. 4-11 Lay-out of sensor 1

When the lay-out of sensor 1 is compared to the general lay-out of the sensors of figure 4-6, one can note the following details:

The outer edges of the read-out electrodes on the mass are connected by vertical bars. This is done to avoid sticking of one single read-out electrode to a counter electrode. Note that the two outermost electrodes are stiffened by the use of a ladder structure.

The outer edges of the folded flexure springs are connected by vertical bars. This is also done to improve device yield. In versions without this vertical connection lateral sticking of the springs, which are the most
4.4 Design of epipoly acceleration sensors

flexible part of the sensor, was observed. Coupling the upper and lower spring helped to improve the yield.

In the real design, anchored islands containing overtravel-stops are located at the long sides of the mass, and at the ‘U-turns’ of the springs. A polysilicon shielding layer is located under the mass of the sensor, and driven by the same carrier signal.

**Predicted performance of sensor 1**

The following values were taken for the Young’s modules, density, and electrical permittivity: \(E=170 \text{ GPa}, \ \rho=2330 \text{ kg/m}^3 \text{ and } \varepsilon=8.85 \text{ pF/m} \).

The spring constant of the sensor becomes (see equation (4-12)):

\[ k = 2.7 \text{ m/N} \]

The approximate area of the mass is \(9.4 \times 10^{-8} \text{ m}^2\), making the total mass (see equation (4-8)):

\[ m = 1.74 \times 10^{-9} \text{ kg} \]

This results in a mechanical resonance frequency of (see equation (4-14)):

\[ f_{\text{res}} = 6.3 \text{ kHz} \]

The nominal capacitance of one single capacitor finger is 8.8\text{ fF} (see equation (4-9)), making the total nominal capacitance (see equation (4-10)):

\[ C_0 = 0.42 \text{ pF} \]

Now, let us calculate the change in capacitance for a 1g acceleration. The displacement of the mass for a 1g \((-10\text{ m/s}^2\) acceleration is (see equation (4-15)):

\[ \Delta d(1g) = 6.4 \text{ nm} \]

Making the change in capacitance of one capacitor (see equation (4-17)):

\[ \Delta C(1g) = 1.4 \text{ fF} \]
Design of sensor 2

Sensor 2 was made much larger than sensor 1 in order to obtain a higher electrical sensitivity. The device was fabricated using the combined epipoly/porous silicon process, which was described in section 3.8. The lay-out of the sensor is given in figure 4-12. The mass consists of 26 vertical beams, with a length of 475μm, and a width of 5μm. Connected to the mass are 23 horizontal beams, with a length of 1150μm, and a width of 4μm. The springs are 3μm wide, and have a length of 455μm. The capacitor plates are formed by the horizontal beams, which overlap 450μm with the read-out electrodes. The thickness of the epipoly layer is again 8μm.

Fig. 4-12  Lay-out of sensor 2.

Note that the uppermost and lowermost read-out electrodes are wider than the others. This was done to stiffen them in the sensitive direction as these electrodes contain the overtravel-stops. The read-out electrodes are only clamped at the sides of the sensor, because the substrate under the mass and read-out electrodes was electropolished to make the total mass to
substrate gap 10μm. A disadvantage of this structure is that it is no longer possible to vertically connect the far sides of the parts of the read-out electrodes, which are connected to the mass as in sensor 1. This, together with the larger area and lower spring constant make the fabrication of sensor 2 more sensitive to the sacrificial etch process step. The large substrate gap and rough substrate surface caused by the electropolished surface, on the other hand, facilitate the drying procedure, and have a positive effect on device yield.

**Predicted performance of sensor 2**

The spring constant of the sensor becomes (see equation (4-12)):

\[ k = 0.78 \text{ m/N} \]

The approximate area of the mass is \(1.7 \times 10^{-7} \text{ m}^2\), making the total mass (see equation (4-8)):

\[ m = 3.12 \times 10^{-9} \text{ kg} \]

This results in a mechanical resonance frequency of (see equation (4-14)):

\[ f_{res} = 2.5 \text{ kHz} \]

The nominal capacitance of one single capacitor finger is 16fF (see equation (4-9)), making the total nominal capacitance (see equation (4-10)):

\[ C_0 = 0.73 \text{ pF} \]

The displacement of the mass for a 1g acceleration is (see equation (4-15)):

\[ \Delta d(1g) = 40 \text{ nm} \]

Making the change in capacitance of one capacitor (see equation (4-17)):

\[ \Delta C(1g) = 14 \text{ fF} \]
4.5 Sensor measurement results

This section describes the results which were obtained from the measurements on the accelerometers which were described in section 4.4. Capacitance versus voltage (CV) measurements were performed before the sensors were packaged and connected to the read-out electronics. Then the DC response was measured, followed by the AC frequency response.

4.5.1 CV response

The CV response of two sensors of type 1 was measured. On one of the sensors, the beam width of the spring was 2µm, instead of the 3µm which was standard for sensor 1. The capacitance between the mass and one of the read-out electrodes was measured, and is plotted in figure 4-13. Note that the sensor with the 3µm spring is stiffer than the same device with a 2µm wide spring. For the stiff sensor the same electrostatic force leads to a smaller deflection, and thus a smaller change in capacitance. A small asymmetry in the CV response can be observed which is caused by parasitic capacitances of the device to the semiconducting substrate.

![Diagram](image)

Fig. 4-13 CV measurement for two sensors of type 1
4.5 Sensor measurement results

4.5.2 DC sensitivity

The fabricated sensors were connected to the read-out electronics described in section 4.4.3. For sensor 1 a 100kHz 600mV_{pp} carrier signal was used, and for sensor 2 the amplitude was set to 200mV_{pp}. The +1g and -1g output voltage of the sensors was measured and from these measurements the DC sensitivity was calculated.

**sensor 1**

The DC sensitivity of sensor 1 was 0.23 V/g. With an input carrier voltage of 600mV_{in}, this can be calculated back to a single sided capacitance change of (see equation (4-23)):

\[ \Delta C(1g) = 1.9 \text{pF} \]

This value is 30% larger than the calculated value in section 4.4.5. This can be explained by two reasons:

Formula 4-9, which was used to calculate the nominal capacitance, is based on a parallel plate approximation. In reality, fringe fields at the edges of the capacitor plates will result in a larger nominal capacitance and thus in a larger capacitance variation. If the length of the fingers is large, compared to the thickness of the epiply layer and the capacitor gap, the fringe field contribution from the ends of the finger can be neglected compared to the fringe field, resulting from the height of the finger. In that case, and under the assumption that the ratio between the capacitor gap and the epipoly layer thickness is smaller than 3, an expression, which gives capacitance values within 3% of the exact value, can be found as [4.10]:

\[
C_{\text{finger}} = \varepsilon_0 l_{\text{finger}} \left( \frac{h}{d} + \frac{1}{\pi} \left( 1 + \ln \left( 2 \pi \frac{h}{d} \right) \right) \right) \tag{4-24}
\]

The new calculated nominal capacitance, \( C_0 \), now becomes 0.57pF which is 30% larger than the value which was calculated using formula 4-9. The capacitance change of the sensor for a 1g acceleration now cannot be calculated using equation 4-17 anymore, since the assumptions which were used to arrive at this equation are no longer valid. So the deflection of the mass for 1 g acceleration is calculated. This leads to a new value for the capacitor gap. Then the capacitance for this new gap is calculated.
Epipoly accelerometers

difference of this calculated capacitance with $C_0$ is the sensitivity and is calculated to be 1.5fF/g.

The difference with the measured value lowers to a value of 24%. Apparently, the nominal capacitance is much more sensitive to fringe field effects than the capacitance variation.

Perfect anisotropy of the epipoly etching process was assumed when the sensor was dimensioned. In reality, underetching of the epipoly layer will result in a decrease in beam width. Therefore one would expect higher sensitivity, since the spring constant lowers with the third power of the beam width. This effect, however, is counterbalanced by an increase in capacitor gap and a decrease in sensor mass. For the DC behaviour of the sensor these effects cancel each other to a large extent, but the resonance frequency will decrease.

sensor 2

The DC sensitivity of sensor 2 was 0.66 V/g. With an input carrier voltage of 200mV, this can be calculated back to a single sided capacitance change of (see equation (4-23)):

$$\Delta C(1g) = 16.5 \text{ fF}$$

The difference with the predicted sensitivity is 11%. If we do not neglect the influence of fringe fields the predicted nominal capacitance becomes 0.98pF and the predicted sensitivity is 16.2fF/g, which is within 2% of the predicted value.

4.5.3 AC frequency response

The AC frequency response of both sensors was measured using a shaker, a reference accelerometer, and at a spectrum analyzer. Figure 4-14 shows a schematic view of the measurement set-up, while figure 4-15 shows a photograph of the set-up which was actually used. The shaker was exited by the output sweep signal of the spectrum analyzer. The acceleration of the shaker head is measured by both the device under test (DUT), and the reference accelerometer. The frequency response of the DUT is measured by dividing its measured signal by the reference accel output for all frequencies.
Fig. 4-14 *Frequency response measurement set-up.*

Fig. 4-15 *Photograph of a frequency response test in progress.*

It is important to keep the mass load of the shaker as low as possible. Therefore, only the part of the read-out electronics which really needs to be placed close to the sensor is mounted on the test fixture, together with the sensor. All parts of the fixture were glued to each other and IC sockets were not used, in order to avoid disturbing mechanical resonances in the test fixture. The sensor chip was securely fitted to the test fixture using super-glue. Figure 4-16 shows a photograph of the test head including the DUT and reference sensor.
Fig. 4-16 *Test head showing the reference accelerometer the device under test and a part of the charge amplifiers.*

Figure 4-17 shows the frequency response of the sensors. The response of sensor 1 is flat up to 3kHz. This is in the same order as the calculated value of 6kHz. A numerical value of the damping of the sensors cannot be well determined from these measurements, but sensor 1 does not seem to be over- or under-damped. The response of sensor 2 is flat up to 1.5kHz and shows an over-damped behaviour around the calculated resonance frequency of 2.5kHz.

![Frequency response of the acceleration sensors.](image)
4.6 Conclusions

In this chapter the theory, design, simulation, and measurement results of two epipoly acceleration sensors has been presented. The measured performance of the fabricated sensors agrees relatively well with the predicted values, especially when one considers that only simple analytical formulas have been used during the design of the sensors. It was demonstrated that both the standard epipoly process, and the fabrication process which combines epipoly and porous silicon, yield working devices.

4.7 References


Epipoly accelerometers


5.1 Introduction

In addition to the acceleration sensors of the previous chapter, two more demonstrator structures have been fabricated. In this chapter the working principles, fabrication, and testing of these structures will be presented. In section 5.2 thermal actuators will be presented and in section 5.3 an epipoly pressure sensor will be described. The conclusions of this chapter will be drawn in section 5.4.

5.2 Thermal actuators

5.2.1 Introduction

Thermal actuators use the thermal expansion of a material to achieve movement of a structure. The heated material can either be a gas, a fluid or a solid material. An example of a structure which utilizes thermal expansion of gas or fluid is a micropump. In this device the thermal expansion of a gas or fluid in a sealed cavity is used to deflect a
membrane. This deflection is then used to pump fluid or gas. An example of such a structure is shown in figure 5-1 [5.1]

![Diagram of micropump with heating element](image)

Fig. 5-1 Example of a micropump which utilizes thermal actuation [5.1].

A different approach is to use the thermal expansion of the heating element itself. This principle is used in bimetallic actuators and in buckling actuators. An example of a thermally actuated beam using the bimetallic principle is shown in figure 5-2. This actuation principle has been utilized to provide a self test feature on a bulk micromachined accelerometer [5.2]

![Diagram of heater on and off](image)

Fig. 5-2 Example of a micropump which utilizes thermal actuation.

### 5.2.2 Fabricated devices

Thermal actuators which are derived from stress measurement structures were built and tested. The first structure is shown in figure 5-3 [5.3]. When a voltage is applied between the two bondpads, a current will flow through the horizontal beams, causing them to heat up and expand. The expansion of these beams will result in a counterclockwise rotation of the vertical beam. Figure 5-4 shows the tip deflection at 0V and 15V supply voltage.
5.2 Thermal actuators

Fig. 5-3 Thermal actuator based on a stress measurement structure. Schematic view (a) and photograph (b).

Fig. 5-4 Tip deflection of the thermal actuator of figure 5-3, at a supply voltage of 0V (a) and 15V (b).

A second structure which was realized in epipoly, is based on buckling of a double sided clamped beam in a predetermined direction. The structure is shown in figure 5-5 [5.4]. Thermal expansion of this structure will lead to an upward movement of the center of the beam. In theory a large tip angle (α close to 180°) will result in maximum deflection. In practice, however, it is not advisable to make the angle too large, since in this case the beam will also start to deflect out of plane. The beam structure was originally introduced as a stress measurement structure in [5.4].
Fig. 5-5  *Thermal actuator based on buckling of horizontal expanding beams.*

Figure 5-6 shows a photograph of a realized device. In this device two buckling beams which move towards each other are combined. The horizontal beams are not straight as in figure 5-5 but have a staircase structure. This is done to facilitate the fabrication of the photomask. Two different structures with a length, \( l \), of 300\( \mu \)m and 180\( \mu \)m and a height, \( h \), of 7\( \mu \)m and 4\( \mu \)m respectively were fabricated and two of each were measured. A vertical beam with a micrometer scale is attached to the buckling beams in order to be able to measure the deflection of the device when a current is applied. The value of the deflection is measured by observing the structure though a microscope. This measurement is not very accurate since the pitch of the scale is 4\( \mu \)m, but it can still give some insight in the quantitative behaviour of the actuator.

Fig. 5-6  *Photograph of a realized device.*

Figure 5-7 shows the deflection vs. power curve of the devices. It can be seen that more power is needed to obtain the same deflection for the short device.
5.2 Thermal actuators

![Graph showing power vs. displacement for two actuators with lengths 180\mu m and 300\mu m.]

Fig. 5-7  *Deflection vs. power curve for four fabricated actuators, two with a length of 180\mu m and two with a length of 300\mu m.*

Now, let us have a closer look at the expected behaviour of the thermal actuators. The beam is uniformly heated by the current which flows through the beam. The beam cools down by a heat flow from the beam towards the environment. Mechanisms for heat loss are thermal conduction, radiance, and convection. Silicon is an excellent thermal conductor, so it is expected that thermal conduction is the main heat loss mechanism here. The temperature of the bondpads is constant since these have a very low heat resistance towards the thermal conducting substrate. If the thermal conductivity is constant, and the heat generation is uniform, the relation between thermal conduction and heat generation is [5.5]

\[
k \frac{d^2 T(x)}{dx^2} = -q_G
\]

(5-1)

where \(q_G\) is the rate of heat generation per unit volume, \(k\) is the thermal conductivity of the beam, and \(T(x)\) is the temperature profile of the beam. Integrating this expression once gives:

\[
\frac{dT(x)}{dx} = -\frac{q_G}{k} x + C_1
\]

(5-2)
One last integration leads to the temperature distribution in the beam:

\[ T(x) = -\frac{q_G}{2k}x^2 + C_1x + C_2 \]  

(5-3)

The values of \( C_1 \) and \( C_2 \) are determined by the boundary equations. In the fabricated actuators the temperature at \( x=0 \) and \( x=L \) is the same, namely \( T_{amb} \). In this case the temperature distribution becomes:

\[ T(x) = \frac{q_G L^2}{2k} \left[ x - \left( \frac{x}{L} \right)^2 \right] + T_{amb} \]  

(5-4)

The temperature distribution is parabolic and symmetric about the center of the beam. The maximum temperature at \( x=L/2 \) is:

\[ T_{max} = T_{amb} + \frac{q_G L^2}{8k} \]  

(5-5)

So the maximum temperature of the beam is proportional to the generated heat per unit volume and to the square of the beam length.

The thermal expansion of the beam is proportional to the temperature change of the beam. If the temperature of the beam is uniform the change in length of the beam is

\[ \Delta L = \beta L (T - T_{amb}) \]  

(5-6)

Where \( \beta \) is the thermal expansion coefficient of the beam. In our case the temperature of the beam is not uniform, so the change in length of the beam must be calculated by integration of the temperature distribution:

\[ \Delta L = \beta \int_0^L (T(x) - T_{amb}) \, dx = \frac{\beta q_G L^3}{12k} \]  

(5-7)

Now that the expansion of the beam is known it is possible to calculate the deflection of the actuator using the Pythagorean theorem on a triangle with sides \( l/2, L/2 \) and \( h \) (see figure 5-8).
5.2 Thermal actuators

Fig. 5-8 Triangle used to calculate the deflection of the thermal actuator.

When the beam heats up the length of the diagonal of the triangle will increase with a value of $\Delta l/2$, while the horizontal length remains unchanged. This means that the value $\Delta h$, which is the deflection, can be calculated using:

\[
(h + \Delta h)^2 = \left(\frac{L + \Delta l}{2}\right)^2 - \left(\frac{l + \Delta l}{2}\right)^2
\]  

(5.8)

The only missing variables, which are needed to predict the behaviour of the actuators are the thermal expansion coefficient, $\beta$, and the thermal conductance, $k$, of silicon which are $2.6 \times 10^{-6}$ K$^{-1}$ and 150 W m$^{-1}$ K$^{-1}$ respectively. The behaviour of the actuators was predicted using the dimensions and constants mentioned earlier in this section. A plot of the calculated and measured deflection of the devices is given in figure 5-9.

From this figure it is clear that the order of magnitude of the deflection is the same as the measured deflection. The measured deflection is always smaller than the calculated deflection. This is not a surprise, since the heat losses due to radiation, and heat conduction through the thin air gap between the beam and the substrate, were neglected in the calculations. These effects also explain why the difference between calculated and measured behaviour is larger for the larger structure. The heat loss will be higher for a larger structure because both the maximum temperature will be higher (800°C vs. 490°C for a power of 100 mW), and the area interacting with the environment is larger. In the calculations the energy which is needed to bend the beams was also neglected. This too contributes to a lower measured value of the deflection.
5.3 Pressure sensors

5.3.1 Introduction

Silicon bulk micromachined pressure sensors were first fabricated using isotropic etching in 1962 [5.6]. One of the first devices which was made using anisotropic etching of KOH was made in 1984 [5.7]. The same technique, using EDP and electrochemically controlled etching, was applied to a silicon diaphragm pressure sensor in 1985 [5.8]. In this case the thickness of the diaphragm was 20 μm and the area was 1×1mm². Surface micromachined pressure sensors have been made using LPCVD polysilicon membranes [5.9]. The membrane deflection of the sensors is usually measured using capacitive or piezoresistive techniques.

The piezoresistive technique utilizes a half or full Wheatstone bridge configuration. The advantage of this read-out principle is the simplicity. No extra electronic circuitry is needed since the output voltage of the Wheatstone bridge is directly proportional to the applied pressure. A disadvantage however, is the high temperature sensitivity of this technique, which can be eliminated by the use of an external temperature compensation circuit [5.10].

Fig. 5.9 Calculated and measured deflection of the thermal actuators.
The capacitive read-out method has the advantage of a low temperature sensitivity, but requires more complicated read-out circuitry to obtain an output signal. Moreover, a counter electrode is needed to form a capacitor, which makes it almost impossible to use this technique in a differential pressure sensor.

The most important part of a silicon pressure sensor is the deflecting membrane. This diaphragm can either be a simple square or a membrane with a bossed centre. The last method is usually used in low-pressure ranges. These two structures are given in figure 5-10.

![Diaphragm and Bossed Membrane](image)

Fig. 5-10 Pressure sensor configurations: (a) single diaphragm and (b) membrane with bossed center.

The properties of pressure sensors are largely sensitive to both the lateral and vertical dimensions of the membrane. The lateral dimensions are controlled by the back-side mask, the anisotropy of the etchant and the thickness of the wafer. An etch stop technique is required to accurately control the vertical dimensions of the membrane. These techniques were already discussed in section 2.2.

A new technique is the use of epipoly as membrane material. The epipoly layer is grown on top of an oxide layer which serves as an etch stop. This technique is similar to the use of SIMOX wafers, but is much cheaper since it does not require expensive SIMOX wafers. A disadvantage is the polycrystalline structure of the layer, which makes it impossible to use crystal directions with optimum performance for the piezoresistors. As already mentioned in section 3.6, the epipoly growth can be combined with the simultaneous growth of monocrystalline epi, which can be used to fabricate read-out electronics.
5.3.2 Fabrication process

The basic fabrication process for a pressure sensor integrated with a standard single crystal epi for bipolar electronics, is given in figure 5-11.

Fig. 5-11 Pressure sensor fabrication process.

First, the oxide and polysilicon seed layer are formed where epi-poly is required. (figure 5-11(a)). Without this polysilicon layer, the epi-poly would be of poor quality. The epi-poly and the standard single crystal epi for the electronics are grown in a single step (figure 5-11(b)). The basic deposition parameters for the epi are the same as for the epipoly structures described in chapter 3.2.2. Since the epi layer takes it crystal information from the substrate areas of single crystal silicon will be covered with
single crystal epi. A nitride layer is deposited on the epipoly in order to
shield it from oxygen penetration during the bipolar fabrication steps.
5-11(c).

At the end of the standard processing (bipolar devices not shown in this
figure) the nitride is stripped. Then piezoresistors were formed by ion
implantation of boron. With epi-poly either n or p type piezoresistors can
be used since they do not rely on crystal orientation, as is the case with
single crystal devices. Then a thin LPCVD nitride layer is grown, followed
by an anneal. Now, contact windows are opened and metallization is
formed, as shown in figure 5-11(d). The wafers are then etched in KOH
from the backside stopping on the oxide layer. This results in the
membrane shown in figure 5-11(e). At this stage the membrane is under
stress due to the presence of the oxide. This could be observed by buckling
of the membranes. Stress in these thermal oxides have been measured to
be in the range of 300-400MPa [5.11]. Therefore the oxide is removed
using a short HF vapor etch. The final structure is given in figure 5-11(f).
A detailed process description can be found in the appendix.

In this example the piezoresistors are formed in the epi-poly. Alternatively
these can be formed in LPCVD polysilicon layers deposited on top of the
epi. If capacitive read-out is used the metallization layer can be used as the
electrode.

5.3.3 Measurements

A schematic view of the device is given in figure 5-12(a) and figure
5-12(b) shows a photograph of a packaged device. The pressure is applied
via a tube at the back-side of the package. The membranes were 2.5mm x
2.5mm x 4μm.

Measurements have been performed on the realized pressure sensors. Each
resistor had a value of approximately 15kΩ, representing a sheet resistance
of approximately 50Ω/square at room temperature. The resistance as a
function of temperature is given in figure 5-13. This gives a temperature
coefficient of resistance of 0.07%/°C at room temperature. The bridge
output as a function of pressure is given in figure 5-14. This bridge was a
full Wheatstone bridge constructed using resistors both perpendicular and
parallel to the edge of the membrane.

The sensitivity at 0.2 bar was estimated to be 97mV/bar for a supply
temperature of 5V.
Fig. 5-12  *Planar view of the pressure sensor (a) and packaged device (b).*

Fig. 5-13  *Resistance as a function of temperature*
5.4 Conclusions

Epipoly thermal actuators and a bulk micromachined pressure sensor have been successfully built and tested.

The thermal actuators are based on stress measurement structures, and show a displacement which is proportional to the applied power. These devices can be used to extend the functionality of mechanical sensors by the addition of a self-test feature. A simple model was developed, which does not take heat loss due to radiation, and air conduction into account, and also neglects the energy which is needed to bend the devices. As a result of these simplifications the measured deflection is lower but in the same range as the predicted deflection.

The use of epi-poly in the fabrication of pressure sensors yields a complete etch-stop without the use of complicated etch-stop techniques. Although this device represents a departure from single crystal device, experiments have shown that epi-poly has excellent mechanical properties for micromechanical devices and can be applied to produce piezoresistive devices.
5.5 References


New micromachining techniques using layers grown in an epitaxial reactor have been presented. Devices which show the potential of these techniques have been designed, fabricated, and tested. Epi micromachining processes combine the advantages of both bulk and surface micromachining. The area of the structures is relatively small, while the output signals are large enough to allow off-chip read-out circuitry.

In MELO epi micromachining, structures are fabricated in a layer which is laterally grown over a sacrificial oxide layer. This technique is useful in the fabrication of single monocrystalline beams, but is not useful when large areas of underetched epi need to be fabricated.

In porous silicon epi micromachining, a top layer of the substrate is used as the sacrificial layer. An advantage of this technique is the large sacrificial layer thickness which can be achieved by the porous silicon process, and the rough surface of the layer underneath the fabricated structures. Both properties help to avoid sticking of the fabricated structures.

Epipoly is polycrystalline silicon which is grown using an epitaxial reactor. The high growth rate of this material makes it possible to grow 4μm to 8μm polysilicon layers in less than 10 minutes. Directly after
Conclusions

deposition the mechanical strain level of epipoly layers is very low. Oxidation of epipoly layers leads to high compressive strain levels, due to oxygen penetration into the layer. This unwanted strain can be avoided by shielding the epipoly layer from oxygen by the use of a nitride protection layer. This technique is similar to the LOCOS processes which are commonplace in CMOS device fabrication.

Two types of lateral acceleration sensors have been fabricated using the epipoly process. The first sensor was made using a conventional oxide sacrificial layer, and showed a sensitivity of 0.23V/g and a bandwidth of 3kHz. The second sensor was produced in the combined epipoly and porous silicon micromachining process. The sensitivity of this sensor was 0.66V/g and the bandwidth was 1.5kHz. The nominal capacitance and sensitivity of the fabricated devices was well in agreement with the predicted performance.

To further demonstrate the capabilities of the epipoly layer thermal actuators and a pressure sensor have been designed, fabricated and measured. Discrepancies between the measured and predicted behaviour of the thermal actuator can be explained by some invalid assumptions in the model which was developed. The pressure sensor proves that it is possible to fabricate piezoresistive devices in the epipoly layer.

This work clearly demonstrates the usefulness of the epitaxial reactor to grow layers for micromachining purposes. Epipoly offers the flexibility to use both p- and n-type material to construct a variety of micromechanical devices. This work has shown it’s suitability for accelerometers, pressure sensors and thermal actuators.
Appendix

Fabrication process flows

On the next pages the exact process flows of the conventional acceleration sensor fabrication process, the combined epipoly/porous silicon process, and epipoly pressure sensor process is presented.
Conventional epipoly process for acceleration sensor fabrication

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     | t 92 min |
| 19 | Anneal (in situ) in N₂ | T 605 °C  
     | t 60 min |
| 20 | Epipoly growth 8μm | T 1050 °C  
     | P 60 Torr  
     | DCS 360 sccm  
     | dope As 10¹⁶cm⁻³  
     | t 8 min |
| 21 | PECVD oxide 2μm | Novellus |
| 22 | Alignment mark clear | Job epi 4.0  
     | E 150 |
| 23 | Dry etch silicon (remove epipoly from URK) | Drytek silicon 2 times |
| 24 | Wet pccvd oxide strip | BHF 1:7 |
| 25 | Epipoly dope | Type P / As / B  
     | Energy 100 KeV  
     | Dose 5e15 |
| 26 | Nitride deposition 300 nm | T 850 °C  
     | p 150 mTorr  
     | DCS 170 sccm  
     | NH₃ 30 sccm  
     | t 41 min |
| 27 | dope drive in | T 1100 °C  
     | t 280 min |
| 28 | Strip back side of wafers | dry, wet, until silicon |
| 29 | Wet strip nitride | H₃PO₄ 157 °C  
     | t 3 hr |
| 30 | Al/Si deposition 1.4 μm | in trikon Ω |
| 31 | Al Patterning | E 300 resist special  
     | IC |
| 32 | Al etch | Al etch 35 °C |
| 33 | Poly dip etch | HF/HNO₃  
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<td>Dilute for electropolishing</td>
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<td>I 1.5 mA t 60 min (= 60 mA/cm\textsuperscript{2})</td>
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## Epipoly pressure sensor process

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<th>Step</th>
<th>Parameters</th>
<th>Mask</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Starting material</td>
<td>P-type boron (100) process wafers, resistivity 2.5 Ωcm</td>
<td></td>
</tr>
<tr>
<td>2 Marker oxidation 1</td>
<td>T 1100 °C, O₂ 2.25 slm, H₂ 3.85 slm</td>
<td></td>
</tr>
<tr>
<td>535-550 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 Alignment mark litho</td>
<td>E 150</td>
<td>comurk</td>
</tr>
<tr>
<td>4 Window etch</td>
<td>BHF 1:7</td>
<td></td>
</tr>
<tr>
<td>5 Marker oxidation 2</td>
<td>T 1100 °C, O₂ 2.25 slm, H₂ 3.85 slm</td>
<td></td>
</tr>
<tr>
<td>535-550 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 Poly seed deposition</td>
<td>T 575 °C, p 150 mTorr, SiH₄ 45 sccm, t 92 min</td>
<td></td>
</tr>
<tr>
<td>200nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 Anneal (in situ) in</td>
<td>T 605 °C, t 60 min</td>
<td></td>
</tr>
<tr>
<td>N₂</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8 Epipoly growth</td>
<td>T 1050 °C, P 60 Torr, DCS 360 sccm, dope As 10¹⁶cm⁻³, t 4 min</td>
<td></td>
</tr>
<tr>
<td>4μm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9 PECVD oxide</td>
<td>Novellus</td>
<td></td>
</tr>
<tr>
<td>1μm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 Alignment mark clear</td>
<td>Job epi 4.0, E 150</td>
<td>open</td>
</tr>
<tr>
<td>11 Trench etch</td>
<td>Drytek silicon</td>
<td></td>
</tr>
<tr>
<td>(remove epipoly from URK)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12 Wet pcvd oxide strip</td>
<td>BHF 1:7</td>
<td></td>
</tr>
<tr>
<td>13 Nitride deposition</td>
<td>T 850 °C, p 150 mTorr, DCS 170 sccm, NH₃ 30 sccm, t 41 min</td>
<td></td>
</tr>
<tr>
<td>300 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14 Alipoly anneal</td>
<td>T 1100 °C, t 280 min</td>
<td></td>
</tr>
<tr>
<td>15 Strip back side of wafers</td>
<td>dry, wet, untilt silicon</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<tr>
<td>---</td>
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<td>---</td>
</tr>
<tr>
<td>16</td>
<td>Wet strip nitride</td>
<td>H&lt;sub&gt;3&lt;/sub&gt;PO&lt;sub&gt;4&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>t</td>
</tr>
<tr>
<td>17</td>
<td>Piezoresistor litho</td>
<td>E</td>
</tr>
<tr>
<td>18</td>
<td>Piezoresistor implant</td>
<td>Type B</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Dose 1e15</td>
</tr>
<tr>
<td>19</td>
<td>Nitride deposition 100 nm</td>
<td>T</td>
</tr>
<tr>
<td></td>
<td></td>
<td>p</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NH&lt;sub&gt;3&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>t</td>
</tr>
<tr>
<td>20</td>
<td>Anneal</td>
<td>T</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N&lt;sub&gt;2&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>t</td>
</tr>
<tr>
<td>21</td>
<td>Contact litho</td>
<td>E</td>
</tr>
<tr>
<td>22</td>
<td>Al/Si deposition 0.6 µm</td>
<td>in trikon</td>
</tr>
<tr>
<td>23</td>
<td>Al Patterning</td>
<td>E</td>
</tr>
<tr>
<td>24</td>
<td>Al etch (wet)</td>
<td>Al etch 35 °C</td>
</tr>
<tr>
<td>25</td>
<td>Poly dip etch</td>
<td>HF/HNO&lt;sub&gt;3&lt;/sub&gt;</td>
</tr>
<tr>
<td>26</td>
<td>Alloy</td>
<td>T</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N&lt;sub&gt;2&lt;/sub&gt;/H&lt;sub&gt;2&lt;/sub&gt;</td>
</tr>
<tr>
<td>27</td>
<td>PECVD nitride 0.5µm on back side</td>
<td>Novellus</td>
</tr>
<tr>
<td>28</td>
<td>Back side litho</td>
<td>E</td>
</tr>
<tr>
<td>29</td>
<td>Window patterning in drytek</td>
<td>recipe sin15bak</td>
</tr>
<tr>
<td>30</td>
<td>Wet KOH etch</td>
<td>KOH</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T</td>
</tr>
<tr>
<td></td>
<td></td>
<td>t</td>
</tr>
<tr>
<td>31</td>
<td>Oxide strip</td>
<td>In HF vapor</td>
</tr>
<tr>
<td>32</td>
<td>Dice</td>
<td></td>
</tr>
</tbody>
</table>
Summary

This thesis describes the development of new micromachining techniques using layers grown in an epitaxial reactor. After a general introduction in micromachining, the development of three new micromachining techniques is presented. Two of these techniques were used to fabricate acceleration sensors, thermal actuators and pressure sensors.

Chapter 1 introduces the reader into the world of micromachining. If sensors and actuators can be produced using fabrication techniques, similar to those of chips, the price to performance ratio will improve dramatically. This will lead to lower cost and higher reliability of systems consisting of sensors, electronic circuitry, and actuators.

Chapter 2 gives an overview of several micromachining techniques which are used to produce miniature sensors and actuators. Bulk micromachining yields relatively large devices which are rugged, and produce large output signals. Surface micromachined structures are usually smaller than their bulk-micromachined counterparts, and yield small output signals. The small output signals of surface micromachined parts make on-chip integration of read-out electronics mandatory.

Chapter 3 presents epi micromachining methods. Epi micromachined devices are constructed using a layer which is grown in an epitaxial reactor. Devices which are fabricated in these techniques combine the advantages of both surface- and bulk micromachining methods: They consume the same small area as their surface micromachined counterparts, but produce a much larger output signal due to their larger vertical dimensions. Therefore on-chip integration of read-out electronics is no longer mandatory. The chapter starts with a brief introduction of silicon epitaxy, followed by a presentation of sacrificial etching techniques. Subsequently the development of three epi micromachining techniques is presented: MELO, Porous silicon epi micromachining, and epipoly.

Chapter 4 presents the theory, design, and measurement results of epipoly acceleration sensors. The measured response of the sensors is in good agreement with the simulated behaviour.

In chapter 5 epipoly two more epipoly structures are presented. A simple thermo-electrical model which predicts the behaviour of thermal actuators is described. This model agrees with the measured response of the
fabricated actuators. The measured response from piezoresistive epipoly pressure sensors show that these sensors can serve as a low-cost alternative to pressure sensors which are fabricated using ECE.
Samenvatting

Dit proefschrift beschrijft de ontwikkeling van nieuwe micromachining technieken, die gebruik maken van lagen die gegroeid worden in een epitaxiale reactor. Na een algemene inleiding over bestaande micromachining methoden wordt de ontwikkeling van drie nieuwe methoden gepresenteerd. Twee van deze methoden zijn later gebruikt om versnellingsensoren, thermische actuatoren en drukssensoren te maken.

In hoofdstuk 1 wordt de lezer geïntroduceerd in de wereld van micromachining. Als sensoren en actuatoren geproduceerd kunnen worden in fabricageprocessen, die nauw verwant zijn aan de fabricageprocessen voor elektronica, zal de prijs/prestatieverhouding dramatisch verbeteren. Dit zou leiden tot een sterke kostendaling en verhoogde betrouwbaarheid van systemen die bestaan uit sensoren, elektronica en actuatoren.

Hoofdstuk 2 geeft een overzicht van reeds bestaande technieken voor de fabricage van microsensoren en actuatoren. De bulk micromachining techniek leidt tot relatief grote en sterke structuren die grote uitgangssignalen produceren. Surface micromachining aan de andere kant leidt tot veel kleinere structuren die kleinere uitgangssignalen produceren. Deze kleine signalen maken het vaak noodzakelijk om uitleeselektronica te integreren op dezelfde chip die ook de micromechanische structuur bevat.

In hoofdstuk 3 worden epi micromachining methoden gepresenteerd. Epi micromachined structuren zijn gevormd in lagen die gegroeid zijn in de epitaxiale reactor. Deze methoden combineren de voordelen van surface- en bulk micromachining: De oppervlakte die ze innemen op een chip is even klein als bij surface micromachined structuren en ze produceren veel grotere uitgangssignalen, doordat ze in een veel dikkere laag gemaakt worden. Hierdoor is het niet langer noodzakelijk om uitleeselektronica te integreren op dezelfde chip. Het hoofdstuk begint met een korte introductie in silicium epitaxie. Vervolgens worden verschillende methoden voor het etsen van offerlagen gepresenteerd. Daarna wordt de ontwikkeling van drie epi micromachining methoden gepresenteerd, namelijk MELO, poreus silicium epi micromachining en epipoly.

Hoofdstuk 4 beschrijft de ontwikkeling van epipoly versnellingsensoren. Nadat de benodigde theorie over versnellingsensoren is gepresenteerd, wordt het ontwerp en verwachte gedrag van twee van deze sensoren
beschreven. Vervolgens worden meetresultaten van gerealiseerde versnelligssensoren vergeleken met het verwachte gedrag. De gemeten respons komt goed overeen met het verwachte gedrag.

In hoofdstuk 5 worden twee andere epipoly structuren gepresenteerd. Een sterk vereenvoudigd model voor het gedrag van epipoly thermische actuatoren is ontwikkeld en vergeleken met het gedrag van gefabriceerde actuatoren. Het verwachte gedrag blijkt redelijk overeen te komen met het daadwerkelijke gedrag van de gefabriceerde structuren. Ook zijn epipoly drukssensoren geproduceerd. Metingen aan deze sensoren tonen aan dat het mogelijk is om piezoresistieve duksensoren te maken met behulp van epipoly technieken. Deze techniek kan dienen als een goedkoop alternatief voor de produktie van duksensoren die anders met behulp van ECE gemaakt worden.
Acknowledgments

The work presented in this thesis would not have been possible without the help of many people. I would like to thank all the members of the Electronic Instrumentation Laboratory and the DIMES IC processing crew for creating a stimulating working environment. The discussions about technological problems as well as about activities not related to work were always pleasant. Especially I would like to thank the following people:

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M. Bartek, Y.X. Li, P. Gennissen, P.J. French and R.F. Wolffbenettel, 
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electronics in SEG silicon”, Proceedings Eurosensors 94, Toulouse, 

P.T.J. Gennissen, M. Bartek, P.J. French, P.M. Sarro and R.F. 
Wolffbenettel, "Automatic etch-stop on buried oxide using epitaxial 
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27 September 1995, pp 593-596.

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in a single deposition step", Proceedings National Sensor Conference, 

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G.M. O'Halloran, M. Kuhl, P.M. Sarro, P.T.J. Gennissen and P.J. French, 
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About the Author

Paul Gennissen was born in Rotterdam, the Netherlands, on October 18, 1968. He received his M.S. degree in electrical engineering from Delft University of Technology, Delft, the Netherlands, in 1993. In the same year he worked 6 months for EG&G ICsensors Inc., Milpitas, Ca, U.S.A. In 1994 he started a postgraduate study on silicon microstructures at Delft University of Technology. In the same year he spent three months at the University of Michigan in Ann Arbor, Mi, U.S.A., as a visiting scholar, to work in their IC laboratory. Since 1995 he has been at the Laboratory for Electronic Instrumentation at Delft University of Technology, working towards a Ph. D. degree in the field of micromachining technology for smart sensor applications. During the last year of his Ph.D. research he worked for 5 months at Exar Corp, Fremont, Ca, U.S.A., where he worked on bulk micromachined capacitive acceleration sensors.