Fabrication of Al-based superconducting high-aspect ratio TSVs for quantum 3D integration

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ABSTRACT

We describe a microfabrication process that, thanks to a specifically tailored sidewall profile, enables for the first-time wafer-scale arrays of high-aspect ratio through-silicon vias (TSVs) coated with DC-sputtered Aluminum, achieving at once superconducting and CMOS-compatible 3D interconnects. Void-free conformal coating of up to 500 μm-deep and 50 μm-wide vias with a mere 2 μm-thick layer of Al, a widely available metal in for IC manufacturing, was demonstrated. Single-via electric resistance as low as 468 mΩ at room temperature and superconductivity at 1.25 K were measured by a cross-bridge Kelvin resistor structure. This work establishes the fabrication of functional superconducting interposers suitable for 3D integration of high-density silicon-based quantum computing architectures.

KEYWORDS

Through-silicon vias, superconducting, quantum

INTRODUCTION

Through-silicon vias (TSVs) are vertical conductive structures used to connect ICs or MEMS devices on the top surface of a silicon wafer with others at the bottom of the same wafer, or to use the wafer as interposer layer between two separate substrates. TSVs increase functional density and device performance while reducing interconnection-related parasitic effects [1-5]. Increasing interest has been recently directed toward the possibility of using TSVs at extreme cryogenic temperatures. Such interest was in particular boosted by the emergence and demonstration of silicon-based quantum computing, which need to operate at temperatures lower than 1 K [6]. CMOS circuitry is thereby also required for the control and readout of the many quantum bits (Qubits) required [7]. Therefore, TSV-based 3D integration is arguably necessary to pursue large scalable superconducting qubit systems, providing suitable connections between qubits- and CMOS-based devices (Figure 1).

Copper, doped polysilicon and tungsten are the most used materials for interconnections and filled vias in semiconductor industry, thanks to their good electrical conductivity and/or thermal stability [8, 9]. However, none of these materials is superconductive. Moreover, prior works on superconducting interconnections (i.e., indium bumps and TSVs with polymer-filled metallic liner [10, 11]) rely on materials or fabrication methods that are not CMOS-compatible or not easily scalable [12]. The microfabrication process that we present here enables for the first time TSVs with high-aspect ratio (up to 10) to be conformally coated with DC-sputtered Aluminum, and achieves at once superconducting and CMOS-compatible 3D interconnects.
undercuts. Hence the funnels were subsequently anisotropically plasma-etched, using a SF6- and CH3FS-based plasma generated in closer proximity of the substrate. This step removed the aforementioned undercuts and broadened the openings of the funnels. The aligned funnels at the other side of the wafer were fabricated in the same way. A protective layer of SiO2 deposited by plasma-enhanced chemical vapor deposition was then added on the bottom side of the wafer (Figure 2b), and the inner, cylindrical section of the vias was drilled by anisotropic sidewall etching, landing on the previously deposited SiO2 layer (Figure 2c). The wafer was then thoroughly cleaned through exposure to oxygen plasma and immersion in HF and HNO3 solutions. This procedure was required to clean the SiO2 surface after completing the etching process, and before growing an additional thermal SiO2 layer as electric via insulation (Figure 2d). Figure 3 shows micrographs of vias fabricated through a) a 300 μm-thick Si wafer and b) a 500 μm-thick Si wafer.

Figure 2: Sketches of cross-sections of a Si substrate showing the via fabrication process. a) Etching of bottom cavities, b) oxidation of bottom cavities and etching of top cavities, c) DRIE of vias, d) cleaning and thermal growth of SiO2 insulating layer e) double-side sputtering and lithographical patterning of Aluminum and TiN.

VIAS METALLIZATION

The second part of the process, the metallization of the vias (Figure 2e), was performed by sequential sputter depositions of Al followed by TiN capping layer on each side of the wafer using a cryo-pumped Trikon Sigma 204 sputter-coater with a base pressure of 10^{-10} Pa. Sputter-etching with Argon was used in between the depositions to remove any Al oxide formed in the TSVs. The depositions were performed with a substrate temperature of 25 °C, 50 sccm of Argon gas flow and a DC power of 1.3 kW on the 16” Al target. The chamber pressure was set to 226.65 Pa, obtaining an Al deposition rate of approximately 2.2 nm/s. The 20 nm-thin layer of TiN was deposited to protect Al from oxidation and damage during patterning and chemical cleaning. The TiN layer was deposited with a substrate temperature of 350 °C, 20 sccm of Argon gas flow, 70 sccm Nitrogen gas flow and 6 kW DC power on the 16” Ti target.

The micrographs in Figure 4 show the resulting vias after the metallization. Figure 4a shows 300 μm-deep TSVs coated with Al, evidencing the stacked layers of materials introduced during the fabrication process. A close-up of the metallized via is presented in Figure 4b. A cross-sectional view of the 500 μm-thick Si wafers (Figures 4c-d) clearly shows the uniformity of the coating on an array of high aspect-ratio vias.

The metallic layers were finally patterned on both sides of the wafer by optical lithography and inductively-coupled plasma etching at 25 °C using HBr (30 sccm) and Cl (20 sccm) as reaction gases and 500 W of RF power. An optical image of a fully processed Si wafer is shown in Figure 5.
VIAS CHARACTERIZATION

Electrical measurements were performed at both room and cryogenic temperature to characterize the fabricated, Al/TiN-coated vias. Single TSV resistance was measured using a cross-bridge Kelvin resistor structure (Figure 6) [13,14]. I-V measurements at room temperature were performed by means of a parameter analyzer and a multi-probe station. Current was applied at the I terminal of Figure 6b, and the ensuing voltage drop was measured across terminals $V_1$ and $V_2$. Cryogenic DC resistance through the vias was measured as a function of temperature using a standard 4-point probe method using a commercial adiabatic demagnetization refrigerator (ADR, Entropy GmbH).

EXPERIMENTAL RESULTS

The sidewalls of the TSVs were completely and conformally coated without voids by sputtering only 2 μm of Aluminum on both 300 μm and 500 μm-thick wafers (Figure 4). The Aluminum and capping TiN layers could be successfully patterned over the full surface on both sides of the wafer (Figure 5a).

The electrical resistance of a single via, located in the center of the cross-bridge Kelvin resistor structure, measured as low as 487±68 mΩ (Figure 7). Cryogenic resistance measurements are presented in Table 1. Two superconducting transitions were measured, respectively at ~1.25 K and ~1.32 K. The transition at ~1.25 K originates from the Al of the planar and funnel sections of the Kelvin resistor.
structure, where the sputtered Al film is thicker. The second transition at 1.32 K is associated to the transition of the Al film in the via, where the film is thinner than in the funnels. This is consistent with prior reports, as for Al the superconducting transition temperature increases for thinner films with higher sheet resistance [15].

Figure 7: I-V characterization of a single Al-coated TSV at room temperature. An ohmic behavior is observed for the investigated voltage range.

Table 1: Resistance vs temperature measurements for 300 μm deep Aluminum Through-silicon vias

<table>
<thead>
<tr>
<th>Temperature [K]</th>
<th>Resistance [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>300,00</td>
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</tr>
<tr>
<td>2,00</td>
<td>3,26</td>
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<td>1,32</td>
<td>1,35</td>
</tr>
<tr>
<td>1,25</td>
<td>0,00</td>
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</tbody>
</table>

CONCLUSION

Superconducting high-aspect ratio TSVs were demonstrated for both 300 and 500 μm-thick Si wafers. The fabrication of high-density TSVs with specifically funneled sidewalls enabled the conformal DC-sputtering of the full vias with Al, a superconductor compatible with any CMOS process. Four-terminal cross-bridge Kelvin resistor structures were fabricated for the TSVs electrical characterization at room and cryogenic temperature. Single-via resistance as low as 487 mΩ was measured for 300 μm-deep TSVs at 25 °C, and superconductivity was measured at 1.25 K. This works prompts the fabrication of superconductive interposer layers that can suit high-density 3D integration for Si-based quantum computing.

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REFERENCES


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