Stellingen (Propositions)

behorende bij het proefschrift

A New Synthetic Test Circuit for Ultra-High-Voltage Circuit Breakers

Baoliang SHENG

Delft, 21 December 1995

1. In the IEC and ANSI standards for high voltage circuit breakers the topology of test circuits for the creation of TRV waveform is not prescribed. This is an omission, because the topology of the test circuit is of great influence on the arc-circuit interaction around current zero.

In de IEC en ANSI voorschriften voor vermogenschakelaars wordt de topologie van het testcircuit, dat de TRV golfvorm genereert, niet voorgeschreven. Dit is een gemis, omdat de topologie van het testcircuit een grote invloed heeft op de boog-circuitinteractie rond stroomnul.

2. Computer calculations with arc model are a valuable and effective tool for the design and comparison of test circuits.

Computerberekeningen met boogmodellen zijn een waardevol en effectief hulpmiddel voor het ontwerpen en vergelijken van testcircuits.

3. As the synthetic techniques employed in producing the goods of daily life lower their cost, the synthetic techniques used in the high power laboratory decrease the testing cost and make it possible for a testing laboratory to simulate the actual electric power system.

Evenals de synthetische technieken bij het produceren van de dagelijkse consumptiegoederen, reduceren de synthetische technieken in het kortsluitlaboratorium de kosten van de beproeving en maken het mogelijk om het gedrag van een elektriciteitsvoorzieningssysteem na te bootsen.

4. Happiness itself is a kind of journey, but it is not one of the destinations of this journey.

Geluk is een soort reis maar het is geen bestemming van deze reis.

5. Honesty doesn't mean blaming other people for their defects, but it does mean never flattering them for these defects.

Eerlijkheid is niet het afkeuren van de fouten van anderen, maar het nooit goedkeuren van deze fouten.

6. A smart leader makes everyone feel that he is the sole possible occupant for his position.

Een slimme leider laat iedereen voelen dat hij de enige kandidaat is voor zijn positie.

7. If a man cannot endure loneliness, he doesn't properly respect his life - partner : himself.

Als iemand eenzaamheid niet kan verdragen, heeft hij niet genoeg respect voor zijn levensgezel: zichzelf.

8. People think about revolution only when they live in poverty.

Mensen denken alleen aan revolutie wanneer ze in armoede leven.

9. The developed countries have the right to help in the development of the developing countries: But, they don't have the right to interfere in the internal affairs of these countries.

De ontwikkelde landen hebben het recht om de ontwikkelende landen te helpen bij de ontwikkeling. Ze hebben echter geen recht om zich met de interne zaken van deze landen te bemoeien.

10. The people of a country know best the problems of and in their country. Only they can solve these problems without the potential of dispute.

De inwoners kennen het best de problemen in hun eigen land. Alleen deze mensen kunnen de problemen oplossen zonder mogelijke geschillen.

11. Sometimes, politicians sacrifice the benefit of a country on their own profit.

Soms laten politici hun eigen belangen zwaarder wegen dan de landsbelangen.

12. While we are pursuing our luxurious daily life, we should think about the protection of the environment and protection of the earth's resources. Instead, with each step we take in our luxurious life, the state of the environment gets worse and still worse.

Tegelijkertijd met het najagen van ons luxe dagelijkse leven, dienen we aan het milieu te denken. In tegenstelling tot ons steeds luxer wordende leventje, gaat het met het milieu steeds slechter.

13. The importance of a conference is inversely proportional to its attendance.

Het belang van een conferentie is omgekeerd evenredig met het bezoekersaantal.

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A New Synthetic Test Circuit for Ultra-High-Voltage Circuit Breakers

A New Synthetic Test Circuit for Ultra-High-Voltage Circuit Breakers

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft
op gezag van de Rector Magnificus Prof.ir. K.F. Wakker,
in het openbaar te verdedigen ten overstaan van een commissie,
door het College van Dekanen aangewezen,
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Printed in the Netherlands

*To my wife Lin,
my parents and
my daughter Yu*

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Chapter 1

Introduction

1.1 The Power System and the Circuit Breakers

Electricity is one of the many forms of energy used in industry, homes, businesses, and transportation. The use of electricity is flexible, clean (particularly at the point of use), convenient, and in some cases, irreplaceable by any other energy source [76]. With these characteristics, the world growth rate for electricity consumption increases 7% annually or two-fold each ten years [77] as indicated in Figure 1.1.

The first large-scale use of electricity was initiated by Thomas Edison in 1882 in what became known as "Edison's Illuminating Companies". Edison's system was a direct current generation system. The system had a load of 400 lamps each consuming 83 W. The alternating current electricity generating system began its fast development with the invention of the transformer in 1886 by Karoly Zipenowski, Miska Déri and Otto Blathy, engineers from Ganz in Hungary [77]. The successful development of the three-phase generator and the transformer in 1891 stimulated the progress of the electric energy transportation technique significantly. Modern high voltage a.c. power systems are all three-phase systems.

An electric power system consists of three principle components: the generating stations, the transmission systems and the distribution systems. The transmission systems are the connecting links (systems) between all the generating stations and the distribution systems. A distribution system connects all the individual loads in a given

area via the transmission links.

Figure 1.1 World consumption of electricity, 1960-1990.

A small portion of a transmission system is shown on a one-line diagram in Figure 1.2. The circuit breakers are the necessary equipment to the transmission system.

Circuit breakers, which have the function of opening and closing a circuit, are indispensable for protecting other transmission devices in a power system. When a short-circuit fault occurs, they quickly eliminate the fault to secure system stability. They are also used for modifying the system configuration under normal conditions. The International Electrotechnical Commission (IEC) defines the circuit breaker as a mechanical switching device, capable of making, carrying and breaking currents under

normal circuit conditions and also making, carrying for a specified time and breaking currents under specified abnormal circuit conditions such as those of short-circuit. It adds, as a note, that a circuit breaker is usually intended to operate infrequently, although some types are suitable for frequent operations.

Figure 1.2 One-line diagram of transmission system

Circuit breakers must have the following basic functions [73]:

1. *When closed, they are good conductors, and they withstand normal currents as well as short-circuit currents, thermally and mechanically.*
2. *When open, they are excellent insulators, and they withstand the voltage to ground or to the other phase and the voltage between contacts.*

3. *When closed, they can interrupt a rated, or lower, interrupting current quickly without generating an abnormal voltage.*
4. *When opened, they can close a shorted circuit quickly and safely without incidental contact erosion.*

With the development of power systems, the requirements for circuit breakers have become increasingly severe. During the past 50 years *network voltages have risen from 132kV to 765kV in this period and experimental systems are now being built for 1000kV. Short-circuit ratings have risen from the order of 1×10^6 kVA on networks with low circuit severity factors and associated with ill-defined proof testing techniques, to 50×10^6 kVA on networks that involve very high circuit severity, and associated with elaborate proof testing [72].* During this period, the total break time required to interrupt short circuits has also been reduced considerably in the interests of system stability. The early circuit breaker designs required a rather variable time of the order of 10-20 cycles because of the long arc durations. The introduction of arc-controlled systems quickly reduced this to 6-9 cycles, and with improved techniques, new circuit breaker designs (in particular SF₆ circuit breakers) can operate within 2 cycles.

Figure 1.3 Trend of voltage and capacity rise of puffer-type SF₆ circuit breaker units [ref. 73]

To keep pace with the requirements of our still expanding power systems, much research and development have been done on circuit breakers. These have led to a better understanding of the basic principles of arc extinguishing and contact erosion, and a better mechanical design of circuit breakers. Figure 1.3 shows the trend in the breaking capacity of power system gas circuit breakers. There was a tenfold increase in interrupting power for SF₆ in the decade of the 1970s. In 1992 successful development of an 800kV-63kA rated Gas-insulated Switchgear was reported [8].

The first arc-extinguishing medium in the history of electric power switching was air, and experience with mineral insulating oil is almost as old as that with air. The first 40 years of experience of high power switching was based on oil, which satisfied the requirement of high power in both current- and voltage-rating in that time. An example of the early application of compressed air for blasting the arc can be found in the 1920s. In the 1940s, the investigation on the use of compressed sulphur hexafluoride (SF₆) gas as an insulating medium produced successful results. Fundamental research on SF₆ as an interrupting medium began in the 1950s, and in 1959 the first SF₆ breaker for practical use was introduced by Westinghouse in the United States.

There are four basic forms of high voltage circuit breakers:

Oil circuit breaker The oil circuit breaker employs the properties of the arc by using its energy to crack the oil molecules and generate gas, principally hydrogen, which with properly designed control systems can be used to sweep, cool and compress the arc plasma and so deionize it in a self-extinguishing process [72]. The early oil circuit breakers are tank-type or bulk oil breakers. Today oil circuit breakers are "minimum oil" type. The result of the limited "accumulated" fault current interrupting ability and the limited voltage on a single break result in that the oil circuit breakers are not suitable for use in the extra- or ultra-high-voltage system. The oil circuit breaker is used in the power system with a rated voltage below 420kV.

Air-blast circuit breaker The air-blast circuit breaker uses compressed air for "blowing out" the arc between the contacts. The air blast is confined by a nozzle which directs the flow axially through the arc space. Both single flow and double flow (blasting in opposite directions through two nozzles facing each other) are used. For voltages above 110kV, the air-blast breaker is popular because of the feasibility of having several contact gaps in series per phase.

Vacuum circuit breaker The vacuum circuit breaker is the simplest circuit breaker in the view of its mechanical construction, for it consists, in principle, of only a fixed contact and a movable contact located in a vacuum vessel. When the contacts are separated, the arc is supported by ionized metal vapor derived from the contacts instead of by ionized gas as in other forms of interrupter, and at current zero the collapse of ionization and vapor condensation is very fast, the ensuring interruption virtually independent of the rate of rise of the recovery voltage [72]. The vacuum circuit breaker is mainly applied in distribution systems with a voltage rating of 110kV and below, because of the limited voltage rating for a single break.

SF₆ circuit breaker Because SF₆ is of electronegative attraction for electrons and has a high ionization energy and as well as a high dielectric strength, it is a good alternative to the air in an air-blast circuit breaker. SF₆ has an interrupting characteristic at 5atm which is comparable to compressed air at around 50atm, so that it offers the possibility of working at much lower pressure or at much higher ratings per break [72]. SF₆ circuit breakers are available in three types in the breaker design. One is the double-pressure breaker, another one is the puffer breaker and the last one is the self-extinguishing breaker.

The SF₆ puffer circuit breakers and the SF₆ self-extinguishing circuit breakers are the most important breakers in power systems today. They are becoming the main equipment in switchgear from the distribution voltage to the transmission ultra-high-voltage (for the SF₆ puffer circuit breakers only) level. The range of applications of SF₆ switchgear is wide and is mainly determined by network demands. At the ultra-high-voltage level SF₆ puffer circuit breakers dominate the market because of their good interrupting behavior.

1.2 Testing Techniques of Circuit Breakers

According to the IEC-56 (1987), type tests of circuit breakers include:

1. *mechanical and environmental tests, including mechanical operation test at ambient air temperature, low and high temperature tests, humidity test, test to prove operation under severe ice conditions and static terminal load test;*
2. *short-circuit current making and breaking tests including terminal fault tests, short-line fault test, and also out-of-phase test;*

3. *capacitive current switching tests, including line-charging, cable-charging, single capacitor bank and back-to-back capacitor bank tests;*
4. *magnetizing and small inductive current switching tests.*

Except for the mechanical and environmental tests, all the tests in the IEC-56 type test requirements are designed to prove the interrupting ability of circuit breakers. The fault current interrupting ability is the basic function of a circuit breaker. The testing techniques discussed in this thesis are those that are used to verify the interrupting ability of circuit breakers according to the IEC-56 and IEC-427.

The development of circuit breakers depends on the progress of circuit breakers testing techniques in high power laboratories, because the physical process of arc interruption is complicated. The interrupting process in a circuit breaker involves electro-magnetic fields, thermodynamics, static and dynamic mechanics, fluid dynamics and chemical processes. As it is difficult to give a set of formulas to design and calculate the behavior of circuit breakers, testing is an indispensable procedure in their development and verification.

In the early years of the growth of electric power systems, there was a fairly complete understanding of mechanical and electromagnetic theory as applied to rotating machinery. The circuit-interruption devices, however, were developed by "cut and try" methods, and they all relied on the somewhat mysterious properties of the electric arc to switch the current. As short-circuit current increased, some of the interrupting failures were quite spectacular [72]. Study of the testing techniques started as early as the 1920s with the beginning of a worldwide study of the mysteries of high power circuit interruption.

Circuit breaker testing requires high short-circuit power in conjunction with both the current and voltage being variable over a wide range. The testing of circuit breakers can be conducted either in the actual system or in a simulated test laboratory situation.

System testing offers the advantages of: 1) no special investment necessary for the testing equipment. 2) real fault conditions for the interrupting test of the circuit breaker in service. However, the disadvantages of system testing limit the applicability in practice. System testing on the scale required would not only interfere seriously with system operation and security, but difficulty might be experienced in providing the flexibility and the variety of conditions required. Moreover, it would not readily supply

the facilities for development testing.

A high power laboratory provides the possibility to test circuit breakers conveniently under the simulated system conditions. Based on different configurations of source circuit, there are two types of high power laboratories. One is the network (grid) testing station (Figure 1.4) and the other is the specially built short-circuit generator testing station (Figure 1.5).

Figure 1.4 One-line diagram of testing station using the network as the power source

Figure 1.5 One-line diagram of testing station using the short-circuit generator as the power source

The network testing station is a station that is built in the network and uses the grid to provide short-circuit power directly. The lower investment together with easy

operation and maintenance service are the main advantages. Problems for this kind of station are that the maximum test power is limited by the system capacity and stability. The maximum test power is in general not over one fourth or one third of the total system power. The short-circuit duration and operation time are also limited by the system.

The generator testing station is a station in which short-circuit generators are used to supply the testing power. In this station, a motor is used to drive the short-circuit generator at a synchronous speed before the testing begins. During the short-circuit testing, the kinetic energy stored in the short-circuit generator transfers into the electric energy to supply the necessary testing power. The grid power required by this kind of station is low and the grid is not interfered with by the testing. Another advantage offered by this kind of station is the possibility to increase the testing capability by adding the new short-circuit generators in parallel. Most of the biggest test laboratories in the world are short-circuit generator type testing stations. The KEMA High Power Laboratory is the largest one among them (Figure 1.6). The maximum direct testing power of the KEMA high power laboratory in the test bay is 8,400MVA. The KEMA installed its first short-circuit generator in 1937. In 1973 an expansion of testing capability at KEMA High Power Laboratory was finished by installing four new short-circuit generators in use at present.

A direct test implies a test circuit with a single power source with an MVA capability that is at least equal to the full power demand of the test. In a direct test circuit, both the interrupting current and the recovery voltage are supplied by one single power source as can be seen in Figure 1.4 and in Figure 1.5. A direct test is made with a three-phase circuit.

Although direct testing may be preferred, where there is a choice, over more intricate techniques, there are limits beyond which it is not practical or economical to provide the power for direct testing. Considering present-day short-circuit ratings, these limits are quickly reached. For example, a direct three-phase test on a circuit breaker rated at 145kV and 40kA would require a three-phase source capable of supplying 10,000MVA. However, for high voltage breakers the test codes permit a single-phase test which reduces the power required to one-half, or 5,000MVA. Even so, there are few laboratories in the world that can make single-phase tests at 5,000MVA, and they soon find their capability inadequate for direct testing at slightly higher ratings.

Direct testing, where possible, has the advantage of providing a straightforward

Figure 1.6 KEMA High Power Laboratory

representation of the environment of the breaker in service, allowing little question as to the breaker being properly stressed. Disadvantages are in the size and extent of the facilities required and in the wear and tear on the facilities and test breakers, especially the possibility of severe damage to the test breaker as a result of interruption failures under full power [71].

It was in the early fifties that the interrupting capacities of circuit breakers began to surpass the power available for direct tests. A means to overcome the shortage of test power was offered for many years by unit testing. In this method, units are tested separately at a fraction of the rated voltage of the complete breaker. This technique, however, retains some problems such as the understanding of the influence of the post-arc conductivity upon the voltage distribution along the units. For economy, the interrupting capacity of a single breaker unit continues to rise, particularly with SF_6 as an arc-quenching medium. Modern SF_6 puffer circuit breakers have a high interrupting rating per break. This interrupting rating surpasses both the direct power and the classical current injection synthetic power installed in high power laboratories.

The synthetic testing method was being developed during the 1930s to overcome the problem of insufficient direct test power. The synthetic testing method applies two source circuits to supply the high current and the recovery voltage separately. After many years of investigation into the validity of this synthetic testing method, it is proven that the current injection synthetic test method has the best equivalence with the direct test method if the current injection frequency is in the range of 250Hz to 1000Hz and the current injection circuit is injected at the right instant which is specified by the standards. Therefore, the parallel current injection synthetic test circuits (Weil-Dobke circuit) are commonly used in test laboratories to verify the interrupting performance of the high voltage circuit breakers. The synthetic testing method is discussed in more detail in the next chapter.

The complication of additional equipment (extra breaker) and controls required for synthetic testing necessitates special care in circuit arrangement, switching device design, and instrumentation.

Timing control of the test sequence is very important for high power testing, especially for synthetic testing. The synthetic testing techniques made it possible to test the high power circuit breaker in a laboratory. The synthetic testing circuits use more equipment than the direct testing circuit. The additional equipment requires more accurate control, especially an accurate triggering of the spark gap of the voltage source circuit in both the current injection synthetic test circuit and the voltage injection synthetic test circuit is very important.

At any valid current injection frequency of the current injection test circuit, the spark gap must be controlled to operate about 200 μ s to 500 μ s ahead of the current zero in the main current circuit. *The security of this control is critical because operation at the wrong time may lead to failure of the auxiliary breaker and the consequent possibility of feeding higher than normal voltages back into the main power source [13].*

Results from an interruption test are essentially a set of measurements that represent the stress applied to the breaker and the reaction of the breaker to those stresses. The ability to analyze the test results effectively depends on the quality of the measurements: the accuracy of transducer outputs, the integrity of transmission, and the resolution of the recording devices.

Traditionally, one of the biggest problems has been that of operating in a severe

environment of high electromagnetic fields. Operation requires the recording of transients in an extremely short time frame when the transients themselves are the source of disturbance. Fortunately, the newer digital and fiber-optic techniques are being applied very successfully in coping with this problem. Optic isolators and transmission of signals by fiber-optic light pipes offer a great advantage in eliminating electromagnetic interference in high power testing [71].

For any interruption test, a number of records of current and voltage are needed and they must be recorded on several different time scales. Other time-varying parameters, such as the position of the breaker contact, pressure and temperature of the interrupting medium describe the environment within the interrupter. For these records, a magnetic oscillograph provides a relative slow but inclusive record over the complete time span of a test, which may last for several cycles of current. With a time resolution of about 0.2ms, the magnetic oscillograph gives an overall record of current, voltage, and the position of mechanical parts for adjusting the timing and travel of the breaker elements. The application of computer data acquisition and processing system in the high power laboratory results in that the position of the traditional magnetic oscillograph has been replaced by the digital recorders recent years.

For faster records, digital recorders are now being applied which have sampling rates of one point in 50ns or even faster under a resolution of over 10bits. Digital recording techniques not only increase the available resolution, but provide other advantages. The overriding advantage is that once the data are in digital form they can be analyzed by computer, reconstituted in any form, and stored permanently for future recall. One attractive feature for the test engineer is that the digital data can be presented on a cathode ray screen form of analog waves, which the engineer is accustomed to seeing, and portions can be expanded and analyzed. The value of any point can be read out, and any other parameter, such as rate of change of current or power in the arc, can be read out if programmed properly.

Although accuracy can be no better than that provided by the transducers themselves, recent improvements in instrumentation have made it possible to overcome many traditional problems. Optical isolators and fiber-optic transmission techniques go far in eliminating interference from the severe electromagnetic environment of power testing. High-speed cathode ray and digital recording devices offer resolution of the fastest transients, while computer processing rapidly provides all the worthwhile output possible from the raw data.

Another task for a high power laboratory is to find an optimum test method that has a better equivalence with the direct test circuit and makes less use of test equipment. The finding of an optimum test circuit is based on the understanding of the interrupting characters of the different types of circuit breakers.

The development of a power system requires a highly reliable circuit breaker operation. More and more normal and fault switching abilities are required to be verified for the circuit breakers in order to guarantee the reliability of power systems. These factors involve problems for the high power laboratory in determining which method has the best equivalence with the field testing and how to lay out the testing circuit in a laboratory situation.

Besides the terminal fault interruption, short line fault (SLF) interruption, and out-of-phase interruption, some other switching requirements for the circuit breaker have been studied in the high power laboratory over the years. These are the capacitive breaking test, the inductive breaking test, the synthetic making test, and the new test method for ultra-high-voltage circuit breakers. The testing techniques for these tests are given in reference [42] [43]. Some study still needs to be done on these subjects.

The successful development of metal-enclosed and dead-tank circuit breakers requires the test laboratory to study three-phase synthetic testing methods [41] [43].

Further development of the circuits, the instrumentation, and the testing techniques now going on in many laboratories throughout the world will continue to advance the capability for interruption testing.

1.3 Criteria for Circuit Breaker Testing

In a development testing or a verification testing program, the results should convince the test engineer that the breaker will meet all of its ratings and will perform satisfactorily in service. The criteria used by the test engineer to judge performance is specified by the IEC-56, IEC-427 and the design specifications.

The three variables, which mainly designate the electrical stress of the circuit breaker, are the interrupted current I , the highest instantaneous voltage after current interruption U , and the time variation of the recovery voltage dU/dt . In the case of a short line fault, the dU/dt immediately after current zero is particularly severe. With

terminal faults, high instantaneous voltages occur during the dielectric recovery phase, and may cause breakdown.

Because one power system differs from another, developing a circuit breaker with the ability to cover a set of ratings entails extremely large expense, and therefore standard circuit breakers covering standard ratings are selected. High power laboratories use these standard rating as the criteria to confirm the interrupting capability of the designed circuit breakers. Many years of system investigations have found the general transient recovery voltage (TRV) patterns after fault interruptions. Based on these investigations, IEC specified the parameters of the TRV for circuit breaker interruption at different voltage ratings. The standard values specified in IEC-56 cover the majority of the system requirements.

A two-parameter TRV is specified by the IEC standards for circuit breakers with a voltage rating lower than 110kV and a four-parameter TRV is specified for circuit breakers with a voltage rating of 110kV and above.

1.4 Object of Research

Since the physical process of arc interruption is complicated, testing the breaking capacity is important in the design engineering stage of new circuit breakers. Testing is the only method accepted by the IEC at present. To test circuit breakers, a test circuit which can simulate the network conditions has to be built in the high power test laboratory. This test circuit is generally accomplished by the short-circuit generators installed in test laboratories. Theoretically, it is always possible to produce higher short-circuit currents and voltages by using larger generators and placing them in parallel. This method, however, would involve very high expenses for the installation, as well as for keeping them running. Instead of building more short-circuit generators in test laboratories, new testing techniques by means of synthetic tests are accepted.

Although synthetic test circuits have been successfully used in the test laboratories to deal with the high power test of the high-voltage and extra-high-voltage circuit breakers [10] [26] [30] [32] [33] [41], there are still no suitable test circuits to verify the interrupting performance of the circuit breakers with an ultra-high-voltage rating (765kV and above) for two reasons. The principle limitation of the parallel current injection test circuit makes it impossible to perform the interrupting test for the 765kV circuit breaker with a single parallel current injection synthetic test circuit even regardless of the huge capacitive energy requirement. The proposed test

circuits are either too complicated to operate or of a doubtful validity.

It is the purpose of this thesis to report on the development of a new synthetic test circuit for the high power testing of ultra-high-voltage circuit breakers. This new synthetic test circuit should follow the general rules in the design:

- Validity of the synthetic test circuit.
The comparability test and calculation results of synthetic test circuits in respect to the validity and the practical operating experience gained during the last two decades should be borrowed and used in the development of new ultra-high-voltage synthetic test circuits in order to keep the equivalence.
- Simple operation and less use of facilities in the test laboratories.
The ultimate aim of the research work is application. In practice, in a laboratory situation, conditions that could contribute to test invalidity should be obviated. Generally, a minimal use of circuit elements and easing of the working condition of each element, in particular for the spark gap and for the auxiliary circuit breaker are the key factors in decreasing the number of invalid tests.
- A modification to the current injection circuit is the starting point to enabling test laboratories to construct a new synthetic test circuit at a reasonable investment cost.

With the above general requirements, an Enhanced Parallel Current Injection Circuit (EPIC) is proposed and studied in this research work. The EPIC circuit has the possibility of high power testing for 765kV rated circuit breakers.

The topology of a testing circuit has a significant influence on circuit stress because of the arc-circuit interaction. This influence mainly takes place during the thermal interaction interval of interrupting process. The thermal interaction interval is the most important interval for the circuit breakers, especially for SF₆ circuit breakers, to clear the fault. An arc model which resembles the behavior of the circuit breaker in practice can be used to study the validity of test circuits.

Among the arc models developed over the years, the KEMA arc model has proven its better applicability in some experimental tests in the simulation of circuit breaker interrupting behavior [56] [63]. The KEMA arc model for the SF₆ puffer circuit breaker [51] is used to study the validity of the EPIC circuit .

One of the purposes of this thesis is to make a summary of the synthetic testing circuits used in high power laboratories to test the extra- and ultra-high-voltage circuit breakers. The influence of arc-circuit interaction is studied and the equivalence conditions for synthetic testing circuits are discussed. Numerical computing methods for the calculation of power system transients are also discussed.

The calculations reported in this thesis were programmed with the Advanced Continuous Simulation Language (ACSL) [69].

1.5 Outline of this Dissertation

Chapter 1 gives a general introduction which covers the development of the power system and circuit breakers. The high power laboratory and the high power testing techniques of circuit breakers are introduced. Problems of ultra-high-voltage circuit breakers are discussed. The purpose of this study and the definition of the purpose of this thesis are given.

Chapter 2 describes the synthetic test technology used in the high power laboratories. Some possible synthetic test circuits to verify the interrupting performance of extra- and ultra-high-voltage circuit breakers are listed and generally discussed in this chapter.

Chapter 3 proposes a new synthetic test circuit (EPIC circuit) for 765kV rated circuit breakers. The circuit topology is depicted and the operating principle of the circuit is described. A general analysis of this circuit is given in this chapter.

Chapter 4 discusses the switching transients in networks and the numerical methods for the calculation of transients. The Gear's Stiff method is discussed and the ACSL language is briefly introduced in this chapter.

Chapter 5 presents several arc models to resemble the interrupting behavior of circuit breakers. The KEMA arc model is introduced in detail and the arc model parameters for the 765kV-63kA-50Hz SF₆ puffer circuit breakers are given. The validity of the EPIC circuit is studied using the KEMA arc model in this chapter.

Chapter 6 deals with the practical application of the EPIC circuit in a test laboratory. The configuration of the EPIC circuit is further studied and the parameter sensitivity in the EPIC circuit is discussed. The overvoltage and overvoltage protection

technique for the EPIC circuit are analyzed and discussed.

Chapter 7 lists the applicability of the EPIC circuit for test duty 3, SLF test duties and test duty 4 half-pole test of a 765kV-63kA-50Hz rating circuit breaker. The applicability of the EPIC circuit for circuit breakers with a rated voltage over 765kV is discussed. A better equivalence with the direct test circuit is proven by comparisons with three ultra-high-voltage synthetic test circuits.

Chapter 8 gives the conclusions of this dissertation.

Chapter 2

Synthetic Test Techniques and Test Circuits

2.1 Introduction

To catch up with the rapid increase in the interrupting capability of high voltage circuit breakers, a large amount of money has been invested in the high power laboratories. The result is the maximum of 8,400MVA direct test power available today. However, even with such a high capacity, it is still not sufficient for testing extra- and ultra-high-voltage circuit breakers.

To increase the power of a short-circuit laboratory simply by increasing generating power is neither an economical nor a very practical solution. Using the network source on such a scale would not only interfere seriously with system operation and security, but difficulty would be experienced in providing the flexibility and the variety of conditions required. Moreover, it would not readily supply the facilities for development testing.

Since the 1930s, synthetic test techniques have been applied and further developed in order to reduce the investment in direct test laboratories. One of the earliest circuits designed for a " special test " on circuit breakers was described in 1936 by Skeats [9]. This was followed by " The Weil Circuit for Testing High-Voltage Circuit Breakers with High Rupturing Capacities " by J. Biermanns [10]. There are many methods to combine the two energy sources in a synthetic test circuit, but two basic systems have proven their effectiveness and are described by the standards: current injection and voltage injection.

The principle difference between the two being that in the current injection method the circuit breaker is conducted through the zero period by the voltage source and in the voltage injection method by the current source.

Extensive studies, carried out in the early 1960s, were primarily intended to compare direct and synthetic test methods and they revealed that the synthetic test methods have a good equivalence with the direct test method [20] [21] for air-blast circuit breakers. The calculations, carried out in the 1980s, showed that this equivalence is available for the SF₆ circuit breakers too. In addition to this equivalence, synthetic testing offers more advantages:

1. **Amplification of testing power:**
Apart from being the only practical way to test the highest breaker ratings, synthetic testing methods can increase the testing capability of laboratories by a factor about 10 and at a relatively low cost.
2. **Nondestructive testing:**
Synthetic testing not only amplifies the testing capacity of a laboratory, but it also does this without the risk of destroying the breaker under test when it fails to interrupt the short-circuit current. This benefit is a result of the isolation provided by the auxiliary breaker, which prevents the power flow from the current source into the still arcing breaker. The economic and technical advantages of saving the test breaker for continued and repetitive testing are obvious. Also, the wear and tear on the power-testing facility itself is less than for full-power direct testing.
3. **Applicability for interrupting tests at the lower current levels:**
Synthetic testing makes it possible to create the correct dU/dt of the TRV when interrupting a current from 10% - 30% the rated interrupting current according to the IEC specified test conditions. The large parasitic capacitance of the short-circuit transformer in the direct test circuit usually results in a lower dU/dt for the lower duty interrupting testing.
4. **A versatile tool for development testing:**
In the development stages of circuit breaker design, synthetic testing techniques can be modified and applied to study particular aspects of circuit breaker performance.

The combination of validity and advantages makes the synthetic test methods as

approved by IEC and ANSI standards a good alternative to verify the interrupting performance of high voltage circuit breakers.

The disadvantage of the synthetic testing is its complication. The complication of additional equipment and controls required for synthetic testing necessitates special care in circuit arrangement, switching device design and instrumentation. In some cases synthetic testing has a difficulty to provide both the correct interrupting current and the correct recovery voltage simultaneously. This happens for instance when three-phase synthetic testing is performed.

In the first part of this chapter, a fundamental study and short review of the most important synthetic test techniques are presented. Subsequently the principle limitation of the parallel current injection synthetic test circuit, which is mostly used in the high power laboratories for the testing of extra-high-voltage circuit breakers, is demonstrated. In the last part of this chapter some extra- and ultra-high-voltage synthetic test circuits are discussed.

2.2 Synthetic Testing

2.2.1 Principle

By analyzing the fault interrupting process of a circuit breaker in the power system, it can be seen that two distinct phases exist during the fault current interruption process as shown in Figure 2.1. After the fault occurs, the short-circuit current flows through the breaker and establishes an arc when the contacts of the breaker begin to separate. The arcing period is characterized by a high current and a low voltage between the arcing contacts (arc voltage), and the post-arc period (after the arc extinction point) is characterized by the presence of high recovery voltage.

Synthetic testing methods are based on the fact that the circuit breaker is stressed by high current and by high voltage at different time periods. Two separate energy sources apply different stresses on the test breaker (TB) corresponding to the different time periods. The current stress occurs during the high current interval followed by the voltage stress during the high voltage period. The overlap of the current and voltage stress takes place during the "interaction interval".

Two different synthetic methods, current injection and voltage injection, are employed in the synthetic testing techniques. They differ according to which energy

source is in operation during the interaction interval. If the synthetic test uses the principle that the current from the voltage source is superimposed on the current circuit prior to the interaction interval and the auxiliary breaker (AB) interrupts the current from the current circuit prior to the interaction interval, this is referred to as the current injection method. If the synthetic test uses the principle that the voltage from the voltage circuit is applied to the TB after the interaction interval only and, an AB in combination with a parallel capacitor is used to apply the recovery voltage from the voltage circuit or from both the current circuit and the voltage circuit to the TB, this is referred to as the voltage injection method.

Figure 2.1 Short-circuit current and recovery voltage for circuit breaker clearing a system fault

In a synthetic test circuit using the current injection method, the superimposition of the currents takes place shortly before the current zero of the power-frequency short-circuit current. A current of small amplitude and high frequency, supplied from the voltage circuit, is superposed on the source current either in the TB or in the AB. The instant of injection of this current is triggered by means of a current-dependent control circuit. The injection should be such that the shape of the resulting current wave in the TB corresponds to the waveform of the specified interrupting current prior to the current zero during the interval of significant change of arc voltage. Thus, the breaker under test is automatically stressed by the voltage circuit after the interruption of the current by the AB, so there will be no delay between the current stress and the application of the voltage stress.

In a synthetic test circuit using the voltage injection method, the current circuit provides the entire short-circuit current for the TB and also, after current zero, the first part of the transient recovery voltage (TRV). A few microseconds before the first peak of the TRV of the current circuit, the voltage circuit is injected by means of a voltage-dependent control circuit in such a way that the total TRV is continuous and that there is no delay in time between the current stress and voltage stress.

2.2.2 Validity rules of synthetic testing

Since two separate energy sources are used in the synthetic test circuit instead of only one source in the direct test circuit (Figure 2.2), and a series connected auxiliary circuit breaker (AB) is present in the current circuit (Figure 2.9), some rules have to be followed to keep the equivalence of synthetic testing as specified on the IEC-56 and IEC-427. These rules can be stipulated by two criteria, one for the current, the other for the voltage.

Figure 2.2 Direct test circuit, used as reference circuit

2.2.2.1 Interrupting current (or arc channel energy input)

1. High current phase

In the ideal case, the prospective current in a test circuit has a sinusoidal shape, but during the operation of the breaker a distortion of current wave will take place as depicted in Figure 2.3. The current distortion depends on the form and magnitude of the arc voltage relative to the driving voltage of the current source. In a direct test circuit the arc voltage of the circuit breaker is small compared to the driving voltage, and the current

distortion is in general negligible. In synthetic test circuits, the ratio of the driving voltage of the current source with respect to the arc voltage is lower, and current distortion has to be taken into account. Further, the presence of the AB in a synthetic test circuit in the current circuit introduces an extra arc voltage causing current distortion. The sum of the arc voltages of the TB and the AB causes a significant current distortion. The arc voltages shorten the first current loop and extend the second current loop as can be seen in Figure 2.3 [16]. Corresponding to the current distortion, the arc energy input into the TB is affected too. According to the IEC-427 standard, the influence of arc voltage in a synthetic test circuit is limited to such a condition that the distorted current peak and the duration of the last current loop shall be not less than 90% of the values specified. This corresponds with a reduction of approximately 12% of the energy input in the last current loop.

Figure 2.3 Short-circuit current distorted by a constant arc voltage

The minimum arc energy input and the most severe distorted current condition are present when the circuit breaker interrupts a short-circuit current with an arcing time of one current loop or less. The interrupting current is described by equation 2.1 for a constant arc voltage, by equation 2.2 for a trapezoidal arc voltage and by equation 2.3 for a linear rising arc voltage. It is a quick method for test engineers to verify the validity of the synthetic test circuit by calculating the ratio between the driving voltage and the arc voltages. In Figure 2.4, a calculated relationship of relative arc energy reduction and the ratio of driving voltage to arc voltages for one-current-loop testing is presented [56]. The K in Figure 2.5 and Figure 2.6 is the ratio between the current source driving voltage U_s (with a root-mean-square value) and $U_{arc}(AB+TB)$, the sum of the voltages in the AB and the TB. For a trapezium-shaped and a linear rising arc voltage, the $U_{arc}(AB+TB)$

is the maximum voltage in the AB and the TB. For the calculation of Figure 2.4, Figure 2.5, and Figure 2.6, identical arc voltage shapes are used for both the TB and the AB. The E_s and E_d represent the total arc energy input in the TB in a synthetic test circuit and direct test circuit respectively in Figure 2.4, Figure 2.5 and Figure 2.6.

$$i_s = \frac{\sqrt{2} U_s}{\omega L_s} \sin \omega t - \frac{U_{\text{arc}}(AB+TB)}{L_s} (t - t_0) \quad (2.1)$$

$$i_s = \frac{\sqrt{2} U_s}{\omega L_s} \sin \omega t - \frac{U_{\text{arc}}(AB+TB)}{2 L_s} (t - t_0) - \frac{U_{\text{arc}}(AB+TB)}{4 L_s} (t - t_0) \quad (2.2)$$

$$i_s = \frac{\sqrt{2} U_s}{\omega L_s} \sin \omega t - \frac{U_{\text{arc}}(AB+TB)}{2 L_s} (t - t_0) \quad (2.3)$$

$U_{\text{arc}}(AB+TB)$ is the sum of the arc voltages in the AB and the TB

Figure 2.4

Arc energy reduction in the TB in a synthetic test circuit with one current loop arc duration

The reduced ratio between the driving voltage and the arc voltages in a synthetic test circuit results in a lower arc energy input for the TB as can be seen in Figure 2.4. The relative total arc energy reduction in the TB in the synthetic test circuits depends on the arc duration. Figure 2.5 shows the change of the total arc energy reduction as a function of the arc duration. From Figure 2.4 and Figure 2.5 we learn that the total arc

energy reduction in the TB in a synthetic test circuit mainly depends on the ratio of the current source driving voltage to the arc voltages in the AB and the TB. The maximum arc energy reduction takes place when the TB has a one-current-loop duration. If the driving voltage is 12 times the arc voltage of the AB and the TB, the total arc energy reduction in the TB is 12% for a constant value of the arc voltage.

Figure 2.5

The relative total arc energy reduction in the TB as a function of arc duration in the synthetic test circuit

2. Interaction interval

The shape of the current waveform around current zero is important because the physical processes in the arc column have a very short time constant, in the order of a few microseconds. It is necessary for the synthetic test circuit to keep the rate of change di_v/dt of the interrupted current just before current zero the same as the di_d/dt for the direct test circuit. Equation 2.4 is one of the conditions that must be met when designing a synthetic test circuit.

$$\left. \frac{di_v}{dt} \right|_{i_v=0} = \left. \frac{di_d}{dt} \right|_{i_d=0} \quad (2.4)$$

Equation 2.4 can simply be realized by any synthetic testing method when the arc voltages in TB and AB are neglected. But, as we have seen in Figure 2.4, the ratio

between the driving voltage and the arc voltages in the synthetic test circuit is relative low and the influence of the arc voltages has to be taken into account.

With the current injection method, the rate of change of the injection current i_v is influenced by the parameters in the voltage circuit (equation 2.5). Because the charging voltage U_0 of the main capacitor C_0 roughly equals the peak value of the rated test voltage in the direct test circuit and the arc voltage is negligible compared with this charging voltage, the di/dt around current zero is about the same as that in the direct test circuit. As a reference, the di_d/dt for the direct test circuit is given in equation 2.6.

$$\frac{di_v}{dt} = \frac{U_0 - U_{\text{arc}}(TB)}{L_1} \cos \omega_s t \quad (2.5)$$

$$\frac{di_d}{dt} = \frac{\sqrt{2} U_d \cos \omega t - U_{\text{arc}}(TB)}{L_d} \quad (2.6)$$

With the voltage injection method, the sum of the arc voltages in both the TB and the AB affects significantly the prospective current near current zero. For one-current-loop arc duration and constant arc voltages in both the TB and the AB, the rate of change of the current has a general expression of equation 2.7. It can be deduced from this equation that the di/dt of the voltage injection method at current zero is higher than the di_d/dt of the direct test method because of the lower source inductance in the voltage injection circuit as depicted in equation 2.8.

$$\frac{di_v}{dt} = \frac{\sqrt{2} U_s \cos \omega t - U_{\text{arc}}(AB+TB)}{L_s} \quad (2.7)$$

$$\text{Because } \frac{U_s}{L_s} = \frac{U_d}{L_d} \quad \text{and} \quad U_d > U_s \quad (2.8)$$

$$\text{Therefore } \left. \frac{di_s}{dt} \right|_{i_s=0} = \left| - \frac{U_s + U_{\text{arc}}(AB+TB)}{L_s} \right| > \left. \frac{di_d}{dt} \right|_{i_d=0} = \left| - \frac{U_d + U_{\text{arc}}(TB)}{L_d} \right|$$

The di/dt value itself is of greatest importance to the interruption of a circuit breaker. The higher di/dt before current zero of the voltage injection test circuit results in a higher energy input into the arc channel of the TB just before the current zero as shown in Figure 2.6 [56]. This will overstress the TB during the test.

The curves of Figure 2.4, Figure 2.5 and Figure 2.6 are computed for a breaker rating of 245kV-63kA-50Hz full pole under a series voltage injection synthetic test circuit [56]. The breaker rating has hardly any influence on the shape of the curves, so Figure 2.4, Figure 2.5 and Figure 2.6 can be used for other breaker ratings as well.

Figure 2.6

The increase of arc energy just before the first current zero in the series voltage injection synthetic test circuit

2.2.2.2 Transient recovery voltage

In a transmission system, the terminal faults of a circuit breaker have several forms. They are multiple line fed bus-fault, line and transformer fed bus-fault, and multiple line and transformer fed bus-fault. The circuit breaker is subjected to sustain a Figure 2.7 like TRV waveform after its fault interruption [3].

This TRV waveform is generally adequately represented by an envelope consisting of three line segments defined by means of four parameters (Figure 2.8). To reproduce the TRV with the four-parameter envelope is required by IEC standards for the interrupting test.

To design a test circuit with a four-parameter TRV is not very difficult, because only an inherent waveform is required by the IEC and ANSI standards. Several TRV circuits [23] [24] [25] were developed in the past decade in both the direct test circuit and the synthetic test circuit.

Figure 2.7 A typical TRV waveform applied on the circuit breaker after its bus-fault interruption

Figure 2.8 The representation of the specified TRV by a four-parameter reference line and a delay line

The criteria stipulated in the IEC-427 standard for the TRV are less strict than the criteria for the short circuit current: only the prospective waveform of the TRV is described. However, the topology of the test circuit influences the stress of test circuit on the TB [51] [62]. This is caused by the arc-circuit interaction. An identical prospective interrupting current and an identical prospective TRV waveform don't guarantee the same stress on the TB. The surge impedance of the test circuit is one of the important parameters for the determination of the stress of a test circuit. Therefore the surge impedance is an important criterium in the design and the parameter consideration of a synthetic test circuit.

The short-circuit current is supplied by the current source circuit, and let us assume that the fault starts at t_0 . At instant t_1 the spark gap is fired and the main capacitor bank C_0 discharges through the inductance L_1 resulting in a high-frequency injected current i_v , which is superimposed on the power-frequency current i_g with the same polarity. During the time span from t_1 to t_2 the generator current circuit and the current injection voltage circuit are in overlap and the current through the TB is the sum of the currents from the current circuit and the voltage circuit.

At time instant t_2 , the current i_g from the current circuit reaches zero. The AB clears the generator current and separates the high current circuit from the high voltage circuit. The TB is stressed by the voltage circuit alone after time t_2 . The voltage circuit supplies the injection current i_v . When this current reaches zero, the TB can clear and there is a TRV resulting from the voltage oscillating in the voltage circuit across the TB. The spark gap is still conducting in this time period.

In the parallel current injection synthetic test circuit, for a fixed value of L_1 , the rate of change of current is dependent only on the charging voltage of C_0 as can be seen in equation 2.5, and is independent of its capacitance. The value of L_1 in the parallel current injection circuit is generally larger than the value of direct test circuit because of the limited voltage source energy and the principle limitation of the current injection method. Calculations show that the parallel current injection circuit holds its equivalence when the L_1 is not over 1.5 times the L_d . Because, unlike the arc voltage in the direct test circuit, the arc voltage in the current injection synthetic test circuit reduces the prospective value of the di_v/dt at the current zero, the charging voltage of C_0 in the synthetic test circuit should be higher than the value of L_1 multiplying di_v/dt at the current zero after taking the arc voltage into account. The energy dissipation in the arc channel results in a decreased voltage (U_0) at the injected current zero on the C_0 in the current injection synthetic test circuit. This is demonstrated by the different decrease rates of current at current zero in equation 2.9 and equation 2.10 for the direct test circuit and the current injection circuit respectively. $U'_0 < U_0 = \sqrt{2} U_d$ (if $L_1 = L_d$).

$$\frac{di_d}{dt} \Big|_{i_d=0} = - \frac{\sqrt{2} U_d + U_{\text{arc}}(TB)}{L_d} \quad (2.9)$$

$$\frac{di_v}{dt} \Big|_{i_v=0} = - \frac{U'_0 + U_{\text{arc}}(TB)}{L_1} \quad (2.10)$$

Figure 2.11 Interrupting current nearby zero

Now let us study the period of overlap of the current source and the voltage source in the parallel current injection circuit (Figure 2.11). It is clear, as can be seen in Figure 2.10, that the injection current always distorts the power-frequency current whether the injection frequency is high or low. A low frequency injection current distorts the power-frequency interrupting the current considerably. The rate of change of the current just before zero is correct, but there is a significant increase of the arc duration, and as a result of that in the total arc energy. Although the total arc energy is increased, for a considerable period before current zero from t_1 to t_3 , the energy input to the arc channel is less than it would be in the direct test. In order to prevent undue influence on the waveform, so does the arc energy input, the lower limit of the injection circuit current is fixed by IEC-427 at 250Hz. At high frequencies, there is a short period, t_2 to t_3 , before the final current zero, where the energy being fed into the arc channel is less than for a direct test, and where the required rate of change of current exists only for a very short time before current zero. Further, the interval of arc voltage with a significant change may be larger than the short period t_2 to t_3 of higher injection frequency. Therefore, the maximum current injection frequency is fixed by IEC-427 too at 1000Hz.

Another important factor closely related to the distortion of the power-frequency current is the moment of injection. It is a normal procedure to inject the current at such an instant that the superposition time of the two currents is approximately a quarter of the period of the current injection frequency. An early injection time, Figure 2.12 a, results in additional energy being fed into the TB during the period from t_1 to t_2 and gives a very high di/dt just before t_2 . This will obviously overstress the TB. The AB is also likely to fail due to the little time, t_2 to t_3 , for its dielectric recovery. A late injection time, Figure 2.12 b, gives an appreciable period t_2 to t_3 before the final current zero. The power-frequency current is severely distorted. There is no doubt that the energy fed into the TB

during this period will be less than that in the direct test. For a certification test this is an invalid test and the test result is invalid.

Figure 2.12 Diagram illustrating current forms as a result of extremes in the injection timing

It is very important to realize that the validity of the parallel current injection test circuit is not only related to the correct current injection frequency but relies also on the moment of injection. *The initiation of the injected current shall be adjusted such that the time, during which the test circuit-breaker is fed only by the injected current, is not more than a quarter of the period of the injected current frequency with a maximum of 500μs* -- IEC-427.

2.2.4 The series current injection synthetic test method

The series current injection synthetic test method was suggested by V.V. Kaplan, *et al*, and developed in the former USSR during the 1960s. The method has a typical structure shown in Figure 2.13. The operation of the series current injection synthetic test circuit is as follows.

After injecting the voltage circuit, shortly before the current zero of the power-frequency short-circuit current, the high-frequency current i_v is superimposed (Figure 2.14), with opposing polarity, on the power-frequency short-circuit current i_g , in the AB. After the resulting current in the AB has ceased to flow, the current i , commutates into the TB. The TB is now part of a circuit formed by the series-connected current circuit and the voltage circuit. After the extinction of the current in the TB, the TRV is supplied by both the voltage circuit and the current circuit.

The advantages claimed for the series current injection method are that there is less

distortion of the current wave, especially around current zero, than in the parallel current injection method, and that the recovery voltage appearing across the TB is the sum of the voltages in the current source circuit and voltage source circuit. However, it has disadvantages because of the series-connected nature of the current and the voltage circuit. First, it is not easy to select circuit parameters such that both the current circuit and the voltage circuit give the required TRV at the same time. Second, the current source circuit must be able to withstand a high recovery voltage when the TB fails to clear. Further a high-frequency voltage oscillation, caused by the parasitic capacitance and inductance in the branches from the current source to the voltage source, can occur. Such a voltage oscillation will be superimposed on the TRV and will result in an incorrect initial TRV across the breaker contacts. It is difficult to predict and to control the voltage oscillation because of its strong dependence on the connection of the test circuit and the TB.

Figure 2.13 Series current injection synthetic test circuit

Figure 2.14 Current and recovery voltage of series current injection

2.2.5 The voltage injection synthetic test method

The difference between voltage injection test circuits and current injection synthetic test circuits is that, in the voltage injection synthetic test circuits, the AB and the TB interrupt current simultaneously, and the recovery voltage is not produced by one circuit only but both the current source circuit and the voltage source circuit contribute to it. The initial part of the TRV comes from the current source circuit, and after current zero the voltage source circuit, via the spark gap, is injected supplying the rest of TRV to the peak and thereafter.

Figure 2.15 The parallel voltage injection synthetic test circuit

Similar to the current injection methods, there are two different ways to connect the voltage circuit with the current source circuit. One is the parallel voltage injection scheme (Figure 2.15) and the other possibility is the series voltage injection scheme (Figure 2.16). Both of these two methods work according to the same principle: The current source circuit provides the total current through the TB including the post-arc current and, during that period when the arc voltage changes significantly, the arcs in the AB and the TB are connected in series. The AB and TB clear almost simultaneously at instant n_1 (Figure 2.17). There can be a few microsecond delay for TB to clear, this depends on the value of the parallel capacitor on the AB. When the TB and AB clear, the short-circuit current recovery voltage of the source is brought to the TB via the parallel capacitor. Just before this recovery voltage reaches its peak value (instant n_2), the voltage circuit is injected by triggering the spark gap. The resulting TRV is supplied by the voltage circuit only (for the parallel voltage injection method) or mainly by the voltage circuit (for the series voltage injection method). The current in the interaction interval and the TRV after current zero in the voltage injection methods are shown in

Figure 2.16 The series voltage injection synthetic test circuit

Figure 2.17 The current and recovery voltage of the voltage injection circuit

Figure 2.17.

Because the current injection from the voltage circuit is small, the amount of capacitive energy in the voltage circuit is relatively low. The voltage injection method has an advantage over the current injection method because of its economy. The disadvantage lies in the doubtful validity of the test circuit to verify the thermal behavior of circuit breakers, because in the interaction interval the parameters of the voltage circuit differ from the direct circuit values. As discussed earlier, the series-connected arc of AB and the low driving voltage of the current source put a more severe stress on the TB just before current zero. Compared with current injection method, the voltage injection methods always overstress the TB because of the higher arc energy input into the TB just before current zero (see Figure 2.6). The value of the parallel connected capacitor on

the AB affects the circuit stress significantly in the voltage injection method. If we know the interrupting performance of both the AB and the TB exactly, it is possible to arrange the voltage injection circuit parameters in such a way that the thermal stress on the TB equals the stress of a direct circuit [17] [18].

Another disadvantage of the voltage injection methods is that there is a dip in the recovery voltage when the two voltages add up, as can be seen from Figure 2.17. To obviate this voltage dip in the recovery voltage, a close matching of the initial TRV in the current source and voltage source is necessary. A lower parallel capacitance across the AB improves the shape of the voltage transition but negatively affects the thermal stress on the circuit breaker under test. More stored capacitive energy, however, can improve the voltage waveform significantly.

2.2.6 The duplicate test circuit method

The duplicate circuit or Skeats circuit [9] is the earliest synthetic test method proposed for circuit breakers. In the duplicate test circuit (Figure 2.18), the short-circuit current is supplied from a current source to the series combination of the AB and TB. The recovery voltage is applied to the TB, via a resistor, from a transformer. The primary winding of the transformer is connected to the current circuit.

Figure 2.18 Duplicate (Skeats) test circuit

Similar to the voltage injection methods, the arc voltages of the AB and the TB in the interaction interval are connected in series. The arc voltages of the AB and the TB appear on the primary side of the transformer and induce a high current i_r in the high-voltage circuit. This current adds to the current following through the TB: $i_t = i_g + i_r$. The current i_r causes the AB to clear a time Δt prior to the TB. During the time span Δt , the rate of change of the current through the TB is different from the direct test circuit

(equation 2.11). For the TB the di/dt at current zero is about $1/n$ times the prospective value.

$$\frac{di_t}{dt} = \frac{\sqrt{2} n U_s + U_{TB}}{n^2 L_s + L_T} \approx \frac{\sqrt{2} n U_s}{n^2 L_s + L_T} \approx \frac{\sqrt{2} U_s}{n L_s} \quad (2.11)$$

n - transformer ratio

U_{TB} - arc voltages in TB

The lower value of the di/dt eases the stress on the TB during the period Δt . The Δt can be reduced by increasing the value of R_r as expressed in equation 2.12. The upper limit of R_r is restricted by the low source impedance requirements during the dielectric recovery period. Normally, values of R_r in the range of some kilohms are used giving a time span $\Delta t \leq 10 \mu s$. The duplicate test circuit cannot be used for testing SF_6 circuit breakers or for tests where attention has to be paid to the thermal failure mode of a circuit breaker. The large stray capacitance of the transformer in the duplicate test circuit is another problem in producing the correct initial part of the TRV especially for the higher test voltage. The equivalence at current zero is even far less than in the case of voltage injection methods.

$$\Delta t = \frac{n (U_{AB} + U_{TB}) - U_{TB}}{\sqrt{2} n U_s} \cdot \frac{n^2 L_s + L_T}{R_r} \quad (2.12)$$

Figure 2.19 Parallel voltage injection circuit using the transformer as the voltage source

G.C. Damstra and H.W. Kempen modified the Skeats circuit by inserting a making switch (MS) and a triggered vacuum gap (TVG) between the TB and the transformer

(Figure 2.19) [34] [35]. This modification makes the circuit in fact a parallel voltage injection synthetic test circuit. The transformer is used as the voltage source to supply the recovery voltage. The di/dt at current zero of this circuit is larger than the value in the direct test circuit due to the arc-circuit interaction as discussed in 2.2.2.1.

In spite of the inherent shortcomings of the duplicate synthetic test circuit, the method using a transformer to provide the recovery voltage is still used at high power laboratories because of its a.c. recovery voltage after current interruption, simple circuit configuration and easy operation for the test duties when the thermal stress is of less importance, such as for out-of-phase fault testing. The correct recovery voltages of duplicate synthetic test circuits on three different test phases for three-phase synthetic testing are attractive in the selection of test circuit.

2.3 The Principle Limitation of the Weil Circuit

Comparability tests and calculations performed over the years have proven that the parallel current injection synthetic test method (Weil circuit [10]) gives the best equivalence with the direct test circuit. The Weil circuit is commonly used by most of the high power laboratories in the world. However, the Weil circuit has inherent limitations, which can be simply explained, in relation to the main capacitor C_0 and the inductor L_I (see Figure 2.9). During the period of current injection, the charging voltage U_0 reverses its polarity. After current interruption by the TB, the injection branch will charge the TRV adjusting branches and this results in the TRV. By the time the TRV oscillations have damped out, the recovery voltage across the TB is d.c. voltage U_{con} . The value of the d.c. voltage is governed by the conservation of the electric charge before and after the moment of injection.

$$U_{con} = \frac{C_0}{C_0 + C_1} U_0 \quad (2.13)$$

Comparing the simplest direct test circuit, Figure 2.20, and the simplest Weil equivalent, Figure 2.21, it is clear that to acquire the same di/dt it is necessary that $U_0 / L_I = \sqrt{2} U_d / L_d$ and, when $L_I = L_d$, this results in $U_0 = \sqrt{2} U_d$. Therefore, in the case of identical inductances, the charging voltage of U_0 is equal to the crest value of the power-frequency recovery voltage of the direct circuit: $U_0 = \sqrt{2} U_d = U_I$. In the direct test circuit, the TRV oscillates around the voltage U_I as can be seen in Figure 2.22. In the synthetic circuit, the TRV oscillation is around U_{con} , which is lower than U_I as can be found in equation 2.13. The $C_0 - L_I - C_I$ oscillating circuit can never reach the TRV crest

U_c . A damping resistor in the test circuits will further reduce the TRV crest value. A solution is to increase the C_0 . An infinite C_0 will result in no difference between the direct test circuit and the synthetic test circuit with respect to the recovery voltage. A large value of C_0 results in a lower impedance for the current supplied by the TRV branch. Only under such a condition is the TRV produced with respect to a nearly constant supply voltage, maintained by C_0 , as the Weil circuit requires. This means that the TRV frequency must be much higher than the current injection frequency.

Figure 2.20 TRV with a generator source

Figure 2.21 TRV with a charged capacitor source

Figure 2.22 Comparison of the TRV waveforms of figure 2.22 and figure 2.23

A general way to make the $C_0 - L_1 - C_1$ oscillating voltage peak reach the TRV crest U_c in a synthetic testing is to overcharge the capacitor bank C_0 by a factor of β (equation 2.14). Corresponding to this overcharging the inductance L_1 has to be increased β times in order to maintain a correct di/dt of the injected current. A difference in inductance value results in different circuit parameters during the current zero period. However, calculations show that β should not be over 1.5 in a synthetic testing circuit in order to keep the equivalence of Weil circuit.

$$\beta = \frac{C_0 + C_1}{C_0} \quad (2.14)$$

Assuming an unchanged inductance L_i (unchanged short-circuit current) in the different testing voltage ratings, we know, because the TRV frequency is inversely proportional to the testing voltage, both the C_0 and the C_1 in the synthetic testing are proportional to the testing voltage. This gives a lower injected current frequency at higher testing voltages. To keep the equivalence with direct testing the IEC specified the minimum current injection frequency as 250Hz and the maximum current injection frequency as 1000Hz. Under conditions of the minimum current injection frequency and the maximum overcharge factor $\beta=1.5$, the maximum testing ability with the Weil-Dobke circuit is for 525kV rated circuit breakers.

Units test doesn't contribute any solution when the synthetic testing of extra-high-voltage circuit breakers is limited by the principle limitation of the Weil circuit. Under units tests, the voltage source inductance L_i keeps unchanged as what in the full pole test because of the identical interrupting current. However, a higher C_1 and as well as a higher C_0 are required due to the low frequency recovery voltage at the units test. Higher C_1 and C_0 lower the injected current frequency only.

2.4 Extra- and Ultra-High-Voltage Synthetic Test Circuits

For the principle limitation of Weil circuit in the use of testing of ultra-high-voltage circuit breakers, several synthetic test circuits have been developed since 1970s. These circuits are discussed in this section.

2.4.1 The Cascade-Weil synthetic test circuit

Figure 2.23 shows the principle lay-out of the Cascade-Weil circuit as developed by AEG [14]. This circuit uses a three-circuit scheme. It differs in the way the circuit parameter are selected and how the TRV is produced. In the Cascade-Weil circuit the first part of the TRV is produced by a current injection circuit and the voltage injection circuit produces the remaining part of the TRV. An additional spark gap (*Gap 3* in Figure 2.23) takes care of the task of injecting different currents into the AB2 at the appropriate intervals.

Figure 2.23 Cascade-Weil synthetic test circuit

The operation of the Cascade-Weil circuit shown in Figure 2.23 is briefly described in the following steps.

1. The first voltage circuit is injected prior to the power-frequency current zero to complete the current injection. The injected current is superimposed on the current through both the *TB* and *AB2*.
2. *AB1* clears at the instant of power-frequency current zero. *Gap 2* is fired between the power-frequency current zero and the current zero of the injected current to complete the second series current injection.
3. The second current injection is cleared by the *TB* and the *TB* is stressed by recovery voltage from the first voltage source. The parameters of the first voltage source branch and second voltage source branch are selected such that the recovery voltage from the first voltage source branch stress the *TB* until t_f of the IEC four-parameter TRV envelope. The *AB2* remains closed until t_f . After the *AB2* clears the two voltage sources are connected in series.
4. *Gap 3* is triggered to short circuit the branch $C_h - R_h$ (Figure 2.23). The voltage oscillation of the second voltage source branch adds up over the contacts of the *TB* and the result is a complete four-parameter TRV.

J. Tomiyama [38] simplified the Cascade-Weil circuit by using transformer instead of the precharged capacitor bank. A detail study of this simplified circuit (Figure 2.24) was given by G. Witte [36]. The number of spark gaps is reduced to two in this improved Cascade-Weil circuit. The operating reliability is improved by this simplification. The operation of the improved Cascade-Weil circuit is similar to the Cascade-Weil circuit and is not described here.

Figure 2.24 Improved Cascade-Weil synthetic test circuit

2.4.2 The balanced synthetic test circuit

The balanced synthetic test circuit for the testing of extra-high-voltage circuit breakers was introduced by A.D.Stokes, *et al* [32]. The philosophy behind the balanced circuit arrangement lies in using two voltage sources to create the TRV. The arrangement of the TRV and the injection circuits is similar to a Weil circuit. The two voltage circuits have a symmetrical lay-out as shown in Figure 2.25.

Figure 2.25 Balanced synthetic test circuit

C_0 is precharged and by triggering Gap 1, a current is injected in the branch C_0 - Gap 1 - L_1 - TB . The value of C_0 is only determined by the injection frequency and is not connected with the TRV frequency. At the current zero of injected current, the second gap (Gap 2) is fired and a second voltage source is connected which discharges into the first voltage source circuit, since the complete circuit is electrically balanced

A four-parameter TRV is created in two steps. The first part of the TRV is connected to the current I_2 which flows through the series impedance branch $R_{22} - C_{22} - C_{21}$. When the recovery voltage rises to the first peak of the TRV I_2 is interrupted by AB2. The voltage divided by C_1 and C_2 is supplied to C_{21} through the branch $L_h - R_h$. The second peak of the TRV is formed by the total voltage across C_{22} and C_{21} .

An economical four-parameter TRV circuit lay-out for extra- and ultra-high-voltage circuit breakers achieved by this arrangement. Test laboratories do not have to make big investments to build this circuit for testing of the extra- and ultra-high-voltage rated circuit breakers.

A fundamental problem with this circuit, however, is the equivalence with the direct test circuit and the permissible tolerance of the circuit parameters. Because the maximum attainable surge impedance in this circuit is about 28Ω , a value lower than the prospective value, the equivalence of this circuit at current zero is not good [51] [52]. The small value of the capacitors C_{22} and C_{21} makes the circuit sensitive to the influence of the parasitic capacitance of the AB2, the TB and the other circuit elements. These parasitic capacitances affect the TRV waveform significantly.

2.4.4 Other three-circuit arrangement synthetic test circuits

To be able to test circuit breakers for the higher voltage and current levels, the so called three-circuit arrangement synthetic test circuits were proposed in the early 1980s [33] [41]. The idea behind three-circuit test circuits is to combine the current injection circuit and the voltage injection in one scheme. The current injection method covers the interaction interval and the voltage injection method takes care of the recovery voltage and realizes TRV specified by the IEC. There are, basically, two possible schemes depending on the place of the second auxiliary circuit breaker AB2. The operating procedure for these two test schemes is the same. The high current is provided by the current source, and just before the current zero of this main current the current injection circuit is triggered. Both the AB2 and the TB clear the injected current simultaneously at the first current zero of this injected current. The recovery voltage produced by this current injection circuit is coupled to the TB through the capacitor connected in parallel with the AB2. When this recovery voltage is close to its peak value, the voltage injection circuit is triggered. The recovery voltage across the TB is the sum of the recovery voltages of the current injection circuit and the voltage injection circuit.

In the three-circuit scheme of Figure 2.27, proposed by Siemens [33], the AB2

is in the main current loop. The driving voltage of the current source must be higher than in the parallel current injection circuit because of the extra arc voltage of AB2. This is often a limitation for existing test plants. When the driving voltage is too low, the result is a distorted high current through the TB, and also a distorted energy input into the TB arc during the high current phase. Because AB1 and AB2 have the same interrupting ability requirement, the two identical arcs being in series connection around the injection current zero over stresses the TB.

Figure 2.27 Example of a three-circuit scheme with AB2 in the main current loop

Figure 2.28 UHV synthetic test circuit studied by KEMA

Another three-circuit scheme similar to the principle of the scheme of Figure 2.27 was studied by KEMA at about the same time [41]. The circuit scheme is depicted in Figure 2.28. A transformer is used as the second voltage source instead of a charged capacitor. The advantages of this substitution in combination with the circuit arrangement give the circuit the possibility to perform making test and to supply an a.c. recovery voltage after the TB clears. Another advantage of this circuit is the possibility to supply a 1 per unit recovery voltage across the TB after the first half power frequency recovery voltage cycle. This because the parallel current injection circuit supplies 0.3 per unit of the TRV for half a cycle and then is damped out and, the transformer voltage injection circuit supplies a 1 per unit of the TRV. Scale tests of Figure 2.28 circuit were performed at 10% of the rated voltage and current of a circuit breaker with a rating of 1050kV-63kA-50Hz. The oscillogram of the scale test is given in Figure 2.29. The same problems as what discussed for the circuit of Figure 2.27 exist for the Figure 2.28 circuit.

In the three-circuit scheme shown in Figure 2.30, the AB2 is placed in the current injection loop. This requires a very fast dielectric recovery of the AB2 and such requirement makes AB2 expensive in design and difficult to control during an actual test. Like other three-circuit arrangement synthetic test circuits discussed above, the equivalence of this circuit is questionable because of the introduction of an extra arc of the AB2 in the circuit during the interaction interval.

Figure 2.29 Oscillogram of the 1:10 scale test with the test circuit of Fig. 2.28

Figure 2.30 Example of a three-circuit scheme with AB2 not in the main current loop

2.5 Conclusions

To verify the interrupting capability of the high-voltage circuit breakers, the direct test power is usually not sufficient for even units test. The synthetic test method is the only economical and practical way to cope with the increase in the circuit breaker development. The synthetic test method amplifies the testing power in high power laboratories, performs nondestructive testing for circuit breakers and simulates the system fault by interrupting conditions in a correct way.

Over the last 30 years, much attention has been paid to the equivalence studies on synthetic test methods and how to carry out the actual tests on meeting the requirements for high-voltage circuit breakers. It has been established that the parallel current injection method has an equivalence with direct testing. The validity of the parallel current injection method has been proven by many tests on air-blast breakers performed in high power laboratories and calculations on SF_6 circuit breakers all over the world. However, the voltage injection synthetic test method leaves some doubts as to the validity in the interaction interval. Studies have shown that the series voltage injection synthetic test circuits can also be applied, provided that the arc behavior in both the AB and TB are already known and that the circuit parameters are chosen correctly.

When using synthetic test circuits, the following aspects have to be taken into account.

1. Make an estimation of the arc voltage waveform and value and select a driving voltage in order to keep the right arc energy input to the TB during the last loop

of the high current phase.

2. Select the circuit parameter values close to the values of the circuit elements in a direct test circuit. The inductance, the surge impedance and the time delay capacitance are important.
3. Any switching operation in the period with a significant change of arc voltage in the TB must be avoided.

The introductory words in the IEC-427 (1989-10) can be cited here to serve as the conclusion to this chapter about the synthetic test techniques " *During the past few decades experience has been gained with synthetic testing techniques and methods. It has been proven that synthetic testing is an economical and technically correct way to test high-voltage a.c. circuit breakers according to the requirements of IEC Publication 56. This is why it was decided to include synthetic testing methods,, as equivalent to the direct test methods.* "

Most of the extra- or ultra-high-voltage synthetic test circuits developed in various laboratories apply the current injection method during the interaction interval. This method, however, has a principle limitation on its application when only one voltage source is used to produce both the injection current and the TRV. The highest test voltage of the Weil circuit is for the 525kV rated circuit breakers under a strict IEC standard specification. Units test doesn't help to cope with the principle limitation of Weil circuit but do lower further the test voltage rating of the circuit breakers. For circuit breakers with a rated voltage of 765kV and higher, no suitable test circuit is in operation yet. It would be possible to extend the three-circuit arrangement circuits and the Hitachi four-parameter circuit extra-high-voltage test circuits to ultra-high-voltage test circuits. These test circuits either give an over-stress on the TB or are too weak in the interaction period.

Chapter 3

A New Ultra-High-Voltage Synthetic Test Circuit

3.1 Introduction

As discussed in chapter 2, the synthetic test method is a practical and economical way to test circuit breakers with a high breaking ability. Although the parallel current injection circuit has a good equivalence with the direct test circuit, the principle limitation of this circuit is that this test scheme can only be used for circuit breakers with a rated voltage of 525kV and lower. Previously developed synthetic test schemes dealing with this problem either have a bad equivalence or are too complicated to work in practice. The on-going development of circuit breakers for the higher voltage ratings requires that adequate test circuits be developed. From the view of equivalence, it is more or less necessary that the new synthetic circuit makes use of the current injection method during the current-zero interaction interval since many comparison tests and calculations have already proven that there is no significant difference between the parallel current injection method and the direct test method. From the economical point of view, it will be an alternative when the new synthetic test circuit is a modification of the parallel current injection synthetic test circuit which already exists in high-power laboratories.

In the IEC-56, a four-parameter TRV for circuit breakers with a rated voltage 110kV and above is specified as shown in Figure 2.8. Two different slopes can be distinguished. The first slope ($0, t_1$) has a rate of rise of 2kV/ μ s. The second slope (t_1, t_2) has a rate of rise of 1kV/ μ s. To realize a four-parameter TRV, several TRV circuits

are employed [23] [24] [25]. The principle of these TRV circuits is that they produce a two-frequency voltage oscillation after current interruption. In a synthetic test method, very large voltage source energy is needed in order to maintain the d.c. or a.c. recovery voltage.

If the two frequencies are not produced at the same time, a smaller energy source can be used. For this reason, it makes sense to use different circuit structures to realize the two voltage oscillations separately. This philosophy is used in designing the new synthetic test circuit.

To fit the envelopes in the intervals from $(0, t_1)$ and (t_1, t_2) with a basic R - L - C circuit is not difficult. The problem, however, is how to add the two waveforms and create the four-parameter envelope. A new synthetic test circuit which realizes the four-parameter envelop in two stages is described and analyzed in this chapter. The first stage is a current injection scheme producing a two-parameter TRV after current interruption. The second stage is a voltage injection to complete the four-parameter TRV.

One of the severest duties for power circuit breakers is to interrupt the maximum rated short-circuit current. This test is described by test duty 4 of IEC-56. This chapter analyzes the new synthetic test circuit and the circuit parameter for a 765kV-63kA-50Hz rating breaker test duty 4 of IEC-56. The applicability and the circuit parameters of the new synthetic test circuit for test duty 3, SLF test duty and for test duty 4 on a half-pole of a 765kV-63kA-50Hz rating breaker will be studied in chapter 6.

3.2 The New Ultra-High-Voltage Synthetic Test Circuit

3.2.1 Circuit arrangement and its characteristics

The new synthetic test circuit is based on the three-circuit arrangement and has the topology depicted in Figure 3.1. The circuit can be divided into three subschemes. The first part of the new synthetic test circuit consists of a short-circuit generator U_s (the necessary step-up transformer is not shown in Figure 3.1), the current limiting inductor L_s , the TRV elements $R_g - C_g$ and the current source auxiliary circuit breaker (AB1). This part of the test circuit supplies the desired short-circuit current. The second part of the new synthetic test circuit is a parallel current injection circuit ($C_0 - L_l$ and corresponding TRV branches) to supply the injected current and to create the first part of the TRV. The third part is a voltage injection circuit ($C_h - L_h - C_{2l}$) which produces an oscillating voltage across the C_{2l} . The sum of the oscillation voltage and the remaining

voltage on capacitor C_{22} will form the second part of the TRV. The prospective TRV waveform of the new circuit scheme is shown in Figure 3.2. Since the new synthetic test circuit is in fact an Enhanced Parallel Current Injection Circuit (EPIC), we name in short the new synthetic test circuit the EPIC circuit.

Figure 3.1 The EPIC synthetic test circuit

Figure 3.2 The prospective TRV for a 765kV-63kA-50Hz breaker rating test duty 4

Compared with the conventional parallel current injection synthetic test circuit, the EPIC circuit has the following differences with respect to the configuration and the

operation:

1. The triggering gap is replaced by an auxiliary breaker (AB2). This auxiliary breaker services as a triggering gap to conduct the injection current and as a switch to separate the current injection circuit after the injection of the second voltage source circuit. The requirements of AB2 and its working condition will be explained later.
2. The value of inductor L_i in the injection circuit is equal (or slightly less in order to decrease the total capacitive energy necessary of the EPIC circuit) to the short-circuit inductor (L_d) of the direct test circuit.
3. The main capacitor bank C_o and the TRV adjusting capacitor C_i are precharged with the same voltage level and have the same polarity. The injected current is not a half sine wave but a combination of sine wave and an exponential waveform. This means that extra energy is put into the arc because of the exponential current wave. Another precharged capacitor bank C_h is required to form the second part of the TRV.
4. *Gap 1* is controlled by current I_{11} . The working condition of *Gap 1* is relatively easy.
5. The TRV damping resistor R_i must be able to dissipate the capacitive energy stored on the precharged C_i .

The EPIC circuit can be considered as one kind of three-circuit arrangement, however, some futures of this circuit make it significantly differ from these three-circuit arrangement circuits as described in section 2.4.

1. No additional arc channel.
All the three-circuit schemes which have been discussed before (see section 2.4) involve three arc channels (TB, AB and Gap) during the thermal interaction interval. The EPIC circuit, like the conventional parallel current injection circuit, has only two arc channels in this interval.
2. The current injection circuit provides the first part of the TRV until t_f . There is no voltage drop in the initial part of the TRV as there is in the voltage injection circuits (Figure 2.15 and Figure 2.16) and three-circuit schemes (Figure 2.27 and Figure 2.30).

3. The high current doesn't pass through the auxiliary circuit breaker (AB2) like in the Cascade-Weil circuit, Siemens circuit and KEMA circuit (Figure 2.23, Figure 2.24, Figure 2.27 and Figure 2.28).
4. A closer representation of the parameters of the direct test circuit is achieved.
Unlike the Hitachi circuit (Figure 2.26) the actual TRV is not significantly disturbed by the arc-circuit interaction and the parasitic parameters of the practical circuit set up.

3.2.2 Explanation of the breaking process

1. Before the test AB1 is closed and the main current I_{a1} flows as can be seen in Figure 3.3. The current I_{a1} flows via the current-limiting inductor L_s , AB1 and TB. The AB2 is still open.
2. Just before the main current reaches its natural current zero, AB2 is triggered (instant m_1) and AB2 forms a path through the TB for the injected current which is supplied by capacitor banks C_0 and C_1 . The resulting current I_i through the TB is the sum of the main source current I_{a1} and the injected current I_{a2} .

Figure 3.3 Explanation of the breaking process

3. At the natural current zero (instant m_2) of the main current I_{a1} , the main current is interrupted by AB1. The injected current I_{a2} continues to flow through AB2 and the TB. The current flowing through the TB is supplied by the voltage source circuit only.
4. At the current zero of I_1 (instant m_3) the TB clears and AB2 is still conducting. The main capacitor bank C_0 charges the TRV branches $C_1 - R_1$ and $C_{22} - R_{22} - C_{21}$ via L_1 and AB2 and generates the first part of the TRV in the time interval between m_3 and m_4 .
5. When the current I_{11} is close to its peak (instant m_4) *Gap 1* is triggered to create an oscillating current I_2 in the branch $C_h - \text{Gap 1} - L_h - C_{21}$.
6. When the current I_{a2} passes through zero AB2 clears. The sum of the remaining voltage on capacitor C_{22} and the oscillating voltage on C_{21} form the second part of the prospective TRV (time after m_5).

A detail voltage and current relationship on the main elements of the EPIC circuit is depicted in Figure 3.4 to give a better understanding of the working principle of the EPIC circuit.

3.2.3 The circuit parameters

The elements used in the EPIC circuit are lumped capacitances, inductances, resistances and the switching elements: spark *Gap 1* and auxiliary circuit breakers. Each of the elements influences the waveform of TRV. An optimal combination of capacitance-inductance-resistance-values can minimize the necessary capacitive energy and can ease the working condition of AB2.

In the circuit set-up the network damping elements are divided into two parallel branches in order to create voltage oscillations of two different frequencies. Branch $R_1 - C_1$ contributes to the first part of the TRV only and branch $R_{22} - C_{22} - C_{21}$ plays a role during the entire recovery voltage period. An auxiliary circuit breaker (AB2) separates these two branches. The impedance ratio of the two branches determines the di/dt and the dU/dt for the AB2. The lower the impedance of the branch $C_1 - R_1$ is, the lower are the di/dt and dU/dt for the AB2 and the less capacitive energy is necessary for the voltage circuit. However, a higher impedance value of branch $R_{22} - C_{22} - C_{21}$ results in a low capacitance value of this branch resulting in a larger decrease of the power frequency

Figure 3.4 Voltage and current traces of the main elements of the EPIC circuit

Table 3.1 Parameters for a 765kV-50Hz voltage rating

Parameter	63kA Circuit	50kA Circuit	40kA Circuit
C_0 (μF)	5.50	5.50	5.50
L_1 (mH)	28.2	32.9	39.9
C_h (μF)	3.50	3.50	3.50
L_h (mH)	65.0	80.0	92.0
C_1 (μF)	1.96	1.43	1.17
R_1 (Ω)	96.0	120.0	150.0
C_{22} (μF)	.87	.63	.52
R_{22} (Ω)	288.0	360.0	450.0
C_{21} (μF)	2.61	1.90	1.56
C_c (nF)	21.0	15.0	15.0

Table 3.2 Charging voltage and injection parameters for a 765kV-50Hz voltage rating

Parameter	63kA Circuit	50kA Circuit	40kA Circuit
U_0 (kV)	790.0	730.0	710.0
U_h (kV)	618.0	571.0	541.0
f_{inj} (Hz)	404	374	339
Z_{inj} (Ω)	71.6	77.3	85.2
I_{inj} (kA)	11.0 + .32*	9.5 + .12*	8.3 + .07*
dI / dt (A / μs)	28.0	22.2	17.8
R_{Surge} (Ω)	72.0	90.0	112.5

* Value of the discharging current of C_1 when the injected current reaches its peak instant

recovery voltage and a greater value of L_h is necessary for the frequency of the slow oscillating voltage of the second part of the TRV waveform. Based on calculations, in this study the impedance ratio is taken 1 : 3. The second part of the TRV waveform is

formed by the remaining voltage on C_{22} and a voltage oscillation in the loop $C_{21} - L_h - \text{Gap } 1 - C_h$. Similarly, there is another ratio selection problem. A higher ratio of C_{21} and C_{22} requires a higher value of inductance L_h in order to produce a low-frequency voltage oscillation. A lower ratio of C_{21} and C_{22} results in a higher working current for the spark Gap 1. C_{21} and C_{22} have a ratio of 1 : 3 as well.

The parameter combinations for the EPIC circuit suitable for a full pole test on a breaker with a voltage rating of 765kV at 50Hz and a current rating of 63kA, 50kA and 40kA respectively are given in Table 3.1. The charging voltages and injection parameters of the test circuit are calculated in Table 3.2.

3.3 General Analysis of the EPIC Circuit

3.3.1 Required capacitive energy

The capacitive energy necessary in a synthetic test circuit is of great importance. Less required capacitive energy means less capital investment for the construction of the actual synthetic test facility. Table 3.3 shows the minimum required capacitive energy for the EPIC circuit. When calculating Table 3.3, the maximum permissible overvoltage for each capacitor bank (as a result of maloperation as analyzed in chapter 6.3) is taken into account.

Table 3.3 The minimum energy requirements for each capacitor bank calculated for different current ratings

Element	63 kA Circuit	50 kA Circuit	40 kA Circuit
C_0 (MJ)	1.72	1.47	1.39
C_h (MJ)	0.72	0.61	0.54
C_l (MJ)	0.61	0.43	0.35
C_{21} (MJ)	0.67	0.51	0.43
C_{22} (MJ)	0.13	0.11	0.09
Total (MJ)	3.85	3.13	2.80

3.3.2 Working condition for auxiliary breaker 2

The task of AB2 is of vital importance in the EPIC circuit because the realization of the four-parameter TRV is connected with the correct operation of AB2. Special attention has to be paid to the design and operation because of the special operating requirements. The current and recovery voltage waveform for the AB2 are plotted in Figure 3.5. By analyzing Figure 3.5, we can formulate some general requirements for the AB2. These requirements are: 1. AB2 has to act as a spark gap during the classical current injection circuit period and must withstand the precharged voltage. 2. AB2 must not interrupt the injected current but shall interrupt the oscillating current at a later stage. 3. AB2 must also withstand the recovery voltage clearing.

Figure 3.5 The current through and the recovery voltage over the AB2 in the 765kV-63kA-50Hz test circuit

Fortunately, the values for the current and the recovery voltage stressing the AB2 are relative low as can be seen in Table 3.4. Based on the injection parameters and the interrupting requirements for AB2, it can be concluded that a triggering gap with a puffer cooling of SF_6 gas [31] can act as AB2 in the EPIC circuit. The operation principle of such a combination of a triggering gap and a circuit breaker is shown in Figure 3.6. A certain gap distance l is necessary in order to withstand the voltage before triggering and to achieve a higher dielectric recovery after current zero. To operate with a fixed contacts distance a triggering electrode is implemented inside the AB2 to create the triggering spark at the instant of triggering. A moveable piston inside the AB2 is necessary in order to extinguish the arc at the second current zero. The successful design and the operation experience gained with the plasma injection type trigger gap in reference [30] [31]

makes the construction of the AB2 possible. Experiments of similar plasma injection type trigger gap have been reported on the testing of circuit breaker with a rating of 362kV-40kA [31]. A double-pressure type SF₆ circuit breaker design can also be used to build this auxiliary breaker. An accuracy control of the gas valve is necessary in this design.

Table 3.4 Calculated parameter values for the auxiliary breaker AB2 of the 765kV-50Hz test circuit for different current ratings

Parameter	63kA Circuit	50kA Circuit	40kA Circuit
$I_{\max}$ (kA)	11.03 + .32	9.45 + .12	8.33 + .07
I_{last}^* (kA)	1.09	0.84	0.67
m3 - m1 (ms)	1.237	1.335	1.473
m5 - m3 (ms)	0.626	0.605	0.617
Arc Time (ms)	1.86	1.94	2.09
dI / dt^{**} (A / μ s)	4.4	3.4	2.6
U_{peak} (kV)	734	715	693
dU / dt^{***} (kV / μ s)	1.27	1.15	1.16

- * Peak current of the last injected current loop through AB2
- ** From 25 μ s to current zero instant
- *** From current zero to 50 μ s

Figure 3.6 Combination of a trigger gap and a circuit breaker

3.3.3 Working condition for spark Gap 1

Although spark Gap 1 has a relative easy working condition in the EPIC circuit, the gap must withstand the highest charging voltage of the capacitor bank in the second voltage circuit, the gap must be triggerable over a voltage range with small tolerances for the delay time, and the wearing of the electrode after a discharge should be small.

In the EPIC circuit the triggering of Gap 1 is initiated by the change of I_{11} (dI_{11}/dt) in TRV branch $C_I - R_I$. When the I_{11} is close to its peak value (when the dI_{11}/dt is close to zero), the controller gives a trigger pulse to fire the gap. This process can be accomplished in the following way by experienced measuring in the high power laboratory.

1. The branch current I_{11} is measured with a Rogowski coil which results in a differentiated I_{11} output (dI_{11}/dt) to the controller as shown in Figure 3.6.
2. A reference voltage level is pre-set to achieve the desired trigger time.
3. The timer that controls the test sequence blocks the control signal dI_{11}/dt until unlock time in Figure 3.7.

Figure 3.7 Control signal for the triggering of Gap 1

4. The now unlocked control signal is continuously compared with the reference voltage level. As soon as the difference between the control signal and the reference voltage crosses the zero line, as shown in Figure 3.7, a trigger pulse is sent by the controller to Gap 1.

The exact trigger signal of *Gap 1* does not ensure its correct operation. The sustained voltage across *Gap 1* and the current through the gap after triggering are two important parameters for the correct operation of *Gap 1*. As depicted in Figure 3.8, the voltage between *Gap 1* in the EPIC circuit changes slowly, at the predicted triggering instant (dotted line in Figure 3.7 with respected a 95% the peak control current I_{11}) the voltage is 92% the initial sustained voltage. The shaded part in Figure 3.8 is the change of ratio vs the possible deviation of the triggering signal as studied in 5.2.3. Values for the operating current are calculated in Table 3.5. Differently rated breaking currents hardly influence this ratio but result in different operating currents.

Figure 3.8 Voltage change between the gap electrodes as a function of the instant of triggering

Table 3.5 Peak current through *Gap 1* (kA)

	63kA circuit	50kA circuit	40kA circuit
Normal	2.28	1.68	1.36
Maximum	3.06	2.34	1.94

3.3.4 The influence of the precharged capacitor C_1

The same voltage, U_0 , is precharged on the TRV adjusting capacitor C_1 , which leads the current injection to differ from the conventional current injection in the injecting current waveform as shown in Figure 3.9. This arrangement in the EPIC circuit gives following advantages:

- 1) an improvement to the current waveform just before current zero, this is very helpful when the injection frequency is low. The low injection frequency results in a significant current distortion.
- 2) easing the triggering of AB2 because full precharged voltage is applied across the contacts of the AB2 at the triggering instant.

Figure 3.9 The injected current of the new circuit

The superposition on the injecting current of the damped exponential current from C_1 gives an extra energy input into the arc channel of TB during the injection period which is greater than the input of the classical parallel current injection test circuit. The extra energy input to the arc channel caused by the discharge of C_1 can be calculated with equation 3.1.

$$W_{C_1} = \int_0^{t_0} R_{\text{arc}} I_1^2 dt \approx \int_0^{t_0} R_{\text{arc}} \frac{U_0^2}{(R_1 + R_{\text{arc}})^2} e^{-\frac{2t}{\tau}} dt \approx \frac{R_{\text{arc}} C_1 U_0^2}{2 R_1} \quad (3.1)$$

The energy input into the arc channel of the TB in a classical parallel current injection test circuit (for the same injecting frequency) is:

$$\begin{aligned}
 W_{C_0} &= \int_0^{t_0} R_{\text{arc}} I_{\text{arc}}^2 dt = \int_0^{\pi} R_{\text{arc}} \frac{I_m^2}{\omega} \sin^2(\omega t) d(\omega t) \\
 &= \frac{\pi R_{\text{arc}} C_0 U_0^2}{2} \sqrt{\frac{C_0}{L_1}}
 \end{aligned} \quad (3.2)$$

The percentage of higher energy input into the arc channel of the TB is the ratio between equation 3.1 and equation 3.2:

$$\beta = \frac{W_{C_1}}{W_{C_0}} 100 \% = \frac{C_1}{\pi R_1 C_0} \sqrt{\frac{L_1}{C_0}} 100 \% \quad (3.3)$$

Table 3.6 gives the calculated values for the different breaker current ratings.

Similar to the direct circuit and the classical parallel current injection circuit, resistor R_l has a limited energy dissipation during the test. In the EPIC circuit the energy input into R_l is caused not only by the discharge of C_0 via the $C_l - R_l$ branch during the TRV interval, but also by the discharge of C_l to the TB during the current injection interval. Consequently, the energy requirement for resistor R_l is higher than in the classical parallel current injection circuit as can be learned from Table 3.7.

Table 3.6 Related extra arc energy input on the TB during the current injection period in the new circuit

Circuit	63kA	50kA	40kA
β	8.45 %	5.31 %	3.85 %

Table 3.7 Total energy dissipation in R_l as a result of the precharged capacitor banks C_0 and C_l

Parameter	63kA Circuit	50kA Circuit	40kA Circuit
From C_l (MJ)	0.61	0.38	0.30
From C_0 (MJ)	0.45	0.30	0.25
Total (MJ)	1.06	0.68	0.55

3.4 Conclusion

The EPIC circuit combines the current injection scheme and voltage injection scheme in one circuit. This is necessary in order to fulfill the test conditions before, during and after current zero. The EPIC circuit is based on the accepted Weil circuit in the interaction interval around current zero but with circuit parameters closer to the ones of the direct test circuit in this interval. The inductance of the current injection part of the EPIC circuit can be selected equal to the inductance value in the direct test circuit. No extra arc is introduced in the current injection part of the EPIC circuit and, therefore, the basic characteristic of Weil circuit is inherited by the EPIC circuit. The injection current and the first part of the TRV is provided by the Weil circuit. The injected current gains improvement from the discharge current of C , which partly compensates for the current deformation and lower energy input because of the low current injection frequency during extra- and ultra-high-voltage testing. A voltage injection circuit is used to complete the four-parameter TRV across the breaker contacts. This three-circuit arrangement to produce the IEC-specified interrupting current and TRV has a low capacitive energy requirement. The total capacitive energy necessary for the EPIC circuit is less than 4.0MJ for a 765kV-63kA-50Hz, test duty 4, full pole testing. The spark gap in the EPIC circuit faces a low working voltage and current.

A specially designed auxiliary circuit breaker (AB2) is necessary in the EPIC circuit. The circuit requirements are such that the AB2 does not have to clear when the TB clears but AB2 clears at the next current zero at a much lower di/dt value.

Chapter 4

Numerical Methods and Network Computations

4.1 Transient Phenomena in Electrical Networks

An electrical transient is the outward manifestation of a sudden change in circuit conditions, as when a switch opens or closes or a fault occurs in a system. The transient period is usually very short. The fraction of their operating time that most circuits spend in the transient condition is insignificant compared with the time spent in the steady state [74]. The simple circuit shown in Figure 4.1 can be used to demonstrate the transient phenomena of an electrical network when a fault is switched off. In Figure 4.1 the voltage U is the system voltage, the L is the inductance limiting the current to the point of fault and the C is the total parasitic capacitance to ground of bushings, current transformers and the capacitance between circuit contacts.

Assume first that the circuit breaker is an ideal switch and that the fault current is assumed to be symmetrical. This means that at the instant of current zero the source voltage is at its maximum value. The voltage across the circuit breaker and the capacitor C is zero. After the circuit breaker clears the fault current at power frequency current zero, a recovery voltage of the system appears across the circuit breaker terminals. This voltage U_c can be calculated with equation 4.1.

Figure 4.1 Equivalent circuit for a circuit breaker clearing a fault

$$L \frac{dI}{dt} + U_c = U_m \cos \omega t \quad (4.1)$$

When $I = C dU_c/dt$ is substituted in equation 4.1:

$$\frac{d^2 U_c}{dt^2} + \frac{U_c}{LC} = \frac{U_m}{LC} \cos \omega t \quad (4.2)$$

The solution of equation 4.2 is

$$U_c(t) = \frac{\omega_0^2}{\omega_0^2 - \omega^2} U_m (\cos \omega t - \cos \omega_0 t) \quad (4.3)$$

$$\omega_0 = 2 \pi f_0 = \sqrt{\frac{1}{LC}}$$

f_0 in equation 4.3 is called the natural frequency of the circuit. The angular frequency ω_0 of the transient recovery voltage appearing across the circuit breaker contacts is relatively high. Depending on the voltage-rating of the system, this frequency varies from about 10 times the power frequency to 1000 times the power frequency. Reactor switching is a good example of where high natural frequency transients occur as can be learned from reference [74] p.51: Consider such a choke with an inductance of 1mH and an effective capacitance of 400pF, its natural frequency will be

$$f_0 = \frac{1}{2 \pi (10^{-3} * 4 * 10^{-10})^{1/2}} = \frac{10^6}{3.99} \approx 250 \text{ kHz} \quad (4.4)$$

This is equal to a period of 4 μ s.

Figure 4.2 TRV of circuit breaker after the interruption of fault current

In the actual system, this high frequency transient voltage is damped by the system and will disappear after a relatively short period as is shown in Figure 4.2.

Under short line fault conditions, the line side generates a very high frequency voltage oscillation after the circuit breaker clears. The period of this voltage oscillation is also in the range of microseconds.

During the interrupting process, the circuit breaker can be regarded as an arc conductance, and after interrupting the insulation level between contacts, increases with time. The circuit breaker is in fact a non-linear resistance during the interrupting process. The arc channel resistance changes rapidly around current zero with a time constant of approximately a microsecond for SF₆ puffer circuit breakers and approximately ten microseconds for air-blast circuit breakers. The change of the arc resistance around current zero for a rotating arc circuit breaker is shown in Figure 4.3.

Figure 4.3 Measured (+) and calculated (line) arc channel resistance of a rotating arc circuit breaker around current zero [ref. 51]

4.2 The Network Computations

The power system is constructed with basic network elements: linear lumped time-invariant resistors, capacitors and inductors. When a transient happens in a network, it involves some non-linear elements in action in the system such as the arc in the circuit breakers. The transient and the presence of non-linear elements in the network requires time domain analysis of the network.

Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL) can be applied for analysis of both the steady state and the transient state. The network equations are constructed by the nodal admittance or the mesh impedance approaches. The network equations can be written as a set of Differential Algebraic Equations (DAEs).

The calculation of transients in an electrical network is, from the mathematical point of view, equal to solving a set of DAEs. The DAEs have the semi-explicit forms of equation (4.5) and equation (4.6).

$$x'(t) = f(t, x(t), y(t)) \quad (4.5)$$

$$O = g(t, x(t), y(t)) \quad (4.6)$$

where $x(t)$ is a vector of differential variables and $y(t)$ a vector of algebraic variables. Equation (4.5) is a set of ordinary differential equations (ODEs) while equation (4.6) defines the constraints. These equations can be obtained from a network by using the method of state variables.

The inductor current and capacitor voltage are taken as the state variables. The initial values of the inductor currents and the capacitor voltages can be used directly: their derivatives are not needed.

The problem that is typical of the calculation of transients in electrical networks, is the network stiffness. A set of differential equations is called stiff, if the time constants of the first order differential equations are widely different in magnitude or if one of the time constants is quite small in relation to the solution interval.

To solve the stiff ODEs in the DAEs, the step size should be smaller than the minimum time constant of the transient in the calculated network for the fixed step or order integration algorithms (such as Runge-Kutta and Runge-Kutta-Fehlberg methods). These will usually result in a long computation time or instability due to numerical noise for the calculation of the less interested steady state part of network. Using EMTP (Electro Magnetic Transient Program) or ATP (Alternative Transient Program) one encounters the problem of the fixed step size and the trapezoidal (Runge-Kutta fourth order) integration routine. Failure to maintain a sufficiently small step size will lead to a very low resolution in result.

To obtain shorter computation times in such cases, a more general approach of underlying mathematics is necessary. The most general form of a set of DAEs is:

$$F(t, y(t), y'(t)) = 0 \quad (4.7)$$

Gear developed a multistep method to solve stiff differential equations [67]. This method is called the method of Backward Differentiation Formulas (BDF). With the BDF method the differential variables x and the algebraic variables y are treated in similar fashion.

4.3 Gear Multistep Method for Stiff Problems

Gear's stiff method is an implicit self-initializing integration algorithm which uses the BDF method. These formulas are based on the numerical differentiation of the given system of equations. Assume that the approximations $y_{n-k+1}, \dots, y_n$ to the exact solution are known. In order to derive a formula for y_{n+1} we construct a polynomial $q(t)$ which satisfies

$$q_{n+1}(t_j) = y_i \quad \text{for } j = n-k+1, \dots, n+1 \quad (4.8)$$

This polynomial can be expressed in terms of backward differences, namely

$$q(t) = q(t_n + s * h) = \sum_{j=0}^k (-1)^j \binom{-s+1}{j} \nabla^j y_{n+1} \quad (4.9)$$

The unknown value y_{n+1} will now be determined in such a way that the polynomial $q(t)$ satisfies the differential equations at at least one grid-point, i.e.

$$q'_{n+1}(t_{n+1}) = f(t_{n+1}, y_{n+1}) \quad (4.10)$$

so we get the implicit formulas

$$\sum_{j=0}^k \delta_j^* \nabla^j y_{n+1} = h f_{n+1} \quad (4.11)$$

with the coefficient

$$\delta_j^* = (-1)^j \frac{d}{ds} \binom{-s+1}{j} \Big|_{s=1} \quad (4.12)$$

Using the definition of the binomial coefficient

the coefficients δ_j^* are obtained by direct differentiation:

$$(-1)^j \binom{-s+1}{j} = \frac{1}{j!} (s-1)s(s+1)\dots(s+j-2) \quad (4.13)$$

$$\delta_j^* = 0 \quad \delta_j^* = \frac{1}{j} \quad \text{for } j \geq 1 \quad (4.14)$$

Formula (4.11) therefore becomes

$$\sum_{j=1}^k \frac{1}{j} \nabla^j y_{n+1} = h * f_{n+1} \quad (4.15)$$

which are known as the BDF methods. For $k = 1$ we have the implicit Euler method with stability domain $S = \{ \mu; \mid \mu - 1 \mid \geq 1 \}$. For $k = 2$ the root locus curve (Figure 4.4) has $\text{Re}(\mu) = 3/2 - 2 \cos \theta + 1/2 \cos 2\theta$ which is ≥ 0 for all θ . Therefore the method is A-stable and of order 2. However, $k = 3, 4, 5$ and 6 , we see that the methods lose more and more stability on a part of the imaginary axis. For $k \geq 7$, as we know, the formulas are unstable anyway, even at the origin [66].

$$\begin{aligned} K=1: & y_{n+1} - y_n = hf_{n+1} \\ K=2: & \frac{3}{2}y_{n+1} - 2y_n + \frac{1}{2}y_{n-1} = hf_{n+1} \\ K=3: & \frac{11}{6}y_{n+1} - 3y_n + \frac{3}{2}y_{n-1} - \frac{1}{3}y_{n-2} = hf_{n+1} \\ K=4: & \frac{25}{12}y_{n+1} - 4y_n + 3y_{n-1} - \frac{4}{3}y_{n-2} + \frac{1}{4}y_{n-3} = hf_{n+1} \\ K=5: & \frac{137}{60}y_{n+1} - 5y_n + 5y_{n-1} - \frac{10}{3}y_{n-2} + \frac{5}{4}y_{n-3} - \frac{1}{5}y_{n-4} = hf_{n+1} \\ K=6: & \frac{147}{60}y_{n+1} - 6y_n + \frac{15}{2}y_{n-1} - \frac{20}{3}y_{n-2} + \frac{15}{4}y_{n-3} - \frac{6}{5}y_{n-4} + \frac{1}{6}y_{n-5} \\ & = hf_{n+1} \end{aligned} \quad (4.16)$$

As indicated in reference [69] Gear's *Stiff* is for systems which have frequencies of three or four orders of magnitude difference, where the high frequency motions are extremely active at some point (such as in a chemical reaction, explosion, etc.) and smooth to essentially zero amplitude. The Gear's *stiff* algorithm is then able to take large time steps since only the high frequency motions are of interest.

Figure 4.4 Root locus curves and stability domain of BDF

4.4 ACSL Language and Application

The Advanced Continuous Simulation Language (ACSL) program is commercially available and is suitable for the modelling of systems described by time-dependent, non-linear differential equations and/or transfer functions. ACSL provides a simple method for solving ordinary differential system on a digital computer. The program has a free form input, no sequence requirement for sorting the model equations, function generation of up to three variables and independent error control for each integrator.

A useful feature of ACSL is that there are different integration algorithms available for solving the ordinary differential equations. Gear's Stiff (BDF) method is one of them. As discussed in the preceding section the Gear's Stiff method is an adequate way to solve DAEs problems.

In ACSL, it is necessary to estimate the minimum step size for the simulation. The minimum step size criterium ensures the continuous calculations tolerating a certain error for each variable. The initial step size h in the ACSL Gear's Stiff method is determined

by

$$h = \max (MINT, \min (MAXT, CINT/NSTP)) \quad (4.17)$$

MAXT = maximum step size

MINT = minimum step size

CINT = communication (output points) interval

NSTP = number of integration steps in the communication interval

At each time step of the variable step algorithm, an interaction may occur until the predicted slope matches the calculated slope or derivative value. If all state derivatives fail to converge to within a given error tolerance within three attempts, the predictor correction iteration is considered to have failed and the step size is arbitrarily reduced by a factor of 0.25. If the predictor corrector iteration converges, then an estimate of the actual error made in the step can be calculated. This error estimate is compared with the allowable error. If this exceeds unity (i.e., the estimated error is greater than the allowable error), a reduced step size is calculated and the predictor corrector iteration is performed again. This sequence is continued until the step size is such that all the estimated errors are below the actual errors. It is possible for users to redefine the error criteria for each variable in the simulation.

4.5 Conclusion

The computation of power system transients is very important in network design and for its safe operation. The transient occurring in the power system generally involves a high frequency voltage and current oscillation. To calculate these transients, the network equations (Differential Algebraic Equations) are set up using the basic laws of circuit theory with the nodal admittance and the mesh impedance methods.

The calculation of transients in an electrical network is, from the mathematical point of view, equal to solving a set of DAEs. Stiff problems in the DAEs make the Runge-Kutta and Runge-Kutta-Fehlberg integration methods not suitable to solve the differential equations in power system transient analysis.

Gear's Stiff (BDF) integration method can use calculation steps that are orders of magnitude larger than the smallest time constant in a stiff problem. Gear's Stiff methods deal with stiff problems with good accuracy and with great time saving for the

calculation process.

The ACSL is used to compute the test circuits in this thesis, because of the possibility to apply Gear's Stiff method and because of the free form input of the network equations.

Chapter 5

Validity Study With an Arc Model

5.1 Introduction

The interrupting process for a TB can be divided into three time intervals: the high current phase, the thermal interaction interval around current zero and the dielectric recovery period. It is essential that, during a synthetic test, the breakers are stressed as severely as during a full direct test.

- The high current phase of the TB in the synthetic test circuits differs from the direct test circuit because of the presence of the AB in the current source circuit [16] [56]. The AB can result in a significant distortion of the current through the TB if the current source driving voltage is not properly selected.
- During the thermal interaction interval, a significant change in arc voltage, the current zero itself, and the post-arc current takes place. Different circuit topologies and circuit components contribute differently to the stress on the TB during this interval. The validity of a test circuit depends on the condition of giving " similar " stress in this interval. Stress similarity is difficult to judge by circuit analysis itself: the arc-circuit interaction has to be taken into account by modeling the impedance of the TB by means of an arc model.

- During the dielectric recovery period, the post-arc current is insignificant. Arc-circuit interaction does not play a role in determining the circuit equivalence. If different test circuits produce the same TRV waveform in this interval, it can be assumed that they influence the TB in the same way and do not require further equivalence study.

To verify the validity of test circuits for circuit breakers with a voltage rating of 765kV and above, computer simulations are presently the only practical possibility. When a circuit breaker interrupts a fault current, the whole process of current interruption lasts many milliseconds and the actual extinguishing of the arc takes place in a few microseconds. The arc conductance changes rapidly around current zero, causing a strong arc-circuit interaction. The validity of a laboratory circuit is based on realizing a similar arc-circuit interaction to that in the actual power system. In the computer simulations arc-circuit interaction, the circuit breaker must be represented by an arc model which, in practice, resembles the behavior of the circuit breakers.

In this chapter several arc models are discussed first. The KEMA arc model with parameters for a 765kV SF₆ circuit breaker is introduced, and finally the validity of the EPIC circuit is studied by using the KEMA arc model.

5.2 Arc Models for Circuit Breakers

Despite the complexity of the arc interruption process in circuit breakers, a variety of calculation methods has been developed in the last few decades, ranging from simple scaling laws to sophisticated numerical simulation methods. To simulate the arc interruption process, three groups of arc models can be distinguished (see reference [46]):

1. *Black box models, which consider the arc as a two-pole and determine the transfer function using a chosen mathematical form and fitting the remaining free parameters to measured $U(t)$ and $I(t)$ traces.*
2. *Physical arc models, which include the physical processes in detail, i.e. overall arc behavior is calculated from conservation laws, gas and plasma properties and more or less detailed models of exchange mechanisms (radiation, heat conduction, turbulence).*
3. *Formulae and diagrams which give parameter dependencies for special*

cases and scaling laws (for example short line fault limiting curves, scaling of chopping current with parallel capacitance and number of breakers). They may be derived from tests or from calculations with models 1 or 2.

Circuit breaker designers tend to use physical arc models, since they are particularly useful for designing new prototypes. As their name suggests, these models are based on the laws of physics such as those relating to the conservation of mass, momentum and energy, in combination with the Maxwell equations; they often consist of a large series of differential equations, which often take a long time to solve for every volume element, even by computer.

To describe the interaction of a switching arc and the corresponding electrical circuit during an interrupting process, the black box arc models are most often used because the electrical behavior is of importance rather than internal physical processes. However, the black box arc model appears insufficient to describe the complex interrupting process because of its one differential equation.

When a test circuit simulates a real network configuration, the arc models can be used to judge the equivalence of this test circuit and to determine the influence of individual circuit elements. *For stress which cannot be simulated in a test installation, conditions for a representative reduced test can be determined by model calculations [46].*

5.2.1 Black box models (mathematical models)

The aim of black box arc models is to describe the interaction of a switching arc and the corresponding electrical circuit during an interrupting process. For this purpose, an integral representation of the arc may be sufficient; the electrical behavior of the arc is of importance rather than internal physical processes. Black box arc models aim at results which are quantitatively correct within the accuracy limits of normal circuit breaker testing and measuring techniques. Black box arc models use a single differential equation: electrical conduction in the arc as a function of time.

Black box arc models are based on the energy balance in the arc: the difference between energy input and energy output is the change in the heat content and therefore a measure for the electrical conductance of the plasma between the circuit breaker contacts.

In its basic form, this balance can be expressed as follows:

$$g = F(P_{in}, P_{dis}, t) = \frac{I_b}{U_b} = \frac{1}{R} \quad (5.1)$$

- g = instantaneous arc conductance per unit length
 P_{in} = power supplied
 P_{dis} = power dissipated through cooling per unit length
 t = time
 I_b = instantaneous current
 U_b = instantaneous arc voltage
 R = instantaneous resistance per unit length

The instantaneous arc conductance g varies when the power supplied to the arc is not in balance with the power dissipated through cooling.

If Q is the amount of energy stored in the plasma per unit length, then it follows that:

$$Q = \int (P_{in} - P_{dis}) dt \quad (5.2)$$

$$g = F(Q) = F \left[\int (P_{in} - P_{dis}) dt \right] \quad (5.3)$$

If we differentiate 5.3:

$$\frac{dg}{dt} = \frac{dF(Q)}{dQ} \cdot \frac{dQ}{dt} \quad (5.4)$$

divide by the conductance

$$\frac{1}{g} \frac{dg}{dt} = \frac{1}{g} \frac{dF(Q)}{d(Q)} \cdot \frac{dQ}{dt} \quad (5.5)$$

If we differentiate 5.2 and fill in the result together with 5.3, we have:

$$\frac{d(\ln(g))}{dt} = \frac{F'(Q)}{F(Q)} \cdot (P_{in} - P_{dis}) \quad (5.6)$$

Equation 5.6 is known as the general arc equation. It is a useful equation because the arc temperature, which is difficult to measure as a function of time, is not required. To solve the differential equation, a number of assumptions have to be made. It are these assumptions which form the bases of the various models (named after their originators).

5.2.1.1 Cassie arc model

Cassie assumed the arc channel to be cylindrical. Within the cylinder, the arc temperature remains constant, but the cross-section D varies. The heat content per unit volume therefore remains constant, as consequently does the conductivity per unit volume. The arc diameter varies due to the effects of cooling, which takes place by convection; the outer layers are, so to speak, blown off.

However, the loss of an outer layer does not affect the temperature of the remaining arc channel, or, therefore, the conductivity per unit volume.

Figure 5.1 Cylindrical arc channel, as envisaged by Cassie

Let:

g_0 = the conductivity constant per unit volume

- P_0 = the cooling (or power loss) per unit volume
 D = the cross-section of the arc channel, varying with time
 Q_0 = the heat content per unit volume

By defining the constants g_0 , P_0 , and Q_0 , it is possible to express the voltage gradient as $E_0 = \sqrt{\frac{P_0}{g_0}}$

The conductance is therefore:

$$g = F(Q) = D \cdot g_0 \quad (5.7)$$

Energy as a function of time can be obtained from:

$$Q = Q_0 \cdot D \quad (5.8)$$

From equations 5.7 and 5.8, we have:

$$g = F(Q) = \frac{Q}{Q_0} \cdot g_0 \quad (5.9)$$

and

$$F'(Q) = \frac{g_0}{Q_0} \quad (5.10)$$

For the power dissipated per unit length:

$$P_{dis} = D \cdot P_0 = \frac{Q}{Q_0} \cdot P_0 \quad (5.11)$$

If equations 5.9, 5.10 and 5.11 are incorporated in the basic arc equation, the result is

$$\begin{aligned}
 \frac{d(\ln(g))}{dt} &= \frac{g_0/Q_0}{Q g_0/Q_0} \left(P_{in} - \frac{Q}{Q_0} P_0 \right) = \frac{P_{in} - Q P_0/Q_0}{Q} \\
 &= \frac{U^2 g - Q P_0/Q_0}{Q} \\
 &= \frac{U^2 Q/Q_0 g_0 - Q P_0/Q_0}{Q} \\
 &= \frac{P_0}{Q_0} \left(\frac{U^2}{E_0^2} - 1 \right)
 \end{aligned} \tag{5.12}$$

$$\text{With } E_0^2 = \frac{P_0}{g_0}$$

U = arc voltage changing with time.

The term Q_0/P_0 is called the arcing time constant τ because at the current zero, the current through the arc is zero, so that $U = 0$. The solution of the differential equation

$$\frac{d(\ln(g))}{dt} = - \frac{P_0}{Q_0} \tag{5.13}$$

is:

$$g = g_0 \exp \left(- \frac{t}{\tau} \right) \tag{5.14}$$

The arcing time constant τ can therefore be regarded as the time constant governing the diminution of the arc channel diameter.

5.2.1.2 Mayr arc model

The Cassie formula is valid at high current regions, i.e. not around the current zero.

Mayr's description of the physical processes at work in the arc channel was based on the assumption that around current zero the cross-section of the arc and the temperature remain constant. Mayr saw the arc column as losing its energy by the radial conduction of heat. The temperature of the arc channel lies in the range where conductivity varies more or less exponentially with temperature. Mayr described conduction by

$$g = F(Q) = K \exp(Q/Q_0) = \frac{1}{R} \quad (5.15)$$

in which Q_0 is the characteristic energy content and K a constant.

Mayr also assumed the power dissipated from the arc channel to be constant:

$$P_{dis} = P_0$$

If this is then inserted in the basic arc equation, we have:

$$\frac{d(\ln(g))}{dt} = \frac{F'(Q)}{F(Q)} \cdot (P_{in} - P_{dis}) \quad (5.16)$$

$$\frac{d(\ln(g))}{dt} = \frac{U \cdot I - P_0}{Q_0} \quad (5.17)$$

U = arc voltage changing with time, while

I = arc current changing with time.

At the moment of current zero, the power supply term $U I$ equals zero and the diminution of conductance with time is governed by:

$$\frac{dg}{dt} = -g \cdot \frac{P_0}{Q_0} \quad (5.18)$$

The solution to this differential equation is:

$$g = g_0 \exp \left(\frac{-t}{Q_0/P_0} \right) \quad (5.19)$$

Q_0/P_0 is referred to as the thermal constant τ of the arc, so that conductance can be expressed as follows:

$$g = g_0 \exp (-t/\tau) \quad (5.20)$$

The Mayr equation can therefore be presented as follows:

$$\frac{1}{g} \frac{dg}{dt} = \frac{1}{\tau} \left(\frac{UI}{P_0} - 1 \right) \quad (5.21)$$

5.2.1.3 Generalized arc models

The Cassie formula is valid at the high current region ($T > 10,000 \text{ K}$) and the Mayr formula applies around the current zero ($T < 10,000 \text{ K}$). It has been recognized for a long time that the original Cassie and Mayr arc models are insufficient for the simulation of circuit breakers, in particular after current zero. Many other arc models have been proposed.

Browne pointed out that a simple combination of the Cassie arc model at high current with Mayr arc model at current zero is particularly useful [47]. Based on his investigations, a combination arc model is used with the form of Cassie-Mayr-Cassie. In this model *the Cassie equation for the high current arc is assumed to apply prior to current zero and also following a " thermal " reignition shortly after a current zero. The Mayr equation is employed in the intermediate time region between the two Cassie regimes, or simply following the Cassie regime for a successful interruption (neglecting the possible case of later dielectric breakdown)* [70].

Urbanek combines the Mayr and Cassie arc models in one equation with some necessary modifications as shown in equation 5.22 [17].

$$\frac{dg}{dt} = \frac{1}{\tau} \left[\frac{UI}{u_0^2} - g - \frac{P_0}{u_0^2} \left(1 - \frac{U^2}{u_d^2} - \frac{2\tau U}{u_d^2} \frac{dU}{dt} \right) \right] \quad (5.22)$$

τ = time constant of arc

u_0 = minimum arc voltage at high currents

P_0 = minimum power input to maintain arc

u_d = dielectric breakdown voltage of the cold arc channel

5.2.2 KEMA Arc Model

Mayr, Cassie, Cassie-Mayr-Cassie and Urbanek arc models are all mathematical models devised from greatly simplified physical models. They are more or less with difficulty to match the practical arc phenomena. In this section, the KEMA arc model is introduced which employs the mathematic model (improved Mayr arc model) before current zero and uses the physical recombination model after current zero. This arc model represents the behavior of circuit breaker well [48] [51].

For a circuit breaker, and especially an SF₆ circuit breaker, more attention has to be paid to the thermal interaction interval [63] [64]. Around current zero, the Mayr arc model appears to be appropriate. However, measurements reveal that a simple Mayr arc model, with constant cooling power P and time constant τ , is neither applicable to SF₆ circuit breakers of the puffer type nor for breakers of the rotating arc type. Based on the Mayr arc model, KEMA's arc model before current zero (5.23) takes the influence of the current on the cooling power P into account. With this modification, the arc behavior in SF₆ circuit breakers can be modelled close to reality [48] [56].

$$\frac{1}{g} \frac{dg}{dt} = \frac{1}{\tau} \left[\frac{UI}{p(P_0 + C_0 |I|)} - 1 \right] \quad (5.23)$$

τ = arc time constant

p = gas pressure

P_0 = cooling power at current zero

C_0 = constant

After current zero, the physical processes which take place in the arc column are described in KEMA's arc model by equation (5.24), which computes the changes of the conductivity of the arc channel due to the changes in the electron number density of N_e caused by diffusion γ , electron-ion recombination (β_{e-i}), attachment (η) and ionization

(α).

$$G = C_e N_e \frac{T r^2}{p L} + C_i (N_+ + N_-) \frac{T r^2}{p L} \quad (5.24)$$

T = neutral gas temperature

r = radius of arc channel

L = length of arc channel

C_e, C_i = constants

N_e, N_+, N_- = number of charged particles

The number density of the charged particles (electrons, positive and negative ions) in (5.24) can be computed by the following equations.

$$\begin{aligned} \frac{dN_e}{dt} &= -\gamma N_e - \beta_{e-i} N_e N_+ + \alpha_{eff} |V_{dr}| N_e \\ \frac{dN_-}{dt} &= -\alpha_{eff}^{\min} |V_{dr}| N_e - \beta_{i-i} N_- N_+ \\ N_+ &= N_e + N_- \end{aligned} \quad (5.25)$$

V_{dr} = drift velocity of the electrons

$$\alpha_{eff} = \max(\alpha_{eff}^{\min}, C_a \left| \frac{U}{L} \right| - \frac{p}{T} \left(\frac{E}{N} \right)_{crit}) \quad (5.26)$$

N = gas density

C_a = constant

E = electric field strength (= U/L)

The drift velocity V_{dr} of electrons and ions in an electric field depends on the reduced electric field E/N , in which N represents gas density. Linear dependence on E/N is assumed.

Recombination coefficients for molecular gases at room temperature are in the order of 10^{-14} m³/sec for electron-ion processes and 10^{-13} m³/sec for ion-ion processes. In hot decomposed gases the temperature dependence has been taken into account by a factor proportional to $T^{-3/2}$; also numerical values were taken from measurements and have been standardized at 3,000 Kelvin as shown in equation 5.27.

$$\begin{aligned}\beta_{e-i} &= \beta_{e-i(0)} (3000/T)^{3/2} \\ \beta_{i-i} &= \beta_{i-i(0)} (3000/T)^{3/2}\end{aligned}\quad (5.27)$$

$\beta_{e-i(0)}$ = initial electron-ion recombination

$\beta_{i-i(0)}$ = initial ion-ion recombination

The time dependence of the gas temperature T has the expression of 5.28. The temperature T with a double exponential decay, starting at 8,000 Kelvin.

$$T = 4500 e^{-\frac{t}{10} 10^6} + 3500 e^{-\frac{t}{200} 10^6} \quad (5.28)$$

where t is the time after current zero

The arc radius r decays exponentially too as given in equation 5.29.

$$r = r_0 e^{-\frac{t}{500} 10^6} \quad (5.29)$$

r_0 = arc radius at current zero

5.3 Validity Study of the EPIC Circuit with the KEMA Arc Model

5.3.1 The high current phase

During the high current phase, the test breaker must be stressed by the test circuit in such a way that the starting conditions for the interaction interval, within certain tolerance limits, are the same as for the reference system (direct test circuit) conditions. This includes such conditions as the state of ionization of the plasma, temperature, gas flow pressure, electrode heating, etc. To meet these conditions, the energy input into the arc channel of the TB during the last current loop is important. If the relative arc energy reduction in the last current loop is less than 12% (corresponding to the distorted current peak and the duration of the last current loop, less than 90% of the values specified), equivalence is assumed by the IEC standard. To realize this, a minimum current source driving voltage is needed for the current circuit. According to the calculations (Figure 2.4), the minimum driving voltage should be at least 3.5 times for the linear rising arc voltage waveform, at least 7.7 times for the trapezoidal arc voltage waveform and at least 12 times for the constant arc voltage waveform, the sum of the arc voltages in AB1 and

TB.

In the EPIC circuit auxiliary circuit, AB2 does not contribute to the current distortion in the high current phase. There is no difference between the EPIC circuit and classical Weil circuit in this phase with respect to current distortion. When the current circuit driving voltage is properly selected, the validity of the EPIC circuit is assured in the high current phase.

5.3.2 The thermal interaction interval

During the interaction interval, the short-circuit stress changes into high-voltage stress and the circuit breaker performance can significantly influence the current and voltages in the circuit. As the current decreases to zero, the arc voltage may rise to charge parallel capacitance and distort current passing through the arc. After the current zero, the post-arc conductivity may result in additional damping of the transient recovery voltage and thus influence the voltage across the circuit breaker and the energy supplied to the ionized contact gap. The interaction between the circuit and the circuit breaker immediately before and after current zero (i.e. during the interaction interval) is of extreme importance to the interrupting process.

During the interaction interval, the current and voltage waveforms will be the same for a synthetic test as under a reference system (direct test circuit) conditions, taking into account the possible deviations of the current and voltage from the prospective values due to the interaction between the circuit breaker and the circuit. -- (IEC-427 4.1.2).

In this interval, the arc impedance in the TB changes drastically and also the arc-circuit interaction. A validity study by simple circuit calculations is not appropriate. The arc-circuit interaction must be taken into account. A good representation of the arc channel conductivity is essential for the numerical calculations to prove the test circuit's validity.

5.3.2.1 KEMA arc model parameters for a 765kV-63kA-50Hz SF₆ puffer circuit breaker

The parameters used in KEMA's arc model can be deduced from experimental tests on a specific circuit breaker, and the arc model parameter combination only

represents that particular circuit breaker. When test results are not available, choice of the arc model parameters has to be based on literature and experience. The rated voltage, rated short-circuit current and difference in nozzle design of the different circuit breakers have their influence on the selection of the arc model parameters such as the arc channel length, the arc channel diameter at current zero, the cooling power at current zero, etc. The choice of the arc model parameters has to be supported by a good match of simulation results and test results [56] [63].

Figure 5.2 Arc voltage and current of the TB in the direct test circuit with the modified Mayr arc model

Table 5.1 Arc model parameters for the TB and the AB2 before current zero

Parameters	TB	AB2
P_0 (kW/bar)	10.0	10.0
τ (μs)	1.00	6.0
C_0 (V/bar)	850.0	150.0
p (bar)	5.0	5.0

The arc voltage and the current before current zero have, in general, the form shown in Figure 5.2. If 4.25kV steady state arc voltage is assumed for the TB during the high current interval, and if 0.75kV arc voltage is assumed for the AB2 during the current injection period, the arc model parameters given in Table 5.1 result in the arc voltage and

current waveform shown in Figure 5.2.

The parameters for the KEMA recombination model are assumed for the 765kV-63kA-50Hz SF₆ test circuit breaker as given in Table 5.2. The radius of the arc channel at current zero (r_0) increases proportionally to the interrupting current I . The arc length (L) is proportional with the rated test voltage. The recombination model describes the arc conductance after current zero resulting in a post-arc current and an initial TRV as plotted in Figure 5.3.

Table 5.2 Recombination model parameters for the TB

Parameter	Value
L (cm)	15.0
r_0 (mm)	1.50
$\alpha_{\text{eff}}^{\text{min}}$ (1 / m)	- 0.01
$\beta_{e-i(0)}$ (m ³ / s)	1.0×10^{-14}
$\beta_{i-i(0)}$ (m ³ / s)	5.0×10^{-13}

Figure 5.3 Post-arc current and transient recovery voltage of the TB in the direct test circuit with the KEMA recombination model

The arc model simulating the TB in the reference direct test circuit has a calculated arc channel resistance around the current zero as plotted in Figure 5.4. These computed results match the curves published in literature well [51].

Figure 5.4 Arc channel resistance of the TB in a direct circuit simulated with the KEMA arc model

5.3.2.2 Validity study of the EPIC circuit with the KEMA arc model

To verify the behavior of the KEMA arc model simulating an 765kV-63kA-50Hz circuit breaker in the reference direct test circuit (Figure 2.2), and in the EPIC test circuit (Figure 3.1), a series of calculations was made to compare the difference between the two circuits during the arc-circuit interaction interval. The short-circuit current and the post-arc current around current zero in both test circuits are similar, as can be seen in Figure 5.5. The slightly smaller post-arc current indicates that the EPIC circuit stresses the TB a little less in the thermal interaction interval.

Two parameters in the arc model can be used to quantify the circuit stress on the interrupting behavior of the TB: the arc channel resistance and the minimum gas filling pressure necessary for clearing. The arc channel resistance at current zero is a measure for circuit influence, because the critical arc-circuit interaction takes place before current zero. A higher arc resistance at current zero (R_0) indicates a lower stress of the test circuit on the TB. A comparison of the TB arc channel resistance at current zero in the

reference and the EPIC circuit is given in Table 5.3.

Figure 5.5 Comparison of the TB current during the current zero period

Table 5.3 Arc channel resistance at current zero

Test circuit	R_0 ($k\Omega$)
Direct	1.46
EPIC	1.77

A low arc channel resistance at current zero results in a thermal reignition of the TB. The reignition of the arc model is plotted in Figure 5.6. To improve the interrupting capability of the breaker model, the gas pressure must be increased. Corresponding to the calculation of Figure 5.6, different minimum gas filling pressures are found (Table 5.4) by calculations made in the direct test circuit and the EPIC circuit. The pressure difference in pressure is 1%.

As analyzed in section 2.2.3, the current injection synthetic test circuit always gives less stress on the TB because of the decrease in di/dt before current zero when the arc-circuit interaction is taken into account. A method to compensate for this during a practical test in the high power laboratory is to increase the charging voltage proportionally to the value of the arc voltage in the TB. In the equivalence study of this

chapter, this has not been done. It is clear that if a higher charging voltage for C_0 is used in our computations, more precise values for the TB arc channel resistance at current zero and minimum gas filling pressure of the TB are found.

Figure 5.6 Calculated thermal reignition of the TB in the direct test circuit

Table 5.4 Minimum pressure of TB to clear

Test Circuit	P (bar)
Direct	5.00
EPIC	4.95

5.3.3 The dielectric recovery period

During the dielectric recovery period, the gap of the TB is stressed by the recovery voltage. The prospective TRV waveform must comply with the requirements of the IEC or the ANSI standard, and the impedance of the circuit must be low enough to provide for reignitions or restrikes when they occur.

The voltage source circuit of the EPIC circuit has a surge impedance of Z_{inj} , which is about 72Ω during the first slope of the four-parameter TRV with a sinusoidal current

after reignition or restrike. The impedance of the voltage source after the first slope of TRV is roughly equal to the resistor $R_{22} = 288 \Omega$ with a sum of exponential current and decayed sinusoidal current after restrikes. The exponential current comes from the discharge of C_{21} and C_{22} . This high exponential current provides the major part of the short-circuit current after restrikes. The time constant of the exponential current is about $250 \mu\text{s}$.

Because the EPIC circuit yields a TRV satisfying the IEC four-parameter waveform (Figure 3.2), and the circuit can supply a high current after reignition or restrikes, the EPIC circuit meets the requirements of IEC-56 during the dielectric recovery period.

5.4 Conclusion

At a voltage level of 765kV and above, a validity study of synthetic test circuits by comparability tests is unrealistic, because of the limitation of the direct test source in the test laboratories or the extreme cost of a field test. To prove the equivalence of a synthetic test circuit, other method has to be followed in this case. A good representation of the arc behavior in the TB by means of an arc model makes it possible to study the arc-circuit interaction, and to demonstrate the equivalence between the direct and synthetic test circuits.

It is demonstrated by the analysis in this chapter that the EPIC circuit stresses the TB according to the requirements set by the standard during the thermal interval of the breaking process. The arc-circuit interaction in the EPIC circuit corresponds to what happens in a direct test circuit. The validity of the EPIC circuit is proven when hardly any difference is found in the value for the minimum SF_6 gas filling pressure needed for arc extinction during the thermal interaction interval in the computer simulations. When the gas pressure is used to judge the circuit stress in the arc model, it was found that the relative stress decrease of the EPIC circuit is only 1%.

Like the classical parallel current injection synthetic test circuit, the equivalence of the EPIC circuit in the high current phase is determined by the current source driving voltage, which is limited by the installed short power capacity of current source circuit in the test laboratories. If an appropriate driving voltage is selected for the arc voltage waveforms in the TB and the AB1, the EPIC circuit satisfies the specifications of IEC standards.

The EPIC circuit is a valid circuit in the dielectric recovery voltage period because of its IEC four-parameter waveform.

Chapter 6

Configuration, Parameter Sensitivity and Operation

6.1 Introduction

Because of the topology of the EPIC circuit it is not so easy to select the component values for a certain breaker rating and test duty. It follows from the operating principle of the EPIC circuit that, independent of the capacitive energy requirement and the practical operation, there are many possible parameter combinations to form a test circuit which can produce the IEC four-parameter TRV (Figure 3.2). An optimal circuit parameter combination depends on less use of the capacitive energy and makes the operation of the circuit easy.

The component values used in the EPIC circuit may differ from the calculated values found in the laboratories. Especially, the triggering of AB2 and spark Gap 1 may in practice have a deviation. The parasitic inductance and capacitance of the circuit built in practice also play a role in the arc-circuit interaction and influence the TRV waveform. This must be considered during the test circuit design. In other words, the TRV must not be too sensitive to the circuit parameter values, the circuit operation and the stray inductances and capacitances.

Safety and economical operation are other aspects of the circuit lay-out to be considered. Safety and economical operation are two important factors for test laboratories because of the cost of both the TB prototype and the laboratory equipment.

Potential damage to the test breaker and other test equipment must be avoided or minimized. The overvoltage caused by the reignition or restrike of the switching elements (TB, AB1 and AB2), mistiming in the test sequence is the main cause for damage to the test equipment. A good understanding to the overvoltage is important to design or to use the test circuit.

In the first part of this chapter, the configuration of the TRV branches is analyzed. The influence of different parameter combinations on the interrupting performance of the TB is discussed. A recommended parameter combination for the TRV branches is derived. The influence of the circuit parameter deviation is studied. In the second part of this chapter, a detailed analysis of the operating behavior of the EPIC circuit is given. The overvoltages and the overvoltage protection measures built into the EPIC circuit are calculated and analyzed.

6.2 The Circuit Configuration and Circuit Parameter Sensitivity Study

6.2.1 The current injection circuit and the AB2

Unlike in the conventional parallel current injection synthetic test circuit, the current injection part of the EPIC circuit does not require a higher inductor L_I in its circuit design. On the contrary, a same or even a lower value is selected in order to decrease the charging voltage on the main capacitance bank C_0 , and to reduce the capacitive energy needed for the current injection circuit. The value of C_0 is lower than the value used in the conventional parallel current injection circuit, because C_0 does not have to maintain a constant voltage for charging the TRV circuit element after current zero to form the full four-parameter TRV. The value of C_0 is determined by the peak value of the oscillation voltage, which is roughly equal to the first reference voltage U_I of the IEC TRV waveform. Because of the low component values for inductance L_I and capacitance C_0 , a higher current injection frequency can be realized with the EPIC circuit. A 5% deviation in C_0 and L_I hardly influences the current injection frequency. The di/dt at current zero is independent of the value of C_0 but dependent on the value of L_I . The di/dt deviation caused by the value deviation of L_I can be compensated by adjusting the precharged voltage on C_0 .

The extra injected current from the precharged TRV element C_I in the EPIC circuit deforms the injected current into superposition of a sinusoidal and exponential current. Although the exponential injected current can improve the quality of the actual current

waveform, it is better practice that the exponential current I_{11} damped out before the current zero of the sinusoidal injected current in order to obviate any possible influence on the circuit di/dt before the current zero of the TB. Fortunately, the current injection circuit has a natural damping such that the exponential current is damped out before the sinusoidal injected current zero. This is illustrated in equation 6.1 by the high ratio (K) of one injection current loop in relation to the time constant of branch $R_1 - C_1$.

$$K = \frac{T/2}{\tau} = \frac{\pi \sqrt{L_1 C_0}}{R_1 C_1} \geq \frac{\pi \sqrt{L_1 C_0}}{2 \sqrt{L_1/C} C_1} = \frac{\pi}{2} \sqrt{\frac{C_0^2}{(C_1 + C_0) C_1}} \geq \frac{\pi}{2 \sqrt{2}} = 1.11 \quad (6.1)$$

For the 765kV-63kA-50Hz test circuit K has a value of 6.58. The C_1 is assumed to be completely discharged at the sinusoidal injected current zero.

A spread in the triggering of AB2 is unavoidable. If the triggering takes place at the two extreme injection moments (Figure 6.1 a and Figure 6.1 b), the circuit certainly stresses the TB inappropriately as was explained earlier. According to the requirement of IEC-427 for the parallel current injection testing, the tolerance of the triggering instant for a 400Hz sinusoidal injected current is about 300 μ s. A plasma injection type AB2 can meet this tolerance without problems.

Figure 6.1 Diagram illustrating the current waveforms resulting from the two extremes of the AB2 triggering moment

6.2.2 The TRV branches

To produce a four-parameter TRV in the direct test circuit a double-frequency TRV circuit is necessary. This is often commonly used in the conventional synthetic test methods. In the EPIC synthetic test circuit a different method is used to realize the four-parameter TRV. The four-parameter TRV is provided by two single frequency oscillating circuits which apply the oscillated voltages to the TB in turn. From the current injection moment to the time t_i of the first reference recovery voltage U_i , the first single frequency voltage circuit is in operation. After t_i the second single frequency voltage circuit applies its oscillation voltage to the TB instead of the first one. The two single frequency voltage oscillation circuits have a short overlap in time during the transition from the first circuit to the second circuit.

Figure 6.2 The simplest R-L-C single frequency voltage oscillation circuit

The R-L-C circuit shown in Figure 6.2 is the simplest single frequency voltage oscillation circuit. R_Σ and C_Σ are the TRV circuit. After the TB clears the oscillation voltage taken place in the loop $C_0 - L_1 - R_\Sigma - C_\Sigma$ forms the first slope of four-parameter TRV as shown in Figure 6.3 with the voltage expression of equation 6.2 and rate of rise of voltage of equation 6.3.

$$U = \frac{C_0 U_0}{C_0 + C_\Sigma} \left[1 - e^{-\alpha t} \left(\cos \beta t - \frac{\alpha}{\beta} \left(1 + \frac{2 C_\Sigma}{C_0} \right) \sin \beta t \right) \right] \quad (6.2)$$

$$\alpha = \frac{R_\Sigma}{2 L_1} \quad \beta = \sqrt{\frac{1}{L_1 C} - \left(\frac{R_\Sigma}{2 L_1} \right)^2} \quad C = \frac{C_0 C_\Sigma}{C_0 + C_\Sigma}$$

$$\frac{dU}{dt} = \frac{C_0 U_0}{C_0 + C_\Sigma} e^{-\alpha t} \left\{ \left[\beta - \frac{\alpha^2}{\beta} \left(1 + \frac{2C_\Sigma}{C_0} \right) \right] \sin \beta t + 2\alpha \left(1 + \frac{C_\Sigma}{C_0} \right) \cos \beta t \right\} \quad (6.3)$$

Figure 6.3 Voltage waveform of the R-L-C circuit in figure 6.2

The surge impedance R_Σ is important in determining the circuit stress during the thermal interaction interval for the current injection circuit. The value of R_Σ can be calculated by equation 6.4. The dU/dt is by IEC-56 fixed at a value of $2\text{kV}/\mu\text{s}$ for circuit breakers with a rated voltage of 110kV and above. The di/dt changes with the prospective breaking current rating. For the breaking current 63kA the di/dt is $28\text{A}/\mu\text{s}$. The R_Σ is in that case equal to 72Ω .

$$R_\Sigma = \frac{dU/dt}{di/dt} \quad (6.4)$$

From equation 6.2 and equation 6.3 it can be seen that the dU/dt and the peak value U of the oscillating voltage can remain unchanged for different interrupting current ratings because the value of the capacitance C in equation 6.2 can be changed to cope with the different interrupting current ratings. A higher interrupting current requires a higher value of the total capacitance C and subsequently also a higher value of C_0 and C_Σ . For the same breaker voltage rating, the capacitive energy necessary for the parallel current injection circuit increases with the testing current.

In the EPIC circuit arrangement, the first slope of the four-parameter TRV is realized by Figure 6.2 R-L-C circuit, the TRV branch $R_\Sigma - C_\Sigma$ is divided into two parallel branches with the auxiliary circuit breaker AB2 serving as a "Tie"-breaker (Figure

6.4). The impedance ratio of branch $R_1 - C_1$ and branch $R_{22} - C_2$ (C_2 consists of two capacitors C_{21} and C_{22} connected in series) influences the stress caused by the last current loop and the recovery voltage stress. Different ratios result in different stresses on the AB2 as shown in Figure 6.5. The lower the ratio is the less stress the AB2 undergoes. However, the lower value of this ratio is fixed by the need for a low impedance in the second voltage source circuit. The sum of the impedances in the branch $R_{22} - C_{22}$ and in the second voltage injection circuit must be low enough to provide energy for reignitions and restrikes if they occur. The small current of the last current loop in the AB2 may produce a rather high arc voltage and this will decrease the peak of the TRV across TB a little. A higher extra injection current is supplied by the branch $R_1 - C_1$ when the

Figure 6.4 Simplified TRV oscillating circuit for the current injection circuit

Figure 6.5 Last current loop and recovery voltage on the AB2 under different TRV branches impedance ratios

impedance ratio is low. This cannot be seen from Figure 6.5 because the last current loop and the TRV across the AB2 do not change very much when the ratio is less than 1:3. In the EPIC circuit the impedance ratio between branch $R_1 - C_1$ and branch $R_{22} - C_2$ is fixed at 1:3.

The second slope of the four-parameter TRV is produced by the simplified voltage oscillating circuit in the EPIC circuit arrangement shown in Figure 6.6.

Figure 6.6 Simplified TRV oscillating circuit after the first slope of four-parameter TRV

$$U = U_0 + \frac{C_h(U_h - U_0'')}{C_h + C_{21}} \left[1 - e^{-\alpha t} \left(\cos \beta t - \frac{\alpha}{\beta} \left(1 + \frac{2C_{21}}{C_h} \right) \sin \beta t \right) \right] \quad (6.5)$$

$$\alpha = \frac{R_h}{2L_h} \quad \beta = \sqrt{\frac{1}{L_h C} - \left(\frac{R_h}{2L_h} \right)^2} \quad C = \frac{C_h C_{21}}{C_h + C_{21}}$$

$$\frac{dU}{dt} = \frac{C_h(U_h - U_0'')}{C_h + C_{21}} e^{-\alpha t} \left[\left(\beta - \frac{\alpha^2}{\beta} \left(1 + \frac{2C_{21}}{C_h} \right) \right) \sin \beta t + 2\alpha \left(1 + \frac{C_{21}}{C_h} \right) \cos \beta t \right] \quad (6.6)$$

The damping resistor of the second voltage circuit influences the second voltage slope slightly but decays the voltage oscillation of the second voltage circuit significantly. Therefore no damping resistor is arranged in the second voltage circuit.

6.2.3 The voltage injection circuit and the spark Gap 1

The capacitor C_2 in Figure 6.4 consists in practice of two capacitors C_{21} and C_{22} connected in series. Apart from a role as TRV element in the current injection circuit, the capacitor C_{21} also plays a role in the second voltage circuit. When the value for the C_2 is fixed the division between C_{22} and C_{21} is of importance.

As calculated in Table 6.1, different capacitance ratios of C_{22} to C_{21} result in different component values for the second voltage source circuit.

Table 6.1 Component values for the second voltage circuit for different ratios of $C_{22} : C_{21}$

Ratio	1 : 1	1 : 2	1 : 3	1 : 4
C_{21} (μF)	1.31	1.96	2.61	3.26
C_{22} (μF)	1.31	0.98	0.87	0.82
C_h (μF)	3.50	3.50	3.50	3.50
L_h (mH)	110.0	79.0	65.0	57.0
U_h (kV)	667.0	618.0	618.0	637.0
$i_{2 \text{ peak}}$ (kA)	1.14	1.71	2.28	2.84

All the different parameter combinations in Table 6.1 result in an similar TRV waveform. It can be seen from Table 6.1 that a reasonable capacitance ratio lies between 1:2 and 1:3. A lower capacitance ratio than this or too high a capacitance ratio requires a higher charging voltage on C_h .

The spread in the triggering of spark Gap 1 has a greater impact on the operation of the EPIC circuit. The spread in the triggering influences the peak of the TRV voltage U_c and the reference time t_2 as depicted in Figure 6.7. The first reference recovery voltage U_1 and the reference time t_1 are hardly influenced by the spread in the triggering of spark Gap 1. An early triggering of spark Gap 1 will decrease the peak of the TRV and will shorten the time to peak, and a delayed triggering of spark Gap 1 will increase the peak of the TRV and will increase the time to peak. The changes in the peak voltage U_c and in the reference time t_2 as a function of the spread in the triggering of spark Gap 1 are calculated in Table 6.2.

Figure 6.7 Variation in the waveform of the TRV across the TB as a function of different triggering instants of Gap 1

Table 6.2 The peak voltage U_e and the t_2 vs the deviation of triggering instant of spark Gap 1

Triggering deviation (μs)	Peak Voltage U_e		Time t_2	
	value (kV)	deviation (%)	value (μs)	deviation (%)
-100	1104	-3.24	1088	-9.48
-50	1123	-1.58	1145	-4.74
0	1141 (1137)*	0	1202 (1218)*	0
+50	1157	1.36	1258	4.66
+100	1170	2.45	1315	9.40
+150	1181	3.46	1370	13.98

* The values between brackets are the IEC specified values

Special attention has to be paid to the design of spark *Gap 1* because the spread in the triggering instant has a not negligible influence on the second slope of the recovery voltage ($U_1 t_1$, $U_c t_2$).

The influence of the parasitic capacitance of the connections between the voltage circuits and the terminals of the test breaker can be neglected, because the value of the lumped time delay capacitor exceeds the parasitic capacitance of the connections. The parallel connected time delay capacitor across the terminals of the TB in the EPIC circuit has the same value as in the direct test circuit.

6.3 Overvoltages and Overvoltage Protection

6.3.1 Overvoltage in the current source side circuit

The overvoltage in the current source side circuit appears when there is a reignition or a restrike of auxiliary circuit breaker AB1. The AB1 isolates the current circuit from the voltage circuit after the current zero of main current (Figure 6.8). A reignition or a restrike of AB1 reconnects the voltage circuit and current circuit with each other. The high voltage of the voltage circuits is injected into the current circuit and produces a harmful overvoltage in the current circuit.

Figure 6.8 Current and voltage on the AB1 under normal operating conditions

A typical overvoltage waveform in the current circuit after a thermal reignition of the AB1 is shown in Figure 6.9. The maximum overvoltage in the current circuit occurs at the instant when the AB1 restrikes at the peak of the TRV. The peak value and the waveform of the overvoltage depend mainly on the discharge of the TRV adjusting circuit in the voltage circuits.

The overvoltage in the current circuit can damage the insulation of the transformers and the generators. Test experience shows that an Z_nO surge arrester or a protective gap (P -gap in Figure 6.10) at the high voltage side of the transformer, the parallel connected capacitor and the Z_nO surge arrester at the primary side of the transformer (Z_nO and C_p in Figure 6.10) are sufficient for overvoltage protection. Similar protection techniques can be used to protect the EPIC circuit because there is no difference in the origin of the overvoltage in the current circuit when the AB1 fails to clear in the EPIC test circuit.

Figure 6.9 Overvoltage in the current circuit when the AB1 has a thermal reignition

The current circuit overvoltage protection elements in the EPIC circuit are drawn in Figure 6.10 with dotted lines.

Figure 6.10 Current source circuit overvoltage protection branches

6.3.2 Overvoltages on the voltage source side and analysis of possible maloperations

An overvoltage on a component in the voltage circuits can occur in the case of failure of the test breaker or maloperation of the test sequence. It is necessary to protect the equipment against the harmful overvoltages.

Maloperation or failure of the breakers TB, AB2 and spark *Gap 1* results in different overvoltages on the components of the voltage source circuits. Thus it can occur that a certain component has to withstand a certain overvoltage during a certain maloperation but there is no overvoltage when another maloperation occurs.

Four possible failures in the operation of the EPIC circuit are:

1. The TB fails to clear

A reignition or a restrike of the TB cannot be avoided during actual testing. In the EPIC circuit, failure of the TB results in an excessive current for the second current loop and an overvoltage on the AB2 as shown in Figure 6.11. When the TB fails, the spark *Gap 1* is not triggered because there is no triggering signal sent out by the current zero crossing event of TRV branch $R_1 - C_1$. The precharged capacitor C_h in the second voltage circuit remains charged. No overvoltage stresses the components in the voltage source circuits.

Figure 6.11 Current and recovery voltage on AB2 under TB fails to clear

2. Maloperation of the AB2

Maloperation of AB2 can occur in two ways. First when AB2 clears simultaneously with the TB (indicated fault 1 in Figure 6.12) and second when AB2 fails to clear with a reignition after its current zero (indicated fault 2 in Figure 6.12). These two maloperations produce an overvoltage on TRV capacitor C_i which is dependent on the rated breaking current of test circuit (Table 6.3). A lower breaking current test circuit results in a higher overvoltage factor because of the low damping factor of the circuit.

Figure 6.12 TB recovery voltage with the AB2 maloperations

Table 6.3 Voltage on capacitor C_f in kilovolts at normal working condition and the maximum overvoltage when AB2 fails to clear

	63 kA	50 kA	40 kA
Initial charging voltage	790.0	730.0	710.0
Working voltage	790.0	765.0	767.5
Max. voltage on fault 1	790.0	761.0	757.5
Max. voltage on fault 2	790.0	773.0	776.0

As a reference, the normal TRV across the TB is also plotted in Figure 6.12. There is no recovery voltage across the TB when AB2 and TB clear simultaneously. In that case the test is invalid. In the case that AB2 fails to clear at the prospective current zero but clears at the next current zero, the correct recovery voltage appears across the TB during the first part of the TRV as shown in Figure 6.12. The thermal behavior of the TB has been tested. In both cases the AB2 must withstand a higher voltage stress (dU/dt and peak value) after current interruption as shown in Figure 6.13.

Figure 6.13 Current and recovery voltage on AB2 under maloperation of AB2

3. Incorrect triggering of spark Gap 1

As described in section 3.3.3, spark Gap 1 is fired almost at the peak of the TRV branch current I_{11} . The dI_{11}/dt of this current is used to control the instant of injection of the second (I_2) voltage circuit. The strong electric and magnetic fields in the high power laboratory or a non-optimal lay-out of the measuring devices could cause such an incorrect triggering of spark Gap 1. From experience we know that triggering problems generally occur when switching takes place. They occur at the AB2 triggering instant and the TB clear instant. Incorrect triggering of AB2 by an earlier switching operation in the synthetic test circuit by, for instance, the making switch will not result in higher harmful overvoltages than the incorrect triggering of spark Gap 1 at AB2 triggering instant.

The incorrect triggering of spark Gap 1 at AB2 triggering instant (instant of the second voltage injection) influences the injection current waveform and the recovery voltage waveform. This can be seen in Figure 6.14. As a reference, the correct injected current waveform and recovery voltage waveform are also plotted in Figure 6.14. Capacitor bank C_h encounters a higher oscillating voltage because of the discharge of C_0 in the second voltage circuit. This voltage is higher than the initial precharged voltage on the C_h as can be seen in Figure 6.15.

Figure 6.14 Uncorrected triggering of Gap 1 at AB2 triggering instant

Incorrect triggering of spark Gap 1 at the instant of clearing of TB influences the waveform of transient recovery voltage for the TB. This is demonstrated in Figure 6.16. Although the TRV peak is in that case lower than the specified value, this will not

influence the thermal behavior of the TB.

Figure 6.15 The overvoltage on capacitor C_{11} as a result of uncorrected triggering of Gap 1 at AB2 triggering instant

When such an incorrect triggering occurs, the second voltage circuit can produce a high amplitude oscillation. The oscillating voltage appearing on capacitor bank C_h exceeds the initial charging voltage and the normal working voltage is calculated in Table 6.4.

Figure 6.16 Incorrect triggering of Gap 1 when the TB clears the short circuit current

Table 6.4 Voltage in kilovolts on capacitor C_h under normal working condition and when incorrect triggering of spark *Gap 1* occurs when TB clears

	63 kA	50 kA	40 kA
Initial charging voltage	618.0	571.0	541.0
Working voltage	624.0	575.0	545.0
Max. overvoltage	639.0	587.0	555.0

4. Spark *Gap 1* fails to trigger

A non-fired spark *Gap 1* lets the circuit produce an uncompleted TRV as can be seen from Figure 6.17. No overvoltage is produced during such a maloperation. The thermal interrupting interval of the TB has been verified but nothing can be concluded about the interrupting capability of the TB.

Figure 6.17 Recovery voltage across the TB when spark *Gap 1* fails to trigger

6.4 Conclusion

The configuration of the EPIC circuit does not require a large value for inductor L_i and capacitor C_o in the current injection part of the circuit. This makes it possible to increase the current injection frequency for the ultra-high-voltage test circuit. The current

injection frequency in the EPIC circuit is around 400Hz for a rated test voltage of 765kV.

The damping circuit is divided into two parts so it produces two different oscillating voltage waveforms. The impedance ratio of these two damping branches determines the stress on the AB2. An optimal ratio is 1:3 (i.e. the impedance of branch $R_{22} - C_{22} - C_{2l}$ is three times the impedance of branch $R_l - C_l$). It was found that different ratios $C_{22} : C_{2l}$ influence both the working condition of spark *Gap 1* and the capacitive energy necessary in the second voltage circuit. An optimum for $C_{22} : C_{2l}$ lies between 1:2 to 1:3. A 1:3 ratio is used for further investigation of the EPIC circuit.

The second voltage slope is sensitive to spread in the triggering instant of spark *Gap 1*. An early triggering of spark *Gap 1* will decrease the value of the TRV peak and shorten the peak time. A delayed triggering of spark *Gap 1* increases the value of the TRV peak and increases the peak time.

Other parameters have hardly any influence on the correct operation of the EPIC circuit. The parasitic capacitance and inductance in the EPIC circuit do not change the TRV waveform significantly because of the presence of the large time delay capacitor C_c directly connected to the terminals of the TB.

The protection for overvoltages in the current source circuit is similar to that used in the Weil-Dobke parallel current injection circuit. The protection techniques used on the classical parallel current injection circuit can therefore be used in the EPIC circuit for the protection of the current source circuit. No special protection is required for the circuit elements in the high-voltage circuits. The calculated maximum voltage appearing on each capacitor bank due to the maloperations is:

- the initial charging voltage for capacitor C_0 .
- about 5% higher than the initial charging voltage for capacitor C_h .
- about 5% higher than the normal working voltage for capacitor bank C_l and C_{2l} .
- about 25% higher than the normal working voltage for capacitor bank C_{22} .

Chapter 7

Application, Comparison and Realization

7.1 Introduction

As the last protective equipment in the network, circuit breakers must be able to disconnect a fault under all circumstances. To be able to verify the circuit breakers performance for fault interruption in the network, several different test duties are described in the IEC-56 standard. The test duty 4 and short line fault (SLF) test duties are considered to be the most severe test duties employed to test the thermal interrupting capability. Test duty 3 is also very important for some types of circuit breakers. A test circuit arrangement or test method in the laboratory must be able to cover these test duties.

The parameter range for a test circuit must cover the test duties described by the IEC standards, also for the different voltage ratings. A test circuit that covers a wide range of testing voltage is important for its use in the high power laboratory.

During the last twenty years, in order to catch up with the development of high-voltage circuit breakers in both their current interrupting capability and voltage rating for a single interrupting element, several synthetic test circuits have been developed [30] [31] [32] [33] [41]. At the 765kV ultra-high-voltage level, apart from the EPIC synthetic test circuit presented in this thesis, the three-circuit synthetic test circuit, the

four-parameter synthetic test circuit developed by Hitachi and the voltage injection synthetic test circuit have the potential to be used as laboratory test circuits to verify the interrupting performance of the ultra-high-voltage circuit breakers. From these test circuits, the Hitachi four-parameter circuit (Figure 2.26) and the series voltage injection circuit (Figure 2.16) are attractive because of the simple circuit lay-out and minimal use of auxiliary equipment. Since synthetic tests are not exactly equivalent to full-scale field tests, different synthetic test circuits give different equivalences than field tests or those attained from a direct test circuit. An improved equivalence of the synthetic test method and test circuit is the requirement that has to be fulfilled. Besides the equivalence, the necessary capacitive energy and ease of operation of the synthetic test circuit must also be considered.

The application of the EPIC circuit arrangement for test duty 3, the SLF test duty and test duty 4 for a half-pole test of a 765kV-63kA rating breaker are first studied in this chapter. The applicability of the EPIC circuit arrangement for voltages above 765kV is discussed later. The circuit parameters and corresponding prospective TRV waveforms for these circuits are presented. In the second part of this chapter, the superiority of the EPIC circuit is demonstrated by a comparison study of the EPIC synthetic test circuit and the other two ultra-high-voltage synthetic test circuits with respect to equivalence, operation, necessary capacitive energy and applicability. A reference direct test circuit is used which is dimensioned such that all the power is supplied from one source. The KEMA-improved Mayr arc model is used to represent the circuit breaker in the network calculations.

7.2 Application Study of the EPIC Circuit

7.2.1 The SLF test

The most severe high-current breaking test to be performed on power circuit breakers is to clear not a breaker terminal fault at 100% short-circuit current but a short line fault which may occur a few hundred meters downstream and have an associated current that is a few percent lower than a breaker terminal fault because of the added line inductance. However, circuit breakers in the process of interruption at current zero are stressed by the product of the prior rate of decay of the current (di/dt) and the following rate-of-rise of the recovery voltage (dU/dt), of which the latter may be ten times greater for SLF than for a breaker terminal fault.

This very severe dU/dt of the SLF is due to the discharge of a short line producing

a triangular wave rather than a simple harmonic $(1 - \cos)$ wave found in the breaker terminal fault TRV. To take account of this important aspect, both IEC and ANSI have produced standards that specify the requirement for the TRV produced during SLF tests. These requirements have become more exacting with the advent of SF_6 circuit breakers, which are sensitive to a time delay of less than $1\mu s$ in the TRV [40].

Figure 7.1 The EPIC circuit for an SLF test

Like the original Weil circuit, the EPIC circuit structure can easily cope with the artificial line [39] [40] in the main circuit without limitation (Figure 7.1). The SLF test duties for 90% of the rated short-circuit breaking current (90% SLF) and for 75% of the rated short-circuit breaking current (75% SLF) calculated for a 765kV-63kA-50Hz breaker rating have the parameters given (in appendix) in tables: Table A.1 for the source circuit, Table A.2 for the current injection parameters and Table A.3 for the artificial line parameters. The circuit and parameters produce TRV waveforms as shown in Figure 7.2 for the TRV and in Figure 7.3 for the initial part of the transient recovery voltage.

Because of the presence of the artificial line in the EPIC circuit, the injected current is no longer the sum of the sinusoidal current and the exponential current. The exponential current changes into a damped oscillating current. The sinusoidal current is also influenced by the TRV branch currents because the line side short-circuit voltage drop affects the voltage in the TRV branches during the short-circuit interval. The injected current I_i is I_l minus the currents I_c , I_{11} and I_{22} . The oscillating current between the artificial line elements and the current I_c through the time delay capacitor C_c are so small that they can be neglected in calculating the I_{11} , I_{22} and I_l from equation 7.1.

Figure 7.2 TRV of SLF test circuits

Figure 7.3 Initial part of the TRV of the SLF test circuits

$$\begin{aligned}
 (L_1 + L_t) \frac{dI_1^2}{dt^2} + \frac{I_1}{C_0} - L_t \frac{dI_1 dI_{11}}{dt^2} - L_t \frac{dI_1 dI_{22}}{dt^2} &= 0 \\
 L_t \frac{dI_{11}^2}{dt^2} + L_t \frac{dI_{11} dI_{22}}{dt^2} - L_t \frac{dI_{11} dI_1}{dt^2} + R_1 \frac{dI_{11}}{dt} + \frac{I_{11}}{C_1} &= 0 \quad (7.1) \\
 L_t \frac{dI_{22}^2}{dt^2} + L_t \frac{dI_{22} dI_{11}}{dt^2} - L_t \frac{dI_{22} dI_1}{dt^2} + R_{22} \frac{dI_{22}}{dt} + \frac{(C_{21} + C_{22}) I_{22}}{C_{21} C_{22}} &= 0
 \end{aligned}$$

The differential equation 7.1 can be solved numerically. The injected current in the EPIC circuit is calculated from equation 7.2 and is plotted in Figure 7.4 and in Figure 7.5 for the 75% SLF circuit and in Figure 7.6 and in Figure 7.7 for the 90% SLF circuit. The corresponding reference injected current (with an uncharged C_f) is plotted in these figures as comparison.

$$I_t = I_1 - I_{11} - I_{22} \quad (7.2)$$

Figure 7.4 Injected current in the 75% SLF circuit

Figure 7.5 The slope of the injected current in the 75% SLF circuit just before current zero

As can be seen in Figure 7.4 and in Figure 7.6 the precharged capacitor C_i in the EPIC circuit transfers a part of its energy to the artificial line inductance L_i and this results in a slightly higher injected current. Most of the energy transfer is completed in the first half of the injected current loop. For the 90% SLF test duty the increase in di/dt at current zero is no more than 5% (Figure 7.7), and for the 75% SLF test duty the increase in di/dt at current zero is no more than 10% (Figure 7.5). The values are within the tolerance range allowed by the standard. It can be concluded that from the analyses and calculations the precharged C_i hardly influences the initial part of the dU/dt of the SLF test circuit.

Figure 7.6 Injected current in the 90% SLF circuit

Figure 7.7 The slope of the injected current in the 90% SLF circuit just before current zero

For the EPIC circuit for the SLF test duty (for both 75% SLF and 90% SLF) a minimum capacitive energy is necessary as calculated in Table 7.1.

Table 7.1 Capacitive energy necessary in the EPIC circuit for the SLF test duty for a 765kV-63kA-50Hz breaker rating

Element	C_0	C_h	C_l	C_{2l}	C_{22}	Total
Energy (MJ)	1.08	.43	.37	.37	.07	2.32

7.2.2 Half-pole testing of test duty 4

When a testing laboratory is not equipped to test a complete three-pole circuit breaker or a complete single-pole of a circuit breaker, the IEC-56 standard permits tests on one or more units when a breaker pole consists of more than one interrupting units. This clause specifies that the following conditions are fulfilled for the test breakers:

1. The opening, in breaking tests, or the closing, in making tests, of the contacts of one pole shall be such that the time interval between the opening or closing of the contacts of the unit which is first to operate and the contacts of the unit which is last to operate is not more than 1/8 cycle of rated frequency.
2. For a circuit breaker using a supply of arc-extinguishing medium from a source external to the units, the supply to each unit shall for all practical purposes be independent of the supply to the other units, and the arrangement of the supply pipes shall be such as to ensure that all units are fed essentially together and in an identical manner.
3. The design of the circuit breaker and its units shall be such that during the breaking or making operations, the condition of the medium in which the arc is created (e.g. temperature, pressure, rate of flow, etc.) in each unit is for all practical purposes not influenced by the operation of the other units.
In particular, neither the supply of extinguishing medium to the unit or units under test nor the ease of exhaust of products from the arc shall be increased owing to the absence of arcing in the other units normally in series with the unit or units under test.

At present, the minimum number of interrupting units of circuit breakers with a

voltage rating of 765kV is two breaks in each pole [8]. The minimum testing unit for this circuit breaker rating is a half-pole test. For other circuit breakers consisting of more than two units per pole, half-pole testing is also recommended for the unit testing because according to the IEC " *All unit testing shall be performed on the maximum number of units in series compatible with the capability of the testing laboratory, at the specified making and breaking currents* ".

For a half-pole test, and when the voltage distribution factor is not taken into account, the recovery voltage on the half-pole unit(s) is half of the rated TRV. The dU/dt applied on the half-pole unit(s) is also half the rated dU/dt ($2kV/\mu s$). To produce half the rated dU/dt the voltage oscillation in the $R-L-C$ in circuit Figure 6.2, the capacitance value C_0 and C_Σ must be increased about four times. Because the principle limitation of the Weil circuit and the capacity limitation of the test laboratories, sometimes a higher dU/dt has to be chosen in order to perform unit testing in the Weil circuit. This method, however, overstresses the testing unit(s) and is therefore hardly accepted by the manufacturers.

Figure 7.8 The prospective TRV of the half-pole test circuit

Although the capacitance value C_0 and C_Σ have to be increased about four times in the EPIC circuit too for the half-pole test, the original low value for C_0 and C_Σ have as a result that the total necessary capacitive energy is not more than 1.9MJ as calculated in Table 7.2. The parameters of the EPIC circuit for half-pole testing of 765kV-63kA-50Hz circuit breakers are given in appendix Table A.1. A 1.05 voltage distribution (grading) factor for the half-pole test is assumed. The prospective TRV of this circuit is

plotted in Figure 7.8. The working conditions for both the AB2 and the spark Gap 1 ease with the testing voltage as calculated in the appendix in Table A.4.

Table 7.2 The necessary capacitive energy in the EPIC circuit for a half-pole duty 4 test for a 765kV-63kA-50Hz breaker rating

Element	C_o	C_h	C_l	C_{2l}	C_{22}	Total
Energy (MJ)	.65	.34	.48	.33	.06	1.86

7.2.3 Test duty 3

Since the two slopes of the TRV are realized by two voltage oscillation circuits, it is easy to adjust the voltage oscillation frequencies in each circuit separately according to the difference in dU/dt requirements. For test duty 3, the first slope of the TRV is specified with a dU/dt of $3.0\text{kV}/\mu\text{s}$ by the IEC standard. The EPIC circuit for test duty 3 has a parameter combination given in appendix Table A.1. The injection parameters of this circuit are given in the appendix in Table A.2. With these parameters the EPIC circuit for the duty 3 has a prospective TRV as shown in Figure 7.9 and has a necessary capacitive energy as shown in Table 7.3.

Figure 7.9 Prospective TRV of test duty 3 of the EPIC circuit

Table 7.3 Capacitive energy necessary in the new circuit for test duty 3 for a 765kV-63kA-50Hz breaker rating

Element	C_0	C_h	C_l	C_{2l}	C_{22}	Total
Energy (MJ)	1.02	.47	.17	.24	.07	1.97

7.2.4 Testing for circuit breakers with a rated voltage over 765kV

From the working principle of the EPIC circuit, it can be understood that the current injection frequency of the EPIC circuit is inversely proportional to the test voltage. Regardless of the capacitive energy necessary, there is an upper test voltage limit to the EPIC circuit because of the lowest injection current frequency specification of the IEC standard.

The 1150kV is assumed as the next system voltage rating. Since there are no IEC TRV parameters available for this voltage rating, the IEC parameters for 765kV are used to extrapolate the TRV parameters for 1150KV. With this assumption, the requirements for the EPIC synthetic test circuit with parameters for the 1150kV-63kA-50Hz duty 4 full pole test are calculated in the appendix in Table A.1.

The circuit has a current injection frequency of 300Hz and a prospective TRV waveform as shown in Figure 7.10. The capacitive energy necessary for this circuit is 7.90MJ.

Figure 7.10 The prospective TRV of the EPIC circuit for a breaker rating of 1150kV-63kA-50Hz

7.3 Comparison of Three Ultra-High-Voltage Test Circuits

7.3.1 Compared circuits and their parameters

Three synthetic test circuits for 765kV-63kA-50Hz circuit breakers test duty 4 are compared in this section. The topologies of these circuits are depicted in Figure 2.26 for the Hitachi circuit, in Figure 2.16 for the series voltage injection circuit and Figure 3.1 for the EPIC circuit. For purpose of comparison, a fictive direct circuit (Figure 2.2) is used. The parameters of this fictive direct test circuit are dimensioned such that all the power is supplied from one source. The circuit parameters of these test circuits are calculated in Table 7.4 and the circuits produce the IEC four-parameter prospective TRV waveforms as can be seen in Figure 7.11. The initial parts of the recovery voltages for these circuits are plotted in Figure 7.12. The calculated rates of rise of recovery voltages in the various test circuits are given in Table 7.5. The dotted lines in Figure 7.11 and in Figure 7.12 are the IEC four-parameter reference lines. The parameter selection of the Hitachi circuit is based on Table 3 in reference [31].

Table 7.4 Parameters for the different test circuits for
765kV-63kA-50Hz circuit breaker rating for
a duty 4 full pole test

Parameter	Direct circuit	EPIC circuit	Hitachi circuit	Voltage inj. circuit
C_0 (μF)	**	5.5	6.0	3.6
L_1 (mH)	29.0	28.2	29.0	180.0
C_1 (μF)	2.0	1.96	4.80	0.35
R_1 (Ω)	72.0	96.0	85.8	450.0
C_{22} (μF)	1.30	0.87	0.055	0.47
R_{22} (Ω)	15.0	288.0	42.9	350.0
L_{22} (mH)	54.0	**	**	160.0
C_{21} (μF)	**	2.61	0.45	**
C_h (μF)	**	3.50	6.17	**
L_h (mH)	**	67.5	178.0	**
R_h (Ω)	**	**	81.2	**

A $2.0\mu\text{s}$ time delay for the TRV is taken into account when selecting the parameter combinations in Table 7.1 according to the IEC-56 standard. To meet the time delay requirement, a value of 21.0nF is chosen for the parallel connected capacitor across the TB for the direct circuit and the EPIC circuit. To ease the working conditions of the AB2 in the EPIC circuit, the same value (21.0nF) of the delay capacitor is also connected parallel to the AB2. No delay capacitor is connected in the Hitachi circuit because the TRV circuit itself has a time delay of about $2.0\mu\text{s}$ in producing the TRV. However, a 0.1nF stray capacitance between the two terminals of the TB has been taken into account in the calculations. A 15.0nF delay capacitance for the TB is chosen in the voltage injection circuit. The parallel connected capacitor of the auxiliary breaker (AB) in the voltage injection synthetic test circuit is $0.1\mu\text{F}$. The instant that the voltage injection takes place is $20\mu\text{s}$ after current zero. The driving voltage of the current source is $50.0\text{kV}_{\text{rms}}$ for the three synthetic test circuits. A right surge impedance (72Ω) and initial dU/dt ($2\text{kV}/\mu\text{s}$) are followed in the selection of the current source circuit parameters in the voltage injection synthetic test circuit.

Table 7.5 Prospective dU/dt in different test circuits ($\text{kV}/\mu\text{s}$)

	Direct circuit	EPIC circuit	Hitachi circuit	Voltage inj. circuit
Maximum dU/dt	2.21	2.20	2.36	2.00

Figure 7.11 The prospective TRV in the various test circuits

Figure 7.12 The initial part of the prospective TRV in the various test circuits

7.3.2 General analysis of the circuits

The three synthetic test circuits have the same breaking current during the high current period. All the three circuits require an auxiliary breaker (AB) during the interaction interval. However, a triggering gap for the main capacitor bank C_0 is not necessary in the EPIC circuit as can be seen in Figure 3.1. The EPIC circuit resembles the Weil circuit better than the Hitachi circuit does. For the voltage injection circuit, the AB and TB interrupt the short-circuit current simultaneously. The circuit parameters of the voltage injection circuit during the current zero period deviate from the parameters of the direct circuit significantly. Both the EPIC circuit and the Hitachi circuit can operate with an inductance similar to the one in a direct test circuit. In the voltage injection circuit the same high current flows through the TB and AB. There is also a relatively large coupling capacitor present across the AB to combine the TRV from the supply circuit and the injection circuit. This makes it necessary for the AB to have a very good interrupting performance. The auxiliary breaker (AB2) in the Hitachi circuit and the EPIC circuit sees only the injection current.

The injected current waveforms of the EPIC circuit and of the Hitachi circuit are plotted in Figure 7.13 (A) and Figure 7.13 (B). The injection frequencies corresponding to these two circuits are calculated in Table 7.6.

The three circuits have more or less the same prospective TRV waveform as can be seen in Figure 7.11 and Figure 7.12.

Table 7.6 Injection current frequencies of the Hitachi circuit and the EPIC circuit

Circuit	Hitachi circuit	EPIC circuit
Frequency (Hz)	382	404

Figure 7.13 Breaking current near the zero instant in the synthetic test circuits

7.3.3 The required capacitive energy

The total necessary capacitive energy in a synthetic test circuit is an important economic factor for a test laboratory when it wants to realize the synthetic test circuit in practice. From the economical point of view, synthetic test circuits are used instead of the direct test circuit. Capacitors are a costly investment to make in synthetic test circuits. This is one of the reasons why the balanced synthetic test circuit [32] is not as economical as a choice as the synthetic test circuit for ultra-high-voltage circuit breakers. The maximum voltage appearing on each capacitor bank after maloperation or a restrike of the TB or the AB during an actual test is a guideline to calculate the minimum capacitive energy that is required for the EPIC circuit. The necessary capacitive energy

for each test circuit is given in Table 7.7.

Table 7.7 Minimum capacitive energy requirement
for various test circuits (MJ)

Test Circuit	EPIC circuit	Hitachi circuit	Voltage inj. injection
C_o	1.72	1.96	1.75
C_h	0.72	0.30	**
C_l	0.61	0.41	0.17
C_{2l}	0.67	0.05	**
C_{22}	0.13	0.02	0.44
Total	3.85	2.74	2.36

The necessary capacitive energy in the three circuits is low compared with the value of about 14.0MJ which would have been used in the conventional Weil circuit when the current injection frequency limit is left out of consideration. Comparing the three circuits, we can find the voltage injection synthetic test circuit requires the lowest capacitive energy. The required capacitive energy for the Hitachi synthetic test circuit is 2.74MJ. Compared with the voltage injection test circuit, there are two additional capacitor banks necessary in this circuit with a minimum capacitive energy of 0.30MJ each. The capacitive energy necessary for the EPIC synthetic test circuit is 3.85MJ. Three additional capacitor banks are necessary for this circuit with a minimum capacitive energy of 0.61MJ each. Two of the capacitor banks must be precharged, so charging equipment is necessary.

It should be noted that the total capacitive energy which is necessary for each circuit is closely related with the prospective value of the dU/dt for this circuit. A lower dU/dt always results in a higher capacitive energy. The parameter selection for the Hitachi circuit brings the dU/dt over the upper tolerance limit of 2.2kV/ μ s as can be seen in Table 7.5.

7.3.4 Equivalence study

Without a good equivalence with the direct test circuit, the synthetic test circuit is not applicable. As analyzed in the preceding sections, the voltage injection synthetic

test circuit over-stresses the TB during the thermal interaction interval. The current injecting circuits distort the power frequency short-circuit current and give less stress on the TB if the arc-circuit interaction is not taken into account in the charging voltage on C_0 .

Although all the three synthetic test circuits have the identical prospective short-circuit current and similar TRV waveforms (Figure 7.11 and Figure 7.12), the arc-circuit interaction is different for the three circuits. An arc model is used to study the equivalence of these circuits.

The arc model parameters for the TB and the AB2 are given in Table 5.1. The AB2 in the Hitachi circuit is assumed to have the same arc model parameters as the AB2 in the EPIC circuit because they have similar interrupting requirements. Arc voltage between the gap electrodes in the Hitachi circuit is not considered. Ideal switch model is assumed for this trigger gap.

The strong arc-circuit interaction can be demonstrated best by comparison of the prospective initial part of the TRV Figure 7.14 and of the calculated initial part of the TRV Figure 7.15 with the arc-circuit interaction on the implantation of an arc model in the circuits. The arc-circuit interaction affects the initial part of the TRV in a different way. The varying arc-channel resistance of the test breaker (Figure 7.16) and the interrupted currents and post-arc currents (Figure 7.17) are the result of arc-circuit interaction.

Figure 7.14 The prospective initial part of the TRV across the TB for the various test circuits

It can be calculated from Figure 7.16 and Figure 7.17 that the voltage injection circuit gives the most severe stress on the TB because of the highest di/dt before current zero and the highest post-arc current. The Hitachi circuit gives the lowest stress on the TB because of the lowest di/dt before current zero and the smallest post-arc current. The EPIC circuit results in a di/dt and a post-arc current very close to the values in the direct test circuit.

Figure 7.15 The initial part of the TRV across the TB for the various test circuits

Figure 7.16 Arc channel resistance for the different test circuits around current zero

For a better understanding of the different stresses produced by each circuit, one can calculate the value of the arc-channel resistance of the TB at current zero instant (R_0) for the various circuits because this reflects the test circuit stress on the TB before current zero.

A higher value of R_0 of the TB represents less stress. For the various synthetic test circuits, a value of R_0 close to the value of R_0 in the direct test circuit resembles a better equivalence of the circuit in the interaction interval before current zero.

Figure 7.17 The current at the current zero period for the various test circuits

Table 7.8 Arc channel resistance at instant of current zero

Circuit	R_0 ($k\Omega$)
Direct	1.46
EPIC	1.77
Hitachi	1.97
Voltage inj.	0.95

The arc-circuit interaction takes place not only before current zero but also for a short period after current zero because of the presence of post-arc current in the circuit breakers. The minimum clearing pressure, necessary for the TB in each circuit to clear,

represents the influence of the arc-circuit interaction before and after current zero. By adjusting the gas pressure parameter of the KEMA arc model the minimum gas pressure necessary for the TB to clear is found. The calculated values of the gas pressure for each circuit are shown in Table 7.9.

Both the arc channel resistance shown in Table 7.8 and the minimum gas pressure shown in Table 7.9 give the same results: 1. the voltage injection synthetic test circuit over-stresses the TB significantly: the difference in clearing pressure is +23% compared with the direct test circuit. 2. the Hitachi synthetic test circuit puts less stress on the TB: the difference in clearing pressure is -12%. 3. the EPIC synthetic test circuit stresses the TB in a comparable manner as the direct test circuit: the difference in clearing pressure is -1%.

Table 7.9 The minimum pressure necessary for the TB to clear without a thermal reignition

Circuit	P (bar)
Direct	5.00
EPIC	4.95
Hitachi	4.40
Voltage inj.	6.15

7.3.5 Circuit application and operation

Apart from the bad equivalence, the voltage injection circuit introduces another problem when it is applied for an SLF test duty. The insertion of an artificial line in the current source circuit requires a very high driving voltage even when the value of the arc voltages in both the AB and the TB are modest. For the 90% SLF test duty and 75% SLF test duty of a circuit breaker with a rating of 765kV-63kA, the voltage drop across the artificial line is 44kV and 110kV respectively. Such a voltage drop on the artificial line requires a higher current source driving voltage in the voltage injection circuit. However, the maximum driving voltage for the test laboratory is limited by its installation.

The introduction of AB2 in the Hitachi synthetic test circuit and in the EPIC

synthetic test circuit affects the operational reliability of the test circuit. The reliable operation of AB2 is very important. An easy working condition for AB2 eases the design of AB2 and increase the reliability of the test.

There are two significant differences in the operating conditions for the Hitachi circuit and for the EPIC circuit. One is the working condition of AB2 and the other one is the working condition of the spark gap used in the voltage circuit. In the EPIC circuit, AB2 serves as a spark gap as well to separate the current source. No spark gap is needed in the current injection circuit. The precharged voltage on the main capacitor bank is supplied to AB2 and makes it easier for AB2 to trigger. In contrast to this, AB2 in the Hitachi circuit has no voltage across its contacts at the instant of triggering. Another triggering gap is required for separating the precharged capacitor bank from the current source TRV circuit. A withstand voltage of 812kV and a $11.6\text{kA}_{\text{peak}}$ short-circuit current are required for the triggering gap in the Hitachi circuit, and this makes it certainly difficult to design and operate for ultra-high-voltage. Apart from this, a problem of the triggering of AB2 still remains because of the zero voltage across the contact gap at the triggering instant. Although also a spark gap is used in the EPIC circuit, the working conditions for the spark gap have been greatly improved with a requirement of the withstand voltage of 620kV and a maximum attainable short-circuit current of $3.1\text{kA}_{\text{peak}}$, because this spark gap is only used in the second voltage injection part. However, the three precharged capacitor banks in the EPIC circuit arrangement require more hardware investment in the test laboratory.

7.4 Realization of the EPIC Circuit in Laboratory

The experimental tests with the EPIC circuit are limited because of the presently unavailable 765kV auxiliary circuit breaker. This auxiliary circuit breaker has a triggering function as discussed in 3.3.2. A lower voltage (362kV) design of this type auxiliary circuit breaker has been reported to be in use by Hitachi [30] [31]. The specification requirements of this auxiliary circuit breaker in the 765kV-63kA EPIC circuit are given in 3.3.2.

To realize the EPIC circuit in the high power laboratory, some adjustments are necessary on the conventional parallel current injection synthetic test circuit. The number of independent high power capacitor banks increases to four. Each bank has a capacitive energy necessary as calculated in 3.3.1. Because three capacitor banks are precharged at two different voltage levels and polarities, the charging system of laboratory should be improved too. If an 10% charging voltage rise is used to compensate the voltage decrease

of capacitor banks at the injection current zero due to the energy dissipation of arc voltages, the charging equipment should have an 870kV voltage output in the EPIC circuit.

There are no special requirements for controlling system, measurement system and overvoltage protection system.

A detail analysis about the operation of the EPIC circuit is given in Chapter 6 of this dissertation.

7.5 Conclusion

The EPIC circuit can meet the most severe test duties as stipulated by the IEC standards. When the EPIC circuit is designed to perform test duty 3 or the SLF test duty, the necessary capacitive energy and the working conditions of test circuit are relatively less and easy compared with the duty 4 test. Regardless of the necessary capacitive energy (about 7.9MJ) the EPIC circuit can be used to perform the duty 4 test of circuit breakers with a rated voltage 1150kV using an injection frequency of 299Hz.

The equivalence of the EPIC circuit, the Hitachi circuit and the voltage injection circuit is demonstrated with the use of an arc model that simulates the interaction behavior of both test breaker and auxiliary breakers in the test circuits. The EPIC synthetic test circuit gives the best equivalence with the direct test circuit. The voltage injection synthetic test circuit significantly overstresses the TB, and the Hitachi four-parameter synthetic test circuit significantly understresses the TB during the thermal interaction interval. When the gas pressure is used to judge the circuit stress in the arc model, it was found the relative stress decrease is 1% for the EPIC circuit and 12% for the Hitachi circuit. It was found the voltage injection circuit overstresses the TB with a relative stress increase of 23%.

Calculations prove that an identical prospective breaking current and TRV do not result in the same stress for the various test circuits. The arc-circuit interaction plays an important role in the determination of circuit stress. It is recommended that the circuit breaker standards should take the arc-circuit interaction into account and give a more accurate description of the test circuits generating the transient recovery voltages.

Because of lack of the 765kV plasma injection type auxiliary circuit breaker no experimental tests can be performed at present. Analyses show some modifications to the

conventional parallel current injection test circuit are necessary in order to realize the EPIC circuit .

Chapter 8

General Conclusions

During the past few decades experience has been gained with synthetic testing techniques and methods. It has been proven that synthetic testing is an economical and technically correct way to test high-voltage a.c. circuit breakers according to the requirements of IEC Publication 56. This is why it was decided to include synthetic testing methods, after a thorough revision of the first edition of IEC publication 427, as equivalent to the direct test methods. (introduction of IEC publication 427)

The high current phase and the interaction interval are two important periods in synthetic testing circuits, because the arc-circuit interaction may result in a significant distortion of the prospective breaking current when the circuit parameters are not properly selected. In the IEC requirements, the maximum current distortion in synthetic testing is specified as: *the amplitude of the final loop of the actual test current in a single phase circuit shall be not less than 90% of the value specified; the duration of the final loop of the actual power-frequency test circuit shall be not less than 90% of the loop duration given by the rated frequency after taking into account, where this is appropriate, the effect of the specified d.c. component.*

The ratio between the driving voltage of the current source and the sum of arc voltages in the AB and the TB determines whether the synthetic testing circuits satisfy the IEC standard. In correspondence with the above requirements, the minimum driving voltage of the current source circuit in synthetic test circuits should be at least :

1. 3.5 times the sum of the arc voltages in AB1 and TB for a linear rising arc

voltage waveform,

2. 7.7 times the sum of the arc voltages in AB1 and TB for a trapezoidal arc voltage waveform and,
3. 12 times the sum of the arc voltages in AB1 and TB for a constant arc voltage waveform.

The stress on the breaker in the interaction interval cannot be analyzed simply by looking at the circuit structure and its parameters, because of the non-linear behavior of resistance in the arc channel. Only by using an appropriate arc model which takes the arc-circuit interaction into account can the stress on the breaker be simulated.

Comparability tests and calculations performed over the years have proven that the parallel current injection synthetic test circuit (Weil-Dobke circuit) gives the best equivalence with the direct test circuit. The Weil-Dobke circuit is commonly used by most of the high power laboratories in the world. But, there is for the Weil-Dobke circuit a limit to its application. The maximum voltage rating of the breakers that can be tested is 525kV.

A new ultra-high-voltage synthetic test circuit (EPIC circuit) combining a parallel current injection circuit and a voltage injection circuit is presented and studied in this thesis. Similar to the Weil-Dobke circuit, a parallel current injection circuit is used for the interaction interval in order to keep a good equivalence with a direct test circuit. To overcome the problem of insufficient recovery voltage, a voltage injection circuit is used to supply the second part of the TRV. In the EPIC circuit, the size of the main capacitor bank C_0 is determined by the first part of the TRV. The necessary capacitive energy in the parallel current injection circuit is rather low. Calculations show the total necessary capacitive energy in the new EPIC circuit is 3.85MJ for a 765kV, 63kA 50Hz breaker full pole 100% terminal fault duty 4 testing. An extra auxiliary circuit breaker is necessary in the EPIC circuit. This auxiliary breaker acts as an isolating element before it is triggered, and it clears the small oscillating current in one of the TRV branches after the test breaker clears. The spark gap used in the EPIC circuit has easier working conditions than the spark gap used in the Weil-Dobke circuit.

The validity of the EPIC circuit is studied by employing a physical arc model with parameters derived from real tests, because of laboratory limitation on performing the experimental test at present. These limitations include the on availability of the 765kV

rated voltage auxiliary circuit breaker (AB2) in the EPIC circuit, and the physical size of the voltage circuit installation in high power laboratories.

The establishment of the KEMA arc model was based on literature and tests. By using this arc model, the arc-circuit interaction and the validity of the EPIC circuit are studied. Because the parallel current injection circuit is used during the thermal interaction interval of the test breaker and the circuit parameters resemble the ones in the direct test circuit, the EPIC circuit has a good equivalence with the direct circuit. This ensures that the stress of the EPIC circuit is close to that in the direct test circuit. When the gas pressure is used to judge the circuit stress in the arc model, it was found the relative stress decrease of the EPIC circuit is only 1%.

For comparison, two other synthetic test circuits published in other literature for a 765kV-63kA-50Hz circuit breaker test duty 4 (the Hitachi four-parameter synthetic test circuit and the series voltage injection synthetic test circuit) are analyzed with respect to the necessary capacitive energy, operation and equivalence. The results show that, although the two circuits supply the identical interrupting current and the similar IEC standard specified prospective TRV, the Hitachi circuit understresses the test breaker by 12%, and the voltage injection circuit overstresses the test breaker by 23% when the gas pressure is used as the comparing parameter.

Studying the operation performance of the EPIC circuit reveals the produced overvoltages after a reignition or a restrike of the TB or AB. The consequences of mistiming or maloperation of the test sequence with respect to the current source circuit is the same as for the Weil-Dobke circuit. The same protection techniques can be used for the EPIC circuit. No notable overvoltage appears across the individual circuit elements under any circumstances.

The studies in this thesis show that similar prospective TRV waveforms generated by the different test circuits does not guarantee an equal stress from these test circuits on the test breaker.

Appendix

Circuit Parameters for SLF Test, Test Duty 3, Half-pole Test Duty 4 for a 765kV Breaker Rating and Test Duty 4 for a 1150kV Breaker Rating

Table A.1 Circuit parameters for SLF test, test duty 3, half-pole test duty 4 for circuit breakers with a rating of 765kV-63kA-50Hz and full pole test duty 4 for circuit breakers with a rating of 1150kV-63kA-50Hz

Parameter	SLF	Duty 3	Duty 4 Half-pole	Duty 4* 1150kV
C_0 (μF)	5.50	5.50	5.00	7.00
L_1 (mH)	22.3	40.0	18.0	40.5
C_h (μF)	3.50	3.00	3.50	4.00
L_h (mH)	37.0	190.0	47.0	135.0
C_1 (μF)	1.95	0.53	3.75	2.40
R_1 (Ω)	105.0	230.0	50.7	96.0
C_{22} (μF)	0.87	0.23	1.67	1.07
R_{22} (Ω)	315.0	688.0	152.0	288.0
C_{21} (μF)	2.60	0.70	5.00	3.20
C_c (nF)	1.0	10.0	15.0	21.0

With a maximum dU/dt 2.3kV/ μs

Table A.2 Injection parameters for the different circuits

Parameter	90% SLF	75% SLF	Duty 3	Duty 4 Half-pole	Duty 4* 1150kV
U_0 (kV)	625.0	625.0	672.0	504.0	1134.0
U_h (kV)	495.0	482.0	572.0	420.0	930.0
f_{inj} (Hz)	431	393	375	530	299
Z_{inj} (Ω)	67.1	73.5	94.3	60.0	76.1
I_{inj} (kA)	9.31 + .79**	8.61 + 1.03**	7.13 + .01**	8.40 + .97**	14.90 + .34**
di/dt (A/ μ s)	25.2	21.0	16.8	28.0	28.0
R_{Surge} (Ω)	80.0***	96.0***	119.0	38.0	72.0

* With a maximum dU/dt 2.3kV/ μ s** Value of the discharging current of C_1 when the injected current reaches its peak value

*** Source circuit side

Table A.3 Calculated interrupting parameters for the AB2 for the different test duties

Parameter	90% SLF	75% SLF	Duty 3	Duty 4 Half-pole	Duty 4* 1150kV
I_{max} (kA)	10.10	9.64	7.14	9.94	15.24
I_{last} (kA)	0.82	0.65	0.48	1.10	1.49
$m_3 - m_1$ (ms)	1.17	1.31	1.33	0.95	1.67
$m_5 - m_3$ (ms)	0.53	0.51	0.46	0.59	0.86
Arc time (ms)	1.70	1.82	1.79	1.54	2.53
di/dt ** (A/ μ s)	3.8	3.4	2.3	4.8	4.3
U_{peak} (kV)	513	472	666	447	1116
dU/dt *** (kV/ μ s)	1.3	1.2	1.1	0.9	1.3

* Peak current of the last injected current loop through the AB2

** From 25 μ s to current zero instant*** From current zero to 50 μ s after current zero

Table A.4 Artificial line parameters of SLF test circuit

Parameter	L_t (mH)	C_t (nF)	R_t (k Ω)	L_u (mH)	R_u (Ω)	L_v (mH)	C_v (nF)
90% SLF	2.48	4.08	5.0	0.36	450	0.18	8.16
75 % SLF	7.44	12.25	5.0	0.54	450	1.08	24.5

Figure A.1 KEMA Artificial line

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List of Symbols and Abbreviations

The following symbols are used throughout the thesis. Several symbols are defined within a specific context and have no meaning outside that context.

AB	: Auxiliary circuit breaker
AB1	: Auxiliary circuit breaker used in the current source network
AB2	: Auxiliary circuit breaker used in the voltage source network
ANSI	: American National Standards Institute
di/dt	: Rate of change of current
dU/dt	: Rate of rise of recovery voltage
Test duty 3	: 60% of the rated short-circuit breaking current test
Test duty 4	: 100% of the rated short-circuit breaking current test
f_{inj}	: Current injection frequency
I_{inj}	: Injected current
IEC	: International Electrotechnical Commission
IEC-56	: International Standard on "High-voltage alternating-current circuit-breakers" issued by International Electrotechnical Commission in 1987
IEC-427	: International Standard on "Synthetic testing of high-voltage alternating current circuit-breakers" issued by International Electrotechnical Commission in 1989
KEMA	: Testing and Research Institute of the Dutch Utilities
P	: Gas pressure in the circuit-breaker
P_0	: Cooling power at current zero of the test breaker
R_0	: Arc channel resistance at current zero instant
SLF	: Short line fault
τ	: Arc time constant

TB	: Circuit breaker under test
U_0	: Charging voltage on the first main capacitor bank C_0
U_h	: Charging voltage on the second main capacitor bank C_h
ω_0	: Natural angle frequency

Summary

The interrupting capability of SF₆ puffer circuit breakers has increased with the development of power system voltage ratings and the increase in short-circuit power. A modern single-break circuit breaker design can have a rating of 550kV-63kA. Higher voltages and currents for a single break are expected to be developed in the near future.

The verification of the interrupting performance of high voltage circuit breakers is carried out in the high power laboratory. The short-circuit capacity of a direct test circuit which uses short-circuit generators or the grid as supply is insufficient to perform even unit testing for these large voltage and current ratings. A solution that is both economical and practical is to use synthetic test methods to overcome this problem. The short-circuit generators or the grid are used to supply the short-circuit current and a separate voltage oscillation circuit with a precharged capacitor bank and an inductance is used as the source of the recovery voltage. This method has been approved and described by the IEC standards for high voltage circuit breakers. There are different kinds of synthetic test circuits, depending on the connection of the voltage circuit, the current circuit and injection moment of the voltage circuit. For all the synthetic test circuits, a minimum current source driving voltage, depending on the arc voltage waveforms in the test circuit breaker and the auxiliary circuit breaker, is required in order to keep the current distortion within the IEC specifications. Comparisons tests and calculations carried out over the years have proven that the parallel current injection synthetic test circuit (Weil-Dobke circuit) gives the best equivalence with the direct test circuit in the interaction interval, provided that the current injection frequency is between 250Hz and 1000Hz and, the circuit is injected at the right instant which is specified by the IEC standards. The Weil-Dobke circuit is today used in most laboratories.

The principle limitation of the Weil-Dobke circuit (which is that the requirements for the frequency of the TRV (f_{TRV}) and the frequency of the injected current (f_{inj}) cannot be fulfilled at the same time for testing the ultra-high-voltage circuit breakers because of their dependence on the impedance of the voltage circuit), and the fact that the capacitive energy necessary in the voltage part of the Weil-Dobke circuit is

proportional to the square of the test voltage, have as consequence that this circuit cannot be applied for voltage ratings of 765kV and above.

A new synthetic test circuit (EPIC circuit) is proposed in this thesis. The EPIC circuit can be applied for voltage ratings of 765kV and higher. The EPIC circuit is a three-circuit configuration. The first circuit consists of either generators or the grid, a current-limiting reactance, and a transformer to supply the interrupting current. The second circuit is a parallel current injection circuit consisting of a precharged capacitor bank, an inductance, control circuit, and an auxiliary circuit breaker to supply the injection current and to generate the first part of the transient recovery voltage (TRV). The third circuit is a voltage injection circuit consisting of a precharged capacitor bank, a spark gap, an inductance and a control circuit to supply the second part of the TRV. Analyses and calculations demonstrate that the EPIC circuit can be used for the IEC test duty 4, test duty 3 and SLF test duties with the four-parameter waveform as specified by the IEC standards.

The validity of the EPIC circuit has been demonstrated by using the KEMA arc model. Because a parallel current injection circuit is used, in which an identical short-circuit inductance is chosen ($L_i = L_d$) and no extra arc is introduced in the circuit configuration, during the thermal interaction interval of the test breaker, the EPIC circuit has a good equivalence with the direct circuit in this most important interval. When the gas pressure is used as the comparing parameter, the stress difference between the EPIC circuit and the direct circuit is not over 1%.

Two other possible synthetic test circuits for 765kV-63kA-50Hz circuit breakers in an IEC test duty 4 (the Hitachi four-parameter synthetic test circuit and the series voltage injection synthetic test circuit) are studied and compared with the EPIC synthetic test circuit. Calculation results show that the Hitachi circuit stresses the test breaker 12% less than the direct circuit, and the voltage injection circuit overstresses the test breaker by 23%, when the gas pressure is used as the comparing parameter.

It has been demonstrated that an identical prospective waveform in the different test circuits does not lead to identical stress across the breaker terminals, because the difference in the test circuit topologies results in different arc-circuit interaction. The surge impedance is a very important parameter for the equivalence in the thermal interaction interval.

Calculation of the circuit parameters of the EPIC circuit for a 765kV test duty 4 with short-circuit current rating of 63kA, 50kA and 40kA are reported in this thesis.

Circuit parameters for 765kV-63kA circuit breakers test duty 3, SLF test duties and test duty 4 half-pole test are also given. The applicability of the circuit for a 1150kV-63kA circuit breaker test duty 4 is studied.

Samenvatting

(Summary in Dutch)

Het afschakelvermogen van SF₆-pufferschakelaars wordt steeds groter met de alsmaar toenemende kortsluitvermogens en de hogere spanningen in de elektriciteitsvoorzieningssystemen. Een moderne vermogenschakelaar met een enkel onderbrekingsselement kan een rating hebben van 550kV-63kA. Vermogenschakelaars voor nog hogere spanningen en stromen zullen in de nabije toekomst ontwikkeld worden.

De verificatie van het afschakelvermogen van vermogenschakelaars vindt plaats in het kortsluitlaboratorium. Het kortsluitvermogen van een direct testcircuit, dat wordt geleverd door kortsluitgeneratoren of het net, is echter onvoldoende voor het beproeven van een enkel onderbrekingsselement bij deze hoge spannings- en stroomratings. Een economische en tevens praktische oplossing voor dit probleem is het toepassen van synthetische beproevingstechnieken. De kortsluitgeneratoren, of het net, leveren dan alleen de kortsluitstroom terwijl een apart spanningsoscillatiecircuit met een opgeladen condensatorbank en een inductiviteit wordt gebruikt om de transiënt wederkerende spanning te genereren. Deze methode is beschreven in het IEC-voorschrift voor vermogenschakelaars. Er zijn verschillende soorten synthetische circuits, afhankelijk van de verbinding van het spanningscircuit, het stroomcircuit en het injectiemoment van het spanningscircuit. Voor alle synthetische circuits is een minimale drijvende spanning noodzakelijk, deze varieert met de boogspanning van de beproevingsschakelaar en de hulpschakelaar, om de stroomvervorming binnen de grenzen van de IEC-voorschriften te houden. Uit de vergelijkende testen die in de afgelopen jaren zijn uitgevoerd, is gebleken dat het parallel-stroominjectie synthetische testcircuit (Weil-Dobke circuit) het best overeenkomt met het directe testcircuit in het interactie-interval; aangenomen dat de stroominjectiefrequentie tussen de 250Hz en 1000Hz ligt en dat het circuit op het juiste moment wordt geïnjecteerd, zoals gespecificeerd in de IEC standaard. Op dit moment wordt het Weil-Dobke circuit het meest toegepast in de testlaboratoria.

Zowel de principiële beperking van het Weil-Dobke circuit, namelijk dat aan de frequentie van de TRV (f_{TRV}) en van de geïnjecteerde stroom (f_{inj}), die gerelateerd zijn aan de impedantie van het spanningscircuit, voor een ultra-high-voltage circuit niet tegelijkertijd voldaan kan zijn, als het feit dat de capacitieve energie, benodigd in het spanningsdeel van het circuit, evenredig is met het kwadraat van de testspanning, heeft tot gevolg dat dit circuit niet geschikt is voor een spanningsrating van 765kV of hoger.

In dit proefschrift wordt een nieuw synthetisch testcircuit (EPIC circuit) beschreven. Het EPIC circuit kan worden toegepast voor spanningsratings van 765kV en hoger. Het EPIC circuit heeft een drie-circuit configuratie. Het eerste circuit levert de kortsluitstroom en bestaat uit generatoren of het net, een stroombeperkende reactantie en een transformator. Het tweede circuit is een parallel-stroominjectie circuit dat de injectiestroom levert en het eerste deel van de TRV genereert; het circuit bestaat uit een opgeladen condensatorbank, een inductiviteit, een regelcircuit en een hulpschakelaar. Het derde circuit is een spanningsinjectie circuit dat het tweede deel van de TRV genereert; het circuit bestaat uit een opgeladen condensatorbank, een vonkenbrug, een inductiviteit en een regelcircuit. Analyses en berekeningen tonen aan dat het EPIC circuit kan worden toegepast voor de IEC test duty 4, IEC test duty 3 en IEC SLF test duties met de vier-parameter golfvorm zoals die in de IEC-voorschriften gedefinieerd is.

De geldigheid van het EPIC circuit wordt aangetoond met behulp van het KEMA boogmodel. Omdat een parallel-stroominjectie circuit wordt toegepast gedurende het thermische interactie-interval van de beproevingsschakelaar, waarin een identieke kortsluitinductiviteit wordt gekozen ($L_f=L_d$) en geen extra boog in de circuitconfiguratie wordt geïntroduceerd, komt het EPIC circuit goed overeen met het directe testcircuit in het belangrijkste interval. Wanneer de vuldruk van de schakelaar als vergelijkingsmiddel wordt gebruikt, blijkt dat het verschil in gasdruk voor het EPIC circuit niet groter is dan 1%.

Twee andere synthetische testcircuits voor 765kV-63kA-50Hz vermogensschakelaars in een IEC test duty 4 (het Hitachi vier-parameter synthetische testcircuit en het serie-spanningsinjectie synthetische circuit) worden bestudeerd en vergeleken met het EPIC synthetische testcircuit. Berekeningen tonen aan dat, wanneer de vuldruk wederom als vergelijkingsmiddel wordt gebruikt, het Hitachi circuit de schakelaar 12% minder zwaar belast; het spanningsinjectie circuit belast de schakelaar echter 23% zwaarder.

Er wordt aangetoond dat testcircuits die een identieke inherente TRV genereren,

de vermogenschakelaar niet per definitie gelijk belasten. Een verschillende topologie van de testcircuits resulteert in een verschillende boog-circuit interactie. De karakteristieke impedantie van het TRV circuit is een erg belangrijke parameter voor de equivalentie in het thermische interactie-interval.

De circuitparameters van het EPIC circuit voor een 765kV test duty 4 met kortsluitstroomratings van 63kA, 50kA and 40kA worden in dit proefschrift berekend. De circuitparameters voor een 765kV-63kA schakelaars test duty 3, SLF test duties en test duty 4 met een halve schakelaarpool worden eveneens gegeven. De toepasbaarheid van het circuit voor een 1150kV-63kA schakelaar test duty 4 wordt bestudeerd.

内 容 摘 要

随着电力系统运行电压和容量的不断提高,对电力系统主要保护设备断路器的开断容量要求也在不断地提高。目前SF₆断路器的单断口最大开断容量已达550kV-63kA。断口电压更高、开断容量更大的断路器的开发和研究正在进行之中。

验证断路器的开断能力主要是在大容量试验室中进行,用突发短路发电机或网络进行的直接试验早已不能满足断路器直接开断试验容量要求。以短路发电机或网络为电流源,电容器振荡回路为电压源的合成试验回路是解决大容量试验室直接短路容量不足的一种较为经济合理的试验方法。此方法经多年的对比试验验证现已被国际电工委员会所采纳。取决于电压回路不同联接方式及电压回路的不同投入时刻存在有几种合成试验方法。在近二十余年进行的对比试验表明:并联电流引入回路(威尔回路)在规定的电流引入频率内具有较高的等价性。因此,此回路被大多数容量试验室所采用。

然而威尔回路的原理性限制及其电压回路电容容量随试验电压平方增长的关系使之不能应用于对超高压(765kV及以上)断路器的试验。

本文描述了一种新的合成试验方法及其回路用以解决765kV及以上断路器的短路开断试验。该方法采用的是三回路结构:第一回路为电流源回路由发电机或网络、限流电抗器、升压变压器等组成;第二回路为并联电流引入回路由主充电电容器、电抗器、调频回路的一部分及辅助开关组成;第三回路为电压引入回路由次充电电容器、点火球、电抗器及调频回路的一部分组成。分析计

算表明,该试验回路能够在较低电容容量要求下进行 765kV-63kA-50Hz 断路器试验方式 4、试验方式 3 及近区故障试验。其暂态恢复电压波形满足 IEC 标准的四参数要求。

使用 KEMA 电弧模型对新回路的等价性进行了研究。计算结果表明:由于新回路在电弧电压显著变化及弧后电流阶段采用了并联电流引入回路,并且其回路参数的选取与直接试验回路参数的一致,从而保证了新回路在此关键阶段与直接试验回路的一致性。当以断路器气体压力为临界值比较各试验回路的强度时,新回路的相对试验强度降低仅为 1%。而另外两个可能用于 765kV 断路器试验的合成试验回路(Hitachi 四参数回路和串联电压引入回路)的相对试验强度分别为降低 12% 和增高 23%。

计算表明合成试验回路固有暂态恢复电压与直接试验回路下的一致并不能保证合成试验回路具有与直接试验回路相同的强度。电弧-回路的相互影响将使得不同的试验回路具有不同的试验强度。合成试验回路参数在电弧电压显著变化及弧后电流阶段与直接试验回路的一致是至关重要的。在这些参数中冲击阻抗的影响较为显著。

本文给出了 765kV 断路器在各额定开断电流下试验方式 4 的回路参数组合并对 63kA 额定开断电流下的试验方式 3,近区故障及试验方式 4 二分之一极,1150kV 试验方式 4 试验进行了讨论并同时给出了其相应试验回路的试验参数。

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Curriculum Vitae

Baoliang SHENG was born in Hebei, China, on June 21, 1961. He graduated with a B.Sc in Electrical Engineering on a thesis entitled " Single-break 220kV-50kA SF₆ circuit-breaker interrupting chamber design " from Xi'an Jiaotong University, China, in July 1982. After his graduation he joined Xi'an High Voltage Apparatus Research Institute's High Power Laboratory (National High Voltage Apparatus Quality Supervising and Testing Center), China, as a test engineer in charge of the high power testing of high-voltage apparatus, and was involved as a research engineer in the development of a data acquisition system for the high power laboratory. He has been involved in the study of synthetic test methods and circuits for high-voltage circuit breakers since 1990. He is a member of the Chinese Society of Electrical Engineering and is active in the IEC 17 (A) (C) study group of China. In 1988, he studied and worked at the High Power Laboratories of KEMA (Testing and Research Institute of the Dutch Utilities), the Netherlands, as a visiting engineer for half a year. Since August 1992, he has been working at KEMA as a research engineer and has been working towards his Ph.D. at the Delft University of Technology, the Netherlands, in the field of high power testing of circuit breakers. His research covers arc-circuit interaction, the three-phase synthetic test circuit and the ultra-high-voltage synthetic test circuit. The main result of his research is reported in this Ph.D. thesis.

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盛宝良 1961年6月21日生于吉林省长春市。1982年7月毕业于西安交通大学电机工程系电器技术专业，获学士学位。毕业后就职于西安高压电器研究所(国家高压电器产品质量监督检测中心)大容量试验室从事高压电器产品的试验检测工作。1988年以访问学者身份到荷兰公用事业试验研究院(KEMA)进修半年从事大容量试验室数据采集系统软件开发及硬件联接工作。

1992年8月起被KEMA聘为研究人员在代尔夫特大学电力系统试验室从事电弧-电路相互影响，三相短路试验条件和765kV超高压断路器合成试验方法的研究。其主要研究成果被编写成此博士论文。