M.Sc. Thesis

An Oscillator System for a Quadrature Downconversion Auto-Correlation Ultra-Wideband (UWB) Receiver

Student: Gaurav Mishra
Supervisor: Dr. ir. Wouter A. Serdijn
An Oscillator System for a Quadrature Downconversion Auto-Correlation Ultra-Wideband (UWB) Receiver

THESIS

Submitted in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

In

Electrical Engineering (Microelectronics)

By

Gaurav Mishra
Student number: 1287834

Department of Microelectronics (ELCA)
Faculty of Electrical Engineering, Mathematics, and Computer Science
Delft University of Technology, The Netherlands
ACKNOWLEDGMENTS

I am extremely grateful and indebted to my advisor and mentor Dr. ir. Wouter A. Serdijn for granting me an opportunity to pursue research on this topic for my thesis. This work would never have been possible without his constant encouragement, support, thoughtfulness and tutelage.

I would like to express my gratitude to Prof. Dr. John R. Long and Dr. ir. G.J.M. Janssen for being a part of my thesis committee.

I am extremely indebted to Prof. Dr. John R. Long, for his guidance and helping me in completion of my studies. I am very much grateful towards Drs. E. Janssen of the Department of Electrical Engineering and Mr. J.B.A. Stals of International Office, for supporting me financially and morally during my stay at Delft University of Technology.

This work, my sojourn at TU-DELFT and all my endeavours would never have been possible without the love, encouragement and patronage of my parents and my brotherly friends Dr. ir. Akshay Visweswaran, ir. Vincent R. Bleeker and ir. Maxim A. Volkov. It is through them, that I felt to live and dream again and realize it through sheer grit and perseverance.

Above all I am thankful to RAM for bestowing me with everything I possess in life.
Abstract

The fast development of CMOS IC process technology and the opening up of high frequency bands by regulatory bodies has aided wireless communication industry with development and commercialization of long-medium and short range wireless communication applications, for example GSM, Wireless LAN, Bluetooth and UWB. Ultra Wideband (UWB) is a promising technology that covers a bandwidth from 3.1GHz to 10.6GHz, which features distinctive advantages, such as high data rate over short and medium range, low interference or co-existence with other wireless technologies and robustness towards multipath fading and possible usage in personal area network (PAN) and body area network (BAN), targeting especially health care monitoring applications. Impulse radio UWB or ir-UWB, is one of the UWB technologies, which applies transmission of short duration (pico-nano second) and carrier less pulses. Several receiver architectures [1, 2 & 3] based on the principle of correlation has been proposed, with Quadrature Downconversion Auto-Correlation Receiver (QDAcR) [3] being one of them. This thesis work builds up further on the generalized QDAcR model of [3], starting with an advanced time domain analysis of principle of Downconversion in QDAcR and exploring the dependency of QDAcR on downconverter related stochastic perturbations such as phase noise, jitter and amplitude perturbations. The use of Stationary Stochastic Process Theory, Fokker-Planck Equation and Floquet’s Theory resulted in a simplified equation, incorporating the effect of stochastic perturbations; this equation of prominence, further can be extrapolated to perturbation analysis of Zero (low) – IF receivers. A complete system modeling of QDAcR downconverter resulted in vital specifications for the QDAcR downconverter being the requirement of a 5.6 GHz quadrature voltage controlled oscillator (QVCO) with a minimum phase noise of -90dBC/Hz at 1MHz offset and with a maximum permissible phase error of 4 degrees. This relaxed nature of specifications has opened a plethora of trade-offs. The main aim being the design of low power Quadrature oscillator, a push-pull LC tank voltage controlled oscillator, consuming 1mW of power and exhibiting figure of merit of 187.1dB with a tuning range of 12.7% was designed. The Bottom Series QVCO, Parallel Coupled QVCO and Push-Pull –Polyphase QVCos were compared for their respective
advantages and disadvantages, which resulted in the selection of the Parallel Coupled QVCO, because of less power consumption and robust design. The Parallel QVCO consumes a power of 2.4mW, while having a FOM of 186.36dB. The final design includes the complete QVCO system and differential buffer (Common Source) with neutralization capacitors having ability to drive variable loads.

References:


Table of Contents

1 CHAPTER 1 .................................................................................................................. 11
  1.1 Introduction ........................................................................................................ 11
  1.2 Ultra-Wideband Communication Systems .......................................................... 13
  1.3 UWB Regulations and Ultra Wideband System’s comparison with Narrowband Communication system ................................................................. 15
  1.4 Ultra Wideband Transceiver Architectures and Challenges .............................. 19
  1.5 Thesis Objectives .............................................................................................. 22

2 CHAPTER 2 .................................................................................................................. 23
  2.1 System Level Design ........................................................................................ 23
  2.2 Quadrature Downconversion Autocorrelation Receiver .................................... 24
  2.3 Time Domain Analysis of QDAcR ................................................................. 26
  2.4 Modeling of an Oscillator in QDAcR .............................................................. 38
    2.4.1 The Phase Noise Characterization: Basics and Noise Sources .............. 39
    2.4.2 The Phase Noise Characterization: Noise Distribution in a Single Sideband Spectrum ................................................................. 44
    2.4.3 Modeling of Oscillator in time domain (Jitter and Phase Noise conversion) ................................................................. 47
  2.5 Conclusion ........................................................................................................ 52

3 CHAPTER 3 .................................................................................................................. 53
  3.1 Introduction ....................................................................................................... 53
  3.2 Designing and Simulation of the Oscillator in MATLAB .................................. 53
  3.3 Analysis of QDAcR architecture .................................................................... 56
    3.3.1 Frequency Planning in QDAcR architecture ........................................ 61
    3.3.2 The Noise Block ...................................................................................... 63
  3.4 Designing of the Quadrature Downconversion Auto Correlation Receiver (QDAcR) in MATLAB ................................................................. 64
  3.5 Conclusion ........................................................................................................ 102

Section II .......................................................................................................................... 104

4 CHAPTER 4 .................................................................................................................. 106
  4.1 Overview of Oscillator Fundamentals ............................................................... 106
  4.2 Quality Factor (Q-Factor), Impedance Transformation, Single Transistor Oscillators and Differential Oscillators ......................................................... 109
    4.2.1 Differential Topology Oscillators ......................................................... 113
  4.3 -Gm (Negative Transconductance) and LC-Tank Design Essentials ............ 114
    4.3.1 Designing of LC-Tank for Low Power and Low Phase Noise ............ 115
  4.4 LC-Tank Design .............................................................................................. 118
    4.4.1 Inductor Modeling and Characterization ........................................... 118
    4.4.2 Defining Process Related Parameters* .............................................. 120
    4.4.3 The optimized inductor design methodology ................................... 121
    4.4.4 Varactor Design Methodology .......................................................... 131
  4.5 Oscillator Design Methodology ....................................................................... 141
    4.5.1 Phase Noise in an Oscillator System ................................................. 142
    4.5.2 The Oscillator Start-up condition ...................................................... 143
    4.5.3 Methodology for Oscillator Design ................................................... 144
  4.6 Oscillator Design and Comparison .................................................................. 147
4.6.1 Comparison of Different Oscillator Designs

Layout Design Considerations

Conclusions

CHAPTER 5

Methods of Quadrature Signal Generation and Q-VCO Principle

Q-VCO Principle

Principle of Injection locking

Implementation of Q-VCO using injection locking

Methodology for Quadrature Oscillator Design

Q-VCO implementation using Complementary VCO, Poly-Phase filter and output buffers

Poly-Phase Filter Design and Implementation

The design of Output Buffer

Conclusion

CHAPTER 6

Conclusions

Future Work

References
Table of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>The block diagram of ir-UWB receiver with time domain correlation using a template [2]</td>
</tr>
<tr>
<td>1.2</td>
<td>Transmitted Reference Auto-Correlator [1]</td>
</tr>
<tr>
<td>1.3</td>
<td>The Block Diagram of ir-UWB Transceiver [2]</td>
</tr>
<tr>
<td>1.4</td>
<td>A Narrowband Sinusoidal in (a) the time domain and (b) the frequency domain</td>
</tr>
<tr>
<td>1.5</td>
<td>Gaussian Mono pulse in time and frequency domain</td>
</tr>
<tr>
<td>1.6</td>
<td>The UWB emission mask for the indoor &amp; outdoor communication</td>
</tr>
<tr>
<td>1.7</td>
<td>Distinction between the different communication techniques</td>
</tr>
<tr>
<td>1.8</td>
<td>Comparison of Data throughput and range for IEEE 802 Standards [12]</td>
</tr>
<tr>
<td>1.9</td>
<td>Coexistence of UWB signals with narrowband and wideband signals in the RF spectrum</td>
</tr>
<tr>
<td>1.10</td>
<td>Time domain Correlator Receiver architecture [2]</td>
</tr>
<tr>
<td>2.1</td>
<td>Quadrature Downconversion Auto-Correlation Receiver Architecture [19]</td>
</tr>
<tr>
<td>2.2</td>
<td>UWB Frequency Spectrum before (top) and after (below) Downconversion [20]</td>
</tr>
<tr>
<td>2.3</td>
<td>State-Space diagram of an oscillator in V-I plane</td>
</tr>
<tr>
<td>2.4</td>
<td>Change in Auto-Correlation Vs. Phase Error</td>
</tr>
<tr>
<td>2.5</td>
<td>The Power Spectrum of an Oscillator and Phase Noise power of the carrier at certain offset</td>
</tr>
<tr>
<td>2.6</td>
<td>Phase perturbation due to charge injection</td>
</tr>
<tr>
<td>2.7</td>
<td>The Single Side Band Spectrum of an Oscillator</td>
</tr>
<tr>
<td>2.8</td>
<td>The various types of Jitters present in a oscillating signal</td>
</tr>
<tr>
<td>2.9</td>
<td>The Block Diagram of LO modeled in MATLAB</td>
</tr>
<tr>
<td>3.1</td>
<td>Complete Block Diagram of Micro Noise Source with AWGN Channel</td>
</tr>
<tr>
<td>3.2</td>
<td>Phase Noise of -100dB @ an offset of 1MHz</td>
</tr>
<tr>
<td>3.3</td>
<td>Unperturbed Oscillator Output along with perturbed I/Q outputs</td>
</tr>
<tr>
<td>3.4</td>
<td>Block Diagram of QDACR [19]</td>
</tr>
<tr>
<td>3.5</td>
<td>Dual-IF Heterodyne Receiver Topology [39]</td>
</tr>
<tr>
<td>3.6</td>
<td>A Direct-Conversion Receiver</td>
</tr>
<tr>
<td>3.7</td>
<td>Showing the various interferers present</td>
</tr>
<tr>
<td>3.8</td>
<td>Modeling of Noise</td>
</tr>
<tr>
<td>3.9</td>
<td>Modeling of Noise Block in MALAB</td>
</tr>
<tr>
<td>3.10</td>
<td>QDACR Block Diagram Representation</td>
</tr>
<tr>
<td>3.11</td>
<td>The Transient levels of Gaussian Pulse</td>
</tr>
<tr>
<td>3.12</td>
<td>The PSD levels of Gaussian Pulse</td>
</tr>
<tr>
<td>3.13</td>
<td>The PSD levels at ( \sigma = 0.205e-09 )</td>
</tr>
<tr>
<td>3.14</td>
<td>Transient response of the Gaussian for ( \sigma = 0.205e-09 )</td>
</tr>
<tr>
<td>3.15</td>
<td>The PSD levels of Gaussian Mono Pulse</td>
</tr>
<tr>
<td>3.16</td>
<td>The Transient levels of Gaussian Mono Pulse</td>
</tr>
<tr>
<td>3.17</td>
<td>The PSD levels of Gaussian Doublet Pulse</td>
</tr>
<tr>
<td>3.18</td>
<td>The PSD levels of Gaussian Doublet Pulse</td>
</tr>
<tr>
<td>3.19</td>
<td>Block Diagram for the Wavelet Modeling</td>
</tr>
</tbody>
</table>
Figure 3.21: The Transient levels of Daubechie’s Wavelet ........................................ 72
Figure 3.22: The PSD levels of Daubechie’s Wavelet .............................................. 72
Figure 3.23: The PSD levels of a Morlet Wavelet Function ......................................... 73
Figure 3.24: The transient levels of a Morlet Wavelet Function ..................................... 73
Figure 3.25: The PSD Levels of a Sinc Wavelet Function ........................................... 74
Figure 3.26: The transient Levels of a Sinc Wavelet Function ................................... 75
Figure 3.27: The Block Diagram for the Implementation of the Interferers .................... 76
Figure 3.28 Matlab Noise Model Output showing the main interferers and the Thermal Noise Floor .................................................................................................................. 77
Figure 3.29: The Phase Distortion vs. Auto Correlation Graph .................................... 79
Figure 3.30: The Total Noise PSD levels for UWB (In-Band and Out-Band both) .... 81
Figure 3.31: The Total Noise PSD levels after the Filtration for UWB (In-Band and Out-Band both) .......................................................... 82
Figure 3.32: The Total Noise PSD levels for UWB (In-Band and Out-Band both) .... 82
Figure 3.33: The Total Noise PSD levels after the Filtration for UWB (In-Band and Out-Band both) .......................................................... 83
Figure 3.34 The Total Noise PSD levels after the Filtration for UWB (In-Band and Out-Band both) .......................................................... 84
Figure 3.35: UWB Spectrum after bandpass filter ..................................................... 85
Figure 3.36: Phase Noise requirements Vs. Correlation Coefficient for Gaussian Pulse .......................................................... 88
Figure 3.37: The Spectrum Before Downconversion ................................................. 89
Figure 3.38: The Downconverted Spectrum ............................................................... 89
Figure 3.39: Showing the transient response of the downconverter I/Q signals .. 90
Figure 3.40: Phase Noise requirement Vs. Correlation Coefficient for Gaussian Mono Pulse .......................................................... 91
Figure 3.41: The Signal Spectrum for Gaussian Mono Pulse before Downconversion .......................................................... 92
Figure 3.42: The Signal Spectrum for Gaussian Mono Pulse after Downconversion .......................................................... 92
Figure 3.43: Phase Noise requirement Vs. Correlation Coefficient for Gaussian Doublet Pulse .......................................................... 93
Figure 3.44: Phase Noise requirement Vs. Correlation Coefficient for Morlet Wavelet .......................................................... 94
Figure 3.45: The Signal Spectrum for Morlet Wavelet Function before Downconversion .......................................................... 95
Figure 3.46: The Signal Spectrum for Morlet Wavelet Function after Downconversion .......................................................... 95
Figure 3.47: Phase Noise requirement Vs. Correlation Coefficient for Daubechies’ Wavelet .......................................................... 96
Figure 3.48: Phase Noise requirement Vs. Correlation Coefficient for SINC Pulse 97
Figure 3.49: The Signal Spectrum for SINC function before Downconversion .......... 98
Figure 3.50: The Signal Spectrum for SINC function after Downconversion .......... 98
Figure 3.51: The Phase Noise vs. Correlation Coefficient for different pulses 99
Figure 3.52: Modeling of Low Noise Amplifier Block in MALAB ............................. 101
Figure 3.53: Correlation vs. Noise Figure of LNA .................................................... 102
Figure 4.1: Oscillator Block Diagram ............................................................... 107
Figure 4.2: RC Network Transformation ........................................................... 110
Figure 4.3: RL Network Transformation ........................................................... 110
Figure 4.4: Single Transistor implementation of an oscillator (a) Direct Feedback, (b) With Impedance Transformer ............................................................... 111
Figure 4.5: (a) Hartley Oscillator, (b) Colpitts Oscillator and (c) Single Ended Oscillator using a Source Follower as a positive Active Feedback ......................... 112
Figure 4.6: (a) PMOS cross-coupled differential oscillator with current sink and (b) NMOS cross-coupled differential oscillator with current source ......................... 113
Figure 4.7: Negative Transconductance transformation ....................................... 114
Figure 4.8: (a) Compact lumped-element π-model of an inductor and (b) Single Port Excitation of equivalent inductor model ................................................... 119
Figure 4.9: Test Bench for Inductor Simulation .................................................... 123
Figure 4.10: Showing the fault in the model predicted inductance value ............... 124
Figure 4.11: (a) Q-Factor for the set of Hollow Inductors .................................... 126
Figure 4.12: (a) Ratio of Effective Inductance to Parasitic Capacitance ................ 128
Figure 4.13: Peak Real (Z11) Vs. Inductance at Oscillation .................................. 129
Figure 4.14: The Basic Layout of the symindp inductor of value 2.1nH .................... 131
Figure 4.15: Variation of Capacitance for change in Bulk-Gate Voltage .......... 134
Figure 4.16: Effective Capacitance Vs. Tuning Voltage Sweep .......................... 136
Figure 4.17: Varactor Capacitance Vs. Tuning Voltage for different gate bias voltages ............................................................... 138
Figure 4.18: Tuning Range offered by the characterized varactor ....................... 139
Figure 4.19: The change in parasitic resistance over the tuning range ................. 140
Figure 4.20: The LC-tank reactance sweep over frequency ............................... 141
Figure 4.21: Starting Condition for an Oscillator .............................................. 144
Figure 4.22: (a) Diagram of a PMOS Differential Oscillator, (b) NMOS Differential Oscillator ............................................................... 149
Figure 4.23: (a) Tuning Range NMOS Diff-Pair Oscillator .................................. 151
Figure 4.24: (a) Phase noise of NMOS Diff-Pair Oscillator @ 1MHz offset ......... 153
Figure 4.25: (a) Peak to Peak Differential Voltage output of NMOS Oscillator .. 155
Figure 4.26: (a) Tuning Range comparison of push-pull oscillator for all the process corners ............................................................... 157
Figure 4.27: (a) Tuning range comparison of push-pull oscillator for all SS-F & FF- F process corners ................................................................................. 159
Figure 5.1: Two Quadrature Coupled Oscillators .............................................. 165
Figure 5.2: BS-QVCO (Half Circuit) ............................................................... 170
Figure 5.3: The Mirror half circuit of P-QVCO .................................................. 172
Figure 5.4: (a) Phase Noise comparison between P-QVCO and BS-QVCO ....... 174
Figure 5.5: Process Corner Analysis of P-QVCO for tuning range ...................... 176
Figure 5.6: Process Corner Analysis of P-QVCO for phase noise ..................... 177
Figure 5.7: Process Corner Analysis of P-QVCO for Quadrature Swing .......... 177
Figure 5.8: Implementation of Q-VCO with Poly-Phase Filter ....................... 178
Figure 5.9: RC-CR Network (Poly-Phase) [39] .................................................. 179
Figure 5.10: Circuit Design for Poly-Phase Filter Q-VCO ..................... 180
Figure 5.11: Phase Noise Vs. Neutralization Cap ........................................... 182
An Oscillator System for UWB QDAcR

Figure 5.12: Output Swing Comparison for Oscillator, Buffer and Poly-Phase outputs................................................................. 182
1 CHAPTER 1

Introduction: Ultra Wideband Systems & Technology and Thesis Objectives

1.1 Introduction

The advent and development of wireless communication systems and integrated circuit technology have revolutionized the contemporary life by combining the two main aspects firstly the access to all the required information at any time and anywhere and secondly the feasibility to perceive information in a friendlier manner that is portability, flexibility and scalability. There are a many subsystem and standards of communication within Wireless Communication Systems. A few of them of are as follows:

1. Cellular/Mobile Telephony (Technology: FDM, TDMA, CDMA and Bands: GSM, IS-95, IS 136 and UMTS etc.)
2. Wireless Local Area Networks (WLANs: 802.11a, 802.11b, 802.11g)
4. Bluetooth (ISM Band)
5. Ultra Wideband Radio (3.1GHz. -10.6GHz. ; Impulse radio, MB-OFDM UWB)

The latest being Ultra-Wideband Radio (UWB), is center of attention among the emerging communication technologies, it is still in developing stage and promises significant advantages over other communication technologies. The main advantages are transmission of high data rate over short-medium distances (10m-100m) with low power consumption and due to spread spectrum characteristics of UWB communication technology, it is less susceptible to multipath fading and more or less immune to electromagnetic interference (EMI) [1]. The system design issues for UWB technology have been addressed using two methods (1) Single Band Radio (Impulse Radio - IR), in which the system operates on the entire bandwidth as a single-wide band [2,3,4,5] and (2) Multiband OFDM Alliance for UWB (MBOA-UWB). In this the entire bandwidth is divided in to 14 sub-bands of 528MHz bandwidth each with highest data speed of 480Mb/s. [6] and the system design treats each band as in the case of narrowband communication technology.

There have been proposed different types of single-band transceiver architectures at system level, which provide novel solutions and which are mainly based upon the Correlation technique or Energy detection. The correlation is achieved either by the template mixing and integrating as shown in Figure 1 or by “the transmitted reference scheme receiver or “autocorrelation receiver” as proposed by [7] as shown in Figure 2. The example of single-band UWB transceiver is shown in Figure 3.
However, these proposed architectures are mostly at system level design and have not yet been translated into a complete circuit level system or into a fully operational IC. There has been reported very little work regarding parametric extraction, which serves as the basis of translating system level RF-building blocks to the actual circuit design. Most of these system designs consist of black box models of explicitly designed subsystems, which are interconnected and presented in the form of fully functional system design, without taking into account the jitter analysis, mismatching, noise and nonlinear coupling that happens between the various subsystems at the circuit level. Few circuit level designs have been reported for ir-UWB receiver’s RF-building blocks, which are mainly partial and inexplicit in nature and do not answer the main questions regarding the performance of the complete system fabricated into the IC-chip.
At system level an excellent and in depth research has been reported about the basic RF-building blocks required in ir-UWB receivers; however, there is a scarcity of information about the solutions for possible bottlenecks that can seriously degrade the receiver’s performance at circuit level. The advantages of low power consumption and simple processing circuitry posed by ir-UWB receiver are results of ‘Auto-Correlation’ technique, which in turn is totally dependent upon the mixing and matching of pulses; for these ir-UWB receivers a severe bottleneck is the ‘Timing Jitter’ and its implications on performance of the receiver. The existence and production of ‘Jitter’ in IC’s circuitry is a natural phenomenon due to presence of the noise, device fabrication and mismatching in the devices. The ‘jitter’ induced by the circuitry can be translated into circuit noise and therefore by designing the circuits, which meet the specific requirements, a possible solution for the severe bottleneck like timing jitter is found and as a result an optimized and coherent design for a fully functional IC can be derived.

In this work implications of the ‘jitter’ (produced predominantly in the downconverter) on performance of the ir-UWB based Quadrature Downconversion Autocorrelation Receiver (QDAcR) [8] at system level are being investigated and the findings lead to a very important result, which defines the constraints and parameterizes the downconverter in QDAcR, which acts as an integral and important part of UWB signal processing in analog domain. The importance of the result signifies the circuit design of QDAcR downconverter for optimal performance. The result outcome also provides an insight into the design perspective for Wideband Communication technologies like UWB, in which stringent requirements of narrowband communication technologies are eased and low power, simple and efficient circuit designs can be used and researched further. Also, the use of different types of (nano-pico seconds duration) pulses as carrier has been reported, whilst the Gaussian mono or Gaussian double being the most widely used carrier for information transfer in the UWB system; in this work, the QDAcR system is tested for different kind of pulses, which fulfills the UWB band in frequency domain, and the outcome is summarized as the choice of pulse which best suits the optimum performance of the QDAcR.

1.2 Ultra-Wideband Communication Systems

Ultra-wideband communications is a radio frequency technology that uses extremely narrow RF pulses to communicate between a set of transmitters and receivers. It is distinct from conventional sinusoidal narrowband wireless technology in which transmission is done on different frequencies, in UWB the signal is spread over wide range of frequencies. Historically, UWB communication technology was first used by Guglielmo Marconi in 1901 to transmit Morse code sequences across the Atlantic Ocean using a spark gap transmitter. The UWB communication technology gained impetus in military applications such as impulse radar and UWB technology was restricted for just military purposes from 1960s-1990s [9].

The Figure 4 show a UWB pulse in time domain and in frequency domain and a comparison with a sinusoidal narrowband pulse in time and frequency domain.
In UWB the pulse train of extremely short duration (nano second – pico second) is used for communication as the information carrier in time domain and this generates a very wide spectrum across different frequencies in frequency domain. “The spectrum of such a pulse sequence (usually Gaussian) has a single broad main lobe with a low spectral roll-off [10]” and offers advantages like robustness to jamming, co-existence with current radio services. There are many wideband signals that qualify for UWB communication systems and a few of them are Gaussian, Gaussian Mono (First Derivative of Gaussian), Gaussian Second Derivative, Morlet, Sinc, chirp or Daubechies wavelet. The Figure 5 below shows a Gaussian Mono signal a pulse of 500picosecond in time domain and wide spectrum with a single main lobe at fc = 2GHz and with a low spectral roll-off in frequency domain.
1.3 UWB Regulations and Ultra Wideband System’s comparison with Narrowband Communication system

In UWB communication technology a pulse train is used as information carrier and in comparison to narrowband technologies, UWB communication technology has very low average transmission power. The transmission power in UWB technology is in the order of microwatts whereas it is many-folds higher in magnitude for narrowband communication systems. The reason for extremely low average transmission power in UWB communication technology is that in UWB the short pulses (nano seconds – pico seconds) are used and such sort pulses have very low duty cycle. Also a low average transmission power translates into a longer battery life for UWB communication system devices. According to the FCC regulations regarding the use of UWB, states that UWB signal must have at least a bandwidth of 500MHz for operation at frequency 3.1GHz to 10.6GHz ‘OR’ a fractional bandwidth which is at least or larger than the 20% of the center frequency at all times of transmission. The fractional bandwidth is a measure of bandwidth between the points which are at -10dB distance from the central frequency [11]. As seen from Figure 4. The-10dB points are located at $f_h = 1.2$ GHz and $f_l = 2.8$GHz with a central frequency $f_c = 2$GHz. Therefore, for this signal to qualify as UWB signal, the fractional bandwidth $B_f > 0.2f_c$. Calculating the fractional bandwidth in accordance with the FCC rules, it follows that

$$B_f = \left( \frac{f_h - f_l}{f_c} \right) \times 100 = \frac{2.8 - 1.2}{2} \times 100 = 80\%$$

which confirms that the signal is an UWB signal.
The classification of the signal on the basis of fractional bandwidth is as follows.

Narrowband \( B_f < 1\% \)

Wideband \( 1\% < B_f < 20\% \)

Ultra Wideband \( B_f > 20\% \)

The maximum allowed power spectral density (PSD) levels for UWB systems are limited to -41.3dBm/MHz for both indoor as well as outdoor operations; this protects other contemporary wireless systems having interference from the UWB systems, as these PSD levels for UWB system are equivalent to the PSD levels of systems like television and computer monitor etc. Figure 6 shows the emission levels prescribed by the FCC for the UWB communication systems under indoor conditions. The difference between the indoor and outdoor emission limits for UWB systems is that the spectral mask for outdoor devices is 10dB lower than that of indoor devices between frequencies 1.6GHz and 3.1GHz. The Figure 6 shows the emission levels prescribed by the FCC for the UWB communication systems under outdoor conditions.

![Figure 1.6: The UWB emission mask for the indoor & outdoor communication.](image)

The spread spectrum is also a wideband communication technique, with advantages like low PSD levels, resistance to jamming, resistance to fading and multiple access capability. All of these advantages are
An Oscillator System for UWB QDAcR

similar to the merits of UWB systems; however there is a significant difference between both techniques and this is in the method of achieving the large bandwidth

As mentioned in [10] ir-UWB communication system uses the pulse in-itself as carrier. In narrow band system sinusoidal is used as carrier in the same way the pico-second Gaussian or other pulses acts as a carrier for transmitting the data in the ir-UWB systems. “However in a properly designed UWB system the carrier is indistinguishable from the other spectral components of the UWB signal [10]”. The UWB pulses provide several GHz of bandwidth while in spread spectrum a few MHz of bandwidth is achieved. Figure 7 shows the distinction between the narrowband, wideband and ultra wideband communication systems. The UWB technology poses several advantages over the narrowband communication systems. The main advantages are high data rate, ability to co-exist with narrowband systems and high performance in multipath channels

![Distinction between the different communication techniques.](image)

The data rate transfer in any system can be described using the well-known Shannon – Hartley’s Equation, which is $C = B \log_2(1 + SNR)$ ; where $C$ = Channel Capacity, $B$ = Bandwidth of the system and $SNR$ = Signal to Noise Power Ratio. The channel capacity ‘C’ is the data rate or maximum data that can be transmitted per second over the communication channel and as we see from the Equation that channel capacity ‘C’ is directly proportional to the Bandwidth of the system and effective signal to noise ratio ‘SNR’. Therefore, the channel capacity can be improved by increasing the bandwidth or effective SNR of the communication system. In UWB systems the highest allowed PSD allowed by FCC is -41.3dBm/MHz, which translates to very small value of SNR ($SNR_{UWB} = 0dB$). In comparison to the narrowband communication systems the UWB system poses a poor SNR value, however it can be seen from the
Shannon’s Equation that ‘C’ is proportional to the Logarithmic of the SNR; therefore UWB system provides high channel capacity or data rate only by using very wide bandwidth which is usually 7.5GHz. A comparison of data rate for various IEEE Standards is shown in the Figure 8 below.

![Figure 1.8: Comparison of Data throughput and range for IEEE 802 Standards [12]](image)

It can be discerned from the above Figure 1.8 that data rate decreases for the UWB (IEEE 802.15.3a) for high ranges, this is due to the fact that UWB communications uses pulses or carrier frequency waves (like Gaussian, Gaussian Mono, Morlet etc.), which have very low Power Spectral Density (PSD) levels and in some cases the PSD levels are below the noise floor. Therefore, it is hard to detect UWB carriers for higher ranges and data rate drops significantly. The low PSD levels allow UWB system to co-exist with other contemporary narrowband communication systems; in Figure 9 it is shown that the UWB PSD levels resides a few dB above the noise floor if considered for entire 7.5GHz bandwidth, also shown are the PSD levels of the main Narrowband interferes in this band.

![Figure 1.9: Coexistence of UWB signals with narrowband and wideband signals in the RF spectrum](image)
The UWB systems perform with high efficiency in multipath systems; where multipath is generated due to the signal reflection/refraction with some object. In narrowband communication systems the multipath can degrade the signal strength due to out of phase addition of LOS (line of sight; non interfering signals) and NLOS (non-line of sight; interfering signals). The short duration UWB pulses are less susceptible to the multipath effect, because the time period of UWB pulses is of order of nano or pico seconds. Therefore the reflected pulses have very low chances of colliding, adding, overlapping and/or superposition with the LOS pulses and as a result having no or extremely less signal strength degradation. By choosing proper modulation technique signal strength degradation can be ceased further, the commonly used modulation techniques for ir-UWB systems are Pulse Position Modulation (PPM), On-Off Keying (OOK), Pulse Amplitude Modulation (PAM) and Bi-Phase Modulation (BPM). Besides these UWB systems poses many other significant advantages like low interception and detection by other system i.e. low chances of eavesdropping because of low PSD signal levels.

1.4 Ultra Wideband Transceiver Architectures and Challenges

The transceiver architecture for the UWB communication technology can be broadly classified into two categories, based on the transceiver architecture topologies. These primarily differentiate in the way of treatment of the complete bandwidth offered by the UWB communication technology. These two methodologies as previously stated are:

1. Multiband OFDM Alliance for UWB (MBOA-UWB): In MBOA-UWB system the entire 7.5 GHz bandwidth is divided into 14 bands of 528MHz bandwidth each and in total covering the entire frequency range of 3168 MHz to 10560MHz [13]. The use of OFDM and multiband hopping technique ensures high data rates and ease from the problem of high speed Analog to Digital Converter and pulse distortion. The main advantage of MBOA-UWB technique is that it can handle the problem of interference in a far better manner than ir-UWB technique. As in MBOA-UWB system there is not data transmission in 5GHz-6GHz band, which alienates the main in-band interferer HIPER LAN and its modulated components from degrading the receiver’s performance. However, as MBOA-UWB employs narrowband communication architecture this imposes very stringent circuit level design requirements. The main problems encountered in this architecture are design of band switching circuit which involves band select and high gain LNA and high phase noise requirements for LO and accurate frequency synthesizer that should synthesize frequencies for multiband operation with (a low jitter) high phase noise [13,14]. The typical design parameters of a MBOA-UWB transceiver are given in [13, 15]. A well designed and thorough architecture of multiple band UWB receiver is given in [16]. The problem of spurs also effect the performance of the receiver, therefore a high linearity is essential for mixers, which translates into high power consumption, low conversion gain and small output swing. The multiband OFDM architecture does provide a solution to complete design and a fully functional IC for UWB system; however, it requires highly complex circuitry,
high power consumption and stringent design requirements. In addition, one of the severities attached to MBOA-UWB is use of power amplifier (PA) in the transmitter part, which not only increases the power consumption but adds to the non-linearity and noise issues as well. Besides these disadvantages, the design of MBOA-UWB system prefers Bipolar technology over CMOS [16] to tackle issues of spurs, phase and gain mismatch and conversion gain, which can be expensive and not compatible with prevailing CMOS IC technology for mass production.

2. Impulse Radio UWB system (ir-UWB or Single band Radio): In ir-UWB system, the entire bandwidth is treated as a single band and processed upon by using the correlation and sampling techniques. The ir-UWB system is supposed to provide advantages like low power consumption and immunity towards the electromagnetic interferences. However, these advantages are very much dependent upon the efficiency of system design for ir-UWB transceiver architecture. The very basic architecture for ir-UWB transceiver proposed is shown in Figure 3 [2]. In order for this design to work an ADC (analog to digital converter) should sample and digitize the complete bandwidth of 7.5GHz at the Nyquist rate of minimum 15Gsamples/sec, this high sampling speed will lead to design of an ADC that consumes excessive power and results in the loss of one of the primary advantages of low power consumption for ir-UWB systems. The solution to this problem caused by the high sampling rate is presented in [2] in form of the (1) Time-Interleaved Architecture, (2) Frequency-Domain Channelizing and (3) signal processing in analog domain, the first two topologies do reduce the complexity of ADC design by reducing the sampling speed, but still suffer from higher power consumption and large die area due to Band Pass Filter. The generalized architecture of receiver design is presented in Figure 10 [2] in which either time domain correlation or down-conversion is done, this decimates the sampling frequency and provides with a viable solution for ir-UWB receiver architecture.

Figure 1.10: Time domain Correlator Receiver architecture [2]

However, ir-UWB correlation receivers do suffer from severe bottleneck of jitter and template mismatching, other important issue regarding the performance of the ir-UWB receivers is narrowband interference that can potentially jam the ir-UWB system due to the presence of high power narrowband
interferes, which are presented by the existing narrowband communication standards of WLAN or Hiperlan and IEEE802.11a.

Another challenge is channel estimation, as we know that in ir-UWB correlation receivers the received signal is correlated with the predefined template. Therefore for proper matching with the received signal knowledge of channel parameters is of foremost importance while deciding about the template. As it is mentioned previously that UWB pulses are prone to shape distortion, therefore channel estimation becomes more complex and more important for the UWB communication systems.

To counter the problem of template mismatching and time synchronization a novel solution for ir-UWB receiver system is presented in the form of QDAcR [8], which is based upon the delay hopped transmitted reference scheme (DHTR) proposed by [7], in DHTR the correlation takes place between the two pulses per symbol, which are transmitted with a delay of ‘\( \tau_d \)’ as shown in Figure 2, the first pulse, which acts as reference pulse is delayed by the same time delay of ‘\( \tau_d \)’ and multiplied with the second pulse, which acts as a modulated one and the correlation is achieved by integrating the mixed pulse over one delay length [8].

This technique of autocorrelation is very much advantageous as it does reduce the system design complexity arising from pulse distortion and mismatching with template. However, it also suffers from timing synchronization that is, mismatch in the delay time between the transmitter and receiver parts; the reliability and efficiency of QDAcR is closely dependent upon the design of the delay [8]. The major factor that eases the complexity of the design constraints is by processing the bandwidth in analog domain [2], likewise downconversion reduces the circuit design complexities and maintains the ir-UWB system inherited advantages. The use of analog signal processing and DHTR or autocorrelation technique in system design proposes the most feasible and optimized design for a complete ir-UWB receiver; Quadrature Downconversion Autocorrelation Receiver (QDAcR) is such an example. In QDAcR the bandwidth is downconverted and processed as to reduce the circuit complexity and save power by reducing the sampling speed of ADC, also the selection of Local Oscillator frequency makes it possible to clear the bandwidth of existing interferes [8]. However, to realize QDAcR into a fully functional IC, in depth system analysis of QDAcR should be performed and the first step is to find the parameters of the conventional RF building blocks, while taking into account the system and design constraints produced by the RF building blocks and the composite implication of all of these factors on the performance of the QDAcR.

In this chapter the theory of ultra wideband systems and the main system level design issues were dealt in a concise but comprehensive manner. The main focus of this chapter was to provide an insight into the developments in the field of UWB system design and gathering the background knowledge of the advantages as well as the bottlenecks and design issues, with comparison based on the literature research between the two prominent styles of system architectures that are ir-UWB and MBOA-UWB. Also, a comparison between the ultra wideband and narrowband communication system is presented, which
highlights the different advantages inherited by UWB system over the Narrowband communication system due to its definition. In brief in this chapter an overview of existing UWB system designs, their advantages and serious flaws were discussed, which lay down path to objective of this thesis.

1.5 Thesis Objectives

The thesis titled “An Oscillator system for a Quadrature Downconversion Auto-Correlation Ultra Wideband (UWB) Receiver,” is produced to reflect the work done as Master’s Degree Project. The thesis work can be predominantly divided into two sub fields. Firstly, the system level study, design and extraction of the required specifications and parameters for the circuit level design. Second field was to translate these specifications into circuits.

Primary focus of the work was concentrated towards the system level design and parametric extraction; which starts with a study of previously done ‘Quadrature Auto-correlation Downconversion Receiver [8] at the system level design using matlab; however, the previous system design was proposed at the generic level that is laying down the concept of QDAcR and implementing it in matlab as system design without taking into consideration the problem of jitter, interferer and specs for the RF building blocks. The next and the most important step was to design the complete system in order to find the desired phase noise that can be induced by the local oscillator while meeting the correlation requirements. As an enhancement of this result was to test the design for various impulse inputs and find for which pulse, the design can have highest degree of correlation with the least amount of phase noise

The next step was to work on circuit design for the Quadrature Oscillator Q-VCO; in this first step was to decide upon the oscillator topology while meeting the specifications and utilizing the importance of the outcome from the system level design. This was followed by the investigation of different Q-VCO topologies, in order to find a suitable oscillator design topology, which not just meet the specifications but should provide a robust circuit design. First step involved, the choice of oscillator topology followed by the optimization for a low power design. The designed LO is then used as an essential element in designing of Q-VCO, the complete design involves the design of output buffer, able to drive the variable load.
2 CHAPTER 2

Methods and Techniques for System Level Design of QDacR Downconverter

In this chapter the quantitative methods and techniques used for modeling and assessing the implications of the ‘jitter’, induced by the local oscillator in the downconverter are presented in detail. First up a brief overview of the previously done work on QDacR is presented, this is followed by the most important part of devising a complete mathematical analysis of basic QDacR. This analysis helps us in understanding the implication of phase noise on QDacR performance. The exercise of quantitative analysis provides in end with a relationship between phase noise and timing jitter. This relationship serves as the very basis of advanced system level modeling of QDacR.

2.1 System Level Design

The importance of the downconverter in QDacR has been highlighted in earlier chapter; the severe bottlenecks that are present in QDacR are firstly, the design of downconverter that gives optimal autocorrelation and secondly, design of time delay circuit; the solution of the latter is published in [8, 17 & 18]. In this section the complete system modeling of the QDacR is presented. Starting with a brief explanation of the existing model succeeding it with an in-depth Time domain modeling of the QDacR, this analysis in certain conditions can also be extrapolated to general receiver theory. In time domain modeling for the first time the stochastic nature of the signal and their overall effect is considered, this leads to the relationship which signifies the role of phase noise (presented as phase perturbation) in the QDacR to be specific and can be generalized onto other receivers. The following section presents in brief about the noises present in the system and the constituents of the phase noise, further in this section the reasoning of using $1/f^2$ region as the prime region for noticing the phase noise in context with the QDacR specific design is presented.

In the next section the Time-Jitter analysis of an oscillator and the relationship between the jitter and phase noise is re-visited, this relationship already exists, but in this section the relationship is derived by characterizing phase perturbation and timing jitter as two similarly distributed variables, which are correlated and this effect leads to the description of “accumulating jitter” and/or “cyclostationary” property of the phase noise. This relationship is used to model the oscillator in MATLAB.
2.2 Quadrature Downconversion Autocorrelation Receiver

In this section, a brief overview of the QDAcR is presented; the Quadrature Downconversion Autocorrelation Receiver or QDAcR [8] is based on the Delay Hopped Transmitted Reference scheme as proposed in [7]. By use of ‘autocorrelation’ architecture, the problem of template mismatching is circumvented. Other major problem of high speed signal processing is curtailed by using the downconverter, which down converts or wraps the entire frequency band of 7.5GHz to a smaller band around dc, which can be processed by the ADC (analog to digital converter). Furthermore, this frequency wrapping or downconversion gives the advantage to clear off strong narrowband interferes like WLAN, HiperLAN and 802.11a/n by choosing the appropriate Local Oscillator frequency and followed by filtering the band, these interferes can potentially jam the QDAcR. The block diagram of the QDAcR is given in the Figure 2.1.

As shown in the Figure 2.1 above, the system design of QDAcR consists of four main stages, 1. Antenna and LNA (Gain Stage) 2. Downconversion (Frequency Wrapping) Stage, which consists of an Ideal Oscillator with Quadrature outputs and Ideal Multiplier 3. The Filtering Stage that has Band pass filters employed to clear off interferes and 4. The Autocorrelation Stage, which consist of time delay, Ideal Multiplier and an Integrator. In [8] the system analysis of QDAcR under the ideal conditions is presented, in which the 3.1GHz to 10.6GHz UWB band is downconverted. The oscillation frequency of the ideal Local Oscillator (LO) is chosen to be 5.5GHz, so that the potentially jamming interferes present around 5.15GHz and 2.4GHz, are downconverted to (5.5-5.1) GHz = .350GHz = 350MHz and 2.4GHz interfere is converted to (5.5-2.4) GHz = 3.1GHz. The 36% of UWB bandwidth is also lost in frequency wrapping. The Figure 2.2 shows the principle of band downconversion and also shows downconverted frequency band.
The band-pass filters are used for the rejection of the interference is presented in [21]; after downconversion, the interferes appear at below 350MHz and above 2.4GHz, for the steepest slope an eight order elliptic band-pass filter with corner frequencies at 350MHz and 2.6GHz, is designed as an interference rejection filter [21].

In [8] the time domain analysis of the QDAcR is given, which explains the autocorrelation principle of QDAcR. In which the downconverted Quadrature components are delayed and multiplied intrinsically and then added. The time domain analysis also signifies the implications of the time delay on the performance of the receiver and the stringent design condition it poses, besides this the final mathematical relation, which signifies the importance of the time delay is given by the Equation 

\[ Y = -\frac{A(t')^2}{4} \cos(\omega_{osc} \tau_d) \]  

(2.1)

where ‘Y’ is the output of the mixed signals before integration and this equation shows the dependency of the autocorrelation coefficient on the time delay or the performance of the receiver is directly related to the oscillators angular frequency ‘\( \omega_{osc} \)’ and the time delay ‘\( \tau_d \)’. Further, the results of the error analysis in time domain on QDAcR confirms this, in which the analysis for ‘\( \alpha \)’ (the amplitude mismatch), ‘\( \beta \)’ (the mismatch between the delay time ‘\( \tau_d \)’ in transmitter and receiver), and ‘\( \phi \)’ (the phase error between the Quadrature outputs of the oscillator) is presented [8]. The results of the error analysis are summarized in [8] and analyzes sow that how important is ‘\( \beta \)’ that is the error in the delay time ‘\( \tau_d \)’ is for the proper performance of QDAcR. It also shows that for a mismatch of 20 - 30 picoseconds the autocorrelation is dropped from 85% to around 65%; therefore, designing of the perfect delay is very important for the performance of the QDAcR.
2.3 Time Domain Analysis of QDAcR

The time domain analysis and system level simulation done in [8] does not take into account the jitter and noise analysis and other non-idealities that are present in a real downconverter and other circuits. Therefore, an upgradation in present system design is required so that the system analysis result can provide with the accurate and real parameters for circuit level designing of QDAcR. First step in this direction is to establish mathematically the dependence of the autocorrelation factor on the random aberrances (such as jitter or phase noise, phase error etc.) contributed by RF building blocks used in the downconverter. The mathematical model is necessary because the results of quantitative modeling will make the base for the matlab modeling and also provide the interdependency between various parameters.

The output (voltage signal) of an ideal local oscillator can be defined by the Equation 2.2 as given below, where \( A_{\text{out}}(t) = V_{\text{out}}(t) \) is LO output at time \( t \), where \( A_{\text{in}} = V_0 \) is the maximum signal (voltage \( V_0 \)) swing amplitude of LO, the angular oscillation frequency is \( \omega_0 \) and a constant phase reference of \( \phi_0(\ ) \).

\[
A_{\text{out}}(t) = A_{\text{in}} \cos(\omega_0 t + \phi_0(t))
\]  

However in a practical oscillator there exist non-idealities due to the fluctuations in phase and the amplitude owing to power supply, non-ideal active devices, passives etc. The Equation for the output now can be defined as shown in Equation 2.3, where phase is expressed as the function of time \( t \) and denoted by \( \phi(t) = \phi_0(t) + \Delta\phi(t) \) and the perturbation in phase as \( \Delta\phi(t) \) and the perturbation in the LO amplitude is denoted by \( \alpha(t) \). The perturbations present in the phase and the amplitude of the LO are random in nature [22]. The in-phase (I) output of LO is given in Equation below as:

\[
A_{\text{in}}(t) = A_{\text{in}}(1 + \alpha(t)) \cos(\omega_0 t + \phi(t))
\]

Taking the signal carrier as defined in [8] for the pulse-based signals having a finite band-pass spectrum, therefore characterizing the pulse signal with a Gaussian envelope, with \( \omega_c \) being the angular center frequency and \( \phi(t) \) as the phase; the real signal carrier is given by the Equation 2.4.

\[
g(t) = A(t) \cos(\omega_c t + \phi(t))
\]

In QDAcR, the carrier signal is mixed with the outputs of a Quadrature Local Oscillator, which are described as in-phase component (I) and quadrature (Q) component, therefore if an in-phase (I) component of an oscillator is given by Equation 2.3 then the Quadrature (Q) is given by Equation 2.5 as shown below; where \( \phi_e \) is the phase error between the Quadrature outputs of the oscillator.

\[
A_{\text{out}}(t) = A_{\text{in}}(1 + \alpha(t)) \sin(\omega_0 t + \phi(t) \pm \phi_e)
\]
An Oscillator System for UWB QDAcR

path the downconverted output is given by \( M_1(t) \) as shown by Equation 2.6. As mentioned in [22] the random perturbations in phase and amplitude of LO are stochastic and instantaneous; therefore, for a particular oscillation cycle that multiplies with the first pulse signal at any instance ‘\( t \)’, the actual instantaneous phase ‘\( \phi(t) \)’ (sum of constant phase and excess phase) for the particular mixing oscillator cycle is given by \( \phi(t) = \phi_0 + \Delta \phi(t) \) and amplitude perturbation by \( \alpha(t) \).

\[
M_1(t) = A(t)A_\nu(1 + \alpha(t)) \cos(\omega_f t + \phi(t)) \cos(\omega_f t + \phi(t))
\]

(2.6)

Further simplifying the Equation 2.6 using the identity \( \cos(a).\cos(b) = \frac{1}{2}[\cos(a+b) + \cos(a-b)] \), therefore, the mixed and filtered component given by Equation 2.7;

\[
\frac{1}{2}[A(t)A_\nu(1 + \alpha(t)) \cos((\omega_f - \omega_a) t + \phi(t)) - \phi(t))]
\]

(2.7)

Delaying the first pulse by time ‘\( \tau_d \)’, the Equation 2.7 is now given as Equation 2.8; where ‘\( t = t - \tau_d \); there are no changes in the expected values of amplitude perturbation and excess phase as their values were decided at the instance of oscillator cycle generation, by the non-idealities present in the form of active device noise and other affecting parameters. There is always noise associated with any active circuit component; therefore, an ideal delay element in the QDAcR does not affect the value of phase and amplitude perturbations. Therefore the Equation for a delayed and filtered signal can be written as equation 2.8

\[
\frac{1}{2}[A(t)A_\nu(1 + \alpha(t)) \cos((\omega_f - \omega_a) t + \phi(t)) - \phi(t))]
\]

(2.8)

Now considering the second pulse, which was delayed in the transmitter by time ‘\( \tau_d \)’; mixing this pulse with the oscillator cycle at time any instance of time ‘\( t \)’; the mixed output is given by the Equation 2.9

\[
M_2(t) = A(t)A_\nu(1 + \alpha(t)) \cos(\omega_f t + \phi(t)) \cos(\omega_f t + \phi(t))
\]

(2.9)

Where ‘\( t = t - \tau_d \)’ and for the second pulse signal the values of ‘\( \phi_2(t) \)’ and ‘\( \alpha_2(t) \)’ are defined for a particular oscillator cycle at an instance of time ‘\( t \)’ when mixing of RF-UWB Impulse signal is done with oscillator signal. The perturbations as defined earlier are produced by the non-idealities present in the real downconverter. Simplifying the Equation 2.9 and neglecting the summing components of ‘\( \omega_f \) & \( \omega_a \)’, which are filtered and as the response through the band-pass filter, we have the final outcome, which is given by the Equation 2.10

\[
\frac{1}{2}[A(t)A_\nu(1 + \alpha_2(t)) \cos((\omega_f - \omega_a) t + \omega_a \tau_d + \phi(t)) - \phi(t))]
\]

(2.10)

Now multiplying the Equations 2.8 and 2.10, we have the multiplied in-phase output required for the autocorrelation; the multiplication of two mixed and delayed pulses is given in Equation 2.11 below.
An Oscillator System for UWB QDAcR

\[
\frac{A(t')^2 A_n(1 + \alpha_i(t)).A_n(1 + \alpha_i(t))}{4} \left[ \cos((\omega_0 - \omega_j)t - \omega_j \tau_j + \phi(t) - \phi_j(t)) \right] \left[ \cos((\omega_0 - \omega_j)t' + \phi(t) - \phi_j(t)) \right]
\]

(2.11)

Simplifying the Equation 2.11 by using the identity \( \cos(a) \cos(b) = \frac{1}{2} [\cos(a+b) + \cos(a-b)] \), we have output as given in Equation 2.12

\[
\frac{A(t')^2 A_n(1 + \alpha_i(t)).A_n(1 + \alpha_i(t))}{8} \left[ \cos(2(\omega_0 - \omega_j)t - \omega_j \tau_j + 2\phi(t) - \phi_j(t)) + \cos(\phi(t) - \phi_j(t) - \omega_j \tau_j) \right]
\]

(2.12)

The above shown Equation 2.12 gives the total mixed (LO x RF-UWB Impulse Signal), filtered and delayed (delayed and multiply) IN-Phase component of QDAcR.

In order to see the dependence of QDAcR on the non-idealities presented by the downconverter, a complete time domain analysis is necessary. The time domain analysis of the Quadrature path is done similarly in the same fashion as of the In-Phase path.

The quadrature mixed component \( M_q \) is given by Equation 2.14; which shows the mixing of RF-UWB Impulse signal with an LO signal. The RF-UWB signal is given by Equation 2.13

\[
g(t) = A(t) \cos(\omega_0 t + \phi(t))
\]

(2.13)

The quadrature mixed component is given below by Equation 2.14, where \( \phi_j(t) \) and \( \alpha_j(t) \) are the expected values of the total phase and amplitude change for a particular quadrature oscillator cycle, which is multiplied to the first signal pulse in order to downconvert.

\[
M_q = A(t) A_n(1 + \alpha_i(t)). \cos(\omega t + \phi(t)). \sin(\alpha t + \phi_i(t) \pm \phi_j(t))
\]

(2.14)

The Equation 2.14 is further simplified using the identity \( \cos(a) \sin(b) = \frac{1}{2} [\sin(a+b) - \sin(a-b)] \). The simplified mixed and filtered quadrature component is given by Equation 2.15 as shown below.

\[
-\frac{1}{2} [\frac{A(t) A_n(1 + \alpha_i(t))}{2}]. \sin((\omega - \omega_j)t + \phi(t) - \phi_i(t) \pm \phi_j(t))
\]

(2.15)

Now delaying this quadrature filtered and mixed component by time \( \tau_d \) and substitute \( t' = t - \tau_d \) in Equation 2.15, the Equation 2.16 is obtained.

\[
-\frac{1}{2} [\frac{A(t') A_n(1 + \alpha_i(t'))}{2}]. \sin((\omega - \omega_j)t' + \phi(t) - \phi_i(t) \pm \phi_j(t))
\]

(2.16)

The time domain analysis for the second pulse which is being sent by a delay of time \( \tau_d \) from the transmitter, mixed with quadrature LO signal at any instance of time \( t' \), filtered and simplified is given by the Equation 2.17 as shown below. Where \( \phi_i(t) \) and \( \alpha_i(t) \) are the expected values of the total phase and amplitude change for a particular quadrature oscillator cycle, which is mixed with the second signal pulse.

-28-
An Oscillator System for UWB QDAcR

\[-\frac{1}{2}[A(t'), A_e(t) + \omega_0 \tau_d + \phi(t) - \phi_1(t) + \phi_2(t)] \quad (2.17)\]

The two mixed and filtered pulse responses in Equations 2.16 and 2.17 are multiplied as for the process of the autocorrelation; therefore the final Quadrature path response is obtained by simplifying using the identity \(\sin(a) \cdot \sin(b) = \frac{1}{2} \{\cos(a-b) - \cos(a+b)\}\) and the simplified answer is given by the Equation 2.18.

\[
\frac{A(t')^2 A_e(t + \omega_0 \tau_d + \phi(t) - \phi_1(t) + \phi_2(t))}{4} \{\cos((\omega_0 - \omega_0)x' + \phi(t)) - \cos((\omega_0 - \omega_0)x' + \phi(t) \pm \phi_2(t))\}
\]

\[
\frac{A(t')^2 A_e(t + \omega_0 \tau_d + \phi(t) - \phi_1(t) + \phi_2(t))}{8} \{\cos(2(\omega_0 - \omega_0)x' + \phi(t)) - \cos(2(\omega_0 - \omega_0)x' + \phi(t) \pm \phi_2(t))\}
\]

(2.18)

Now for the complete output of the QDAcR the in-phase and quadrature phase responses are added up. Therefore the final auto-correlated output of the QDAcR is given by adding the Equations 2.12 and 2.18, which is given by the Equation 2.19.

\[
\frac{A(t')^2 A_e(t + \omega_0 \tau_d + \phi(t) - \phi_1(t) + \phi_2(t))}{8} \{\cos(2(\omega_0 - \omega_0)x' + \phi(t)) - \cos(2(\omega_0 - \omega_0)x' + \phi(t) \pm \phi_2(t))\}
\]

\[
+ \frac{A(t')^2 A_e(t + \omega_0 \tau_d + \phi(t) - \phi_1(t) + \phi_2(t))}{8} \{\cos(2(\omega_0 - \omega_0)x' + \phi(t)) - \cos(2(\omega_0 - \omega_0)x' + \phi(t) \pm \phi_2(t))\}
\]

(2.19)

The above Equation holds quite a significance as it shows on which variables and in what manner the autocorrelation in the QDAcR is dependent upon, the perfect or near perfect level of autocorrelation is vital for QDAcR in order to perform with distinctive advantages posed by ir-UWB system over MBOA-UWB system as explained previously in Chapter 1. Also, by the analysis of the Equation 2.19, a first insight into the circuit design of downconverter is provided.

In Equation 2.19, the autocorrelation is dependent upon the time delay \(\tau_d\) as is shown in [8, 23]. However, the delay is considered to be an ideal one, but in real circuit this is not a fact. Therefore the perturbation in the Equation 2.19 can be modeled appropriately as a composite perturbation and the effects of the perturbations in amplitude and phase of the carrier (Pulse) due to the delay can be taken into account.

In the time domain analysis presented in this work, the effect of perturbations in an Oscillator and the effect of phase error (which is also treated as a stochastic variable) between the in-phase and quadrature outputs is primarily investigated. The Equation 2.19 also signifies the importance of the oscillator design for proper
An Oscillator System for UWB QDAcR

autocorrelation in order to reduce the BER (Bit to Error Ratio); which is a crucial parameter while assessing the ir-UWB receiver’s or any receiver’s performance.

The Equation 2.19 can be further simplified using a few approximations, these are as follows.

The perturbations due to uncorrelated noise, which follow the stationary stochastic process that is the random variables $\{x_{nk}, \ldots, x_{nk}\}$ and $(x_{nk+1}, \ldots, x_{nk+n})$ for every $k \geq 1$ in some sample space have same joint distribution; therefore all the uncorrelated noise perturbations characterized by stationary stochastic process have same distribution and mean is time independent; this approximation is in accordance with [24] in which the random perturbations in an oscillator due to uncorrelated noise that is white noise (stationary) and modulated white noise(cyclostationary) can be characterized by the Gaussian distribution in time. This follows that in Equation 2.19, the phase noise stochastic perturbations $\phi(t)\&\phi(t)$ are uncorrelated and have same Gaussian distribution and the same applies on the phase noise perturbations given by $\phi(t)\&\phi(t)$. This can be mathematically proved; we know that the (auto) correlation between two random variables 'X' and 'Y or $X^*$'is case of autocorrelation, for the autocorrelation random variables are associated with a repetitive process e.g. An Oscillator) and is given by

$$C_{X,X}(t,t) = \rho_{X,Y}\sigma_X\sigma_Y$$

where $\rho_{X,Y}$ is the coefficient of correlation and $C_{X,X}(t,t)$ is the coefficient of autocorrelation, $\sigma_X$ & $\sigma_Y$ are the standard deviations and $\mu_X$ & $\mu_Y$ are the means and the operator 'E' defines the expected value of a random variable. Let consider a oscillation cycle which is given by Equation 2.2, considering the LO output at instances ‘$t_1$ & $t_2$ ’ which are given by the following Equations

$$A_n(t_1) = A_0(\omega(t_1) + \phi(t_1)) \& A_n(t_2) = A_0(\omega(t_2) + \phi(t_2)),$$

where $\phi(t_1) = \phi(t_2) = \phi_0 + \Delta\phi(t_1)$ and $\phi(t_2) = \phi(t_2) = \phi_0 + \Delta\phi(t_2)$, since the phase perturbations have joint Gaussian distribution, therefore the sum and differences of instantaneous phases are also Gaussian and can be described as shown in Equation 2.20.

$$\phi(t_1)-\phi(t_2) = \Delta\phi(t_2) - \Delta\phi(t_1) = \Delta\phi$$

$$\phi(t_2)+\phi(t_1) = 2\phi_0 + \Delta\phi(t_1) + \Delta\phi(t_2) = 2\phi_0 + \Delta\phi$$

Since the Probability density function (PDF) is Gaussian, the process can be described as the ‘Wiener Process’ as shown in [25], which defines mean to be ‘zero’, therefore the autocorrelation is given by Equation 2.21

$$C(t_1,t_2) = E[A_n(t_1)A_n(t_2)] = A_0^2E[\cos(\omega(t_1) + \phi(t_1)) \cos(\omega(t_2) + \phi(t_2))]$$

Solving the Equation 2.21 using the identity $\cos(a)\cos(b) = \frac{1}{2}[\cos(a+b)+\cos(a-b)]$, the simplified Equation is given as 2.22

$$C(t_1,t_2) = \frac{A_0^2}{2}\left\{E[\cos(\omega(t_2 - t_1) + \Delta\phi(t))]+E[\cos(\omega(t, t_1 + t_2) + 2\phi(t_1) + \Delta\phi(t))]\right\}$$

(2.22)
Now solving the Equation 2.22 for the expected value operator ‘E’; breaking the Equation 2.22 into two parts for simplified solution. The expected values is defined by

\[ E \left( \int_{-\infty}^{\infty} f_X(x) \, dx \right) = \int_{-\infty}^{\infty} f_X(x) \, dx \]  

(2.23)

Where ‘ \( f(X) \) ’ is the PDF and for the Gaussian process it is given by Equation 2.24 as

\[ \text{PDF} = \frac{1}{\sigma_{\Delta\phi(t)} \sqrt{2\pi}} \exp \left( -\frac{\Delta\phi^2(t)}{2\sigma_{\Delta\phi}^2} \right) \]  

(2.24)

\[ E[\cos(\alpha_0(t_2 - t_1) + \Delta\phi(t))] = E[\cos(\alpha_0(t_2 - t_1))\cos\Delta\phi(t) - \sin((\alpha_0(t_2 - t_1))\sin\Delta\phi(t)] \]  

(2.25)

Solving for the expected value ‘E [ ]’ in Equation 2.25, by using the Equations 2.23 and 2.24. The solution is shown in the subsequent steps.

\[ E[\cos(\alpha_0(t_2 - t_1))\cos\Delta\phi(t)] = \cos(\alpha_0(t_2 - t_1))E[\cos\Delta\phi(t)] \]  

(2.26)

\[ E[\cos\Delta\phi(t)] = \int_{-\infty}^{\infty} \cos\Delta\phi(t) \frac{1}{\sigma_{\Delta\phi(t)} \sqrt{2\pi}} \exp \left( -\frac{\Delta\phi^2(t)}{2\sigma_{\Delta\phi}^2} \right) d(\Delta\phi(t)) = \exp \left( -\frac{\sigma_{\Delta\phi(t)}^2}{2} \right) \]  

(2.27)

Therefore simplified form of Equation 2.26 is given by

\[ \exp \left( -\frac{\sigma_{\Delta\phi(t)}^2}{2} \right) \cos(\alpha_0(t_2 - t_1)) \]  

(2.28)

Solving for the other half of Equation 2.25, first simplifying as shown in 2.29

\[-E[\sin((\alpha_0(t_2 - t_1))\sin\Delta\phi(t)]) = -\sin((\alpha_0(t_2 - t_1))E[\sin\Delta\phi(t)] \]  

(2.29)

\[ E[\sin\Delta\phi(t)] = \int_{-\infty}^{\infty} \sin\Delta\phi(t) \frac{1}{\sigma_{\Delta\phi(t)} \sqrt{2\pi}} \exp \left( -\frac{\Delta\phi^2(t)}{2\sigma_{\Delta\phi}^2} \right) d(\Delta\phi(t)) \rightarrow 0 \]  

(2.30)

The simplified form of Equation 2.25 is given by Equation 2.31

\[ E[\cos(\alpha_0(t_2 - t_1) + \Delta\phi(t))] = \exp \left( -\frac{\sigma_{\Delta\phi(t)}^2}{2} \right) \cos(\alpha_0(t_2 - t_1)) \]  

(2.31)

Now simplifying the other half of the main autocorrelation Equation, which is Equation 2.22; first finding the expected values of \( E[\cos(\alpha_0(t_2 + t_1) + 2\phi(t_1) + \Delta\phi(t))] \). The simplification is shown in the subsequent steps.

\[ E[\cos(\alpha_0(t_2 + t_1) + 2\phi(t_1) + \Delta\phi(t))] = E[\cos(\alpha_0(t_2 + t_1))\cos(2\phi(t_1) + \Delta\phi(t)) - \sin(\alpha_0(t_2 + t_1))\sin(2\phi(t_1) + \Delta\phi(t))] \]  

↓

\[ \cos(\alpha_0(t_2 + t_1))E[\cos(2\phi(t_1) + \Delta\phi(t))] - \sin(\alpha_0(t_2 + t_1))E[\sin(2\phi(t_1) + \Delta\phi(t))] \]  

↓

\[ \cos(\alpha_0(t_2 + t_1))E[\cos(2\phi(t_1))\cos(\Delta\phi(t)) - \sin(2\phi(t_1))\sin(\Delta\phi(t))] \]  

\[ - \sin(\alpha_0(t_2 + t_1))E[\sin(2\phi(t_1))\cos(\Delta\phi(t)) + \cos(2\phi(t_1))\sin(\Delta\phi(t))] \]  

(2.32)

Now further simplifying Equation 2.32 by using the results of Equations 2.27 and 2.30, the solution of 2.32 is given in the following steps.
An Oscillator System for UWB QDAcR

\[
\exp\left(-\frac{\sigma^2_{\Delta\phi(t)}}{2}\right)\{\cos(\omega_0(t_2 + t_1))E[\cos(2\phi(t_1))] - \sin(\omega_0(t_2 + t_1))E[\sin(2\phi(t_1))]| \right) \tag{2.33}
\]

Now solving the Equation 2.33 for the expected value operator ‘E’; breaking the Equation 2.33 into two parts for simplified solution.

‘\(\phi(t_1)\)’ is defined as net phase of the oscillation cycle at instance ‘\(t_1\)’ and \(t_1 \in [t_0, t_2]; t_0 \rightarrow -\infty\), therefore \(\phi(t_1)\) can be expressed as the phase change in the time period ‘\(t_2 - t_0\)’ or the value of \(\phi(t_1)\) can be approximated as \(\phi(t_1) = \Delta\phi(t_2) - \Delta\phi(t_0) = \Delta\phi(t); t \rightarrow -\infty\) OR \(E[\cos(2\phi(t_1))] = E[\cos(2\Delta\phi(t))]| \right)

\[
E[\cos(2\Delta\phi(t))] = \int_{-\infty}^{\infty} \cos(2\Delta\phi(t)) \frac{1}{\sigma_{\Delta\phi(t)} \sqrt{2\pi}} \exp\left(-\frac{4\Delta\phi^2(t)}{2\sigma^2_{\Delta\phi(t)}}\right) d(\Delta\phi(t)) \tag{2.34}
\]

Solving Equation 2.34 the same way as Equation 2.27, the solution is

\[
E[\cos(2\Delta\phi(t))] = \int_{-\infty}^{\infty} \cos(2\Delta\phi(t)) \frac{1}{\sigma_{\Delta\phi(t)} \sqrt{2\pi}} \exp\left(-\frac{4\Delta\phi^2(t)}{2\sigma^2_{\Delta\phi(t)}}\right) d(\Delta\phi(t)) = \frac{1}{2} \exp(-2\sigma^2_{\Delta\phi(t)}) \tag{2.35}
\]

In the final solution of Equation 2.35, the variance \(\sigma^2_{\Delta\phi(t)} \rightarrow \infty\) when lower limit of ‘\(t \rightarrow -\infty\)’. As explained in the reasoning of formulation of Equation 2.34 that the value of ‘\(t\)’ is upper bound with \(\text{max}(t) \rightarrow t_2\), which defines the range of phase perturbation ‘\(\Delta\phi(t)\)’. The variance ‘\(\sigma^2_{\Delta\phi(t)}\)’ of the perturbation is directly proportionate to the time or \(\sigma^2_{\Delta\phi(t)} \propto |t|; t \rightarrow -\infty\) therefore the final solution \(\frac{1}{2} \exp(-2\sigma^2_{\Delta\phi(t)}) \rightarrow 0\).

Similarly \(E[\sin(2\phi(t_1))]\) can be approximated with \(E[\sin(2\Delta\phi(t))]\) and as solved in Equation 2.30 the solution is given by \(E[\sin(2\phi(t_1))] = E[\sin(2\Delta\phi(t))] = 0\) \(\tag{2.36}\)

The Equation 2.33 in the simplified form can be written as shown in 2.37

\[
\lim_{\sigma_{\Delta\phi(t)} \rightarrow \infty} \exp\left(-\frac{\sigma^2_{\Delta\phi(t)}}{2}\right)\{\cos(\omega_0(t_2 + t_1)) \frac{1}{2} \exp(-2\sigma^2_{\Delta\phi(t)})\} = 0 \tag{2.37}
\]

The final solution of Equation 2.21 in a simplified is shown in Equation 2.38 below.

\[
C(t_1, t_2) = \frac{A^2}{2} \exp\left(-\frac{\sigma^2_{\Delta\phi(t)}}{2}\right) \cos(\omega_0(t_2 - t_1)) = \frac{A^2}{2} \cos(\omega_0(t_2 - t_1)) \exp\left(-\frac{\sigma^2_{\Delta\phi(t)}}{2}\right) \tag{2.38}
\]

The above Equation 2.38 is of prime importance, if we consider the process of autocorrelation and correlation. Firstly, for the case if we consider the correlation then \(A_{\phi}(t_1)\) & \(A_{\phi}(t_2)\) has to be considered distinctive, that is two different oscillation cycles initiated at time instances \(t_1\) & \(t_2\), therefore the correlation can only exist in time period \(t; \forall t \in [t_2, \infty]\), however if the results of Equation 2.32 and 2.38 are analyzed it shows that correlation factor \(\rho_{\phi_{x,y}}(t) \rightarrow 0; \forall t \in [t_2, \infty]\), this result also coincides with the result in [24], which says that phase noise perturbations have a Gaussian PDF and are uncorrelated. Second case, if we consider just autocorrelation then \(A_{\phi}(t_1)\) & \(A_{\phi}(t_2)\) are considered the response of a single oscillation cycle.
An Oscillator System for UWB QDaCR

at two different instances $t_i$ & $t_j$ then there exists a definite autocorrelation given by the solution of Equation 2.38. Therefore the approximation made earlier that $\phi_i(t) \& \phi_j(t)$ (and $\phi_i(t) \& \phi_j(t)$) are uncorrelated is proved mathematically correct. The same result as in Equation 2.38 can be inferred from [25] and section VIII (Equation 33) of [24]; which signifies that there does not exist any correlation between the two distinctive oscillation cycles, that is the oscillation cycles originated at different time instants do not have any correlation as the phase noise process is characterized as Markovian process or mathematically $R_{i_1,i_2}(t,\tau) = 0$; if $i \neq k$. However, there exist a definite autocorrelation as proved by Equation 2.38 and the similar results presented in correlation analysis in Equation 34 in [24], which mathematically gives the autocorrelation of an oscillation cycle at two distinctive time instances as $R_{i,k}(t,\tau) = \sum_{j=-\infty}^{\infty} X_{i,j} \exp(-ji\omega\tau) \exp(-\frac{1}{2} \omega^2 \tau^2)$; for every $i = k$. Also, the other main result conclusion from the above analysis is that excessive phase keeps on adding in the form of the correlation, which is present in the Oscillatory cycle.

Further deductions form the above obtained results are as follows. The perturbations present in the oscillator’s phase are of random nature and the value of perturbation associated with a particular oscillation cycle at any two given instances, that is for time ‘$t$’ and ‘$t + \tau_g$’ are different. If the in-phase (I) and quadrature components (Q) are derived from a single source and or correlated sources (in the case back gate connected / Injection locked Q-VCO), then there will be a definitive correlation between the phase and amplitude perturbations of in-phase and quadrature LO outputs for a given oscillation cycle at any time instance ‘$t$’, but no correlation between the in-phase and quadrature components generated at two distinctive time instances for e.g. I and Q responses at time ‘$t$’ and ‘$t + \tau_g$’.

The in-phase and quadrature outputs are correlated if and only if generated at the same instance of time ‘$t$’ and therefore, we can apply the equality of random variable theorem, which states that if the two random variables are equal if and only if the probability of their being different approaches zero, that is $P(x_{i_1} \neq x_{i_2}) = 0 \Rightarrow 0 < corr(x_{i_1},x_{i_2}) \leq 1 \Rightarrow x_{i_1} = \lambda x_{i_2}$ (incase of linear dependence between the two random variables). Where $P$ is the probability function, $corr(x_{i_1},x_{i_2})$ gives the correlation between the random variables $x_{i_1}$ and $x_{i_2}$ and where $\lambda$ is some constant. Therefore for a cycle that at any given instance ‘$t$’, providing the in-phase component and the quadrature component, the perturbations for one particular cycle will be correlated and linearly dependent. That is, for a single source generation or a correlated source generation the valid approximation will be $\langle \phi_i(t) \rangle = \lambda_i \langle \phi_i(t) \rangle$ and $\langle \phi_i(t) \rangle = \lambda_i \langle \phi_i(t) \rangle$, where ‘$\lambda_i$’ is linear scalar constant defining the correlation between the respective phase change for in-phase and quadrature components of an oscillator and as specified before $\langle \phi_i \rangle$ is the expected stochastic
value of the phase error between the In-Phase and Quadrature components. If any further perturbation in the phase induced in quadrature output, due to the mechanism of generation of the quadrature output signal is to be considered and integrated, then it can be expressed can be approximated with the random variable \( \phi \). then it can be estimated that \( \langle \phi \rangle = \langle \phi_i \rangle \) and \( \langle \phi_q \rangle = \langle \phi_i \rangle \); Therefore the expected values of the random perturbations in in-phase and quadrature phase components are equal that is \( E\langle f(\phi, \phi) \rangle = E\langle f(\phi, \phi) \rangle \).

2. Amplitude Perturbations Approximations: As described in [26], the response of a perturbed oscillator can be best described using the state-space or phase plane diagrams. Figure 2.3 below represents the state space of an oscillator in V-I plane, the response of the unperturbed oscillator is given by the perfect closed limit cycle, which represents a stable oscillator with a perfect periodicity. If at any instance ‘\( t_0 \)’ the oscillator is perturbed from its perfect periodic state, there occurs a change in amplitude which marked by \( \alpha(t_0) \) and change in the phase is \( \Delta\phi(t_0) \).

Figure 2.3: State-Space diagram of an oscillator in V-I plane

In Hajimiri-Lee Model [22] the change in amplitude is characterized by the amplitude impulse sensitivity function given by ‘\( \Lambda(\alpha(t)) \)’ and mathematically the change is given by \( \alpha(t) = \Lambda(\alpha(t)) \frac{\Delta V(t)}{V_0} \), where \( \Delta V(t) = V_0 - V(t) \) is the change in voltage due to instant perturbation, the modeling presented in [22] is based on heuristic and empirical treatment of the problem rather than quantitative and analytic. The amplitude impulse response ‘\( h_i(t, \tau) \)’ is given by Equation (4.36) in [22] which is reproduced here as Equation 2.39. Where ‘\( d(t - \tau) \)’ is exponentially decaying function and signify the excess amplitude, the decaying function is given by Equation 2.40 [Equation 4.44 in 22].
An Oscillator System for UWB QDAcR

\[ h_n(t, \tau) = \frac{N(\omega t)}{q_{\text{max}}} d(t-\tau) \quad (2.39) \]

\[ d(t-\tau) = e^{-\mu_t(t \tau)} u(t-\tau) \quad (2.40) \]

The same result as shown in Equation 2.42 below can be obtained by using the Floquet vectors theory for solving the differential algebraic Equation, describing the nonlinear oscillatory system [24]. The final solution for the perturbation in the amplitude is given by Equation 20 in [24], on analysis of this Equation it can be clearly verified that change in amplitude is directly dependent on integrand of Floquet periodic exponents over the time period ‘t’ and is given by Equation 2.41, where ‘\( \mu(t) \)’ is the Floquet exponent and \( \exp(\mu(t)) \) is called the characteristic multiplier. It can be deduced form the Equation 2.41 that the resultant change in the amplitude, which is given by ‘\( \alpha(t) \)’ decays exponentially with time and that the amplitude tends to rest back at the normal levels as the time increases. This mathematical analysis also bolsters the approximation made in this section in which the overall effect of amplitude perturbations on the phase noise characteristics is proved to be mathematically negligible.

\[ \alpha(t) \propto \sum_{i=0}^{n} \mu(i) \int_{0}^{t} \exp(\mu(i-r)).dr \tag{2.41} \]

Using the approximations presented in statements 1 and 2 in order to simplify Equation 2.19

By Equation 2.39, 2.40 and 2.41 it is clear that the amplitude change \( \alpha(t) \rightarrow 0 \) when \( t \rightarrow \tau \& \tau = (0, \infty) \)

therefore first approximating for amplitude perturbations effect in 2.19 by taking the response of QDAcR over a time period ‘t’

\[ \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ + \]

\[ \frac{A(t)^2}{A_0} \left\{ \cos(\phi(t) - \phi(t) - \omega \tau_a) + \cos(2(\omega - \omega) t - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ + \]

\[ \frac{A(t)^2}{A_0} \left\{ \cos(\phi(t) - \phi(t) - \omega \tau_a) + \cos(2(\omega - \omega) t - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]

\[ = \frac{A(t)^2}{A_0} \left\{ \cos(2(\omega - \omega) t - \omega \tau_a) + \cos(\phi(t) - \phi(t) - \omega \tau_a) \right\} \]
3. Approximations for the Phase Error: In this section the effect of phase error is heuristically calculated on the total autocorrelation of the QDAcR, as it can be calculated from 2.42 that at any instance the expected value of phase error can be quantized between the limits or mathematically as given by Equation 2.44

\[ E(\phi(t)) = (0, \pm 2\phi_0) \]  

(2.44)

The cause of phase error in the In-phase and Quadrature components is primarily associated with the process variations in the passives and devices manufacturing, which is stochastic in nature, for QDAcR the effect of phase error on the autocorrelation coefficient can be modeled heuristically, using the MATLAB modeling of QDAcR and inducing the phase error between the In-Phase and Quadrature components the change in the autocorrelation factor is measured. The graph plotted below shows the change in autocorrelation versus the phase error.

As it can be analyzed from the above graph that the maximum phase error of \( \phi_{\text{max}} \approx 17.5^\circ - 18^\circ \) is possible in order to have desirable autocorrelation factor in range of 100\% - 80\%, therefore in the worst case scenario the value of \( \phi_{\text{max}} \) possible is \( \approx 8.75^\circ \). The Equation can therefore be simplified further if by process and circuit design the possible maximum phase error can be fixed below 8.5\%. 

-36-
Now using the results obtained by the heuristic analysis in order to simplify the main time domain QDAcR Equation given by 2.41; let take \( K = \frac{A(t) - A_{io}}{8} \) (2.45)

Therefore the Equation 2.43 can be re-written as shown in Equation 2.46 below.

\[
K \left[ \cos(\phi(t) - \phi(t) - \omega z_1 \tau_d) + \cos(\phi(t) - \phi(t) - \omega z_1 \tau_d + 2\phi_{max}) \right]
+ K \left[ \cos(2(\omega z_1) - \omega z_1 \tau_d - \phi(t)) - \cos(2(\omega z_1) - \omega z_1 \tau_d - \phi(t) - \phi(t) + 2\phi_{max}) \right]
\]

The Equation 2.46 can be further simplified, if we limit the value of \( \langle \phi(t) \rangle \), that is the phase error should be as less as possible, as given by Equation 2.47, in which \( \lim_{\phi \to 0} \) and therefore we have Equation 2.47,

\[
\psi = 2(\omega z_1 - \omega z_1 \tau_d - \phi(t))
\]

where &
\[
\Phi = \phi(t) - \phi(t) - \omega z_1 \tau_d
\]

\[
\lim_{\phi \to 0} K \left\{ \cos(\Phi) + \cos(\Phi + 2\phi_{max}) \right\}
+ \lim_{\phi \to 0} K \left\{ \cos(\psi) - \cos(\psi + 2\phi_{max}) \right\}
\]

The final solution of time domain analysis of QDAcR, whilst considering the approximations (mathematically proven) and process non-idealities present in the downconverter is derived in Equation 2.47. The solution shows the dependence of the auto correlation on the time dependent phase present in the system due to the oscillator and the time delay.
The Equations 2.46 and its extremely simplified version, which is Equation 2.47, both provide distinctive merits over the all previous analysis presented so far, which are as follows:

1. The time domain analysis proves that the autocorrelation factor, which is of prime importance in QDAcR, is directly dependent upon the phase perturbations of an Oscillator, which is further characterized as the oscillator phase noise. The time domain analysis in itself provides the analysis for general homodyne and as well as heterodyne receiver architectures as a subset. The time domain analysis is not just limited to the QDAcR.

2. An accurate mathematical treatment of time domain analysis is presented; which, firstly characterize the nature of the perturbations that is ‘Stochastic’ and then rightly assess the effect of these perturbations. The mathematical model provides the scalability of characterizing the overall effect of noise, mismatch and process variations (which can be characterized as stochastic perturbations) for the mixer. E.g. if we wish to characterize the effect mismatching in the mixing, then by defining the effect of mismatch as one of the random variable in the solution Equation. At system level we can directly see the effect by plotting the results vs. the Expected or range bound (heuristic) value of the process stochastic variable.

3. A first insight into the circuit level design, firstly the empirical processing of phase error provides the answer as which circuit design method should be used in order to generate the In-Phase and Quadrature components and the amount of phase error that can be incorporated in the receiver in order to attain the desired auto-correlation levels.

4. This model can be easily extrapolated onto the Combined Auto-correlation Receiver (CAcR) architecture which is proposed in [23]. The final Equation at which we will arrive will be the same

2.4 Modeling of an Oscillator in QDAcR

The time domain analysis of QDAcR results in Equation 2.19 and 2.47, that shows the dependence of the autocorrelation on the phase and amplitude of a LO, that is dependence on ‘’ and ‘’ . In order to model an oscillator with all the non-idealities, the effects of the phase change on ‘’ should be modeled. The frequency domain uncertainties of LO are represented by random phase and change in the amplitude, due to the phase modulation (PM) and amplitude modulation (AM) present in the oscillator in frequency domain and as a measure of the oscillator performance these uncertainties are expressed as the spread of noise power spectrum around the central frequency / fundamental harmonic. While in time domain the uncertainties in an oscillator are combined denoted by the ‘Timing Jitter’ or simply called as ‘Jitter’. In circuit design the performance of the Local Oscillator is characterized by the phase noise, which is in the frequency domain, in order to model the LO, that is characterizing the sources of uncertainties and the effects of uncertainties in the frequency domain one must first understand the
dependence and transformation between the time domain and the frequency domain, that is the relationship between the ‘Jitter’ and the ‘Phase Noise’.

2.4.1 The Phase Noise Characterization: Basics and Noise Sources

The performance of an oscillator is characterized by the amount of power spread at a certain offset frequency around the carrier frequency or the fundamental tone (if carrier waveform is not sinusoidal) of the oscillator output and is measured in a bandwidth of 1 Hertz; As low the power spread, as close the performance will match the performance of an ideal oscillator. The power spread is measured through analyzing the RF spectrum of the oscillator; the spectrum is symmetric about the carrier frequency [27].

The voltage output of an oscillator is given by the Equation 2.48.

\[
V_{out}(t) = V_o(1 + \alpha(t)).\cos(\omega_f t + \phi(t))
\]

Where ‘\(V_{out}(t)\)’ is the output voltage at any time instance ‘\(t\)’ and ‘\(V_o\)’ is the maximum voltage swing possible for the LO output. The spread around the carrier frequency (the sidebands) is caused by the fluctuations in phase and amplitude, which are represented by ‘\(\phi(t)\)’ and ‘\(\alpha(t)\)’.

The power spectrum around the central frequency is resultant of the perturbations in the phase and the amplitude of the oscillator output, therefore the total power spectral density of the spectrum around oscillation frequency can be denoted as the sum of the noise power due to the phase and amplitude perturbations that is the noise power due to phase modulation (PM) and amplitude modulation (AM).

The measure of the performance of the oscillator is done in terms of the measure of single sideband noise spectrum power density at a certain offset frequency (and bandwidth of 1Hz.) from the carrier frequency and it is termed as ‘Phase Noise’, expressed in dBc\(\Delta\omega\) or \(L\{\Delta\omega\}\). Figure 2.5 shows the characterization of the phase noise.
Figure 2.5: The Power Spectrum of an Oscillator and Phase Noise power of the carrier at certain offset.

The power under the spread power spectrum as shown in the Figure 2.5 represents the total power, that is, power that includes the effect of both amplitude as well as phase uncertainties. The total effect of perturbations is given by the Equation 2.49:

\[ L_{\text{total}} \{ \Delta \omega \} = \log_{10} \left( \frac{P_{\text{sideband}} (\omega_0 + \Delta \omega, 1\,\text{Hz})}{P_{\text{carrier}}} \right) \]

Where ‘\( L_{\text{total}} \{ \Delta \omega \} \)’ is the total of the effect of phase and amplitude fluctuations, which is measured at an offset angular frequency of ‘\( \Delta \omega \)’, ‘\( P_{\text{sideband}} (\omega_0 + \Delta \omega, 1\,\text{Hz}) \)’ gives the SSB (single sideband) power at the offset frequency and ‘\( P_{\text{carrier}} \)’ represents the total power under the power spectrum [22].

The effect of amplitude noise can be reduced by amplitude limiting mechanism such as automatic gain control circuit to control amplifier gain or the finite supply voltage [27] and intrinsic nonlinearity of the device [22]. The amplitude restoring mechanism can be explained by the LTV impulse response model, which is described in [22]. As stated in [22] that if an ideal parallel LC tank oscillating at voltage amplitude \( V_{\text{out}}(t) = V_0 \) across the capacitor, is injected with an impulse of current and as a result there is sudden change (increase) in the voltage through the capacitor that is given by \( \Delta V(t) = \frac{\Delta q}{C_{\text{total}}} \), where \( \Delta q \) is the total charge injected by the current impulse and the total capacitance is given by \( C_{\text{total}} \). There will be only Voltage amplitude change given by \( \Delta V(t) \) if the current impulse is applied at the peak of voltage across the capacitor and only phase change given by \( \Delta \phi(t) \) if the current impulse is applied at zero crossing. At any instance ‘t’ the change in the amplitude and phase is shown by the Figure…the amplitude limiting mechanism of AGC and nonlinearity of devices can be treated closely to the change in the amplitude,
An Oscillator System for UWB QDAcR

which is proportional to the amplitude impulse function $\Lambda(\omega, t)$ and mathematically the change is given by $\alpha(t) = \Lambda(\omega, t) \frac{\Delta V(t)}{V_0}$, $\alpha(t) \to 0$ when $t \to \infty$ and $\phi(t) \to \Delta \phi(t)$ as $t \to \infty$.

![Figure 2.6: Phase perturbation due to charge injection](image)

The change in the phase due to the perturbation induced by current impulse is given by the Equation 2.50

$$\Delta \phi(t) = \Gamma(\omega, \tau) \frac{\Delta V}{V_{\text{max}}} = \Gamma(\omega, \tau) \frac{\Delta q}{q_{\text{max}}}$$  \hspace{1cm} (2.50)

Where the change in phase ‘$\Delta \phi(t)$’ is related to the

In [24] the overall effect of the perturbation in the amplitude is explained by considering it as an orbital deviation component of an oscillator. The nonlinear perturbation analysis provides the result that the orbital deviation is small at any give instance of time and further it confirms and adheres to the postulated amplitude stabilization given in [22]. Therefore for practical reasons we can consider $L_{\text{voul}} \{\Delta \omega\} = L \{\Delta \omega\}$, that is the total noise power present in the SSB spectrum can be equated with the noise power produced due to the phase modulation, which is commonly known as phase noise. The typical single sideband power spectrum for the phase noise in terms of $L \{\Delta \omega\}$ is shown in the Figure 2.5 The phase noise is given by the Equation 2.51; which is commonly known as Leeson’s Equation of phase noise; this Equation is to model phase noise, which is based on a linear time invariant (LTI) analysis of tuned tank oscillator[28],

$$L \{\Delta \omega\} = 10 \log \left( \frac{2FkT}{P_y} \left[1 + \left( \frac{\omega}{2Q \Delta \omega} \right)^2 \right] \right) \left[1 + \frac{\omega}{|\Delta \omega|} \right]$$  \hspace{1cm} (2.51)

Where $F$ is device excess noise number, ‘$k$’ is Boltzmann’s constant, ‘$T$’ the absolute temperature, $P_y$ is average power dissipated in the tank, $\omega$ and $\Delta \omega$ are the oscillation and the offset frequency and $Q$ is the quality factor of the loaded tank.
The sources of noise in an oscillator can be broadly classified in two categories; firstly, the noise produced by the active devices used in the Oscillator and secondly, by the resonator. On the basis of mechanism the noise present in an Oscillator can be further classified into (1) Thermal noise (2) Shot Noise and (3) Flicker Noise (1/f noise).

1. **Thermal Noise**: The noise caused by the Brownian motion of thermally agitated charge carriers in a conductor, which represents the randomly varying current and consequently the random voltage (via Ohm’s Law) [30], it is also commonly known as ‘White Noise’ or Johnson Noise’. The available noise power is given by the Equation $P_{na} = kT\Delta f$ where $k$ is Boltzmann’s constant, absolute temperature is given by ‘$T$’ and ‘$\Delta f$’ is the frequency bandwidth. The thermal noise has a constant energy per hertz or per required bandwidth. The thermal noise can be associated with the passive circuit components like resistor, where it is given by the Equation $P_{nR} = \frac{1}{2}kTR^2\Delta f$ or in terms of the current by $I^2_n = \frac{v^2}{R^2} = 4kTR\Delta f$

where $R$ is the resistance value and $G$ the conductance, the white noise is also associated with the real time inductors and capacitors (if we consider parasitic resistance). In active devices (MOSFET) the thermal noise is present in the form of drain current noise due to the resistive nature of the drain-source channel; however, in short channel NMOS the drain current noise is far exceeding from the normal values devised by long channel theory; it is due to the role played by the thermal noise produced by the substrate, the substrate can be modeled in terms of simple resistive [29] or as done in [30] as a RC circuit, therefore the excess current noise measured is due to the substrate current noise. The thermal noise can be further associated to the gate noise in MOSFET due to resistive poly gate [29], which is negligible at low frequencies, however can dominate at radio frequencies[30]; the thermal noise is present as a base resistance noise in BJT, which is a major source of thermal noise in BJT and the noise voltage across the base resistance $r_b$ is given as $v^2_b = 4kTR_b\Delta f$, the ‘thermal noise’ can be characterized as the ‘Gaussian Noise’ as amplitude of the thermal noise follows a Gaussian distribution [30].

2. **Shot Noise**: The shot noise can be described as the noise produced by the direct current flowing through a junction that acts as a potential barrier; the randomness is caused by the hopping of the electrons over the potential barrier arriving at the random time. This randomness in the arrival time gives rise to white noise nature of the shot noise, which gets worst with the increase in average current through the junction or increase in the bandwidth. The ‘Shot Noise’ is given by the Equation $I^2_n = 2qI_{dc}\Delta f$, where $I_n$ is the rms noise current, $q$ is electronic charge, $I_{dc}$ is the DC current and $\Delta f$ is the noise bandwidth [30]. The shot noise is a major contributor in the overall noise of bipolar junction transistor, collector current shot noise is given by $I^2_c = 2qI_{dc}\Delta f$ and the shot noise due to the base current, which can become dominant at the radio frequencies and is given by $I^2_b = 2qI_{bc}\Delta f$ however, it is the partial but major component in the total base
noise present in a BJT. The amplitude of the shot noise also follows the Gaussian distribution, as it is similar to the white noise or thermal noise. In MOSFET the shot noise is present in the form of gate leakage current which is given by noise gate current \( i_n^2 = 2qI_n \Delta f \), it becomes significant at radio frequencies or when driven by a high source impedance; besides the shot noise both MOSFET and BJT gate/base consists of flicker and burst noise.

3. **Flicker Noise**: This noise is also known as the ‘1/f’ or ‘pink’ or ‘colored’ noise; the flicker noise has the spectral density which increases with decrease in the frequency, therefore mathematically it is given as \( 1/f^n \), where the index ‘\( n \)’ attains value in the region \( 0 < n \leq 4 \) as described in [31] and it is associated with the roughness distribution of a signal. Furthermore, as illustrated in [31] that in an one-dimensional system for \( n = \{1, 2, 4\} \) the periodic behaviour of flicker noise is seen and for \( n \rightarrow 1 \) the flicker noise behaviour can be associated with the physical phenomenon of voltage fluctuation in a resistor when current is flowing through it. Therefore, the flicker noise in an electrical circuitry can be appropriately described by the following Equation, specified in [30] as \( N^2 = K f^n \Delta f \), where \( N \) is the rms noise, that can be either voltage or current, \( K \) is an empirical parameter it is biased dependent and device specific and ‘\( n \)’ is an exponent close to the unity [30] and in [32] the exponent \( n = 1 \pm 0.2 \). There have been reported several mechanism for the generation of flicker noise in [32] and [29], also among the all semiconductor devise the MOS exhibits the highest amount of flicker noise due to their surface conduction mechanism [29]. In [30] it is stated that flicker noise is a major noise source in MOSFET, as it is most sensitive to the surface phenomenon or the roughness of the surface. One of the measures for the flicker noise is done by measuring the corner frequency of the device that is the frequency where the flicker noise component power spectral density (PSD) is equal to the PSD levels of total of thermal and shot noise under the ceteris paribus conditions. The MOSFET devices (surface devices) are highly sensitive to the surface phenomenon because of the way they are fabricated, which translates into the fact that the corner frequency in MOSFETs is many times higher than the corner frequency of BJT, which are considered to be bulk devices by the way of fabrication; in MOSFET the mean-square 1/f drain noise is given by \( i_n^2 = K g_m^2 \omega L(WC_{ox})^2 \Delta f = K g_m^2 \omega L(WL\Delta f) \), where \( W \) is the width of the MOS, \( L \) is the channel length and \( \omega \) is the MOS cut-off frequency. The 1/f noise in NMOS is typically 50times larger than for PMOS devices [29, 30]; in MOS devices the 1/f noise corners occurs generally between kilohertz to megahertz and even in gigahertz range, while in bipolar from few tens of hertz to hundreds of hertz [30]. The flicker noise is present in the resistor if there is DC current flowing through it and this the cause of excess noise found in resistor apart from thermal noise [30]. The flicker noise is given by 1/f^n, can be characterized by different distributions for different values of the noise index ‘\( n \)’ as shown in [31]. The region
An Oscillator System for UWB QDAcR

corresponding to the electrical flicker noise and point of interest is when \( n \rightarrow 1 \), for values of \( n \leq \frac{1}{2} \) the flicker noise can be characterized by the Gaussian distribution and as \( n \) deviates there is noticed a difference from normal Gaussian distribution. The power spectrum density of flicker noise is characterized by the multiple Lorentzian spectra [33]; the singularity arises in the spectrum for \( n = 1 \), therefore the spectrum is given by Equation 18 in [33]. The other type of noise source, which exhibits the sensitivity similar to the \( 1/f \) noise, is burst noise or popcorn noise and as stated in [33] for the flicker noise the burst noise also mostly exhibits a multiple Lorentzian spectrum and the spectral density of burst noise is mathematically given by equation 31 in [34] as

\[
S_{burst}(f) = K \frac{i^n}{1 + \left( \frac{f}{f_c} \right)^2}
\]

where ‘\( K \)’ is a device constant, ‘\( f \)’ and ‘\( f_c \)’ are the central and 3dB cut-off frequencies of the Lorentzian Spectrum, ‘\( i \)’ the device current and ‘\( n, 0.5 \leq n \leq 2 \)’ is the exponent for the colored noise.

2.4.2 The Phase Noise Characterization: Noise Distribution in a Single Sideband Spectrum

The single sideband phase noise spectrum of an oscillator can be best plotted as shown in the Figure 2.7

![Figure 2.7: The Single Side Band Spectrum of and Oscillator](image)

As it is shown in the Figure 2.7 that ssb phase noise spectrum consists of mainly three frequency region marked by \( 1/f^1 \), \( 1/f^2 \) and \( 1/f^0 \) these regions are characterized by type of noise source they represent, in depth study dealing with the characterization of the noises present in an oscillator has been done and the types of noises influencing each region can be characterized as follows.
1. The most important region in single sideband phase noise spectrum plot i.e. \( L\{\Delta \omega \} \) Vs. \( \Delta \omega \) Plot is the \( 1/f^2 \) noise region; it represents all the white noise (white and modulated white noise) generated in the oscillator. The characterization of the \( 1/f^2 \) noise is very well presented in [24] and it is termed as ‘the unifying theory’, which characterizes all the uncorrelated white noise sources and their effect on the oscillator performance. The phase change is stochastically characterized in the time domain by calculating the time-varying probability density function (PDF) of the phase change, this characterization results that the phase change \( \Delta \phi(t) \) becomes asymptotically with time a Gaussian random variable, with a constant mean \( (\mu) \) and linearly increasing time dependent variance \( \sigma^2(t) \) and \( \sigma^2(t) = ct \), where ‘c’ is a scalar constant. In the spectrum analysis of the oscillator output, the unifying theory states that the phase deviation \( \phi(t) \) changes the power spectral density in the frequency domain; however, the total power of the periodic oscillator signal remains conserved. In frequency domain the PSD of an ideal oscillating signal can be replicated by the Dirac Delta function \( \delta(\omega) \), where the PSD levels take the shape of an impulse function at central frequency and harmonics, the effect of phase deviation in the frequency domain is that it spreads the spectral power given by \( \delta(\omega) \) functions at all harmonics; however the total spectrum power remains the same [24]. The phase noise due to total white noise that is the total \( 1/f^2 \) noise spectrum in a single sideband phase noise plot can be shown as in Figure 2.7; the \( 1/f^2 \) region is marked by the \(-20dB/dec\) noise slope. The phase noise is given by the Equation 2.52, for the approximation that \( 0 \leq \Delta \omega \ll \omega \) and small values of ‘c’.

\[
L\{\Delta \omega \} \equiv 10 \log \left( \frac{\omega^2 c}{\omega^2 c^2 + \Delta \omega^2} \right)
\]

(2.52)

The unifying theory [24] even deals with the shortcomings of the Leeson’s LTI phase noise model which is given in Equation 2.51. If we consider Equation 2.51 and look for behaviour of the SSB phase noise spectrum the offset frequencies approaching the carrier frequency that is \( \Delta \omega \rightarrow 0 \), the solution of Equation 2.51 provides with an infinite noise power density at the carrier which is not accurate. The Equation 2.52 can be equated to the Lorentzian spectrum as shown in Equation 2.53, where ‘\( f_o \)’ is the oscillation frequency and ‘\( \Delta f \)’ is offset frequency at which the phase noise is measured.

\[
L\{\Delta \omega \} \equiv 10 \log \left( \frac{\omega^2 c}{\omega^2 c^2 + \Delta \omega^2} \right) \quad \Rightarrow \quad L\{\Delta f \} \equiv 10 \log \left( \frac{\pi f_o^2 c}{(\pi f_o^2 c^2 + \Delta f^2)} \right)
\]

(2.53)

Furthermore, it can be proved quantitatively that the total power of the phase noise spectrum is conserved and that phase perturbation causes the spread around the harmonics. As the integral of the Equation 2.53 which exhibits the Lorentzian spectrum has a finite value of ‘1’ between minus infinity to the plus infinity
that is \[ \int_{-\infty}^{\infty} L(\Delta\omega) = 1. \] In [35] the power spectral density of noise component due to white noise or the spectrum shown by \(1/f^2\) region, is characterized by high frequency variations in the feedback loop and is given by the Lorentzian function; the feedback loop consists of a frequency select resonator, which filters the undesired noise components and the selective output is provided back to the input of the active device that acts as an amplifier [27].

2. The frequency modulated flicker noise or \(1/f\) noise component is represented by \(1/f^3\) region as marked in the Figure 2.7. There have been several attempts to characterize the effect of flicker noise in an oscillator spectrum; the credible studies are [34, 35, 22]. In [34] the \(1/f\) noise is treated as a special case of the colored noise, where the colored and correlated noise is characterized stochastically, representing it by a one-dimensional Gaussian distributed process with the approximation that the bandwidth of the colored noise source is significantly smaller than the oscillation frequency, to simplify the modeling the colored noise sources are assumed to be auto-correlated only, that is uncorrelated with each other. The [34] treats \(1/f\) noise as a stationary stochastic process, which attains a finite value at \(f = 0\) and deviates from the characterized Lorentzian spectrum below the cut-off frequency \('\gamma_c'\); the spectrum is defined as a function of the 3-db bandwidth \('\gamma'\) and the process operation frequency \('f'\). The spectrum of the \(1/f\) noise is given by \(S_{\nu_f}\) as in Equation (38) in [34], which is \(S_{\nu_f} = \frac{4}{\gamma_c^3} (2\pi f)^2 d\gamma\) and signifies that the spectral density contribution due to \(1/f\) noise is pronounced at the low frequencies near the fundamental frequency of the oscillator and the value of spectrum at \(f = 0\) is given by \(S_{\nu_f}(0) = \frac{4}{\gamma_c}\). The behaviour, which in Figure 2.7 is marked by \(1/f^3\) and is given by -30dB/dec slope and the cutoff frequency if marked by the point where \(1/f^3\) and \(1/f^2\) regions meet, this point as stated previously is commonly called as \(1/f\) corner (it is not same as the \(1/f\) corner frequency of the device). However, in the calculation of phase noise spectrum due to \(1/f\) noise, the approximations in defining the flicker noise spectra are taken; firstly, that is the \(1/f\) noise is a stationary stochastic process, which is bounded in an interval of time, that is classified as ‘Relaxation time’ in [33], this allows to define the continuous spectra \(1/f\) noise over a certain bandwidth defined by the relaxation time interval [33] and which is same as the limits from cut-off frequency to infinity as stated in Equation (38) [34] and Secondly that in the single side band phase noise spectra the power due to \(1/f\) noise is concentrated at the low frequencies [34].

3. The device flicker noise or \(1/f\) noise component: As we have noticed that as the channel length is decreasing the device own \(1/f\) increase and for NMOS and other contemporary technologies it extends to
An Oscillator System for UWB QDAcR

few Megahertz. Therefore, the unmodulated component of the device flicker noise is dominant and it’s
effect is seen at the lower frequencies. As shown in Figure 2.7 the device flicker noise does provide a roll
off with 10dB/decade and is effective at low frequencies level.

2.4.3 Modeling of Oscillator in time domain (Jitter and Phase Noise
crossover)

The effect of uncertainties in an Oscillator can be illustrated in terms of ‘Jitter or Clock Timing Jitter’ in the
time domain, which corresponds to the ‘Phase Noise’ in frequency domain. The Jitter can be broadly
described as the difference between the zero-crossing / transition times of a signal and the absolute value of
the signal time period over a specified time interval; therefore ‘Jitter’ can be classified as the deviation in
the period of a signal over the certain time interval. The Figure 2.8 represents the jitter present in a signal of
mean time period ’ \( T_0 \)' & \( T_n \) = \( \frac{T_0 + T_1 + T_2 + \ldots + T_{n-1} + T_n}{n} \) = \( \frac{1}{f_0} \), where \( f_0 \) is the fundamental and unperturbed
oscillation frequency. The various types of jitter are given by \( \Delta T_1, \Delta T_2, \Delta T_n \) & \( \Delta T_{n+1} \).

![Figure 2.8: The various types of Jitters present in a oscillating signal](image)

In case of an Oscillator these variations occur in each and every cycle and are caused by noise, which in
time domain is translated to ‘jitter’ or can be termed as noise induced jitter. The jitter produced by the noise
in any system is a random variable and can be characterized stochastically in a similar fashion as the noise
in an oscillator. The phase noise dependent jitter can also be classed as an Ergodic Process which also
follows the Gaussian distribution.

The jitter in an Oscillatory system is generally characterized as 1) Absolute Jitter and 2) Cycle Jitter and 3)
Cycle to Cycle Jitter on basis of time of observation.

1. **Absolute Jitter:** The term absolute jitter is associated with the jitter that has been accumulated over a
period of time. As shown in the Figure 2.8 the jitter values \( \Delta T_n \) & \( \Delta T_{n+1} \) are the values associated
with \( n^{th} \) & \( n+1^{th} \) cycles respectively. The jitter \( \Delta T_n \) in the \( n^{th} \) cycle acts as a source for the jitter \( \Delta T_{n+1} \) present
in the $n+1$th cycle, similarly accumulated effect of jitters present in all the previous cycles can be seen in the corresponding oscillation cycle. This shows that jitter once induced in the system can not be get rid off and it keeps on adding due to the non-idealities present in the circuit. Therefore, absolute jitter is also termed as long term jitter and the numerical value of the absolute jitter $\Delta T_{abs}$ is given by the Equation 2.54 below.

$$\Delta T_{abs, K^n} = \sum_{n=1}^{K} \Delta T_n$$  \hspace{1cm} (2.54)

The jitter induced by the phase noise in a circuit is a stochastic quantity, taking in to the account the above Equation 2.54, the standard deviation $\sigma_{abs}(t)$ and the variance $\sigma_{abs}^2(t)$ present in absolute jitter are given by the Equation 2.55 below. The absolute jitter is of importance in describing the jitter induced in a phase lock loop, because the total jitter translates into the total phase error produced in a certain time $t$ and corrected by the phase lock loop.

$$\sigma_{abs}(t) = \sum_{n=1}^{K} (T_n - T_0) \quad \text{and} \quad \sigma_{abs}^2(t) = \left( \sum_{n=1}^{K} (T_n - T_0) \right)^2$$  \hspace{1cm} (2.55)

2. Cyclic Jitter: Cycle Jitter is commonly known as rms (root mean squared) cycle jitter, this rms cycle jitter is a measure of the magnitude of the perturbation in one particular period when compared with the mean period $(T_0)$. Mathematically it is given by the Equation 2.56 below. Where $\Delta T_{cyc}$ is the rms cycle jitter present in the $K^{th}$ cycle. The standard deviation $\sigma_{cyc}(t)$ and the variance $\sigma_{cyc}^2(t)$ present in rms cycle jitter are given by equation 2.57

$$\Delta T_{cyc} = \lim_{K \rightarrow \infty} \sqrt{\frac{1}{K} \sum_{n=1}^{K} \Delta T_n^2}$$  \hspace{1cm} (2.56)

$$\sigma_{cyc}(t) = \lim_{K \rightarrow \infty} \sqrt{\frac{1}{K} \sum_{n=1}^{K} (T_n - T_0)^2} \quad \text{and} \quad \sigma_{cyc}^2(t) = \lim_{K \rightarrow \infty} \left( \frac{1}{K} \sum_{n=1}^{K} (T_n - T_0)^2 \right)$$  \hspace{1cm} (2.57)

3. Cycle to Cycle Jitter: The cycle to cycle jitter is defined as the time period difference between the two consecutive cycles, the difference between the two consecutive cycles provides the magnitude as well as the actual effects the short term perturbations, as a result of white noise and uncorrelated Gaussian distributed noise sources, which is seen as $1/f^2$ noise power in the frequency spectrum. Therefore, mathematically cycle to cycle jitter can be written as given by Equation 2.58

$$\Delta T_{cc} = \lim_{K \rightarrow \infty} \sqrt{\frac{1}{K} \sum_{n=1}^{K} (\Delta T_{n+1}^2 - \Delta T_n^2)} \Rightarrow \lim_{K \rightarrow \infty} \sqrt{\frac{1}{K} \sum_{n=1}^{K} (\Delta T_{n+1}^2 + \Delta T_n^2 - 2\Delta T_{n+1}\Delta T_n)} \Rightarrow \sqrt{2}\Delta T_{cyc}$$  \hspace{1cm} (2.58)
An Oscillator System for UWB QDAcR

In the Equation 2.58 the product terms are neglected and the relationship between cycle and cycle to cycle jitter is obtained. Similarly, the variance and standard deviation can be obtained as shown in Equation. 2.59

\[
\sigma_{cc}^2 = \lim_{k \to \infty} \frac{1}{K} \sum_{n=1}^{K} ((T_{n+1} - T_n) - (T_c - T_n))^2 = \lim_{k \to \infty} \frac{1}{K} \sum_{n=1}^{K} (T_{n+1} - T_n)^2 + (T_c - T_n)^2
\]  

(2.59)

Neglecting the product terms in the Equation 2.59. The above Equation can be considered as the sum of cyclic variances in two consecutive cycles, therefore mathematically it can be expressed as shown in Equation 2.60

\[
\sigma_{cc}^2 (t) = 2 \sigma_{c}^2 (t)
\]  

(2.60)

The stochastic nature of the jitter can be explained by defining the mathematical relationship between the jitter and phase noise. Considering very first Equation of an oscillatory motion given by Equation 2.3 and in this neglecting the amplitude perturbations, therefore the new Equation can be re-written as

\[
A_{out} (t) = A_n \cdot \cos(\omega t + \phi(t))
\]  

(2.61)

Considering the small change in the angular frequency' \( \Delta \omega(t) \)' because of the small phase perturbation \( \Delta \phi(t) \) and neglecting the amplitude perturbations that is considering \( A_{out}(t) = A_n \); then the excess phase can be related to excess angular frequency as in Equation 2.63

\[
A_{out} (t + \Delta t) = A_n \cdot \lim_{\Delta(\omega, \phi(t), t) \to 0} \cos((\omega_n + \Delta \omega) t + \phi(t) + \Delta \phi(t))
\]

\[
= A_n \cdot \lim_{\Delta(\omega, \phi(t), t) \to 0} \{ \cos(\omega_n t + \phi(t)) \cos(\Delta \omega t + \Delta \phi(t)) - \sin(\omega_n t + \phi(t)) \sin(\Delta \omega t + \Delta \phi(t)) \}
\]

\[
= A_n \cdot \lim_{\Delta(\omega, \phi(t), t) \to 0} \cos(\omega_n t + \phi(t)) \cos(\Delta \omega t + \Delta \phi(t))
\]

\[
\frac{A_{out} (t + \Delta t)}{A_{out} (t)} \to 1
\]

\[
1 = \lim_{\Delta(\omega, \phi(t), t) \to 0} \cos(\Delta \omega t + \Delta \phi(t)) \Rightarrow \Delta \omega t + \Delta \phi(t) = 2n\pi
\]

\[
\Delta \omega(t) = \int \Delta \phi(t)d\tau \Rightarrow \phi(t) = \int_0^t \Delta \omega(\tau)d\tau + \phi(0)
\]  

(2.63)

By using the above mentioned Equation...the time varying excess phase \( \Delta \phi(t) \) associated with the \( n^{th} \) period which is directly related to the jitter produced in the \( n^{th} \) period is expressed mathematically as

\[
\Delta T_n = \Delta \phi(t) \frac{T_n}{2\pi}
\]

Similarly, the cycle jitter can be expressed in terms of cyclic phase perturbation \( \Delta \phi_c(t) \),

where \( \Delta \phi(t) = \lim_{k \to \infty} \frac{1}{K} \sum_{n=1}^{K} \Delta \phi_n^2(t) \), therefore

\[
\Delta T_c = \Delta \phi(t) \frac{T_c}{2\pi} = \Delta T_{cc} = \Delta \phi(t) \frac{T_c}{2\sqrt{2\pi}}
\]  

(2.64)
Similarly, the variances in time and frequency domain have the mathematical relationship as defined by Equation 2.65 below.

\[
\sigma^2(t) = \lim_{k \to \infty} \left( \frac{1}{K} \sum_{n=1}^{K} (\Delta \phi(t) - \frac{T_n}{2\pi} \phi_0)^2 \right) = \frac{1}{\omega_0^2} \lim_{k \to \infty} \left( \frac{1}{K} \sum_{n=1}^{K} (\Delta \phi(t) - \phi_0)^2 \right) = \frac{\sigma^2_c}{\omega_0^2} \tag{2.65}
\]

\[
\sigma^2_{\omega}(t) = \frac{2\sigma^2_c}{\omega_0} \Rightarrow \sigma^2_{\omega}(t) = \frac{\sigma^2_c(t) \omega_0^2}{2} \tag{2.66}
\]

Extending the deduced results of section 2.3 to the above Equations numbered 2.66, as the phase perturbation follows the Gaussian distribution and it is proved that the jitter and phase perturbation are linearly dependent. Then by the theorem that if two random variables are linearly dependent and one of them follows Gaussian distribution then other random variable can also be characterized by Gaussian distribution, which is mathematically expressed as for two random variables \( x_i \) and \( x_n \) and considering \( x_i \) to be Gaussian distributed

Theorem (corollary): If \( a_i x_i = a_n x_n \) for any linear constants \( a_i \) and \( a_n \); while \( x_i \) is having Gaussian distribution then it implies that random variable \( x_n \) can also be characterized by Gaussian distribution.

This theorem serves as a corollary to theorem 7.2 in [24]. Therefore, the extrapolated results show that the timing jitter produced in an oscillator does have Gaussian distribution. In the same fashion it can be deduced that the production of timing jitter is an Ergodic process, which in turn justifies the accumulation of the time jitter and corresponding stationary stochastic behavior of phase deviation.

For the time domain modeling of the phase noise, next step is to calculate the relationship between the timing jitter and the phase noise. Firstly, describing the power spectrum density for determining the phase noise. As described in the section 2.4.1 and 2.4.2 the phase noise is given by Equation 2.49. Mathematically it can be derived by starting with the interchangeable relationship between the autocorrelation and the spectral power density, which is given by Weiner-Khinchin theorem, shown as Equation below

\[
C(\tau) = \int_{-\infty}^{\infty} S(\omega) e^{i\omega \tau} d\omega
\]

\[
S(\omega) = \int_{-\infty}^{\infty} C(\tau) e^{-i\omega \tau} d\tau
\]

Using the Einstein diffusivity Equation as described in Equations numbered 13 and 29 in [26] in Equation numbered 2.38, the correlation can be defined in terms of the diffusion coefficient ‘D’ as given by Equation 2.68 below.

\[
C(\tau) = \frac{A^2_t}{2} \cos(\omega_0 \tau) \exp \left( -D_0 |\tau| \right) \tag{2.68}
\]

Now using the Weiner-Khinchin theorem as given by Equation (i), the PSD is given by Equation 2.69 below

\[
S(\omega) = \int_{-\infty}^{\infty} \frac{A^2_t}{2} \cos(\omega_0 \tau) \exp \left( -D_0 |\tau| \right) \exp^{-i\omega \tau} d\tau
\]

\[
\text{-50-}
\]
The solution of the Equation 2.69 is a well known one and given in [25, 26, 28], therefore the value of PSD is

$$S(\omega) = \frac{A_0^2}{2} \frac{D_\phi}{(\omega - \omega_0)^2 + D_\phi^2}$$  \hspace{1cm} (2.70)$$

The single side band spectrum density is given by 'S_{ss}(\omega)' and it is mathematically given as

$$S_{ss}(\omega) = 2S(\omega) = A_0^2 \frac{D_\phi}{(\omega - \omega_0)^2 + D_\phi^2}$$  \hspace{1cm} (2.71)$$

The total PSD by white noise sources (1/f^2) as given by Equation 37 in [24], therefore 'P_{tot}' can be approximated as shown in Equation 2.72 below

$$P_{tot} = \int_0^\infty S_{ss}(\omega)d\omega = 2A_0^2$$  \hspace{1cm} (2.72)$$

Therefore, the phase noise having the Lorentzian distribution as given in 2.49 at an offset frequency \(\Delta \omega\) can be expressed as given by Equation 2.73 below

$$L_{total}\{\Delta \omega\} = 10\log\left(\frac{2D_\phi}{\Delta \omega^2 + D_\phi^2}\right)$$  \hspace{1cm} (2.73)$$

Applying the approximation that as applied in Equation 2.52 that is \(\Delta \omega \gg D_\phi\), the phase noise is given by the Equation 2.74

$$L_{total}\{\Delta \omega\} \approx 10\log\left(\frac{2D_\phi}{\Delta \omega^2}\right) \Rightarrow 10^{-\frac{L_{total}\{\Delta \omega\}}{10}} = \frac{2D_\phi}{\Delta \omega^2}$$  \hspace{1cm} (2.74)$$

For defining the phase noise in time domain by using the Equations number 2, 29 & 30 from [26], we define

$$\sigma^2_{\phi,\Delta \omega}(t) = \frac{2}{k} \sum_{k=1}^{n_k} (D_{\phi_{k}})_{\Delta \omega_{k}}$$  \hspace{1cm} (2.75)$$

Ensemble over a finite time period, which means that \(\sum_{k=1}^{n_k} \frac{t_k}{k} \rightarrow T_0\), combining the above Equation with Equation 2.74 & 2.75, the very important relationship between the cycle to cycle jitter variance and the phase noise is given by the Equation number 2.76

$$10^{-\frac{L_{total}\{\Delta \omega\}}{10}} = \frac{\alpha_0^2}{4\pi \Delta \omega^2} \sigma^2_{\phi}(t) \Rightarrow L_{total}\{\Delta \omega\} = 10\log\left(\frac{\alpha_0^2 \sigma^2_{\phi}(t)}{4\pi \Delta \omega^2}\right) = 10\log\left(\frac{\alpha_0^2 \sigma^2_{\phi}(t)}{2\pi \Delta \omega^2}\right)$$  \hspace{1cm} (2.76)$$

The above Equation 2.76 holds importance as it serves the basis for the modeling of the micro noise source in QDAcR in time domain. The result deduced in the above Equation is a well known one and is in complete uniformity with other similar results [24, 36, 37, 38]; however this proof presented here defines the relationship between the jitter and phase noise, while characterizing them as dependent stochastic variables and describing the mathematical relationship between the Cycle to Cycle jitter and phase noise. This relationship depicts and conforms fully to the Phase Noise stochastic mathematical characterization.
and the relationship between the Timing Jitter and phase noise is used for modeling in MATLAB for the purpose of modeling a real oscillator for QDAcR.

The Equation models the phase noise produced by the white uncorrelated/correlated (modulated) noise sources in an Oscillator, which is given by $1/f^2$ region in the oscillator power spectrum. As explained in the section 2.4.2 that for the wideband systems and the system where the intermodulated signals as well spurs either can be filtered or do not put stringent phase noise condition on the system the spectral density can be estimated by white noise (un-correlated/correlated) spectral power density model only; therefore the effect of $1/f^3$ region in the Oscillator power spectrum can be discounted for the purpose of system modeling and in particular for the QDAcR.

Therefore, for the ir-UWB QDAcR system the total phase noise is modeled as the total amount of phase noise generated by the white noise sources and given by $1/f^2$ region in the oscillator power spectrum. Approximation of the total phase noise using simply $1/f^2$ region indeed is a good estimation technique for the wideband systems, which suits best to the wideband ‘Zero IF’ and even multiple band switching wideband ‘(Super) Heterodyne’ receiver architectures.

### 2.5 Conclusion

In this chapter, we presented an in-depth mathematical analysis of phase noise with respect to QDAcR. The rigorous analysis is based on non-linear time variant system theory, which is extended to stationary stochastic process like white noise. We derived a complex model, which captures the noise/jitter related non-idealities of QDAcR and the same analysis can be extrapolated to other zero-IF or homodyne receiver architecture systems by adjusting the limiting quantities. The study of phase noise as physical process and its stochastic behaviour helped us in better understanding of phase noise and time jitter relationship. This well-known relationship serves as building block for time domain oscillator model, which will be used to find the specifications related to QDAcR downconverter.
3 CHAPTER 3
System Analysis and Modeling of QDAcR

3.1 Introduction
In this chapter, we further build upon the derivations and results deduced from the previous chapter. Starting with modeling of a real oscillator with all phase as well as amplitude perturbation incorporated. It is followed by understanding of QDAcR architecture and its limitations pertaining to total phase error, linearity and noise issues. As a solution a new architecture of QDAcR with added filters is proposed, this change not just eases the operational constraints but also increases the bandwidth usage to 76% of FCC allowed mask. The next section contains the complete modeling of QDAcR in MATLAB, the different pulse shapes were exploited for their interference resistance and as for which pulse highest correlation can be achieved for same phase noise. This leads to an extremely important result as how much phase noise is required in order to have desirable autocorrelation. Also, the analysis of LNA noise factor dependence on autocorrelation is presented.

3.2 Designing and Simulation of the Oscillator in MATLAB
The mathematical model of an Oscillator in the frequency and time domain is being presented in section 2.4, in this section the mathematical model of phase noise in time domain is being implemented in MATLAB and SIMULINK. The phase noise model in the time domain is based on the relationship between time jitter and phase noise, which is illustrated in the Equation 2.76. The oscillator is modeled as an integrated Gaussian distributed macro noise source. The block diagram of Oscillator phase noise model in Matlab is presented in the Figure 3.1. The Oscillator model consists of the following building blocks.

1. The Source / Oscillator: This block consists of Sinusoid signal generator, generating a continuous sinusoidal signal at a specified frequency of \( \omega_0 \) with amplitude of \( A_0 \) and constant phase of \( \phi_0(t) \). Mathematically it is given by \( A_{out}(t) = A_0 \cos(\omega_0 t + \phi_0(t)) \).
2. The integrated Micro Noise source block is represented as AWGN Channel, which stands for additive white Gaussian Noise channel. This represents the combined (integrated) noise effect of the white modulated/un-modulated noise sources present in an Oscillator. The AWGN represents for the random Gaussian noisy channel, when the signal is passed through the AWGN Channel the randomness is introduced in the oscillator signal, this randomness can be seen as the perturbation in the phase as well as the amplitude of the oscillator signal, as proved earlier settling of the amplitude perturbation the block can be estimated with Gaussianly distributed phase perturbation only.

The amount of perturbation which finally translates into the phase noise induced in the QDAcR Oscillator spectrum is controlled from the AWGN Block by varying the variance parameter based on the relationship given by the Equation 2.76. The Gaussian distributed variance is Cyclic Jitter as described in the section 2.4.3, as it can be seen from the block diagram in Figure 3.1 above that the difference between the perturbed and the fundamental signal at instance ‘t’ is measured, which totally coincides with the definition of the cyclic jitter. In calculations the cyclic jitter is replaced by the cycle-to-cycle jitter as it is true representation of the perturbations related to one particular cycle. The random perturbation is translated into the signal as a phase modulation.

The architecture of the AWGN channel is shown in the Figure 3.2 below, the function ‘G(t)’ is a function of the random signal generated by random signal block (generation of a random sequence) which is Gaussianly distributed, with mean = 0 and variance = 1. The function ‘G(t)’ which acts as an asymptotic envelope as described in (Max).
Figure 3.2: Complete Block Diagram of Micro Noise Source with AWGN Channel

Therefore mathematically the output signal of the AWGN channel block can be written as in Equation 3.1, where ‘\( G(t) \)’ is AWGN channel function.

\[
\Delta \omega(t) = G(t)A_0 \cos(\omega t + \phi(t)) ; \quad \text{Since} \quad \Delta \omega(t) = \frac{d}{dt}\phi(t).
\]

Therefore

\[
\frac{d}{dt}\phi(t) = G(t)A_0 \cos(\omega t + \phi(t))
\]  

(3.1)

The final product which reflects the time domain signal of realistic oscillator is obtained when the time domain complex signal (total perturbed phase) is multiplied with an ideal oscillator output. Mathematically it is given by Equation 3.2.

\[
A_{\text{out}}(t) = A_0 \cdot \cos(\omega t + \phi(t)) \quad \text{and} \quad V_{\text{out}}(t) = V_0 \cdot \cos(\omega t + \phi(t))
\]  

(3.2)

The real time output of an oscillator with In-Phase, Quadrature and Ideal responses is shown in the Figure 3.3 below. The Figure 3.3 shows an oscillator with a central frequency of 5.6GHz, amplitude of 1Volts and phase noise of -100dBc/Hz at an offset frequency of 1MHz. In the succeeding Figure 3.4 the unperturbed and perturbed Quadrature Oscillator outputs are shown with the running cycle to cycle jitter of 4.7725 femto seconds to produce the phase noise of -120dBc/Hz@1MHz offset, this jitter is induced through the variance block in the AWGN Channel.
3.3 Analysis of QDAcR architecture

One of the main objectives of this thesis has been to look into the pros and cons of the present system architectures for ir-UWB receivers. The QDAcR architecture proposed in [8, 23] can be characterized as low-IF receiver architecture and is shown in the Figure below. In UWB the processing of bandwidth of 7.5 GHz. poses severe design constraints, typically there has been no transceiver architecture devised to
process such a wideband, the two most common architectures for the transceiver’s design are “(Super) Heterodyne or IF architectures and Zero-IF or Low-IF architectures. Both of these architectures possess specific merits and demerits in accordance with the specific use based on the RF bandwidth, modulation scheme and system design specifications.

Heterodyne transceivers are predominantly used for narrowband communication systems where the channel / entire signal bandwidth measures maximum in Kilohertz or fraction of Megahertz. The heterodyne receiver gives the advantages of high channel selectivity and receiver sensitivity. The functionality of heterodyne receiver is explained by taking an example of Dual-IF Heterodyne Receiver Topology [39] as shown in the Figure 3.6 below. The first step involved in designing the heterodyne receiver is the frequency planning that is choosing the appropriate Oscillator frequencies (in the case of multiple downconversions), this calculation of oscillator frequency plays an important role as it decides the frequencies at which the Image will reside.

The Image is calculated as $\omega_{\text{image}} = \omega_{\text{LO}} \pm \omega_{\text{RF}} \pm \omega_{\text{IF}}$; the proper choice of frequency facilitates that the “Spurs (the Intermodulated components)” do not fall in the RF, IF or LO frequency bands, as if the signal strength is higher it can desensitize the receiver. The “Image Reject Filter” is used before the process of Downconversion and after the LNA as shown in the Figure in order to suppress the Image, the Image reject filter requires a high “Q”, which largely depends upon the strength as position of the Image as well any interferer residing in the concerned band. The requirements of moderate to high “Q” for the Channel Select Filter depends upon the Mixer output, as if high IIP2, IIP3 and conversion gain can relax the Channel Select Filter’s requirements, also the purity of Oscillator spectrum that is the higher phase noise also acts as a major factor in easing the Channel Select Filter’s requirements.
An Oscillator System for UWB QDAcR

However, the heterodyne topology poses advantages like, the use of Image Reject filter not only stops the image but also provide a higher degree of port-to-port isolation for LO-LNA leakage and thus circumventing the chances of higher strength spurs getting mixed into the RF path or LO power seepage to the Antenna and subsequently corrupting the transmitted signal. Other aspects of the IF-Receiver architecture that poses design concerns are integration of the Image reject filter and LNA’s output impedance matching. The Image reject filter is usually realized as an off-chip passive component network [39], which in turn puts the severity on the output impedance of the LNA to match to 50 ohm in order to transfer the maximum RF signal power and this result in the trade-offs between the power dissipation, noise-figure, stability and the gain [39]. Here it was described in brief the functionality, advantages and disadvantages of a “Heterodyne Receiver”.

![Figure 3.6: Dual-IF Heterodyne Receiver Topology [39]](image1)

The other type of receiver architecture is “Direct-conversion, Zero-IF, Low-IF or Homodyne” receivers in which the RF signal is directly downconverted to the baseband levels. The LO frequency is chosen such that it equal to Or approaches to the RF band center frequency, therefore mathematically it can be illustrated as $\omega_{lo} \approx \omega_{center}^{RF}$, which implies that the $\omega_{lo}$, a block diagram representation of direct-conversion receiver is shown in the Figure 3.7 below.

![Figure 3.7: A Direct-Conversion Receiver.](image2)
The Zero-IF topology results in reducing the design complexity by avoiding the use of Image reject Surface Acoustic Wave (SAW) filter, which in turn eases out the severity of output impedance matching on the LNA. Furthermore, by avoidance of SAW filters, the Zero-IF topology simplifies the possibility of designing the front end as monolithic process (No off chip components). However, there are other kinds of receiver topology specific severities that downgrade the performance of the Zero-IF receiver. These are as follows:

DC Offsets & LO Leakage
Noise (Flicker) Issues
I/Q Mismatches

These direct-conversion receiver’s drawbacks are being analyzed in the perspective of the QDAcR, as QDAcR architecture as shown in Figure 3.5 falls under the direct-conversion receiver’s category. The functionality of the QDAcR at system level and circuit level, while taking components discretely is very well described in [8, 19, 20 and 23]. As one of the primary objectives is to analyze the QDAcR as a fully integrated receiver at the system level and for this purpose it is of utmost importance to first analyze the architecture and find the possible bottlenecks and the corresponding solutions.

a) DC Offsets and LO Leakage: The DC offsets can corrupt the RF signal since the downconversion folds the RF signal band around the DC and the centre frequency is shifted to “Zero”. Therefore, any data folded around the DC levels could be corrupted in presence of unwanted products at DC or at quite low frequencies and these unwanted signals are generated due to the phenomena of “Self Mixing” and Interferer leakage [39]. The self mixing happens as the LO power leakage due to improper isolation between the LO-LNA and LO-Mixer input ports, once the leaked signal (power) either enters the LNA or Mixer and it gets mixed further and downconverted to near DC levels, which in turn corrupts the signal. The main reasons of LO leakage are capacitive coupling, substrate coupling and bond wire coupling (in case of off-chip LO) [39]. When a strong interferer (in-band poses more severity than out of band interferer) with its central frequency close to LO frequency leaks through the LNA input port and in turn it mixes with LO signal and producing a furthermore strong interferer at the DC levels. DC offsets is a major problem, which severely degrades the performance of the homodyne receiver.

If we analyze DC offset effect in the context of QDAcR, we notice that the extent of severity is more than any other normal direct-conversion receiver, because of the presence of primary and in-band interferers with their center frequency close to the LO frequency. The degradation in the performance is measured as the resultant of net BER ratio and the effect of interference is quantitatively shown in the [40, 23]. A novel solution is also reported in [23], which is in form of a band-reject LNA with a simulated notch of 20dB
along with the 7th order transformer orthonormal-C band-reject filter with a 25dB interference rejection and LNA+Band-Reject Filter in combination with an antenna having a notch of 15dB. The total interference rejection reported by this combination is in the range of 35-60dB for IEEE802.11a/n WLAN.

The IEEE802.11a/n interferer sweeps across the entire band of 4.915GHz to 5.825GHz, with data transmission in different channels depending upon the local regulations. Therefore, while doing the system level analysis, it is considered the entire band of 910MHz~1GHz bandwidth as interferer band with central frequency of in the range of 5.35-5.37GHz. Now if we extrapolate the results of [23] then we find that combination of the antenna +B-Reject Filter +B-Reject LNA, gives the total maximum rejection (simulated) of 15dB over the entire interferer bandwidth. Undoubtedly, this approach provides a novel solution but still it lacks in providing the appropriate isolation for interferer leakage as well as LO leakage (feed-through) to the antenna. The problem of interferer and LO leakage is circumvented with much more effectiveness in heterodyne receiver topology by the use of Image reject filter in the LO-LNA path, which increases the port to port isolation, while doing the filtering and second the LO frequency is not equal to the RF signal center frequency. The solution to problem of DC offsets specifically in context to the QDAcR is discussed in detail in the section 3.4, where the proposed solution is tested at the system level.

b) Noise (Flicker) Issues: As described in detail in section 2.4.1 the device flicker noise exists from a few KHz to MHz and the device corner frequency increases with every decrease in the channel length in the CMOS. Generally the received RF signals are in the order of +10dBm to -120dBm and as the signal is converted to the DC in direct-conversion receiver, the downconverted band coinciding with the device’s corner frequency becomes vulnerable of being corrupted. Therefore, a high gain is required in the receiver’s front end architecture, as it can be seen from the Frii’s Noise Equation (given below) that the gain ‘G’ is of prime importance in controlling the total noise Figure. The higher the gain, lower is the noise Figure, and noise defines the minimum detectable receiver for the receiver system.

\[
F_{total} = F_1 + \frac{F_i - 1}{G_i} + \frac{F_2 - 1}{G_1G_2} + \ldots + \frac{F_N - 1}{G_1G_2\ldots G_{N-1}}
\]  

(3.3)

Therefore in the direct conversion receiver the gain of the front end blocks becomes more important in order to reduce the overall noise effect of the system, the direct-conversion uses the single stage downconversion to the baseband level, while in the heterodyne system couple or more downconversion stage are used. Since each stage introduces some gain as well as noise, however the overall noise-figure is less in heterodyne than the homodyne receiver.

c) I/Q Mismatches: As explained in the [39] the importance of the quadrature components especially in the any other modulation scheme other than the amplitude modulation, therefore any mismatches between I and Q signals corrupt the downconverted signal. The effect of phase error on the QDAcR is being explored in the previous section and it is seen that the performance drastically deteriorates as the phase error
An Oscillator System for UWB QDAcR

increases. Also, all the stages in the RF front end (LNA, Mixer, Oscillator etc.) add their own amplitude and phase errors thus corrupting the signal. Therefore, the phase and amplitude errors arising due to I/Q mismatches are important factor in the QDAcR performance.

3.3.1 Frequency Planning in QDAcR architecture

The frequency planning is the very first and a necessary step towards determining the receiver’s system specifications, it gives the view of channel availability and interferer free region. In case of Ultra wideband it is essential to know all the interferers and mitigate them through the receiver design and the signal modulation techniques. Since UWB has a bandwidth of 7.5GHz, which makes it prone to wide number of out of band and in-band interferers, a detailed analysis of all the possible interferers is presented here, which lays the foundation of system specs as well as the desired receiver architecture. The following Figure 3.8 shows the possible interferers with their maximum possible signal power at the receiver’s end marked by the various colored lines.

![Figure 3.8: Showing the various interferers present.](image)

The desensitization and blocking of the receiver happens when a strong interferer owing to the non-linearity of the device / system decreases the average gain of the circuit. There are generally three different types of non-linear effects seen in a circuit, these are as follows.

Harmonics: Any given function, which is Fourier series decomposable, when applied to a nonlinear system, where the output is expressed as \( y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots \) show the frequency components in the output, which are integral multiple of the fundamental frequency. If the amplitude (strength) of these harmonics is high then by self mixing or through port leakage (as in the case of LO-LNA path) or mixing with the RF signal, these harmonics create spurs and these spurs can easily desensitize the receiver, these issues are major source of concern especially in “homodyne or Zero/Low-IF” receivers.
Cross-Modulation: This Non-Linearity arises when in a non-linear system; an amplitude modulated interferer transfers the modulation to the desired RF signal. It is a third order non-linearity and is proved mathematically in [39] and this effect the receiver’s dynamic range, with cross modulation corrupting the RF signal in the channel. The receiver system with high IP3 and high linear mixer output also shows a good resistance towards the cross-modulation.

Intermodulation: The Intermodulation is a process in which when two RF inputs are applied to the input of any non-linear system then as a result there are components which are not the harmonics of the input frequencies [39]. If we take the inputs to be at the frequencies \( \omega_1 \) & \( \omega_2 \) then the main third order Intermodulated products occur at \( 2\omega_1 \pm \omega_2 \) & \( 2\omega_2 \pm \omega_1 \) frequencies and ratio of fundamental to the third order non-linearities is described as the third order intercept point and is represented in the form of IIP3(Input IP3) or OIP3(Output IP3). Similarly, the second order non-linearity is given by the Intermodulated products occurring at the frequencies \( \omega_1 \pm \omega_2 \) & \( \omega_2 \pm \omega_1 \). The level of the distortion (compression in the output with respect to the input) in any circuit due to the third order and second order Intermodulated products is given by the Figures of merits for circuits called IIP3 and IIP2. The Intermodulated products falling in the RF band are called in-band interferers which cause more severity than the out of band interferers that is the Intermodulated products falling outside the RF signal band. The concept of Intermodulated products with mathematics in detail is explained in [39].

Pertaining to the UWB we can decipher from the above Figure 3.8 the number of interferers possible, the number of possible third order and second order. With a possible of ‘341’ third order Intermodulated products falling in the UWB band and a possible number of ‘262’ second order in band Intermodulated product interferers. Therefore the interferers literary jammed the UWB band; however with proper selection of the appropriate filter topology and proper QDAcR architecture topology can mitigate the effect of most of these interferers.

If we see the Intermodulated product (both third and second order) tables we find that if the interferers with frequency 3.7GHz and below are filtered out then the UWB can be free of almost 90% of the possible in band interferers. Other most important source of interference is IEEE802.11a/n which sweeps bandwidth of approximated to 1GHz, with centre frequency hopping around 5.35-5.37 GHz, therefore the oscillation frequency is chosen in such a way that the major interferers can be downconverted to the DC levels and then can be easily filtered out. Therefore the present QDAcR architecture definitely requires some additional changes in order to meet the basic specifications for the in band communication. The possible solutions are discussed in detail in the next section.
3.3.2 The Noise Block

This block is modeled to calculate the desired Noise Figure of a circuit, to find the desired value in order achieve the proper level of correlation. The Noise Figure is one of the important parameters for measuring the system’s performance. The Noise Figure ‘NF’ mathematically is given by

\[ NF = \frac{SNR_{in}}{SNR_{out}}, \text{SNR}_{in} \geq \text{SNR}_{out} \]  

(3.4)

The noise produced in an active circuit is both device parameter and bias dependent, which is hard to model in matlab without knowing the bias conditions and device in use. Therefore, the active circuit is treated as a noiseless black box and all the noise is referred to the input of the two port network [39]. In the Figure 3.9 below it is shown that the total increase in the input noise floor is equal to the “Noise Figure” of the that particular, the variable ‘F’ is the ‘Noise Factor’.

![Figure 3.9: Modeling of Noise](image)

In MATLAB the noise source is taken as an Additive White Gaussian Noise Channel (AWGN) which covers all the thermal and shot noises. The input level of noise \( N_{in} \) is calibrated to the receiver’s thermal noise floor (minimum noise present in the receiver chain) and the output level of the noise \( N_{out} \) is calibrated as per the desired “Noise Figure”. The block is easily integrated into any of the circuits (for e.g. LNA, Mixer, Amplifier) and enabling the measurement of the output for the desired Noise Figure.

![Figure 3.10: Modeling of Noise Block in MATLAB](image)
3.4 Designing of the Quadrature Downconversion Auto Correlation Receiver (QDAcR) in MATLAB

The QDAcR is modeled fully in the MATLAB in order to find the complete system specifications under the realistic circuit operating conditions, while taking care of the possible bottlenecks. For this purpose first task is to describe the Matlab model for the QDAcR (old architecture) which is as shown in the Figure 3.11. The different blocks in the model are described in the detail in the following section, first the system specification are calculated and then the proposed changes at block level are described, which in end lead to a composite renewed architecture for the QDAcR.

![QDAcR Block Diagram Representation](image)

Figure 3.11: QDAcR Block Diagram Representation
An Oscillator System for UWB QDAcR

1. The RF Input Block: The foremost task is to define the specifications for the received radio signal, as the accurate signal modeling serves as the start point for further system calculations. This block replicates the RF-Input from the antenna as in the case of ir-UWB communication system. The block implements a few nano-pico second pulses as the received RF-Signal; the strength of the received RF signal for the modeling and link budget analysis is calculated using the formula as given in [41] and reproduced below. According to the FCC the maximum emissions level in UWB is \(-41.3\, \text{dBm/MHz}\) therefore taking the maximum transmitted power to be

\[
P_T = -41.3 + 10\log(f_H - f_L) \, \text{dBm}
\]

Where \(P_T\) = Received input power of RF Signal, \(G_{\text{T,ANT}}\) = Gain Antenna at transmitter side, \(G_{\text{R,ANT}}\) = Gain Antenna at the receiver end and \(L_p\) = Path Loss or the amount by which the signal strength has deteriorated due to interference, continuous reflection and other effects. The value of path loss is given by the following Equation as

\[
L_p = 20\log\left(\frac{4\pi f_c}{c}\right) + 20\log(d) \, [\text{dBm}]
\]

Where \(d\) = Path Length in meters and \(c\) = Speed of light. Since the bandwidth of UWB is 7.5GHz, which ranges from 3.1-10.6GHz and is characterized as IEEE802.15.4a. The UWB centre frequency is given by the \(f_c = \sqrt{f_L f_H} = 5.732\, \text{GHz}\), where ‘\(f_c\)’ is the geometric mean [41] or if taking arithmetic mean then it is \(f_c = \frac{f_L + f_H}{2} = 6.85\, \text{GHz}\). Second approximation is about the path length ‘d’, the main purpose of UWB is to work as short distance radio and it is shown in the Figure 1.8 as the relation between the throughput and distance. Therefore, calculating the received power for \(d = [5, 10, 20] \, \text{m}\). Approximating antenna gains \((R_{\text{T}} \& T_{\text{T}})\) to be ‘zero’; therefore we have

\[
\begin{align*}
P_{R_{\text{T}}} &= -64.1367\, \text{dBm} \\
P_{R_{\text{T}}} &= -70.1573\, \text{dBm} \\
P_{R_{\text{T}}} &= -76.1779\, \text{dBm}
\end{align*}
\]

As it can be discerned relatively easily that power received at the \(R_{\text{T}}\) end decrease with increase in the path length and also the throughput decreases with increase in distance.

For, the modeling of the input RF-Signal, the worst case scenario is used while considering the 20m path distance and further calculating the minimum level of signal that can be detected (MDS) and it given by

\[
MDS = -174\, \text{dBm} + 10\log B + \text{NF}_{\text{sys}}
\]

As the starting point for the calculations, first the value of receiver’s noise-figure has to be calculated. The thermal noise floor of the UWB receiver is \(-75.249\, \text{dBm}\) (considering the total bandwidth of 7.5GHz), this shows that the desired RF signal is already buried inside the noise-floor. If the receiver’s own noise is added to this value it further deteriorates the problem posing designing complexities, for the desired
processing of the signal the front end needs to have lowest noise-figure as well as high gain for the attaining the proper signal levels for the Analog to Digital Converter Input stage. Therefore, a trade off between the system gains, system noise Figure as well as the total power consumption has to be devised.

Approximation for the receiver’s Noise Figure (NF): first up, the noise contribution from the primary candidates (most noisy) Mixer and LNA is considered. For this purpose first approximating the mixer’s specifications as given in [42, 43], the reported noise-figure varies with the frequency, going up as the frequency increases, therefore sticking to the center frequency of 5.732GHz and doing all the calculations at this frequency. Therefore as in [43] the NF is averaged to be 17dB, with a conversion gain of around 5.5dB, in [42] the reported noise Figure is about 7dB with a conversion gain of around 2.5dB. The two mixers, which are quoted as referenced are designed in two different circuit topologies and assumptions. For the calculation and requirement of the QDAcR, we have to go with a HIGH-Gain Active mixer, which results in a relatively high noise Figure. Therefore, with some more margins taking noise Figure of mixer to be $\approx 20$dB, the net value of the noise Figure seen at the receiver’s antenna end is given by the Frii’s noise Equation, by which having a high gain LNA becomes a necessity.

A few good reported UWB LNAs are [p.139 of 23], with the highest gain of 19±2 dB in [23-[121]] and lowest NF of $2.51\pm 0.47$ dB [23-[114]]. Since the gain and the noise figure, which are reported happen to be technology and circuit design dependent, therefore it is not wise to average any of the required parameters, however this provides hint to have approximated gain value (the mode value) which is around 16.5dB and a maximum noise Figure of 4.5dB. Taking these as the approximated values (starting point) the total noise Figure approximated by the Frii’s Equation is $\text{NF}_{\text{system}} = 10\text{dB (2dB Duplexer + 7.96dB from LNA+Mixer)}$. Therefore the value of maximum detectable signal is -65.25dBm or higher, therefore for distance of 5meters or less UWB proves to be a useful communication in comparison to various existing platforms.

However, designing system for 20meters distance with a maximum signal level of -76.18dBm, to this adding an extra margin of 10dB for other circuit and process related irregularities such as transmitter leakage to the receiver, effect of parasitic, signal loss due to jamming etc. therefore for calculation taking the received signal value to be -86.18dBm. Next step is to define the total receiver gain, which will define the level of input for the ADC stage. Considering the input levels of ADC in the order of a few hundreds of mV [atmel], and approximating the value to be around $\pm 250$ mV or $+1$dBm. Therefore the total desirable receiver gain = 87.2dBm to be a minimum.

There are many different pulses reported as carrier/signal for ir-UWB system, modeling and testing of some of them is presented here in order to find which pulse performs the best for the QDAcR. Matlab model of QDAcR is modeled with the different pulses as RF-Signal inputs, these pulses are namely
An Oscillator System for UWB QDAcR

Gaussian, Gaussian Mono, Gaussian Doublet, Sinc function, Mortlet Wavelet of Gaussian and Daubech"ie’s Wavelet of Gaussian.

a) Gaussian Pulse: The Gaussian Pulse is given by $g(t) = \frac{1}{\sqrt{2\pi\sigma}} \exp\left(\frac{-(t-\mu)^2}{2\sigma^2}\right)$, where the width of the Gaussian pulse is given by $\sigma$, and the value of $\mu$ is the mean and it signifies the position of axis of symmetry. According to [23] Gaussian pulse has good time-frequency resolution however poor spectral efficiency. The Figures below show the transient and power spectral density of a Gaussian pulse, for $\sigma = 1e-09$ and time period of 1nsec. The PSD diagram shows the output from $-f_s/2, 0, f_s/2$, the bandwidth of the Gaussian can be changed by changing the $\sigma$.

![Figure 3.12: The Transient levels of Gaussian Pulse](image1)

![Figure 3.13: The PSD levels of Gaussian Pulse](image2)
It can be seen that the signals levels are well below the FCC limits and if the point of pulse origin is shifted from negative axis to the origin or to 3.1GHz, the Gaussian covers a bandwidth of approximately 11GHz, which covers the entire desired band from 3.1GHz-10.6GHz. The bandwidth is a function of sigma; it shows that by choosing the appropriate variance a better spectral efficiency for the desired bandwidth can be attained. The Figures 3.14 and 3.15 below shows the bandwidth of around 7.5GHz (axis can be shifted to 3.1GHz by changing the mean of the Gaussian) covering the entire Ultra Wideband and signals levels ≤ -86.2dBm for $\sigma = 2.05e-9$

![Figure 3.14: The PSD levels at $\sigma = 2.05e-09$](image1)

![Figure 3.15: Transient response of the Gaussian for $\sigma = 2.05e-09$](image2)
b) Gaussian Mono or First Derivative of the Gaussian Pulse is also widely used as a carrier for the ir-UWB systems. The PSD and transient response of the Gaussian mono pulse are shown in the Figures 3.16 and 3.17 below. The bandwidth is adjusted to meet the UWB requirement and provide, higher spectral efficiency by providing a higher roll-off at the ends of band. This can be seen as over the half bandwidth the Gaussian mono provides the fall of over-60dB, which is 20dB greater than the provided by the Gaussian or Gaussian Doublet.

Figure 3.16: The PSD levels of Gaussian Mono Pulse

Figure 3.17: The Transient levels of Gaussian Mono Pulse
c) Gaussian Doublet or Second Derivative of the Gaussian Pulse is used as a carrier for the ir-UWB systems. The PSD and transient response of the Gaussian doublet pulse are shown in the Figures 3.18 and 3.19 below, the bandwidth is adjusted to meet the UWB requirement by varying the $\sigma$, and provide, higher spectral efficiency by providing a higher roll-off at the ends of band in comparison to the simple Gaussian.

![Figure 3.18: The PSD levels of Gaussian Doublet Pulse](image1)

![Figure 3.19: The Transient levels of Gaussian Doublet Pulse](image2)

The Daubechie’s, Morlet and Sinc function are modeled in the matlab as the wavelet. The design principle for the wavelet based filters is explained comprehensively in [23]. The typical flowchart involves the following stages in respective order [23]. Starting with the Polynomial Approximation, 2) Laplace Transformation, 3) Rational Approximation, 4) State Space Optimization and 5) Designing of the desired transfer function on to the silicon. The transfer functions for Daubechie’s and Morlet Wavelet are taken from [44, 23] and the coefficients of the state spaces elements are changed in order to comply to the QDAcR system design.
The generalized model used in the Matlab modeling for these wavelets is shown in the Figure 3.20 below. When the Unit Impulse is multiplied with the Gaussian function, it provides the impulse output which has Gaussian distribution, this replicates as the Gaussian Envelope for the transfer function and desired wavelet output is achieved.

![Figure 3.20: Block Diagram for the Wavelet Modeling](image)

d) Daubechie’s Wavelet: The transfer function of the Daubechie’s is taken directly from the [23], the coefficient of state space matrix are found by Matlab command. The co-efficient are multiplied by constants to have entire bandwidth response. The values are as follows

[A]: 
```
[0 2.066e11 0 0 0 0 0; -2.66e11 0 3.146e11 0 0 0 0; 0 -3.146e11 0 3.399e11 0 0 0; 0 0 -3.399e11 0 3.531e11 0 0; 0 0 0 -3.531e11 0 4.016e11 0; 0 0 0 0 -4.016e11 0 5.297e11 0; 0 0 0 0 0 -5.297e11 0 10.74e11; 0 0 0 0 0 -10.74e11 -17.99e11]
```

[B]: [0; 0; 0; 0; 0; 0; 2.393e11]

[C]: [.9831 .3831 .02877 -.179 0.1166 -.02037 0 0]

[D]: [0]
An Oscillator System for UWB QDaC

Figure 3.21: The Transient levels of Daubechies Wavelet.

Figure 3.22: The PSD levels of Daubechies Wavelet.

e) Morlet Wavelet: The co-efficient of state space matrix [A,B,C,D] are given below. The following Figures 3.23 and 3.24 show the PSD levels and the transient response of the Morlet Wavelet Function.

[A]: 
\[
\begin{bmatrix}
0 & 2.649 \times 10^{11} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-2.649 \times 10^{11} & 0 & 7.412 \times 10^{10} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -7.412 \times 10^{10} & 0 & 2.669 \times 10^{11} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -2.669 \times 10^{11} & 0 & 1.102 \times 10^{11} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -1.102 \times 10^{11} & 0 & 2.58 \times 10^{11} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & -2.58 \times 10^{11} & 0 & 1.575 \times 10^{11} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -1.575 \times 10^{11} & 0 & 2.539 \times 10^{11} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -2.539 \times 10^{11} & 0 & 2.381 \times 10^{11} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -2.381 \times 10^{11} & 0 & 4.24 \times 10^{11} \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -4.24 \times 10^{11} & -5.391 \times 10^{11}
\end{bmatrix}
\]

[B]: [0; 0; 0; 0; 0; 0; 0; 0; 0; 8.303e9]
The Equation of the morlet wavelet filter is given by Equation 3.11 below and it is obtained by multiplying a Gaussian envelope with the cosine function.

\[ \psi(t) = \cos(5\sqrt{2}(t - 3))e^{-(t-3)^2} \]  

(3.11)

f) SINC Wavelet Function: The co-efficient of state space matrix [A,B,C,D] of a Sinc function are given below. The following Figures show the PSD levels and the transient response of the Sinc Wavelet Function.
The Equation of the Sinc wavelet function is given by Equation 3.12 below as

\[
\psi(t) = \frac{\sin(\pi t)}{\pi t} \quad (3.12)
\]

As it can be discerned from the above Figure that among all the wavelet and normal Gaussian functions plotted and tested for the RF signal, the Sinc function has the highest spectral efficiency. It can be seen that the decay of 50-60dB over a bandwidth of 4GHz can be used for the system design advantage for example where high roll-off is required in the filter response. In [23] it is mentioned that Sinc wavelet has a ‘Brick Wall’ kind of response, which is ideally suitable for the UWB communication system. The Transient response of a Sinc function is shown in the Figure 3.26 below.
2. The Narrow Band Interferers (NBI) and White Noise Block: Through this block the effect of the channel white noise and the interference induced by the Narrow Band signals such as Wi-Max(2.3GHz-2.7GHz & 3.3GHz-3.7GHz), IEEE 802.11b/g and 802.11a/n standards is being applied to the receiver system design. As postulated by the [40] that these interferes further corrupts the quality of the desired Radio Frequency (RF) signal and as a result the final RF signal at the input of the Low Noise Amplifier (LNA) can be mathematically denoted by the following Equation

\[ r(t) = s(t) + n(t) + i(t) \]  

(3.13)

Where \( r(t) \), \( s(t) \), \( n(t) \) and \( i(t) \) denotes the resultant (Corrupted + Noisy) RF input at the LNA, the UWB signal, the Gaussian white noise and the narrow band interferes respectively. The effect of narrow band interferes can be modeled as a correlation between the narrow band signal interferes \( i(t) \) and UWB signal \( s(t) \), narrow band signal \( i(t) \) and the noise \( n(t) \) and the (auto) correlation between the narrow band signal \( i(t) \) itself. The following are expressed numerically as \( \mu^{(\text{ni})}, \mu^{(\text{ni})} \text{ and } \mu^{(\text{ni})} \text{ respectively, the severity caused by the narrowband interferes and noise in the ir-UWB receiver’s performance is appropriately measured in terms of the Bit Error Ratio (BER) as given in [40]. The results deduced in [40] shows that \( \mu^{(\text{ni})} \text{, or the correlation between the narrow band interferer and the Gaussian random noise, downgrades the performance of the receiver severely than any other interference/signal/noise correlations that is } \mu^{(\text{ni})} \text{ or } \mu^{(\text{ni})} \text{, the severity effect on the performance of receiver can be characterized as } \mu^{(\text{ni})} > \mu^{(\text{ni})} > \mu^{(\text{ni})} \text{. This result shows that it is necessary to filter out the narrow band interferes before performing the auto-correlation of the received signal. The narrow band interferes can be modeled mathematically as sinusoid signal with a complex envelope function ‘} u(t) \text{’, which remains constant for the} \]

![Figure 3.26: The transient Levels of a Sinc Wavelet Function](image-url)
entire UWB symbol duration [23, 40]. Mathematically it is given by

\( i(t) = \sqrt{2} \Re \{ u(t)e^{j2\pi f_{\omega} t} \} \)

where \( u(t) = |u(t)|e^{j\phi(t)} \) is a low-pass function for the narrow band interferer function ‘i(t)’, the interferers can be filtered out by modeling them as real band-pass signals with central frequency ‘\( f_{\omega} \)’ and bandwidth \( B \ll W \), where ‘\( W \)’ is UWB Bandwidth. Considering the NBI sinusoid function \( i(t) \), putting the values for IEEE standards 802.11a/b/g/n in the Equation 3.14.

\[ i(t) = \sqrt{2} \Re \{ u(t)e^{j2\pi f_{\omega} t} \} \] (3.14)

The NBIs are modeled as the impulse response of a filter, the exact function is constructed by defining the transfer function ‘\( H(s) \)’. The transfer function is calculated according to the algorithm described in [23], the transfer functions for IEEE802.11a/b are calculated and implemented in MATLAB in order to replicate the exact NBI responses, the effect of thermal noise / channel white noise floor is added to total noise output. The Wi-max interferer is also modeled based on the above Equation as a sinusoid. The Figure 3.27 below shows the matlab model of the ‘Interferer - Noise’ Block. The interferers’ output level is quantized to the -10dBm level for 50ohm impedance (this to analyze the QDAcR in the worst case scenario, as typical interferer power is between -30dBm to -80dBm levels), the noise floor / receivers’ noise floor is modeled for entire 7.5GHz bandwidth‘(\( \Delta f \)’).

Figure 3.27: The Block Diagram for the Implementation of the Interferers

The Figure 3.28 below shows the output of the interferer block; the NBIs are shown, first the zoom picture of OFDM 802.11b, then 802.11a and the white noise as thermal noise floor.
3. Filtering Stage: As seen in the QDAcR linearity analysis that the UWB system suffers severely from the interferers and most of the in-band interferers are the Intermodulated products of mainly Wi-Max and IEEE802.11a/b/g/n communication standards with other 16 possible interferers. Therefore, for the proper functioning of the QDAcR it is very necessary to filter out the interferers. As discussed before that the solution proposed in [23] offers a maximum of around 35-40dB rejection for the W-LAN interferer and then downconverting the entire band by wrapping the spectrum around the baseband and filtering the main downconverted interferers by using a Band pass filter. However, the existence of Wi-Max interferer and Intermodulation due to device non-linearity makes it impossible to have an interferer free baseband signal.

In broad terms the published work on QDAcR is a good design proposition, however if we see the possible interferer table (2nd and 3rd Order interferers), then we find that even after the downconversion and filtering, most of the baseband spectrum is full of Intermodulated interferers. It is of utmost necessity to filter the major interferers before they can enter LNA, otherwise it will not only put high linearity requirements on the LNA but result in complex design and higher power consumption. and importantly a low “Q” with respect to passives, also in active filters there is a possible chance of direct interferer leakage.

Therefore, here now is proposed a band-pass filter with the system level simulations, showing its advantages as well as the possible drawbacks. Taking the all the interferers from 450MHz (GSM) to
An Oscillator System for UWB QDAcR

3.7GHz (Wi-Max) and their possible 2nd order and 3rd order modulated effects. The first approach is to block all these interferers entering the device and having any Intermodulated products, hence having a band-pass filter in between the antenna and the LNA. The BPF should have steeper transition and should offer as high rejection as possible and as flat as possible output over the entire bandwidth. Here it is required a wideband BPF, choosing the lower passband frequency to be 3.7GHz and upper frequency to be 10.6GHz. It can be seen that by choosing the lower cut-off frequency to be 3.7GHz a UWB signal bandwidth of around 600MHz is lost, however it is necessary in order to make receiver operable and to be robust.

The filter needs to stop all the interferes from 0Ghz-3.8GHZ range, providing the maximum rejection possible, the passband exists from 3.8GHz-10.6GHz, with a wideband notch at 5GHz-6GHz that attenuates the WLAN interferer as much as possible. It is necessary to attenuate these major interferers entering active device circuitry in order to circumvent the number of intermodulated products and keep the downconverted band clean. The possible candidates are only passive filters, which are SAW (surface Acoustic Wave) filter (off-chip) and Microstrip Filters; use of active filter is ruled out, because of the requirement of the high levels of band rejection and as low as possible insertion losses, which translates into a filter with a high ‘Q’ quality factor. Also for large bandwidth response active filters show poor linearity, noisier (because of the accumulation of device noise) and consume higher power.

The effect of phase distortion in QDAcR is modeled using matlab and is depicted in the Figure below. This graph represents the maximum phase distortion that can be tolerated with in QDAcR, the assumption that is made during the modeling of the phase distortion is as follows: All the components are ideal, including the delay block. The consideration of the delay block being ideal is justifiable because of we see the QDAcR architecture it can be noticed that the correlated UWB pulses are subject to same frontend signal processing, only distinction being the that one is delayed by the delay block and its replica is delayed in the transmitter. The discernable information from the graph below is that maximum tolerable single-ended phase error of 24degrees is permissible for auto-correlation coefficient of 0.85.
The next estimation for the total phase distortion is to subtract the feasible quadrature phase error between the In-Phase and Quadrature responses from the maximum permissible phase error of 22.8 degrees. As it is proved in the section 2.3 that the maximum allowable phase error between I/Q responses is 8.75 degrees and it can be curtailed down by designing a good Q-VCO. Therefore as a design parameter for the circuit designer fixing the maximum allowable quadrature phase error to be 5 degrees or less, this will result in fixing in single ended permissible maximum error to be 20degrees. Therefore, the maximum composite phase error for the Delay block, Mixer, LNA and filter stages is 20degrees.

The next step is to choose the topology for the band pass filter and the candidates are Chebyshev Filter (Type1 and Type 2): Both kind of chebyshev filters are considered for the system topology, as these both provide distinctive advantages. Type 1 has the high roll off, however more flatness in the passband is observed in the Type 2 filter. There exist a ripple in the stopband in the type 2 topology, however by deciding the lower band and upper band cut-off frequencies carefully; the ripple can be turned out to be advantageous in improving the spectral efficiency as in the case of multiple-wide band rejection. The phase distortion or the group delay in the Chebyshev filters is on the higher side in comparison to the Butterworth and Bessel filters.
Elliptic Filter: These filters provide steeper transition from passband to stopband in comparison to the Chebyshev filters. The phase distortion is the highest in the elliptic filters, when compared to the Bessel, Butterworth and Chebyshev filters, therefore it will put additional burden on the time delay accuracy required in the QDAcR.

The next step requires choosing the implementation of the filter using the passives. As mentioned earlier that the specifications required for the bandpass filter can be matched either by the Microstrip (Transmission Line) filter or SAW-Passive filters. The choice is a Microstrip (Transmission line) Bandpass Filter, in which the passives or lumped elements can be implemented using the Microstrip line as stubs or transmission line resonators etc. The choice of using Microstrip filter is a conducive one as it offers the lowest insertion loss possible, which helps the low RF signal levels from having much more attenuation, thus relaxing the power-Gain budget for the subsequent active stages in the circuit. As reported loss of 0.58dB in [45] and of 2dB [46] across the complete 7.5GHz bandwidth in comparison to insertion loss of 8-9dB over a narrowband [23]

The Microstrip / transmission line filters offer high Rejection in comparison to its other counterpart topologies, the QDAcR system requires to have highest possible rejection in the stopband, as it is seen in [45, 46, 47] that a rejection levels of 30-50dB are quite achievable.

Power consumption in Microstrip filters is less and the signal power is delivered to the load much more efficiently than other implementable filter designs for e.g. the active filters; this is because of the precise input/output impedance matching to the antenna and LNA.

Use of Microstrip line with RF-MEMS as described in detail in [48] offers the far better solution than the other implementation methods. It offers a high ‘Q’, high linearity and less power consumption. In the context of QDAcR the phase distortion plays an important role, the main principle of Auto Correlation relies on the accuracy of the time delay with respect to the transmitted signal. Therefore, the phase error which is imparted by any of the frontend stages puts an extra burden on the time delay as well as reduces the level of the correlation. In transmission lines the delay is less and much more quantifiable than passives implemented as lumped elements, because lumped element system or even monolithic passives are susceptible to higher degree of process variation or ambient conditions than the Microstrip line filters.

The Microstrip line or Microstrip line +RF-MEMS turn out to be a suitable solution for implementing the BPF, however implementing the BPF this way do have some drawbacks. The primary drawback is off the chip implementation, this brings in the issues of bondwire passives and IC packaging and housing, signal

-80-
corruption and other non-linearities and non-uniformities into the context. However, a careful understanding of these issues while designing the subsequent stage (LNA) is applied then the effect of these non-uniformities can be mitigated to certain extent. These non-uniformities play similar role in any other lumped element filter, therefore under the circumstances it can be discerned that the performance and requirement met of Microstrip line filter suits more than the any other implementation method.

At the system level looking at the specifications requirement Vs the choice of topology, a comparison is made between the chebyshev and elliptic filters and is modeled in MATLAB.

1. Chebyshev (type2, order 8): In the Figures 3.30 and 3.31 below, we see the PSD of in-band interferes, which are Wi-Max and IEEE802.11b/g and Bluetooth and IEEE802.11a/n or WLAN. The maximum level of interferer signal at the antenna is taken to be -10dBm. The filter is modeled for the rejection of 50dB and it can be seen from the response that in the bandpass filter only a notch of around 15dB (total of 65dB) in addition to the overall rejection.

![Figure 3.30: The Total Noise PSD levels for UWB (In-Band and Out-Band both)](image)
2. Chebyshev (type1, order 8): Taking the same input conditions as in the previous case, for the interferers; modeling the filters based on the Chebyshev Type1 function.

In the Figure 3.33 below the filtered response of Chebyshev-1 is shown, if compare the two responses we find that the notch has significantly disappeared and also the rejection is 30dB@ Wi-Max and IEEE802.11b/g and Bluetooth, while due to the implementation of a wideband notch the rejection levels
drop to 50-60dB. This topology also provides the desirable rejection however the simulated value comparison makes Chebyshev-2 a better choice than the Chebyshev-1.

![Figure 3.33: The Total Noise PSD levels after the Filtration for UWB (In-Band and Out-Band both)](image)

3. Elliptic Filter (Order 8): Testing and analyzing filter response of an elliptic filter and comparing it with previous responses. Since the PSD levels of the total interferes (noise) are the same, therefore just the filtered response of the Elliptic Filter is shown in the Figure 3.34 below. The analyses of the response shows that Elliptic filter does provide the faster roll-off from stopband to passband than the Chebyshev filter, however the attenuation obtained is low and typically comparable to Chebyshev-1 response.

Therefore the simulation results show that the appropriate choice of filter would be a Chebyshev-2 type. The filters in general can be further refined from the basic system level design by using the algorithm devised for the orthonormal filters using the wavelets [44, 23]. This algorithm focuses on the optimization of the filter response in frequency domain by windowing the response using the wavelets and finding the more optimized scalar coefficients. But, the application of this algorithm for the wideband BPF system will not be as useful as for the narrowband filtered response, despite the fact that the windowed responses can be scaled up and down using a constant factor. This scaling factor if raised in its value in order to compensate the entire 7.5GHz bandwidth then it effects the ‘resolution’, that is trade-off within degree of optimization and the filter response. Therefore, a conventional and optimized Chebyshev-type2 filter is proposed for the bandpass filter. The primary objective of the proposed BPF is to shield the active front end from all the interferers (most rejection for interferers till 3.7GHz) and the any development of the Intermodulated products. Looking from the circuit level aspect, the use of filter between the Antenna and
LNA, will not only solve the major problem of the interferers to a higher degree, but will also provide isolation for the LO and interferer feedthrough, which is of concern in the direct downconversion topology.

![Figure 3.34 The Total Noise PSD levels after the Filtration for UWB (In-Band and Out-Band both)](image)

3.1 Band Reject Filter (5GHz-6GHz stop band): In this section a second filter is proposed at the system level, the proposed band reject filter is to be placed after the LNA. The function of this filter is to provide a notch or have a stop band in 4.9-5.9GHz frequency range. The topology and requirements for this filter are very much similar with the propose Band Pass filter, apart from the functionality that here a band reject filter is proposed.

The other big merit of this design apart from cleaning the UWB signal is to increase the port to port isolation between the LO and the LNA port. When the stop band reject be implemented than the LO, whose oscillating frequency is inside this region sees highest rejection or port to port isolation on its feedthrough path towards the antenna and LNA. Also implementing filter separately will provide further head room to increase the gain of LNA, with less design complexity and less power consumption also.

The Time and Frequency domain interplay: The uniqueness of ir-UWB relies in the principle that pulses of nano-pico seconds duration in time domain, when seen in the frequency domain covers a wideband. The pulses are modulated and shaped specifically in order to meet the FCC mask requirements and cover the
entire bandwidth of 7.5GHz. The area under the PSD curve shows the total energy associated with the signal and when a signal is processed the total area under the curve changes. The signal processing in the receiver’s frontend as well as any other electrical circuitry happens in the time domain and its effect is seen in the frequency domain, after expressing the signal in the form of its Power Spectrum. This interplay between time and frequency domain can be used advantageously in order to process, shape or code the information in a signal in an efficient manner. As explained earlier the necessity of filtering received UWB signal, this step does help in making the received signal free from the interferers but at the cost of loss of information.

The selection of lower cut-off frequency for the band-pass filter around 3.7GHz is necessary; however, this results in the loss of the information between 3.1GHz to 3.8GHz frequency levels. Similarly, the filtering of IEEE802.11a/n interferer through the band-pass filter, antenna and LNA + Band-reject filter [23] results in the loss of information between the 5GHz to 6GHz frequency levels. If we see the PSD graph of any of the pulse used as a signal/carrier in ir-UWB, it is evident that the major concentration of signal power spectrum is central that is concentrated around the UWB band central frequency. Therefore, the major portion of the coded information, which exists in 5GHz -6GHz frequency range is also filtered out along with the interferer. The Figure 3.35 below shows the filtered PSD levels and loss of information during filtering of the interferers.

![Figure 3.35: UWB Spectrum after bandpass filter](image)
An Oscillator System for UWB QDAcR

The one and most rational solution to this problem is to have a proper pulse shaping and modulation scheme in the time domain, which when plotted in frequency domain shows a possible notch or low PSD levels in the 5GHz to 6GHz frequency region. This recommendation if implemented will not only help the information from getting lost but it will also provide a great ease in the filtering of the existing interferers in the specified bandwidth and also alleviate the problem of the DC-offsets, which significantly degrade the performance of the QDAcR or Homodyne receivers in particular. As described in section 2.2, the QDAcR employs the principle of band downconversion by using LO and this principle results in the form of convolution of all the information present around the LO frequency to the DC levels, which is then lost and filtered out unprocessed by the subsequent band-pass filter stage.

The composite effect of the bandpass filter after the antenna and a band stop filter after the LNA and proper pulse shape modeling results in the processing of a higher amount of the stipulated 7.5GHz bandwidth in comparison to the QDAcR proposed in [8]. Considering the LO frequency to be the same 5.5GHz as given in [lee-bgga] then the UWB band is downconverted from DC to 5.1GHz, and the WLAN interferer shifted between DC to 500MHz range. If downconverted band is filtered by another bandpass filter or a highpass filter with lower rejection frequency to be 500MHz, then we achieve a bandwidth of 4.6GHz to process, which is a significant increase of 105% more information bandwidth then the previously proposed QDAcR architecture.

4. The Oscillator Block: In this section, application of previously described MATLAB model of LO is presented. This section precedes the LNA modeling, as firstly the main objective of this thesis is to model an oscillator for the QDAcR, find the desired phase noise for various pulses. Followed by narrowing down on the choice of the pulse for further modeling and transfer the system level specifications into a circuit. In section 2.4 & 2.5 the mathematical modeling of an oscillator in MATLAB has already been described in detail and in this section the LO is tested for different pulses, to find out the lowest phase noise requirements for QDAcR in order to have a desirable Auto-Correlation levels. The desired phase noise is induced by controlling the timing jitter variance for the AWGN channel, the Phase Noise vs. Auto Correlation graph is plotted which signifies the importance and requirements of phase noise in QDAcR.

First step in simulation is to zero upon the frequency of the oscillation. This decision is influenced by the following factors, position of the interferers and their Intermodulated products, the central frequency of the UWB Bandwidth, which is 5.733GHz and the specifications of the succeeding bandpass filter stage after downconversion. Looking at the interference table it is visible that the main in-band interferers is WLAN (considering that all other interferences are filtered by the BPF after the antenna and so are their possible Intermodulated products) and that the WLAN as well as possible second order products reside in the 5GHz to 6GHz frequency bandwidth. Therefore, the appropriate frequency turns out to be 5.5GHz which will put the interferers and Intermodulated products in between DC and 500MHz band. Considering the second
dominant factor of the central frequency which is 5.733GHz, the central frequency is important as the information band should be downconverted equally on both sides of the DC; otherwise its consequences will be seen in the circuit designing. As most of the circuits are designed based on the specifications, which are derived from the modeling of the Single Sideband Spectrum (SSB), also because of unequal distribution the performance of the QDAcR (Homodyne) receiver will degrade. The difference between the central frequency and 5.5GHz is 233MHz, in order to divide this difference equally across the DC the LO frequency should be equal to 5.615GHz.

The next step involves finding the appropriate phase noise that QDAcR can tolerate, while having auto correlation of 85% or more. The significance of phase noise has already been explained in detail in the previous sections throughout this chapter, from the circuit designer perspective phase noise holds prominent importance in LO or transceiver circuit design as there exist trade off between the phase noise, power consumption, the choice of particular oscillator topology and LO circuit complexity. These trade-offs are explained in more detail in the next chapter; besides this phase noise is a most important factor in deciding the Figure of merit (FOM) of an oscillator. The phase noise graphs for different pulses are plotted here under, the phase noise is induced by inducing the jitter, which is controlled by the amount of noise perturbation that in turn is controlled through the variance introduced in the signal through the AWGN block. The phase noise model runs for different values of phase noise and noticing the amount of correlation between the signal levels without any perturbation and with phase noise. The data for different pulses is tabulated and plotted, at an offset frequency of 1MHz, with modeled NBIs, LNA and proposed BPF filter stage.

a) Gaussian Pulse: The phase noise specifications for the Gaussian pulse are modeled here. The result is presented in the tabulated and graph form and it can be seen that the correlation levels of 90% or more is achievable for the phase noise of Figure 3.36 of -75dBc/Hz @ an offset of 1MHz.

<table>
<thead>
<tr>
<th>Jitter ((\sigma), sec)</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Correlation Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>1e-09</td>
<td>-15.537907</td>
<td>0.45334</td>
</tr>
<tr>
<td>5e-10</td>
<td>-21.5585038</td>
<td>0.57471</td>
</tr>
<tr>
<td>1e-10</td>
<td>-35.537907</td>
<td>0.66967</td>
</tr>
<tr>
<td>5e-11</td>
<td>-41.5585038</td>
<td>0.73108</td>
</tr>
<tr>
<td>1e-11</td>
<td>-55.537907</td>
<td>0.8112</td>
</tr>
<tr>
<td>5e-12</td>
<td>-61.5585038</td>
<td>0.85178</td>
</tr>
<tr>
<td>1e-12</td>
<td>-75.537907</td>
<td>0.9475</td>
</tr>
<tr>
<td>5-13</td>
<td>-81.5585038</td>
<td>0.9877</td>
</tr>
<tr>
<td>1e-13</td>
<td>-95.537907</td>
<td>0.99999</td>
</tr>
</tbody>
</table>

Table 3.1: Depicting the values of the Phase noise induced and the Correlation levels achieved.
The following Figures 3.37 and 3.38 show, the frequency response of the In-Phase signal before and after downconversion of the signal and the Figure 3.39 shows the transient response of the I/Q downconverted Signal. The responses are under real condition, it means under the noisy channel and interference filtering. It is clearly visible from the comparison of the two power spectrums of the signal that the entire band get downconverted around the LO frequency and shifts to the DC. The In-Phase and Quadrature downconverted signal is shown in the time domain, also verifies the validity of the modeling and downconversion.
An Oscillator System for UWB QDAcR

Figure 3.37: The Spectrum Before Downconversion

Figure 3.38: The Downconverted Spectrum

-89-
b) Gaussian Mono Pulse: In the following table 3.2 and graph the phase noise requirement for the Gaussian mono pulse is plotted in Figure 3.40

<table>
<thead>
<tr>
<th>Jitter (σ, sec)</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Correlation Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>1e-09</td>
<td>-15.537907</td>
<td>0.52618</td>
</tr>
<tr>
<td>5e-10</td>
<td>-21.5585038</td>
<td>0.6384</td>
</tr>
<tr>
<td>1e-10</td>
<td>-35.537907</td>
<td>0.7298</td>
</tr>
<tr>
<td>5e-11</td>
<td>-41.5585038</td>
<td>0.7995</td>
</tr>
<tr>
<td>1e-11</td>
<td>-55.537907</td>
<td>0.8817</td>
</tr>
<tr>
<td>5e-12</td>
<td>-61.5585038</td>
<td>0.93118</td>
</tr>
<tr>
<td>1e-12</td>
<td>-75.537907</td>
<td>0.9875</td>
</tr>
<tr>
<td>5e-13</td>
<td>-81.5585038</td>
<td>0.99973</td>
</tr>
<tr>
<td>1e-13</td>
<td>-95.537907</td>
<td>0.99999</td>
</tr>
</tbody>
</table>

Table 3.2: Depicting the values of the Phase noise induced and the Correlation levels achieved.
It can be seen that the Gaussian mono requires less phase noise for the same correlation coefficient in comparison to the Gaussian Pulse. The interferers, signal levels, as well as the LO signal are the same for all the pulses, which means that the dispersion of the power spectrum of the LO signal will be the same for all the pulses. Therefore, this scenario can be looked upon as that Gaussian mono pulse offers better correlation than the Gaussian pulse. This is also proves the analogy; that some pulses offer better spectral efficiency in terms of higher roll off at the desired frequencies than the others. The following Figures 3.41 and 3.42 show the downconversion of the filtered band, first Figure showing the spectrum before the downconversion and second showing
Figure 3.41: The Signal Spectrum for Gaussian Mono Pulse before Downconversion

Figure 3.42: The Signal Spectrum for Gaussian Mono Pulse after Downconversion
c) Gaussian Doublet Pulse: The Second Derivative of a Gaussian is used as an UWB pulse RF signal in QDAcR and the phase noise analysis of QDAcR for the Gaussian Doublet is presented here. It can be seen that Gaussian Doublet too require a less phase noise in comparison to Gaussian pulse for same value of correlation coefficient, as explained earlier because the spectral efficiency of the doublet is better than the Gaussian pulse. The table 3.3 and graph in Figure 3.43 below show the data from the modeling of the phase noise Vs. Correlation for the Gaussian doublet pulse.

<table>
<thead>
<tr>
<th>Jitter ((\sigma_v), sec)</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Correlation Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>1e-09</td>
<td>-15.537907</td>
<td>0.4992</td>
</tr>
<tr>
<td>5e-10</td>
<td>-21.5585038</td>
<td>0.5803</td>
</tr>
<tr>
<td>1e-10</td>
<td>-35.537907</td>
<td>0.70412</td>
</tr>
<tr>
<td>5e-11</td>
<td>-41.5585038</td>
<td>0.7747</td>
</tr>
<tr>
<td>1e-11</td>
<td>-55.537907</td>
<td>0.8704</td>
</tr>
<tr>
<td>5e-12</td>
<td>-61.5585038</td>
<td>0.9218</td>
</tr>
<tr>
<td>1e-12</td>
<td>-75.537907</td>
<td>0.9738</td>
</tr>
<tr>
<td>5-13</td>
<td>-81.5585038</td>
<td>0.9993</td>
</tr>
<tr>
<td>1e-13</td>
<td>-95.537907</td>
<td>0.99999</td>
</tr>
</tbody>
</table>

Table 3.3: Depicting the values of the Phase noise induced and the Correlation levels achieved.

Figure 3.43: Phase Noise requirement Vs. Correlation Coefficient for Gaussian Doublet Pulse
d) Morlet Wavelet Pulse: The phase noise requirement of QDAcR is modeled for the Morlet wavelet of a Gaussian Pulse. The phase noise graph of Morlet wavelet function as shown in Figure 3.44 is very similar to the Gaussian Doublet graph, though the spectral efficiency that is the rate of roll off the edges at the cut-off frequencies is not similar to Gaussian doublet. If we notice the spectrum graph carefully in Figures 3.45 and 3.46 then we see that due to the shape of morlet wavelet pulse the notch near the LO frequency, betters the spectral efficiency after downconversion hence providing higher correlation than the anticipated one.

<table>
<thead>
<tr>
<th>Jitter ($\sigma$, sec)</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Correlation Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>1e-09</td>
<td>-15.537907</td>
<td>0.487</td>
</tr>
<tr>
<td>5e-10</td>
<td>-21.5585038</td>
<td>0.5883</td>
</tr>
<tr>
<td>1e-10</td>
<td>-35.537907</td>
<td>0.7138</td>
</tr>
<tr>
<td>5e-11</td>
<td>-41.5585038</td>
<td>0.78203</td>
</tr>
<tr>
<td>1e-11</td>
<td>-55.537907</td>
<td>0.8417</td>
</tr>
<tr>
<td>5e-12</td>
<td>-61.5585038</td>
<td>0.903</td>
</tr>
<tr>
<td>1e-12</td>
<td>-75.537907</td>
<td>0.9714</td>
</tr>
<tr>
<td>5e-13</td>
<td>-81.5585038</td>
<td>0.9991</td>
</tr>
<tr>
<td>1e-13</td>
<td>-95.537907</td>
<td>0.9999</td>
</tr>
</tbody>
</table>

Table 3.4: Depicting the values of the Phase noise induced and the Correlation levels achieved.

Figure 3.44: Phase Noise requirement Vs. Correlation Coefficient for Morlet Wavelet
An Oscillator System for UWB QDAcR

Figure 3.45: The Signal Spectrum for Morlet Wavelet Function before Downconversion

Figure 3.46: The Signal Spectrum for Morlet Wavelet Function after Downconversion
e) Daubechies’s Wavelet function of Gaussian Pulse: The phase noise analysis of QDAcR for the Daubechies’s’ wavelet function as RF input signal is shown below in Figure 3.47. If we compare Daubechies’s’ wavelet with the Gaussian pulse, then it is visible that Daubechies’s’ wavelet resembles Gaussian with ringing at the higher cut off frequencies. The same similarity we find in the phase noise vs. correlation graph of these two pulses.

<table>
<thead>
<tr>
<th>Jitter ($\sigma$, sec)</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Correlation Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>1e-09</td>
<td>-15.537907</td>
<td>0.4618</td>
</tr>
<tr>
<td>5e-10</td>
<td>-21.5585038</td>
<td>0.5792</td>
</tr>
<tr>
<td>1e-10</td>
<td>-35.537907</td>
<td>0.67315</td>
</tr>
<tr>
<td>5e-11</td>
<td>-41.5585038</td>
<td>0.74308</td>
</tr>
<tr>
<td>1e-11</td>
<td>-55.537907</td>
<td>0.8177</td>
</tr>
<tr>
<td>5e-12</td>
<td>-61.5585038</td>
<td>0.87802</td>
</tr>
<tr>
<td>1e-12</td>
<td>-75.537907</td>
<td>0.95916</td>
</tr>
<tr>
<td>5e-13</td>
<td>-81.5585038</td>
<td>0.9981</td>
</tr>
<tr>
<td>1e-13</td>
<td>-95.537907</td>
<td>0.9999</td>
</tr>
</tbody>
</table>

Table 3.5: Depicting the values of the Phase noise induced and the Correlation levels achieved.

![Figure 3.47: Phase Noise requirement Vs. Correlation Coefficient for Daubechies’ Wavelet](image-url)
f) SINC Function Pulse: As it is noticed in the RF Input description of the QDaCr that SINC function poses to be an ideal pulse for the UWB communication, with high spectral efficiency and the same is reflected in phase noise vs. correlation result. The SINC function achieves the high correlation for the lower phase noise in comparison with all other pulses. The graph Figure 3.48 below shows the phase noise vs. correlation for SINC. The RF signal and downconverted spectrum are shown in Figures 3.49 and 3.50.

<table>
<thead>
<tr>
<th>Jitter ($\sigma_v$, sec)</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Correlation Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>1e-09</td>
<td>-15.537907</td>
<td>0.5283</td>
</tr>
<tr>
<td>5e-10</td>
<td>-21.5585038</td>
<td>0.6428</td>
</tr>
<tr>
<td>1e-10</td>
<td>-35.537907</td>
<td>0.74331</td>
</tr>
<tr>
<td>5e-11</td>
<td>-41.5585038</td>
<td>0.8526</td>
</tr>
<tr>
<td>1e-11</td>
<td>-55.537907</td>
<td>0.89771</td>
</tr>
<tr>
<td>5e-12</td>
<td>-61.5585038</td>
<td>0.9376</td>
</tr>
<tr>
<td>1e-12</td>
<td>-75.537907</td>
<td>0.989</td>
</tr>
<tr>
<td>5e-13</td>
<td>-81.5585038</td>
<td>0.99998</td>
</tr>
<tr>
<td>1e-13</td>
<td>-95.537907</td>
<td>0.99999</td>
</tr>
</tbody>
</table>

Table 3.6: Depicting the values of the Phase noise induced and the Correlation levels achieved.

Figure 3.48: Phase Noise requirement Vs. Correlation Coefficient for SINC Pulse
Figure 3.49: The Signal Spectrum for SINC function before Downconversion

Figure 3.50: The Signal Spectrum for SINC function after Downconversion
The graph as Figure 3.51 shown below summarizes the phase noise vs. correlation plots for different pulses into a single plot. It is visible from the graph below that SINC and Gaussian Mono are the best pulses in the group of pulses which is being tested as ir-UWB RF input signal. This result totally coincides with the findings in the RF input signal section and has been explained, as the spectral efficiency of pulses, which helps them correlate better than other pulses.

**Figure 3.51: The Phase Noise vs. Correlation Coefficient for different pulses**

The significance of the Figure 3.51 is that, it gives an insight into the phase noise requirement of an ir-UWB Oscillator, which is of utmost importance in designing ir-UWB downconverter. The result holds its uniqueness because the result obtained is a resultant of through quantitative analysis and complete system level modeling. The approach is fundamental because it takes whole QDAcR system in consideration and modeled for a very much realistic scenario. The phase noise specifications for QDAcR are reported for the first time and among the first in ir-UWB transceiver category.
As mentioned earlier that phase noise specification set the base for circuit designer to choose the correct topology, trade-offs in order to optimize the circuit design, therefore the obtained results are necessary as well as form the base for circuit design of ir-UWB oscillator and henceforth downconverter.

5. The Low Noise Amplifier Block (LNA): For the purpose of complete QDAcR modeling, LNA is also modeled in MTLAB. LNA is modeled for the optimization of the desired gain at the minimized noise Figure levels simultaneously for the maximum auto-correlation levels. The prime parameters that govern the functioning of LNA are stability, input/output matching, low noise Figure, linearity and high gain. Every parameter is important and there exist certain trade-offs, which designer has to take care of in order to have an optimum solution. The stability and maximum stable gain, are largely device dependent parameters therefore S-parameters of the device has to be known at the system level in order to model. Second, major parameter that is also partially device dependent (bias) and dependent on the strength and position of the interferers is ‘Linearity’. The importance having a high linear system and high gain stages at the same time is a necessity of ir-UWB receivers and QDAcR in particular has been discussed earlier in previous sections; therefore our main focus in LNA modeling is to optimize Gain and Noise Figure for correlation level of 85% or more.

Here a generic model of LNA for ir-UWB (QDAcR) is proposed, with the following assumptions that input and output impedance of the LNA sees 50 Ohms of Source and Load impedances and is matched. In reality, there exists a trade-off between noise Figure and input matching and use of feedback mechanism do ease this trade-off, but it is largely topology dependent, second that assumption that LNA provides same gain for the entire bandwidth that is a flat gain over the entire bandwidth, third the noise Figure (NF) remains same for the entire band, as in real circuit design parameter change with change in the frequency, signal, bias etc. Therefore, these quantities are considered to be stable or as average value over the entire bandwidth. Low noise amplifier is treated as a gain block and is placed as a black box in the noise block as shown in the Figure 3.52 below. The noise is induced in the signal, by the AWGN noisy channel, where the noise spectrum is controlled by the variance. The input to any stage is from the preceding stage and the very first stage has noise floor equal to the receiver’s thermal floor. As, explained in the Noise block description that all the active devices are considered as black box and that the final noise Figure is calculated by having the ratio of input SNR to the output SNR.
The model needs black box parameter that is gain in case of LNA as input and the other input is variance of the AWGN channel to calibrate the system to the desired Noise Figure. The LNA is simulated for various noise Figures pertaining to One particular value of gain and then gain is sweep over different values. The correlation is noticed by comparing the fundamental signal with the iterations, that is for every gain, the autocorrelation levels are noticed when noise Figure is ‘1’ that is the system is totally noiseless and this signal is termed as “fundamental”, then for different values of noise Figure the correlation levels between the transient signal and fundamental signal are calculated. The data is first tabulated and then plotted.

<table>
<thead>
<tr>
<th>Gain (dB)</th>
<th>12</th>
<th>14</th>
<th>15</th>
<th>16</th>
<th>18</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise Figure(dB)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td>99.57</td>
<td>99.66</td>
<td>99.71</td>
<td>99.75</td>
<td>99.80</td>
</tr>
<tr>
<td>3</td>
<td>98.8</td>
<td>99.047</td>
<td>99.18</td>
<td>99.09</td>
<td>99.25</td>
</tr>
<tr>
<td>3.5</td>
<td>98.35</td>
<td>98.6</td>
<td>98.47</td>
<td>98.45</td>
<td>98.516</td>
</tr>
<tr>
<td>4</td>
<td>97.38</td>
<td>97.9</td>
<td>97.94</td>
<td>98.014</td>
<td>98.171</td>
</tr>
</tbody>
</table>

Table 3.7: The Noise Figure and Gain dependency on Auto-Correlation

The graph plotted below shows the correlation for different noise Figures and sweep for different gains. The result is quite interesting as it shows not much deviation or change in the correlation value with respect to the Noise Figure. The reason is inside the mechanism of distribution of the noise on signal and the autocorrelation architecture of the QDAcR. If mechanism be described, the noise interacts with the LNA input signal in 3 ways, it either modulated the Amplitude of the signal (AM) or partially results in the phase modulation of the signal (PM) or AM to PM conversion and rest acts as a thermal floor. As it is shown in the previous section while modeling the LO that QDAcR does not require high phase noise specifications in comparison to the narrowband system, so does the Phase modulation does not result in much of the signal distortion in different active stages. Second, the noise present in the signal as amplitude modulated

-101-
auto-correlates with the delayed amplitude modulated signal, since the two correlated signal are subjected to the same frontend and stochastic perturbations therefore the net effect of such perturbations is reduced and is distributed over a bigger bandwidth or averaged out over a big frequency range.

The succeeding stage to LNA in proposed QDAcR is a band stop filter, which has already been described in detail in the earlier section. The separate inclusion of bandstop filter not just helps cleaning the bandwidth from the interferers, but also eases the complexity of designing a combined LNA and a filter. The main focus is behind having the largest possible stable gain over the entire bandwidth, which is required in order to improve the signal levels and improve the overall Noise Figure and linearity of the QDAcR.

3.5 Conclusion

The main results obtained in this chapter are summarized as follows. The complete system level modeling in matlab of a QDAcR is presented, which provided with vital specifications pertaining to the Downconverter design. The first highlight of this analysis was the use of filters that increased the bandwidth utilization to 76%, also it was shown that time-frequency domain relationship if exploited properly using pulse shaping, then the use of bandwidth can be more efficient. The main highlight was the designing of downconverter for the first time it was shown that a Q-VCO with a phase error of 5degrees
An Oscillator System for UWB QDAcR

and a phase noise of -90dBc/Hz @ 1MHz offset suffices to an autocorrelation of 90% or more for a QDAcR. The modeling and analysis of different possible pulses highlighted the importance of pulse shaping and high spectral efficiency, it finally resulted in the choice of Sinc and Gaussian Mono as the two most efficient pulses for QDAcR. The noise modeling of complete QDAcR provided with the specs in form of Link budget analysis and LNA design. The analysis of LNA provided with the specs of gain and noise figure for optimal correlation.

The circuit design of oscillator for QDAcR is presented in the next section.
Section II

Methods and Techniques for Circuit Level Designing

This section comprises of two chapters, which describe the adopted methodology while designing the circuits for an Oscillator System for impulse radio Quadrature Downconversion Auto-Correlation Receiver. The underlying problem statement is to design a Quadrature Voltage Controlled Oscillator, which meets the specifications that were derived in the previous section (system level analysis of QDAcR).

The problem is approached in a systematic fashion; throughout the design, the problems pertaining to the process technology are being sincerely addressed from the very initial of schematic design levels, so that not much deviation should be noticed between the results obtained at schematic simulation and post layout simulations. This is done by proper component modeling and understanding the process related problems (PVT effects) characterized for generalized components in IBM (130nm node, CMRF8SF) process technology Design Manual.

Initially starting with the understanding of the Oscillator system in Chapter 4. In chapter 4, we further proceed with the choice of oscillator topology and identification of key elements in circuit design that define and translate into performance of an oscillator. This leads to the exploration of merits and demerits posed by different LC-Tank Oscillators, namely Differential NMOS, PMOS and Complementary Oscillators. The choice of Oscillator Topology and passive elements is made based on the analysis of circuit simulation results, while meeting the specifications and targeting low power consumption.

Chapter 5 describes the circuit level implementation of Quadrature Voltage Controlled Oscillator (Q-VCO), starting with the principles and methods of Quadrature generation followed by a circuit design description and discussion about the cross coupled-VCO. The two topologies for Q-VCO were designed and analyzed, these were parallel-coupled Q-VCO and series coupled Q-VCO. The result provided us with a realistic solution to our problem that is a Q-VCO for QDAcR. Furthermore, we investigated Oscillator-Polyphase filter topology, which can be another possible solution, because of its advantages like less chip area and power consumption. Last section related to circuit design in this chapter deals with the design of output buffers for an oscillator system. The buffer is analyzed for its load driving capabilities, power consumption, harmonic output and its loading effect on the oscillator. In these two chapters the complete design procedure is explained, while the results are analyzed with respect to the degree they meet the specifications.
The Q-VCO circuit is designed in IBM (130nm node, CMRF8SF) process technology. The desired specification set for Q-VCO, which were derived in system analysis is as follows.

Design Specifications:
Phase Noise (Spectral Purity): A minimum phase noise of -90dBc/Hz at and offset of 1MHz is required in order to near perfect auto-correlation.
Phase Error: The maximum perceivable Quadrature Phase Error is 4 degrees.
Final Output Signal Power (Buffer Output): A minimum signal level of -5dBm Vpk-pk is required for driving mixer and providing necessary conversion gain.
Tuning Range: As derived earlier that for ir-UWB QDAcR system the Oscillator should run at fixed frequency 5.6GHz, with a tolerance of ±117MHz. This simplifies the design by negating the use of a Phase Lock Loop (PLL). However in order to countermand the Process, temperature and supply voltage (PVT) effects the Oscillator should have a minimum of ±5% tuning range.
Power Consumption: Though none specifications were provided or derived regarding power consumption by the Oscillator system, however a sincere effort has been made to keep the power consumption levels to bare minimum, while meeting the desired specifications.
CHAPTER 4

Oscillators: Introduction and Circuit Design Methodology of Negative Transconductance (-$G_m$) Voltage Controlled Oscillator

Voltage Controlled Oscillators (VCOs) over the years have served as an integral part in RF transceiver design. VCO are mainly used for signal processing jobs like Upconversion/Downconversion of modulated baseband/RF signals, frequency selection or synthesis or the generation of reference periodic signal in time domain (clock) in modern Digital Circuits. The VCO design has continuously advanced over the years owing to developments and innovations in semiconductor process technology, packaging and better understanding of circuit design problems effecting VCO performance. The development has spanned from the use of vacuum tubes to highly precise low frequency crystal oscillators to present day monolithic oscillator design.

In this chapter an attentive attempt has been made to present the design methodology for -$G_m$ VCO in a concise but effective manner covering all the major trade-offs, design rules and VCO performance related nuances. As we know that performance of a VCO is characterized by the spectral purity of the its signal in frequency domain or accurate periodicity in time domain, which directly translates into two variables that define figure of merit of an Oscillator these are 1. Phase Noise and 2. Timing Jitter. The relationship between and effect of these two variables has been discussed and presented in previous chapters, in this chapter circuit design description starts with the understanding of the term -$G_m$ (Negative Transconductance) and further understanding the rules that lead to the design of an efficient LC-Tank. The effectual design algorithm for optimal LC tank design is presented, in which firstly the rules and results regarding the choice of an inductor are stated followed by rules and theory regarding the implementation and choice of MOS varactors. The succeeding section describes designing of MOS LC-Tank Oscillator, with a very brief description about Single transistor Oscillator and then concentrating on the main goal of designing and characterizing LC-Tank VCO by understanding and exploiting various topologies and validating the findings with the help of simulated results. In end all the major findings are summarized and compared against the specifications.

4.1 Overview of Oscillator Fundamentals

Ideally, an oscillator can be defined as a system that produces stable periodic and sustained signal over an indefinite time span. However, due to non-idealities, the signal strength is decayed over the period of time, signal energy is not totally conserved, resulting in a change in period and signal stability. Therefore, in a refined manner an Oscillator can be described as a system which comprises of a sustainable periodic signal generation block synchronized with a signal compensation block (Amplifier).
The output (voltage signal) of an oscillator can be defined by the equation 
\[ A_{out}(t) = A_{0} \cos(\omega_{o} t + \phi_{0}(t)) \]
where \( A_{out}(t) = V_{out}(t) \) is LO output at time \( t \), where \( A_{0} = V_{0} \) is the maximum signal (voltage \( V_{0} \)) swing amplitude of LO, the angular oscillation frequency is \( \omega_{o} \) and a constant phase reference of \( \phi_{0}(t) \).

Based on phase response oscillator can be divided into single phase and multiphase output oscillator; beside phase noise and signal output power, one of the figure of merit for multiphase oscillator is the accuracy between the phase responses. The figure 4.1 below shows the model of an oscillator based on the above discussion. Where \( X(s) \) is the input signal, \( A(s) \) the Amplification function, \( H(s) \) the frequency selective / shaping function and \( Y(s) \) as Oscillator output.

**Figure 4.1: Oscillator Block Diagram**

Obtaining the transfer function

\[
\frac{Y(s)}{X(s)} = \frac{A(s)}{1 - A(s)H(s)} \quad (4.1)
\]

Now solving the above equation for \( s = jo_{0} \), for sustained and indefinite oscillation, we obtain the following conditions

\[ |A(a_{0}).H(a_{0})| = 1 \quad (4.2a) \]

\[ \angle A(a_{0}).H(a_{0}) = 2n\pi; n \in Z \quad (4.2b) \]

Where the set of equations numbered 4.2a and 4.2b forms the Barkhausen’s Criteria. The equation 4.2a implies that the loop gain should be a minimum of ‘1’ in order to start and sustain the oscillations and the condition for phase stability is given by equation 4.2b.

Developing the model for electrical oscillator based on the Barkhausen’s criteria, in this case the startup signal \( X(s) \) is replaced by the white noise, which is then amplified by the amplifier block. The noise is then shaped by the narrowband frequency selective filter \( H(s) \); the signal is fed back to the input through
positive feedback loop formed by the amplifier and narrow band filter block. If the loop gain condition is satisfied the oscillation starts at angular frequency \( \omega_q \) and the signal amplitude continuously grows until it saturates and reaches the peak value. The frequency selective (narrowband) filter implemented by \( H(s) \) ensures single harmonic oscillation that is why commonly known as harmonic oscillator and the oscillator in which the narrowband filter is implemented using passive LC-network is commonly known as LC-Oscillator.

The other type of oscillator is Relaxation Oscillator, which employs the principle of charging and discharging of capacitor through a non-linear element. Due to the use of highly non-linear component, the relaxation oscillators consists of different harmonic components, which translates to the fact that for the same power consumption relaxation oscillators show poor phase noise performance in comparison to the LC-tank oscillators. Owing to non-linear mechanism, relaxation oscillators are not totally sinusoidal; they have typically a saw tooth or a distorted square wave output. A typical example of relaxation oscillator is Ring Oscillator, which forms a ring using an odd number of inverter stages. The oscillation frequency is decided by the switching time \( \tau_p \) and the number of inverter stages used, switching time is determined from the switching current and RC-network time constant at the gate of the inverters. Ring Oscillators can be designed to have a high tuning range by controlling the switching current and number of inverter stages, while consuming comparatively less die area and this gives them a formidable advantage over LC-oscillators. A comparison between the two Oscillators is presented in the table below.

<table>
<thead>
<tr>
<th></th>
<th>LC (Harmonic) Oscillators</th>
<th>Ring (Relaxation) Oscillators</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Noise</td>
<td>High ‘Q’ resonator. Good</td>
<td>Poor</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>Low Power required for same phase noise</td>
<td>Higher Power required for same phase noise.</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>Narrow, require use of Capacitive Banks / Varactors at the cost of higher power consumption /poor phase noise</td>
<td>Wide Tuning Range</td>
</tr>
<tr>
<td>Multiphase Output Generation</td>
<td>Requires filter (Poly-Phase), Couple VCOs</td>
<td>Intrinsically Produced</td>
</tr>
</tbody>
</table>

Table 4.1: Comparison between LC-Tank and Ring Oscillator

Considering design specifications specially targeting lower power consumption for a minimum phase noise of -90dBc/Hz @ 1MH offset and non-desirability of wide tuning range. It seems sensible to go for a LC-Tank Oscillator topology instead of Ring Oscillator. Henceforth, the focal point of this circuit design section will be to design and describe a LC-Tank Oscillator.
4.2 Quality Factor (Q-Factor), Impedance Transformation, Single Transistor Oscillators and Differential Oscillators

The output (voltage signal) of a The ‘Q-Factor’ of a system, often relates to the system’s performance and widely considered as figure of merit, which is used to measure efficiency of the system. Therefore, the conventional way in which ‘Q-Factor’ can be described is shown in equation 4.3 below.

\[
\text{Q-Factor} = \frac{2\pi\text{Energy Stored}}{\text{Energy Dissipated per unit cycle}}
\]  

(4.3)

In case of passive elements and their networks, the ‘Q-Factor’ determines the ideality of the component that is the effect of passives on the performance and the efficiency of energy conversion in a network. There are several definitions of ‘Q-Factor’ pertaining to the parameter, which is being measured. Particularly in case of a passive network the Q-factor can be defined as given by the equation 4.4 below

\[
\frac{\text{Im}(Z)}{\text{Re}(Z)} \text{ Q-Factor(series network)} = \frac{\text{Im}(Y)}{\text{Re}(Y)} \text{ Q-Factor(parallel network)}
\]

(4.4)

The Q-Factor for series and parallel networks are interchangeable and simply corresponds to the system ‘Q-factor’. Sticking to these crude definitions of ‘Q-Factor’, we can delve into the concept of Impedance Transformation, which states that impedance can be converted to higher or lower value and from complex to real. The two popular is to convert series networks to higher Q parallel networks or vice-versa. The impedance transformation is widely used in Oscillators in order to ensure the High Q resonator, which in turn results in a better harmonic oscillator. Figure 4.2a and 4.2b shows the impedance transformation from series to parallel network and vice-versa. The series impedance is converted into parallel admittance and the comparison on real and imaginary parts give the transformed values.

Let \( C_s, L_s \) and \( R_s \) be the values of passive in series configuration and \( C_p, L_p \) and \( R_p \) be the corresponding values in parallel configuration. Then the series impedance for the two networks is given by

\[
Z_s = R_s + \frac{1}{j\omega C_s}
\]

for RC network and \( Z_s = R_s + j\omega L_s \) for RL network, converting series impedance into parallel admittance and finding the value of Q-factor according to equation 4.4 we get equation 4.5 the RC network, which is shown below

\[
Y_s = \frac{j\omega C_s R_s + \omega^2 C_s^2 R_s^2}{1 + \omega^2 C_s^2 R_s^2} \text{ and } Q_s = \frac{1}{\omega C_s R_s}
\]

(4.5)

For RL network the value of admittance and Q-factor are given by equation 4.6, as shown below

\[
Y_s = \frac{R_s - j\omega L_s}{R_s^2 + \omega^2 L_s^2} \text{ and } Q_s = \frac{\omega L_s}{R_s}
\]

(4.6)

Comparing the obtained admittance values of equations 4.5 and 4.6 with the admittance values of parallel networks in figure 4.2 and 4.3. It can be deduced that
$R_p = (1 + Q^2) R_s, \quad C_p = \left( \frac{Q^2}{1 + Q^2} \right) C_s$ and subsequently $L_p = \left( \frac{Q^2}{1 + Q^2} \right) L_s \quad (4.7)$

Figure 4.2: RC Network Transformation

Figure 4.3: RL Network Transformation

As it is proverbial from the Oscillator’s generalized definition that for sustained and periodic oscillation an amplification /compensation block is required. In electronic transistor oscillators this block is often implemented by an active device that is a MOSFET or BJT. Now considering an oscillator with single transistor as shown in Figure 4.4a below, it can be seen from the discussed figure that oscillation can be obtained if the positive feedback is imparted to the Base/Gate or Emitter/Source node of the transistor.
Feedback applied to the Base/Gate will fail to provide the positive feedback as for non-inverting input gate node the drain node will act as an inverting output node and vice-versa, thus this configuration will provide negative feedback. However by the use of 1:n transformer (where n being a high valued integer) in the drain/collector and base/gate feedback loop, the oscillation can be achieved. Moreover, at the resonance frequency, the reactance is zero and net impedance seen by the active device is real, which implies that voltage and current are in phase, therefore in order to maintain the same phase the feedback loop should be connected to the emitter/source node. The problem with configuration shown in Figure 4.4a is that the LC-tank is loaded directly and it sees \( \frac{1}{g_{ds}} - \frac{1}{g_m + g_{mb}} \) as resistance, which severely degrades the Q-factor and the loop gain deteriorates less than one and generation of sustainable oscillation is not possible. This is a perfect example where impedance transformation can be applied that is the source impedance would be converted to much higher value and seen in parallel with the LC-tank, which increases the loop gain and provide sustainable oscillation, as shown in Figure 4.4b. [39]

As seen from the Figure 4.4b the importance of impedance transformation resulting in sustained oscillation. This impedance transformation can be implemented in two ways, firstly either by the use of passive network or by use of active stage in feedback. The two well-known topologies namely Hartley Oscillator and Colpitts Oscillator, which are implemented using passive networks and are shown in the Figure 4.5 below. The impedance transformation is achieved by employing Inductive and Capacitive dividers for...
Hartley and Colpitts oscillators respectively. The other concept involves use of an active feedback loop, that uses transistor as an active impedance transforming element, which provides high impedance between the tank and the emitter of the transistor M1. The transistor M2 further increases the impedance between the tank and M1 emitter by transforming the emitter impedance of M1 using the beta transform (as in the case of source follower) to a higher value. The approximated values of equivalent parallel resistance and inductance in case of Hartley Oscillator are given by the expression as follows

\[
R_{eq} = \left( \frac{1}{g_m + g_{mb}} \right) \left( \frac{L_1 + L_2}{L_2} \right)^2 \quad \text{And} \quad L_{eq} = L_1 + L_2
\]

And in case of Colpitts Oscillator \( R_{eq} = \left( \frac{1}{g_m + g_{mb}} \right) \left( \frac{C_1 + C_2}{C_1} \right)^2 \quad \text{And} \quad C_{eq} = \left( \frac{1}{C_1 + 1/C_2} \right)^{-1} \)

![Figure 4.5](image_url)

Figure 4.5: (a) Hartley Oscillator, (b) Colpitts Oscillator and (c) Single Ended Oscillator using a Source Follower as a positive Active Feedback.

In this section fundamentals of positive feedback loop and single transistor oscillators were discussed in brief. The performance of the single device transistors suffers degradation due to its topology constraints. Firstly, in order to have required transformed impedance ratio required for inductive and capacitive dividers should be high enough in order to compensate the loading effect and have higher voltage swing, however the increased use of passives makes the oscillator more susceptible to process variations. Second, in order to have lower noise contribution from drain and gate of the transistor, the bias current should be decreased and the device size should be increased. However, one degrades the voltage swing and other increases the
parasitic and thus decreasing the tuning range. Third, the common mode noise effects are more pronounced in single ended oscillators as the noise due to supply perturbation and substrate noise bound to lower the phase noise and lastly, single ended oscillators are not much suitable for Zero-IF or Low-IF receiver architectures or differentially operated transceiver architectures.

### 4.2.1 Differential Topology Oscillators

The As it could be interpreted from the conclusions drawn at the end of Single Transistor Oscillator analysis that single transistor topology is marred by constraints that limit its use in modern transceiver architectures. The Differential topology offers simplistic solution by reducing the duty cycle by half that is 50% duty cycle as in the transceiver chain generally, oscillator block output drives the gate of Mixer gate thus reduction in duty cycle improves the $\frac{1}{f}$ switching noise contribution [49]. Further differential topology benefits in improving the common mode noise rejection, in circumventing the even harmonics and easing the dependence upon passive impedance transformation networks. The block diagram of a cross-coupled differential oscillator is shown in the Figure 4.6 below.

![Figure 4.6: (a) PMOS cross-coupled differential oscillator with current sink and (b) NMOS cross-coupled differential oscillator with current source.](image)

Due to its posed advantages the differential topology is chosen as the topology of choice for designing oscillation system required for ir-UWB QDAcR. Its nuances and analysis is presented in detail in the subsequent sections.
4.3 -Gm (Negative Transconductance) and LC-Tank Design Essentials

Negative Transconductance acts as a loss compensating negative resistance in parallel with the loss tank resistance. As we know that LC-tank acts a oscillation damping narrow band filter, the damping happens because of the parasitic present in passive components. Therefore, in order to have sustained oscillations a compensating mechanism is put in place, in case differential topology, it is provided by the Transconductance of two transistors. Considering a lossy LC-tank where Rs and Rc denotes total resistive parasitic loss in the inductor and capacitor subsequently, the Figure 4.7 shows the equivalent parallel RLC network obtained by the impedance transformation of the lossy LC network at the frequency of oscillation \( \omega_0 \). Only the resistive transformation is shown at as oscillation frequency the reactance offered by the tank is zero. In Figure 4.7 below the active compensation stage is implemented by Gm stage, transformation from series parasitic resistance to the parallel given by Rp at oscillation frequency in last stage it the negative resistance -'Rp' depicts the compensation provided by active Gm stage.

In case of differential cross couple topology for e.g. the one shown in the Figure 4.5 the negative resistance seen can be approximated by \( R_{asym} = \frac{-2}{g_m} \), now in order to compensate for the losses in the tank, the value of \( R_{asym} \leq R_p \), to be on the safer side and for the surety of sustainable oscillation \( k.R_{asym} \leq R_p \) where \( 2 \leq k' \geq 3 \). Thus, the emergent propositions from this discussion are that the Transconductance offered by the transistor should be high and second that a LC-tank should have as high ‘Q’ as possible.

For the determination of the angular frequency, let us consider the LC-tank with parallel parasitic resistance. impedance of parallel LC-tank is given by the equation 4.8 below

\[
Z_{tank}(\omega) = \frac{\frac{L^2}{j \omega} R_p \omega^2}{\frac{L^2}{\omega^2} + (R_p - LCR_p \omega^2)^2} + j \frac{LR_p \omega^2 (1 - LC \omega^2)}{\frac{L^2}{\omega^2} + (R_p - LCR_p \omega^2)^2}
\]  

(4.8)
As we know that at resonance the imaginary impedance that is the reactance of the tank is zero, therefore at \( \omega = \omega_r \), the value of angular frequency of oscillation is given by

\[
\omega_r = \frac{1}{\sqrt{LC}}
\]  

(4.9)

Similarly the angular frequency of oscillation for LC-tank with parasitic in series is given by

\[
\omega_s = \sqrt{\frac{L - R_s^2 C}{L C - L C R_s^2}}
\]  

(4.10)

It can be discerned that equation 4.10 results in equation 4.9, if the parasitic are negligible. Therefore, once again the statement that LC-tank should consist of passives with least parasitic is in order to have high phase noise is proved. Therefore, the dominant factor is tank ‘Q-factor’, earlier section a very general-purpose definition of Q-factor was presented, which is not applicable in its totality on the LC-Tank, because LC-tank exhibits band-pass filter response as described in [50]. The normalized equation of transfer function is given as

\[
H(s) = \frac{\omega_o s}{s^2 + \omega_o^2 s + \omega_r^2}
\]  

(4.11)

Where Q-tank is given by the expression \( Q_{tank} = \frac{\omega_o}{\Delta \omega} \), where \( \Delta \omega \) is 3dB frequency bandwidth. Considering the equation 4.8 for parallel LC tank, comparing and solving it for equation 4.11, the Q-factor is given as

\[
Q_{tank} = R_o \sqrt{\frac{C}{L}}
\]  

for \( \omega = \omega_r \) the real part of tank impedance given by equation 4.8, that is

\[
\text{Re}[Z(\omega_r)] = R_o = |Z_{pk}|
\]

where subscript ‘Pk’ stands for peak value of the parameter. However at resonant frequency the \( Q_{tank} = Q_{pk} \), therefore, for and only for \( \omega = \omega_r \) it is a valid assumption to write the tank Q-factor as

\[
Q_{tank} = Z_{pk} \sqrt{\frac{C}{L}}
\]  

(4.12)

The reasoning behind formulation of equation 4.2 will be dealt in more detail while characterizing the Inductor for LC-Tank.

**4.3.1 Designing of LC-Tank for Low Power and Low Phase Noise**

In this section the basics regarding design of LC-Tank as given in [51] are discussed, the quantitative analysis provide the clear insight into designing and optimization of the LC-tank for the desired constraint of Low-power as well as targeting the possible low phase noise.

Applying the principle of energy conservation in the tank as shown in figure 4.6, that is the energy stored in the capacitor is equal to the energy stored in the inductor. We get equation 4.13 as shown below

\[
\frac{1}{2} CV_o^2 = \frac{1}{2} LI_s^2
\]  

(4.13)
Where ‘Vo’ and ‘Io’ represent the peak value of voltage and current across the LC-tank, that is voltage across the capacitor and current through the inductor. However, due to parasitic there is power loss or energy dissipation in LC-tank, which is given by equation 4.14 below

\[
P_{\text{loss}} = \frac{1}{2} R_c I_o^2 = \frac{R_c V_o^2}{L} = \frac{R_c V_o^2}{2\omega_o L} = \frac{\omega_o^2 R_c C^2 V_o^2}{2}
\]

(4.14)

from the previous chapters, we know the fundamental equation of phase noise as described by Leeson’s formula as given by equation 2.51. Considering the leeson’s noise for the phase noise contributed due to thermal noise and re-writing equation 2.51, using the relations we figured out in equation 4.12-4.15, as shown in equation 4.15 below

\[
L\{\Delta \omega\} = 10 \log \left[ 2kT(1 + F) \frac{1}{Q_{\text{tank}}^2 P_{\text{loss}}} \left( \frac{\omega_o}{\Delta \omega} \right)^2 \right] = 10 \log \left[ 2kT(1 + F) \frac{R_c C}{L I_o^2} \left( \frac{\omega_o}{\Delta \omega} \right)^2 \right]
\]

\[
= 10 \log \left[ 2kT(1 + F) \frac{1}{R_c I_o^2} \left( \frac{\omega_o}{\Delta \omega} \right)^2 \right] \text{ OR } = 10 \log \left[ 2kT(1 + F) \frac{1}{Z_{\text{in}} I_o^2} \left( \frac{\omega_o}{\Delta \omega} \right)^2 \right]
\]

(4.15)

The equations 4.5,6,7,12,14 and 15 serves as fundamental equations, which characterize the LC-tank. In their treatment of design of LC-tank under the hood of Linear time invariant theory [52,53,54,55] have emphasized on the ratios of inductance \(L\) and series resistance \(R_s\) and the ratio of inductance and the total oscillator capacitance that is \(L/C\). The crux is that \(L/R_s\) should be maximized in order to have maximum phase noise at minimum power consumption and similarly \(L/C\) ratio should be maximized for same desired effects. These propositions are productive in wholesome, however do suffer from limitations. The limitations as well as effectiveness of maximization of \(L/R_s\) and minimization of \(L/C\) are summed up in the table 4.2 below.
<table>
<thead>
<tr>
<th>Passive</th>
<th>Action</th>
<th>Phase Noise</th>
<th>Power Dependency</th>
<th>Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor (L)</td>
<td>Maximize</td>
<td>Improves</td>
<td>Quadratic, Power gain reduces.</td>
<td>Strictly depends upon the designing and characterization of Inductor. Other issues such as Tuning range, chip area, etc.</td>
</tr>
<tr>
<td>Series Resistance (R)</td>
<td>Minimize</td>
<td>Improves</td>
<td>Linear (for 1st order temperature /Parasitic effects)</td>
<td>Characterization and proper design, depends upon the process and technology. For e.g. properties of Metallization layers.</td>
</tr>
<tr>
<td>Total Capacitance</td>
<td>Minimize</td>
<td>Improves</td>
<td>Quadratic</td>
<td>Device sizes for required gain and operation regions. Design Specific, for e.g. the device size and loading of output stage like buffer/mixer etc.</td>
</tr>
<tr>
<td>Amplitude</td>
<td>Minimize - For lower power consumption Maximize – for high phase noise *Balance should be found, based upon the specifications</td>
<td>Improves phase noise, when increased. However, this improvement comes at the cost of more power consumption.</td>
<td>Quadratic</td>
<td>Power Budget, The device reliability (too high swing can break the Cox faster). Power-Phase Noise trade-off.</td>
</tr>
</tbody>
</table>

**Table 4.2: Summation of prepositions as well as limitations**

In this section the fundamentals regarding the LC-tank were presented, which serve, as the basic guidelines while designing LC-tank. However, there are other process or technology and design related factors, which need to be understood as these factors play an important part in optimization of LC-tank. In next section characterization and choice of Inductor and tank capacitance is presented, while understanding and addressing the process related factors.
4.4 LC-Tank Design

The conclusion drawn at the end of all sections lead to the fact that the design of optimized LC-tank is of prime importance and in this section methodology for optimized LC-tank design is presented. Since the advancement in process technology it is possible to fabricate the passives in a monolithic fashion, which has provided designers with degree of freedom by relatively less dependence on the off-chip passives. The off-chip inductors have high Q-factor in comparison with the monolithic inductors; however, the performance of off-chip inductor is severely degraded and marred by problems like the pad capacitance, package pins and interfacing of off-chip inductor with the integrated circuit at RF frequencies.

4.4.1 Inductor Modeling and Characterization

The monolithic inductors are fabricated using metallization layers offered by the technology and in the form of spiral geometries using microstrips. The monolithic inductors suffer from Ohmic and substrate related losses, based on the possible modes of signal propagation ohmic losses can be further classified as skin-effect, slow wave and quasi-TEM modes specially seen on insulating substrates. The skin effect is visible in heavily doped and low resistive substrates as the graph Figure 3.4 in [50] shows that skin effect is visible in substrate with resistivity one or two fold less than 1 Ohm/cm. Since IBM CMF8SF-RF has substrate resistivity between 1-2 Ohm/cm, therefore the skin-effect is not quite evident in this case. If we look graph carefully with respect to the technology parameters it can be figured out that apart from slow wave effect, other ohmic losses will not dominate at the desired RF-frequency and substrate resistivity.

Substrate Losses: the low resistivity of Si substrate results in degradation of Q-factor due to multiple loss mechanism, as explained in detail in [57, 58]. Firstly, considering the Maxwell-Faraday Equation, this physically translates that any change in the magnetic field creates an electric field. The increase in the number of turns results in delocalization of the coil magnetic field in spiral, which is no longer confined to the center of the inductor; which in ideal case should be. The transient magnetic field expands well into the inner turns, which induces the electric field and ultimately generates eddy current in the inner conductors of spiral. Now interpreting Ampere Circuital Law with respect to the generated eddy currents, it results in a magnetic field that is in opposite direction to the spiral magnetic field. This reduction in net magnetic field results in decrease of the inductance value.

The inductance of any spiral with substrate resistivity of higher than 1 Ohm/cm, can be modeled by its compact $\pi$-model as shown in the Figure 4.8 below. The inductance of any spiral can be calculated by scaling the single $\pi$-model by the number of microstrips in a single spiral that is adding in series of inductance, resistance and parasitic capacitances of each $\pi$-model. The shunt arms of the $\pi$-model denote
the inner and outer winding parasitic, therefore denoted by different set of values because of asymmetry in
the inductor layout. Where \( C_0 \) represents the total capacitance that includes mutual coupling capacitance
\( C_m \) in parallel with the capacitance obtained from sum of bend capacitance \( C_b \) and overlapping underpass
parasitic capacitance, as described in detail in Figure 3-12 [50]

![Diagram](image)

**Figure 4.8:** (a) Compact lumped-element \( \pi \)-model of an inductor and (b) Single Port Excitation of
equivalent inductor model.

Grounding the second port in figure 4.8a, applying the impedance transformation of \( \pi \)-model in to simple
parallel circuit as shown in the Figure 4.8b. Where the values of \( R_p \) and \( C_p \) are given by, equation 4.16
below, these represents the approximated total value of the parasitic resistance and capacitance in an
Inductor. The effect of parasitic in an inductor results in inductance loss, the parasitic resistance gives rise
to substrate loss in the form of eddy current and parasitic capacitor begets substrate loss in the form of
displacement current.

\[
R_p = \frac{1}{\omega C_m^2 R_n} + \frac{R_n(C_m + C_p)^2}{C_m^2} \quad \text{and} \quad C_p = C_m \frac{1 + \omega (C_m + C_p) C_p R_p^2}{1 + \omega^2 (C_m + C_p)^2 R_p^2}
\]

(4.16)

The value of ‘Q-factor’ for an inductor can now be defined in a much robust manner.

The net energy stored in an inductor is calculated as

\[
E_{\text{stored}} = \frac{V_\text{in}^2}{2} \left( \frac{L}{(R_p^2 + \omega^2 L^2)} - (C_p + C_n) \right),
\]

where first
denote the magnetic energy stored in an inductor an second part as electrical energy stored in parasitic
capacitor that is why with negative sign.

Now calculating the energy dissipated per oscillation cycle as

\[
E_{\text{diss}} = \frac{2\pi}{\omega} \frac{V_\text{in}^2}{2} \left( \frac{1}{R_p} + \frac{R_p}{R_p^2 + \omega^2 L^2} \right),
\]

therefore

the calculated Q-factor can be given as shown in equation 4.17 below
An Oscillator System for UWB QDAcR

\[
Q_l = \frac{\omega L}{R_s} \left[1 - \frac{R_c^2(C_n + C_p)}{L} - \omega^2 L(C_n + C_p)\right] \frac{R_p}{R_p + \left(\frac{\omega L}{R_s}\right)^2 + 1} R_s
\]  
(4.17)

Or \[Q_s = \frac{\omega L}{R_s} \cdot \text{Self Resonance Factor} \cdot \text{Substrate Loss Factor} \tag{4.18}\]

Or \[\frac{1}{Q_l} = \frac{1}{Q_{\text{Conductor}}} + \frac{1}{Q_{\text{Substrate-Loss}}} \]

The equation 4.18 is important as in order to find an appropriate and optimized inductor for LC-tank it is necessary to understand effect of parasitic in order to characterize the inductor properly.

### 4.4.2 Defining Process Related Parameters*

*The Information is classified and property of IBM – Technologies, therefore the exact details, component design specifications sheet’s screen-shot, graphs and numbers about process related parameters, simulated plots are not (re-)produced in this thesis. However, inductor model was chosen only after study of design manual and model guide and verifying various model parameters and results as given in model guide.

The choice of inductor is a symmetric and differential driven inductor from the IBM CMRF8SF-DM (Dual Metal) process component model library, the advantages of symmetric, parallel and differential driven inductor are explained in detail in [50]. The merits can be highlighted as, firstly, the differential driven symmetric inductor offers approximately twice large Q-factor, because of enhanced mutual coupling between the windings in contrast to single-ended excited inductor, this is can be seen from graph Figure 3-17 of [50] and secondly differential symmetric inductors consumes less area in comparison to single-ended symmetric inductor.

A symmetric inductor with parallel metal lines and differentially driven ‘Symindp’ was chosen from the model library for LC-tank designing. The preliminary investigation was mainly based upon the simulation and reading from the IBM-Design manual and model guide. The geometrical lay out of symindp spiral is octagonal, which poses an added advantage in terms of less acute turning angles, which lessen the current crowding and bend capacitance. Secondly, symindp is more symmetric than a square or hexagonal spiral, because eccentricity of an octagonal structure is lower and closer to a circle than a square or hexagonal structure. Next was about the decision to choose the metallization layers for inductor design, the process offers different combinations for which the simulated and correlated plots of Q-factor and model predicted inductance value with respect to variable temperature and frequency are presented in IBM classified design manual and model guide. The metal layers combination (metal layer 3 and metal layer 2), which shows the
highest value of Q-factor and best correlation values were chosen for preliminary simulations and model comparisons.

The next step was in making a choice for groundplane for an inductor. The choice of proper groundplane is essential towards partial mitigation of substrate losses, this can be explained as shielding of inductor. As it is described in previous section that currents flow into the substrate through capacitive coupling and induced currents through the magnetic coupling, therefore the isolation of inductor from substrate becomes necessary in order to minimize the substrate losses. Therefore, use of rugged / patterned ground plane is done; it is placed above the substrate in order to stop the currents from entering the substrate. The use of groundplane increases parasitic capacitance that adversely effect the inductance and Q-factor value (eq. 4.18) by decreasing the self-resonance frequency, however if the operating frequency is well lower from the self-resonance frequency, the use of groundplane is advisable. The frequency of operation in our case is 5.6GHz, and from the preliminary simulations and design manual data, it is evident that self-resonance frequency is beyond the operational frequency; therefore in inductor designing the groundplane shielding is used. Other downside of groundplane is that due to conducting nature of groundplane, more magnetic currents are induced, but this problem is circumvented by patterning of the ground plane. In patterning the regular nature of groundplane is broken by cutting slots into it, which are perpendicular to the direction of magnetic current flow. These slots further reduces the loop length, thus magnetic current circulate in much smaller loops and thus less opposing lossy magnetic field, also such patterning helps to cancel out lossy magnetic fields because opposite polarity currents are self induced at the broken edges of ground plane, which helps in canceling out lossy magnetic field effects.

The technology offers two choices in groundplane selection, for the proposed inductor the patterned metal M1 groundplane that acts as a faraday shield is selected. There are other layout related rules specified in design manual regarding specifying the AC-ground and desired way to do ground plane connections during the simulation and layout. The preliminary choice of inductor was defined in this section, hence-forth the word/term inductor in thesis will replicate the inductor symindp, with optimal choice of metal layers and metal-patterned ground plane as provided by the technology.

4.4.3 The optimized inductor design methodology

After preliminary investigation and understanding of inductor and process related variables, the final choice of inductor was made, it was based on the analysis of data collected from iterative simulations. The simulations were performed based on the set of design rules as given in [50, 51, 59], these design principles are mentioned hereunder.

Choice of interline spacing: It should be kept to minimum value, as specified by the technology. This improves the mutual coupling between the metal lines, thus improving the inductance.
The strip width should be kept in between 10 and 15 micrometers. The increase in metal line width results in decrease in Q-factor and making it more susceptible to frequency.

The thickness of isolating oxide layer should be kept as thick as possible, in order to minimize shunt parasitic and dissipation.

Connection of metal layers in parallel, this reduces the Ohmic losses and increase the Q-factor.

Maintaining a space width of minimum of five linewidths, between the outside turn of spiral and any surrounding metal features.

Number of turns: The number turns in an inductor depend upon the operational frequency and desired inductance value and Quality factor. Some propose ‘n’ to be as high as possible [51] because it improves the inductance to series resistance ration. The inductance value ‘L’ is quadratic and directly proportional to number of turns that is $L \propto n^2$ and $R_s \propto n$, therefore the ratio improves by ‘n’. However this comes at the cost of increased parasitic capacitance in the form of interwinding capacitance, which reduces the self-resonance frequency and will effect the Q-factor, therefore the choice must be an optimized one.

These illustrated points served as basic design rules. The start was made first by following the rule number 1 that is keeping the space width to its minimum, which is 5 micrometers as available from the technology.

An iterative algorithm was followed with different set of inductance values in order to find the optimized value. The algorithm followed is as follows.

The line spacing was kept to its minimum value of 5 micrometers as provided by the technology.

Second Step was to find the optimized value of metal line width. Hence, the model determined inductance values of 500 pico Henry, 1nH, 1.2nH, 1.5nH, and 2nH were simulated with an ideal capacitor from analog.lib, for widths of 8, 10, 12, and 12.5 micrometers. The number of turns was kept similar for each inductance value by adjusting the outer diameter length for different widths. The value of capacitor in each simulation was chosen so that LC-tank should resonate nearest to the frequency of oscillation, that is 5.6GHz. The Q-factor of inductor (tank), since the capacitor chosen is ideal one, was calculated as $Q_{\text{3-dB}}$ or $Q_{\text{Bandwidth}}$, it was noted that barring from 500 pico Inductance with width of 8 and 10 micrometers, which has marginally higher Q-factor than same inductance at line width of 12 micrometers, the Q-factor for line width equal to 12 microemeters provided the highest value for each inductance value. The value of Q-factor dipped as line width was increased to 12.5 micrometers. Therefore, after computer simulations and iterations the line width was fixed to 12 micrometers.
The next step involved characterization of inductance value, that is finding the effective value of inductance. The technology model gives extrapolated or interpolated values of inductance based on the generalized inductor characterization as references to variable values. However, for particular variable values the technological model values of inductor are not often correct, therefore it was necessary to find the exact value of the inductance.

For this, the inductor with model predicted values of 500pH, 900pH, 1nH, 1.2nH, 1.5nH, 2nH, 2.5nH and 3nH were simulated as shown in the test-bench Figure 4.9. Again the tank was made to resonate at 5.6GHz with ideal capacitor, with capacitor value given by \( C = \frac{1}{2\pi f \sqrt{L}} \), \( f \) is oscillation frequency = 5.6GHz. But there were seen the aberrations in the oscillator frequency from the desired 5.6GHz, the value of resonating frequency for each model predicted inductance value was tabulated till nearest 4th decimal place and each inductance value has 5 such runs, of which the standard deviation was approximately zero. The deviation from the oscillation frequency can be seen from the Figure 4.10 below. If the tank if not oscillating at its desired frequency of 5.6GHz, when we use ideal capacitor of value calculated in accordance with the inductance value predicted by model, it results that the model specified inductor values are not correct. This
clearly validates that effective inductance is different from model predicted inductance value and we need to characterize inductor properly.

Figure 4.10: Showing the fault in the model predicted inductance value
Next step involved correction of inductance value for the same capacitance and obtained mean frequency and simulating the circuit for corrected inductance value and fixing the oscillation frequency to 5.6GHz to nearest 2 decimal places. Repeating the process for each inductance until the oscillation frequency was fixed to 5.6GHz. The table 4.3 below shows the effective value of inductance

<table>
<thead>
<tr>
<th>Number of Turns</th>
<th>Outer Diameter (um)</th>
<th>Inductance Model (nH)</th>
<th>Inductance Effective (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>130.8</td>
<td>0.5</td>
<td>0.45075</td>
</tr>
<tr>
<td>2</td>
<td>182.7</td>
<td>0.9</td>
<td>0.845226</td>
</tr>
<tr>
<td>2</td>
<td>194.8</td>
<td>1.0</td>
<td>0.9485</td>
</tr>
<tr>
<td>2</td>
<td>218.3</td>
<td>1.2</td>
<td>1.16183</td>
</tr>
<tr>
<td>2</td>
<td>252.18</td>
<td>1.5</td>
<td>1.50304</td>
</tr>
<tr>
<td>3</td>
<td>221</td>
<td>2.0</td>
<td>2.136086</td>
</tr>
<tr>
<td>3</td>
<td>250</td>
<td>2.5</td>
<td>2.85882067</td>
</tr>
<tr>
<td>3</td>
<td>278.2</td>
<td>3.0</td>
<td>3.7297</td>
</tr>
</tbody>
</table>

Table 4.3: Calculation of Effective Inductance.

As an extension to this in same step, another iteration was to choose the optimum number of turns, as it can be seen from the table 4.3 that the following iteration involves the rule to keep the inductor as hollow as possible by maximizing the Outer Dimension (diameter). This is to ensure that all the magnetic flux passes through the core and less parasitic capacitance. However, in order to verify the effect of maximum turn, the same iteration was done and the effective inductance were calculated for maximum number of turns possible for minimum OD as shown in table 4.4 below.

<table>
<thead>
<tr>
<th>Number of Turns</th>
<th>Outer Diameter (um)</th>
<th>Inductance Model (nH)</th>
<th>Inductance Effective (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>156</td>
<td>1.004</td>
<td>0.9593</td>
</tr>
<tr>
<td>3</td>
<td>169.7</td>
<td>1.201</td>
<td>1.201475</td>
</tr>
<tr>
<td>3</td>
<td>189</td>
<td>1.492</td>
<td>1.4965</td>
</tr>
<tr>
<td>4</td>
<td>195.4</td>
<td>2.0</td>
<td>2.1345</td>
</tr>
<tr>
<td>3</td>
<td>215.9</td>
<td>2.5</td>
<td>2.875</td>
</tr>
<tr>
<td>5</td>
<td>224</td>
<td>3.106</td>
<td>3.99983</td>
</tr>
</tbody>
</table>

Table 4.4: Calculation of Effective Inductance

4. The next step was to finalize between the two set of inductors, in order find the best suitable inductor with optimize number of turns. Therefore, the Q-factor that is 3-dB Q-factor was calculated for both set of inductors. The LC-tank was oscillated for nearest possible values to the desired oscillation frequency using the effective inductances and ideal capacitor. The following Figure 4.11 (a) and (b) shows the Q-factor comparison between the inductance obtained by maximizing the outer dimension while keeping the number of turns to minimum that is Q-factor (Hollow) in Figure 4.11(a) and inductor designed with maximizing the
number of turns Q-factor (Max. Turns) in Figure 4.11(b). This comparison leads to the first result that at desired frequency we should go for inductor with less number of turns, as Q-factor of hollow inductor is higher than the Q-factor value for the comparable inductance with more number of turns in design.

![Q-Factor Comparison](image1.png)

**Figure 4.11:** (a) Q-Factor for the set of Hollow Inductors.

![Q-factor (Max. Turns)](image2.png)

**Figure 4.11:** (b) Q-factor for the set of Inductors with Maximum Turns.
An Oscillator System for UWB QDAcR

5. After deciding on the number of turns, the main point was to decide upon the value of Inductance. As it can be figured out from the analysis of Q-factor for the set of hollow inductors (Figure 4.11a) that peak value of Q-factor at the desired frequency occurs at inductance value of around 1nH. However, this criterion of having highest Q-factor does not substantiate the proposition that we should go for 1nH inductor. Firstly, until now we have not calculated the net parasitic associated with each inductor as well as we have not looked for highest inductance to parasitic series resistance ratio or highest inductance to parasitic capacitance or required capacitance ratio as postulated earlier. Therefore going for highest value of Q-factor at 5.6GHz is amateurish and needs to be verified.

First step is to find the value of all the parasitic associated with the inductor model. In this regard, we simulate S-parameter analysis of the inductor set from 1Hz to 100GHz frequency, our main interest is to find the parasitic value. We know that at the self resonance frequency the reactance offered by inductor model is zero that is the value of Imaginary (Z11)=0, the frequency at which Im(Z11)=0 is called the self resonance or imaginary bandwidth frequency. In order to have the value of parasitic series resistance, we plot the value of Real(Z11) and see the value of resistance at DC that is at very low frequency. It is noticed, which is inline with the theory that series resistance is frequency dependent and it shoots up drastically at very high frequencies close to self-resonance frequency and remains very much constant at lower frequencies. We have spoiled the value of effective inductance from previous iterations, now we calculate the net parasitic capacitance and resistance from the present set of simulation, the tabulated data is shown in table 4.5 below. The series resistance for LC-tank at 5.6 GHz is calculated separately using the previous test bench as shown in Figure 4.9, where by adding the capacitor and then making the LC-tank to Oscillate at 5.6GHz.

<table>
<thead>
<tr>
<th>Effective Inductance (nH)</th>
<th>Imaginary Bandwidth Frequency (Hz)</th>
<th>Value of Net Parasitic Capacitance (Cp+Co) in Farads</th>
<th>Value of Net Simulated Capacitance required by LC-tank. (Farads)</th>
<th>Value of Series Resistance (Rs) @ DC in Ohms</th>
<th>Value of Series Resistance (Rs) in Ohms (When LC-tank Oscillating at 5.6GHz)</th>
<th>Peak Value of Re(Z11) at the oscillation frequency in Ohms.</th>
</tr>
</thead>
<tbody>
<tr>
<td>.45075</td>
<td>6.51E+10</td>
<td>13.2544E-15</td>
<td>1.79E-12</td>
<td>0.1981</td>
<td>0.8238</td>
<td>305.32</td>
</tr>
<tr>
<td>.845226</td>
<td>3.79E+10</td>
<td>20.8667E-15</td>
<td>9.56E-13</td>
<td>0.29264</td>
<td>1.22343</td>
<td>715.22</td>
</tr>
<tr>
<td>.9485</td>
<td>3.44E+10</td>
<td>22.5919E-15</td>
<td>8.51E-13</td>
<td>0.31458</td>
<td>1.36</td>
<td>806.134</td>
</tr>
<tr>
<td>1.16183</td>
<td>2.90E+10</td>
<td>25.8488E-15</td>
<td>6.95E-13</td>
<td>0.35707</td>
<td>1.72</td>
<td>953.21</td>
</tr>
<tr>
<td>1.50304</td>
<td>2.36E+10</td>
<td>30.2399E-15</td>
<td>5.37E-13</td>
<td>0.41841</td>
<td>2.52</td>
<td>1074.533</td>
</tr>
<tr>
<td>2.136086</td>
<td>1.74E+10</td>
<td>39.3199E-15</td>
<td>3.77E-13</td>
<td>0.50082</td>
<td>4.716</td>
<td>1150.22</td>
</tr>
<tr>
<td>2.85882067</td>
<td>1.43E+10</td>
<td>43.306E-15</td>
<td>2.80E-13</td>
<td>0.57939</td>
<td>8.4675</td>
<td>1134.68</td>
</tr>
<tr>
<td>3.7297</td>
<td>1.22E+10</td>
<td>45.893E-15</td>
<td>2.12E-13</td>
<td>0.65589</td>
<td>15.385</td>
<td>1092.79</td>
</tr>
</tbody>
</table>

Table 4.5: Simulated and Tabulated values for Parasitic at self-resonance and at Oscillation Frequency (with ideal capacitor).
The table 4.5 shows a variety of simulated data, firstly calculation of all the parasitic resistance and capacitance for Inductor, which are necessary in order to characterize it fully. With the help of this data we can verify the various postulates for optimized LC-tank, as mentioned in section 4.3. Firstly, plotting the ratio of inductance to parasitic capacitance and ratio of inductance to series resistance, which seen from Figure 4.12(a) and (b) below.

![Figure 4.12: (a) Ratio of Effective Inductance to Parasitic Capacitance.](image)

![Figure 4.12: (b) Ratio of Effective Inductance to Series Resistance](image)
If we analyze Figure 4.12 (a) and (b) in light of the prepositions developed in section 4.3, that in order to have higher phase noise less power consumption, the desired ratios should be maximized. As it can be seen that the desired ratios keep on increasing with increase in the value of inductor, while we noticed previously that Q-factor drops for higher inductances. These two are not in line with each other. Therefore, an upper limit over the value of ratio must be specified in-order to have the optimized inductance value. In [56] defines the upper limit of the inductance value by defining the upper limit on series resistance, which is termed as effective resistance. However, this theory also falls short because it can be applied only and only after complete characterization of tank capacitance, which is highly dependent upon the choice of varactors and other source of parasitic capacitance like active devices, loading stages, current source size etc. Therefore, there is a need to have a theory that allows to optimize the LC-tank and inductance as a whole, while targeting phase noise and power consumption also.

In this regard, if we go back to the Figure 4.8 and equation 4.17 and 18 then it can be discerned that for an optimize inductance or tank, it is necessary to consider the effect of substrate loss and self resonance also. Therefore maximization of ratio of inductance to series resistance will not suffice as it does not include the effect of parasitic resistance ‘R_p’; in order to include the simultaneous effect or parasitic resistance as well as series resistance, we should look to parameter ‘Z_{pk}’, which is defined as the peak Re(Z11). The peak value that is the real value of Z11 at the oscillation frequency, clearly and compositely takes into account the effect of all the Ohmic losses at resonance. Now, plotting the graph for inductance value versus peak Re(Z11) in Figure 4.13

![Figure 4.13: Peak Real (Z11) Vs. Inductance at Oscillation.](image-url)
An Oscillator System for UWB QDACR

If we analyze Figure 4.13 and Q-factor graph, some similarities are noticed easily. Firstly, the peak value starts dropping as inductance value increases because capacitive substrate losses start dominating, same can be confirmed, if we see the value of self-resonance frequency from table 4.5. The imaginary bandwidth frequency starts dropping, which means that it starts becoming more effective as inductance value goes high. In terms of physical behavior inside inductor it can be explained as capacitive component of substrate losses (that is gradient increase in the opposing magnetic field due to coupling of induced current with substrate) takes over the parasitic resistive component (effect due electric field penetration of the substrate that is eddy current generation).

Therefore, if we look back and analyze Figure 4.13 with regard to equations 4.12 and 4.15, it can be discerned that in our case in order to design an optimized LC-tank, which simultaneously meets low phase noise and low power consumption requirements, then $Z_{pk}$ should be maximized. Furthermore, it can be noticed that maxima for peak resistive impedance occurs for inductance value of 2.13 nH, therefore it is wise and desirable to choose an inductor with effective inductance in range of 2.1-2.3 nH. The proposition to go for peak value, in reality gives the value of optimized Q-factor of a tank as it captures all the lossy effects and provides an effective solution to meet the limitations, as expressed in table 4.2. This approach is further validated by running the simulation for a differential pair oscillator with LC-tank comprising of an ideal capacitor and firstly with an inductor of 2.13 nH and in second run with an inductor of 1nH. It was found that for the same power consumption the phase noise obtained from optimized inductor was approximately 5dB better than the one obtained from 1nH inductor. This in short concludes the characterization and designing of inductor and in order to have optimize LC-tank at 5.6 GHz the symindp with an effective inductance of 2.134 nH will be used. Figure 4.14 below shows the basic layout of the used inductor, the peripheral dimensions are 254.08umx254.08um.
4.4.4 Varactor Design Methodology

In LC-tank design, we mainly emphasized on design of the inductor, with an assumption that the capacitance required is having very high ‘Q-factor’. However, in reality capacitors have finite ‘Q-factor’, which means that they do affect LC-tank performance and in turn performance of an oscillator. Therefore, it becomes imperative to define LC-tank capacitance and its characterization. First, we should define the term capacitance with in the LC-tank, the term ‘C’ in angular frequency formula stands for the total capacitance which is seen by the tank. This includes capacitance from varactors, parasitics from active as well as passives and loading capacitance. Therefore, we can define tank capacitance as given by equation 4.19 below.
An Oscillator System for UWB QDaCR

\[ C_{\text{Tank}} = C_{\text{Varactor}} + C_{\text{Parasitic (Active+Passive)}} + C_{\text{Load (Buffer, Miscellaneous)}} \] (4.19)

therefore, a more refined expression in order to describe angular frequency of an oscillator can be written as

\[ \omega_0 = \frac{1}{\sqrt{L_{\text{eff}} C_{\text{Total}}}} \].

If we consider the system to be oscillating at frequency of 5.6GHz, with effective inductance of 2.1nH, then the value of \( C_{\text{Total}} \) should be equal to 385fF. Therefore, while designing the oscillator we should be careful that the total capacitance seen by the LC-tank should not increase more than 385fF. If we analyze equation 4.19 it can be seen that varactor capacitance offers designers degree of freedom to counter against Process and temperature variations and to re-calibrate the tank to defined oscillation frequency in case of any mismatch. Another important property of varactor capacitance is to provide tuning range to an oscillator, that is an oscillator can often be used to generate oscillations at different frequencies depending upon the application requirement and this be done by changing the capacitance across the tank for e.g. by switching the capacitive bank. As stated earlier that in our system design we do not have any such tuning range requirement, also relaxation of roughly \( \pm 120 \text{ MHz} \) eases the frequency stabilization problem and fends off the use of Phase lock loop or PLL in circuit design. However, oscillator circuit does need a desired tunability of 10% in order to cope with PVT variations.

The tuning range of a varactor is defined as the ratio between the maximum and minimum capacitance, when MOSFET is swept over certain voltage range. Mathematically it is given by equation 4.20

\[ \alpha = \frac{C_{V, \text{Max}}}{C_{V, \text{Min}}} = \left( \frac{f_{\text{Max}}}{f_{\text{Min}}} \right)^2 + 2 \left[ \left( \frac{f_{\text{Max}}}{f_{\text{Min}}} \right)^2 - 1 \right] \frac{C_{\text{Parasitic}}}{C_{V, \text{Max}}} = \frac{C_{\text{Variable, Max}} + C_{V, \text{Paras}}}{C_{\text{Variable, Min}} + C_{V, \text{Paras}}} \] (4.20)

Where \( C_{\text{Variable}} \) is the series capacitance of the gate oxide capacitance \( C_{ox} \) and depletion region capacitance \( C_d \) and the varactor’s parasitic capacitances are given by overlap and fringing capacitances between the gate and source-drain regions [60]. The MOSFET application as a variable capacitor or Varactor (Change in capacitance due to change in voltage across the capacitor) is a well-known method. When the Drain-Source and Bulk (depending on the bias voltages and process technology) terminals are tied together then MOSFET works as a capacitor, whose capacitance can be modulated by controlling the Bulk to Gate voltage \( V_{BG} \), as shown in Figure 4.15 below. As seen in the Figure 4.15 below, five distinctive regions are marked namely 1 to 5, therefore in accordance with the design requirements, we can choose mode of varactor operation.

The varactor modeled is a P-Channel device and it works in moderate inversion or region 2 if bulk to gate voltage is greater than the threshold voltage \( V_{bg} > |V_{th}| \). In region 2, the capacitance is series sum of gate oxide capacitance \( C_{ox} \) and capacitance \( C_d \) due to space charge width \( (x_n) \) [61], since in this region we see moderate inversion that is the concentration of holes in channel (minority carriers in PMOS) is not yet peaked. Which means that the minority charge carrier concentration beneath the channel is same as in the

-132-
bulk, and it improves on increasing $V_{BG}$, which means that on increasing $V_{BG}$ the dominance of space charge density starts diminishing and effect of holes channel charge density starts increasing. If $V_{BG}$ is increased further, it ensures device operation in region 1 that is in strong inversion region, in this region a complete channel of holes is created beneath the gate and total capacitance seen is dominated by channel charge density capacitance that is gate oxide capacitance $C_{ox}$, also space charge width is at its minimum, which means $C_d = 0$. However, lowering of $V_{BG}$ or increase in the gate voltage drives the device towards region 3, which is a weak inversion region, in this region space charge width reaches its maxima and the effect of gate-oxide capacitance is at its minima. The space charge density is peaked and in this region we do not see any big change in capacitance over change in voltage or this region offers least tunable range. However, due to best varactor sensitivity, which is offered in this region, translates into an Oscillator with better phase noise performance, but negligible tunability, which undermines the very definition of VCO and pragmatic feasibility of such oscillator.

A-MOS varactor can be defined when varactor operates in regions 4 and 5. That is further decrease in $V_{BG}$ OR increasing the positive gate voltage, the electrons majority carriers in case of P-Channel device, start filling the channel and a depletion layer of electrons is formed beneath the gate and device starts working in region 4 of depletion. On increasing the gate voltage in region 4, the channel charge density capacitance $C_{ox}$ becomes prominent. But this time channel now comprises of higher concentration of majority charge carriers (electrons for PMOS) and the varactor capacitance is controlled totally by positive gate voltage or $V_g > V_b$. If we further increase the gate voltage it drives the device into accumulation, which means that a complete channel of majority charge carriers appears underneath the gate. However, the gate-oxide capacitance $C_{ox}$ in case of accumulation is lower than gate-oxide capacitance when device is working in strong inversion mode. This happens because of change in effective channel length beneath the gate, which reduces the maximum value capacitance $C_{ox}$ in two cases. The reasoning followed is that when device is working in inversion mode the gate and drain nodes have same charge polarity that is minority charge carriers as in the channel therefore the effective length of channel under the gate is higher than it is in case of accumulation mode when channel consists of majority carriers only OR $C_{V,Max-Inversion} > C_{V,Max-Accumulation}$. Furthermore, it can be noticed that because of the change in effective length under the gate, varactor working in inversion mode or (I-MOS Varactor) has high sensitivity when compared with Accumulation mode varactor (A-MOS). Here sensitivity relates to gradient of change in capacitance with respect to voltage. The better sensitivity offered by accumulation mode varactor results in marginal better phase noise performance than an inversion mode varactor oscillator. The proper quantitative reasoning is presented in the next section.
Figure 4.15: Variation of Capacitance for change in Bulk-Gate Voltage

In our above analysis of varactor we did not, much considered the effect of parasitic. If we carefully analyze Figure 4.15, it can be noticed that the minimum capacitance occurs in region 3 that is weak inversion mode and as discussed space charge depletion capacitance \( C_d \) dominates. In weak inversion the gate control of channel conductance is controlled by the parasitic gate-channel capacitance in this case is given by gate-source capacitance \( C_{gs} \) and gate-drain capacitance \( C_{gd} \), where \( C_{gs} \) and \( C_{gd} \) are formed by overlapping of source and drain regions with gate. Mathematically the value is given by expression as follows \( C_{gs} = C_{gd} = \frac{W.L.C_{ox}}{2} \), therefore \( C_{V, Min} = C_{gs} + C_{gd} + C_d \), similarly in strong inversion mode or accumulation mode \( C_{V, Max} = C_{acc} + C_{gs} + C_{gd} \). As stated in [62] that the effect of \( C_{gd} \) is minimal when the device is in deep saturation, since MOSFET works as a capacitor that is \( V_{DS} = 0 \), therefore when operating in accumulation mode the effect of parasitic capacitance \( C_{gd} \) is minimized.
The next in parasitic analysis is comparison channel resistances for I-MOS and A-MOS varactors. The comparison between A-MOS, I-MOS and Diode in Figure 10 of [63], clearly shows that A-MOS offers shows least parasitic resistance, while diode varactor shows the most resistance. The parasitic resistance offered by I-MOS is given in [64] can be expressed as:

$$R_{\text{para}} = \frac{1}{12N} \left( R_{\text{Channel},i} \cdot \frac{I}{W} + R_{\text{Poly},i} \cdot \frac{W}{l} \right).$$

This gives insight into parasitic resistance, in order to have minimum parasitic firstly the number of gate fingers ‘N’ should be large, second the process available node length should be kept to its minimum value. This analysis also substantiate the fact that channel length should be kept at minimum to reduce the parasitic resistance and increase the ‘Q-factor’.

The analysis presented so far depends upon the small-signal behavior of device. However the signal at the gate of varactor is a large signal sinusoid, which changes from +Vpk to –Vpk for a complete cycle, this changes the value as well as mode of operation of Varactor. Therefore, it becomes mandatory to investigate the large-signal behaviour and make sure the mode of operation of varactor. A detailed quantitative analysis explaining the large signal behaviour is presented in [65], which is summed up and presented as follows.

1. The total capacitance seen by tank is given by term effective capacitance $C(v(t))$ or $C_{\text{eff}} = C_{\text{avg}} \left( \frac{1}{2} \right) C_{\text{harmonic}}$, where $C_{\text{avg}}$ is dominant and the total capacitance at fundamental for a complete oscillation cycle and can be approximated as:

$$C_{\text{avg}} \approx C_{\text{eff}} = \frac{C_{\text{Max}} + C_{\text{Max}} - C_{\text{Max}}}{2} + \frac{C_{\text{Max}} - C_{\text{Max}}}{\pi} \left( \sin^{-1} \left( \frac{V_{\text{eff}}}{V_{\text{lo}}} \right) + \frac{V_{\text{eff}}}{V_{\text{lo}}} \sqrt{1 - \left( \frac{V_{\text{eff}}}{V_{\text{lo}}} \right)^2} \right)$$

In equation 4.21, $V_{\text{eff}} = V_{\text{Gate}} - V_{\text{Tune}} - V_{\text{Threshold}}$

2. The Low frequency AM noise is upconverted and translated into Phase noise due to varactor non-linearity and varactor noise conversion sensitivity can be defined as:

$$K_{\text{AM}} = -\frac{\omega_{\text{lo}}}{2C_{\text{eff}}} \frac{\partial C_{\text{eff}}}{\partial V_{\text{lo}}}$$

This clearly shows that phase noise can be better if the sensitivity can be lowered. A little tweaking to above expression leads us to:

$$K_{\text{AM}} = -\frac{\omega_{\text{lo}}}{2C_{\text{eff}}} \frac{\partial C_{\text{eff}}}{\partial V_{\text{lo}}} = -\frac{\omega_{\text{lo}}}{2C_{\text{eff}}} \frac{\partial C_{\text{eff}}}{\partial V_{\text{lo}}} \frac{\partial V_{\text{lo}}}{\partial V_{\text{lo}}} \frac{\partial V_{\text{Tune}}}{\partial V_{\text{lo}}}$$

the equation 4.22 clearly indicates the dependency of phase noise over the tuning range sensitivity and also predicts upon the need of stabilize amplitude over the tuning range. Also highest phase noise can be obtained when either $V_{\text{eff}} = V_{\text{lo}}$ or $V_{\text{eff}} = 0$. In both cases it means that biasing the varactor either to value of
Further it can be deduced from equation 4.22 that larger the tuning range less is the phase noise. As a solution a digitally controlled capacitor switch bank can be employed.

Using the postulates of large signal analysis in order to find the Varactor providing the effective capacitance as required, which in turn will automatically provide the lowest AM to FM noise conversion sensitivity. Therefore simulating for $C_{eff} \equiv C_{var}$, by using the iterative process in which different set of values for DC biasing variables that includes $V_{gate}$ and $V_{var}$ were used.

![Figure 4.16: Effective Capacitance Vs. Tuning Voltage Sweep](image)

It can be seen from Figure 4.16 above, that using large signal analysis the size of varactor, which shows constant value of average capacitance over complete tuning range voltage for different values effective voltage, the graph is derived from parametric sweep of tuning voltage for each seep of effective voltage. Also, it can be noticed from Figure 4.16 that value of average capacitance is 373fF, which is very close to the theoretical value derived for 2.13nH inductor to resonate at 5.6GHz.

Next step in our analysis involves to do the small signal analysis of varactor. Before going forward, firstly we need to decide on the mode of operation, as far we have seen through parasitic analysis and sensitivity analysis that A-MOS offers best solution in comparison to I-MOS and it can be verified from detailed
results published in [60, 63, 66]. If we see carefully, it is found that the tuning voltage and gate large signal voltage play crucial role in defining tuning range and capacitance value for a varactor. In case of PMOS varactor, in order to make MOSFET work as A-MOS \( V_G > V_t \) and \( V_{BG} << V_{th} \), the value of gate voltage depends upon the root means square value of oscillation cycle amplitude that is \( V_o \), the peak value of \( V_o \) in ideal case can be 1.2volts. Firstly, the value of threshold is technology define and in order to have higher Q-factor and low resistance, we should keep the gate length to its minimum value, as we can change lower the threshold by increasing the gate length. Now considering the case when D-S-B nodes are tied together and typical threshold value \( V_{th} \) of 450-550mV, which implies that device can work in accumulation mode if and only tuning voltage is less than 650mV. This means the reduction in tuning range and increase in sensitivity. Therefore, to ensure accumulation working the novel solutions have been proposed in [50, 60, 63, 64, 66], these mainly includes doping the source and drain of PMOS with n+ impurity or tailor made varactors as technology do not provide such devices. Also, in comparison analysis through literature it was noticed that A-MOS does not provide much significant betterment in phase noise value and specifications for phase noise are bit relaxed therefore, it was logical to go for Inversion mode or I-MOS varactors. Next step was to look for tuning range, because as described in [50, 67] the tuning range can be increased by use of differential varactors that is PMOS and NMOS varactors in inversion mode. However on the count of tuning range also our specification are bit relaxed and the tuning range required is to meet the PVT variations. After carefully looking at all aspects, finally it was decided to use I-MOS varactors.

In I-MOS varactor the bulk node was connected to highest positive supply that is 1.2Volts, in order to ensure operation in inversion region. The typical I-MOS capacitor change is shown below in Figure 4.17. The Figure 4.17 also shows the effect of gate bias voltage, as discussed and proved earlier the graph shows the anticipated change for gate bias voltage. As it increases the tuning range that is the ratio of maximum to minimum varactor capacitance decreases.
Figure 4.17: Varactor Capacitance Vs. Tuning Voltage for different gate bias voltages

The Figure 4.18 and 4.19 below show the tuning range and resistance of the desired MOSFET varactor, when gate bias voltage is kept at 500mV. In Figure 4.18 the maximum capacitance achieved is around 430fF when tuning voltage is 1.2V and minimum capacitance is 239fF at tuning voltage of 0V. therefore the maximal tuning range that can be possibly attained by this varactor is given by equation 4.23 below:

\[
\alpha = \frac{C_{V,\text{Max}}}{C_{V,\text{Min}}} = \frac{430}{239} = 1.79 \approx 18\%
\]  

(4.23)

this is the maximal attainable tuning range, however in an oscillator this capacitance needs to be trimmed and tweaked in order to maintain as high tuning range as possible. The capacitance from active circuit and loading circuit will degrade the tuning range as the tunable capacitance provided by varactor needs to be decreased in order to compensate for other parasitic. In Figure 4.19 the net parasitic resistance is modeled, it can be witnessed that the resistance increases when the varactor is in moderate inversion or triode region. In moderate inversion the holes concentration at the gate start increasing, in beginning space charge region controls the active area (area beneath the gate and P+ region) and in reverse bias condition the hole-electron pair generated in space charge region combined to keep the thermal equilibrium. However, as change in bias makes holes migrating towards the gate, the diffusion currents [61] come into play and so does the
effect of diffusion resistance. As the device migrates towards the inversion region the diffusion resistance peaks and when the channel is made or device enters in strong inversion the effect of diffusion process recedes and so does the value of diffusion current and parasitic resistance. Another dominant parasitic effect is because of well resistance ‘$R_{\text{well}}$’ as described in [60] and is determined by the active area. Therefore from figure 4.19 we can say that rise in the value of dominant series parasitic resistance in moderate inversion region is a cumulative effect of Diffusion, well and Poly resistances, which then reduces mainly to the effect of Channel and well resistances in strong inversion mode.

Figure 4.18: Tuning Range offered by the characterized varactor.
In this section analyses and characterization of the desired varactor was presented. The emphasis was to keep the varactor design simple and as per the requirements, which fortunately are relaxed. Therefore, the design of differential varactors was not implemented at final design level. The varactor was optimized using large signal analysis for its property to convert low frequency AM noise generated in tail current or power supply to FM noise near the fundamental and second harmonic.

The varactor biased at tuning voltage of 619mV, when used in tank with characterized inductor; the tank oscillates at 5.6GHz frequency. This can be seen from the Figure 4.20 below, it can be noticed that the zero crossing for the reactance graph occurs nearly at 5.6GHz. The Q-factor of varactor was calculated to be 95.4, which determines over-all tank Q-factor of 14.7. This concludes the study of LC-tanks fundamentals and design of LC-tank for the proposed oscillator. The LC-tank was designed keeping in mind phase noise and low power consumption. In next section the design methodology for oscillator is explained in brief.

Figure 4.19: The change in parasitic resistance over the tuning range.
4.5 Oscillator Design Methodology

In this section the circuit design aspects for an oscillator are discussed and implemented. As mentioned at the time of Phase Noise modeling at system level, the understanding of phase noise due to oscillator circuit is dealt in succinct manner in starting. This then followed by a short discussion about the oscillator start-up condition and highlighting the design points that can improve the results. It is succeeded by step-by-step design methodology, starting with cross-coupled and complementary oscillator topologies description, the parameters that affect the oscillation start-up, the choice of active device and rules followed. The last section compares the results of different oscillators and complements results with the reasoning for choice of Complementary Differential Cross Coupled Oscillator, which is then verified by treatment of design for its robustness and resilience towards other process and temperature related variations.
4.5.1 Phase Noise in an Oscillator System

The phase noise at system level was modeled and discussed in detail in Chapter 2 and 3. However, our discussion fell short of effect of real device and circuit parameters. In this section, the phase noise analysis is revisited but pertaining to differential cross-coupled topology only. Our previous analysis of phase noise was based on Demir’s model which consider phase noise as a stationary random process which is non-linear and time variant system, and the system can be diluted to a linear time variant system for the condition of stationary process as presented in [22]. The time invariant model of phase noise based on circuit analysis has been researched and developed very well, to name a few classic papers, the model is presented in [28, 54, 68, 69]. As proved in [69] that for a memory-less non-linear system the ratio of carrier to phase modulated noise sidebands is equal at the input and output of a system. This helps in transforming and analyzing various noise sources in an oscillator and allow us to use basic circuit analysis laws.

The first step is about defining the noise sources present in cross-coupled oscillator. If we look at Figure 4.5, we see three possible and distinctive source of noise, which are LC-Tank or Resonator, The active gain part or transistors and lastly biasing / power sources which includes tail current source and other low frequency bias/power sources for e.g. Vdd.

Resonator Noise: We have characterized the LC-tank in previous sections and know that loss can be depicted in terms of a parasitic resistance ‘Rp’ as shown in Figure 4.6. The value of output voltage ‘Vo’ over an oscillation cycle, across the parallel RLC tank is given by the well known expression $V_o = \frac{2}{\pi}I_oR_p$, where ‘Io’ is tail current. The phase noise component of the tank is given by equation 4.15 which can be re-written as

$$L(\Delta \omega) = 10 \log \left[ \frac{4kTR_p}{V_o^2} \left( \frac{\omega_o}{2Q\Delta \omega} \right)^2 \right].$$

Phase noise contribution by active part of an oscillator: The simplistic view of the switching diff-pair can be a tail current source with a cascoded transistor and the output noise is a current noise pulse as described in [54, 68]. The switching effect of diff pair at oscillation frequency $\omega_o$, mixes and folds all the components of noise from all the sources around the fundamental and even harmonics. The total contribution by diff-pair is given by

$$L(\Delta \omega) = 10 \log \left[ \frac{8kTR\gamma I_o R_p^2}{\pi V_o^3} \left( \frac{\omega_o}{2Q\Delta \omega} \right)^2 \right],$$

where $\gamma$ is noise factor for non-linear circuit and for MOSFET typically $\gamma = \frac{2}{3}$. It can be seen from the expression for diff-pair phase noise contribution that phase noise contribution is independent of device sizes [54, 68].

-142-
As we understood from our non-linearity analysis of varactor and from \([65, 69, 70]\) that upconverted AM noise is transformed into phase noise. The low frequency tail current noise is upconverted to with sidebands around the fundamental. However, this AM noise is modulated by the varactor, with components at low frequency and at \(2\omega_n\). Therefore, the noise current at frequency \(2\omega_n\) is commutated in the loop and shows noise sidebands at fundamental and third harmonic. The total phase noise contribution by tail current source is given by \(L\{\Delta \omega\} = 10.\log \left[ \frac{kT \gamma \pi^2}{2I V_{eff}} \left( \frac{\omega_n}{2Q\Delta \omega} \right)^2 \right]\) as in \([68, 70]\).

Therefore if we sum up phase noise contribution by all the noise sources, the final phase noise equation we arrive at is given by equation 4.24 below

\[
L\{\Delta \omega\} = 10.\log \left[ \frac{4kTR_p}{V_o^2} \left( 1 + \frac{2\gamma I R_p}{\pi V_o} + \frac{\gamma I R_p}{2V_{eff}} \right) \left( \frac{\omega_n}{2Q\Delta \omega} \right)^2 \right] \quad (4.24)
\]

Now in order to design low phase noise oscillator we can target optimization of phase noise at each noise source level. This done by applying set design rules as expressed here under.

### 4.5.2 The Oscillator Start-up condition

It is extremely necessary to select the proper set of devices in order to make sure that oscillator starts properly. It becomes imperative to find the oscillation condition, according to the theory of negative resistance the active part should compensate for the losses in the tank. Losses in the tank are defined by the term ‘\(R_p\)’ therefore active part should provide Transconductance (Gm) which is equal or more than tank losses or \(G_{tank} \leq G_m\). Mathematically \(\frac{1}{G_m} = R_{\text{inv}} \leq R_p\), however to safeguard the start the \(k' R_{\text{inv}} \leq R_p\), where \(k = 2-3\), which means the value of active resistance should be as low as possible.

If we look at the Figure 4.21 below, the tank voltage \(V_o\) connects to its driving transistor M1 through cross coupled transistor M2. The capacitor \(C_v\) denotes the capacitance of the current source. The path sees transistor M2 as a source follower, therefore the input impedance is given by

\[
Z_m = \frac{1}{j\omega C_{p1}} + \frac{1}{j\omega C_v} - \frac{g_m2}{\omega^2 C_{p1} C_v} \quad (4.25)
\]

The total active impedance seen by tank is given by equation 4.26 as

\[
Z_{tot} = \frac{-1}{g_m1} + \frac{1}{j\omega C_{p1}} + \frac{1}{j\omega C_v} - \frac{g_m2}{\omega^2 C_{p1} C_v} \quad (4.26)
\]

The condition for start-up is given as \(R_p \geq k' \left| 2Z_{tot} \right|\), the factor ‘2’ because of diff-pair topology.
Therefore, analyzing the factors, which influence the start-up condition, the effect of parasitic capacitance $C_{ss}$, as discussed previously it reduces the tuning range, this calls for device with minimum channel length in order to reduce the overlapping capacitance.

The maximization of Transconductance, this can be done by increasing the width of the device as higher value of $g_m$ ensures stable start-up. The $g_m$ of a transistor depends more on the transistor geometry than the bias current as it is directly proportional to the width, while in square-root to the bias/tail current. Another factor is capacitance of the tail current source, which adversely effect the start-up condition, as it loads the tank as parasitic capacitance hence decrease the tuning range as well lowers the LC-tank Q-factor.

The current source design is discussed in detail in next section.

### 4.5.3 Methodology for Oscillator Design

In order to meet the criteria of low power consumption and low phase noise, certain design rules needs to be followed, which are described hereunder:

Firstly, considering the resonator noise source, we have already tried to optimize the resonator associated phase noise component during LC-tank design. However, there is always some room for certain trade-off, that is to better the phase noise at the expense of tuning range. As reducing the varactor average value
results in reduced tuning range and less non-linearity, which directly results in reduced phase noise contribution from LC-tank and the tail current source.

The focus shifts to the optimization of phase noise component due to diff-pair. On careful screening and simplification it can be discerned that active device phase noise contribution can be better by increasing the tail current. However, in low power or power-limited regime this is not the case, therefore a careful attention needs to be given to the choice of device sizes. There are two contradictory theories one by [68], which mathematically proves that phase noise is independent of device size. On the other hand in [71, 72] propose that phase noise in $\frac{1}{f^2}$ and $\frac{1}{f^3}$ is dependent upon the device parameters, specifically on the overdrive voltage ($V_{os} - V_{th}$) and transistor cut-off frequency $f_c$, and as the device width is reduced so does the improvement in the phase noise. The reasoning presented in [71] gives useful insight in preliminary device selection, however the optimum limit on overdrive voltage derives from the oscillator start-up condition which is dependent upon higher value of ‘$g_m$’. The value of ‘$g_m$’ decreases steadily on increase in overdrive voltage under constant current scheme and in our case, lower power is a big constraint.

The choice of devices for the diff-pair was made first by setting the DC bias-points and maximizing the overdrive voltage for the sufficient value of ‘$g_m$’. The DC bias points were checked at -50, 30, and 140 degree Celsius. This was done to ensure that the over-drive value of minimum 80-100mV does exist and under no condition any transistor should be switched off. The gate length was kept at minimum, because the parasitic capacitance effects the tuning range and since our design does not employ any switchable capacitor bank, we have to make sure the practicality of the tuning range. Another reason as discussed is adverse effect of parasitic in providing stable oscillation start-up. Second constraint was power consumption, to keep it as low as possible, while achieving derivable, this also put constraint on maximization of over-drive voltage, as a trade-off between ‘$g_m$’ and over-drive voltage needs to be strike.

In case of complementary diff-pair topology the Transconductances of NMOS and PMOS were kept as close as possible so that cycle can have equal fall and rise time that is symmetry over the horizontal axis. Next is to make sure that diff-pair always work in saturation mode, any increase in the oscillator output voltage, will result in increase of gate voltage for the diff-pair MOSFETs and can make transistor to go in triode region. Such instance will initiate non-linearity in the current and thus affecting the phase noise. The saturation mode can be assured if the gate-source feedback if decoupled and gate of diff-pair transistors can be biased separately. But this will definitely de-Q the tank and influence the tuning range as well degrade the phase noise based upon the value of biasing circuit impedance. However, as described in [49] decoupled and switched biasing can improve the phase noise performance in $\frac{1}{f^3}$ region. In our case, this situation is dealt by selecting the minimum length device for highest threshold, so that even increase in
over drive can be compensated for. Second The cascoded tail current stabilize the source voltage and source degeneration reduces the tank voltage swing thus effectively checking the gate bias.

Design of Current source: A cascoded current mirror source is employed in the design. The current mirror serves as tail current biasing source and does modulates the value of \( g_m \) in order to guarantee sufficient loop gain for sustainable oscillations. However, tail current degrades the phase noise by introducing flicker noise into the oscillator. As discussed in [54, 68, 70, 73] in detail the mechanism, effect and filtering of low frequency tail current noise, which is seen at frequencies around the fundamental in carrier power spectrum and flicker noise commutates in loop with the frequency of \( 2\omega_c \). Several solutions have been proposed in literature, with most of them converging on the deployment of LC filter with resonance frequency of \( 2\omega_c \), as source degeneration in an oscillator. In our design we have approached the problem in two ways.

Firstly, design of basic current mirror, The large transistors, in width and gate length larger than the process node. The main reasoning behind this was that larger transistors offer less \( 1/f \) contribution, because short channel MOSFET exhibits higher flicker noise in comparison bipolar or large channel MOSFET. The flicker noise current spectral density is inversely proportional to width and channel length, therefore increasing \( W/L \) products improves the phase noise. Second benefit from large channel current mirror is that the threshold voltage is reduced, which enables to have higher overdrive voltage and higher \( g_m \). However, the draw back of big devices is capacitive loading of Oscillator, as we saw from our analysis that it can affect oscillator stability. Another effect is that due to capacitive loading the tuning range is reduced and also due to capacitive loading the amplitude modulation or amplitude instability sets in due to difference in high frequency oscillator time constants and low frequency bias circuitry time constants.

Secondly, as stated in [50, 74] a smaller transistor as cascode was implemented. Firstly, it reduces the effect of capacitive loading and secondly that it provides high output impedance for the current source, which is a desirable effect. It further, improves the performance of the Oscillator in two ways. If we look from the oscillator node the tail current cascode transistor works as source degeneration impedance for the common node of diff-pair. The smaller cascode transistor works in triode mode, which replicates a resistive degeneration at the common node for the Diff-pair and increasing the CMRR; however trade off should be attained so as the triode-resistive effect should not load or change the parallel resistance of tank. Therefore, a small sized and optimized cascode current source not only reduces flicker noise and capacitive coupling (as smaller capacitor in series with big current source) but also suppress the common mode variations. As an extension to this, the further improvement in the phase noise can be achieved if resistors are put at the source of diff-pair. However, a trade-off based in simulations is required, because this will decrease the output voltage swing across the tank. As presented in detail in [71] the PMOS offers less noise contribution than NMOS for both thermal noise and flicker noise regions, when transconductance of both PMOS and
4.6 Oscillator Design and Comparison

We have discussed the basic design methodology for an oscillator so far. Now we compare the performance of three basic oscillators, namely NMOS, PMOS and Complementary (Push-Pull) Oscillator; which were designed on the basis of methodology discussed.

Firstly, a discussion about complementary oscillator topology. As it is seen from Figure 4.20c, that a push-pull topology consists of two PMOS and NMOS cross-coupled diff-pair, which inherently bears the functionality of a typical CMOS Inverter and called as push-pull topology. If we look at the start-up condition then for a push-pull topology, then negative resistance is given by

\[ R_{\text{active}} = \frac{-2}{g_{mp} + g_{mn}} \]

and as we know that

\[ k' |R_{\text{active}}| \leq R_p \] if we compare the starting condition under ideal case that is parasitic to be zero, for a simple PMOS / NMOS and Push-pull than the tank transconductance

\[ G_{M_{\text{Push-Pull}}} \approx 2G_{M_{\text{PMOS}}}/G_{\text{NMOS}} \], considering that \( g_{mp} = g_{mn} \). This results easily into increase of the output voltage amplitude and in case of Push-Pull the output

\[ V_{o(Push-Pull)} = \frac{4}{\pi} I_o R_p = 2V_{o(\text{PMOS}/\text{NMOS})} \] . These deliberations are under ideal case scenario and considering that LC-tank remains the same. This means that for same current consumption large transconductance as well as large voltage swing is achieved by Push-Pull topology. This directly results in better phase noise performance (by equation 4.15) and more stable oscillation condition for Push-Pull in comparison to simple cross couple diff-pair topology.

However, if we consider the effect of parasitic added by extra diff-pair stage then it is clearly visible that the swing is not exactly two times. It will suffer a loss of 3dB due to the parasitic \( C_{gs} \) added by extra diff-pair and also degrade the tuning range. Secondly, the addition of extra active devices will add the noise to the oscillator. Therefore, in order to reap the benefits from push-pull stage a few trade-off should be made. Firstly, the size of added diff-pair and \( g_{om} \) obtained, should be optimized; because parasitic increase with increase in width and this can be done by iterative computer simulations and measuring the tuning range change ratio. Secondly, making \( g_{mp} \approx g_{mn} \), this provides better symmetry that same rise and fall time for the oscillator cycle across the horizontal axis. In [74] the detailed large signal analysis of push-pull topology is provided, however the theoretical claim of 6dB improvement is not noticed in simulations. A modified equation of phase noise for a push-pull topology is as given below and in [50]
An Oscillator System for UWB QDAcR

\[ L\{\Delta \omega\} = 10 \log \left[ \frac{4kTR_c}{V_c^2 + \frac{1}{2}} \left( \frac{\omega}{2Q \Delta \omega} \right)^2 \right] \]  

(4.27)

The Figure 4.22 shows the block diagram of implemented circuit for (a) PMOS, (b) NMOS and (c) Push-pull. The circuits were implemented based on the discussed design methodology and trade-off for lower power consumption. In order to find the correct choice for oscillator topology it was critical to test these three configurations for there figure of merit and meeting the specifications. The three oscillators were primarily compared using same LC-tank for amplitude swing, phase noise and tuning range provided for the same power consumption, the oscillation frequency deviation was kept to a minimum of 50MHz using the tuning voltage. The power specs chosen were to consume between 1-1.5mW at 1.2V supply.

Degeneration Resistance: The use resistance ‘Oprrpres’ from the process library. This resistor was chosen based on the study of design manual. The resistor with lowest parasitic capacitance and lowest mismatch is provided by L1 BEOL, however the use of this resistance comes with a rider. Firstly, after layout the parasitic of L1BEOL is not extracted by software tools and second rule is that there should not be any device or wiring placed under or above the L1BEOL resistors, also many foundries does not include either L1BEOL or KxBEOL in their library. These rules prompted for the use of other resistor.

The next option after careful simulation was ‘OPRRPRES’ it is a P type, lightly doped OP (Mask Level) poly silicon resistor. The OPRRPRES provides the highest sheet resistance with lowest parasitic capacitances and best absolute resistance sensitivity. On the hind side, this resistor suffers from higher mismatch and tolerances. However, for tolerance and mismatches the effect can be taken care at the time of simulation. The simulation with \( \pm 25\% \) were done, and also since the value of source degeneration resistance is 100 Ohms. Therefore the effect of higher mismatches and tolerance does not make much effect on the result. It was calculated that a resistance of 100 ohms, will have a change of 23.46 Ohms over a temperature gradient of 200 degree Celsius. Therefore over complete process and temperature variance the resistor can have values between 57 and 120 Ohms. The results at 50 Ohms and 120 Ohms are taken and tabulated. The polysilicon resistor has voltage limit 5V, which is under control as highest voltage swing attainable is 2.4V; and Current Limit in our case varies from a minimum of 5mA to 90mA. This is not an issue in our case as the current in oscillator is between 800micro Amp to 2mA, consumption in buffer is also less than 6 mA range in buffers.
Figure 4.22: (a) Diagram of a PMOS Differential Oscillator, (b) NMOS Differential Oscillator
Figure 4.22:(c) The Block Diagram of Push-Pull Differential Oscillator Schematic

4.6.1 Comparison of Different Oscillator Designs

In our comparison we start with the comparison of the tuning range for same varactor, which was designed in previously in this chapter followed by phase noise and swing comparison for power consumption of 1mW. Figure 4.23, 4.24 and 4.25 shows subsequently the tuning range that is frequency variation over the
An Oscillator System for UWB QDAcR

tuning voltage, phase noise and amplitude comparison between (a) NMOS, (b) PMOS and (c) Push-Pull oscillator

1. For NMOS diff pair Oscillator the tuning range is least, which is 245MHz or 4.3%. The main reason is because of the size of NMOS devices, which was needed to make high in order to have firstly, the much required over drive and high $\frac{g_m}{g_{ds}}$ ratio in order to make device work in saturation region. The device length was increased to 480nM in order to lower the threshold to maximize the overdrive and then maximize for $g_m$, while the device length of PMOS/Push-Pull diff-pair was kept at minimum. The influence of parasitic in NMOS can be seen in the phase noise graph, which for 1mW of power was found to be -104.2dBc/Hz. These leaves us with a definite result that NMOS only Oscillator is not going to be used in Q-VCO. Firstly, the tuning range is poor and secondly the phase noise is not so good in comparison to PMOS and Push-Pull for same amount of power consumption.

2. Since we are left with now PMOS only and Push-Pull topology, and analyzing Figures 4.23 and 4.24 (b) and (c), we notice that the tuning range offered by PMOS only topology is around 800MHz or 14.28% in comparison to 721MHz or 12.78% offered by Complementary oscillator. The Phase noise comparison follows the analysis that was presented in section before, with an improvement of around 1dB of phase noise in push-pull topology not 6dB as derived in [74]

Figure 4.23: (a) Tuning Range NMOS Diff-Pair Oscillator
Figure 4.23: (b) Tuning Range PMOS Diff-Pair Oscillator

Figure 4.23: (c) Tuning Range Complementary Diff-Pair Oscillator
An Oscillator System for UWB QDAcR

Figure 4.24: (a) Phase noise of NMOS Diff-Pair Oscillator @ 1MHz offset

Figure 4.24: (b) Phase noise of PMOS Diff-Pair Oscillator @ 1MHz offset
An Oscillator System for UWB QDACR

Figure 4.24: (c) Phase noise of Push-Pull Diff-Pair Oscillator @ 1MHz offset

The Figure 4.24(c) also shows the variation of phase noise with respect to change in value of source degeneration resistor, as we can analyze that phase noise get better by 2.3dBc@1MHz offset when a source degeneration resistor of 100 Ohms is used when compared to phase noise when a resistor of 500m Ohms was placed.

If we try to arrive at certain result using the tuning range and phase noise results, it is found that not much conclusive enough to choose between PMOS only and Push-Pull topology as one offers 1.5% higher tuning range and other offers phase noise improvement of 1.2dBc/Hz. Next is to look onto the swing offered by PMOS only and Push-Pull topology. The swing is differential peak to peak oscillator output voltage. Which can be maximum of 2.4V as our Vdd is 1.2V. The swing as stated is plotted in Figure 4.25 below.
On comparing Figure 4.25 (a) and (b), it is noticed that NMOS offers terribly low swing of 559.61 mV in comparison to PMOS swing of 1.365V. If we look at the Figure 4.25 (c) the push-pull topology offers the highest swing of 1.955V, which follows the theory and as anticipated. Therefore, voltage swing, which is needed to be as high as possible in order to compensate for the loss in buffer and or poly-phase filter, is chosen. This translates that push-pull topology to hold merit over PMOS only topology for low power consumption.

Figure 4.25: (a) Peak to Peak Differential Voltage output of NMOS Oscillator

Figure 4.25: (b) Peak to Peak Differential Voltage output of PMOS Oscillator
An Oscillator System for UWB QDAcR

Figure 4.23: (c) Peak to Peak Differential Voltage output of push-pull Oscillator

The Results of complete analysis are summed up in the table 4.6 below

<table>
<thead>
<tr>
<th>Oscillator</th>
<th>Tuning Voltage (V)</th>
<th>Oscillation Frequency (GHz)</th>
<th>Phase Noise @ offset of 1MHz (dBc/Hz)</th>
<th>Tuning Range (%)</th>
<th>Differential Voltage Swing peak to peak (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS only</td>
<td>.43</td>
<td>5.59981</td>
<td>-104.2</td>
<td>4.3</td>
<td>0.55961</td>
</tr>
<tr>
<td>PMOS only</td>
<td>.65</td>
<td>5.60207</td>
<td>-111</td>
<td>14.28</td>
<td>1.365</td>
</tr>
<tr>
<td>Push-Pull</td>
<td>.68</td>
<td>5.6063</td>
<td>-112.2</td>
<td>12.78</td>
<td>1.955</td>
</tr>
</tbody>
</table>

Table 4.6: Oscillators Comparison

Since we have made choice of going for push-pull oscillator, therefore for its robustness and functionality it should be tested. From the very start of circuit design through the reading of design manual, the process related variations like (stress effect, matching proximity and body resistance etc.) were used to strict conditions so that final circuit can qualify for its robustness. However, a few changes and small parameter tweaking were required in end.

In Figure 4.26 (a) and (b) the results of all the process corners (7 in total), 5 performance based which are TT (typical or normal run), FF (fast-fast, used for delay and particularly for oscillators), SS (slow-slow, for delay and for oscillator performance of jitter that is phase noise), SF and FS (Slow-Fast and Fast-Slow, for

-156-
skewness between NMOS and PMOS devices) and FF-Functional and SS-Functional (to verify circuit performance under extreme conditions). *For more on process corners, refer to IBM-CMRF8SF Model Design Kit.

![Figure 4.26: (a) Tuning Range comparison of push-pull oscillator for all the process corners.](image)

If we analyze the Figure 4.26 (a), it is noticeable that circuit does qualify for extreme SS-F and FF-F corners. An average tuning range of 13.6% is observed over all the process with worst of close to 13% for FS corner. Therefore the circuit needs some tweaking and the varactor average capacitance needs to be reduced to around 350 fF in order to raise the oscillation frequency. This is done also because the layout and packaging related parasitic are mainly capacitive and resistive in nature, which will automatically bring down the oscillation frequency. Therefore to be sure that post layout oscillator works in the vicinity of 5.6GHz frequency, it becomes imperative that we raise the oscillation frequency. Now the question is by how much, because the net effect of parasitic can only evaluated after post layout simulation and parasitic extraction. However by some reading from manual and mainly learning from the experience of IC-designers, an offset of 100-200MHz was considered, also QDAcR architecture provides a tolerance of
±125MHz, which safely qualifies our oscillator. The Figure 4.26 (b) shows the value of differential peak to peak amplitude for all the process corners.

![Amplitude comparison of push-pull oscillator for all the process corners.](image)

The amplitude 4.26 (b) shows that highest amplitude is noticed for SF corner and lowest for FFF corner, in phase the worst phase noise -110.55dBc/Hz was recorded for SS-F corner, while the best phase noise was found out to be -114.88dBc/Hz for FS corner. However, during circuit design care was taken that transconductance of both PMOS and NMOS should be same however it is noticed that PMOS transistors have higher influence, reason could be their comparatively large size and/or the use of PMOS current source.

The final corner analysis with changed varactor for SS-F and FF-F corners is given below in Figure 4.27 (a) and (b).
The Figure 4.27 (a) shows the tuning range with reduced varactor capacitance. The tuning range is somewhat reduced to average value of 12.33%, however our circuit can safely work in extreme conditions and some effect of possible parasitic has been compensated during schematic design only. Figure 4.27 (b) shows the differential peak to peak output voltage swing and it can be inferred that the voltage swing in adverse effect has changed by ±4%. The phase noise values of two corners SS-F and FF-F at 5.75GHz oscillation frequency were noticed to be -113.8dBc/Hz and -113.38dBc/Hz respectively. Therefore, we can now comment for sure that our design does meet low power (1mW), considerable better phase noise than required and high swing.
Hence, this concludes our design of LC-tank oscillator, the in depth process analysis was necessary as this oscillator will serve as the main component while design of Quadrature output VCO (Q-VCO), whether we use the cross-coupling method or poly-phase RC-filter for the generation of quadrature signals, this oscillator will serve has the back-bone of Q-VCO.

4.7 Layout Design Considerations

Points to ponder about layout: The layout in itself has required complete set of design rules to be followed, which are mostly process technology specified. But, it is advisable to consider the effect of parasitic while designing the schematics. The parasitic, which can de-Q (lessen the Q-factor) or affect change in the value of any vital component should be paid attention. With regard to LC-tank performance the main elements are parasitic capacitance from interconnects, bond-pads and active devices and parasitic resistances and inductances from interconnects, bond-wires, rf-lines etc.

The value of bond-wire inductance in some cases is very much comparable to the required value, therefore it becomes essential to mitigate such performance degrading effects, the effect of bond-wires depend solely upon the type of packaging used for the chip, for e.g. flip-chip does not require bond-wires but suffer from high capacitive loading. In order to connect chip to outer-pads bond wires are not required then the value of
chip inductor is not influenced till extent and taken care by proper ground shielding and isolation. In this case the advantages of high Q-factor of inductor and high-phase noise can still be reaped. The length of interconnects between the oscillator and other RF on chip components, because as discussed previously interconnects serves as transmission lines and do suffer from ohmic losses in different mode of operations. The inductive parasitic component of the parasitic can be harmful, this can be taken care of by having high width or increased maximizing interconnects, which not only decrease the parasitic inductance but parasitic resistance also. However, this comes with cost of increased parasitic capacitance. The resistivity and capacitance of different metal layer as interconnect are defined and characterized in the design manual. However as of now, the oscillation frequency is offset by 150MHz. to take care of parasitic capacitance and inductances. The layout of current-source should be as symmetrical and square or in ring geometry, with high numbers of fingers as prescribed and simulated in [68].

4.8 Conclusions

In this chapter a complete overview of LC-tank design was discussed, our discussion and analysis resulted in design of a LC-tank, which based on analysis should provide optimum results. Further in the chapter a design methodology regarding oscillator design was discussed and verified through simulations. Three differential oscillators, namely NMOS, PMOS and Complementary (Push-Pull) oscillators were simulated and analyzed. The Push-Pull topology turns out to provide best results which meet our required specifications and mainly constraint of low power consumption. The complementary oscillator was tested over all the process corners and the result seconds our choice of topology. Therefore, Push-Pull oscillator is a solution to proceed further on to the design of Quadrature VCO. An Oscillator being the fundamental component for Q-VCO design, the solution turns out to be a complementary oscillator. In next chapter we discuss and design Q-VCO, which meets our specifications.
5 CHAPTER 5

Quadrature Voltage Controlled Oscillators (Q-VCO): Introduction and Circuit Design Implementation

We have seen in our discussion of receiver architectures in chapter 3, that for LOW-IF, Zero-IF or Homodyne receiver architectures the importance of a proper quadrature signal becomes even more crucial. As we see that for high data rate or high bandwidth applications the LOW-IF topology is becoming popular and gaining more and more interest of designers. In this chapter we explore and compare the ways to generate the quadrature signals from an oscillator, this study is primarily based on the literature research. The next section follows with the description the principle of quadrature generation, followed by principle of injection locking. We then further investigate primarily two Q-VCO topologies, these are Parallel Q-VCO or P-QVCO and Bottom Series Q-VCO or BS-QVCO. The conclusions are drawn after careful analyses over wide range of influencing parameters.

Next, we try to investigate the suitability of quadrature signal generation using a Polyphase filter and delve into the merits and demerits and which way suits most our specifications, whilst consuming the low power. The succeeding topic discusses the usability, design and implementation of the output buffers. The buffers are loaded with variable output, to test the robustness and worthiness of our complete design. The final conclusions are drawn on the basis of quantitative analysis of the results obtained. In this chapter the process corner run or lay-out issues have been discussed invariably, where ever required. This chapter in total presents a complete picture of proposed quadrature oscillator required for impulse radio QDAcR.

5.1 Methods of Quadrature Signal Generation and Q-VCO Principle

In theory and practice we define signals (consisting of real and imaginary parts) to be quadrature in nature if over a period they differ by an angle of ±45° or ±\(\pi/4\) in their phases. For example if we consider a oscillator output sinusoid, then its equation in the form of quadrature components can be written as given by equation 5.1 below.

\[ I(t).\sin(\omega t) + Q(t).\cos(\omega t) \]  

(5.1)

where I(t) is generally termed as in-phase component and Q(t) as quadrature component. And these components are given by equation 5.2 as
An Oscillator System for UWB QDAcR

\[ I(t) = V_o(t) \cos(\phi(t)) \quad \text{and} \quad Q(t) = V_o(t) \sin(\phi(t)) \]  \hspace{1cm} (5.2)

For Q-VCOs the quadrature signals are generally generated in three different ways and these are described as following

1. Q-VCO using a frequency divider: The basic principle of designing of Q-VCO, using an oscillator and a frequency divider is to take a high performance oscillator, which oscillates at twice the required frequency of oscillation and then the frequency is downconverted using a digital divide by two flip-flop or an analog divider as described in [75]. This solution serves two purposes firstly it saves the chip area as the operational frequency goes up the ladder the size and value of inductance required goes down the ladder. Secondly, digital divider generates a more precise quadrature signals, by using digital inverters, which inherently produces Quadrature signals. However, at very high frequencies the ‘Q-factor’ of LC-tank degrades severely, with decrease in inductance value and shifting of operational frequency towards the self-resonance frequency. Until and unless the phase noise and power requirements are relaxed, the digital frequency divide by two solution in not advised. Due to power budget constraints and relaxed specifications for phase error, this solution was not opted.

2. The Use of Poly-Phase filter: Poly-phase filter consists of a RC-CR network, which provides signal a phase shift of ±45°. This solution consumes less power in comparison to previous one. However, this solution is also marred with process related PVT variations, degradation in phase noise and relatively high phase error. Also, the loading of poly-phase filter to an oscillator directly, can cause the change in the LC-tank properties and therefore it requires buffers or high de-caps. In our case, a poly-phase can be a solution due to relaxed specification on phase noise and phase error, and we shall discuss it in detail later in a separate section.

3. The third option consists of cross-coupling of two LC-tank oscillators, as firstly proposed in [76]. This solution surpasses above two in power consumption and offers a variety of other advantages. However, this comes with extra chip area, which should not be much of a constraint if the specification demands so. The option of cross coupled Q-VCO provides high phase noise and more precise quadrature signals than a poly-phase filter and at lower power. Next, the output swing that is provided by LC-tank cross coupled Q-VCO is a much desired output quantity as generally in a RF-chain the next stage is depicted by a mixer, for which LO output serves as an input. Therefore, due to posed advantages the option to have two VCO cross-coupled together seems to be a lucrative one for low power design, while matching all the specifications.

5.2 Q-VCO Principle

In this section we discuss the principle of quadrature signal generation through the cross coupling of two VCOs. This principle was first published in [76], which involves two LC-tank oscillators coupled together
through MOSFETs in parallel to the oscillator transistors, where one coupling is direct one and other is cross coupled. The Figure 5.1 adapted from [76] shows the complete principle of Q-VCO. The two core oscillators are with transistors pairs M1,M2 and M'1,M'2 and the direct coupling transistors are Mc3 & M'c4, while the cross coupling transistors are Mc3 & Mc4.
Figure 5.1: Two Quadrature Coupled Oscillators.
The principle involves that the oscillation in two oscillators can only happen when and only when they synchronize and are in quadrature to each other that is oscillations are anti-phase.

A more generic but in-depth quantitative analysis for couple Q-VCO is presented in [77], this serves as a classic as it deals with the issue of stability and oscillation start-up conditions, irrespective of oscillator’s circuital parameters like sizes of device, dc voltages and currents etc. The postulates from [77] were investigated thoroughly through simulations and quantitative analysis and it was found that there arrives no need to reproduce the mathematical analysis in the thesis. However, the main postulates, are analyzed and further simplified and are presented in brief here, as they serve the very basis for the design of Q-VCO.

1. Stability: The stability is foremost criteria, which is addressed by the Barkhausen’s criteria. This stands for start-up condition as well as phase stability. The solution given is given by equations 24-26 in [77], where the stable modes of oscillation and amplitude stability are expressed. The equation are given as equation 5.3 here

\[
\omega_{\text{osc},1} = \omega_o - \frac{\omega_o \cdot m \cos \phi}{2Q \cdot 1 + m \sin \phi}; A_1 = \frac{4I_o R_p}{\pi} (1 - m \sin \phi) \\
\omega_{\text{osc},2} = \omega_o + \frac{\omega_o \cdot m \cos \phi}{2Q \cdot 1 + m \sin \phi}; A_2 = \frac{4I_o R_p}{\pi} (1 + m \sin \phi)
\]

The subscript ‘1’ and ‘2’ stands for two stable modes, however first mode is conditionally stable and second mode is unconditionally stable and \( m = \frac{I_{\text{coupling}}}{I_{\text{osc}}} \) and \( \phi = \text{Phase Shift between Direct and Cross coupling currents} \). Now, if we consider the two LC-tank oscillators with exact devices and all passives parameter and coupling transistors with transconductance of ‘\( g_{mc} \) ’ then the loop gain equation according to Barkhausen is given by equation 5.4

\[
1 \leq -g_{mc}^2 \left( \frac{j \omega_{\text{osc}} L}{1 + j \omega_{\text{osc}} L \left( \frac{1}{R_p} - g_m \right) - \omega_{\text{osc}}^2 LC} \right)^2
\]

Solving this equation for composite oscillation frequency of both the oscillators, we can deduce that it also shows two modes of oscillation, one with oscillation frequency which is ahead of normal oscillation frequency that is without coupling. In second state the oscillation frequency lags behind the normal oscillation frequency. The values are given by equation 5.5

\[
\omega_{\text{osc}} = \omega_o \pm \frac{g_{mc}}{2C}
\]

If we analyze we see that the coupling transconductance and coupling factor are dependent through the tank ‘Q-factor’, higher the quality factor most strong will be coupling. Therefore for quadrature oscillation
stability and amplitude stability a high ‘Q’ and high value of ‘m’ or high value of transconductance of coupling transistors is necessary

2. Phase Error due to mismatches: In [77] it is postulated that phase error Δϕ is a function of phase shift ‘ϕ’ and the quadrature accuracy is most dependent on the mismatches and PVT variations when ϕ = 0° and least dependent when ϕ = 90°. In [78] this postulate is extend to the circuit parameter, and it results that in order to have a better phase noise and less amplitude and mismatch errors than a common current source should be used for oscillator core as well as coupling transistors.

3. Phase Noise: the phase noise of Q-VCO is given by equation 52 in [77], which is as follows and reproduced as equation 5.6

\[ \Delta \omega = \frac{1}{2} \log \left( \frac{kT(1+F)}{O_{eff,Tank}^2 V^2 \left( \frac{\omega}{\Delta \omega} \right)^2} \right) \]

where \( O_{eff,Tank} = Q \sqrt{1 + \frac{m \cos \phi}{1 + m \sin \phi}} \) (5.6)

If we see the value of phase noise for couple Q-VCO we find that for \( 0 \leq \phi \leq \frac{\pi}{2} \) the value of phase noise improves with a maximum of 2dBc/Hz in comparison to un-coupled or stand-alone oscillators.

This sums up as fundamental but robust analysis of main factors, which can seriously degrade the performance of a cross coupled Q-VCO.

5.3 Principle of Injection locking

So far we analyzed all the major influencing factors for quadrature accuracy and stability. However, we have not discussed about the limit of frequency fluctuation. We have noticed that cross coupled Q-VCO operates at a common frequency, which is deviated or at a difference from the oscillation frequency of a stand-alone oscillator. This deviation or the frequency range over which two oscillators can lock with each other is called lock range ‘Δω’ and the principle in itself as injection locking. Mathematically it is given by equation 14 and 15 in [77], which are expressed here as equation 5.7

\[ \frac{I_{inj}}{I_{osc}} \geq \frac{4}{\pi} \frac{1}{\left( \frac{\omega}{2Q} \right)^2 + \Delta \omega^2} \]

where \( \Delta \omega = \frac{\omega_o}{2Q} \left( \frac{1}{\sqrt{\frac{2}{Q} I_{inj}}} \right) - 1 = \frac{\omega_o}{2Q} \left( \frac{1}{\sqrt{\frac{2}{Q} I_{osc}}} \right) - 1 \) (5.7)

If we analyze this equation of importance then we see that in order to safe guard that our oscillator lock to provide quadrature oscillator then we should trade off with phase noise, by decreasing the Q-factor or...
increasing the Injection current of coupling transistors, which in turn results in higher $g_m$ and higher oscillator bias current. Therefore, we should go for high transconductance for coupling transistors or high value of coupling factor ‘m’ for robust locking range and ensuring quadrature oscillations.

5.4 Implementation of Q-VCO using injection locking

If we consider any differential pair cross-coupled stand-alone oscillator, then we can easily find that the injection into this oscillator can happen in 3 ways, firstly by parallel injection, which is most common and proposed in [76] and commonly known as P-QVCO or parallel coupled Q-VCO. The second topology is as described in [79, 80] where injection is done in series with the oscillator core transistor, this can be done at drain or source node therefore commonly known as Top series Q-VCO or TS-QVCO and bottom series or BS-QVCO. Third and lastly by modulating the gate of cross-coupled oscillators by injecting signal [81]. The far reaching claims of better performance has been made by [79, 80, 81] over the P-QVCO. Therefore it was decided to investigate P-QVCO and BS-QVCO topologies in their entity and use the best option. The last topology was left out of analysis, because preliminary analysis showed not much conclusive difference between the results with respect to BS-QVCO.

5.4.1 Methodology for Quadrature Oscillator Design

The basic design principles for oscillator design remain the same as discussed in the previous chapter in detail. Also, the push-pull topology designed oscillator is used to design the Q-VCO. The points of consideration we have mentioned in our stability and injection locking analysis. Now we first start with analysis of BS-QVCO followed by analysis of P-QVCO and then arriving at the conclusion. A few design considerations

1. Increasing the oscillator bias current to 1mA, in order to ensure proper locking.

2. DC-Biasing re-evaluation, in order to make sure sufficient overdrive and to ensure sufficient gain to keep diff-pair transistors in saturation

3. Using same or common current source as mentioned in [78, 79, 80] to reduce amplitude related errors and better quadrature performance.
a) **Bottom Series Q-VCO**: The theory and implementation of series injection has been reported with added emphasis and quoting very good results in [79, 80]. The model for BS-QVCO with its basic analysis has already been presented in these papers. The highlighted points are that series QVCO provides better phase noise, higher output swing and better phase error than P-QVCO, under the conditions of same power consumption and same coupling factor.

We started with taking already optimized push-pull VCO which suits our requirements. Then two transistors were added in series with the PMOS-diff pair as shown in Figure 5.2. The single VCO is shown as two vco are exactly similar and the coupling nodes are connected in direct and cross-coupled fashion as desired. Two points are worth mentioning here 1) Use of Degeneration resistor, in order to keep the simulations and design conditions as similar as possible, we did not omit out the degeneration resistors. One would argue that when series transistor in itself acts as a degenerated source, but it was seen in preliminary analysis that phase noise was 2dBc/Hz. better with degeneration resistors. Therefore resistors were kept part of the circuitry. 2) The DC analysis of the circuit, as we have already designed the push-pull topology in accordance with the prescribed design methodology therefore all the changes were made in the coupling transistor in order to change the coupling factors for analysis.
Figure 5.2: BS-QVCO (Half Circuit)
As mentioned in [80] the coupling factor in series injection is defined by the ratio of transconductances of coupling transistor and Oscillating transistor that is ratio transconductances of transistors Mc1 and M1. The results for various values of coupling factor are tabulated below.

<table>
<thead>
<tr>
<th>Coupling Factor</th>
<th>Tuning Voltage @ 5.6GHz (V)</th>
<th>Phase Noise @ 1MHz offset (dBc/Hz.) 1.2V=Vtune</th>
<th>Phase Error (degrees)</th>
<th>Tuning Range (%)</th>
<th>Differential Voltage Peak to Peak (V)</th>
<th>Amplitude Error (Relative)</th>
</tr>
</thead>
<tbody>
<tr>
<td>.3302</td>
<td>1.022</td>
<td>-115.5</td>
<td>0.1</td>
<td>13.06</td>
<td>1.8173</td>
<td>.055</td>
</tr>
<tr>
<td>.354</td>
<td>.99</td>
<td>-114.892</td>
<td>0.2</td>
<td>12.75</td>
<td>1.972</td>
<td>.051</td>
</tr>
<tr>
<td>.4362</td>
<td>.91239</td>
<td>-113.982</td>
<td>0.25</td>
<td>11.55</td>
<td>2.131</td>
<td>.05</td>
</tr>
<tr>
<td>.4826</td>
<td>.8344</td>
<td>-113.92</td>
<td>0.25</td>
<td>10.95</td>
<td>2.21</td>
<td>.047</td>
</tr>
<tr>
<td>.5162</td>
<td>.7535</td>
<td>-113.93</td>
<td>0.1</td>
<td>10.51</td>
<td>2.247</td>
<td>.043</td>
</tr>
<tr>
<td>.5416</td>
<td>.67109</td>
<td>-113.98</td>
<td>0.08</td>
<td>10.16</td>
<td>2.265</td>
<td>.035</td>
</tr>
<tr>
<td>.5975</td>
<td>.01</td>
<td>-114.33</td>
<td>0.013</td>
<td>9.25</td>
<td>2.27</td>
<td>.031</td>
</tr>
</tbody>
</table>

Table 5.1: BS-QVCO Simulation Analysis

In the simulation analysis of BS-QVCO two important observations were made.

1. The coupling factor in BS-QVCO is very much range bound. This means that for constant current and low supply voltage regime, the way to change coupling factor is to change the device size. Therefore, for low coupling factors in our case m=0.3, the coupling transistor MC1 sends the oscillator transistor to cutoff region that is the gate drive voltage of M1 becomes less than the threshold voltage. Second, the upper limit of coupling factor is dictated by current clipping. Because on increasing the coupling factor or transconductances ratio we observe that, the current drawn into the oscillator become higher, the reason is the increase in the current source output impedance, due to coupling transistor, which works as a high resistive impedance in triode region. However, after certain value in our case m=0.54, the amplitude swing starts to saturate.

2. If we observe the table 5.1 carefully then it can be noticed that better phase noise performance is also range bound. The reason of high phase noise associated with degeneration/triode state of coupling transistor has been commented and appreciated in [80]. However, the effect of series coupling topology in lowering of flicker noise contribution is optimal till only certain extent, as matter of fact Mc1 working in deep triode region starts adding its own thermal noise current to the oscillator and the desired advantage to be reaped from less flicker noise up conversion is lost in total. In addition, the parasitic capacitive effect due to large
b) **Parallel Coupled QVCO or P-QVCO**: In P-QVCO the desired coupling is performed by putting coupling transistors in parallel with the oscillator diff-pair. The principle, mathematics has been described in detail in [76, 77]. The half circuit of P-QVCO is shown in figure 5.3 below. The coupling transistors Mc1 and Mc2 necessitate the proper injection locking with the core oscillator. As discussed and derived previously the quadrature accuracy and locking can be achieved through high coupling factor values. The results of simulation are tabulated in table 5.2, where the coupling factor is changed by changing the width of the coupling transistor, while keeping the devices in saturation mode of operation.

![Figure 5.3: The Mirror half circuit of P-QVCO](image)

In conclusion, it can be said that BS-QVCO is best suited for much more power budget relaxed oscillator. It definitely offers higher swing as anticipated and explained in [80] but on the other hand deteriorates tuning range and phase noise. In low power oscillator design the advantages offered by BS-QVCO can not be fully explored or some drastic design changes needs to be made for e.g. use of switchable capacitive bank as varactor in order to preserve the tuning range.
An Oscillator System for UWB QDAcR

<table>
<thead>
<tr>
<th>Coupling Factor</th>
<th>Tuning Voltage @ 5.6GHz (V)</th>
<th>Phase Noise @ 1MHz offset (dBc/Hz.)</th>
<th>Phase Error (degrees)</th>
<th>Tuning Range (%)</th>
<th>Differential Voltage Peak to Peak (V)</th>
<th>Amplitude Error (Relative)</th>
</tr>
</thead>
<tbody>
<tr>
<td>.3293</td>
<td>1.001</td>
<td>-115.5</td>
<td>0.21</td>
<td>12.4</td>
<td>1.8139</td>
<td>.063</td>
</tr>
<tr>
<td>.3512</td>
<td>.98871</td>
<td>-115.48</td>
<td>0.2</td>
<td>12.33</td>
<td>1.807</td>
<td>.0635</td>
</tr>
<tr>
<td>.435</td>
<td>.9623</td>
<td>-115.4</td>
<td>0.16</td>
<td>11.7</td>
<td>1.78</td>
<td>0.54</td>
</tr>
<tr>
<td>.4828</td>
<td>.94276</td>
<td>-115.28</td>
<td>0.13</td>
<td>11.56</td>
<td>1.77</td>
<td>0.051</td>
</tr>
<tr>
<td>.5170</td>
<td>.9263</td>
<td>-115.25</td>
<td>0.1</td>
<td>11.49</td>
<td>1.764</td>
<td>0.045</td>
</tr>
<tr>
<td>.5425</td>
<td>.91814</td>
<td>-115.21</td>
<td>0.03</td>
<td>11.41</td>
<td>1.76</td>
<td>0.044</td>
</tr>
<tr>
<td>.613</td>
<td>.9103</td>
<td>-115.169</td>
<td>0.015</td>
<td>11.23</td>
<td>1.74</td>
<td>0.040</td>
</tr>
</tbody>
</table>

Table 5.2: P-QVCO Simulation Analysis

The coupling factor ‘m’, this is given by $m = \frac{I_{\text{coupling}}}{I_{\text{dc}}} = \frac{W_{M1}}{W_{M1}}$, serves as the most influencing parameter in defining the Quadrature accuracy and as far now, it was varied by changing the device width. For simulation purposes this works fine. However, in real circuit, one the device has been fabricated, no more changes in geometry are plausible. Therefore, three solutions are possible, first that choose a fixed geometry that corresponds to a particular coupling factor. However, this solution suffers from PVT variations and mismatch, therefore in order to guarantee Quadrature oscillations, the designer needs to characterize the design for its robustness and secondly need to keep the a large coupling factor. The necessity to keep large coupling factor comes at an added cost of lowering the phase noise and swing.

The other method is to control the gate bias of the coupling transistors and thus controlling the current through the device and hence controlling the coupling factor. In such design, an extra reference circuitry is required in order to calibrate against the PVT and mismatch variations. Therefore, this solution does not guarantee much desired dynamic coupling factor, until and unless the reference circuitry characterized for its accuracy.

The third viable option is to put switchable bank of coupling transistors in parallel to the oscillator diff-pair. This solution is best suited, since we can control the coupling factor dynamically. In order to ensure Quadrature generation the initial factor can be set to high value like .5 or .6 and then reduced to .3 or .2 in order to take full advantage of better phase noise and large swing.
The use of option three seems to be lucrative because of its posed advantages, however in low and constant current regime, the option one is most suitable. The reasoning being that the transconductance of the diff-pair plays an important role in the start-up condition and it is dependent on the oscillator bias current. Since we are using a common current source for coupling transistors as well as oscillator biasing, therefore the bias current is being shared by oscillator core, and coupling transistors in accordance with the coupling factor value. So, any sudden switching of coupling transistors will lead to change in the transconductance of the diff-pair.

If we analyze tables 5.1 and 5.2 simultaneously, we can draw some realistic comparisons between the performance of BS-QVCO and P-QVCO. Firstly, if we compare the phase noise change in two Q-VCOs with respect to the same coupling factor and for same power consumption. As shown in the Figure 5.4 (a) the phase noise of P-QVCO is less susceptible to coupling factor in comparison to BS-QVCO. P-QVCO performance is better than BS-QVCO for low power consumption and smaller device size. A difference of 1dBc/Hz @1MHz offset is measured for coupling factor of 0.6.

![Figure 5.4: (a) Phase Noise comparison between P-QVCO and BS-QVCO](image)

The next graphs 5.4 (b) and (c) depicts the comparison between P-QVCO and BS-QVCO for tuning range and the phase error. If we analyze these graphs then again it is quite visible that P-QVCO give better phase noise and comparative phase error. Therefore, apart from swing, on all accounts the P-QVCO performances better than BS-QVCO. These results and analysis which shows that P-QVCO is best choice for low power and constant current regime. Therefore, we zero upon P-QVCO as our choice for Quadrature oscillator for QDAcR. In next section we test the robustness of our P-QVCO over all the process corners and Monte Carlo analysis.
After making the choice between the BS-QVCO and P-QVCO, the robustness of P-QVCO design is tested against the PVT variations. The process corner analysis of P-QVCO is presented in Figures 5.5, 5.6 and
5.7. The Figure 5.5 shows the tuning range across all the process corners. It can be seen that design and devices do qualify for specs regarding the tuning range requirement, the worst tuning range provided is 11.231% at coupling factor value of 0.6. The phase noise variation across all the process corners is shown in the Figure 5.6, from which it can be discerned that even for a higher coupling factor of 0.6 the circuit provides good enough phase noise of -115dBc/Hz @1MHz offset, which is better than the required specs and provide the extra cushion at low power consumption. Furthermore, from Figure 5.7 we can discern that output signal of P-QVCO in worst case provides a single ended Vpk-pk swing of 800mV, which allows extra headroom in power consumption for succeeding buffer stage.

Figure 5.5: Process Corner Analysis of P-QVCO for tuning range
Figure 5.6: Process Corner Analysis of P-QVCO for phase noise.

Figure 5.7: Process Corner Analysis of P-QVCO for Quadrature Swing
The process corner analysis confirms the robust design nature of Q-VCO. This P-QVCO stands on all the counts of performance and suffices to be a good solution to our problem statement. Therefore, with a total power consumption of 2.4mW, phase noise of -115dBc/Hz @1MHz offset and average differential swing of 1.7Vpk-pk, this P-QVCO is our choice as a Quadrature oscillator for QDAcR. Therefore, it can be concluded that P-QVCO proves to be best possible option when compared with BS-QVCO. However, Poly-Phase filter does provide another viable option, which is being exploited in next section.

5.5 Q-VCO implementation using Complementary VCO, Poly-Phase filter and output buffers

This Q-VCO is designed using the basic and optimized push-pull VCO from the Chapter 4. The Poly-Phase filter is loaded to the VCO using the output-buffers, which are designed to drive variable and can be implemented as output stage in case of P-QVCO. The implementation in block diagram is show as in Figure 5.8

![Figure 5.8: Implementation of Q-VCO with Poly-Phase Filter](image)

5.5.1 Poly-Phase Filter Design and Implementation

In this section the design and implementation of Poly-phase filter is depicted. As described in previous sections that a poly-phase filter consist of RC-CR networks. The generic poly-phase filter is shown in the Figure 5.9 below, the two outputs are in quadrature that the phase difference between the two outputs is 90 degrees. The mathematics is described in detail is [39], which results that the outputs are in quadrature for all the values of frequency, however they are equal in magnitude that is in amplitude only when the angular frequency, \( \omega = \frac{1}{RC} \).
Due to very nature of passives, the poly-phase performance is dependent upon the PVT variations, therefore an intelligent design methodology has to be adopted for choosing the appropriate passives and passive specs based on the simulation and information gathered from technology design manual and taking into account layout and PVT variation considerations. The design strategy is explained hereunder.

1. Calculation for number of stages required: The desired poly-phase filter should be able to provide quadrature outputs while meeting the specs. Firstly, the bandwidth of the filter response should match or more than the tuning range of the oscillator. Therefore, the best way is to put two poles at lowest and highest frequency of the tuning range. Therefore, the minimum required stage turns out to be a 2 stage poly-phase filter.

2. The choice of proper passive from the process library: The spreads in RC filter should be as minimum as possible for less amplitude error and phase error. Based on the investigation of design manual and comparing all the resistors for best mis-match sensitivity, least parasitic, absolute resistance value and tolerance. It resulted in the choice of L1-BEOL, however this resistance does poses layout hardship, but by having one extra mask and proper layout this problem can be taken care of. Therefore, finalizing on L1-BEOL resistor.

3. The choice of capacitor was limited to MIM cap as offered by process technology (DM), while High K MIM cap are available for OL/LM options. Therefore, deciding on the MIM cap, next step was to choose the number of layers. In DM process metal layers 2, 3 and 4 can be used as thin metal later and 1 and 2 as thick metal layers. Choosing layer 3-2 for the MIM caps, by simulating and reading the correlation plots in design manual for the least parasitic and feature size. The next step involved was to choose between the single or dual MIM cap, analyzing the data from manual results that for small value of capacitance single MIM cap gives better error% and less parasitic for comparable mismatch. Therefore, finalizing on single MIM cap with 3-2 metal layers.

4. Next Step, was to choose the proper values of passives that is the values for resistor L1-BEOL and MIM cap. In case of resistance the resistor cut-off frequency plays the limiting constraint as parasitic capacitance increases, which results in increased phase error. Also, large resistors induce
more thermal noise, but since phase noise and phase error requirements are bit relaxed and importantly larger resistor helps in low power design, therefore we go for largest resistor. This makes to minimize the value of MIM cap, which in turn also effective as it reduces the capacitive loading and amplitude squegging. Choosing the minimum capacitance size that is 97fF for 5micron x 5micron MIM cap feature size, gives us resistance value of approximately 293 Ohms.

5. Since we have chosen passives with lowest possible error, parasitic and mismatch offered my technology, therefore spreads are curtailed down therefore choosing poles with total tolerance of 10%

The design process described above serves as the basis poly-phase filter design. The Figure 5.10 below shows the complete circuit design of VCO, buffers and Poly-phase filter. The design of output buffer is presented in the next section

![Figure 5.10: Circuit Design for Poly-Phase Filter Q-VCO.](image)

### 5.5.2 The design of Output Buffer

In order to mitigate the effect of direct loading of Poly-Phase filter either a de-coupling capacitor of a minimum value of 30pF, however it will De-Q the resonator, as well compromise the amplitude swing of the oscillator and employing such a big de-cap depends upon the layout size also. Therefore, a careful option is to employ output buffers, the output buffer presented here also serves for P-QVCO as the S-parameter analysis provides with almost similar matching impedances, because of common VCO in both the cases. In case of P-QVCO buffer drives the bond-pad (modeled on the basis of design manual) or mixer
An Oscillator System for UWB QDAcR

gate, therefore tested to drive predominantly capacitive load from 50fF to 600fF for a maximum power consumption of 3mW.

Choice of buffer topology: Voltage buffer or common drain serves as a basic topology for VCO buffers, however the swing is sacrificed in this case and also big biasing ‘T’ inductor and capacitor is required in order to make voltage buffer functioning for low power regime. Also, the output loading at source node of common drain buffer can severely degrade oscillator’s performance, because the effect of Beta transformation the capacitive load or impedance effects the input impedance of the buffer and this needs careful matching and designing. However, Common source topology, if properly biased serves as a basic output buffer withholding the oscillator swing amplitude. Nevertheless, in order to have proper design and desired gain at low power consumption a proper design of common source is required like use of neutralization capacitors and inductor for biasing as well as proper pole management. The differential parallel inductor is used in buffers.

Also, common source buffer further reduces the common-mode noise, therefore choosing Common Source as out-put buffer topology. Starting with the biasing current source/Mirror design, the approach as used in oscillator current source design is being employed here. For the same reasons of lesser noise contribution and suppression of common-mode oscillations at fundamental and second harmonic as explained in detail in previous chapter. The net contribution of common-mode noise and common-mode oscillation is tackled using cascode source with a very small transistor, the common mode oscillation is highly undesirable in order to ensure stability.

The instability or unwanted oscillation can also be caused by $C_{gd}$ of buffer transistors, that needs to be mitigated by use of inductive biasing and mainly using the neutralization capacitance. This neutralization capacitance reduces the effect of $C_{gd}$ and improves the gain of amplifier by reducing the feedback effect through parasitic gate-drain capacitance. The neutralization capacitors are implemented as shown in Figure 5.10 as the cross-connected capacitors. The small signal analysis provides the mathematical insight into neutralization capacitance value, which is given as $C_{nc} \equiv (1+\alpha)C_{gd}$, where $\alpha$ is a ratio of gate resistance of buffer transistor and total negative resistance of the oscillator at oscillation frequency. it can be further approximated as $C_{nc} \approx C_{gd}$, however a bit higher value is good, however over compensation can lead to positive feedback and in turn oscillation and instability. Since, the value of $C_{gd}$ is device size and bias dependent, therefore S-Parameter analysis of the buffer, looking at the input impedance is desirable in order to find value of neutralization cap. The value for the chosen buffer comes out to be approximately 80fF. Therefore, neutralization capacitance in nearing range is used. The Figure 5.11 shows the sweep of phase noise for various values of neutralization cap, which additionally supplements the value derived from S-
An Oscillator System for UWB QDAcR

Parameter analysis. The best phase noise of -109.6dBC/Hz@1MHz is observed for neutralization cap of 80fF.

The other validation of proper design of output buffer is proved by Figure 5.12 below, it shows the differential amplitude swing and it can be seen that for 80fF and power consumption of 3mW the buffers provides output gain of approximately 4dB, where as the loss of 6dB is noticed within poly-phase filter.

Figure 5.11: Phase Noise Vs. Neutralization Cap

Figure 5.12: Output Swing Comparison for Oscillator, Buffer and Poly-Phase outputs.
An Oscillator System for UWB QDAcR

The comparison for performance of P-QVCO and Poly-phase Filter is presented in the table 5.3 below as

<table>
<thead>
<tr>
<th>Oscillator</th>
<th>Tuning Voltage (V)</th>
<th>Oscillation Frequency (GHz)</th>
<th>Phase Noise @ offset of 1MHz (dBc/Hz)</th>
<th>Differential Voltage Swing peak to peak (V)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-QVCO</td>
<td>.800</td>
<td>5.6530</td>
<td>-115.1</td>
<td>1.7815</td>
<td>2.4</td>
</tr>
<tr>
<td>Poly-Phase</td>
<td>.680</td>
<td>5.60689</td>
<td>-109.7</td>
<td>1.16</td>
<td>4.8</td>
</tr>
</tbody>
</table>

Table 5.3: Comparison between P-QVCO and Poly-Phase Implementation

It can be seen that P-QVCO surpasses the performance of poly-phase implementation on all specs and mainly the low-power consumption. Therefore, it is a right decision to choose P-QVCO as a Q-VCO required for QDAcR.

5.6 Conclusion

In this chapter, we extensively investigate various Q-VCO topology, a comparison between P-QVCO and BS-QVCO serves as highlight, as it is realized that different topology offers different merits. BS-QVCO definitely matches ad surpass the performance of P-QVCO but this is only possible in higher power consumption regime. For low power consumption P-QVCO is a definite and best possible choice among the options investigated. A complete robust design of P-QVCO with degenerate resistors being provided and its comparison with a poly-phase implementation further stamps the selection of the P-QVCO. The output buffers with neutralization cap and variable load driving capacity were also presented. This in total suffices as a complete circuit design for an Ultra-wideband Oscillator system, designed to perform at low power consumption, while exhibiting noticeable figure of merit. A Q-VCO system with a figure of merit of 186.36dB is presented, which satisfies all the laid down specifications.
6 CHAPTER 6
Conclusions and Future Work

6.1 Conclusions

This thesis work encompasses a complete design of QDAcR Downconverter and Quadrature Oscillator System for QDAcR in particular. The extensive quantitative analysis and modeling at system level helped in deriving the vital specifications, while the proper and robust circuit design resulted in a pragmatic and fully operational Q-VCO system.

Starting by highlighting the results obtained and important conclusions drawn from system level modeling, which hold importance to this work as well as in regard to scientific community.

1. A complete quantitative modeling of QDAcR is being presented in chapter 2. This results in arriving at equation of prominence (Equation 2.43), which not only captures the total effect of stochastic perturbations such as noise, jitter and device behaviour for QDAcR in particular, but provides a simplified and ready to use model for other low (Zero) – IF receivers.
2. Re-visiting the relationship between timing jitter and phase noise, while characterizing jitter as a Gaussianly distributed stationary stochastic variable.
3. Modeling of a real oscillator in matlab, this modeling served as the basis in order to find the desired specifications for a QDAcR downconverter.
4. Unraveling for the first time based on comprehensive quantitative modeling and system analysis the phase noise requirement in QDAcR in particular and fully extendible to template and energy correlating wideband receivers.
5. Modeling, implementing and testing of different pulse for their spectral efficiency
6. An all-inclusive modeling of QDAcR while addressing the issue of interference, a proposed architecture with filters, which increases the process able bandwidth to 76% of the total available bandwidth. The composite view of time and frequency domain treatment of bandwidth.

Thus summing up the important conclusions drawn from the system level modeling, this helped in laying the basis for the circuit design. The circuit design involved the design of Q-VCO, that meets all the desired specifications. The work in circuit design can be highlighted as follows:

1. Development and Implementation of algorithm in order to find best suitable or to say optimized value of inductor ‘L’ and capacitance ‘C’ whilst targeting low power consumption and better phase noise.
2. Exploiting possible differential topologies for LC-Oscillator and comparing them in depth for the best possible option in accordance with the specs.
3. Designing of a robust Push-Pull Oscillator, which satisfies all the specs and operable in deep sub milli-watt power regime. This oscillator exhibits a figure of merit of 187.5dB and serves as a basis for designing of Q-VCO

4. Vital comparison between the BS-QVCO and P-QVCO, this helped in deducing the facts regarding operating conditions and performance. The results rectifying the claims that BS-QVCO always performs better than P-QVCO

5. Comparison between Poly-Phase based Q-VCO and the P-QVCO, this analysis further stamped the authority of P-QVCO. Poly-Phase filter does not offer the theoretically expected advantages, though working at higher frequency poly-phase oscillator can emerge as a contender for Q-VCO design

6. Design of a robust P-QVCO, which meets all the requirements under all the process corners.

7. A comparison of the present work with other notable work as presented below further stamps the usefulness, scientific viability and credibility of this thesis work

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.25um CMOS</td>
<td>0.18um CMOS</td>
<td>0.18um CMOS</td>
<td>0.25um CMOS</td>
<td>0.13um CMOS</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.5V</td>
<td>1.8V</td>
<td>1V</td>
<td>2.5</td>
<td>1.2V</td>
</tr>
<tr>
<td>Frequency</td>
<td>1.8GHz</td>
<td>5.1GHz</td>
<td>17GHz</td>
<td>4.88GHz</td>
<td>5.64GHz</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-143dBc/Hz. @3MHz offset</td>
<td>-132.6dBc/Hz. @3MHz offset</td>
<td>-110dBc/Hz. @1MHz offset</td>
<td>-125dBc/Hz. @1MHz offset</td>
<td>-115dBc/Hz. @1MHz offset</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>17%</td>
<td>17%</td>
<td>16.5%</td>
<td>13%</td>
<td>11.4%</td>
</tr>
<tr>
<td>Power</td>
<td>20mW</td>
<td>27.7mW</td>
<td>5mW</td>
<td>22mW</td>
<td>2.4mW</td>
</tr>
<tr>
<td>FOM</td>
<td>185.5dB</td>
<td>192dB</td>
<td>187.6dB</td>
<td>185dB</td>
<td>186.36dB</td>
</tr>
<tr>
<td>Phase Error</td>
<td>3 Degrees</td>
<td>N/A</td>
<td>1.4 Degrees</td>
<td>2.6 Degrees</td>
<td>0.2 Degrees</td>
</tr>
</tbody>
</table>

As stated earlier that this work comprehensively exploits and mainly builds upon the existing models and design principles in circuit design and system design simultaneously. This resulted in the form of results, which are new, publishable and credible.

### 6.2 Future Work

It is necessary as well as beneficial for the scientific community if the research done raises the question marks and opens the door for further research and/or investigation. So, does is offered by this work.

1. At system level present models can be advanced in order to exploit the use of pulse based, energy/template correlation based systems at higher frequency, preferable in open band that is 22-29 GHz. This requires new facets to be added to present wideband receiver architecture, with emphasis on low-IF architectures.
2. The system development can open door for fast digital processing near the antenna, further exploiting the role of pulse shaping and spread spectrum techniques.

3. At circuit level, a more in depth study into Q-VCO is desirable, this should not only include the quantitative aspect but provide with a comprehensive design strategy and topology for Q-VCO.

4. Possibly comparison present P-QVCO with Q-VCO realized by digital divider and VCO.

5. Exploiting the devices and topology as why $\frac{g_m}{g_d}$ ratio serves as a bottleneck, specially for regenerative oscillators in sub nano nodes.

6. A complete functional QDAcR IC.

These were a few recommendations for the future work. This work accomplished all its desirables, nw time to build up further.
References


An Oscillator System for UWB QDAcR


14. Jri Lee; Da-Wei Chiu; Nat. Taiwan Univ., Taipei, Taiwan ; A 7-band 3-8 GHz frequency synthesizer with 1 ns band-switching time in 0.18 µm CMOS technology; Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International; page 204 - 593 Vol. 1; February 2005.


An Oscillator System for UWB QDAcR


27. John R. Long et. al.; RFIC-Class Notes, Oscillator Design; March 2009.


An Oscillator System for UWB QDACR


31. T. Antal, M. Droz, G. Gyorgyi and Z. Racz; Roughness distributions for $1/f^\alpha$ signals; Physics Review E 065, 046140; April 2002.

32. Kent H. Lundberg; Noise Sources in Bulk CMOS; Published 2002.


37. Rick Poore; Phase Noise and Jitter; Agilent EEs of EDA © Agilent Technologies.

38. T. C. Weigandt, B. Kim, P. R. Gray; Analysis of Timing Jitter in CMOS ring oscillator; Proc. OF IEEE symposium on Circuits and Systems; pages 27 – 30, Published 1994.


42. Amin Q. Safarian, Ahmad Yazdi, Payam Heydar, Design and Analysis of an Ultrawide-Band Distributed CMOS Mixer; IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 13, NO. 5, MAY 2005.


48. Kamran Entesari; Development of High Performance 6-18 GHz Tunable/Switchable RF-MEMS Filters and Their System Implications; PhD Dissertation, University of Michigan; Published: 2006.


55. Tiebout, Marc; A Fully Integrated 1.3GHz VCO for GSM in 0.25µm Standard CMOS with a Phase noise of -- 142dBc/Hz at 3MHz Offset, 30th European Microwave Conference, October 2000.


An Oscillator System for UWB QDacR


An Oscillator System for UWB QDAcR


